EZ-USB™ HX2G3 Dock USB 2.0 Hi-Speed Hub

Overview

EZ-USB™ HX2G3 is a USB 2.0 hub controller with a Arm® Cortex®-M0+ CPU with, 32 KB of SRAM, and 32 KB of ROM. EZ-USB™ HX2G3 includes programmable USB 2.0 PHYs and one serial communication block (SCB) that supports I2C or SPI. It can run from firmware (FW) on ROM, or an external I2C EEPROM/ SPI flash, or downloaded from an external I2C master.

EZ-USB™ HX2G3 is available in two packages for dock applications:

- 40-QFN
- 48-QFN

Features

- USB 2.0 hub controller
  - Supports Hi-Speed (480 Mbps), Full-Speed (12 Mbps), and Low-Speed (1.5 Mbps) data rates
- Multiple port configuration options
  - One upstream port and four downstream ports (1:4)
  - One upstream port and two downstream ports (1:2)
  - Two upstream ports and four downstream ports (2:4)
  - Three upstream ports and three downstream ports (3:3)
- Integrated Arm® Cortex®-M0+ CPU
  - 32 KB RAM, 32 KB ROM
- Embedded eFuse to support trimming, VID/PID, and PHY configuration
- Optional configurable Full-Speed device function support
  - Optional CDC/billboard device class support
  - Firmware download and configuration supported through USB (CDC interface) to the I2C EEPROM/SPI flash connected externally to EZ-USB™ HX2G3
  - Firmware download and configuration supported through I2C from an external I2C master, saving BOM for external SPI flash or I2C EEPROM for boot
- Individual and ganged port power control
- Support Active and Deep Sleep power modes
- No power sequence needed
- Supports Hub cascade mode
  - Configurable option to output the reference clock for the cascaded hubs to share the source clock and save crystal cost
- Feature support for USB PD
  - Dynamic US port selection control through GPIO or EZ-USB™ HX2G3 I2C slave in 2-US/4-DS or 3-US/3-DS hub configuration
  - Configurable and integrated Billboard device class support with controllability from an external I2C master
  - Configurable hub container ID/UUID support over EZ-USB™ HX2G3 I2C slave interface
- Extensive configuration support with EZ-USB™ HX2G3 configuration utility for
  - Vendor ID (VID)/Product ID (PID), manufacturer and product string descriptors
  - Enabling or disabling the DS ports
  - Setting removable and non-removable devices
  - Number of non-removable devices
  - Ganged or individual power switch enables for downstream ports
  - Polarity selection for power enable outputs and overcurrent inputs

Features

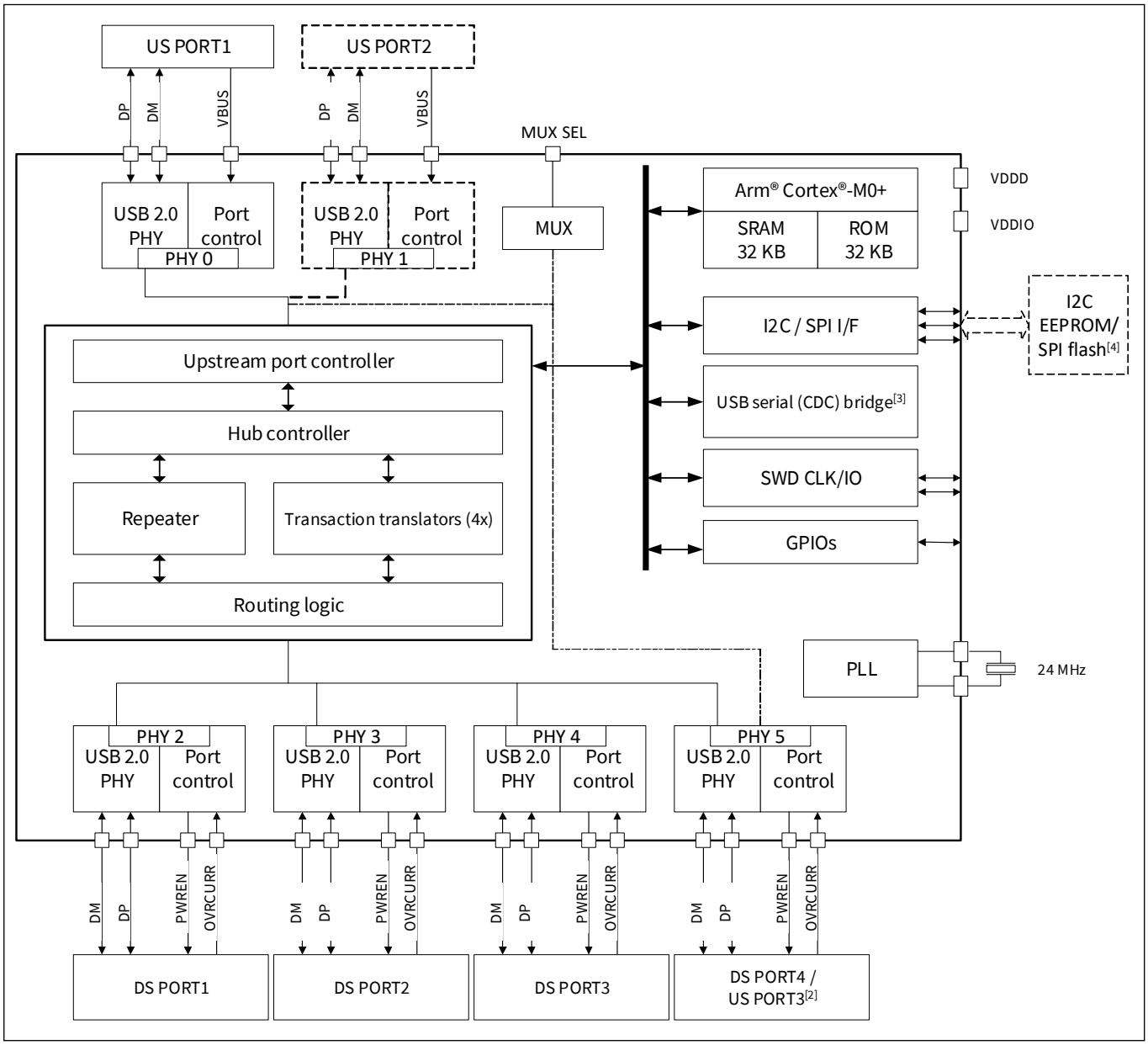
  - USB 2.0 PHY parameters
  - Swap DP/DM signals for flexible PCB routing
- Multiple boot options to load configuration and firmware
  - ROM
  - External EEPROM
  - External I2C Master
  - External SPI flash
- Available in two packages[1]
  - 40-QFN, 5×5 mm, 0.4 mm pitch (–40°C to 85°C)
  - 48-QFN, 6×6 mm, 0.4 mm pitch (–40°C to 85°C)

Notes

1. For more details on package information, see **Table 17**.

EZ-USB™ HX2G3 Block diagram

EZ-USB™ HX2G3 Block diagram



Notes

2. DS Port4 can be re-purposed as US Port3.
3. Enabling the embedded USB-serial (CDC) bridge/Billboard device will reduce the number of externally available DS ports. The CDC bridge /Billboard device will always get enumerated on DS Port1.
4. External I2C EEPROM/SPI flash is optional.

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1 EZ-USB™ HX2G3 resources

Table 1 EZ-USB™ HX2G3 resources

Resources	Description
Application notes	EZ-USB™ HX2G3 hardware design guidelines
Development kits	KIT_HX2G3_40QFN
Infineon developer community	**Infineon Developer Community** enables connection with fellow EZ-USB™ developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated Infineon Community
EZ-USB™ HX2G3 Configuration Utility	A windows desktop application that guides users through the process of configuring and programming EZ-USB™ HX2G3 devices

2 Application

2.1 USB 4 and Thunderbolt dock application

USB 4, Thunderbolt 4, and Thunderbolt 5 docks are typically self-powered or bus-powered docks with a dock management controller and PD controller(s), for managing the US and DS PD ports in the design. Thunderbolt 4/Thunderbolt 5 and USB 4 dock designs must have a USB 2 hub with an integrated USB 2 MUX feature to select the USB 2 data lines from one of the two/three possible USB 2 data ports in the design. In such applications, EZ-USB™ HX2G3 can be used in one of the two following configurations:

- 2:4 hub configuration selects USB 2 port from either Type-C connector or the USB 4/Thunderbolt controller, depending on the mode entered. In Thunderbolt mode, USB 2 lines come from the ridge/USB 4 controller. For all other modes, USB 2 lines come from the Type-C connector
- 3:3 hub configuration selects the USB 2 port from SoC/ IoT/Wi-Fi controller, where it would act as a USB host controller, in addition to the possible USB 2 data sources in 2:4 configuration

Figure 1 and **Figure 2** show how EZ-USB™ HX2G3 is used in USB 4/Thunderbolt dock application.

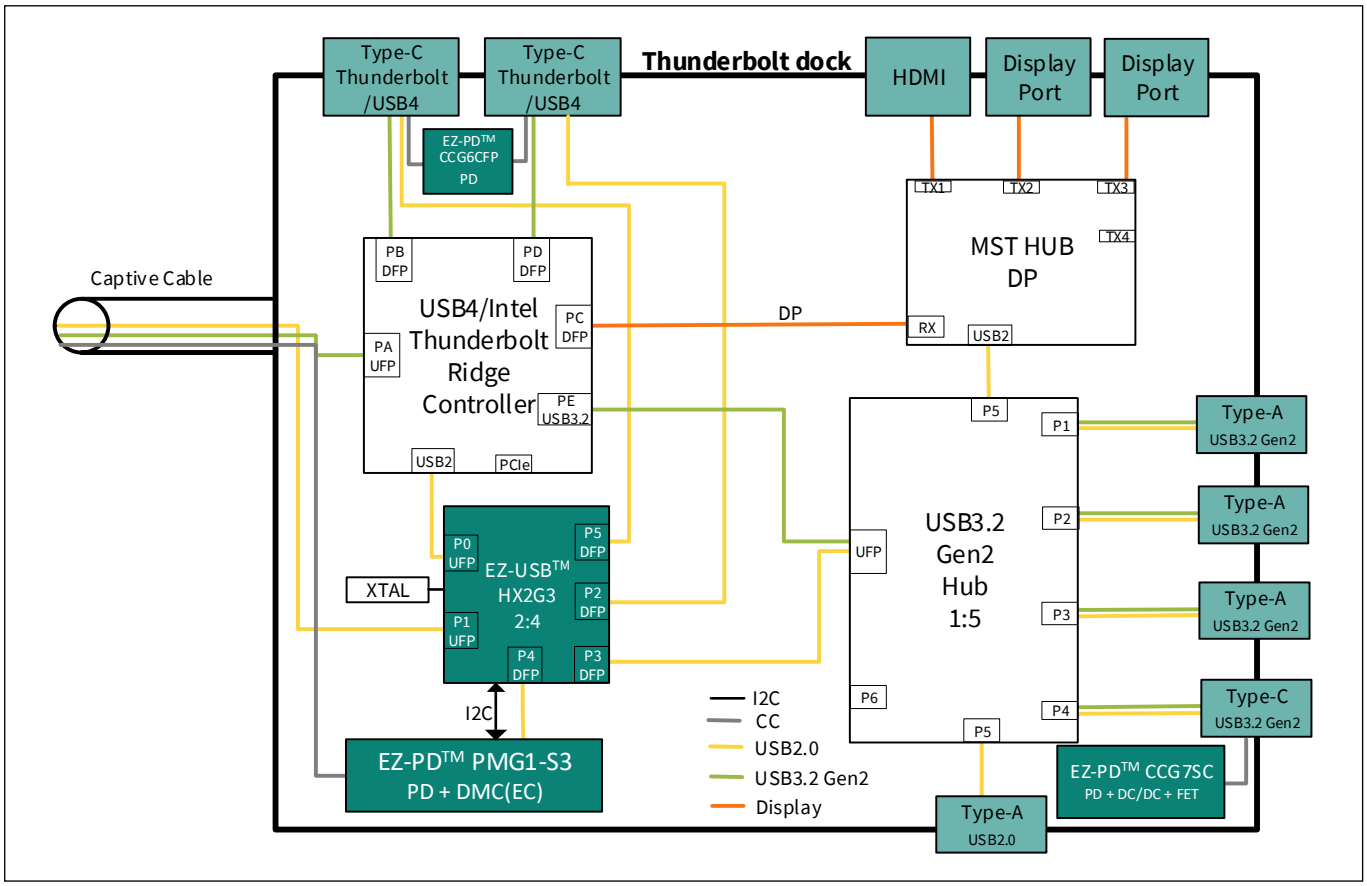


Figure 1 EZ-USB™ HX2G3 as 2:4 hub in a Thunderbolt 4, and Thunderbolt 5 dock[5, 6, 7]

Application

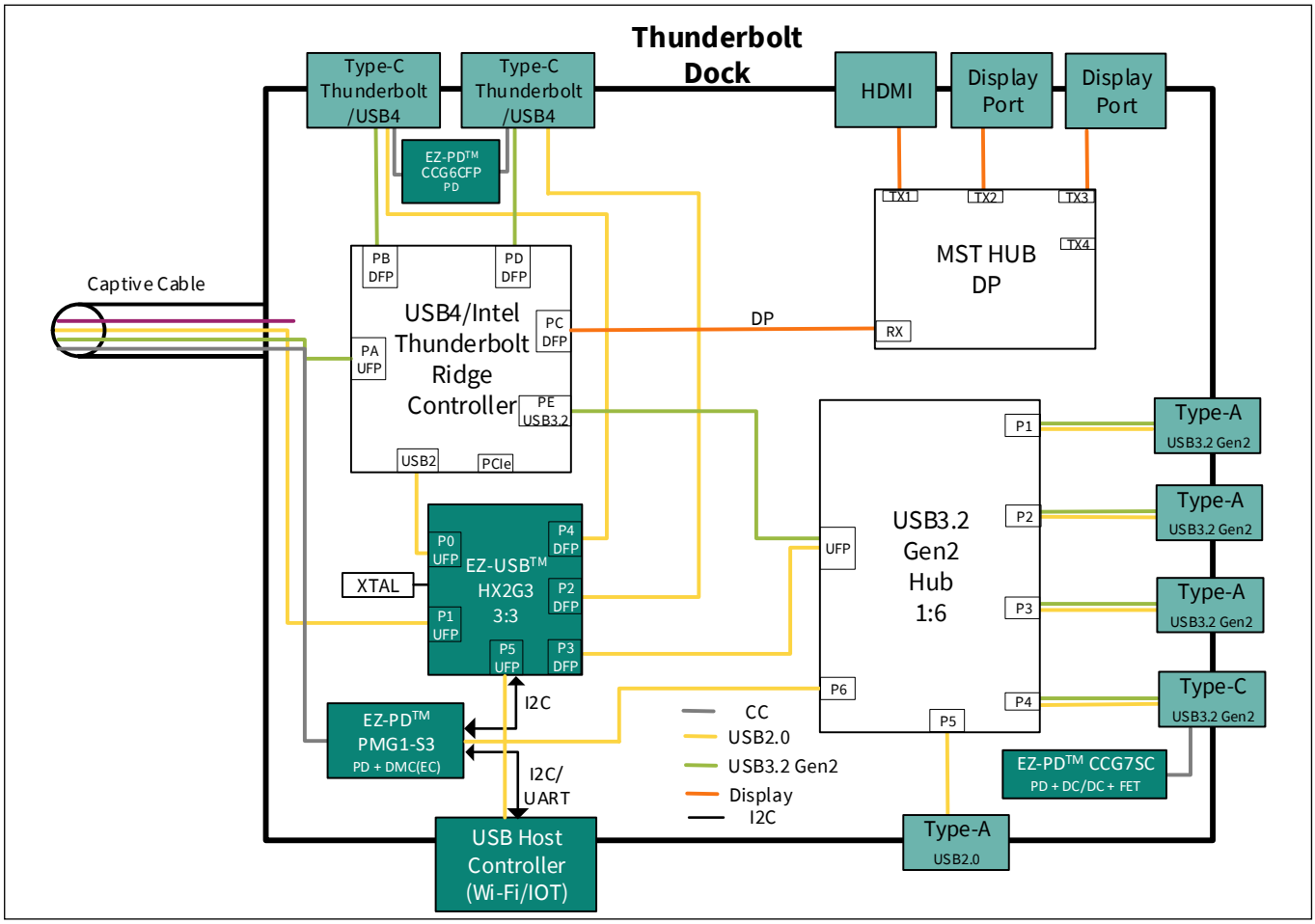


Figure 2 **EZ-USB™ HX2G3 as 3:3 hub in a USB 4, Thunderbolt 4, and Thunderbolt 5 dock, or AIO monitor[5, 6, 7]**

Notes

5. Figures are for illustrative purposes only.
6. Thunderbolt 4, Thunderbolt 5, and the Thunderbolt logo are trademarks of Intel Corporation in the U.S. and/or other countries.
7. Contact Infineon for the recommendation of PD controller.

Application

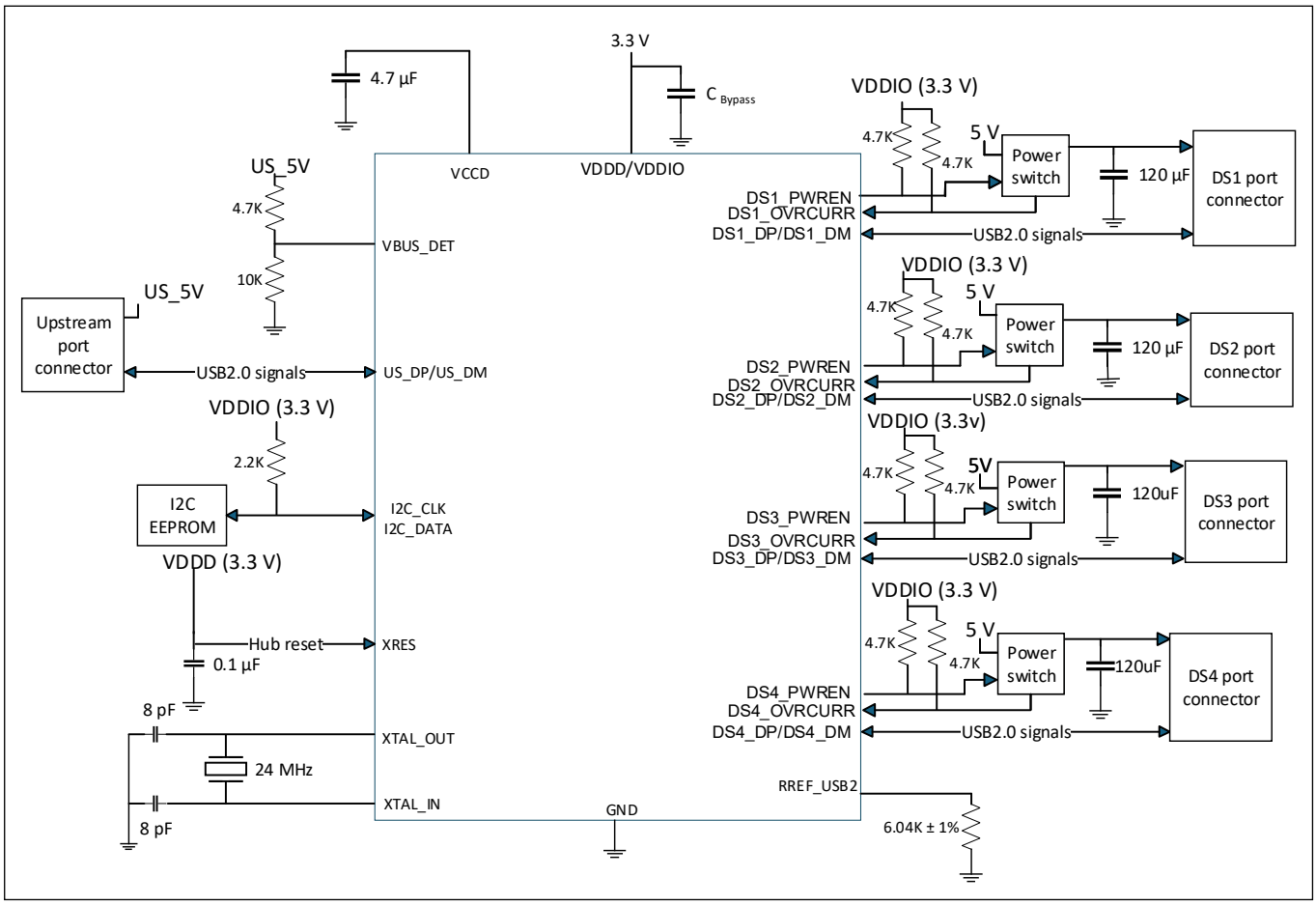


Figure 3 Generic application schematic for EZ-USB™ HX2G3

3 Product features

EZ-USB™ HX2G3 is a USB 2.0 hub controller that supports multiple downstream and upstream port configurations. It includes an optional composite full-speed (FS) device. EZ-USB™ HX2G3 includes the firmware in internal ROM to initialize the hub and can operate as a stand-alone hub controller. It can also run with FW downloaded from an external EEPROM, external I2C Master, or an external SPI.

The following sections provide an overview of the features and capabilities of the EZ-USB™ HX2G3 device.

3.1 USB 2.0 hub

The USB 2.0 hub operates as defined by the **USB 2.0 specification** and based on the configuration settings in the EEPROM or eFuse settings.

3.1.1 Upstream port

The upstream port includes an integrated 1.5 KΩ pull-up resistor and termination resistors. In docking application, there are two upstream ports and a third upstream port can be configured. See **Table 3** for possible port configurations.

3.1.1.1 Upstream port selection

EZ-USB™ HX2G3 can have up to three different upstream ports depending upon the configuration.

The number of upstreams and the upstream ports can be selected using the following two methods.

1. Using MUX selection GPIO namely: US_MUX_SEL_0 and US_MUX_SEL_1

The truth table in **Table 2** represents the US_MUX_SEL_0 and US_MUX_SEL_1 configuration with their corresponding upstream port selected.

Table 2 US_MUX_SEL pin truth table

US_MUX_SEL_1	US_MUX_SEL_0	Upstream physical port
0	0	US_DP/ US_DM
0	1	US_ALT_DP/ US_ALT_DM
1	0	US_ALT1_DP/ US_ALT1_DM
1	1	US_DP/ US_DM

For changing the MUX during runtime, carry out the following sequence after setting the “VbusDetectEnable” parameter in the configuration table.

1. Assert VBUS_DET pin to LOW (depending on the polarity)
2. Change the MUX selection GPIO pins (US_MUX_SEL_0 and US_MUX_SEL_1)
3. Assert VBUS_DET pin to HIGH (depending on the polarity)

2. Using I2C Slave register configuration

I2C Slave register configuration can be used to select the upstream port. By configuring the register address 0xF00C, desired UFP and DFP configurations can be achieved. The external MUX selection GPIO pin configuration can be overridden by configuring the register address 0xF018. See **Table 2** for all possible combinations. For more information, see **“I2C Slave register space”** on page 28.

3.1.2 Downstream port

Downstream ports are compliant to USB 2.0 specification and has integrated 15-KΩ pull-down and termination resistors. The ports are disabled or enabled using configuration options through external I2C EEPROM or eFuse.

Note that enabling FS device in EZ-USB™ HX2G3 will reduce the number of DS ports independently. For example, if FS device is enabled with hub in 2:4 configuration, number of DS ports will be reduced to three. FS device is enabled by default for every dock part. For more information, see **Table 3**.

Table 3 Downstream ports

EZ-USB™ HX2G3 configuration	Number of US ports available	Number of DS ports available	
		Without FS device enabled	With FS device enabled
1:4	1	4	3
2:4	2	4	3
3:3	3	3	2

Table 4 Comparison of downstream and upstream port configurations

Product	Number of DS ports		Number of US ports
	With FS device enabled	With FS device disabled	
CYUSB2343-40LTXI	3 (default)	4	1 (default)
	3	4	2
	2	3	3
CYUSB2344-48BFXI	3	4	1
	3 (default)	4	2 (default)
	2	3	3
CYUSB2345-48BFXI	3	4	1
	3	4	2
	2 (default)	3	3 (default)

3.2 Power management

EZ-USB™ HX2G3 internally implements control signaling for external power switching. The initial conditions of these signals are in disabled state in order to reduce inrush currents.

EZ-USB™ HX2G3 provides Active, Deep Sleep, and Reset modes to control power consumption at different operational states. The core logic operates at 1.1 V (LP). In conjunction with clock gating at peripheral and bus levels, this permits fine-grained optimization of energy usage over system life. The application ROM code will transition the chip to appropriate power states based on the repeater state.

3.3 CPU

The CPU supports initialization and power mode transitions. It is a single-core subsystem consisting of a 60-MHz Arm® Cortex®-M0+.

3.4 Clocking

The system clock has the following parameter:

- 24 MHz crystal input
- 24 MHz external clock

In case of external oscillator, connect the output of the oscillator to XTAL IN, while XTAL OUT is NC.
The following are the recommended crystal parts:

- ECS-240-8-36CKM-TR (manufacturer: ECS)
- ABM10 W-24.0000 MHZ-6-B1U-T3 (manufacturer: Abracon)

The following is the recommended oscillator part:

- ECS-2520MV-240-DN-TR (manufacturer: ECS)

See **Table 5** for crystal/clock specification.

Table 5 XTAL/clock specification

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
EXT_CRY_RES_FREQ	External crystal resonator frequency	–	24	–	MHz	Resonator reference clock frequency. Fundamental oscillation mode.
EXT_CRY_RES_FREQ_TOL	External crystal resonator frequency tolerance	–30	–	30	ppm	Resonator reference clock frequency
EXT_CRY_RES_CLOAD	External crystal resonator load capacitance	–	9.5	–	pF	PCB load
EXT_CRY_RES_CSHUNT	External crystal resonator shunt capacitance	–	0.4	1	pF	No ground connection
EXT_CRY_RESCMOTIONAL	External crystal resonator motional capacitance	–	–	3	pF	No ground connection
EXT_CRY_RES_ESR	External crystal resonator ESR	–	–	60	Ω	Equivalent value resistance
EXT_CRY_RES_PDRIVE	Drive level for external crystal oscillator	–	50	200	µW	Resonator drive level
EXT_CRY_RES_START	External crystal resonator start-up time	–	–	1.6	ms	Maximum start-up time required by resonator to meet the USB 2.0 timing requirements.

3.5 Communication interfaces (I2C or SPI)

The communication interface bus is a part of serial communication block (SCB) that is controlled by the bootloader and is one of the optional methods for initializing the hub. It follows the I2C bus specification or SPI interface. This SCB can be configured as any of the below:

1. **I2C master:** This is used when the EZ-USB™ HX2G3 is loaded with an external Configuration/FW from an I2C EEPROM or any I2C Slave device
2. **I2C slave:** In this case external I2C master can write the Configuration/FW to the SRAM of the EZ-USB™ HX2G3, and EZ-USB™ HX2G3 shall boot with the new Configuration/FW
3. **SPI master:** EZ-USB™ HX2G3 boots from the Configuration/FW from the external SPI flash

See **EZ-USB™ HX2G3 Boot flow to load configuration/firmware**.

3.6 Full-Speed device

The embedded USB Serial device controller is internally connected to DS1 downstream port of the EZ-USB™ HX2G3 hub. This is used for programming the configuration/FW into the external memory devices connected to the HX2G3 hub over I2C or SPI. FS device is enabled by default for every dock part.

3.7 Boot options

EZ-USB™ HX2G3 is integrated with ROM that contains FW, including Bootloader code, hub controller code, and the default configurations to ensure that EZ-USB™ HX2G3 is able to work as a standalone hub. The CPU executes the ROM code to boot up the device, load configurations, and execute the FW to control GPIOs and enable downstream power. HX2G3 can boot from external devices as well as defined below.

3.7.1 EZ-USB™ HX2G3 Boot flow to load configuration/firmware

EZ-USB™ HX2G3 provides multiple options to load configuration and firmware that includes accessing EEPROM, PD-Controller, SPI flash or default option as ROM. To select source for the configuration and firmware, there are four possibilities:

- EZ-USB™ HX2G3 SCB configured in I2C master mode
  - In this mode, the EZ-USB™ HX2G3 bootloader looks for a slave device such as EEPROM. If the device is found, the EZ-USB™ HX2G3 downloads the configuration, firmware, or both from the slave device and initiates the rest of the initialization from the newly downloaded firmware stored in RAM. If the image in the slave device is corrupted, the EZ-USB™ HX2G3 ignores this image and boot from ROM, which holds the default firmware and configuration
- EZ-USB™ HX2G3 SCB configured in I2C slave mode
  - In this mode, the EZ-USB™ HX2G3 bootloader waits for an external I2C master (e.g., PD controller) to download the configuration, firmware, or both into the EZ-USB™ HX2G3 within a given configuration time. If the image is corrupted, the EZ-USB™ HX2G3 ignores this image and boots from ROM
- EZ-USB™ HX2G3 SCB configured in SPI master mode
  - In this mode, the EZ-USB™ HX2G3 bootloader looks for a flash device. If the flash device is found, the EZ-USB™ HX2G3 downloads the configuration, firmware, or both from the flash device and initiates the rest of the initialization from the newly downloaded firmware stored in RAM. If the image in the SPI flash device is corrupted, the EZ-USB™ HX2G3 ignores this image and boot from ROM
- ROM as source for configuration and firmware
  - If the firmware is not available from any external device, ROM is the last option the EZ-USB™ HX2G3 bootloader looks for available configuration and firmware. The rest of the system is initialized from the firmware that is available in the ROM

Figure 4 shows the overall flow of the boot sequence.

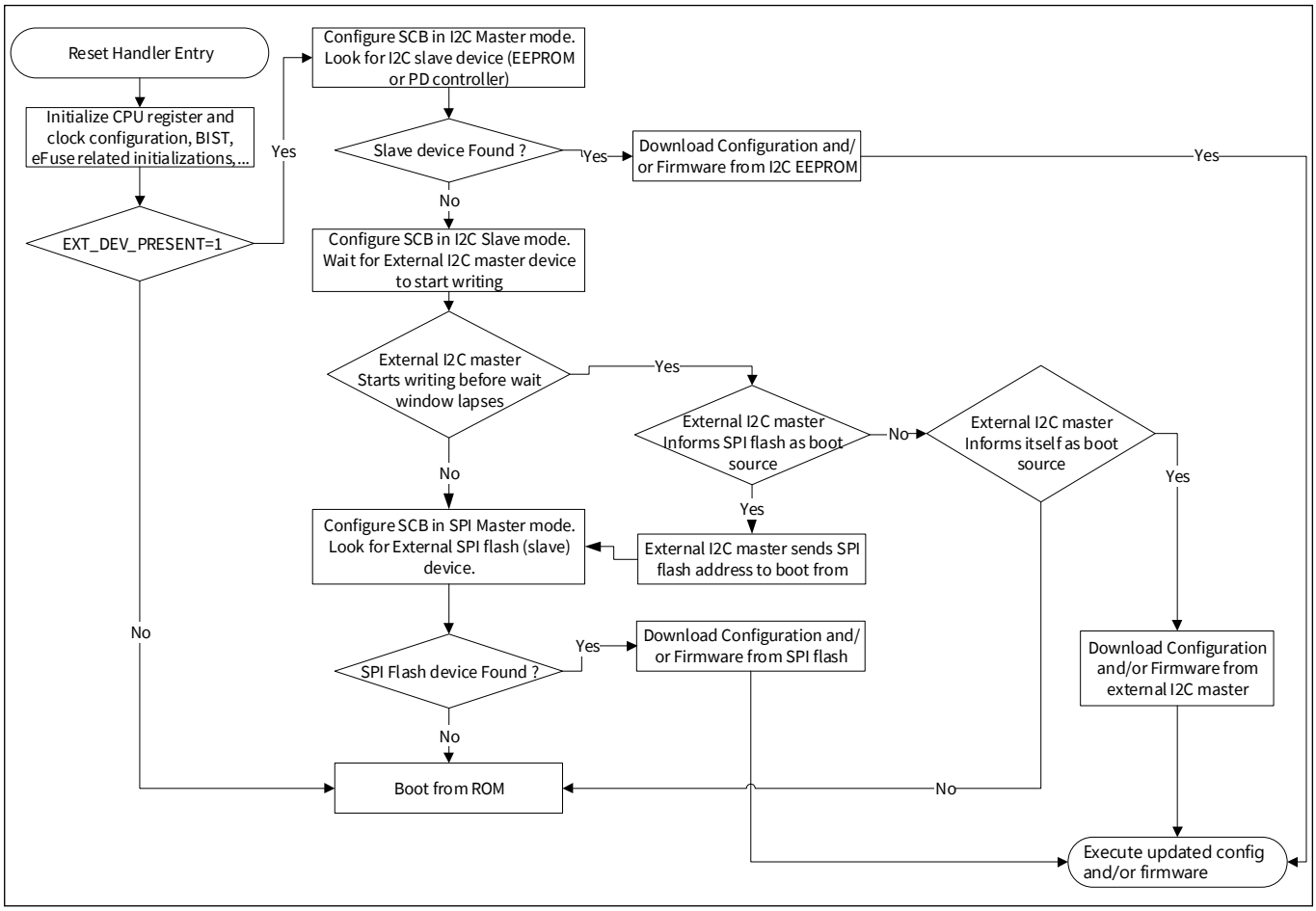


Figure 4 Boot flow[8]

Note

8. EXT_DEV_PRESENT – 'External device is present' is set in order to boot in I2C master mode, SPI master mode or I2C slave mode.

3.8 EZ-USB™ HX2G3 configuration

EZ-USB™ HX2G3 can be configured using one of the following:

- External I2C master
- External I2C slave such as an EEPROM
- External SPI flash

On top of static configuration, EZ-USB™ HX2G3 also offers an I2C slave interface in the application firmware for reading status and some level of dynamic configuration.

For more details, see the **Configuration utility.**

3.8.1 Configuration table structure

Note: To modify the PHY CONFIG parameters, contact **Infineon local support**.

Table 6 Parameter configuration table

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
Header	0	7:0	bSignature LSB (“C”)	The first byte of the 2-byte signature initialized with “CY” ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device.	0x43	0x43	0x43
	1	7:0	bSignature MSB (“Y”)	The second byte of the 2-byte signature initialized with “CY” ASCII text. When the signature is not valid, the hub enumerates as a vendor-specific device.	0x59	0x59	0x59
	2	7:0	bImageCTL	Bits 3:0 ==> 0 Bits 5:4 ==> I2C clock frequency (0: 1 MHz, 1: 400 KHz, 2: 100 KHz, 3: 100 KHz) Bits 7:6 ==> SPI clock frequency (0: 10 MHz, 1: 7.5 MHz, 2: 5 MHz, 3: 1 MHz)	0x00	0x00	0x00
	3	7:0	bImageType	0xD4: Load only configuration 0xB0: Load firmware boot image All other bImageType will return an error code	0xD4	0xD4	0xD4
	4	7:0	wTableLength LSB	Lower byte of the length of the config table in bytes	–	–	–
	5	7:0	wTableLength MSB	Upper byte of the length of the config table in bytes	–	–	–
	6	7:0	wChecksum LSB	LSB of checksum calculated over bytes 8 to N of the config table	–	–	–
	7	7:0	wChecksum MSB	MSB of checksum calculated over bytes 8 to N of the config table	–	–	–
Hub config	8	7	I2CSlaveEnable	Enables I2C slave interface once application has booted up. 0: I2C slave mode disabled 1: I2C slave mode enabled	1	1	1
		6:0	I2CSlaveAddr	I2C slave address (7-bit) to be used when Hub application is running	0x38	0x38	0x38
	9	7:6	Reserved	Reserved	–	–	–
		5	MuxCtrlPinEnable	Enables US_MUX_SEL_1 and US_MUX_SEL_0 pin functions to select upstream port If UpstreamPortCount is 1, US_MUX_SEL is not useful. If UpstreamPortCount is 2, US_MUX_SEL_0 is used to select US port. 0 -> Port0, 1 -> Port1 If UpstreamPortCount is 3, US_MUX_SEL_1/0 are used to select USB port. 00 -> Port0, 01 -> Port1, 10 -> Port5, 11 -> Port0	1	–	1

Table 6 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
Hub config	9	4	MuxCtrlPinSelect	Selects pins used as US_MUX_SEL_1/0: 0: US_MUX_SEL_1 pin and is US_MUX_SEL_0 pin (CYUSB2344 and CYSUB 2345) 1: DS4_OVRCURR/SPI_MISO/US_MUX_SEL_1 pin and DS4_OVRCURR/SPI_MISO/US_MUX_SEL_0 pin (CYUSB2343)	0	1	0
		3	singleTTEnable	0: Multi-TT hub 1: Single-TT hub	0	0	0
		2	compoundDevice	gives information about presence of FS device. 0: FS device not present 1: FS device present	1	1	1
		1:0	FSDevFunc	Select USBFS device function on DS1 port: 0: No function 1: CDC Serial bridge function enabled 2: Billboard function enabled 3: Both CDC serial bridge and billboard enabled	1	1	1
	10	7:4	REMOVABLE_PORTS [3:0]	Indicates if the port is removable. bit[7:4]=DS4, DS3, DS2, DS1 0: Non-removable 1: Removable	0xE	0xE	0x6
		3:0	PORT_PRESENT[3:0]	Indicates if a USB 2.0 port is active. bit[3:0]=DS4, DS3, DS2, DS1 0: Not active 1: Active	0xF	0xF	0x7
	11	7	GANG_PWR_EN	Whether hub uses ganged power switching	0	1	0
		6	BUS_POWER	Whether the hub is bus powered	0	0	0
		5:2	PWR_EN_POLARITY[3:0]	POWER ENABLE polarity for the DS ports (DS4, DS3, DS2, DS1): 0: Power enable signals are active LOW 1: Power enable signals are active HIGH	0	0	0
		1	OC_SUPPORT_DISABLE	Whether OverCurrent notifications are disabled for DS ports	0	0	0
		0	INDIVIDUAL_OC	0: Global over-current protection is supported 1: Individual port over-current protection is supported	1	1	1
	12	7:4	OC_POLARITY[3:0]	Over Current Polarity for all DS ports (DS4, DS3, DS2, DS1): 0: OC indicators are active LOW 1: OC indicators are active HIGH	0	0	0
		3	fwAvailable	Firmware is available and should be downloaded from external device: 0: Firmware Not available 1: Firmware available	0	0	0
		2:1	Reserved	Reserved	–	–	–

Table 6 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
Hub config	12	0	pwrSwSupport	Power Switch Support: 0:Power switching not supported by HUB 1: Power switching supported by HUB	1	1	1
	13	7:5	UFP_CONFIG	These three bits are used to decide UFP config: 001: 1UFP + 4DFP 010: 2UFP + 4DFP 100: 3UFP +3DFP 101: 1UFP + 3DFP	2	2	4
		4:3	Reserved	Reserved	–	–	–
		2	BootModePinEnable	Whether BOOT_MODE indicator pin function is enabled: 0: No BOOT_MODE indication 1: SWDDIO/I2C_ARB pin (CYUSB2344 and CYUSB2345) or SWDDIO/SPI_CS/I2C_ARB pin (CYUSB2343) will be driven high until boot as HX2G3 I2C slave is complete	1	1	1
		1	IgnoreStringDescriptors	0: String descriptors will be updated based on values from config table 1: String descriptors as pre-defined by ROM will be used	0	0	0
		0	IgnorePhyConfig	0: PHY config registers will be updated based on values from config table 1: PHY config registers will be programmed based on eFUSE contents	1	1	1
	14	7:0	HUB_VID[7:0]	Custom Vendor ID - LSB	0xB4	0xB4	0xB4
	15	7:0	HUB_VID [15:8]	Custom Vendor ID - MSB	0x04	0x04	0x04
	16	7:0	HUB_PID [7:0]	Custom Product ID (PID) Default: 0x6560 Different PID values for different product numbers	0x12	0x12	0x14
	17	7:0	HUB_PID [15:8]	–	0x65	0x65	0x65
	18	7:0	DID [7:0]	LSB of bcdDevice field in Device Descriptor. Represents Silicon/ROM revision information B7:4 -> Major Revision B3:0 -> Minor Revision	0x0A	0x0A	0x0A
	19	7:0	DID [15:8]	MSB of bcdDevice field in Device Descriptor. Represents application firmware version when present.	0x50	0x50	0x50
	20	7:0	MAX_POWER	USB Descriptor specific. bMaxPower -> Configuration Descriptor	0x32	0x32	0x32
	21	7:0	MAX_CURRENT	USB Descriptor specific bMHubContrCurrent -> Hub Descriptor	0x64	0x64	0x64
	22	7:0	powerGoodTime	Time (in 2-ms intervals) from the time the power-on sequence begins on a port until power is good on that port (bPwron2PwrGood)	0x32	0x32	0x32
	23	7	PllRefClockSel	0: Use ECO to obtain 24 MHz reference clock for the PLL 1: Use external clock input as reference clock for the PLL	0	0	0

Table 6 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
Hub config	23	6:4	SuspPinFunction	Select functionality of SUSPEND pin 0: No function 1: Connect to clk_eco (24 MHz) output for cascaded hubs 2: Indication of upstream suspend (L2) state: Active LOW 3: Indication of upstream suspend (L2) state: Active HIGH 4: Use as external power present indicator input (active LOW) 5: Use as external power present indicator input (active HIGH) 6: Reserved 7: Reserved	3	3	3
		3	VbusDetectEnable	Whether Vbus detection function is enabled: 0: Vbus detection is disabled 1: Vbus detection function is enabled on VBUS_DETECT_IO pin	1	1	1
		2	VbusDetectPolarity	Selects polarity of VBUS_DETECT_IO input pin: 0: Active LOW 1: Active HIGH	1	1	1
		1	LedIndicationEnable	Whether per-DS port LED indication is enabled.	0	0	0
		0	LedIndicatorPolarity	0: LED glows when IO is driven LOW 1: LED glows when IO is driven HIGH	0	0	0
	27:24	31:0	USB2EXTATTR	Bit map encoding of supported device level features (Refer USB 2.0 ECN Errata for LPM) Bit 0 - Reserved. Must be zero Bit 1 - LPM. A value of one in this bit location indicates that this device supports LPM Bit 2 - BESL & Alternate HIRD definitions supported. The LPM bit must be set to a one when this bit is one Bit 3 - Recommended Baseline BESL valid Bit 4 - Recommended Deep BESL valid Bit 11:8 - Recommended Baseline BESL value. Field shall be ignored by system software if bit[3] is a zero Bit 15:12 - Recommended Deep BESL value. Field shall be ignored by system software if bit[4] is zero Bit 31:16 - Reserved. Must be set to zero.	0x0006	0x0006	0x0006
	29:28	15:0	bcdUSB	bcdUSB -> Device Descriptor	0x210	0x210	0x210
	30	7:0	iMANUFACTURER	Offset of Hub Manufacturer string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	31	7:0	iPRODUCT	Offset of Hub product string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	32	7:0	iSERIAL_NUM	Offset of Serial Number string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	33	7:0	iCFG_HS	Offset of HS configuration string descriptor stored in variable part of configuration table	0x00	0x00	0x00

Table 6 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
Hub config	34	7:0	iCFG_FS	Offset of FS configuration string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	35	7:0	iINTF_FS	Offset of FS interface string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	36	7:0	iINTF_HS_AS0	Offset of HS alt setting 0 string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	37	7:0	iINTF_HS_AS1	Offset of HS alt setting 1 string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	38	7:4	OC_TIMER	Time in milliseconds for which the overcurrent inputs will be filtered	8	8	8
		3	I2cIntrDisable	Disable support for I2C_INT pin: 1: I2C_INT function is not supported 0: I2C_INT function is supported	0	0	0
		2	I2cIntrPinSelect	Select pin used for I2C_INT function: 0: I2C_INT pin is used 1: SWDDIO/I2C_ARB pin (CYUSB2344 and CYUSB2345 only) is used	0	0	0
		1	I2cIntrConfig	Configuration for I2C_INT pin: 0: Active low with internal pull-up enabled 1: Active low in open drain mode	1	1	1
		0	I2CArbitrationEnable	Whether I2C_INT pin should be used for I2C access arbitration with PD controller.	0	0	0
	39	7	SpiMasterEnable	Whether SPI interface is supported on this part	1	0	1
		6	SpiBootConfigEnable	Whether bootloader should wait for I2C based config update before attempting to boot from SPI flash	1	0	1
		5:4	SpiSsnPinSelect	Select pin to be used for SPI_CS function: 0: SPI_CS pin (CYUSB2344 and CYUSB2345 only) 1: DS4_PWREN/SPI_CS pin (CYUSB2343 only) 2: SWDDIO/SPI_CS/I2C_ARB pin (CYUSB2343 only) 3: Invalid	0	2	0
		3:2	SpiClkPinSelect	Select pin to be used for SPI_CLK function: 0: SPI_CLK pin (CYUSB2344 and CYUSB2345 only) 1: DS3_PWREN/SPI_CLK pin (CYUSB2343 and CYUSB2345 only) 2:VBUS_DET_IO/SPI_CLK (CYUSB2343 only) 3: Invalid	0	1	0
UUID	55:40	1	DieSpecificUUIDEnable	Enable generation of die specific UUID (Container ID) for both Hub and USBFS device	1	1	1
		0	DieSpecificSerialNumber Enable	Enable generation of die specific Serial Number string for the hub	1	1	1
		127:0	UUID (Container ID)	Unique serial number to be used Container IDs/UUIDs. When provided as part of boot, will provide the default values to be used. Bytes 2 to 15 can be over-ridden with die specific values generated by ROM based on DieSpecificUUIDEnable setting. When config table is read after application is running, will reflect the UUID actually in use (with generated bytes)	Die ID	Die ID	Die ID
PHY0 CONFIG (US port 1)	56	7:4	PHY0_HS_TX_AMPLITUDE	HS driver amplitude control	5	5	5
		3:2	PHY0_HS_N_PRE_ DRIVER_SEL	HS NMOS pre-driver skew	0	0	0
		1:0	PHY0_HS_P_PRE_ DRIVER_SEL	HS PMOS pre-driver skew	0	0	0

Table 6 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
PHY0 CONFIG (US port 1)	57	7	PHY0_EN_LANE_SWAP	The DP/DN pins are swapped on both the transmit and receive direction. 0: disabled 1: enabled	0	0	0
		6	PHY0_HS_TED_LP_MODE	HS TED low power mode 0: Normal operation 1: Reduced current mode	0	0	0
		5:3	PHY0_HS_DRIVER_ FINE_SLEW_SEL	HS driver fine slew rate control	0	0	0
		2:0	PHY0_HS_TX_PRE_ EMPHASIS	HS driver pre-emphasis amplitude	4	4	4
	58	7:6	PHY0_FS_DRIVER_SR_ SEL_1	FS driver slew rate control	0	0	0
		5:3	PHY0_FS_TRIGGER_ VOLTAGE	FS receiver trigger voltage control	0	0	0
		2:0	PHY0_HS_CTLE	HS receiver CTLE control	0	0	0
	59	7	PHY0_DIS_PRE_ EMPHASIS_HS_SOF	Setting this bit to '1' disables the PRE_EMPHASIS during the EOP of an SOF packet. BIT_TIME_DIS_PRE_EMPHASIS determines the bit position at which the pre-emphasis is disabled.	0	0	0
		6:5	PHY0_HS_TX- _PRE_EMP_DURATION	Selects pre-emphasis phase 0: Pre-emphasis disabled 1: pll phase 2 2: pll phase 4 3: pll phase 6	2	2	2
		4	PHY0_HS_TED_25_MODE	HS Squelch VDDD selection bit 1: VDDD = 3.3 V range (**do not use this setting for normal operation**) 0: VDDD = 1.8 V range	0	0	0
		3:2	PHY0_LS_DRIVER_SR_SEL	FS driver slew rate control	0	0	0
		1:0	PHY0_FS_DRIVER_ SR_SEL_2	FS driver slew rate control	0	0	0

Table 6 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
PHY1 CONFIG (US port 2)	60	7:4	PHY1_HS_TX_AMPLITUDE	HS driver amplitude control	5	5	5
		3:2	PHY1_HS_N_PRE_ DRIVER_SEL	HS NMOS pre-driver skew	0	0	0
		1:0	PHY1_HS_P_PRE_ DRIVER_SEL	HS PMOS pre-driver skew	0	0	0
	61	7	PHY1_EN_LANE_SWAP	The DP/DN pins are swapped on both the transmit and receive direction.	0	0	0
		6	PHY1_HS_TED_LP_MODE	HS TED low power mode 0: Normal operation 1: Reduced current mode	0	0	0
		5:3	PHY1_HS_DRIVER_ FINE_SLEW_SEL	HS driver fine slew rate control	0	0	0
		2:0	PHY1_HS_TX_PRE_ EMPHASIS	HS driver pre-emphasis amplitude	4	4	4
	62	7:6	PHY1_FS_DRIVER_ SR_SEL_1	FS driver slew rate control	0	0	0
		5:3	PHY1_FS_TRIGGER_ VOLTAGE	FS receiver trigger voltage control	0	0	0
		2:0	PHY1_HS_CTLE	HS receiver CTLE control	0	0	0
	63	7	PHY1_DIS_PRE_EM-PHASIS_ HS_SOF	Setting this bit to '1' disables the PRE_EMPHASIS during the EOP of an SOF packet. BIT_TIME_DIS_PRE_EMPHASIS determines the bit position at which the pre-emphasis is disabled.	0	0	0
		6:5	PHY1_HS_TX_PRE_ EMP_DURATION	Selects pre-emphasis phase 0: Pre-emphasis disabled 1: pll phase 2 2: pll phase 4 3: pll phase 6	2	2	2
		4	PHY1_HS_TED_25_MODE	HS Squelch VDDD selection bit 1: VDDD = 3.3 V range (**do not use this setting for normal operation**) 0: VDDD = 1.8 V range	0	0	0
		3:2	PHY1_LS_DRIVER_SR_SEL	FS driver slew rate control	0	0	0
		1:0	PHY1_FS_DRIVER_ SR_SEL_2	FS driver slew rate control	0	0	0

Table 6 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
PHY2 CONFIG (DS port 1)	64	7:4	PHY2_HS_TX_AMPLITUDE	HS driver amplitude control	5	5	5
		3:2	PHY2_HS_N_PRE_ DRIVER_SEL	HS NMOS pre-driver skew	0	0	0
		1:0	PHY2_HS_P_PRE_ DRIVER_SEL	HS PMOS pre-driver skew	0	0	0
	65	7	PHY2_EN_LANE_SWAP	The DP/DN pins are swapped on both the transmit and receive direction.	0	0	0
		6	PHY2_HS_TED_LP_MODE	HS TED low power mode 0: Normal operation 1: Reduced current mode	0	0	0
		5:3	PHY2_HS_DRIVER_ FINE_SLEW_SEL	HS driver fine slew rate control	0	0	0
		2:0	PHY2_HS_TX_PRE_ EMPHASIS	HS driver pre-emphasis amplitude	4	4	4
	66	7:6	PHY2_FS_DRIVER_ SR_SEL_1	FS driver slew rate control	0	0	0
		5:3	PHY2_FS_TRIGGER_ VOLTAGE	FS receiver trigger voltage control	0	0	0
		2:0	PHY2_HS_CTLE	HS receiver CTLE control	0	0	0
	67	7	PHY2_DIS_PRE_ EMPHASIS_HS_SOF	Setting this bit to '1' disables the PRE_EMPHASIS during the EOP of an SOF packet. BIT_TIME_DIS_PRE_EMPHASIS determines the bit position at which the pre-emphasis is disabled.	0	0	0
		6:5	PHY2_HS_TX_PRE_ EMP_DURATION	Selects pre-emphasis phase 0: Pre-emphasis disabled 1: pll phase 2 2: pll phase 4 3: pll phase 6	2	2	2
		4	PHY2_HS_TED_25_MODE	HS Squelch VDDD selection bit 1: VDDD = 3.3 V range (**do not use this setting for normal operation**) 0: VDDD = 1.8 V range	0	0	0
		3:2	PHY2_LS_DRIVER_SR_SEL	FS driver slew rate control	0	0	0
		1:0	PHY2_FS_DRIVER_ SR_SEL_2	FS driver slew rate control	0	0	0

Table 6 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
PHY3 CONFIG (DS port 2)	68	7:4	PHY3_HS_TX_AMPLITUDE	HS driver amplitude control	5	5	5
		3:2	PHY3_HS_N_PRE_ DRIVER_SEL	HS NMOS pre-driver skew	0	0	0
		1:0	PHY3_HS_P_PRE_ DRIVER_SEL	HS PMOS pre-driver skew	0	0	0
	69	7	PHY3_EN_LANE_SWAP	The DP/DN pins are swapped on both the transmit and receive direction.	0	0	0
		6	PHY3_HS_TED_LP_MODE	HS TED low power mode 0: Normal operation 1: Reduced current mode	0	0	0
		5:3	PHY3_HS_DRIVER_ FINE_SLEW_SEL	HS driver fine slew rate control	0	0	0
		2:0	PHY3_HS_TX_PRE_ EMPHASIS	HS driver pre-emphasis amplitude	4	4	4
	70	7:6	PHY3_FS_DRIVER_ SR_SEL_1	FS driver slew rate control	0	0	0
		5:3	PHY3_FS_TRIGGER_ VOLTAGE	FS receiver trigger voltage control	0	0	0
		2:0	PHY3_HS_CTLE	HS receiver CTLE control	0	0	0
	71	7	PHY3_DIS_PRE_ EMPHASIS_HS_SOF	Setting this bit to '1' disables the PRE_EMPHASIS during the EOP of an SOF packet. BIT_TIME_DIS_PRE_EMPHASIS determines the bit position at which the pre-emphasis is disabled.	0	0	0
		6:5	PHY3_HS_TX_PRE_ EMP_DURATION	Selects pre-emphasis phase 0: Pre-emphasis disabled 1: pll phase 2 2: pll phase 4 3: pll phase 6	2	2	2
		4	PHY3_HS_TED_25_MODE	HS Squelch VDDD selection bit 1: VDDD = 3.3 V range (**do not use this setting for normal operation**) 0: VDDD = 1.8 V range	0	0	0
		3:2	PHY3_LS_DRIVER_SR_SEL	FS driver slew rate control	0	0	0
		1:0	PHY3_FS_DRIVER_ SR_SEL_2	FS driver slew rate control	0	0	0

Table 6 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
PHY4 CONFIG (DS port 3)	72	7:4	PHY4_HS_TX_AMPLITUDE	HS driver amplitude control	5	5	5
		3:2	PHY4_HS_N_PRE_ DRIVER_SEL	HS NMOS pre-driver skew	0	0	0
		1:0	PHY4_HS_P_PRE_ DRIVER_SEL	HS PMOS pre-driver skew	0	0	0
	73	7	PHY4_EN_LANE_SWAP	The DP/DN pins are swapped on both the transmit and receive direction.	1	0	1
		6	PHY4_HS_TED_LP_MODE	HS TED low power mode 0: Normal operation 1: Reduced current mode	0	0	0
		5:3	PHY4_HS_DRIVER_ FINE_SLEW_SEL	HS driver fine slew rate control	0	0	0
		2:0	PHY4_HS_TX_PRE_ EMPHASIS	HS driver pre-emphasis amplitude	4	4	4
	74	7:6	PHY4_FS_DRIVER_ SR_SEL_1	FS driver slew rate control	0	0	0
		5:3	PHY4_FS_TRIGGER_ VOLTAGE	FS receiver trigger voltage control	0	0	0
		2:0	PHY4_HS_CTLE	HS receiver CTLE control	0	0	0
	75	7	PHY4_DIS_PRE_EM-PHASIS_ HS_SOF	Setting this bit to '1' disables the PRE_EMPHASIS during the EOP of an SOF packet. BIT_TIME_DIS_PRE_EMPHASIS determines the bit position at which the pre-emphasis is disabled.	0	0	0
		6:5	PHY4_HS_TX_PRE_EMP_ DURATION	Selects pre-emphasis phase 0: Pre-emphasis disabled 1: pll phase 2 2: pll phase 4 3: pll phase 6	2	2	2
		4	PHY4_HS_TED_25_MODE	HS Squelch VDDD selection bit 1: VDDD = 3.3 V range (**do not use this setting for normal operation**) 0: VDDD = 1.8 V range	0	0	0
		3:2	PHY4_LS_DRIVER_SR_SEL	FS driver slew rate control	0	0	0
		1:0	PHY4_FS_DRIVER_ SR_SEL_2	FS driver slew rate control	0	0	0

Table 6 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
PHY5 CONFIG (DS port 4)	76	7:4	PHY5_HS_TX_AMPLITUDE	HS driver amplitude control	5	5	5
		3:2	PHY5_HS_N_PRE_DRIVER_SEL	HS NMOS pre-driver skew	0	0	0
		1:0	PHY5_HS_P_PRE_DRIVER_SEL	HS PMOS pre-driver skew	0	0	0
	77	7	PHY5_EN_LANE_SWAP	The DP/DN pins are swapped on both the transmit and receive direction.	0	0	0
		6	PHY5_HS_TED_LP_MODE	HS TED low power mode 0: Normal operation 1: Reduced current mode	0	0	0
		5:3	PHY5_HS_DRIVER_FINE_SLEW_SEL	HS driver fine slew rate control	0	0	0
		2:0	PHY5_HS_TX_PRE_EMPHASIS	HS driver pre-emphasis amplitude	4	4	4
	78	7:6	PHY5_FS_DRIVER_SR_SEL_1	FS driver slew rate control	0	0	0
		5:3	PHY5_FS_TRIGGER_VOLTAGE	FS receiver trigger voltage control	0	0	0
		2:0	PHY5_HS_CTLE	HS receiver CTLE control	0	0	0
	79	7	PHY5_DIS_PRE_EMPHASIS_HS_SOF	Setting this bit to '1' disables the PRE_EMPHASIS during the EOP of an SOF packet. BIT_TIME_DIS_PRE_EMPHASIS determines the bit position at which the pre-emphasis is disabled.	0	0	0
		6:5	PHY5_HS_TX_PRE_EMP_DURATION	Selects pre-emphasis phase 0: Pre-emphasis disabled 1: pll phase 2 2: pll phase 4 3: pll phase 6	2	2	2
		4	PHY5_HS_TED_25_MODE	HS Squelch VDDD selection bit 1: VDDD = 3.3 V range (**do not use this setting for normal operation**) 0: VDDD = 1.8 V range	0	0	0
		3:2	PHY5_LS_DRIVER_SR_SEL	FS driver slew rate control	0	0	0
		1:0	PHY5_FS_DRIVER_SR_SEL_2	FS driver slew rate control	0	0	0
Full-Speed Dev [9] Parameters	80	7:2	laneSwapEnable	This field decides LAN-SWAP parameter from external config is applicable or not.	0x00	0x00	0x00
		1	RESERVED	Reserved	–	–	–
		0	BB_ALWAYS_ON	Billboard operation control: 0 --> Enable BB USB only when I2C command received 1 --> Enable BB USB always	1	1	1

Table 6 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
Full-Speed Dev [9] Parameters	81	7:0	BB_VCONN_Power	Indicates the VCONN power required by Device Container 0x00 – 1W 0x01 – 1.5W 0x02 – 2W 0x03 – 3W 0x04 – 4W 0x05 – 5W 0x06 – 6W 0xFF – VCONN Power not required Other values – Reserved	0x3	0x3	0x3
	83:82	15:0	BB_TIMEOUT	Billboard timeout in ms. The USB interface will be disabled after this period for power saving. Set this to 0xFFFF if the USB interface should be left enabled.	0xFFFF	0xFFFF	0xFFFF
	85:84	15:0	FSDEV_VID	Vendor ID to be used for USBFS device	0x04B4	0x04B4	0x04B4
	87:86	15:0	FSDEV_PID	Product ID to be used for USBFS Device	0X6520	0X6520	0x6520
	89:88	15:0	FSDEV_VERS	bcdDevice used for USBFS device	0x0001	0x0001	0x0001
	90	7:0	BB_NumberOfAlternate OrUSB4vModes	Number of Alternate Modes is supported by Device Container. It takes values from 1 to 8	1	1	1
	91	7:0	BB_PreferredAlternate OrUSB4Mode	Index of the preferred Alternate mode. (bPreferredAlternate OrUSB4Mode of BB capability decriptor). It takes values from 0 to 7 for setting the preferred mode. If USB4 mode is supported, that is the preferred mode (Mode 0). 0xFF - indicates no preference	0xFF	0xFF	0xFF
	107:92	127:0	Reserved	Reserved	–	–	–
	109:108	15:0	BB_SVID_0	SVID for the first Alternate Mode or USB4 mode	0	0	0
	110	7:0	BB_AUM_0	Index of AUM for SVID #0	0	0	0
	111	7:0	BB_AM_STRING_0	Offset of string descriptor for Alternate Mode #0	0	0	0
	113:112	15:0	BB_SVID_1	SVID for the second Alternate Mode or USB4 mode	0	0	0
	114	7:0	BB_AUM_1	Index of AUM for SVID #1	0	0	0
	115	7:0	BB_AM_STRING_1	Offset of string descriptor for Alternate Mode #1	0	0	0
	117:116	15:0	BB_SVID_2	SVID for the third Alternate Mode or USB4 mode	0	0	0
	118	7:0	BB_AUM_2	Index of AUM for SVID #2	0	0	0
	119	7:0	BB_AM_STRING_2	Offset of string descriptor for Alternate Mode #2	0	0	0
	121:120	15:0	BB_SVID_3	SVID for the fourth Alternate Mode or USB4 mode	0	0	0
	122	7:0	BB_AUM_3	Index of AUM for SVID #3	0	0	0
	123	7:0	BB_AM_STRING_3	Offset of string descriptor for Alternate Mode #3	0	0	0
	125:124	15:0	BB_SVID_4	SVID for the fifth Alternate Mode or USB4 mode	0	0	0
	126	7:0	BB_AUM_4	Index of AUM for SVID #4	0	0	0
	127	7:0	BB_AM_STRING_4	Offset of string descriptor for Alternate Mode #4	0	0	0
	129:128	15:0	BB_SVID_5	SVID for the sixth Alternate Mode or USB4 mode	0	0	0
	130	7:0	BB_AUM_5	Index of AUM for SVID #5	0	0	0

Table 6 Parameter configuration table *(continued)*

Parameters	Table offset	Bits	Name	Description	Default value for CYUSB2344	Default value for CYUSB2343	Default value for CYUSB2345
Full-Speed Dev [9] Parameters	131	7:0	BB_AM_STRING_5	Offset of string descriptor for Alternate Mode #5	0	0	0
	133:132	15:0	BB_SVID_6	SVID for the seventh Alternate Mode or USB4 mode	0	0	0
	134	7:0	BB_AUM_6	Index of AUM for SVID #6	0	0	0
	135	7:0	BB_AM_STRING_6	Offset of string descriptor for Alternate Mode #6	0	0	0
	137:136	15:0	BB_SVID_7	SVID for the eighth Alternate Mode or USB4 mode	0	0	0
	138	7:0	BB_AUM_7	Index of AUM for SVID #7	0	0	0
	139	7:0	BB_AM_STRING_7	Offset of string descriptor for Alternate Mode #7	0	0	0
	143:140	31:0	BB_AM_VDO_0	dwAlternateModeVdo value for Alternate Mode #0	0	0	0
	147:144	31:0	BB_AM_VDO_1	dwAlternateModeVdo value for Alternate Mode #1	0	0	0
	151:148	31:0	BB_AM_VDO_2	dwAlternateModeVdo value for Alternate Mode #2	0	0	0
	155:152	31:0	BB_AM_VDO_3	dwAlternateModeVdo value for Alternate Mode #3	0	0	0
	159:156	31:0	BB_AM_VDO_4	dwAlternateModeVdo value for Alternate Mode #4	0	0	0
	163:160	31:0	BB_AM_VDO_5	dwAlternateModeVdo value for Alternate Mode #5	0	0	0
	167:164	31:0	BB_AM_VDO_6	dwAlternateModeVdo value for Alternate Mode #6	0	0	0
	171:168	31:0	BB_AM_VDO_7	dwAlternateModeVdo value for Alternate Mode #7	0	0	0
	172	7:0	iManufacturer_FSDEV	Offset of FSDEV manufacturer string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	173	7:0	iProduct_FSDEV	Offset of FSDEV product string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	174	7:0	iSerNum_FSDEV	Offset of FSDEV serial number string descriptor stored in variable part of configuration table	0x00	0x00	0x00
	175	7:0	iConfig_FSDEV	Offset of FSDev configuration string stored in variable part of configuration table	0x00	0x00	0x00
	176	7:0	iCDCCtrlIntf	Offset of CDC control interface string stored in variable part of configuration table	0x00	0x00	0x00
	177	7:0	iCDCDataIntf	Offset of CDC data interface string stored in variable part of configuration table	0x00	0x00	0x00
	178	7:0	iBillboardIntf	Offset of Billboard interface string stored in variable part of configuration table	0x00	0x00	0x00
	179	7:0	iAdditionalInfoURL	Offset of Billboard additional Info URL string stored in variable part of configuration table.	0x00	0x00	0x00
	191:180	7:0	RESERVED	Reserved	–	–	–

Note

9. All Full-Speed Dev parameters are kept at their default values, without a need for change, as the FS device is optional in consumer product.

3.8.2 Billboard configuration flow

The USB Billboard device class definition describes the methods used to communicate the alternate modes supported by a Device container to a host system. This includes string descriptors that can be used to provide support details in a human-readable format.

The following sequence can configure/change the Billboard parameters:

1. Power on the device
2. I2C command to set the Billboard to “Connect state” in 0xF028 I2C Slave register space. See **I2C Slave register space** for more information
3. Send “Disconnect state” in 0xF028 I2C Slave register space. See **I2C Slave register space** for more information
4. Configure the Billboard parameter in 0xF02C I2C Slave register space. See **I2C Slave register space** for more information
5. I2C command to set the Billboard to “Connect state” in 0xF028 I2C Slave register space. See **I2C Slave register space** for more information

3.8.3 I2C Slave register space

Table 7 lists I2C Slave registers that exist in addition to the configuration table for status and dynamic configuration of EZ-USB™ HX2G3.

Table 7 I2C Slave registers

Register address	Bit range	Register/ Field name	Default value	Description	Access permission[11, 12, 13]
0xF000	31:0	DEVICE_STATE	"APPL"	Device state (boot mode or application) indication[10]	RO
0xF004	31:0	RESERVED	0	Reserved: Will read as zero	RO
0xF008	31:0	RESERVED	0	Reserved: Will read as zero	RO
0xF00C	31:0	UFP_DFP configuration with US port selection	0	This register is used for runtime selection of Upstream - Downstream configuration. • Byte3(MSB) - Reserved • Byte2 - Reserved • Byte1 - 0 valid for 1UFP + 4DFP - 0,1 valid for 2UFP + 4DFP - 0,1,2 valid for 3UFP +3DFP • Byte0 - 001: For 1UFP + 4DFP Configuration - 010: For 2UFP + 4DFP Configuration - 100: For 3UFP +3DFP Configuration All invalid input leads to 1UFP +4DFP and US-0 configuration in system.	W
0xF010	0	US_VBUS_STATUS	0	Upstream Vbus status. If Vbus detect is disabled, this bit will always be set to 1.	RO
	6	US_VBUS_OVERRIDE_VALUE	0	If US_VBUS_OVERRIDE_ENABLE is set to 1, US_VBUS_STATUS will be overridden by the value of this register.	RW
	7	US_VBUS_OVERRIDE_ENABLE	0	Whether US_VBUS_STATUS should be over-ridden. 1: Override the US_VBUS_STATUS value 0: No override. Actual VBUS pin value will be considered	RW
0xF014	1:0	NUM_US_PORT_OPTIONS	1	Number of upstream port options available (1, 2 or 3). This value will get reflected based on the register configuration made in 0xF00C.	RO
	3:2	CUR_US_PORT_ID	0	Currently selected upstream port 0: US_DP/US_DM 1: US_ALT_DP/US_ALT_DM 2: US_ALT1_DP/US_ALT1_DM This value will get reflected based on the register configuration made in 0xF00C.	RO
	6:4	NUM_DS_PORTS	3	Number of external DS ports supported. This value will get reflected based on the register configuration made in 0xF00C.	RO
	7	FSDEV_PRESENT	1	Whether embedded FSDEV is enabled. This value is reflected as per the configuration table parameter.	RO
0xF018	1:0	MUXSEL_OVRD_VAL[1:0]	0	Value to override the MUXSEL1 and MUXSEL0 pin status. See Table 2.	RW
	7	MUXSEL_OVRD_EN	0	Whether MUXSEL pin status is to be overridden. 1: Override the US_VBUS_STATUS value 0: No override. MUXSEL0 & MUXSEL1 GPIO pins will be used.	RW

Table 7 I2C Slave registers *(continued)*

Register address	Bit range	Register/ Field name	Default value	Description	Access permission[11, 12, 13]
0xF01C	3:0	DS_PWREN_STATUS[3:0]	0x0	Power enable status for each of the downstream ports. Each bit can be over-written with the value provided if the corresponding DS_PWREN_OVRD bit is set.	RW
	7:4	DS_PWREN_OVRD[3:0]	0x0	Whether to over-ride the DS_PWREN_STATUS bits for each downstream port with the value provided. 1: Override the US_VBUS_STATUS value 0: No override	RW
0xF024	3:0	OC_FAULT_STATUS[3:0]	0x0	Over-current fault status for each of the downstream ports	RW
	7:4	OC_FAULT_OVRD[7:4]	0x0	Whether to over-ride the OC_FAULT_STATUS for each downstream port with the value provided. 1: Override the OC_FAULT_STATUS value 0: No override	RW
0xF028	0	BB_EVENT_TYPE	0	Type of Billboard event being sent to HX2G3 0: Disconnect, 1: Connect	RW
0xF028	1	BB_EVENT_EN	0	Whether new Billboard connect/disconnect event is being sent through HX2G3. This register configuration will only be applicable, if Billboard functionality is enabled & "Billboard Always ON" is set to NO in the Configuration Table . 1: HX2G3 Controls Billboard events. 0: HX2G3 is not controlling Billboard Events.	RW
0xF02C	1:0	BB_AM_STATE0	0x00	Two-bit status for Alternate mode 0 to be updated in the bmConfigured field of the Billboard capability descriptor **Value and description:** 00b - Unspecified Error 01b - AUM configuration not attempted or exited 10b - AUM configuration attempted but unsuccessful and not entered 11b - AUM configuration successful	RW
	3:2	BB_AM_STATE1	0x00	Two-bit status for Alternate mode 1 to be updated in the bmConfigured field of the Billboard capability descriptor **Value and description:** 00b - Unspecified Error 01b - AUM configuration not attempted or exited 10b - AUM configuration attempted but unsuccessful and not entered 11b - AUM configuration successful	RW
	5:4	BB_AM_STATE2	0x00	Two-bit status for Alternate mode 2 to be updated in the bmConfigured field of the Billboard capability descriptor **Value and description:** 00b - Unspecified Error 01b - AUM configuration not attempted or exited 10b - AUM configuration attempted but unsuccessful and not entered 11b - AUM configuration successful	RW
	7:6	BB_AM_STATE3	0x00	Two-bit status for Alternate mode 3 to be updated in the bmConfigured field of the Billboard capability descriptor **Value and description:** 00b - Unspecified Error 01b - AUM configuration not attempted or exited 10b - AUM configuration attempted but unsuccessful and not entered 11b - AUM configuration successful	RW

Table 7 I2C Slave registers *(continued)*

Register address	Bit range	Register/ Field name	Default value	Description	Access permission[11, 12, 13]
0xF02C	9:8	BB_AM_STATE4	0x00	Two-bit status for Alternate mode 4 to be updated in the bmConfigured field of the Billboard capability descriptor **Value and description:** 00b - Unspecified Error 01b - AUM configuration not attempted or exited 10b - AUM configuration attempted but unsuccessful and not entered 11b - AUM configuration successful	RW
	11:10	BB_AM_STATE5	0x00	Two-bit status for Alternate mode 5 to be updated in the bmConfigured field of the Billboard capability descriptor **Value and description:** 00b - Unspecified Error 01b - AUM configuration not attempted or exited 10b - AUM configuration attempted but unsuccessful and not entered 11b - AUM configuration successful	RW
0xF02C	13:12	BB_AM_STATE6	0x00	Two-bit status for Alternate mode 6 to be updated in the bmConfigured field of the Billboard capability descriptor **Value and description:** 00b - Unspecified Error 01b - AUM configuration not attempted or exited 10b - AUM configuration attempted but unsuccessful and not entered 11b - AUM configuration successful	RW
	15:14	BB_AM_STATE7	0x00	Two-bit status for Alternate mode 7 to be updated in the bmConfigured field of the Billboard capability descriptor **Value and description:** 00b - Unspecified Error 01b - AUM configuration not attempted or exited 10b - AUM configuration attempted but unsuccessful and not entered 11b - AUM configuration successful	RW
0xF030	7:0	BB_ADDL_FAIL_INFO	0x02	Additional failure info field to be added in Billboard capability descriptor **Bit and description:** **0** - If this field is set to one then the Device Container failed due to lack of power. **1** - If this field is set to one then the Device Container failed due to no USB-PD communication. This field is only valid if "BB_AM_STATE*n*" field for the preferred AUM is not set to 11b. 7..2 Reserved for future use, shall be set to zero	RW

Notes

10.In Boot mode, only firmware download is supported.
11.Read operation of I2C Slave register should be always in 4 bytes for one cycle.
12.Write operation of I2C Slave register should be always in 4 bytes for one cycle.
13.Read Only, Read and Write, and Write Only are abbreviated as RO, RW, and W respectively.

3.8.4 Dynamic UFP-DFP configuration

1. Ensure I2CSlaveEnable bit is set to 1 in the configuration table. See **Table 6**
2. External I2C master (DUT is in I2C slave mode) sends 0xF00C command to select the UFP_DFP configuration register (see **Table 7**) followed by 4 bytes of data
   - Data byte 0: UFP_DFP Config number
   - Data byte 1: Active upstream port number
   - Data byte 2: Not applicable
   - Data byte 3: Not applicable
3. Once HX2G3 receives the I2C command, it will update with new configuration, shut down the hub, and re-initialize itself
4. HX2G3 re-enumerates with the new configuration

3.9 Configuration for dock application and UUID read

The default I2C slave address of EZ-USB™ HX2G3 is '0x53'. The default I2C slave address can be changed using the configuration table. See **Table 6** for available configuration parameters.

The length of UUID is 16 bytes. The write and read cycle shown in **Figure 5** and **Figure 6** is for 4-byte data transfer. To obtain the 16-bytes of data, the I2C master application must repeat this cycle four times. The I2C read transaction should utilize the repeated start method. The UUID register address is 0x0A20.

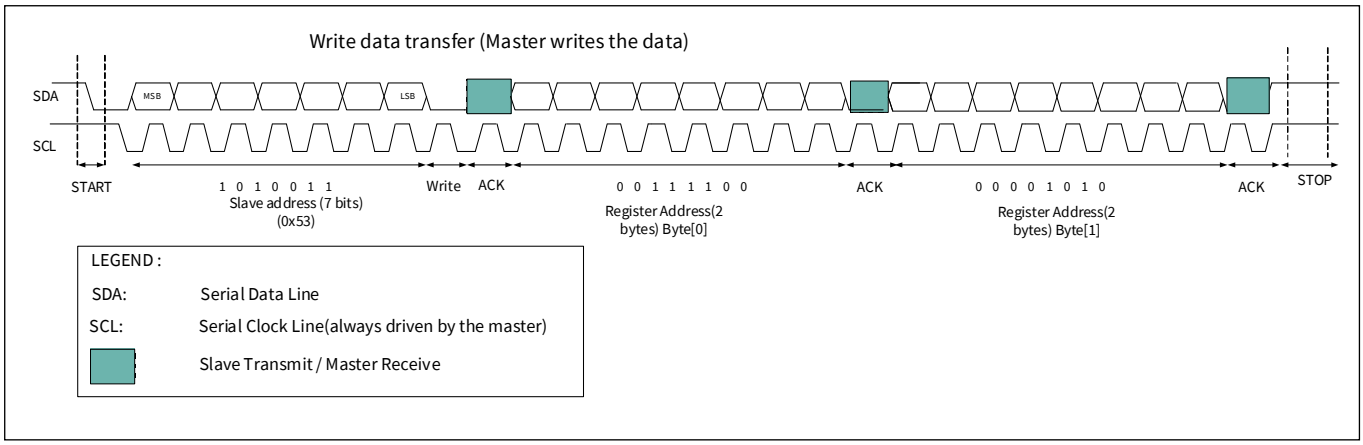


Figure 5 SCB_Master Write

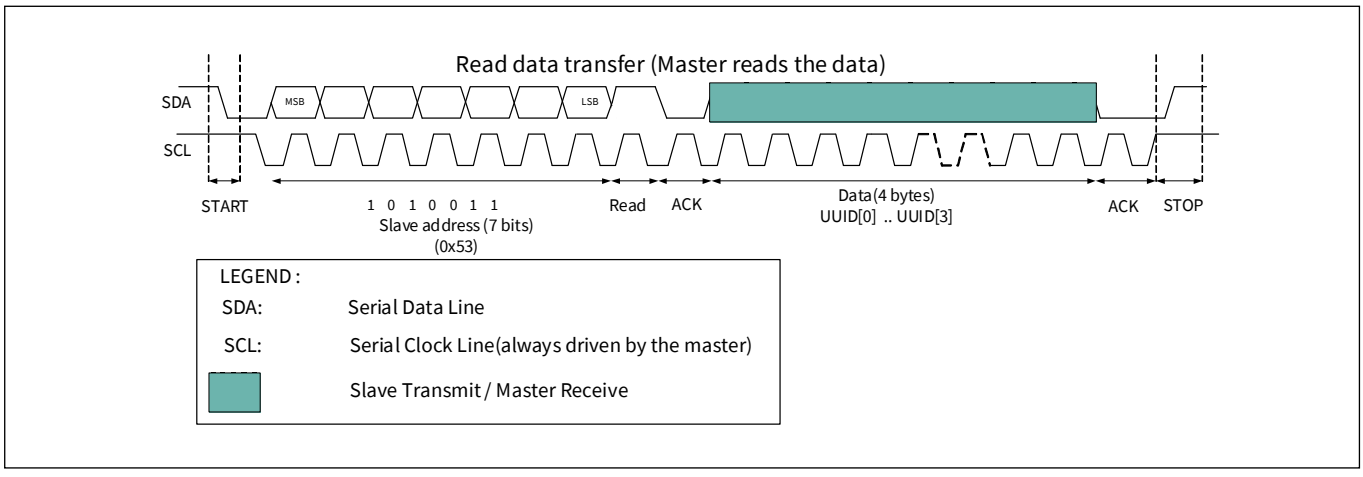


Figure 6 SCB_Master Read

4 Functional overview

4.1 Initialization

No specific power-up sequence is required; the device boots automatically once the input power is stable and the reset pin is HIGH. It is not recommended to provide voltage in I/O pins before the chip is powered using VDDD and VDDIO.

4.1.1 Initialization

The EZ-USB™ HX2G3 power-ON behavior expectation during initialization requires the following:

- Logic initialization: Logic initializes and assumes “nominal” operation within 5 ms after power has reached “nominal” conditions. The oscillator is enabled and remains active during power-up and reset conditioning
- I/O initialization: All output drivers remain in the High-Z state until the power reaches “nominal” conditions
- Program initialization: The CPU executes ROM code and loads configuration into the device’s registers from an external I2C EEPROM, I2C host, eFuse

4.1.2 Reset sequence

EZ-USB™ HX2G3 includes an active-low reset pin. When asserted and released, the Hub registers are initialized, USB communication is stopped, and the bootloader reinitializes the Hub. EZ-USB™ HX2G3 continues to enumerate with the host and the available downstream devices.

4.2 Power modes

EZ-USB™ HX2G3 supports three power modes: Active, Deep Sleep, and Reset.

4.2.1 Active mode

Active mode is the normal operating power mode where all chip resources that are used by the system are active and all clocks are running.

4.2.2 Deep Sleep

In Deep Sleep mode, all states are retained and the high-speed clock (IMO, ECO, PLL) is disabled. The low-speed clock (ILO) remains enabled and low-speed peripherals can remain active (for example, allowing wake up on I2C). This mode allows operation to resume at the same program counter value and will be the most frequently used mode when fast wake-up and operation restart is required. The device state is fully retained in this mode and SRAM is retained. Stack and critical parameters can be retained while allowing memory holding temporary and scratch pad variables to be powered off to reduce the leakage. The USB 2.0 PHYs are in suspend state but can be used for wake-up.

4.2.3 Reset

XRES pin is used for reset operation. Pulling XRES pin LOW resets the device.

5 Pin configurations

5.1 Pinout diagram

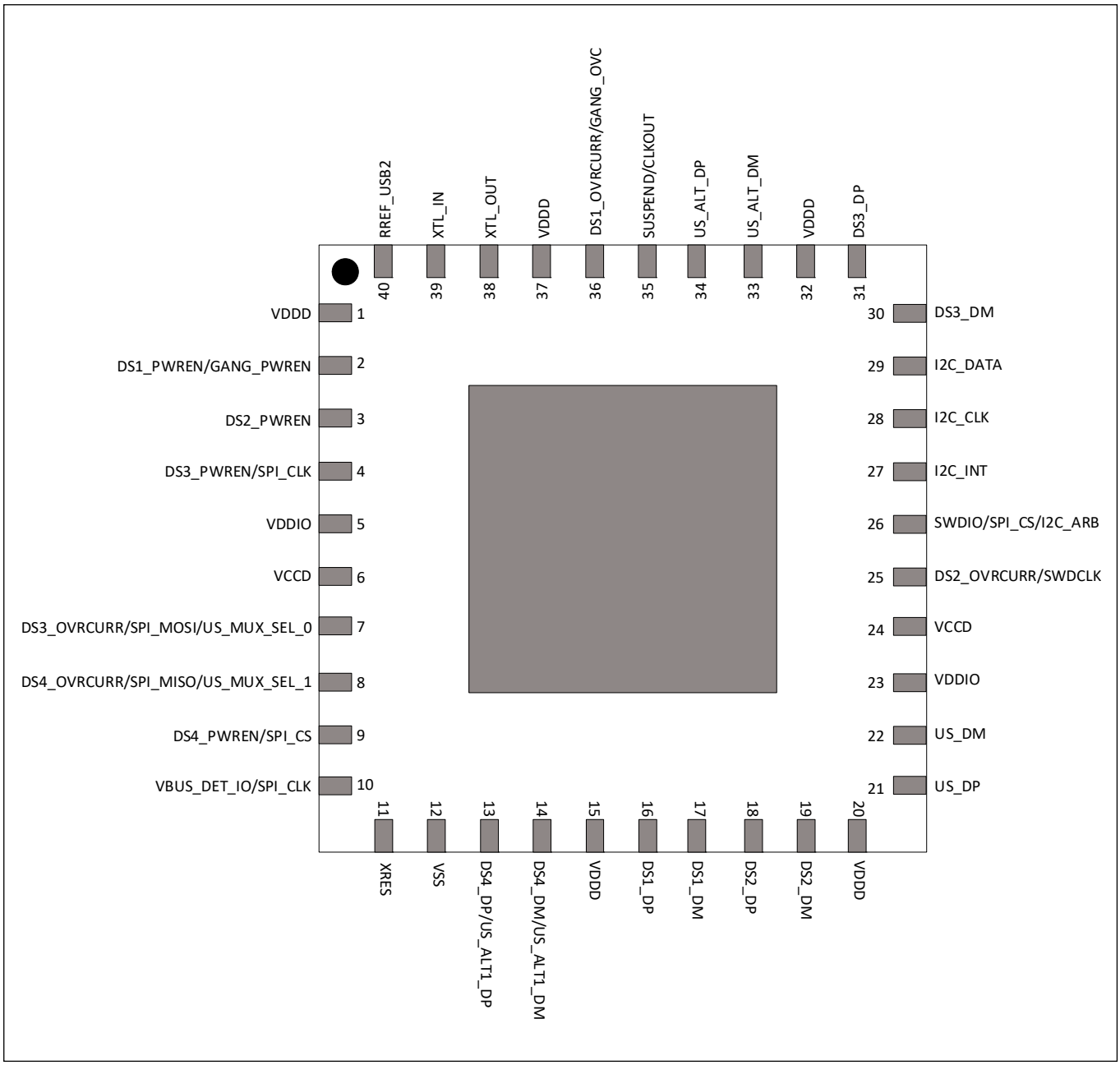


Figure 7 CYUSB2343-40QFN (40-pin QFN) pinout (top view)[15, 16]

Notes

14. If using SPI pins which are multiplexed with PWREN or OVRCURR pins, set the hub in Ganged power mode and ganged over current mode.
15. By default SPI is not enabled. Enable the SPI and pin mappings accordingly in the external config table.
16. For all of the multiplexed pins, only one of the functionality can be enabled after reset.

Pin configurations

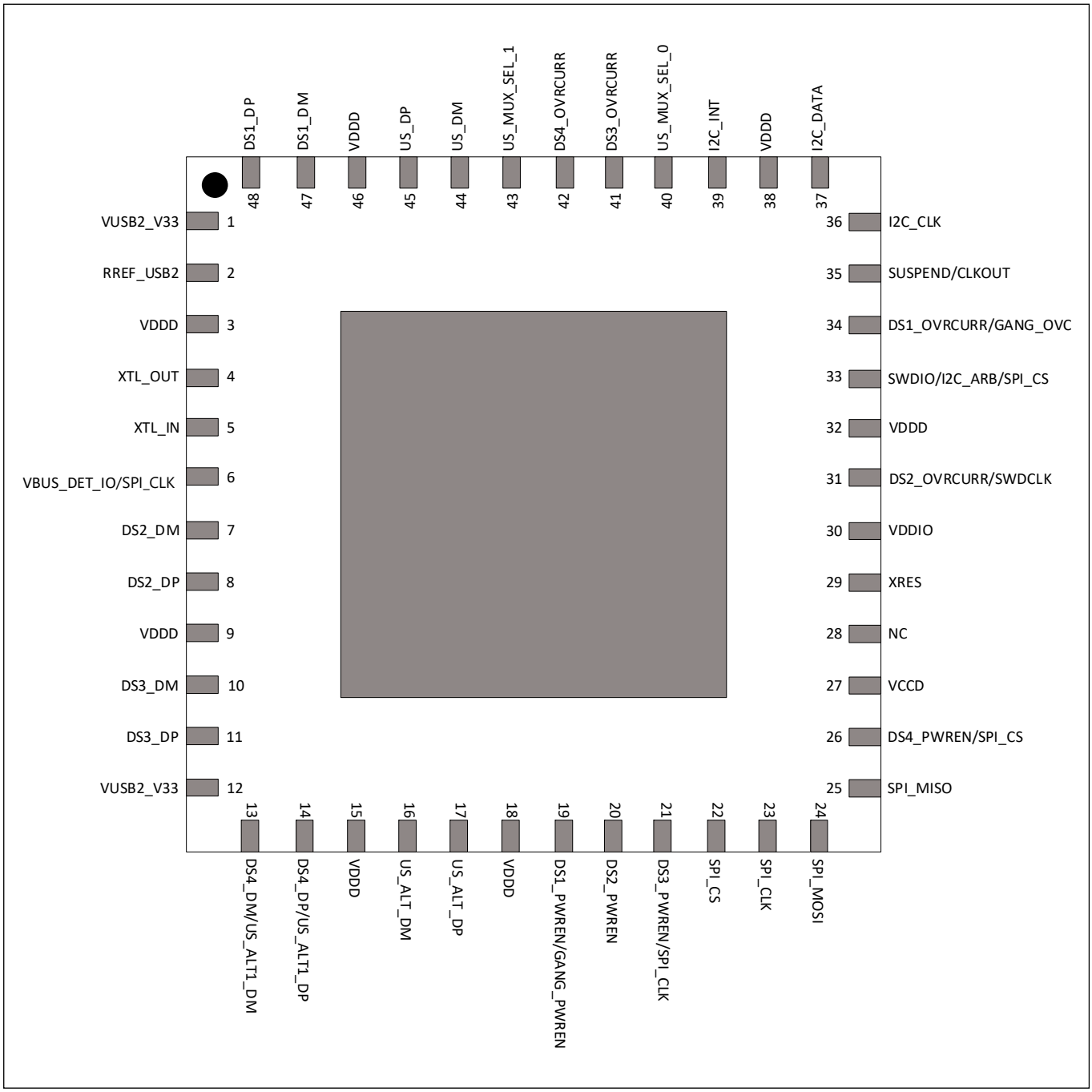


Figure 8 CYUSB2344-48BFXI (48-pin QFN) pinout (top view)[19, 20]

Notes

17. By default, Pin 23 is SPI_CLK. Pin 6 and Pin 21 need to be configured in the external config table to be used as SPI_CLK.
18. By default, Pin 22 is SPI_CS. Pin 26 and Pin 33 need to be configured in the external config table to be used as SPI_CS.
19. By default SPI is not enabled. Enable the SPI and pin mappings accordingly in the external config table.
20. For all of the multiplexed pins, only one of the functionality can be enabled after reset.

Pin configurations

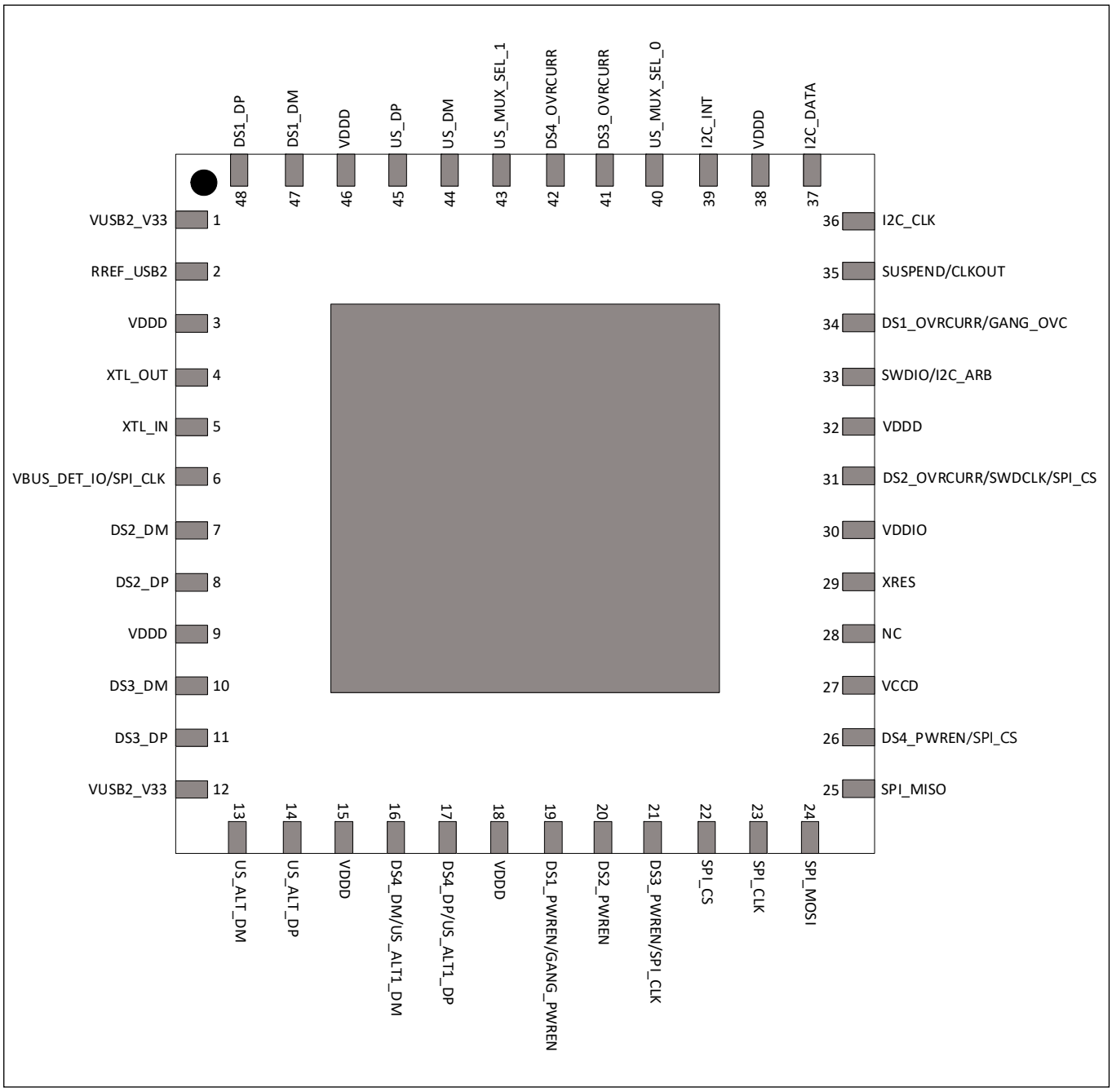


Figure 9 CYUSB2345-48BFXI (48-pin QFN) pinout (top view)[23]

Notes

21. By default, Pin 23 is SPI_CLK. Pin 6 and Pin 21 need to be configured in the external config table to be used as SPI_CLK.
22. By default, Pin 22 is SPI_CS. Pin 26 and Pin 33 need to be configured in the external config table to be used as SPI_CS.
23. For all of the multiplexed pins, only one of the functionality can be enabled after reset.

5.2 EZ-USB™ HX2G3 pinout description

Table 8 EZ-USB™ HX2G3 dock pinout description

Pin type	Pin name	CYUSB 48-QFN (2344-48)	CYUSB 48-QFN (2345-48)	CYUSB 40-QFN (2343-40)	Pin description
A	RREF_USB2	2	2	40	Reference resistor for USB 2.0 current generator (the recommended resistor value is 6.04 KΩ 1%)
PWR	VCCD	27	27	6,24	Internal core logic supply, VCCD, needs to be decoupled externally. See **Table 12** for the recommended capacitor specification. This is not to be used as an input or output power supply.
	VDDD	3,9,15,18, 32,38,46	3,9,15,18, 32,38,46	1,15,20, 32,37	Main digital supply input. It provides the inputs for the internal regulators. Also the power supply for the USB 2 HS PHY.
	VDDIO	30	30	5,23	GPIO input power supply.
	VBUS2_V33	1,12	1,12	–	Separate input power supply for USB 2 HS PHY (48-pin package only)
GND	VSS	EPAD	EPAD	12	Ground for the entire chip.
	EPAD	EPAD	EPAD	EPAD	Exposed pad connected directly to Ground.
I/O	DS1_DM	47	47	17	USB 2.0 Data Minus - DS Port 1
	DS1_DP	48	48	16	USB 2.0 Data Plus - DS Port 1
	DS1_OVERCURR/ GANG_OVC	34	34	36	GPIO, programmable as overcurrent detect for the DS1. By default Over current pin is active low.
	DS1_PWREN/ GANG_PWREN	19	19	2	GPIO, programmable as VBUS power enable output for port DS1. By default power enable pin is active low. When the port is not active, the default state for the pin is tristate.
	DS2_DM	7	7	19	USB 2.0 Data minus - DS Port 2
	DS2_DP	8	8	18	USB 2.0 Data plus - DS Port 2
	DS2_OVRCURR/ SWDCLK	31	31	25	GPIO, programmable as overcurrent detect for the DS2. By default Over current pin is active low. This pin is used as clock pin for SWD Interface
	DS2_PWREN	20	20	3	GPIO, programmable as VBUS power enable output for port DS2. By default power enable pin is active low. When the port is not active, the default state for the pin is tristate. This pin is used as data out for JTAG interface
	DS3_DM	10	10	30	USB 2.0 Data Minus - DS Port 3
	DS3_DP	11	11	31	USB 2.0 Data Plus - DS Port 3
	DS3_OVRCURR	41	41	–	GPIO, programmable as overcurrent detect for the DS3. By default Over current pin is active low.

Pin configurations

Table 8 EZ-USB™ HX2G3 dock pinout description

Pin type	Pin name	CYUSB 48-QFN (2344-48)	CYUSB 48-QFN (2345-48)	CYUSB 40-QFN (2343-40)	Pin description
I/O	DS3_PWREN/ SPI_CLK	21	21	4	GPIO, programmable as VBUS power enable output for port DS3. By default power enable pin is active low. When the port is not active, the default state for the pin is tristate, also programmable as SPI Clock.
	DS4_DM/US_ALT1_DM	13	16	14	USB 2.0 Data Minus - DS Port 4 Programmable as USB 2.0 Data Minus - Alt 1 US Port
	DS4_DP/US_ALT1_DP	14	17	13	USB 2.0 Data Minus - DS Port 4 Programmable as USB 2.0 Data Minus - Alt 1 US Port
	DS4_OVRCURR	42	42	–	GPIO, programmable as overcurrent detect for the DS4. By default Over current pin is active low.
	DS4_PWREN	26	26	–	GPIO, programmable as VBUS power enable output for port DS4. By default power enable pin is active low.When the port is not active, the default state for the pin is tristate
	DS4_PWREN/SPI_CS	–	–	9	GPIO, programmable as VBUS power enable output for DS4. By default, power enable pin is active low. When the port is not active, the default state for the pin is tristate. Alternatively, can be used for SPI chip select pin.
	I2C_CLK	36	36	28	I2C clock, used as GPIO when the I2C interface is not supported.
	I2C_DATA	37	37	29	I2C data, used as GPIO when the I2C interface is not supported.
	I2C_INT	39	39	27	I2C interrupt, used as GPIO when the I2C interface is not supported.
	SPI_CLK	23	23	–	SPI Clock. Output pin in Master mode and input pin in Slave mode.
	SPI_CS	22	22	–	SPI Chip Select. Output pin in Master mode and input pin in Slave mode.
	SPI_MOSI	24	24	–	SPI data from an external source to the hub SPI master/slave. In Master mode, it is an output. In Slave mode, it is an input.
	SPI_MISO	25	25	–	SPI data from the hub to an external SPI master/salve. In Master mode, it is an input. In Slave mode, it is an output.

Pin configurations

Table 8 EZ-USB™ HX2G3 dock pinout description

Pin type	Pin name	CYUSB 48-QFN (2344-48)	CYUSB 48-QFN (2345-48)	CYUSB 40-QFN (2343-40)	Pin description
I/O	DS3_OVRCURR/ SPI_MOSI/ US_MUX_SEL_0	–	–	7	GPIO, programmable as overcurrent detect for the DS3. By default Over current pin is active low. Additionally, programmable as SPI data from an external source to the hub SPI master/slave. In Master mode, it is an output. In Slave mode, it is an input. Alternatively, when the third upstream port configuration is enabled and this pin is set, the third upstream port is enabled and other two are disabled. See **Table 2** for the truth table of the US_MUX_SEL pins.
	DS4_OVRCURR/ SPI_MISO/ US_MUX_SEL_1	–	–	8	GPIO, programmable as overcurrent detect for the DS4. By default overcurrent pin is active low.Also programmable as SPI data from the hub to an external SPI master/ slave. In Master mode it is an input. In Slave mode it is an output. Alternatively, when the hub is configured for 2-US ports, this pin selects which port is the active US port. See **Table 2** for the truth table of the US_MUX_SEL pins.
	SUSPEND/ CLKOUT	35	35	35	GPIO, programmable as HUB Suspend indication. This pin is asserted if the USB 2.0 hub is in suspend state and is deasserted when the hub comes out of the Suspend state. Alternatively, can be used as clock output for cascading the Hub.
	SWDDIO/ SPI_CS/ I2C_ARB	–	–	26	SWDIO pin for SWD interface. Programmable as SPI Chip Select. I2C_ARB functionality is used during I2C Multi-master environment[24].
	US_ALT_DM	16	13	33	USB 2.0 Data Minus - Alternate #1 for US Port
	US_ALT_DP	17	14	34	USB 2.0 Data Plus - Alternate #1 for US Port
	US_DM	44	44	22	USB 2.0 Data Minus - US Port
	US_DP	45	45	21	USB 2.0 Data Plus - US Port
	US_MUX_SEL_1	43	43	–	When the third upstream port configuration is enabled: when set, enables the third upstream port while disabling the other two. See Table 2 for the truth table of the US_MUX_SEL pins
	US_MUX_SEL_0	40	40	–	When the third upstream port configuration is enabled: when set, enables the third upstream port while disabling the other two. See **Table 2** for the truth table of the US_MUX_SEL pins.

Pin configurations

Table 8 EZ-USB™ HX2G3 dock pinout description

Pin type	Pin name	CYUSB 48-QFN (2344-48)	CYUSB 48-QFN (2345-48)	CYUSB 40-QFN (2343-40)	Pin description
	VBUS_DET_IO	6	6	–	VBUS detect
I/O	VBUS_DET_IO/ SPI_CLK	–	–	10	VBUS detect, also programmable as SPI Clock. **Note**: In CYUSB2343-40, SPI is enabled by default, and SPI_CLK is routed to Pin 4 (DS3_PWREN/SPI_CLK) to preserve the VBUS_DET_IO pin. Consequently, since the DS3_PWREN function on Pin 4 is unavailable, CYUSB2343-40 operates in gang-powered mode by default.
	XRES	29	29	11	Active Low Reset input
	XTAL_IN	5	5	39	Crystal in. When oscillator is used this pin acts as an oscillator input.
	XTAL_OUT	4	4	38	Crystal out. When the oscillator is used, this pin should be kept as floating
	SWDDIO/ I2C_ARB	33	33	–	I2C_ARB functionality is used during I2C Multi-master environment[24]. SWDIO pin for SWD interface.
	RESERVED	28	28	–	–

Table 9 Differences in pin between CYUSB2344-48QFN and CYUSB2345-48QFN products

Sl No	Difference
1	In CYUB2344-48QFN, ‘DS4_DM/US_ALT1DM’ pin is ‘13’; In CYUSB2345-48QFN, ‘DS4_DM/US_ALT1DM’ pin is ‘16’.
2	In CYUSB2344-48QFN, ‘DS4_DP/US_ALT1_DP’ pin is ‘14’; In CYUSB2345-48QFN, ‘DS4_DP/US_ALT1_DP’ pin ‘17’.
3	In CYUSB2344-48QFN, ‘US_ALT_DM’ pin is ‘16’; In CYUSB2345-48QFN, ‘US_ALT_DM’ pin is ‘13’.
4	In CYUSB2344-48QFN ‘US_ALT_DP’ pin is ‘17’; In CYUSB2345-48QFN, ‘US_ALT_DP’ pin is ‘14’.

Note

24. EZ-USB™ HX2G3 arbitration feature: In a multi-master system, this feature allows the EZ-USB™ HX2G3 to perform a synchronization with the other I2C master on the bus to request/release control of the bus. This is done by sending a fixed length pulse on the I2C_ARB pin.

6 Electrical specifications

EZ-USB™ HX2G3 meets all USB-IF electrical compliance specifications.

6.1 Electrostatic discharge (ESD)

EZ-USB™ HX2G3 has a built-in ESD protection on all pins. The system-level ESD on all pins is the standard ±2-KV Human-body model (HBM) and 500-V Charged-device model (CDM).

On the DP and DM pins, the system-level ESD is HBM+CDM and IEC61000-4-2 to support ±8-KV contact and ±15-KV air discharge.

6.2 Absolute maximum ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 10 Absolute maximum ratings

Parameter	Description	Min	Typ	Max	Unit
VDD_ABS	Analog or digital supply relative to Vss (Vssd = Vssa)	–0.3	–	4	V
VDDIO_ABS	Max voltage on VDDIO	–0.3	–	4	V
VGPIO_OVT_ABS	OVT GPIO voltage	–0.5	–	4	V
IGPIO_ABS_DS0	Current per GPIO at Drive Strength = 0	–7.5	–	7.5	mA
IGPIO_ABS_DS1	Current per GPIO at Drive Strength = 1	–5.6	–	5.6	mA
IGPIO_ABS_DS2	Current per GPIO at Drive Strength = 2	–3.8	–	3.8	mA
IGPIO_ABS_DS3	Current per GPIO at Drive Strength = 3	–1.9	–	1.9	mA
ESD_HBM	Human body model (HBM) robustness according to ANSI/ESDA/JEDEC JS-001-2024	–2000	–	2000	V
ESD_CDM	Charged device model (CDM) robustness according to ANSI/ESDA/JEDEC JS-002-2022; voltage level refers to test condition (TC) mentioned in the standard	–500	–	500	V
LU	Pin current for latchup free operation	–100	–	100	mA
T_J	Junction temperature	–	–	125	°C
TSTG	Storage temperature	–65	–	150	°C
T_A	Operating temperature	–40	–	85	°C

6.3 Device-level specification

6.3.1 DC specifications

Table 11 DC specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
VDDD[25]	Main analog supply	–	2.97	3.3	3.63	V
VDD_EFUSE	VDDD supply when programming eFuse	E-Fuse programming	2.38	2.5	2.62	V
VDDIO[25]	Power supply voltage for IO	–	2.97	3.3	3.63	V
VCCD	Core logic supply	–	–	1.1	–	V
V_{IH_I2C}	I2C input voltage high threshold	–	0.7 × VDDIO	–	–	V
V_{IL_I2C}	I2C input voltage low threshold	–	–	–	0.3 × VDDIO	V
V_{IH_GPIO}	Input voltage HIGH level	–	0.65 × VDDIO	–	–	V
V_{IL_GPIO}	Input voltage LOW level	–	–	–	0.35 × VDDIO	V
V_{HYST_I2C}	Input hysteresis GPIO	–	0.1 × VDDIO	–	–	V
I_{IL}	Input leakage current (absolute value)	–	–1	–	1	µA
$I_{OH\_V3P3\_0}$	3.3 V pull-up current, Drive Strength = 0	–	–4.24	–	–11.76	mA
$I_{OH\_V3P3\_1}$	3.3 V pull-up current, Drive Strength = 1	–	–2.12	–	–5.88	mA
$I_{OH\_V3P3\_2}$	3.3 V pull-up current, Drive Strength = 2	–	–1.59	–	–4.41	mA
$I_{OH\_V3P3\_3}$	3.3 V pull-up current, Drive Strength = 3	–	–0.53	–	–1.47	mA
$I_{OL\_V3P3\_0}$	3.3 V pull-down current, Drive Strength =0	–	4.24	–	11.76	mA
$I_{OL\_V3P3\_1}$	3.3 V pull-down current, Drive Strength =1	–	2.12	–	5.88	mA
$I_{OL\_V3P3\_2}$	3.3 V pull-down current, Drive Strength =2	–	1.59	–	4.41	mA
$I_{OL\_V3P3\_3}$	3.3 V pull-down current, Drive Strength =3	–	0.53	–	1.47	mA

Table 12 lists the decoupling capacitor information recommended for VCCD.

Table 12 VCCD decoupler capacitor specification

Parameter	Description	Min	Typ	Max	Unit
CDEC1	Decoupling capacitor on VCCD	1.88	4.7	6.58	µF

Note

25.In the 48-QFN package, the pinout of VDDD, VDDIO, and VUSB2_V33 are separate. Therefore, this allows 48-QFN package specifically, to operate VDDD and VDDIO at 1.8 V, while VUSB2_V33 is at 3.3 V for lower power.

6.4 Power consumptions

Table 13 and Table 14 provide the power consumption values for EZ-USB™ HX2G3 under different conditions and combinations of active ports. All specification are valid for –40°C ≤ TA ≤ 85°C and 3.63 V except where noted.

Table 13 Power consumption with VDDD supply at 3.3 V

Parameter	Description	Min	Typ	Max	Unit
HX2G3_SUSPEND	Hub in Suspend and DS devices connected	–	1.1	2.5	mW
HX2G3_L0_SUSPEND	Hub in Suspend and No DS devices	–	1.1	2.5	
HX2G3_L0_1HS1	Hub in L0 and 1 HS device connected	–	210	250	
HX2G3_L0_2HS2	Hub in L0 and 2 HS device connected	–	225	260	
HX2G3_L0_3HS3	Hub in L0 and 3 HS device connected	–	240	270	
HX2G3_L0_4HS4	Hub in L0 and 4 HS device connected	–	255	285	
HX2G3_L0_1HS_RW	1 HS device connected with Read / Write	–	270	310	
HX2G3_L0_2HS_RW	2 HS device connected with Read / Write	–	390	440	
HX2G3_L0_3HS_RW	3 HS device connected with Read / Write	–	500	580	
HX2G3_L0_4HS_RW	4 HS device connected with Read / Write	–	600	665	
Power Down	XRES(RESET_N) asserted	–	200	–	µW

Table 14 Power consumption for 48-LGA with VDDD supply at 1.8 V

Parameter	Description	Min	Typ	Max	Unit
HX2G3_SUSPEND	Hub in Suspend and DS devices connected	–	1.1	1.6	mW
HX2G3_L0_SUSPEND	Hub in Suspend and No DS devices	–	1.1	1.6	
HX2G3_L0_1HS1	Hub in L0 and 1 HS device connected	–	160	175	
HX2G3_L0_2HS2	Hub in L0 and 2 HS device connected	–	160	175	
HX2G3_L0_3HS3	Hub in L0 and 3 HS device connected	–	160	175	
HX2G3_L0_4HS4	Hub in L0 and 4 HS device connected	–	160	175	
HX2G3_L0_1HS_RW	1 HS device connected with Read / Write	–	190	210	
HX2G3_L0_2HS_RW	2 HS device connected with Read / Write	–	250	280	
HX2G3_L0_3HS_RW	3 HS device connected with Read / Write	–	310	340	
HX2G3_L0_4HS_RW	4 HS device connected with Read / Write	–	365	395	
Power Down	XRES(RESET_N) asserted	–	100	–	µW

7 Package information

7.1 Package details

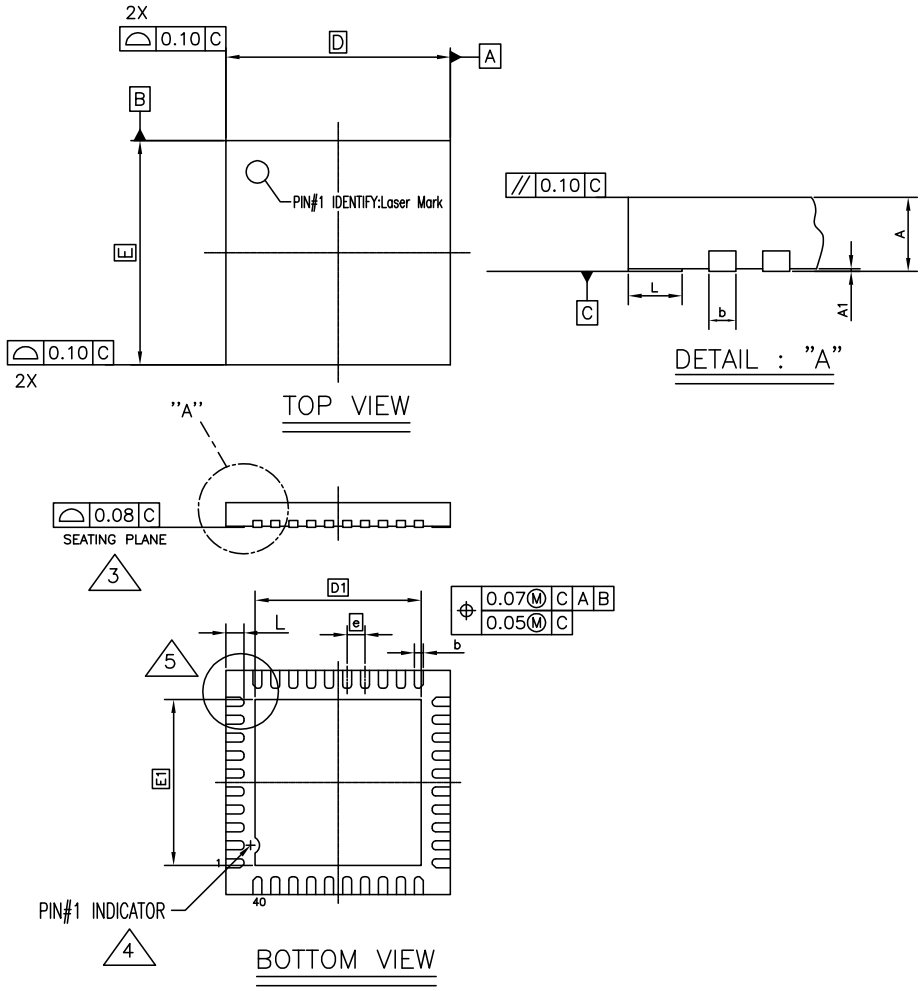
Table 15 40-QFN commercial package details

PKG_1	Package 1: type	Min	Typ	Max	Unit	QFN
PKG_1Z	Package 1: height	–	–	0.6	mm	Must meet customer's system limits (duplicate package rows for each supported package)
PKG_1W	Package 1: width	4.9	5	5.1	mm	Must meet customer's system limits
PKG_1L	Package 1: length	4.9	5	5.1	mm	Must meet customer's system limits
PKG_1PTCH	Package 1: pin / bump pitch	–	0.4	–	mm	Must match customer board capability
PKG_1CNT	Package 1: Total signal pins	–	40	–	–	Must match customer board capability
PKG_1TJA	Package 1: Theta-JA	–	25.4	–	°C/W	Must meet customer's system limits
PKG_1TJC	Package 1: Theta-JC	–	1.8	–	°C/W	Must meet customer's system limits
–	Solder reflow	–	–	260	°C	–
–	MSL	3	–	–	–	–
–	T_A	–	85	–	°C	–
–	T_J	–	97.5	–	°C	–

Table 16 48-QFN commercial package details

PKG_1	Package 1: type	Min	Typ	Max	Unit	Wettable flanks QFN
PKG_1Z	Package 1: height	–	–	0.9	mm	Must meet customer's system limits (duplicate package rows for each supported package)
PKG_1W	Package 1: width	5.9	6	6.1	mm	Must meet customer's system limits
PKG_1L	Package 1: length	5.9	6	6.1	mm	Must meet customer's system limits
PKG_1PTCH	Package 1: pin / bump pitch	–	0.4	–	mm	Must match customer board capability
PKG_1CNT	Package 1: Total signal pins	–	48	–	–	Must match customer board capability
PKG_1TJA	Package 1: Theta-JA	–	53.04	–	°C/W	Must meet customer's system limits
PKG_1TJC	Package 1: Theta-JC	–	28.79	–	°C/W	Must meet customer's system limits
–	Solder reflow	–	–	260	°C	–
–	MSL	3	–	–	–	–
–	T_A	–	85	–	°C	–
–	T_J	–	108	–	°C	–

7.2 Package diagram



SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	-	-	0.05
b	0.15	0.20	0.25
D		5.00 BSC	
E		5.00 BSC	
D1		3.70 BSC	
E1		3.70 BSC	
e		0.40 BSC	
L	0.30	0.40	0.50
N		40	

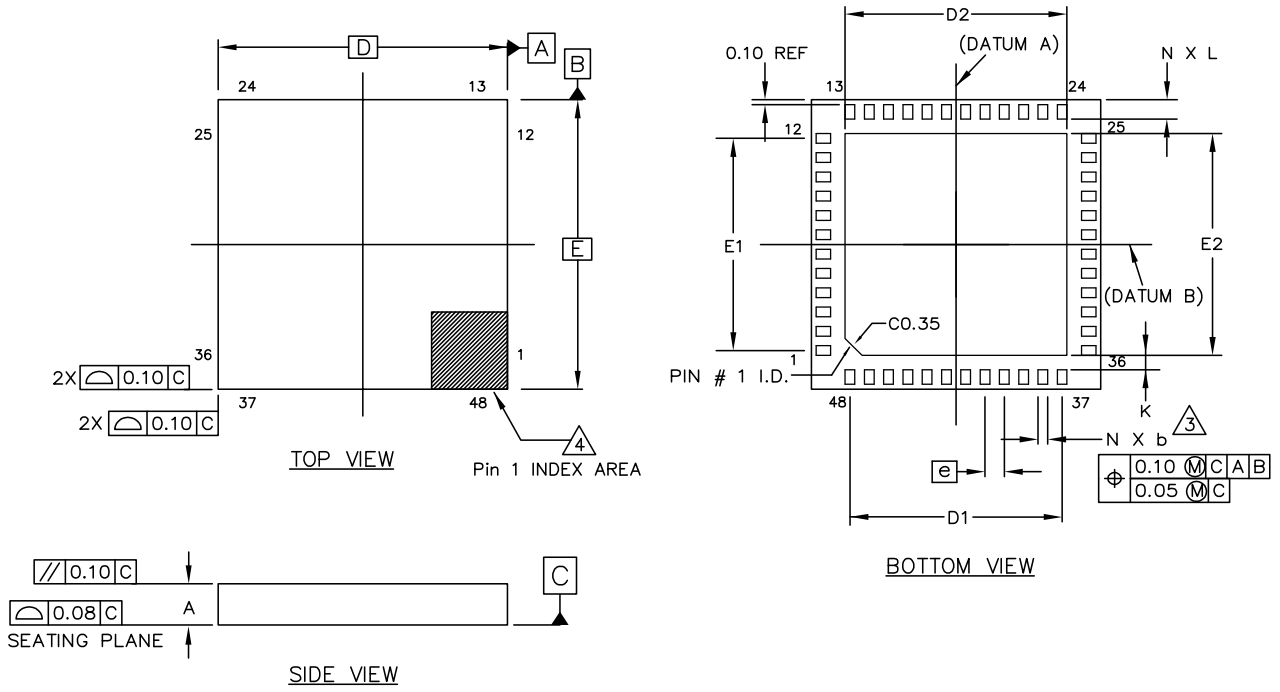
NOTE:

1. ALL DIMENSIONS ARE IN MM.
2. MAX COPLANARITY IS 0.08mm AND APPLIES TO THE EXPOSED PAD AS WELL AS THE LEADS.
3. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
4. EXACT SHAPE AND SIZE OF PIN #1 MARKING MAY VARY.
5. EXACT CORNER LEAD SHAPE MAY VARY. CHAMFER LEADS ARE APPLIED TO MAINTAIN MINIMUM SPACING BETWEEN CORNER LEADS. OTHERWISE, KEEP NORMAL LEAD SHAPE.

002-13583 *B

Figure 10 40-pin QFN (5.0 × 5.0 × 0.60 mm) LQ40D/LQ40E (PG-VQFN-40)

Package information



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.40 BSC	
N		48	
L	0.30	0.40	0.50
b	0.15	0.20	0.25
D1	4.30	4.40	4.50
E1	4.30	4.40	4.50
D2	4.50	4.60	4.70
E2	4.50	4.60	4.70
D		6.00 BSC	
E		6.00 BSC	
A	-	-	0.90
K		0.30 MIN	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" IS MEASURED AT THE MAXIMUM LEAD WIDTH IN A PLANE PARALLEL TO DATUM C.
4. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.

Figure 11 48-pin QFN (6.0 × 6.0 × 0.9 mm) L1A048, (PG-VFLGA-48)

7.3 Package layout guidelines

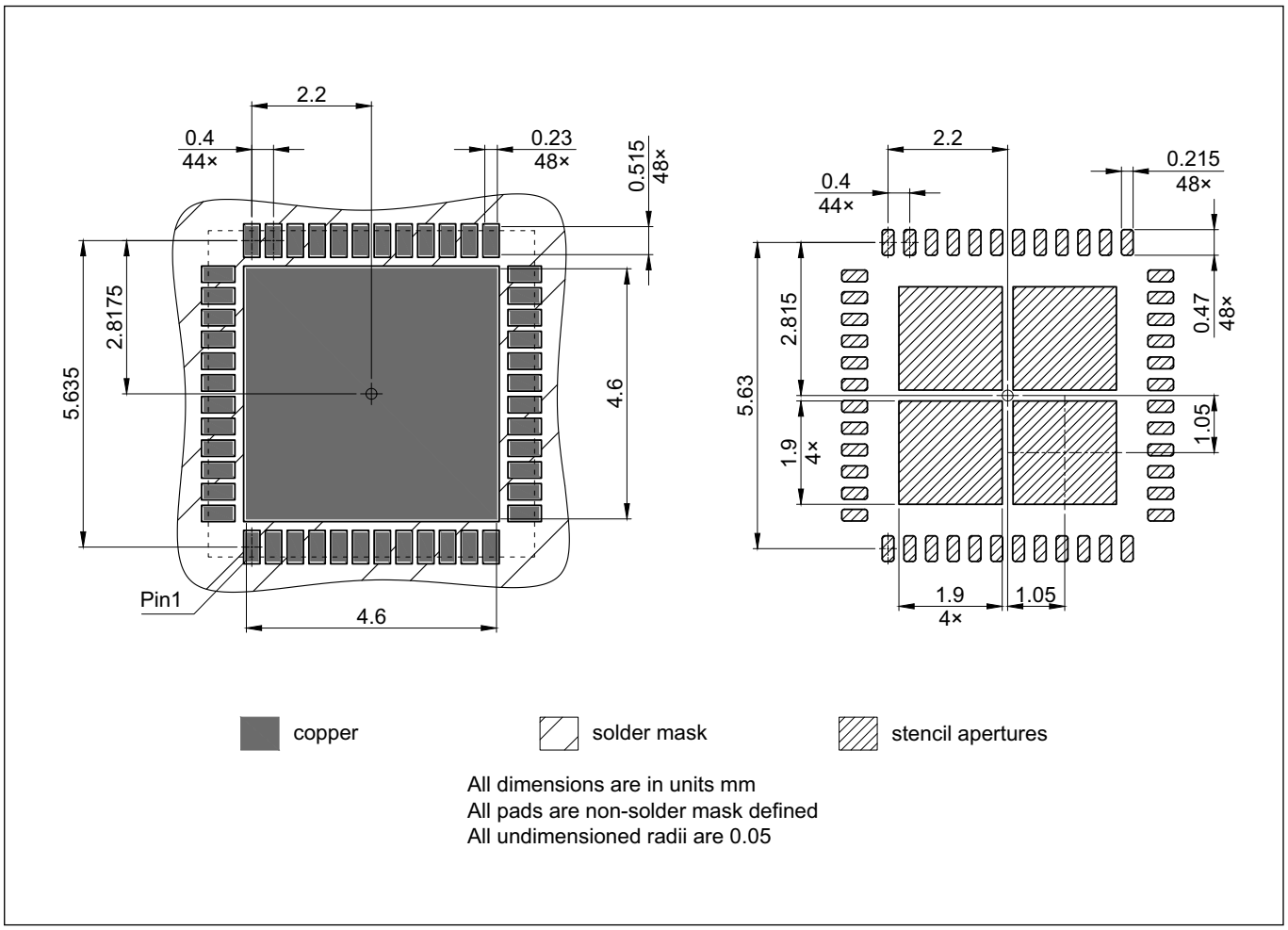


Figure 12 PG-VFLGA-48-1 boardpads and apertures

Package information

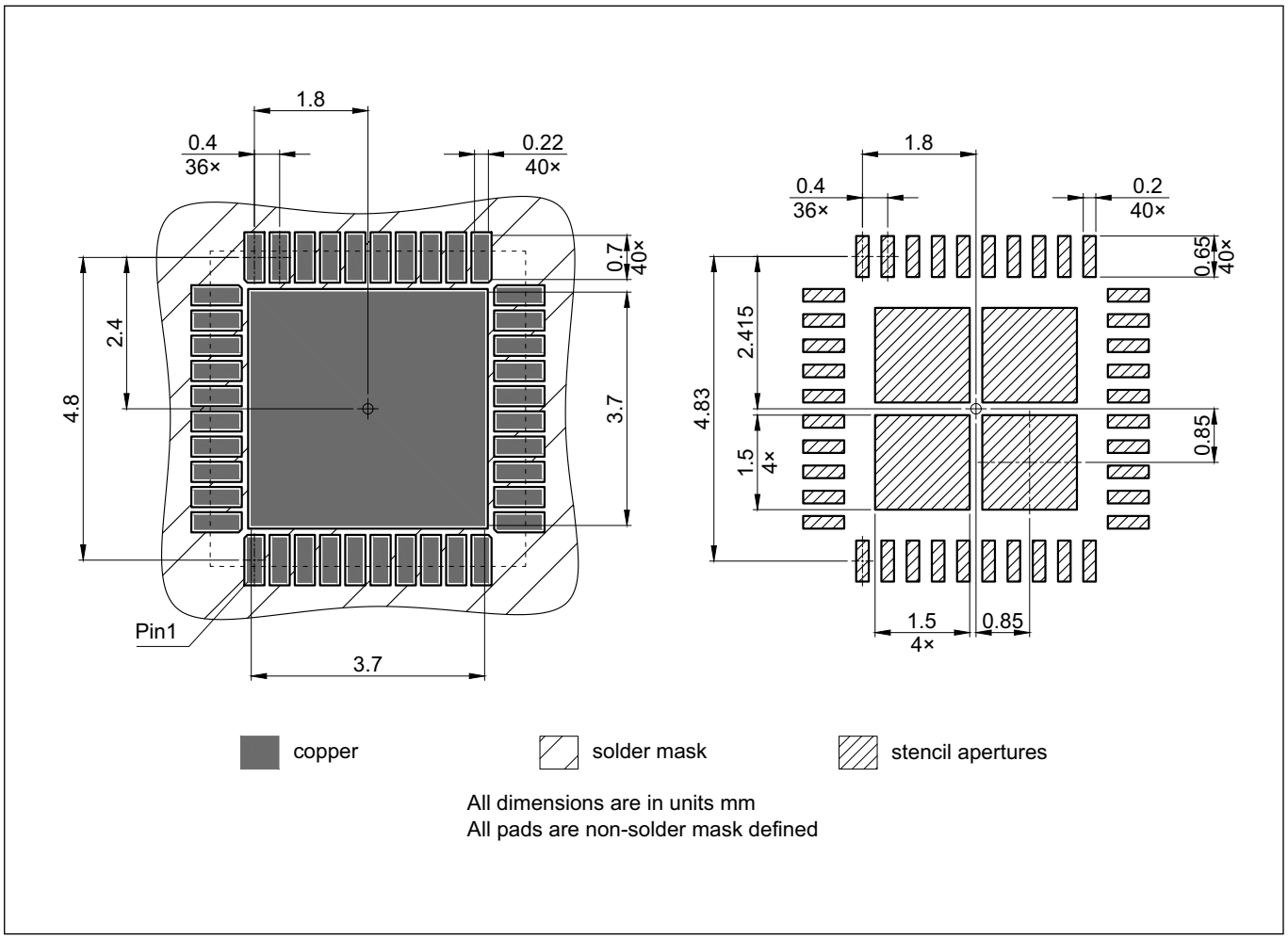


Figure 13 PG-UQFN-40 boardpads and apertures

8 Ordering information

Table 17 Ordering information

Product	Description	Feature differences	TID	Application	Package
CYUSB2343-40LTXI[26]	USB 2.0 Configurable hub with three configurations for docks	40-pin product with limited I/O and multiplexed feature options available. See **Table 8** for more details on features/pins available.	–	Docking application (–40°C to 85°C)	40-QFN, 5 × 5 mm, 0.4 mm pitch
CYUSB2344-48BFXI[26,27]		48-pin product with more I/O. See **Table 8** for more details on features/pins available.	–		48-QFN, 6 × 6 mm, 0.4 mm pitch
CYUSB2345-48BFXI[26,27, 28]		48-pin product with more I/O. See **Table 8** for more details on features/pins available.	–		48-QFN, 6 × 6 mm, 0.4 mm pitch

Note
26. All products can be configured to support 1:4, 2:4, or 3:3 configuration during Boot or over I2C during runtime. See the **"Pin configurations"** on page 33 for more details on PIN configuration.
27. The only difference between CYUSB2344 and CYUSB2345 is that the US_ALT_DM/DP port and US_ALT1_DM/DP ports are swapped between the two.
28. 48-QFN has internal construction as LGA.

8.1 Ordering code definition

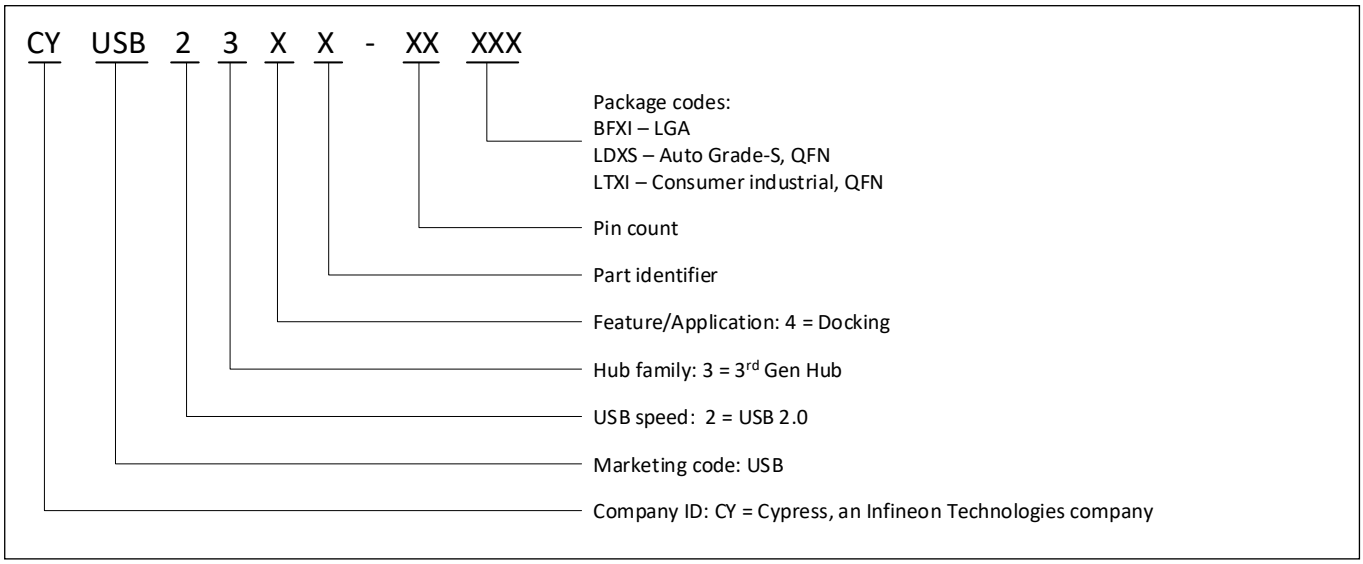


Figure 14 Ordering code definition

8.2 Silicon IDs

Table 18 Silicon IDs

Product	Package	Silicon ID	Family ID	Major/minor die rev ID
CYUSB2344-48BFXI CYUSB2344-48BFXIT CYUSB2344-48BFXIES CYUSB2344-48BFXIEST	48-QFN dock	0xF050	0x121	0x1
CYUSB2345-48BFXI CYUSB2345-48BFXIT CYUSB2345-48BFXIES CYUSB2345-48BFXIEST	48-QFN dock	0xF051	0x121	0x1
CYUSB2343-40LTXI CYUSB2343-40LTXIT CYUSB2343-40LTXIES CYUSB2343-40LTXIEST	40-QFN dock	0xF062	0x121	0x1

9 Acronyms

Table 19 Acronyms used in this document

Acronym	Description
BB	Billboard
CFP	common footprint part
CLK	clock
DC	direct current
DFP	downstream facing port
DMC	dock management controller
DP	Display Port
DS	downstream
EC	embedded controller
EEPROM	electrically erasable programmable read-only memory
ESD	electrostatic discharge
FET	field effect transistor
FSDEV	full speed device
FW	firmware
GPIO	general purpose input output
I/F	interface
I2C	Inter-Integrated Circuit
IoT	internet of things
LSB	least significant bit
MSB	most significant bit
MST	multi string transport
ms	millisecond
MUX	multiplexer
NC	no connection
NVIC	nested vector interrupt controller
PD	Power Delivery
PHY	physical layer
PID	product identifier
PLL	phase locked loop
ROM	read only memory
RX	receiver
SCB	serial communication block
SPI	Serial Peripheral Interface

Acronyms

Table 19 Acronyms used in this document *(continued)*

Acronym	Description
SRAM	serial random access memory
SWD	serial wire debug
TX	transmitter
UART	universal asynchronous receive transmit
UFP	upstream facing port
US	upstream
USB	Universal Serial Bus
UUID	universally unique identifier
VID	vendor identifier
WIC	wake up interrupt controller
XTAL	crystal

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Document revision	Date	Description of changes
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