EZ-PD™ PMG1-B2: 1 to 12-cell battery charge controller with USB-C PD MCU

General description

EZ-PD™ PMG1-B2 is a highly integrated System-In-Package (SIP) consisting of a single-port USB-C Power Delivery (PD) solution with an integrated buck-boost controller for 1 to 12-cell Lithium-ion battery charging. It complies with the latest USB-C and PD specifications. EZ-PD™ PMG1-B2 supports a wide input voltage range (4.5 to 55 V) and programmable switching frequency (200 to 700 kHz).

EZ-PD™ PMG1-B2 is a programmable USB PD solution with on-chip 32-bit Arm® Cortex®-M0 processor, 128 KB flash, and 8 KB SRAM. It also includes various analog and digital peripherals such as ADCs, PWMs, and timers.

Applications

EZ-PD™ PMG1-B2 is targeted at applications that require USB PD integrated battery charging up to 240 W, functioning as a USB PD Sink or USB PD DRP device:

- Cordless power and garden tools
- Cordless vacuum cleaners
- Cordless kitchen appliances
- E-bikes and E-kick scooters
- Drones and robots

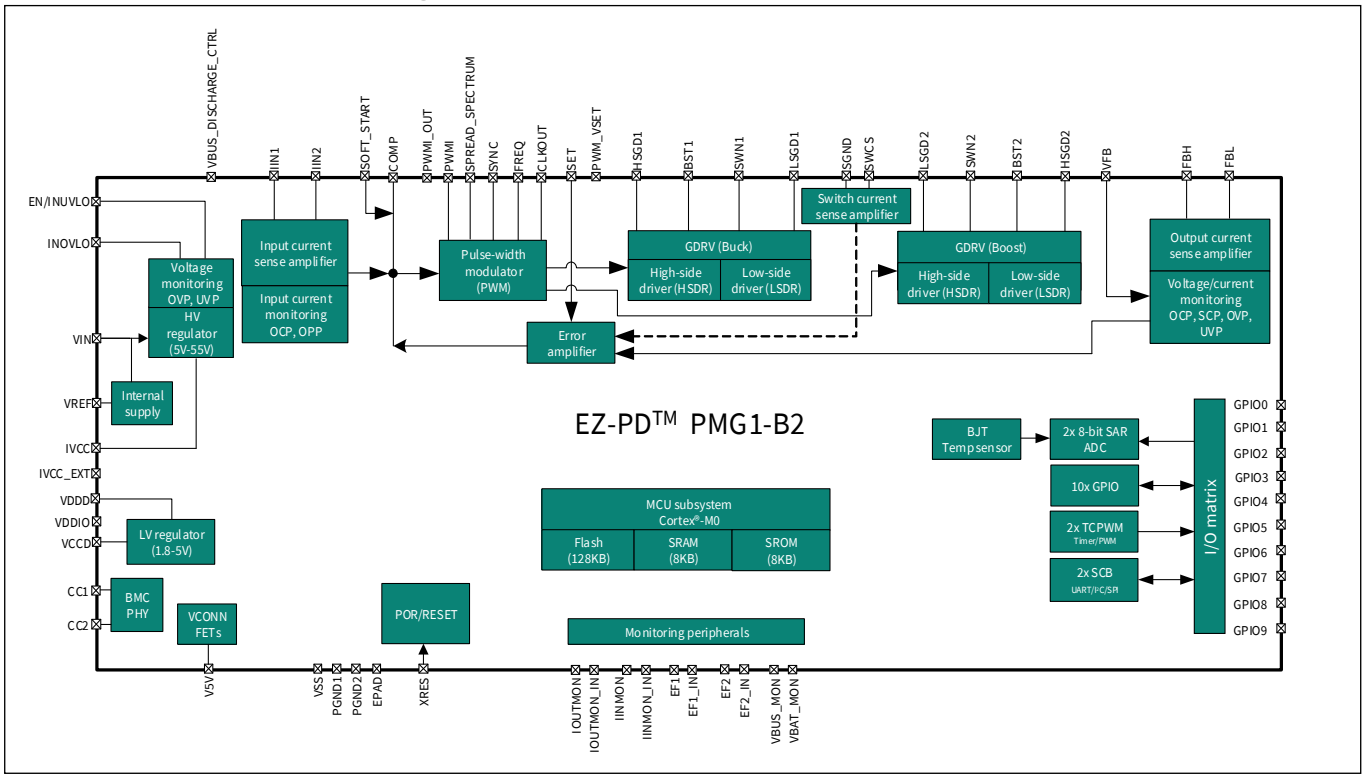
Features

- **Buck-boost controller with battery charging**
  - 1 to 12-cell Lithium-ion battery charging
  - Battery voltage and current monitoring
  - Constant current (CC) mode charging with current accuracy of +/- 3%
  - Configurable charging modes and safety timers
  - 200 kHz to 700 kHz switching frequency
  - Integrated 4x NFET gate-drivers for buck-boost operation
  - 4.5 V to 55 V input
  - Output voltage range up to 55 V
  - Supports soft start
  - Spread spectrum frequency modulation to improve the EMI performance
  - Supports analog current feedback control system
  - Input overvoltage and undervoltage lockout
  - Output overvoltage (OVP) and short-circuit protection (SCP)
  - Open load detection
  - Thermal shutdown
- **Type-C and USB Power Delivery (PD)**
  - USB-IF certified (TID: 15406)
  - Configurable termination resistors R_P, R_D, and $R_{D\text{-}db}$ (dead-battery R_D)
  - Supports one USB-C PD port compliant to USB PD specification R3.2 V1.2, Type-C specification V2.5
  - 1x Integrated USB PD BMC transceiver
  - 2x VCONN FETs
  - Supports USB PD EPR up to 240 W
  - Supports PPS Sink mode
  - Supports VBUS overvoltage protection (OVP)

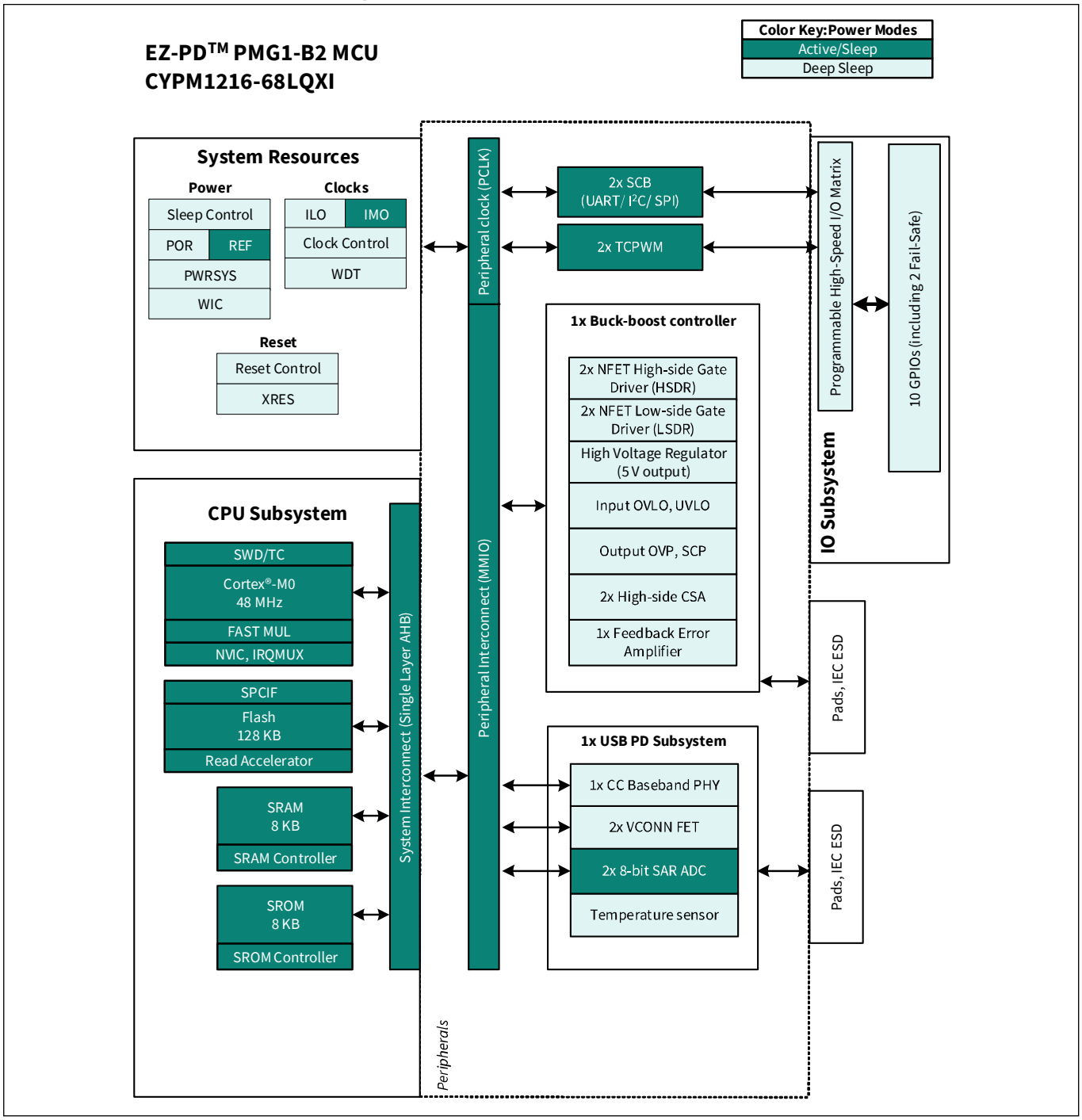
Features

- **32-bit MCU subsystem**
  - 48 MHz Arm® Cortex®-M0 CPU
  - 128 KB flash
  - 8 KB SRAM
- **Peripherals and I/Os**
  - 10x GPIOs including two Fail-Safe GPIOs
  - 9x fixed-function I/O pins
  - 2x 8-bit ADC
  - 2x 16-bit Timer/Counter/PWMs (TCPWM)
  - 2x Serial Communication Blocks (SCB) – UART/I^2C/SPI
- **Clocks and oscillators**
  - Integrated 48 MHz oscillator eliminating the need for an external clock
- **Power supply**
  - 4.5 to 55 V input
  - Integrated 5 V LDO
- **Packages**
  - 68-pin QFN
- **System-level ESD protection**
  - ± 8 kV contact discharge and ±15 kV air-gap discharge based on IEC61000-4-2 level 4C, on CC1 and CC2 pins

Functional block diagram



Architecture block diagram



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1 Pinout

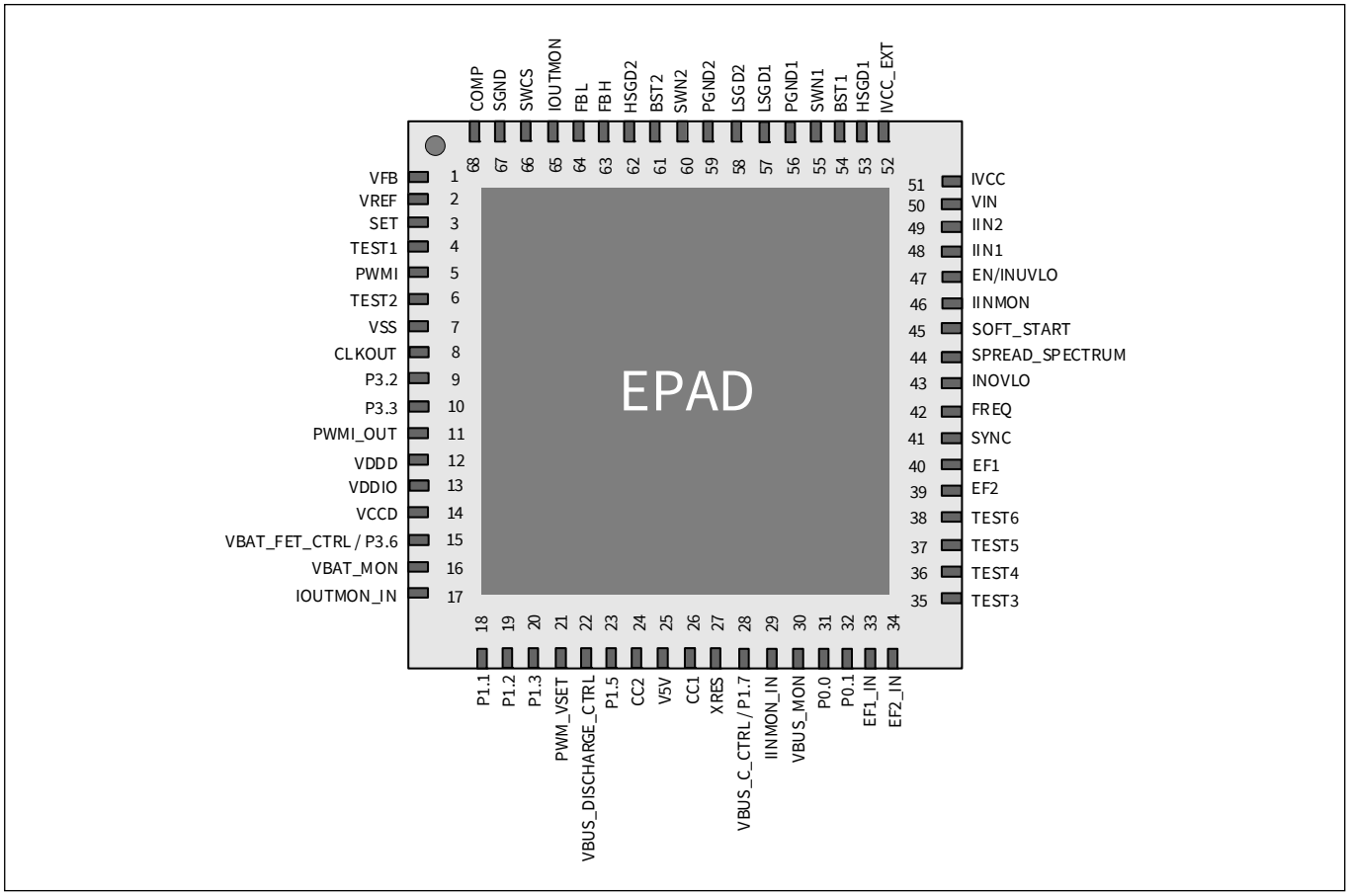


Figure 1 68-QFN pinout

Pinout

Table 1 68-QFN package pin list

Pin #	Pin name	Absolute minimum (V)	Absolute maximum (V)	Input/ output	Description
1	VFB	–0.3	5.5	Input	Output voltage monitor signal
2	VREF	–0.3	6	Output/ PD[1]	Voltage reference output pin; bypass with external 100 nF capacitor
3	SET	–0.3	5.5	Input	Analog reference signal input pin to set the output current
4	TEST1	–	–	–	Test pin
5	PWMI	–0.3	5.5	Input/ PD[1]	Active HIGH control input to start the buck/boost switching
6	TEST2	–	–	–	Test pin
7	VSS	–	–	–	Digital logic ground
8	CLKOUT	–0.3	5.5	Output	Clock output pin for buck-boost PWM
9	P3.2	–0.5	VDDIO + 0.5	Input/ Output	SCB3 /GPIO
10	P3.3	–0.5	VDDIO + 0.5	Input/ Output	SCB3 /GPIO
11	PWMI_OUT	–0.5	VDDIO + 0.5	Output	Enable signal for buck-boost controller from MCU
12	VDDD	–	6	–	VDDD supply for chip
13	VDDIO	–	6	–	1.71 V to 5.5 V supply for I/Os
14	VCCD	–	–	–	1.8 V regulator output for filter capacitor. This pin cannot drive external load
15	P3.6/VBAT_FET_CTRL	–0.5	VDDIO + 0.5	Output	GPIO/Battery charging path FET control
16	VBAT_MON	–0.5	VDDIO + 0.5	Input	Battery voltage monitoring
17	IOUTMON_IN	–0.5	VDDIO + 0.5	Input	Output current monitoring signal to MCU
18	P1.1	–0.5	VDDIO + 0.5	Input/ Output	GPIO/TCPWM output line
19	P1.2	–0.5	VDDIO + 0.5	Input/ Output	GPIO
20	P1.3	–0.5	VDDIO + 0.5	Input/ Output	GPIO
21	PWM_VSET	–0.5	VDDIO + 0.5	Output	PWM reference signal from MCU for buck-boost output current control
22	VBUS_DISCHARGE_CTRL	–0.5	VDDIO + 0.5	Output	VBUS discharge FET control signal

Note

1. PD: Pull-down circuit integrated

Table 1 68-QFN package pin list *(continued)*

Pin #	Pin name	Absolute minimum (V)	Absolute maximum (V)	Input/ output	Description
23	P1.5	–0.5	VDDIO + 0.5	Input/ Output	GPIO
24	CC2	–0.5	6	Input/ Output	USB PD connector detect/Configuration Channel 2
25	V5V	–	6	–	2.7 V to 5.5 V supply for VCONN FET of Type-C port
26	CC1	–0.5	6	Input/ Output	USB PD connector detect/Configuration Channel 1
27	XRES	–0.5	VDDIO + 0.5	–	Reset input (active LOW)
28	P1.7/VBUS_C_CTRL	–0.5	VDDIO + 0.5	Output	GPIO/VBUS consumer path FET control
29	IINMON_IN	–0.5	VDDIO + 0.5	Input	Input current monitoring signal to MCU
30	VBUS_MON	–0.5	VDDIO + 0.5	Input	VBUS voltage monitor signal input to the MCU
31	P0.0	–0.5	VDDIO + 0.5	Input/ Output	GPIO/SCB0/SWD data/Fail-Safe GPIO
32	P0.1	–0.5	VDDIO + 0.5	Input/ Output	GPIO/SCB0/SWD clock/Fail-Safe GPIO
33	EF1_IN	–0.5	VDDIO + 0.5	Input	Error Flag 1 input to MCU
34	EF2_IN	–0.5	VDDIO + 0.5	Input	Error Flag 2 input to MCU
35	TEST3	–	–	–	Test pin
36	TEST4	–	–	–	Test pin
37	TEST5	–	–	–	Test pin
38	TEST6	–	–	–	Test pin
39	EF2	–0.3	5.5	Output	Error Flag 1 for output protection
40	EF1	–0.3	5.5	Output	Error Flag 2 for output protection
41	SYNC	–0.3	5.5	Input	Synchronization input for buck-boost PWM clock
42	FREQ	–0.3	3.6	Input	Frequency select input
43	INOVLO	–0.3	5.5	Input	Input overvoltage lockout
44	SPREAD_SPECTRUM	–0.3	5.5	Input/ PD[1]	Spread spectrum enable pin
45	SOFT_START	–0.3	3.6	Output	Soft start configuration pin
46	IINMON	–0.3	3.6	Output	Input current monitoring signal

Note

1. PD: Pull-down circuit integrated

Table 1 68-QFN package pin list *(continued)*

Pin #	Pin name	Absolute minimum (V)	Absolute maximum (V)	Input/ output	Description
47	EN/INUVLO	–0.3	60	Input/ PD[1]	Enable/input undervoltage lockout
48	IIN1	–0.3	60	Input	Input current sense positive
49	IIN2	–0.3	60	Input	Input current sense negative
50	VIN	–0.3	60	–	Input power supply voltage
51	IVCC	–0.3	6	–	Internal LDO output; bypass with external capacitor
52	IVCC_EXT	–0.3	6	–	External 5 V supply input
53	HSGD1	–0.3	5.5	Output	High side gate driver output 1
54	BST1	–0.3	65	Input/ Output	Bootstrap capacitor 1
55	SWN1	–1	60	Input/ Output	Switch node 1
56	PGND1	–0.3	0.3	–	Power ground
57	LSGD1	–0.3	5.5	Output	Low-side gate driver output 1
58	LSGD2	–0.3	5.5	Output	Low-side gate driver output 2
59	PGND2	–0.3	0.3	–	Power ground
60	SWN2	–1	60	Input/ Output	Switch node 2
61	BST2	–0.3	65	Input/ Output	Bootstrap capacitor 2
62	HSGD2	–0.3	5.5	Output	High-side gate driver output 2
63	FBH	–0.3	60	Input	Output current feedback positive
64	FBL	–0.3	60	Input	Output current feedback negative
65	IOUTMON	–0.3	5.5	Output	Output current monitoring signal
66	SWCS	–0.3	0.3	Input	Inductor current-sense input
67	SGND	–0.3	0.3	Input	Inductor current-sense ground
68	COMP	–0.3	3.6	Output	Compensation network pin
-	EPAD	–	–	–	Chip ground and thermal pad

Note

1. PD: Pull-down circuit integrated

2 Functional overview

2.1 MCU subsystem

2.1.1 CPU

The Arm® Cortex®-M0 core in EZ-PD™ PMG1-B2 device is a 32-bit MCU, which is optimized for low-power operation with extensive clock gating. It primarily uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. It also includes a hardware multiplier, which provides a 32-bit result in one cycle. Additionally, it includes an interrupt controller (the NVIC block) with 32 interrupt inputs and a wakeup interrupt controller (WIC), which can wake the processor up from Deep Sleep mode.

2.1.2 Flash

The EZ-PD™ PMG1-B2 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver two wait-states (WS) access time at 48 MHz and with 0-WS access time at 16 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

2.1.3 SRAM

The device provides 8 KB SRAM that is used under software control to store the temporary status of system variables and parameters.

2.1.4 SROM

The device consists of a supervisory ROM that contains boot and configuration routines.

2.2 USBPD subsystem

This subsystem provides the interface to the USB-C port. This subsystem comprises of the following:

- USB PD physical layer
- VCONN switches

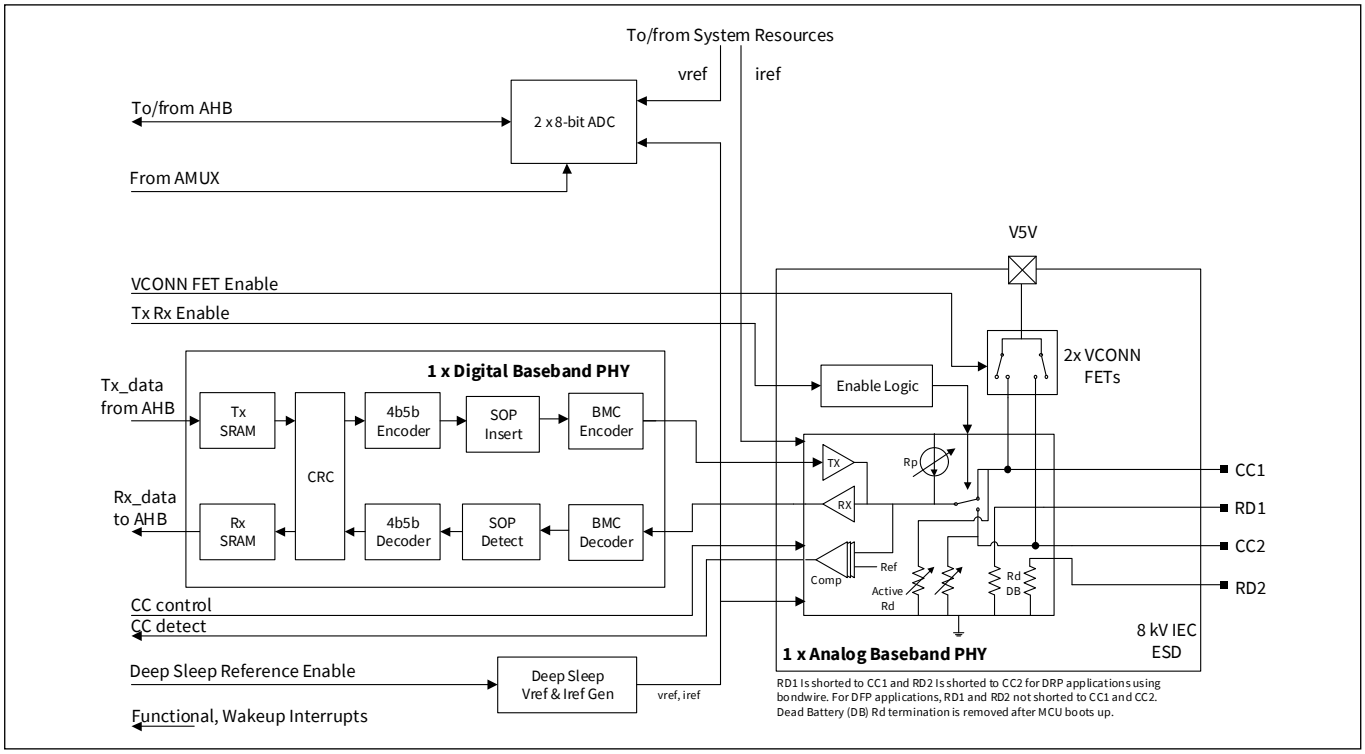


Figure 2 USB PD subsystem

2.2.1 USB PD physical layer

The USB PD subsystem contains the USB PD physical layer block and supporting circuits. The USB PD physical layer consists of a transmitter and receiver that communicate using bi-phase mark coding (BMC) encoded data over the CC channel, per the PD 3.2 standard. All communication is half-duplex. The physical layer or PHY implements collision avoidance to minimize communication errors on the channel. The USB PD block includes all termination resistors (R_P and R_D and dead-battery resistor ($R_{D\text{-}db}$)) and their switches as required by the USB Type-C specifications. R_P and R_D resistors are required to implement connection detection, plug orientation detection and for the establishment of the USB source/sink roles. The R_P resistor is implemented as a current source. The dead-battery termination ($R_{D\text{-}db}$) is used in an unpowered sink to help the source to detect it.

The EZ-PD™ PMG1-B2 device family along with the accompanying firmware is fully compliant with revision 3.2 of the USB power delivery specification.

The EZ-PD™ PMG1-B2 device support USBPD extended messages containing data of up to 260 bytes. The extended messages are larger than expected by USB PD 2.0 hardware. As per the USBPD protocol specification, USBPD 3.1 compliant devices implement a chunking mechanism; messages are limited to revision 2.0 sizes unless both source and sink confirm and negotiate compatibility with longer message lengths.

2.2.2 VCONN switches

EZ-PD™ PMG1-B2 has integrated 2x VCONN FETs which support a minimum of 1 W for powering EMCA cables. These switches help to route the 5 V supply from V5V pin to one of the CC pins, based on the cable orientation as detected through the firmware.

2.3 Buck-boost controller

The EZ-PD™ PMG1-B2 device has an integrated buck-boost controller that supports up to 55 V output voltage. It has an integrated 5 V LDO that can provide a total of 90 mA of current. This block has internal current sense amplifiers and an error amplifier with compensation, which is used for the feedback loop to implement output current regulation. Besides, it also provides features such as soft-start for limiting the inrush current, and spread-spectrum to reduce noise due to EMI. Various faults like overvoltage, undervoltage, open-load, and short-circuit are handled and error flags are triggered.

2.3.1 Control system overview

The control system includes all of the functions necessary to provide constant current to the output, which is commonly used in a battery charging application, as shown in **Figure 3**. It is designed to control four gate-driver outputs in a H-bridge topology, utilizing a single inductor and four external MOSFETs. This topology is able to operate in high power BOOST, BUCK-BOOST, and BUCK mode applications with maximum efficiency. The transition between the different control modes is done automatically by the device itself, with respect to the application boundary conditions. The transition phase between modes is seamless.

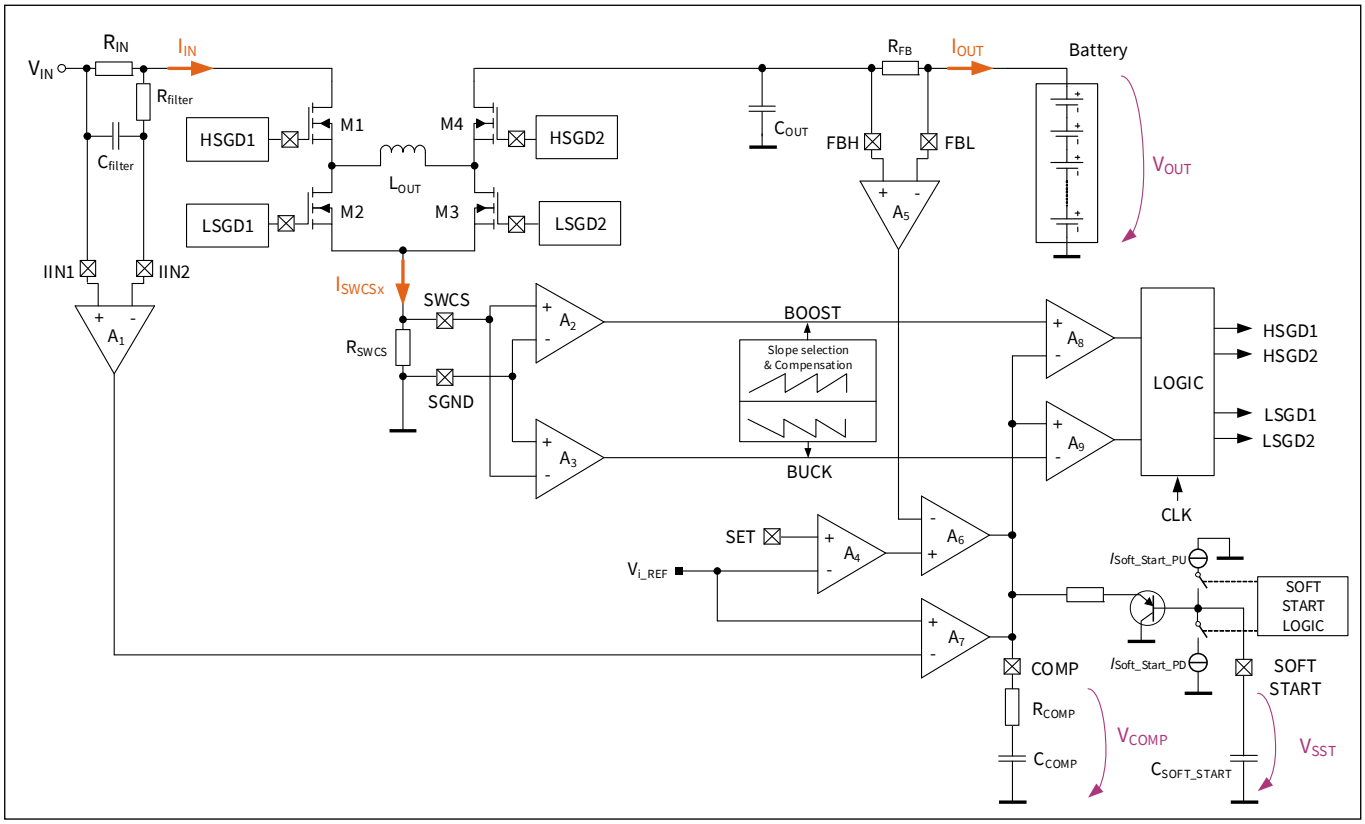


Figure 3 Buck-boost control system block diagram

2.3.1.1 Control loop operation

- The buck-boost controller includes two analog current control inputs (IIN1, IIN2) to limit the maximum input current (block A1 and A7 in **Figure 3**)
- A second analog current control loop (A5, A6 with total gain = $IFBx_{gm}$) connected to the sensing pins FBL, FBH regulates the output current
- The regulator function is implemented by a pulse width modulated (PWM) current mode controller. The error in the output current loop is used to determine the appropriate duty cycle to get a constant output current
- An external compensation network (R_{COMP}, C_{COMP}) is used to adjust the control loop to various application boundary conditions
- The inductor current for the current mode loop is sensed by the R_{SWCS} resistor. R_{SWCS} is used also to limit the maximum external switches/inductor current. If the voltage across R_{SWCS} exceeds its overcurrent threshold (V_{SWCS_buck} or V_{SWCS_boost} for buck or boost operation respectively) the device reduces the duty cycle in order to bring the switches current below the imposed limit
- The current mode controller has a built-in slope compensation as well to prevent sub-harmonic oscillations
- The control loop logic block (LOGIC) provides a PWM signal to four internal gate drivers. The gate drivers (HSGD1,2 and LSGD1,2) are used to drive external MOSFETs in an H-bridge setup. Once the soft-start expires, a forced CCM regulation mode is performed
- The control loop block diagram displayed in **Figure 3** shows a typical constant current application. The voltage across R_{FB} sets the output current. R_{IN} is used to fix the maximum input current

Note The device provides flexible current sense option at the output to enable both high-side and low-side current sensing configurations. **Figure 3** shows R_{FB} shunt resistor connected between FBH and FBL pins for a high-side current sensing.

2.3.2 Adjustable soft start

EZ-PD™ PMG1-B2 provides soft-start ramp to mainly reduce inrush current during the buck-boost startup.

The soft-start routine has two functionalities:

- Fault management by setting fault mask and wait-before-retry time (**Figure 4**)
- Limit input inrush current and output overshoots by limiting V_{COMP} (**Figure 3**) in the Boost mode

The soft-start routine is applied:

- At first turn ON (first PWMI rise after EN/INUVLO = HIGH)
- After output short to GND or open load detection
- After input overvoltage detection

The soft-start routine is active during the rising and falling edges of the V_{SST} (**Figure 3**). The soft-start timing is defined by a capacitor placed at the SOFT_START pin and the pull-up and pull-down current sources ($I_{SOFT\_START\_PU}$, $I_{SOFT\_START\_PD}$). The minimum value for soft-start capacitor has to be designed such that, during startup, the output voltage exceeds the short to ground threshold (VFB pin exceeds $V_{VFB\_S2G\_INC}$), before the soft-start voltage reaches $V_{SOFT\_START\_LOFF}$. The minimum temperature and minimum input voltage shall be considered as the worst-case condition for previously mentioned dimensioning.

Note In case of an overtemperature fault, the device will start up with a soft-start routine after the overtemperature condition disappears.

The soft-start rising edge time is approximately calculated in **Eq. 1**.

$$t_{SOFT\_START} = V_{SOFT\_START\_LOFF} \cdot \frac{C_{SOFT\_START}}{I_{SOFT\_START\_PU}} \quad \text{Eq. 1}$$

The soft-start routine limits the inrush current by clamping the COMP pin through a buffer as in **Figure 3**. Therefore, this functionality is effective only when soft-start capacitor is sufficiently larger than the COMP capacitor and its effect is visible mainly in buck-boost and boost regulation mode. If an open load or a short circuit on the output is detected, a pull-down current source $I_{SOFT\_START\_PD}$ (**P_6.4.20**) is activated. This current brings down the V_{SOFT_START} until $V_{SOFT\_START\_RESET}$ (**P_6.4.22**) is reached. Afterwards, the pull-up current source $I_{SOFT\_START\_PU}$ (**P_6.4.19**) turns on again. If the fault condition hasn't been removed until $V_{SOFT\_START\_LOFF}$ (**P_6.4.21**) is reached, the pull-down current source turns back on again, initiating a new cycle. During the soft-start rise time the device is switching, during fall time the device is halted (**Figure 4**). This hiccup mode will continue until the fault is removed. It is possible to latch the fault condition by sourcing a current higher than $I_{SOFT\_START\_PD}$, through a pull-up resistor connected from VREF to the SOFT_START pin. In this condition the device will restart regulating only if EN/INUVLO pin is toggled. If an input overvoltage is detected, the SOFT_START pin is kept low by discharging C_{SOFT_START} as long as the overvoltage remains.

At first PWMI rise after EN/INUVLO = HIGH, the internal PWM signal is extended until one of the two following conditions is reached:

- Until V_{SOFT_START} exceeds $V_{SOFT\_START\_LOFF}$
- Until $V_{FBH-FBL}$ exceeds $V_{FBH\_FBL\_OL}$

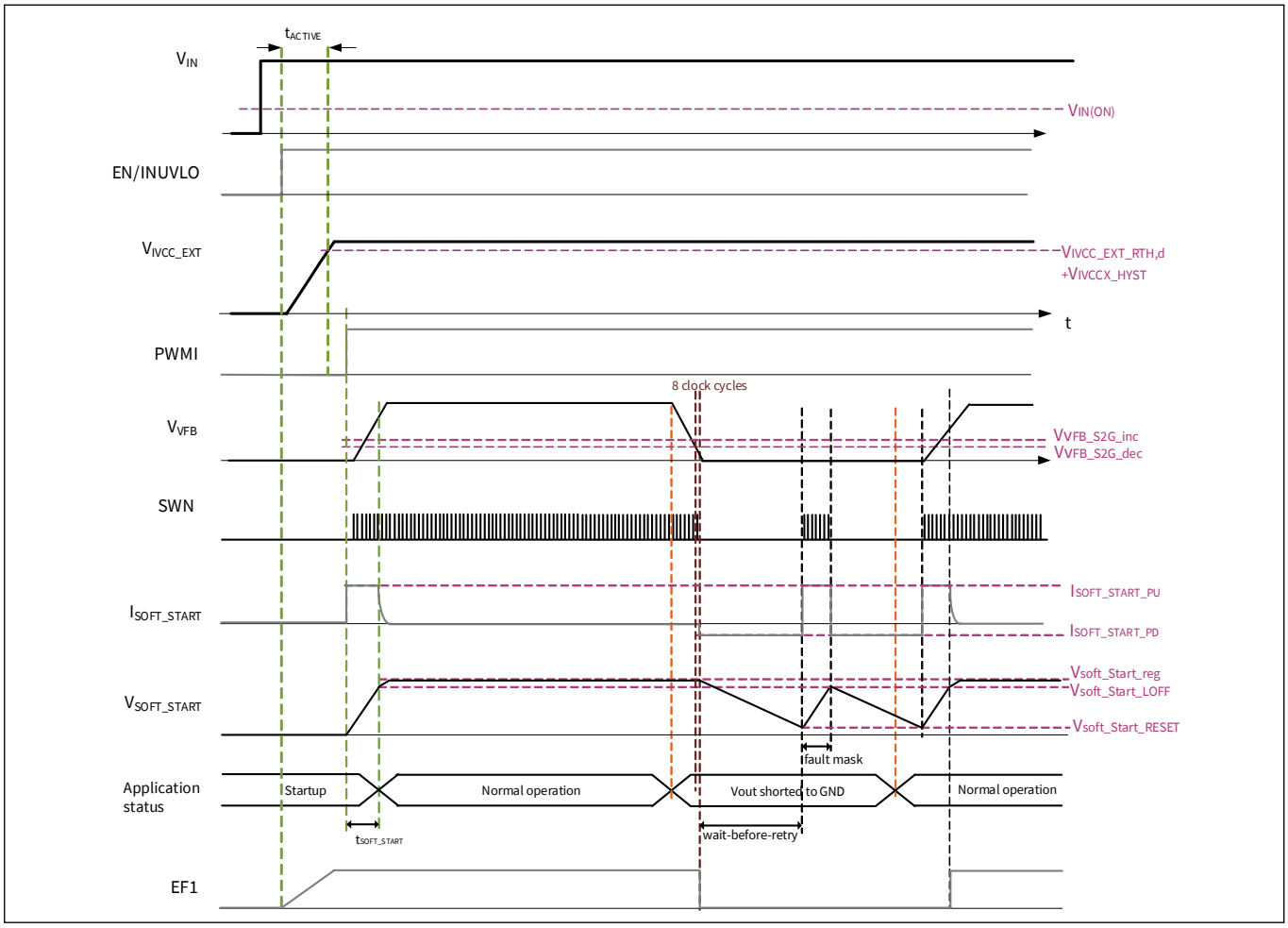


Figure 4 Soft start timing diagram on a short to ground detected by the VFB pin

2.3.3 Compensator design

The analog control loop for output current regulation can be tuned to get the required performance characteristics such as transient response and steady state response, as per the application requirements. This is achieved by connecting suitable RC network at the COMP pin of EZ-PD™ PMG1-B2, which forms the compensation network. Both time domain and frequency domain response of the system can be tuned using the compensation network. See **Figure 3** for more details.

2.3.3.1 Type-I compensator

Figure 5 shows the small-signal AC model of the feedback error amplifier using for deriving the transfer function of the compensator. Here, ro is the output impedance of the operational transconductance amplifiers (OTA) which is in the range of MΩ. R1 and C1 externally connected in series at COMP pin form the compensation network. IFBx$_{gm}$ is the total transconductance of OTAs in the output current control loop.

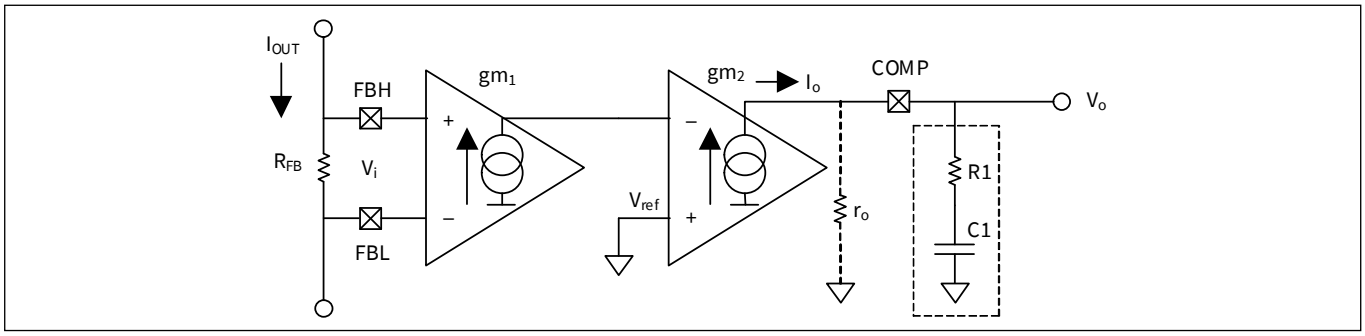


Figure 5 Type-I compensator

Consider the total transconductance of output current sense amplifiers as:

$$IFBx_{gm} = g_m = g_{m1} \cdot g_{m2} \quad \text{Eq. 2}$$

$$V_i(s) = I_{OUT}(s) \cdot R_{FB} \quad \text{Eq. 3}$$

The transfer function H(s) from the output current sense voltage to the compensation node is given as in **Eq. 4**:

$$H(s) = \frac{V_o(s)}{V_i(s)} = g_m \cdot \frac{(1 + sR_1C_1)}{sC_1} \quad \text{Eq. 4}$$

However, this transfer function is derived by considering an infinite output resistance (r_o) for the OTA. Practically, the pole is shifted from origin (0 Hz) due to the finite value of r_o. Therefore, a more accurate representation of the transfer is given in **Eq. 5**:

$$H(s) = \frac{V_o(s)}{V_i(s)} = (g_m \cdot r_o)\frac{(1 + sR_1C_1)}{[1 + s(r_o + R_1)C_1]} \quad \text{Eq. 5}$$

Generally, a Type-I compensator is sufficient for EZ-PD™ PMG1-B2 to achieve a stable current control loop with sufficient phase margin.

2.3.3.2 Type- II compensator

The Type-II compensator design uses an additional parallel capacitor C2 as shown in **Figure 6**, which results an additional pole in the control loop. This allows more flexibility to tune the response of the control loop compared to a Type-I compensator.

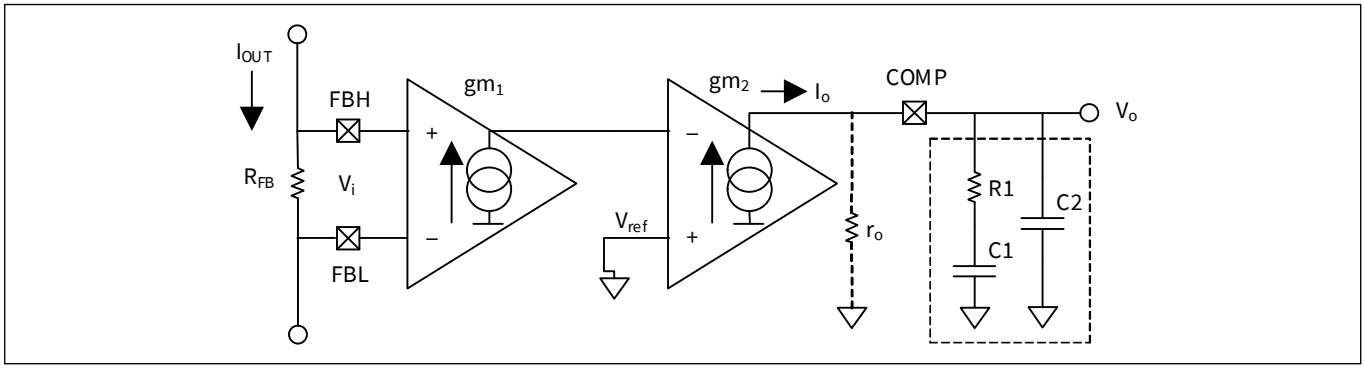


Figure 6 Type- II compensator

The ideal transfer function H(s) from the output current sense voltage to the compensation node is given as in **Eq. 6**:

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{g_m}{s(C_1 + C_2)} \cdot \frac{(1 + sR_1C_1)}{\left[1 + sR_1\left(\frac{C_1C_2}{C_1 + C_2}\right)\right]} \quad \text{Eq. 6}$$

Considering the finite output resistance (r_o) of the OTA a more accurate representation of the transfer is given in **Eq. 7**:

$$H(s) = \frac{V_o(s)}{V_i(s)} = (g_m \cdot r_o) \cdot \frac{(1 + sR_1C_1)}{[1 + s(R_1C_1 + r_o(C_1 + C_2)) + s^2(r_oR_1C_1C_2)]} \quad \text{Eq. 7}$$

In general, r_o of the OTA is very large (MΩ). Therefore, considering dominant pole analogy with r_o >> R1, the transfer function can be simplified as in **Eq. 8**:

$$H(s) = \frac{V_o(s)}{V_i(s)} = (g_m \cdot r_o) \cdot \frac{(1 + sR_1C_1)}{[1 + sr_o(C_1 + C_2)]\left[1 + sR_1\left(\frac{C_1C_2}{C_1 + C_2}\right)\right]} \quad \text{Eq. 8}$$

Note As the signal passes through the second OTA, it gets inverted as it enters the inverting input terminal. However, the negative sign in the transfer functions is omitted by considering it as a negative feedback introduced in the control loop.

Table 2 shows the expression for DC gain, poles and zeros of the compensator, which can be used to calculate the R and C component values.

Table 2 Compensator design

Parameter	Type-I compensator	Type- II compensator	Unit
DC gain	$g_m \cdot r_o$	$g_m \cdot r_o$	–
Pole frequency	$\frac{1}{2\pi(r_o + R_1)C_1}$	$\frac{1}{2\pi r_o(C_1 + C_2)}$	Hz
	–	$\frac{(C_1 + C_2)}{2\pi R_1 C_1 C_2}$	Hz
Zero frequency	$\frac{1}{2\pi R_1 C_1}$	$\frac{1}{2\pi R_1 C_1}$	Hz

Note **Figure 5** and **Figure 6** show only the control signal flow from output current sense amplifier to the compensation node. In reality, the compensation node voltage is also affected by the input current sense amplifier (A1 and A7 in **Figure 3**) which is used for input current limiting.

2.3.3.3 Control loop frequency response

Figure 7 shows the bode plot for loop gain of the control system with Type-I compensator for the parameters listed in **Table 3**. Approximately 100°of phase margin is achieved confirming the stability of the control system.

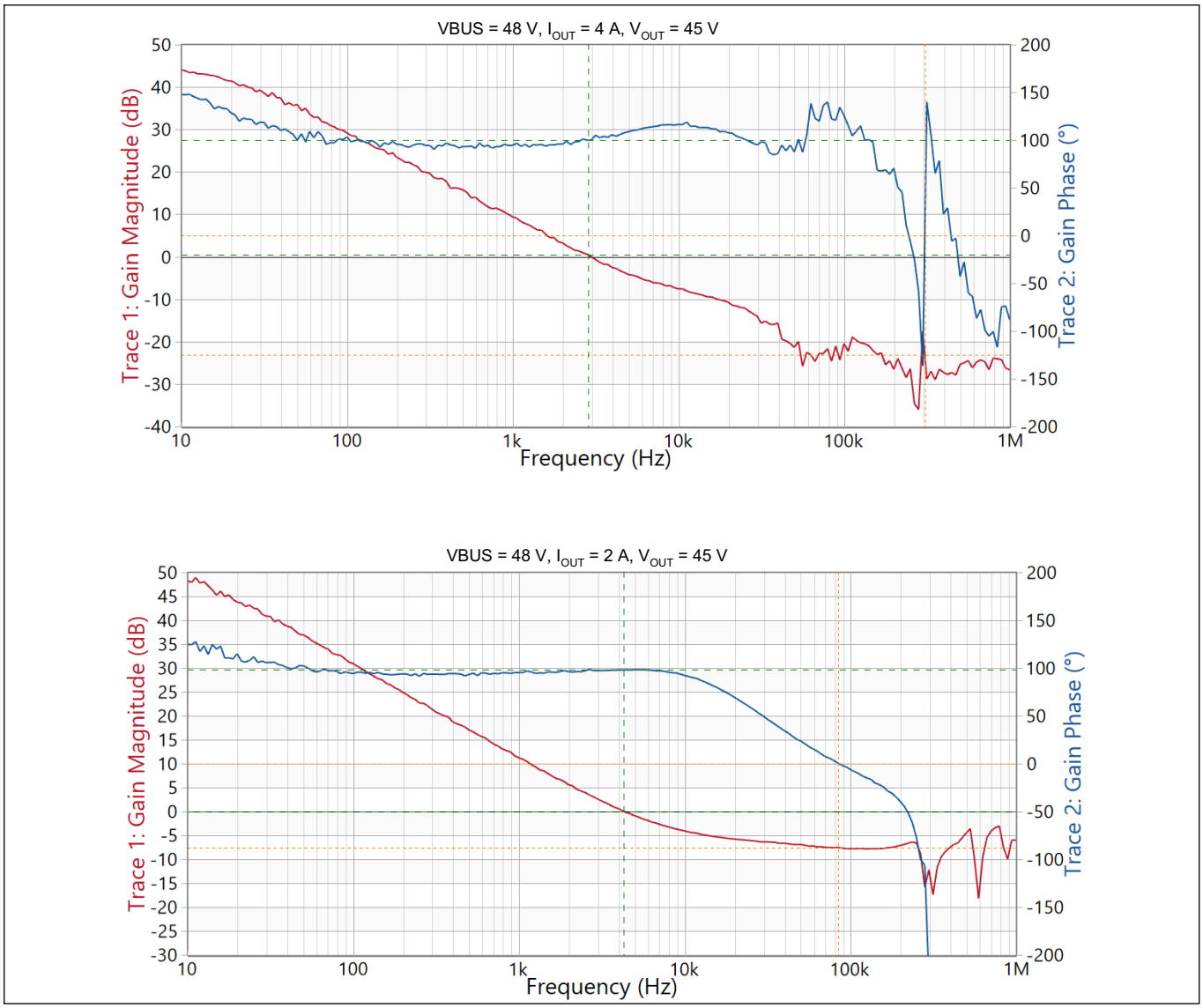


Figure 7 Bode plot for the current control loop

Table 3 System design parameters

Parameter	Value
Type-I compensator - R1	0 Ω
Type-I compensator - C1	22 nF
Buck-boost switching frequency (F_{SW})	280 kHz

2.3.4 Output current control

EZ-PD™ PMG1-B2 provides feasibility to control the output current of the buck-boost converter in constant current mode operation. The two pins which provide the complete control of the buck-boost output are PWMI and SET pins.

2.3.4.1 Buck-boost ON/OFF

The PWMI pin of the device is used to start/stop the buck/boost operation of the controller. Setting the PWMI pin HIGH turns on the power stages of the buck-boost controller to start the switching operation.

The PWMI_OUT pin should be externally connected to the PWMI pin of EZ-PD™ PMG1-B2 to enable to firmware control of buck-boost switching operation by the MCU.

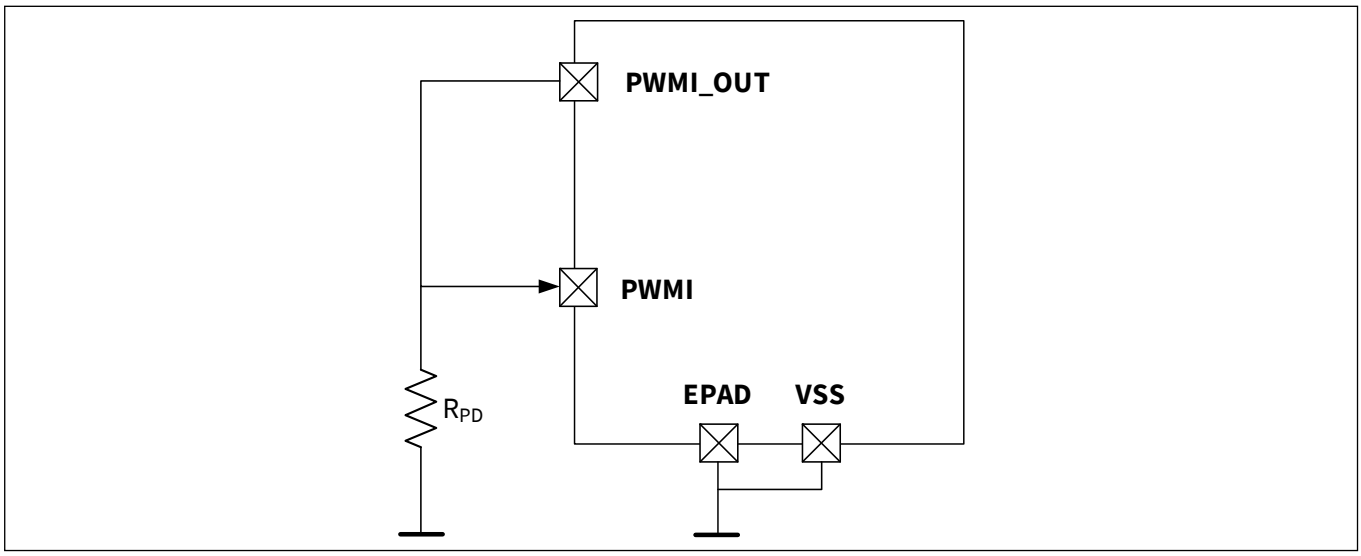


Figure 8 Buck-boost output control using PWMI pin

Note The soft-start feature in EZ-PD™ PMG1-B2 controller is not linked to PWMI signal alone. Therefore, to avoid unwanted output overshoots due to no soft-start assisted startups, PWMI signal in LOW state should not be used to suspend the output current for long time intervals. To stop in a safe manner, EN/INUVLO=LOW should be used.

2.3.4.2 Analog current control

The analog control feature allows a linear control of the output current. This approach is used to control the output current based on an analog reference input voltage applied at SET pin of EZ-PD™ PMG1-B2 controller. The analog control feature adjusts the average load current level via the control of the feedback error amplifier voltage ($V_{FBH-FBL}$). The SET pin is used to adjust the mean output current. The range of V_{SET} input voltage where analog control is enabled is from 0.2 V to 1.5 V, with an almost linear relation throughout this range as shown in **Figure 4**. The output current is directly proportional to the feedback voltage $V_{FBH-FBL}$.

- **Output current vs. SET pin voltage**

The output current I_{OUT} is related to the feedback voltage $V_{FBH-FBL}$ and the feedback shunt resistor R_{FB} as in **Eq. 9**.

$$I_{OUT} = \frac{V_{FBH} - V_{FBL}}{R_{FB}} \quad \text{Eq. 9}$$

The relation between the average output current (I_{OUT}) and the voltage at the SET pin (V_{SET}) between 0.2 V and 1.4 V is mathematical expressed in **Eq. 10**. When the output current is controlled by the firmware using PWM signal from PWM_VSET pin, the relation between the output current and PWM duty cycle is expressed in **Eq. 11**.

$$I_{OUT} = \frac{V_{SET} - 0.2}{8 \cdot R_{FB}} \quad \text{Eq. 10}$$

$$I_{OUT} = \frac{duty_{PWM} \cdot V_{DDD} - 0.2}{8 \cdot R_{FB}} \quad \text{Eq. 11}$$

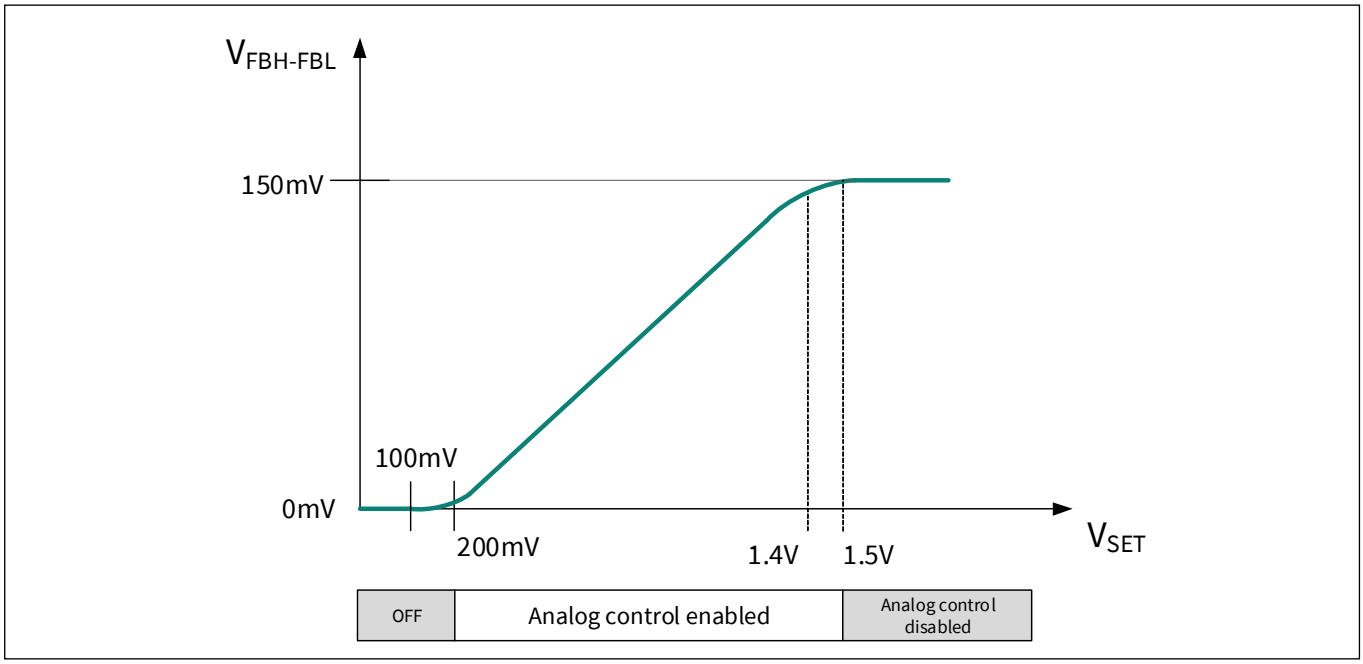


Figure 9 Analog current control using reference input voltage

Note If V_{SET} is 200 mV (typical), the output current is only determined by the internal offset voltages of the comparators. Therefore, to assure the switching activity is stopped and $I_{OUT} = 0$, V_{SET} has to be < 100 mV as shown in **Figure 4**.

Use cases for the analog control pin (SET):

1. Connecting an external voltage divider circuit between VREF (accurate regulated supply output), SET, and GND pins allows for a fixed, hardware-based output current referencing
2. Optionally, a temperature sensitive resistor (thermistor) can be connected in the voltage divider network to protect the load from thermal destruction. This is achieved by automatically adjusting the load current-based on the change in temperature, independent of the microcontroller. The value of the series resistor R_{SET1} of the voltage divider must be set such that the V_{SET} voltage remains within the range of 0.2 V to 1.5 V for the entire operating temperature range, as shown in **Figure 4**
3. If the analog control feature is not needed, connect the SET pin to the VREF pin with an RC filter as shown in **Figure 10**
4. If firmware control of output current is required, EZ-PD™ PMG1-B2 provides a PWM signal from PWM_VSET pin through an external RC filter to produce an analog voltage at SET pin for the analog current control. The voltage level depends on the PWM frequency (f_{PWM}) and duty cycle which can be controlled by the EZ-PD™ PMG1-B2 firmware

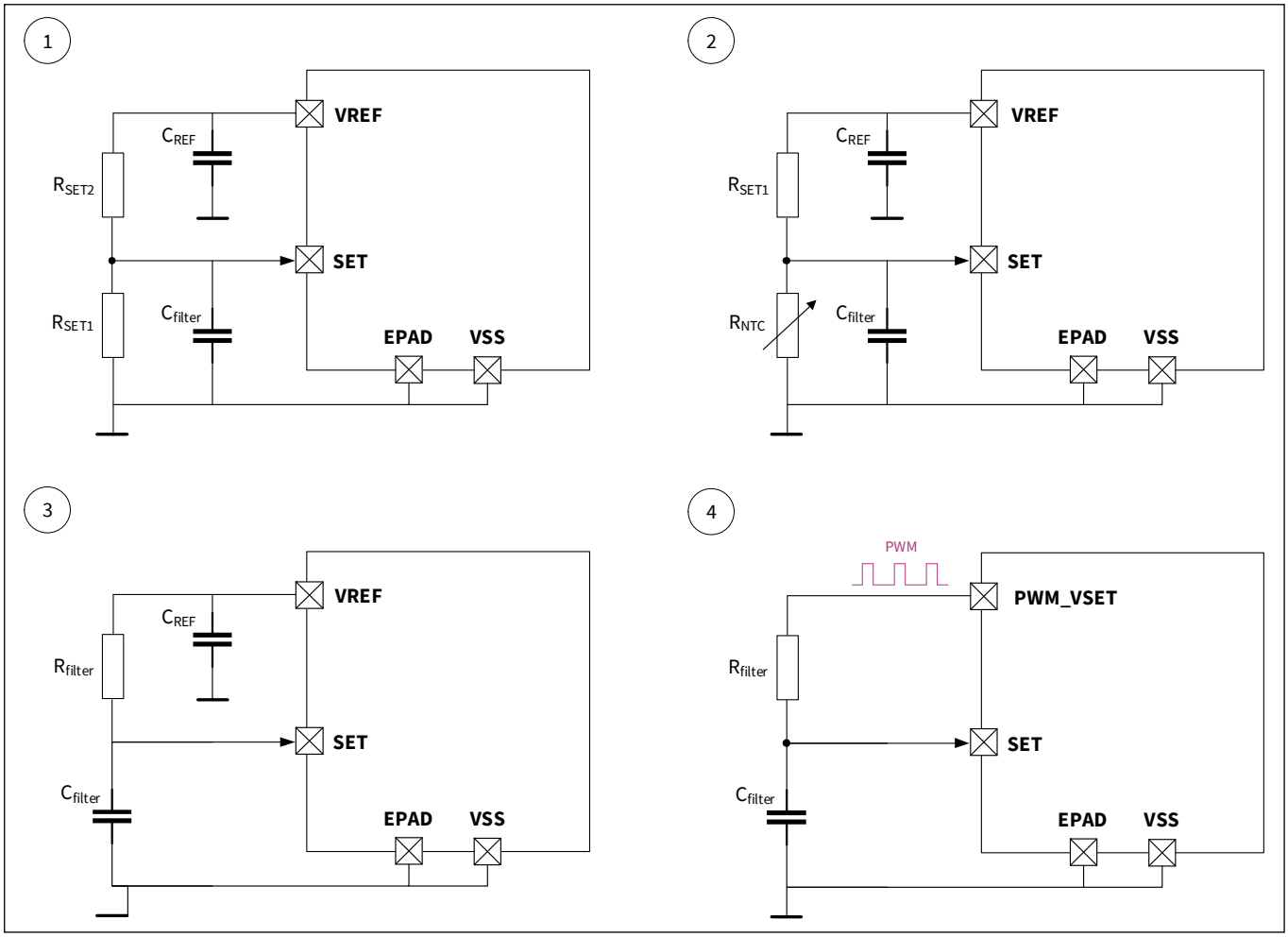


Figure 10 Use cases for analog control pin SET

2.3.5 Buck-boost operating modes

The EZ-PD™ PMG1-B2 device supports synchronous operation in the following three different modes:

- Boost mode
- Buck mode
- Buck-boost mode

The controller automatically manages the transition between these operating modes. The synchronous switching helps in achieving maximum efficiency with minimum conduction loss compared to the traditional synchronous switching by conduction through body diode of the MOSFETs (I^2 x R_{DSON} vs. 0.7 V x I).

The inductor L_{OUT} connects in an H-bridge configuration with four external N-channel MOSFETs (M1, M2, M3, M4) as shown in **Figure 11**. **Table 4** lists the switching states of four MOSFETs in different operating modes.

- Transistor M1 and M3 provides a path between V_{IN} and ground through L_{OUT} in one direction (driven by top and bottom gate drivers HSGD1 and LSGD2)
- Transistor M2 and M4 provides a path between V_{OUT} and ground through L_{OUT} in the other direction (driven by top and bottom gate drivers HSGD2 and LSGD1)
- Nodes SWN1, SWN2, voltage across R_{SWCS}, input and load currents are also monitored by the device

Table 4 Switching status of H-bridge MOSFETs based on operating modes

MOFSET	Boost mode	Buck-boost mode	Buck mode
M1	ON	PWM	PWM
M2	OFF	PWM	PWM
M3	PWM	PWM	OFF
M4	PWM	PWM	ON

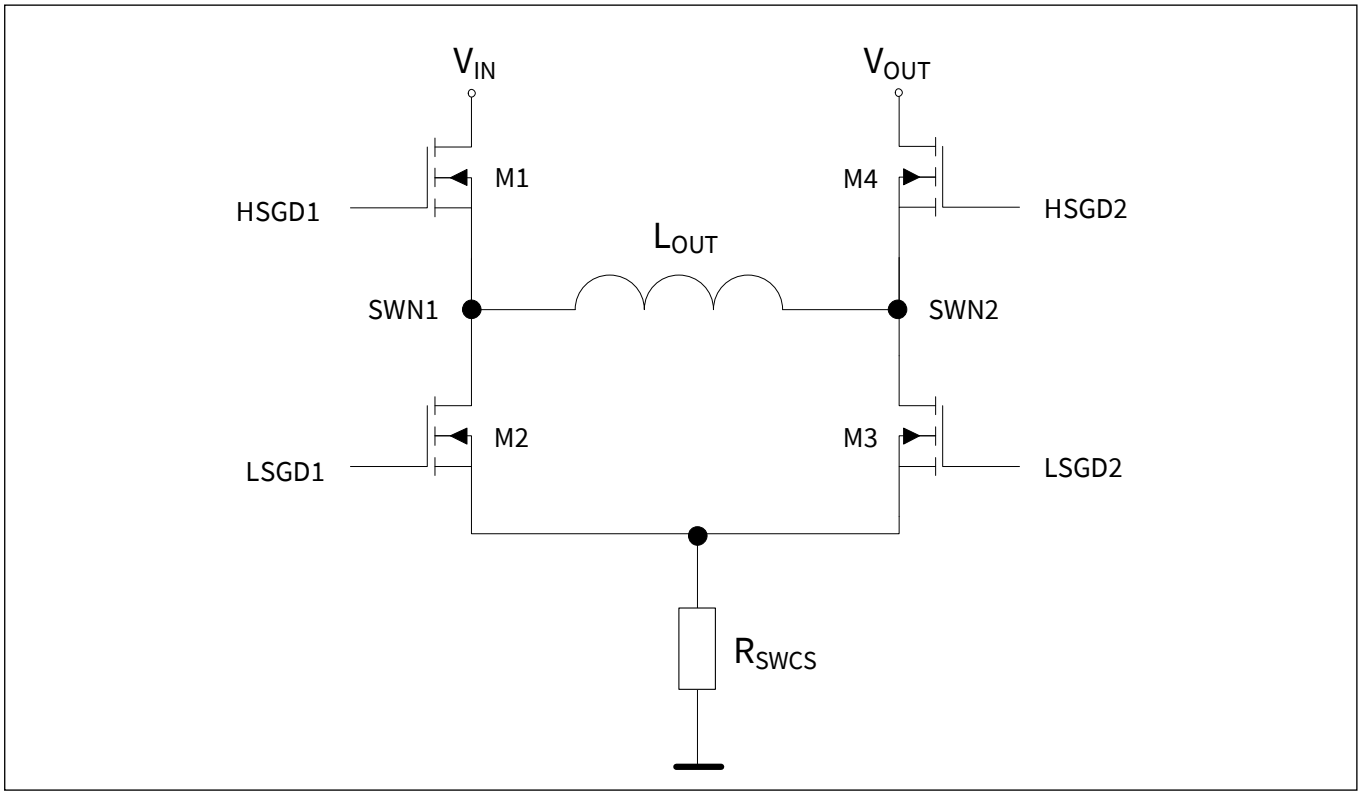


Figure 11 Buck-boost H-bridge architecture

- **Boost mode ($V_{OUT} > V_{IN}$)**
  - M1 is always ON, and M2 is always OFF
  - At the start of each cycle, M3 turns ON first and inductor current is sensed (peak current control). M3 stays ON until the upper reference threshold is reached across R_{SWCS} (Energizing)
  - M3 turns OFF, and M4 turns ON until the end of the cycle (Recirculation)
  - M3 and M4 switches alternatively with PWM control, behaving like a typical synchronous boost regulator (see **Figure 12**)

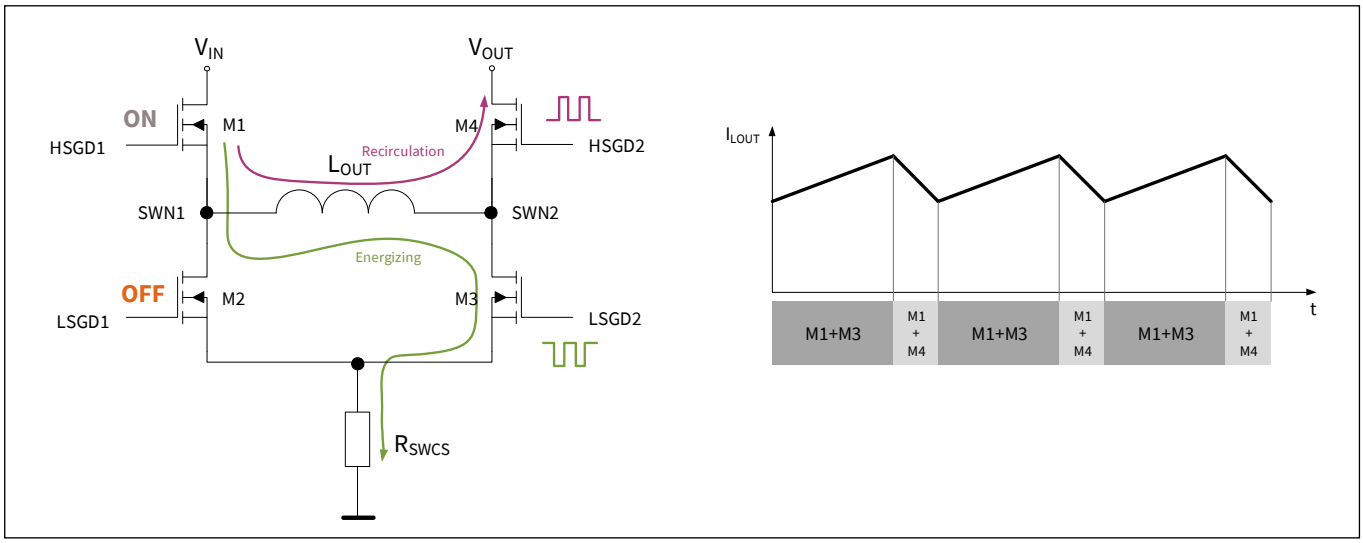


Figure 12 Boost mode operation of H-bridge MOSFETs

- **Buck mode ($V_{OUT} < V_{IN}$)**
  - M4 is always ON, and M3 is always OFF
  - At the start of each cycle, M2 turns ON first and inductor current is sensed (valley current control)
  - M2 stays ON until the lower reference threshold is reached across R_{SWCS} (Recirculation)
  - M2 turns OFF, and M1 turns ON until the end of the cycle (Energizing)
  - M1 and M2 switches alternatively with PWM control, behaving like a typical synchronous buck regulator (see **Figure 13**)

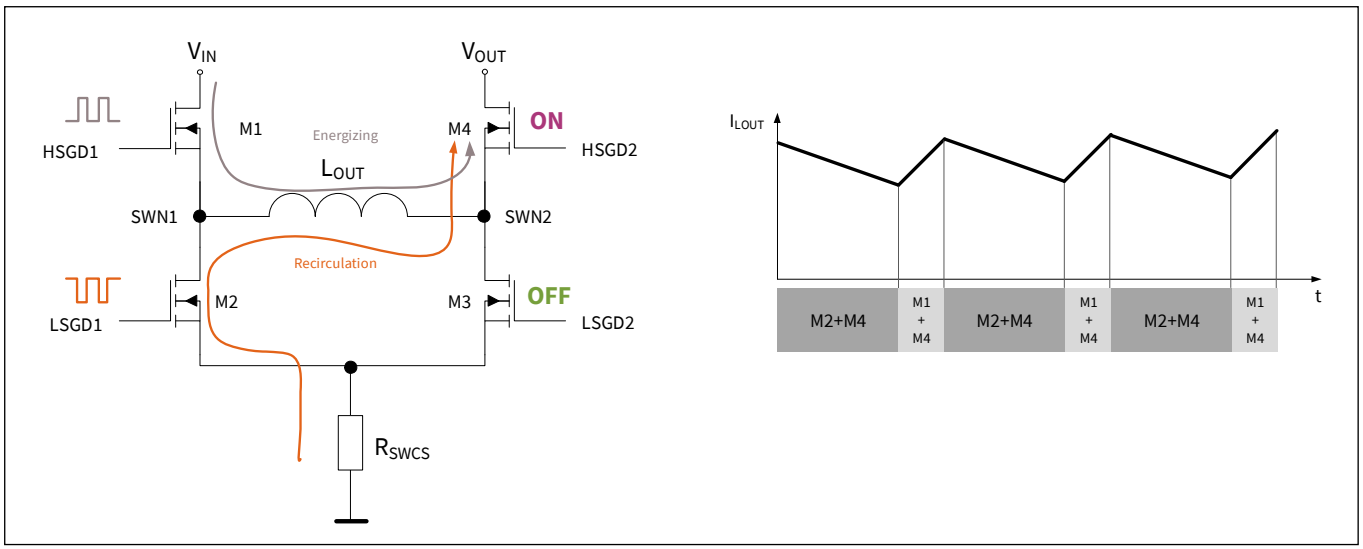


Figure 13 Buck mode operation of H-bridge MOSFETs

- **Buck-boost mode (V_{OUT} ~ V_{IN})**
  - When V_{IN} is close to V_{OUT} the controller operates in buck-boost mode
  - All MOSFETs are switching in buck-boost operation with PWM control. The direct energy transfer from the input to the output (M1, M4 = ON) is beneficial to reduce ripple current and improves the energy efficiency of the buck-boost control scheme
  - The waveforms for two cases of buck-boost operation, and switching behaviors are displayed in **Figure 14**

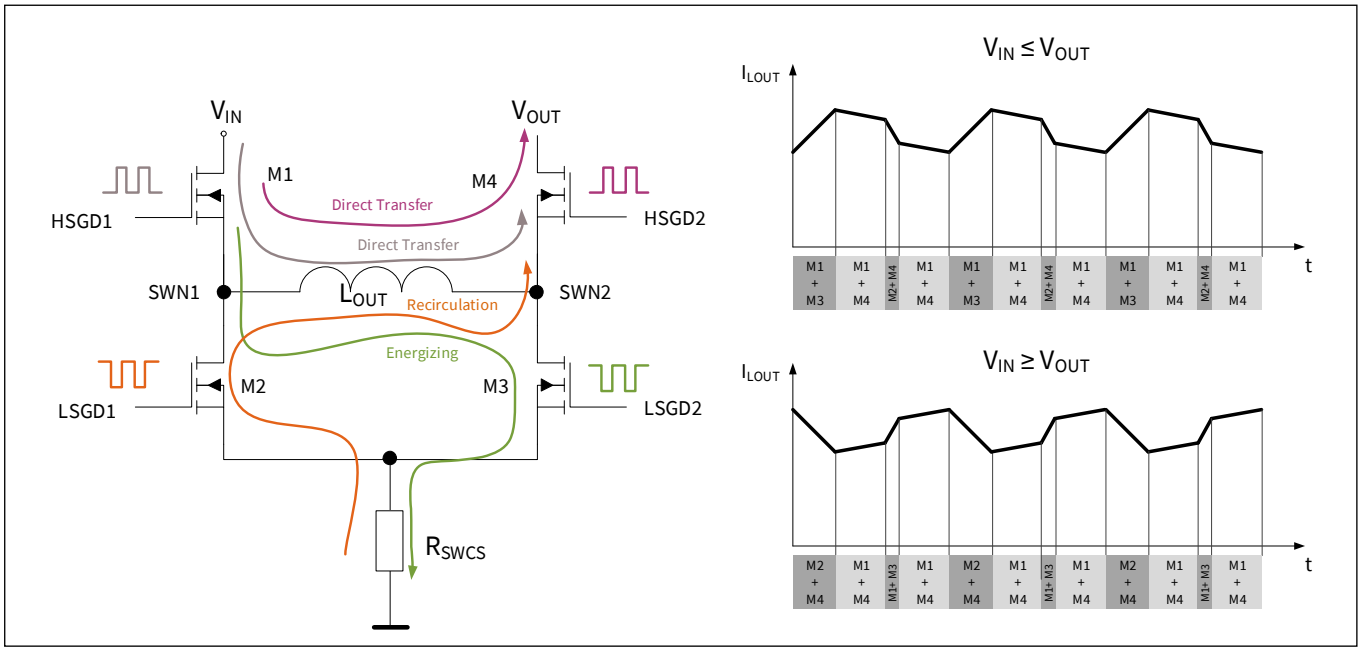


Figure 14 Buck-boost mode operation of H-bridge MOSFETs

2.3.6 Switching frequency

The switching frequency for the buck-boost converter can be set from 200 kHz to 700 kHz defined by an external resistor (R_{FREQ}) connected from the FREQ pin to GND or by supplying a synchronization signal to the SYNC pin. Select the switching frequency with an external resistor according to the graph in **Figure 15** or the following approximate formulas:

$$f_{SW}[kHz] = 5375 \cdot (R_{FREQ}[k\Omega])^{-0.8} \quad \text{Eq. 12}$$

$$R_{FREQ}[k\Omega] = 46023 \cdot (f_{SW}[kHz])^{-1.25} \quad \text{Eq. 13}$$

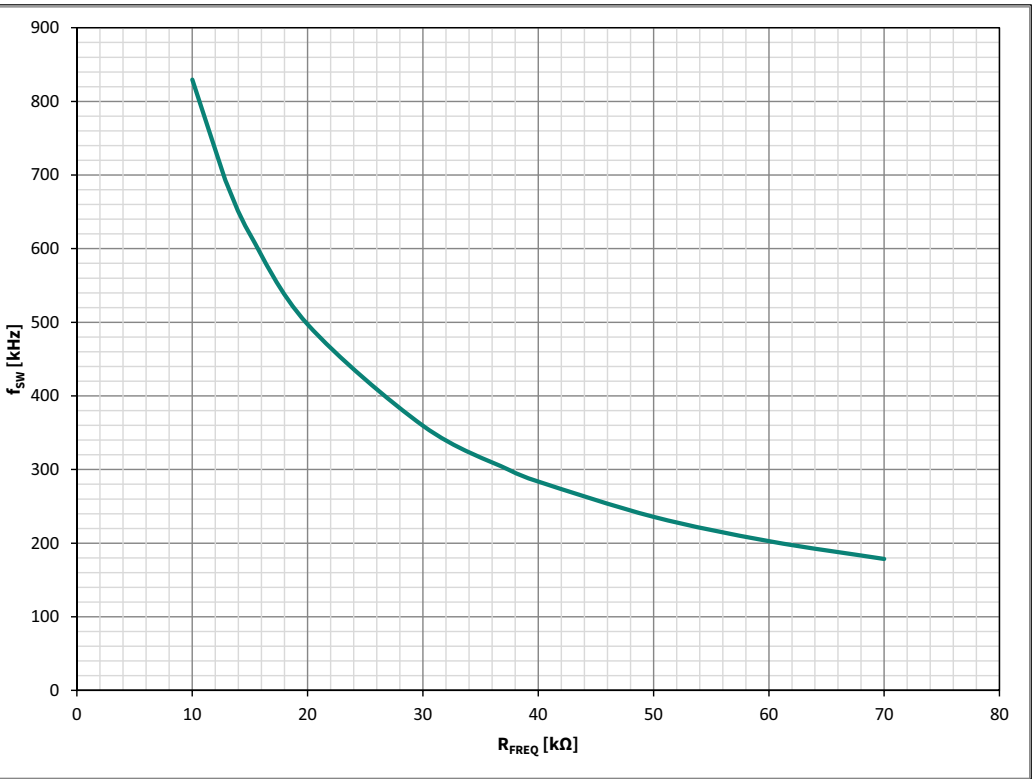


Figure 15 Switching frequency (f_{SW}) vs. Frequency select resistor (R_{FREQ}) value

2.3.7 Protection and diagnostics

The EZ-PD™ PMG1-B2 device has integrated circuits to diagnose and protect against overvoltage, open load, short-circuit of the load, and overtemperature. In IDLE state, only IVCC or IVCC_EXT undervoltage monitor or $V_{EN/INUVLO}$ undervoltage monitor are reported according to specifications. **Figure 16** shows a summary of various protection, diagnostic and monitor functions integrated in the device.

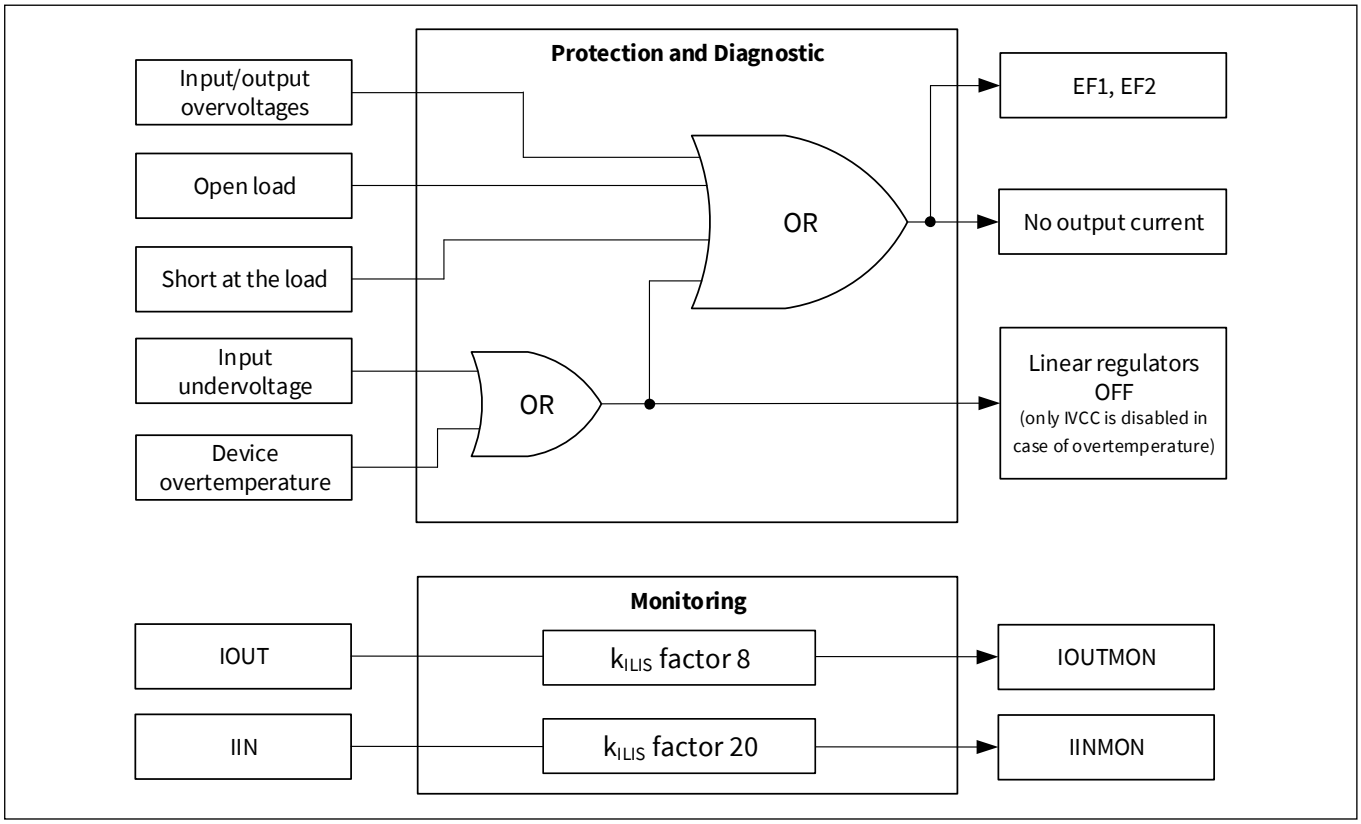


Figure 16 Overview of protection, diagnostics, and monitoring [2]

The device contains two error flags pins, EF1 and EF2, which change their state on occurrence of various faults. The pins EF1 and EF2 must be connected to EF1_IN and EF2_IN respectively, in the external circuit. The firmware reads the state of these error flags to determine the fault condition. **Table 5** shows the diagnostic truth table indicating the states of error flags (EF1 and EF2) for various fault events.

Table 5 Diagnostic truth table[3]

Input		Output			
Condition	**Level**	**EF1**	**EF2**	**Gate-drivers**	**IVCC**
Open load/ overvoltage	False	1	1	Switching	Active
	True	1	0	Both low-side MOSFETs ON	Active
Output short-circuit	False	1	1	Switching	Active
	True	0	1	Both low-side MOSFETs ON	Active
Overtemperature	False	1	1	Switching	Active
	True	0	0	All gate drivers are OFF	Shutdown

Note
2. k_{ILIS} = Ratio of load current to sense current (IL/IS)
3. A device overtemperature event overrules all other fault events

2.3.7.1 Input protections

The device provides following fault protections at the input side:

- Input overvoltage protection
- Input undervoltage protection

The input overvoltage and undervoltage shutdown levels can both be defined through an external voltage divider network, as shown in **Figure 17**. Both INOVLO and EN/INUVLO pin voltages are internally compared to their respective thresholds by means of hysteretic comparators. Whenever the comparator thresholds are crossed, the corresponding fault condition is triggered.

Neglecting the hysteresis, the following equations hold:

$$V_{IN\_UVth} = \left(1 + \frac{R_1}{R_2 + R_3}\right) \cdot V_{EN/INUVLOth} \quad \text{Eq. 14}$$

$$V_{IN\_OVth} = \left(1 + \frac{R_1 + R_2}{R_3}\right) \cdot V_{INOVLOth} \quad \text{Eq. 15}$$

$$P_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{\eta} \quad \text{Eq. 16}$$

$$V_{IN\_boundary} = \frac{P_{IN}}{I_{IN\_max}} = \frac{V_{OUT} \cdot I_{OUT}}{\eta \cdot I_{IN\_max}} \quad \text{Eq. 17}$$

$$I_{IN} = \frac{V_{IIN1 - IIN2}}{R_{IN}} \quad \text{Eq. 18}$$

$$I_{OUT} = \frac{V_{FBH - FBL}}{R_{FB}} \quad \text{Eq. 19}$$

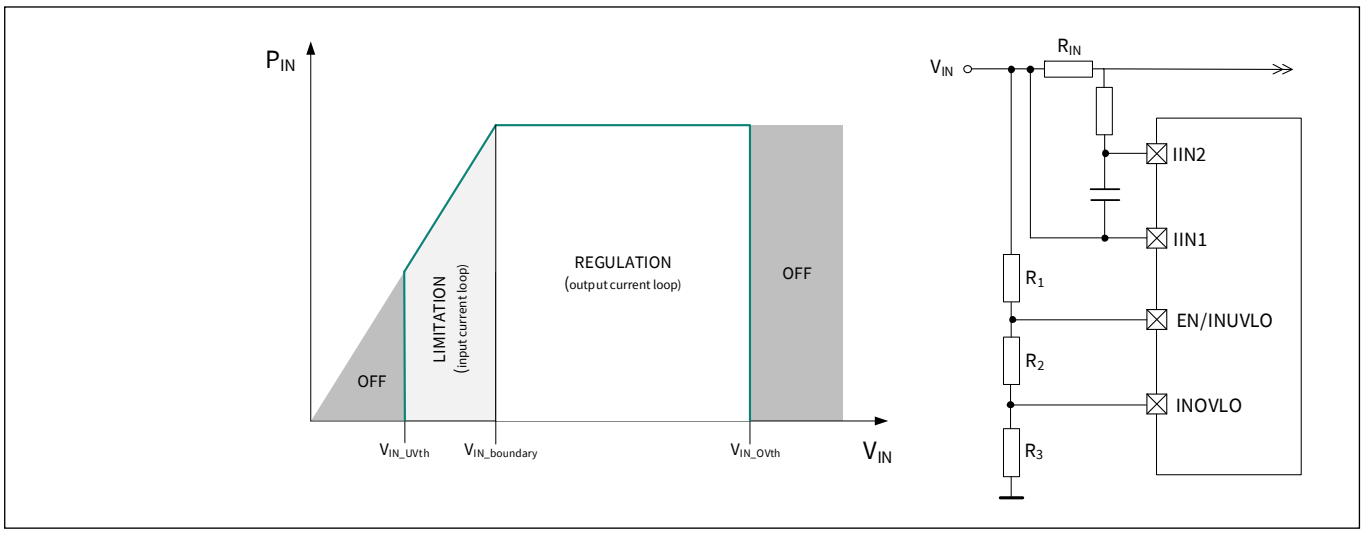


Figure 17 Input voltage protection

In case of overvoltage event at the input, the open-drain status pin EF2 will toggle to LOW, while EF1 will stay at HIGH. The soft-start capacitor will be discharged by an internal pull-down switch. After the overvoltage event disappeared, the device will auto restart with the soft-start function and the status pin EF2 will toggle to HIGH.

2.3.7.2 Output protections

The device provides the following fault protections at output side:

- Output overvoltage
- Open load
- Short-circuit

The VFB pin of the device measures the voltage on the application output and using the voltage divider network. Different faults such as short-to-ground, open load, and output overvoltage are triggered based on the internal thresholds set. See **Figure 18** for more details.

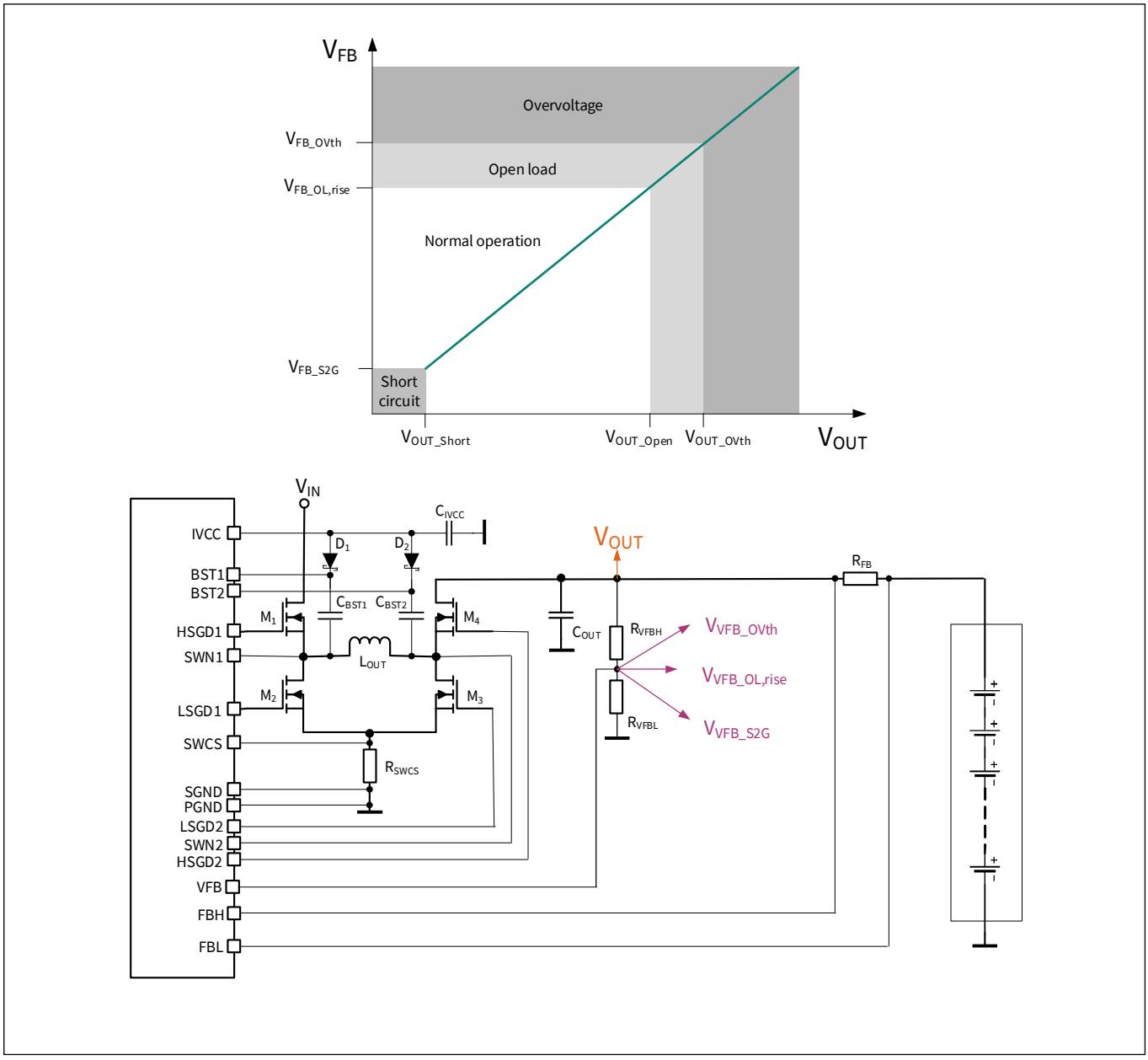


Figure 18 Output protection

2.3.7.2.1 Output overvoltage protection

A voltage divider between VOUT, VFB pin and ground is used to adjust the overvoltage protection threshold (see **Figure 18**).

Use **Eq. 20** to fix the overvoltage protection threshold.

$$V_{OUT\_OVth} = V_{VFB\_OVth} \cdot \frac{R_{VFBH} + R_{VFBL}}{R_{VFBL}} \quad \text{Eq. 20}$$

In case of overvoltage event at the output, the open-drain status pin EF2 will toggle to LOW, while EF1 will stay at HIGH and the gate drivers stop switching for output regulation (Brake-low condition both low-side MOSFETs ON). After the overvoltage event disappeared, the device will auto restart and the status pin EF2 will toggle to HIGH.

If the overvoltage threshold V_{OUT_OVth} is set lower than the maximum V_{IN} application operating range, attention must be paid to the overvoltage behavior.

If load current persists during overvoltage event, repetitive overvoltage triggering may occur with a high frequency. This prevents inductor current regulation and the output current may even increase. To avoid this condition, proper sizing of the external components is needed (that is, increase the output capacitance or the overvoltage threshold to delay the overvoltage trigger).

2.3.7.2.2 Output short-circuit protection

The short-circuit at the output is detected by monitoring the output voltage feedback at VFB pin. The device detects a short circuit at the output if following condition is satisfied:

- The pin VFB falls below the threshold voltage V_{VFB_S2G} for at least eight clock cycles

During the rising edge of the soft-start, the short circuit detection via VFB is ignored until voltage on SOFT_START pin rises to $V_{SOFT\_START\_LOFF}$ (see **Figure 4**).

A voltage divider between V_{OUT}, VFB pin and ground is used to adjust the application short-circuit thresholds as shown in **Eq. 21**.

$$V_{OUT\_Short} = V_{VFB\_S2G} \cdot \frac{R_{VFBH} + R_{VFBL}}{R_{VFBL}} \quad \text{Eq. 21}$$

The device provides an open-drain status pin, EF1, which pulls low when the short circuit is detected.

The only time the VFB pin will be below V_{VFB_S2G} is during start-up or if the output shorted. To prevent a false short-circuit detection during start-up, the device ignores the detection of a short circuit or an open load until the soft-start capacitor voltage reaches $V_{SOFT\_START\_LOFF}$ (1.75 V). Therefore, to prevent false tripping after startup, a large enough soft-start capacitor must be used to allow the output to get up to approximately 50% of the final value within this time.

Note If the short circuit condition disappears, the device will restart with the soft-start routine as described in **"Adjustable soft start"** on page 15.

2.3.7.2.3 Open load protection

An open load or open feedback event at the output is detected by the device based on two conditions:

1. Output voltage threshold: $V_{VFB} > V_{VFB\_OL,rise}$
2. Output current information: $V_{(FBH-FBL)} < V_{FBH\_FBL\_OL}$

During the rising edge of the Soft Start, the open load detection is ignored until the soft-start capacitor voltage reaches $V_{SOFT\_START\_LOFF}$.

The device provides an open-drain status pin, EF2, which pulls low when the VFB pin is above $V_{VFB\_OL,rise}$ threshold and the voltage across $V_{(FBH-FBL)}$ is less than $V_{FBH\_FBL\_OL}$. If the open load clamp voltage is set correctly using the VFB pin, the VFB pin should never exceed 1.28 V ($V_{VFB\_OL,fall}$) when a load is connected.

An open-load error also causes an increase in the output voltage, which may result in an overvoltage condition being reported in combination with the open-load error (in general, multiple error detection may happen if more error detection thresholds are reached during the auto-restart function, as a possible consequence of reactive behavior at the output node during open load).

The compensation capacitor (C_{COMP})is discharged during an open-load condition to prevent spikes if load reconnects. This step could artificially generate short-circuit detection after an open-load event.

2.3.7.3 Input and output current monitoring

EZ-PD™ PMG1-B2 provides two analog output pins, IINMON and IOUTMON, which can be used to monitor the input and output current respectively. The pins route the output of current sense amplifiers which corresponds to input/output currents. The microcontroller can read these analog voltages using the internal 8-bit ADC by connecting the analog pins to IINMON_IN and IOUTMON_IN pins of the device.

2.3.7.3.1 Input current monitoring and limiter

The two inputs (IIN1, IIN2) are used to monitor and limit the input current (Block A1 and A7 in **Figure 3**). The control loop reduces the compensation voltage (V_{COMP}) when the voltage across the pins reaches input current-sense threshold $V_{(IIN1-IIN2)\_th}$ (**P_6.4.13**) to keep the input current below I_{IN_MAX} as shown in **Eq. 22**.

$$I_{IN\_max} = \frac{V_{(IIN1-IIN2)\_th}}{R_{IN}} \quad \text{Eq. 22}$$

The IINMON pin provides a linear indication of the current flowing through the input as shown in **Eq. 23**.

$$V_{IINMON} = 20 \cdot I_{IN} \cdot R_{IN} \quad \text{Eq. 23}$$

Where ‘20’ is the k_{ILIS} factor for input current sensing.

Note If the R_{IN} value is chosen in a way that the current limitation is much higher than the nominal input current in the application, the current measurement becomes inaccurate. Best results for an accurate current measurement via the IINMON pin is to set the current limit only slightly above the specific application’s nominal input current.

2.3.7.3.2 Output current monitoring

The output current monitoring is achieved by the scaling the current sense voltage between FBH and FBL pins using the output current sense amplifier (A5 in **Figure 3**).

The IOUTMON pin provides a linear indication of the current flowing through the output feedback shunt resistor R_{FB} as shown in **Eq. 24**.

$$V_{IOUTMON} = 0.2 + 8 \cdot I_{OUT} \cdot R_{FB} \quad \text{Eq. 24}$$

Where '8' is the k_{ILIS} factor for output current sensing.

2.3.7.4 Overtemperature protection

A temperature sensor is integrated in the buck-boost controller block. The temperature monitoring circuit compares the measured temperature to the shutdown threshold.

If the internal temperature sensor reaches the shutdown temperature (T_{j_SD}), the gate-drivers and the IVCC regulator are shut down.

The CLKOUT function is also disabled during an overtemperature event, and will auto-restart when the device cools down to T_{j_SO} (= T_{j_SD} – $T_{j\_SD\_HYST}$) and IVCC is restored.

Note The buck-boost controller will start up with a soft-start routine after the overtemperature condition disappears.

2.3.8 Spread spectrum feature

The Infineon flat spectrum feature set has the target to minimize external additional filter circuits. The goal is to provide several beneficial concepts to provide easy adjustments for EMC improvements after the layout is already done and the hardware is designed.

The spread spectrum modulation technique significantly improves the lower frequency range of the spectrum (f < 30 MHz). By using the spread spectrum technique, it is possible to optimize the input filter only for the peak limits, and also pass the average limits (average emission limits are -20 dB lower than the peak emission limits). By using spread spectrum, the need for low ESR input capacitors is relaxed because the input capacitor series resistor is important for the low frequency filter characteristic. This can be an economic benefit if there is a strong requirement for average limits. EZ-PD™ PMG1-B2 features a built-in spread spectrum function which can be enabled via an external pin (SPREAD_SPECTRUM = HIGH). Triangular modulation is used with a modulation frequency f_{FM} (**P_11.6.3**), and the deviation frequency f_{dev} (**P_11.6.2**), which are internally fixed. See **Figure 19** for more details. **Figure 20** shows the frequency spectrum with and without spread spectrum modulation.

Note SYNC pin should be connected to ground for using the spread spectrum function.

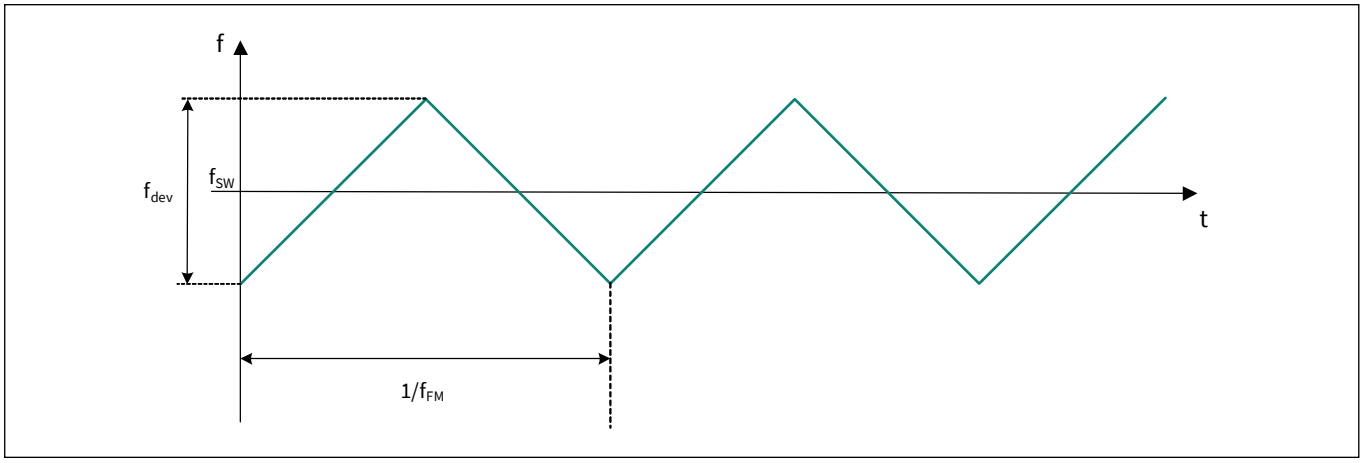


Figure 19 Spread Spectrum modulation in time domain

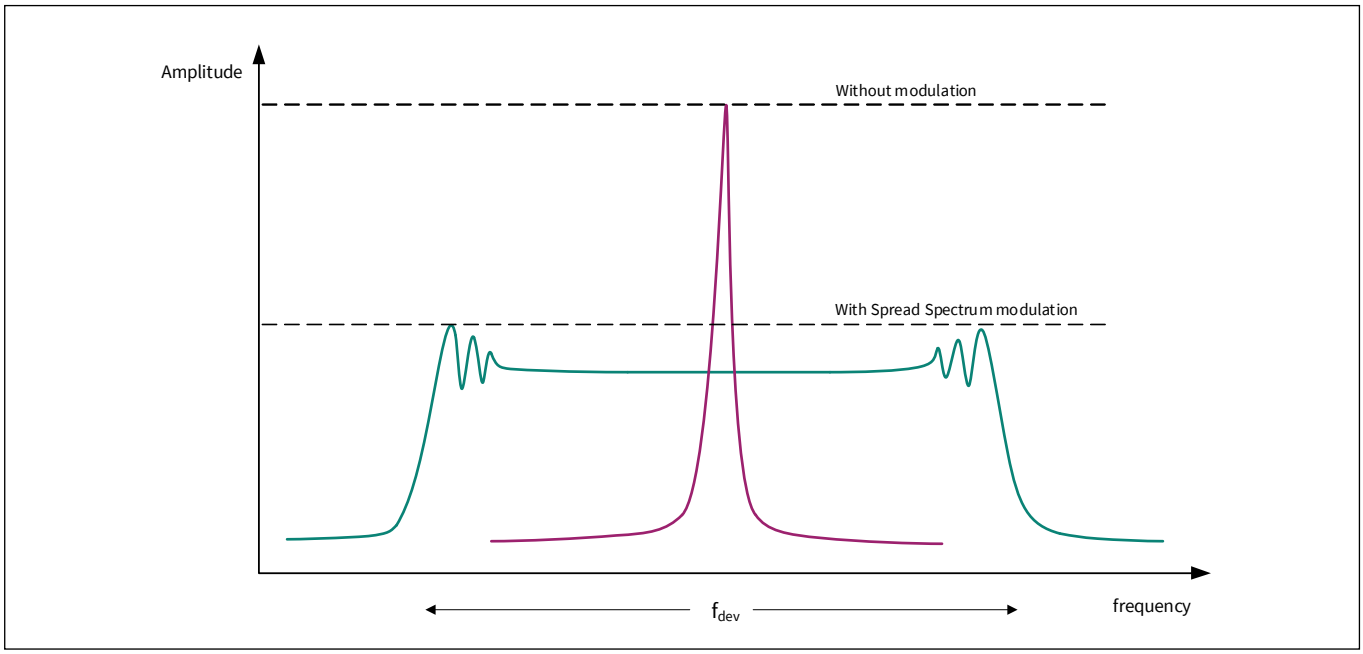


Figure 20 Spread Spectrum response in frequency domain

2.4 Analog blocks

2.4.1 ADC

The EZ-PD™ PMG1-B2 device has two 8-bit SAR ADCs (ADC0 and ADC1). 8-bit SAR ADCs are used for general purpose A/D conversion applications in the chip. ADCs can be accessed from all the GPIOs through on-chip analog multiplexers. Appropriate AMUX splitters must be closed to establish connection from different GPIOs to the analog multiplexer buses (AMUX_A and AMUX_B).

2.4.2 Analog multiplexer (AMUX)

EZ-PD™ PMG1-B2 contains two internal analog multiplexer buses (AMUX_A and AMUX_B), which can be used to route analog signals from GPIOs and fixed function I/Os to internal peripheral blocks. AMUX bus connection of the I/Os are split into two halves (left plane and right plane) via splitter switches. By default, the I/Os on the left plane can be connected to AMUXA/B lines and routed to ADC 0. Similarly, the I/Os on the right plane can be connected to AMUXA/B lines and routed to ADC 1. To route I/Os from left plan to the right plane, the splitter switches must be closed by appropriate peripheral register configurations. **Table 6** provides a detailed list of all I/Os connected to the respective planes.

Table 6 I/O connection to AMUX left/right planes

AMUX segment	I/O type	Connection
AMUX left plane (ADC 0)	GPIO	P0.0, P0.1, P1.1, P1.2, P1.3, P1.5, P1.7
	Fixed-function	VBUS_MON, IINMON_IN
AMUX right plane (ADC 1)	GPIO	P3.2, P3.3, P3.6
	Fixed-function	VBAT_MON, IOUTMON_IN

2.4.3 On-chip temperature sensor

The analog block consist of a bipolar junction transistor (BJT) biased in the form of a diode with a constant collector current. The base-to-emitter voltage (V_{BE}) of the BJT is highly temperature dependent. The ADC can measure this voltage to estimate the approximate die-temperature of EZ-PD™ PMG1-B2.

Note The V_{BE} voltage of BJT has a negative relationship with the die-temperature. The resolution of temperature measurement is better for lower VDDD. For a VDDD equal to 5 V, a measured BJT voltage of 670 mV corresponds to an estimated die-temperature in the range of 85°C to 115°C.

2.5 Integrated digital blocks

2.5.1 Serial communication block (SCB)

The EZ-PD™ PMG1-B2 device has two SCB blocks, one can be configured as UART/I^2C/SPI and the other can be configured as only I^2C. In the SPI mode, the SCB blocks can be configured to act as a master or a slave.

In the I2C mode, these blocks implement full multi-master and slave I^2C interfaces capable of multi-master arbitration.

This I^2C implementation is compliant with the standard Philips I^2C specification v3.0. These blocks operate at speeds of up to 1 Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU. The SCB blocks support 8-byte deep FIFOs for receive and transmit, which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The I^2C port I/Os for SCB0 are fail-safe. The I^2C ports for the other SCB is not fail-safe tolerant (see the **"Fail-safe GPIOs"** on page 36 for more details).

Table 7 SCB functionality

SCB	UART	I^2C	SPI
SCB0	No	Yes	No
SCB3	Yes	Yes	Yes

Note SCB1 and SCB2 are not available.

Table 8 SCB pin assignment

GPIO	UART	I^2C	SPI
P0.0	–	SCB0_I2C_SDA	–
P0.1	–	SCB0_I2C_SCL	SCB3_SPI_SEL
P3.2	SCB3_UART_TX	SCB3_I2C_SDA	SCB3_SPI_MOSI
P3.3	SCB3_UART_TX	SCB3_I2C_SCL	SCB3_SPI_MISO
P3.6	–	–	SCB3_SPI_CLK

2.5.2 Timer, counter, pulse-width modulator (TCPWM)

EZ-PD™ PMG1-B2 device has two TCPWM blocks. One of these functions as a PWM generator on a fixed-function output pin. The other one can be configured as a timer or counter or pulse-width modulator (PWM). This timer is available for internal timing use by firmware or for providing PWM-based functions on a GPIO.

Table 9 TCPWM block (SCB) functionality

TCPWM	Timer/counter	PWM	Routing
TCPWM0	No	Yes	PWM_VSET
TCPWM1	Yes	Yes	P1.1

2.6 I/O subsystem

The EZ-PD™ PMG1-B2 device has a total of 19 I/O pins. I/O subsystem is broadly classified into GPIOs and fixed-function I/O pins.

2.6.1 GPIO

The EZ-PD™ PMG1-B2 device has 10 GPIOs which can be configured as analog or digital pins. The GPIO block can be configured in one of the eight following modes:

- Eight drive modes:
  - Digital input only
  - Strong drive HIGH and LOW
  - Strong drive LOW with weak pull-up
  - Strong drive HIGH with weak pull-down
  - Open drain with strong drive LOW
  - Open drain with strong drive HIGH
  - Weak pull-up with weak pull-down
  - Analog
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enable/disable
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control
- Two fail-safe GPIOs

During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. The pin locations for fixed-function peripherals such as USB-C port are also fixed in order to reduce internal multiplexing complexity. The data output registers and pin state register store, respectively, the values to be driven on the pins and the states of the pins themselves.

The configuration of the pins can be done by the programming of registers through software for each digital I/O port. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

The I/O ports can retain their state during Deep Sleep mode or remain ON. If the operation is restored using reset, the pins shall go to the High-Z state. If operation is restored by an interrupt event, the pin drivers shall retain their state until firmware chooses to change it. The I/Os (on data bus) do not draw current on power down.

2.6.1.1 Fail-safe GPIOs

EZ-PD™ PMG1-B2 has two pins that are fail-safe GPIOs. These are P0.0 and P0.1, which are the I^2C pins for SCB0. The fail-safe feature ensures that, in the absence of VDDD power, a logic high state on these pins due to I^2C line activity will not back-power the MCU.

2.6.2 Fixed-function I/O pins

EZ-PD™ PMG1-B2 has 9 I/O pins which are used for dedicated functions in a typical battery charging application. These are routed to specific internal peripherals to enable the individual pin functionality. **Table 10** lists the fixed-function pins of the device along with their functionality

Table 10 Fixed-function I/O pins

Pin name	Input/ output	Connection	Description
VBUS_MON	Input	AMUX	Analog input pin to measure Type-C VBUS voltage using ADC
VBAT_MON	Input	AMUX	Analog input pin to measure battery voltage using ADC
IINMON_IN	Input	AMUX	Analog input pin to measure input current using ADC
IOUTMON_IN	Input	AMUX	Analog input pin to measure output current using ADC
PWMI_OUT	Output	I/O subsystem	Digital output pin to turn ON/OFF the buck-boost controller
PWM_VSET	Output	TCPWM0	PWM output pin for buck-boost output
EF1_IN	Input	I/O subsystem	Error flag monitoring input pin
EF2_IN	Input	I/O subsystem	Error flag monitoring input pin
VBUS_DISCHARGE_CTRL	Output	I/O subsystem	Digital output pin to control Type-C VBUS discharge FET

2.7 System resources

2.7.1 Watchdog timer (WDT)

The EZ-PD™ PMG1-B2 device has a WDT running from the internal low-speed oscillator (ILO). This allows watchdog operation during Deep Sleep and generate a watchdog reset (WDR) if not serviced before the timeout occurs. The WDR is recorded in the Reset cause register.

2.7.2 Reset

The EZ-PD™ PMG1-B2 device can be reset from a variety of sources including a software reset. The reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is preserved through reset and allows application firmware to determine the cause of the reset. XRES pin is the dedicated pin for asserting an external hardware reset.

2.7.3 Clock system

The EZ-PD™ PMG1-B2 device has a fully integrated clock with no external crystal required. EZ-PD™ PMG1-B2 device's clock system is responsible for providing clocks to all subsystems that require clocks (TCPWM, SCB, and PD) and for switching between different clock sources.

The two clock sources are 24-48 MHz internal main oscillator (IMO) and a 32 kHz internal low-speed oscillator (ILO). High-frequency clock (HFCLK) of up to 48 MHz selected from IMO or external clock. There are dedicated prescalers for HFCLK. Low-frequency clock (LFCLK) is sourced by ILO.

3 Power system overview

EZ-PD™ PMG1-B2 has three supplies:

- VIN (main supply voltage)
- IVCC_EXT (supply for internal gate-drivers)
- VDDD (supply for MCU)

The VIN supply provides internal supply voltages for the analog and digital blocks of the buck-boost controller. VIN supports an absolute maximum voltage of 60 V. IVCC_EXT is the external supply for the low-side driver stages. If no external supply is available, this pin must be shorted to IVCC, which is the output of an internal 5 V LDO. The supply pins VIN and IVCC_EXT have undervoltage detections. Undervoltage on IVCC_EXT or IVCC voltages forces a deactivation of the driver stages, which results in stopping the switching activity. The double function pin EN/INUVLO can be used as an input undervoltage protection by placing a voltage divider network from VIN to GND. If EN/INUVLO pin detects an undervoltage condition, it will turn off the IVCC voltage regulator and stop switching.

The operating power supply for the MCU is derived from VDDD. If external supply is unavailable, externally short the VDDD pin to IVCC pin. VDDD pin is also used for connecting bypass capacitor for voltage stability. EZ-PD™ PMG1-B2 MCU has three different power modes (Active, Sleep, and Deep Sleep), transitions between which are managed by the Power System. A separate power domain VDDIO is provided for the GPIOs. The VCCD pin, the output of the core (1.8 V) regulator, is brought out only for connecting a 1 µF capacitor for stability. This pin is not supported as a power supply.

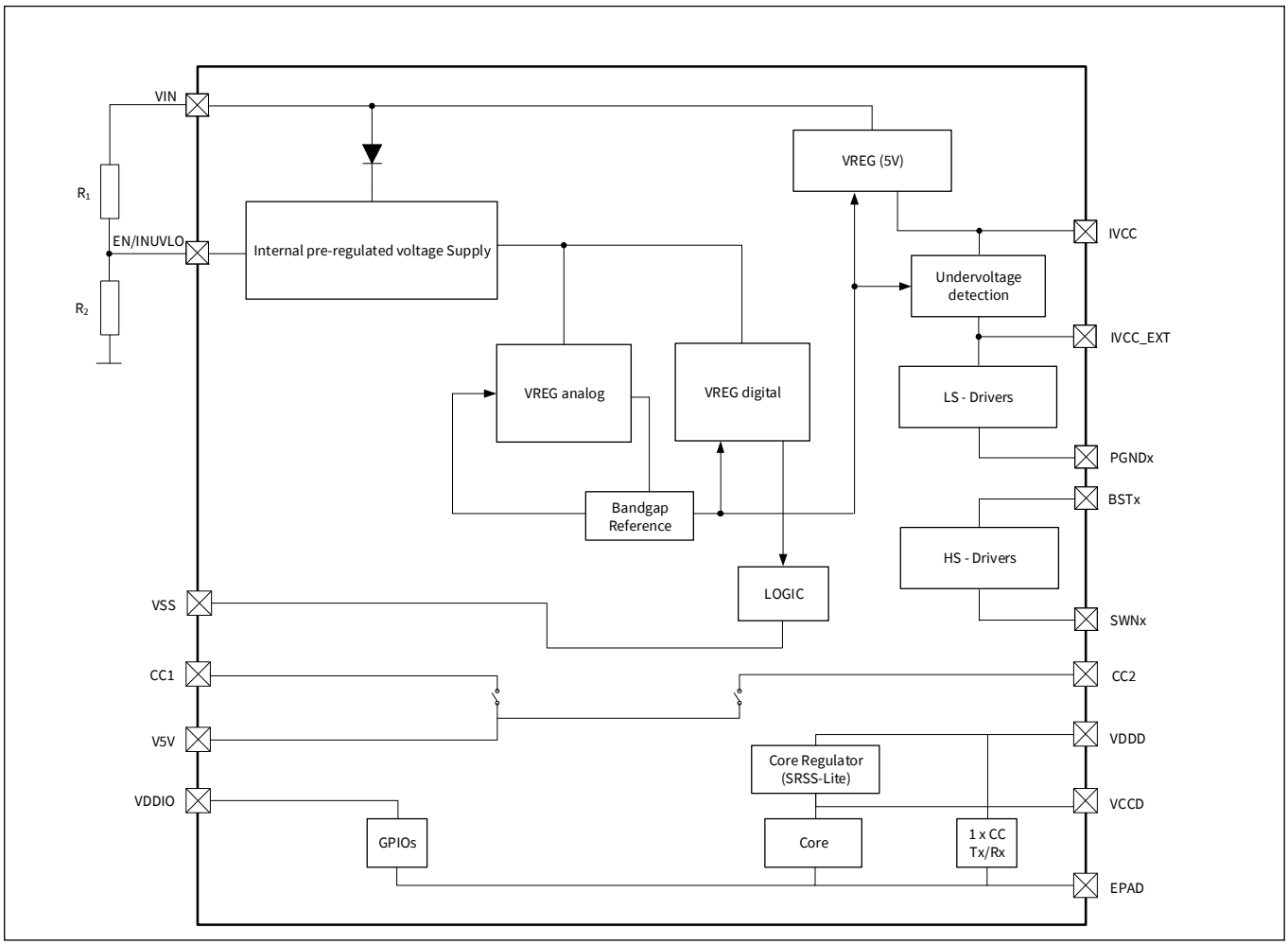


Figure 21 Power system block diagram

3.1 Internal LDO

The integrated internal LDO is used to power the internal gate-driver stages and the MCU. When the IVCC pin is connected to the IVCC_EXT pin, the internal LDO supplies the internal gate-drivers with a typical voltage of 5 V and current up to I_{LIM} (**P_9.2.2**). An external output capacitor with low ESR is required to be connected on IVCC pin for stability and buffering transient load currents. During normal operation, the external MOSFET switches will draw transient currents from the linear regulator and its output capacitor. Therefore, proper sizing of the output capacitor must be considered to supply sufficient peak current to the gate of the external MOSFET switches. A minimum capacitance value is given in parameter C_{IVCC} (**P_9.2.4**).

Note To prevent excessive overheating of the internal LDO, the current drawn from the LDO should not exceed 50 mA (subject to conditions: **Table 51**). Any load connected to the IVCC pin draws current directly from the internal LDO output. The heat generated in the LDO is proportional to the power dissipation which depends on the current drawn. Therefore, the IVCC output of the internal LDO should not be used to power external circuits.

Alternative IVCC_EXT supply:

Alternatively, the IVCC_EXT pin can be used for an external voltage supply to supply the MOSFET gate-drivers. This may be beneficial in cases where the system draws higher power externally from IVCC pin which results in more power dissipation in the IC.

3.1.1 Integrated undervoltage protection on IVCC

An integrated undervoltage reset threshold circuit monitors the LDO output voltage. This undervoltage reset threshold circuit will turn OFF the gate-drivers in case the IVCC or IVCC_EXT voltage falls below their undervoltage reset switch OFF Thresholds $V_{IVCC\_RTH,d}$ (**P_9.2.9**) and $V_{IVCC\_EXT\_RTH,d}$ (**P_9.2.5**). The undervoltage reset threshold for the IVCC and the IVCC_EXT pins help to protect the external switches from excessive power dissipation by ensuring the gate drive voltage is sufficient to enhance the gate of the external logic level N-channel MOSFETs.

3.2 Power states of buck-boost controller

The buck-boost controller block has the following power states:

- SLEEP state
- IDLE state
- ACTIVE state

The transition between the power states is determined according to following variables after a filter time of maximum three clock cycles:

- VIN level
- EN/INUVLO level
- IVCC level
- IVCC_EXT level

Figure 22 shows the state diagram for all the possible power state transitions. The power-up condition is entered when the supply voltage V_{VIN} exceeds its minimum supply voltage threshold $V_{VIN(ON)}$ (P_5.3.1).

- **SLEEP:**

When the block is in the SLEEP state, all outputs are OFF, independently from the supply voltages VIN, IVCC and IVCC_EXT. The current consumption is low $I_{VIN(SLEEP)}$ (P_5.3.3). The transition from SLEEP to ACTIVE state requires a specified time: t_{ACTIVE} (P_5.3.11).

- **IDLE:**

In IDLE state, the internal voltage regulator is working. Diagnosis functions are not available. The output drivers are switched OFF, independently from the supply voltages VIN, IVCC and IVCC_EXT.

- **ACTIVE:**

In Active state, the device starts switching activity to provide power at the output only when PWMI = HIGH. To start the high-side gate-drivers HSGD1,2 the voltage level $V_{BST1,2}$–$V_{SWN1,2}$ needs to be above the threshold $V_{BST1,2}$–$V_{SWN1,2\_UVth}$ (P_6.4.64). In ACTIVE state, the device current consumption via VIN is dependent on the external MOSFET used and the switching frequency f_{SW}.

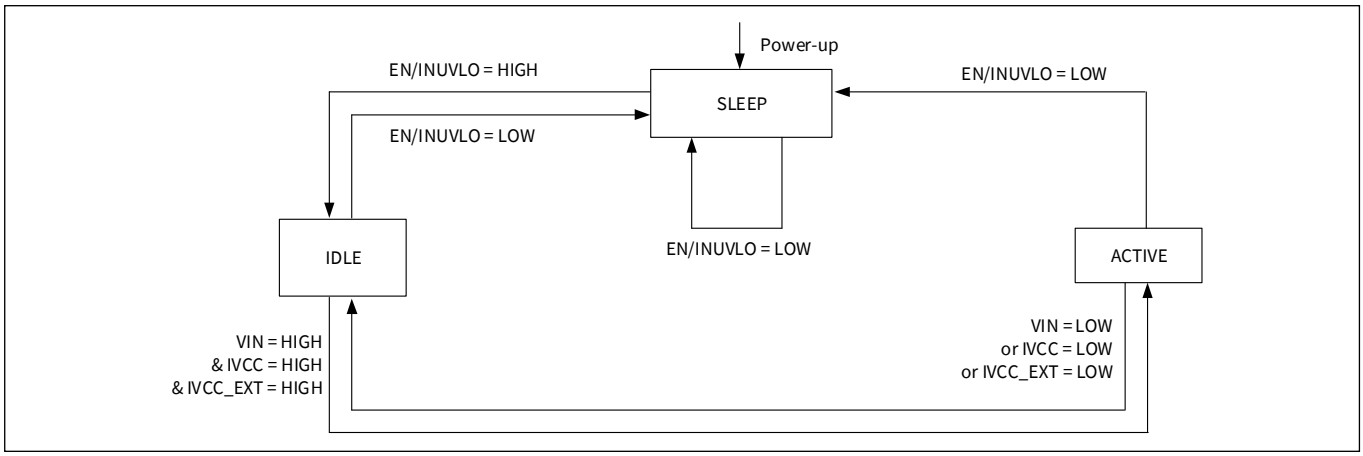


Figure 22 Power state diagram of buck-boost controller

4 Battery charging

EZ-PD™ PMG1-B2 device enables to design a USB-C PD powered 240 W battery charging system to quickly charge the connected battery pack. It also integrates all necessary fault protections to prevent the damage of the connected battery and the charger. It supports different types of battery packs with different number of cells in series and parallel. The hardware and firmware can be configured to suit the particular type of battery pack to be charged. Once the configuration is completed, the system starts the charging process as soon as a USB PD power adapter is plugged-in to the Type-C port.

Note The features and configurations explained in this section are dependent on the system design and the firmware deployed in EZ-PD™ PMG1-B2 MCU. This section explains the battery charging application in line with **Application overview**.

4.1 System monitoring and charge control

EZ-PD™ PMG1-B2 controller monitors the battery parameters throughout the charging process to ensure an efficient and safe charging, and to extend the life of the battery. The control system regulates the battery charging current based on the set point fixed by the system firmware.

The various system parameters monitored by EZ-PD™ PMG1-B2 MCU are:

- Input current
- Output current
- Input VBUS voltage
- Battery voltage
- System/ambient temperature
- EZ-PD™ PMG1-B2 die-temperature

4.1.1 Charging current control

The battery charging is achieved by controlling the charging current based on the system and the battery operating conditions. The buck-boost control system operates in a constant current (CC) mode which helps to maintain the charging current at a particular set point value fixed by the firmware, using PWM_VSET pin. During the normal charging process, the system operates in constant current (CC) mode with the maximum current supplied to the battery based on the input power contract negotiated with the USB PD adapter and the terminal voltage of the battery pack connected. Besides, the charging current may also be limited based on the thermal conditions of the system to prevent any damage caused due to overtemperature.

4.1.2 Battery voltage monitoring

The terminal voltage of the battery pack is measured using the internal 8-bit SAR ADC through VBAT_MON pin. Based on the measured voltage, the firmware adjusts the charging current. The entire charging process is divided into multiple charging cycles wherein the firmware reduces the charging current in CC mode based on the increasing battery voltage. **Figure 23** and **Figure 24** shows the charging current reduction in successive charging cycles.

4.2 Charging modes

EZ-PD™ PMG1-B2 operates in various charging modes to optimize the entire charging process to achieve minimum charging duration, and to extend the life of the battery. All the charging modes are easily configurable in the firmware to fit the exact requirements of a particular battery type and battery chemistry.

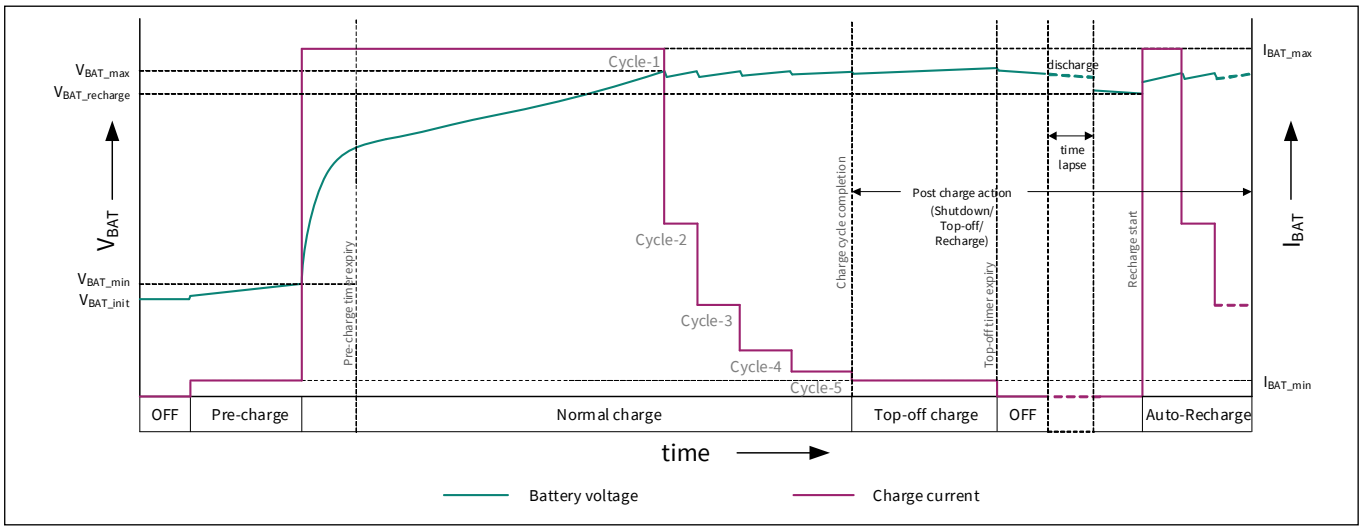


Figure 23 Battery charging modes in EZ-PD™ PMG1-B2 charger

4.2.1 Pre-charge

Pre-charge refers to the charging mode where the charging current is very small. Pre-charge mode is active when the battery voltage measured by the firmware is critically low. During this state, charging the battery with higher current causes over-heating due to high internal resistance. Therefore, the charging current is limited to minimum constant value until the battery voltage picks up and reaches a normal safe operating level.

4.2.2 Normal charge

Normal charging refers to the regular charging in constant current (CC) mode, where the system supplies the maximum possible safe charging current to the battery. The normal charging process is divided into multiple charge cycles with different values of current level set by the system. When the battery voltage reaches the maximum level for the first time, the charging current is reduced to a lower value. This drops the battery voltage slightly lower, and the charging continues with the new current level until the battery voltage further hits the maximum level again. This process continues in multiple cycles as shown in **Figure 23** until the current is reduced to a minimum pre-defined level to top-off the charge until the battery is fully charged. Normal charging mode is active for a longer duration compared to other modes.

4.2.3 Top-off charge

Top-off charging mode starts following the normal charging mode, when the battery is full based on the terminal voltage and current measured by the firmware.

When the normal charging mode completes with the current reduced to minimum level, the system can be configured to further operate in one of the three following post-charge modes:

- **Shutdown mode**: Stop the charging process indefinitely (until a Type-C reconnect)
- **Recharge mode**: Temporarily stop charging until the battery voltage drops to a slightly lower level (due to self-discharge). Thereafter, top up the lost charge again with minimum current until the terminal voltage is restored to maximum value.

- **Top-off charge mode**: Start top-off charging for a pre-determined time to maintain the battery voltage at the maximum level

If the system firmware is configured in top-off charging mode, the system continues to supply a minimum defined current for a particular time period as configured. This helps the battery to hold the maximum possible charge, thereby reaching its full capacity and preventing self-discharge.

4.3 Charging safety timers

EZ-PD™ PMG1-B2 implements safety timers to protect the battery during the entire charging process. This is important to prevent uncertain events such as overheating, overcharging especially in case where the battery is partially damaged. The safety timers are user configurable to fit the specifications of the battery and the charging requirements.

4.3.1 Pre-charge timer

Pre-charge timer defined the maximum pre-charge time during which a critically low-voltage battery is charged with minimum current. This timer prevents the firmware from indefinitely charging a damaged battery which cannot hold any charge leading to no voltage rise. If the timer expires before the battery voltage crosses the minimum operating voltage value, the firmware interprets it as a damaged battery and stops the charging process.

4.3.2 Normal charge timer

Normal charge timer is usually defined with a long duration where the regular battery charging process progresses.

4.3.3 Top-off charge timer

Top-off charge timer defines the duration for which top-off charging operation is active by supplying minimum current to a fully charged battery. When the timer expires, the top-off charging is stopped.

4.3.4 Watchdog timer

Watchdog timer (WDT) is crucial to ensure the safety in charging process in case of any unexpected firmware hang up. When the watchdog interrupts are not cleared regularly to an unexpected firmware crash, the MCU is reset. Thus, WDT ensures a fail-safe operation preventing any possibility such as overcharging/overcurrent/ overtemperature which compromises the safety of the system.

4.4 Lithium-ion battery charging

4.4.1 Charging profile

Figure 24 shows the charging profile for 2, 6, 10, and 12-cells Lithium-ion battery packs using the EZ-PD™ PMG1-B2 charger. The input power for charging is derived from a 240 W (48 V, 5 A) EPR USB PD adapter.

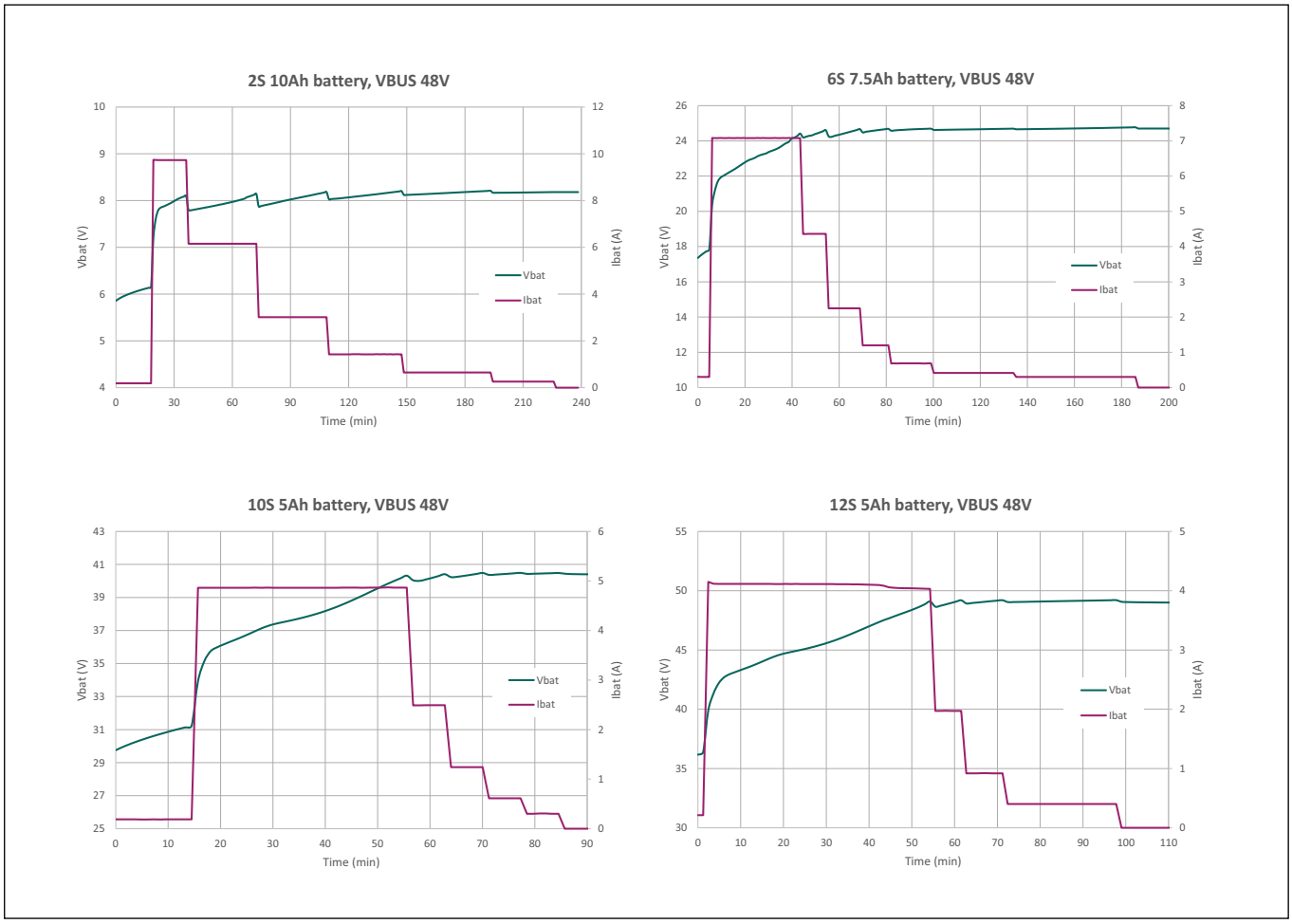


Figure 24 Typical Li-ion battery charging V-I characteristics

4.4.2 Battery protection

Figure 25 shows the battery overvoltage (OVP) and output short-to-ground (S2G) protection configuration in the system hardware, for 12-cell and 2-cell Lithium-ion battery packs. The thresholds for OVP and S2G are set using R_{VFBH} and R_{VFBL} resistors shown in **Figure 25**, and are configured based on the number of cells in series in the battery pack. The hardware protection feature provides a quick reaction time to shut-off the power stage in case of faults, thereby preventing any damage to the battery or system.

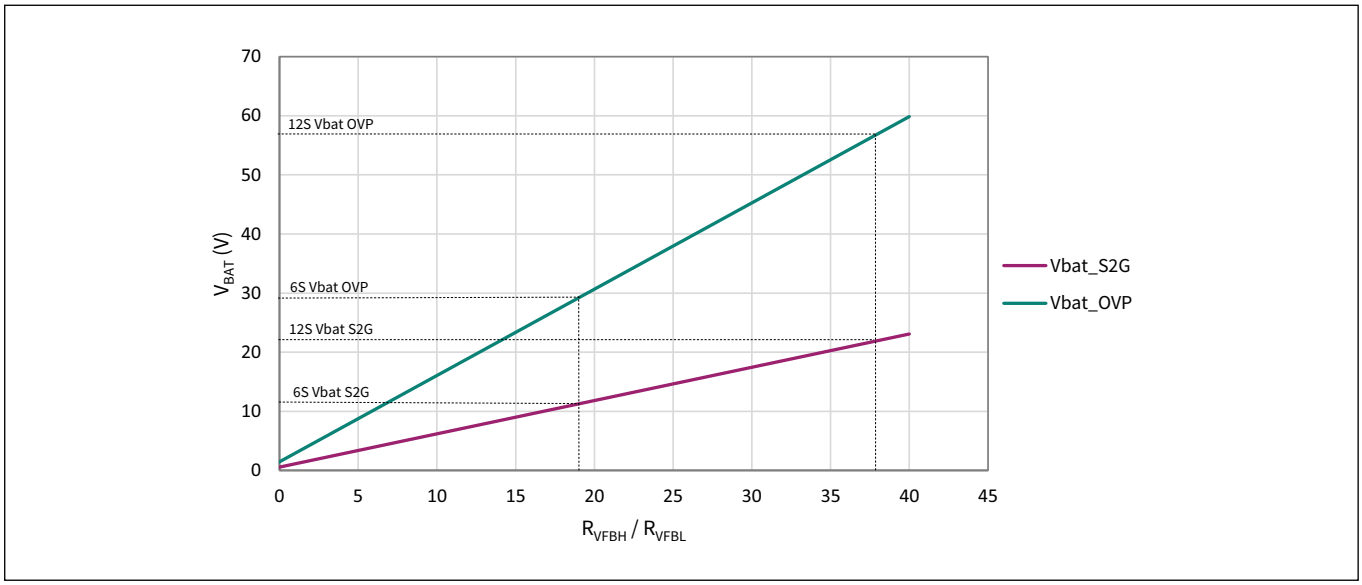


Figure 25 Battery protection configuration in the hardware

Note The device provides short-circuit protection to the system output by turning OFF the power stage on detecting a short-circuit at the output. This does not protect the battery from short-circuit due to external causes.

4.5 Battery charging configuration

EZ-PD™ PMG1-B2 enables to develop a fully configurable battery charging system which can be configured as per the system requirements and battery specifications. This feature helps to customize the system to suit the charging profile for different types of battery packs with different chemistries.

Table 11 lists some of the important configuration parameters of the system.

Table 11 Configurable battery-charging/system parameters

Parameter	Description
Number of series cells	Number of individual cells connected in series in the battery pack
Maximum and minimum voltage per cell	Defined based on the cell chemistry used in the battery pack
Maximum and minimum charging current	Defined based on the capacity and the number of parallel combination of cells in the battery pack
Full-charge end modes	Defines: shutdown, top-up recharge, and top-off charge modes
Maximum pre-charge duration	Maximum time period for which pre-charging is active
Maximum normal charge duration	Maximum time period for which normal charging is active
Maximum top-off charge duration	Maximum time period for which top-off charging is active
Maximum and minimum ambient temperature for charging	Defines the ambient temperature within which the battery can be safety charged
System temperature-based charge current setting	Protects the charger system from damage due to overtemperature

4.6 Buck-boost converter efficiency

Buck-boost efficiency is dependent on the system operating points and the components used in the system design. **Figure 26** and **Figure 27** show the plots for buck-boost operating efficiency with the components listed in **Table 12**.

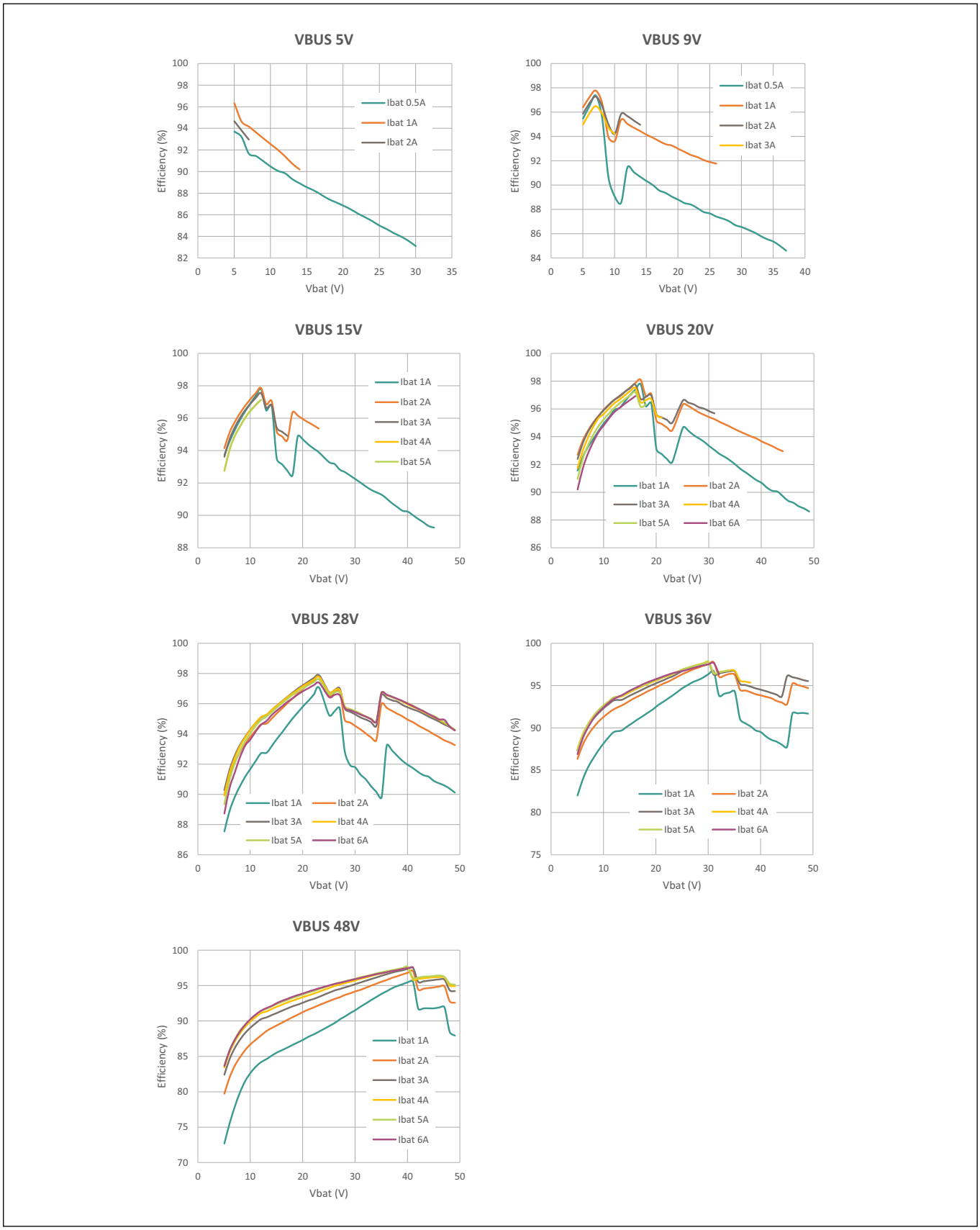


Figure 26 Buck-boost converter operating efficiency (CC mode, FSW = 280 kHz)

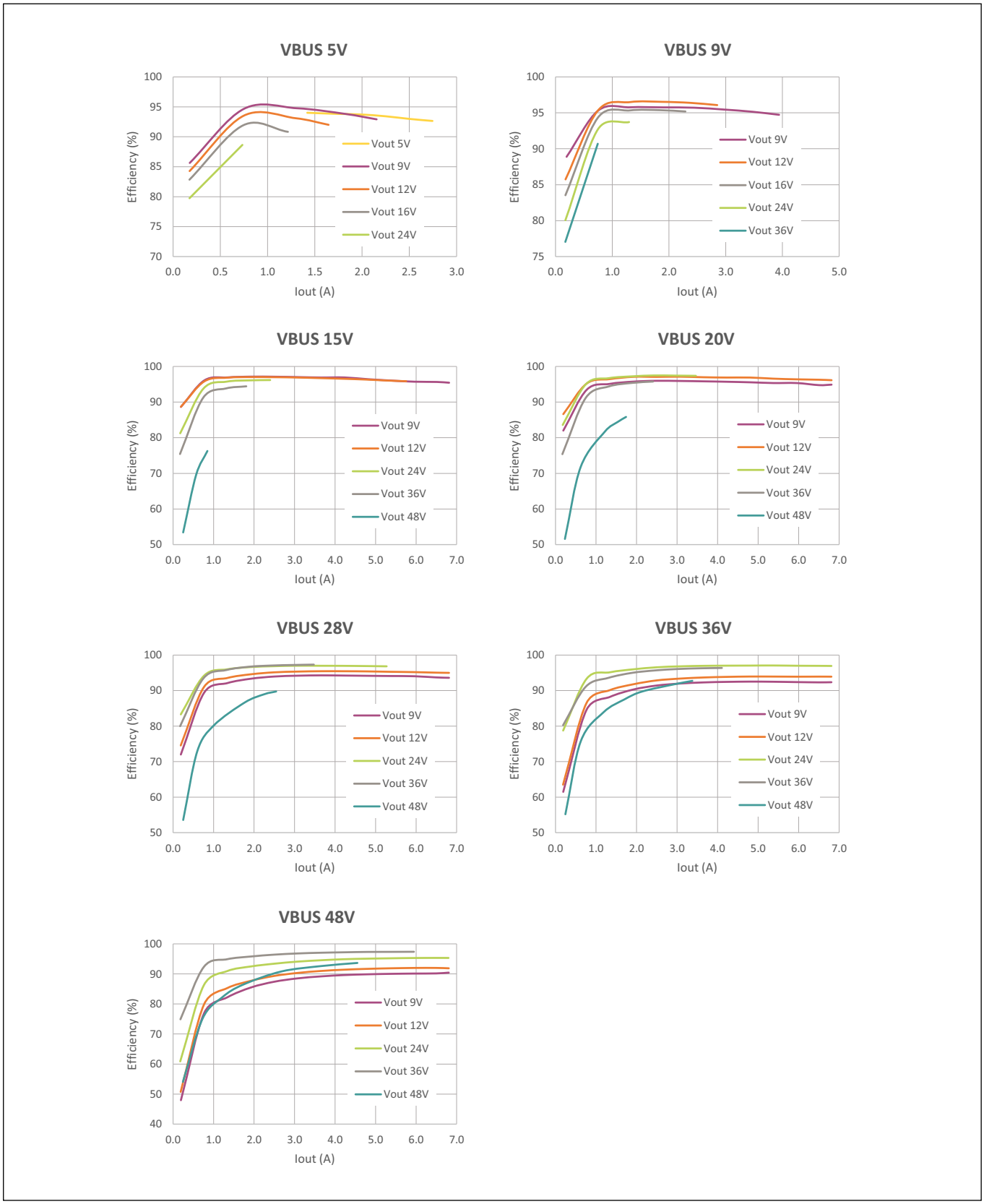


Figure 27 Buck-boost converter operating efficiency (CV mode, FSW = 280 kHz)

Note The efficiency plots in **Figure 26** and **Figure 27** are applicable to REF_PMG1_B2_DRP board design. For battery charging, it is recommended to request the appropriate VBUS voltage from the connected USB PD power adapter to maximize the efficiency referring to **Figure 26**, for a particular battery cell count.

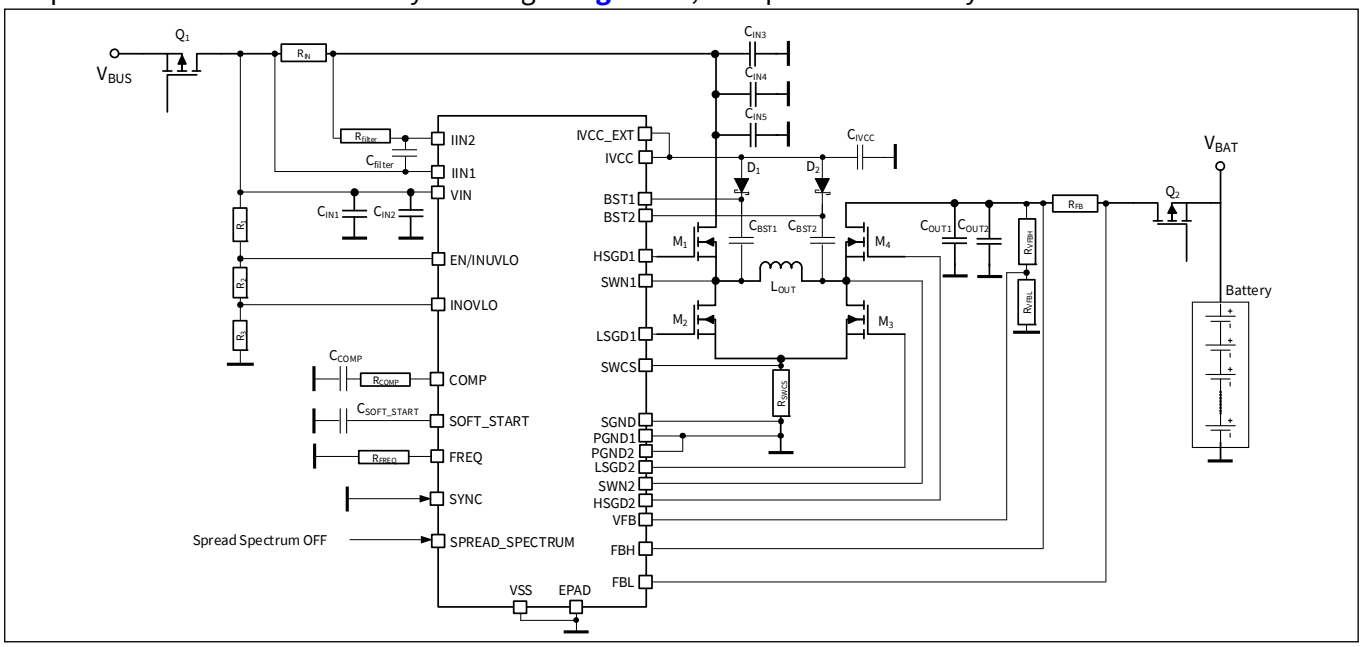


Figure 28 EZ-PD™ PMG1-B2 battery charging system power path

Table 12 12-cell Lithium-ion battery charger system power path BOM

Component	Value	Manufacturer	Part number
R_{IN}	9 mΩ, 5%	Vishay Dale	WFCP06129L000FE66
C_{IN1}, C_{IN2}	100 µF, 63 V	Nichicon	UCM1J101MNS1GS
C_{IN3}, C_{IN4}, C_{IN5}	10 µF, 63 V	Samsung Electro-Mechanics	CL32B106KMVNNWE
R_{filter}	10 Ω, 1%	Stackpole Electronics Inc.	RMCF0603FT10R0
C_{filter}	100 nF, 50 V	Samsung Electro-Mechanics	CL10B104KB8NNNC
R_1, R_2, R_3	x kΩ, 1%	-	-
R_{COMP}	0 Ω	Stackpole Electronics Inc.	RMCF0805ZT0R00
C_{COMP}	22 nF, 25 V	KEMET	C0805C223J3RACTU
C_{SOFT_START}	100 nF, 50 V	Samsung Electro-Mechanics	CL10B104KB8NNNC
R_{FREQ}	39 kΩ, 1%	Stackpole Electronics Inc.	RMCF0603FT39K0
C_{IVCC}	10 µF, 6.3 V	Samsung Electro-Mechanics	CL21B106KQQNNNE
D_1, D_2	BAT46WJ	Nexperia USA Inc.	BAT46WJ,115
C_{BST1}, C_{BST2}	100 nF, 50 V	Samsung Electro-Mechanics	CL10B104KB8NNNC
M_1, M_2, M_3, M_4	60 V, 4 mΩ	Infineon Technologies	BSZ040N06LS5ATMA1
L_{OUT}	10 µH, 9.7 mΩ	Coilcraft	XGL1010-103MED
R_{SWCS}	7 mΩ, 1%	Vishay Dale	WFCP06127L000FE66
C_{OUT1}, C_{OUT2}	100 µF, 63 V	Nichicon	UCM1J101MNS1GS
R_{VFBH}	75 kΩ, 0.1%	YAGEO	RT0805BRD0775KL
R_{VFBL}	2 kΩ, 0.1%	YAGEO	RT0603BRD072KL
R_{FB}	22 mΩ, 1%	ROHM Semiconductor	LTR50UZPFSR022
Q1, Q2	60 V, 11 mΩ	Infineon Technologies	IPB110P06LMATMA1

5 Constant voltage regulation

EZ-PD™ PMG1-B2 device's analog control loop can be configured in output voltage regulation mode to provide a constant output voltage irrespective of the input voltage and load variations. This is achieved by feeding a fraction of output voltage across FBH and FBL pins using the voltage divider resistor network shown in **Figure 29**.

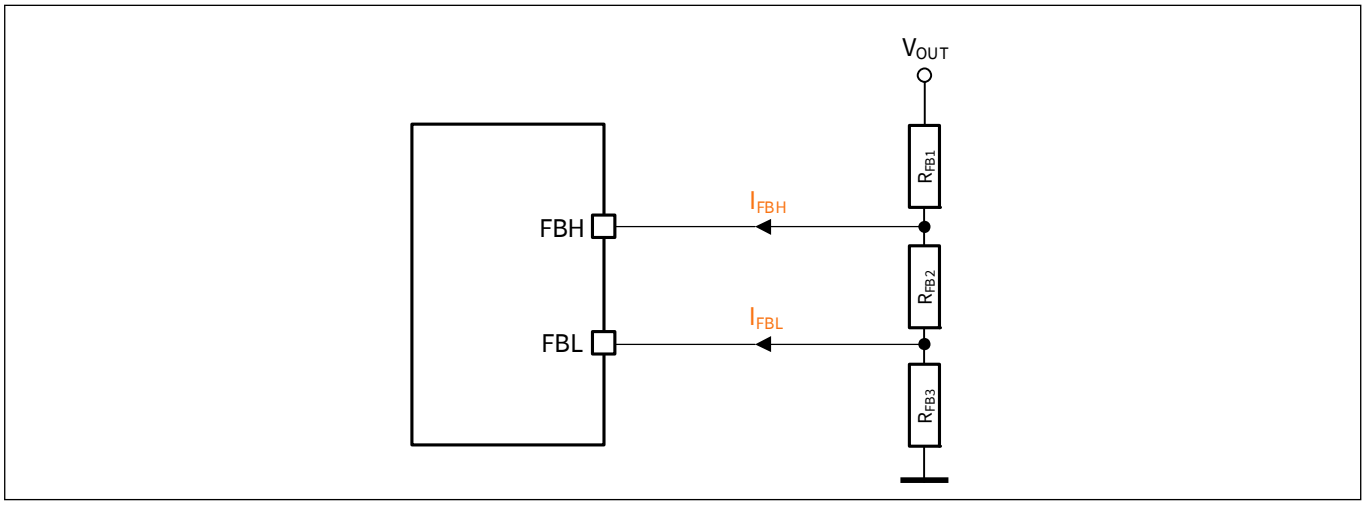


Figure 29 Configuring constant voltage output

The internal analog control system adjusts the buck-boost PWM control signals continuously to set a particular voltage across FBH and FBL pin based on the reference voltage applied at the SET pin (see **"Analog current control"** on page 22).

$$V_{OUT} = \left(I_{FBH} + \frac{V_{FBH} - V_{FBL}}{R_{FB2}}\right) \cdot R_{FB1} + \left(\frac{V_{FBH} - V_{FBL}}{R_{FB}} - I_{FBL}\right) \cdot R_{FB3} + V_{FBH-FBL} \quad \text{Eq. 25}$$

Note If analog control is performed using PWM_VSET pin (V_{SET} < 2 V) to change the output voltage, due to the variations on the I_{FBL} (I_{FBL_HSS} (**P_6.4.9**) and I_{FBL_LSS} (**P_6.4.40**)) current on the entire voltage spanning, a non-linearity in the output voltage may be observed with respect to V_{SET}. To minimize this effect, R_{FBx} resistors should be properly dimensioned referring to equation **Eq. 25**.

When a fixed output voltage is required, it is recommended to short SET pin to VREF pin externally, which results in 100% analog control with reference voltage (V_{SET} = 2 V). The output voltage can be then configured based on the values of R_{CVH} and R_{CVL} feedback resistor network as shown in **Figure 30** based on the simplified equation **Eq. 26**.

$$V_{OUT} = \left(\frac{V_{FBH-FBL}}{R_{CVH}} - I_{FBL}\right) \cdot R_{CVL} + V_{FBH-FBL} \quad \text{Eq. 26}$$

Note See **Figure 27** for more details on operating efficiency in CV mode.

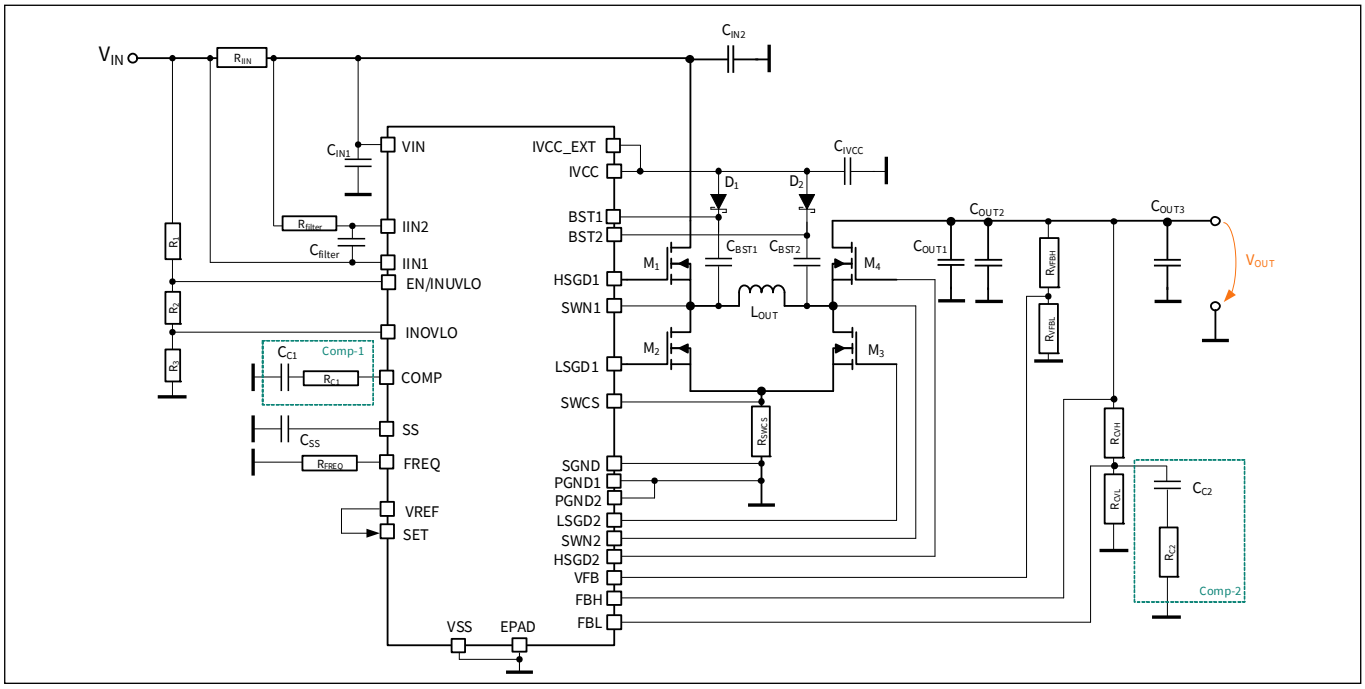


Figure 30 Constant voltage regulation using EZ-PD™ PMG1-B2

5.1 CV mode compensator

The response of the voltage regulator can be improved by adding an external compensator network in the feedback path as shown **Figure 31**, in addition to the compensator discussed in section, **"Compensator design"** on page 16. This secondary compensator helps to improve the bandwidth of the control loop thereby improving the transient response of the voltage regulator during dynamic load variations.

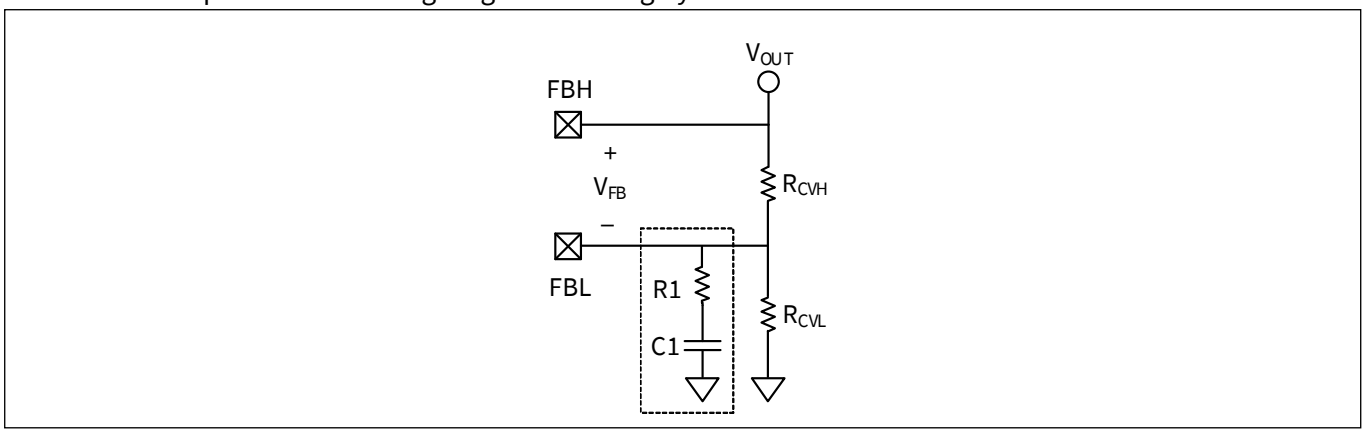


Figure 31 Additional compensator for CV mode

The transfer function of the compensator is given in **Eq. 27**. It acts as a lead compensator by providing an additional pole-zero pair to fine-tune the frequency response of the control loop.

$$H(s) = \frac{V_{FB(s)}}{V_{OUT(s)}} = \frac{R_{CVH}}{(R_{CVH} + R_{CVL})} \left(\frac{1 + s(R_1 + R_{CVL})C_1}{1 + s\left(R_1 + \frac{R_{CVH} \cdot R_{CVL}}{R_{CVH} + R_{CVL}}\right)C_1} \right) \quad \text{Eq. 27}$$

6 Application overview

6.1 1 to 12-cell lithium-ion battery charging with USB-C PD

EZ-PD™ PMG1-B2 device is a system-in-package (SIP) which provides both a microcontroller with USB PD interface, and a high-voltage buck-boost controller in a single package. This integration enables to design a high-power USB PD integrated battery charging system with up to 240 W power delivery. The analog buck-boost control system provides an option to adjust the charging current precisely, based on the charging state of the battery. The MCU firmware can be programmed to best-suit the charging profile of a particular battery type. The hardware ideally supports charging range for 1-12 cells Lithium batteries. The integrated hardware fault protections trigger quick responses whenever the system detects faults either at input or output, to prevent damages to the battery or the system. **Figure 32** and **Figure 33** show typical USB PD battery charging applications block diagram using the EZ-PD™ PMG1-B2 device.

6.1.1 Sink application

In the application shown in **Figure 32**, EZ-PD™ PMG1-B2 operates as a USB PD sink to charge battery using the USB PD power negotiated through the Type-C port. While functioning as sink, it negotiates the power with the connected USB PD source which is then used by the integrated buck-boost controller to charge the lithium-ion battery in constant-current (CC) mode.

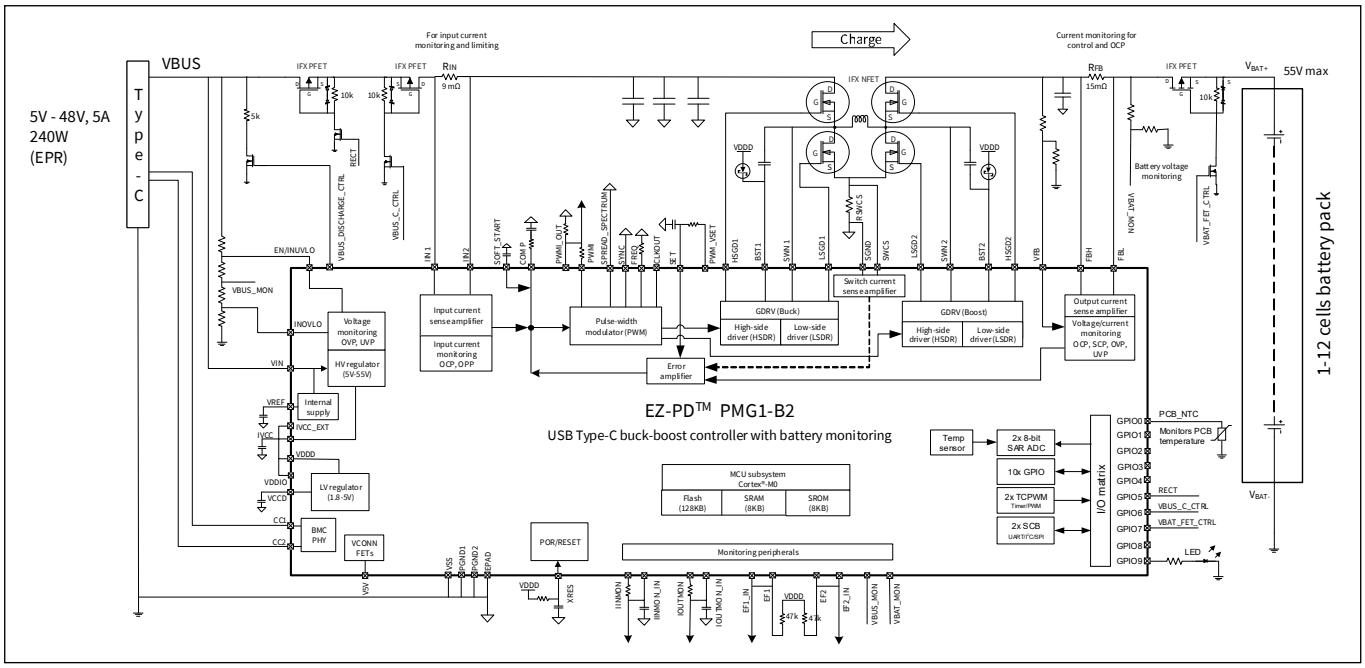


Figure 32 EZ-PD™ PMG1-B2 USB PD sink battery charging solution diagram

6.1.2 DRP application

The application shown in **Figure 33** operates in USB PD DRP role supporting battery charging using the USB PD power as well as sources the battery power back through USB PD on the Type-C port. While operating in the USB PD source mode, an external buck converter is used to draw power from the battery and convert the battery voltage into the negotiated Type-C bus voltage based on the PD contract with a USB PD sink device. The internal microcontroller handles the PD messaging and monitors the Type-C bus voltage to trigger fault protection as a PD source.

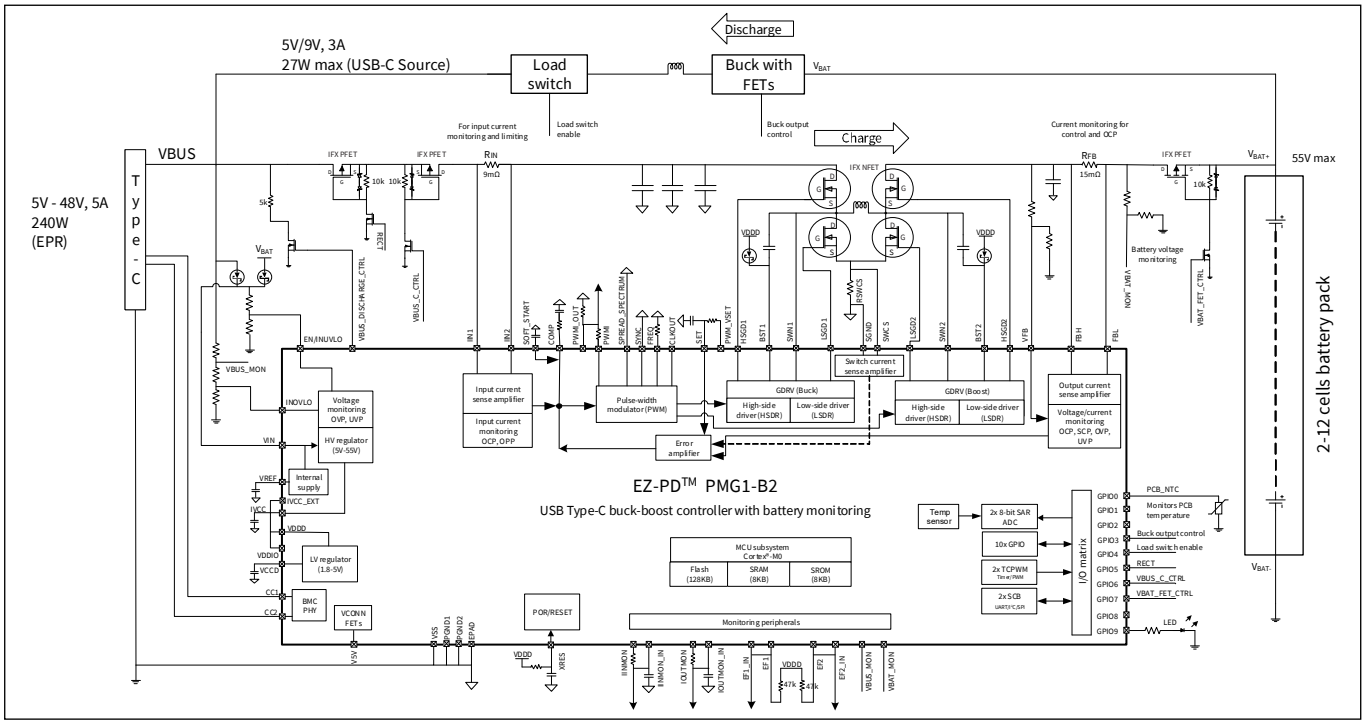


Figure 33 EZ-PD™ PMG1-B2 USB PD DRP battery charging solution diagram

6.2 Constant voltage output regulator with USB-C PD

The EZ-PD™ PMG1-B2 device can also be configured in constant voltage (CV) mode, where the system provides a constant output voltage by deriving USB-C PD power from the input Type-C port. This configuration is suited for power supply applications powered using USB-C. The output voltage regulation is achieved using the internal analog control loop, with minimal firmware usage. **Figure 34** shows the typical USB PD Sink CV mode application block diagram using the EZ-PD™ PMG1-B2 device that receives up to 240 W (48 V, 5 A) input power from USB-C EPR port and converts it into a fixed output voltage set by the hardware configuration.

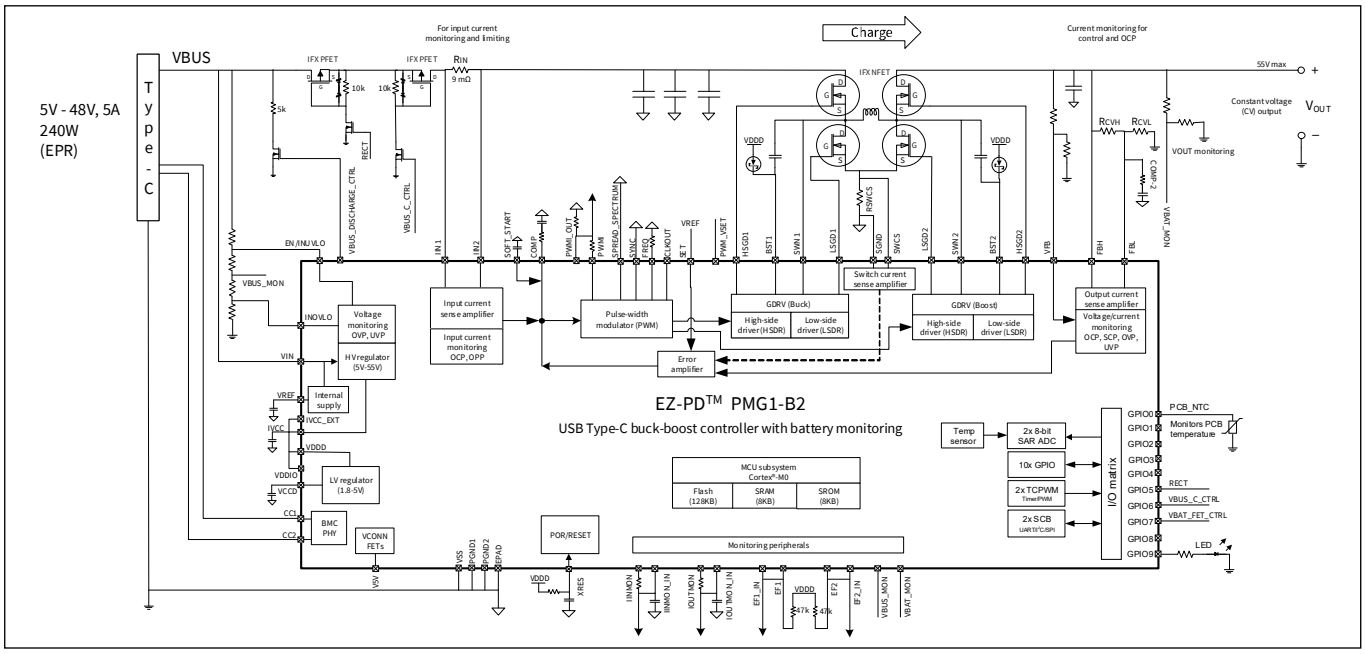


Figure 34 EZ-PD™ PMG1-B2 USB-C PD Sink with CV output regulation

6.3 External pin connections for application-level interface

EZ-PD™ PMG1-B2 integrates both microcontroller and buck-boost controller as a system-in-package (SIP). The package provides flexibility for the user to configure the system according to the application specific needs, thereby helping to reduce the redundant connection causing unwanted power flow. The device provides dedicated external pins for functions such as independent powering, monitoring, and error diagnostics. Some of these pins are bought out for externally connections such as RC filters, pull-up/down resistors, and bypass capacitors to achieve the complete system functionality. **Table 13** shows the recommended external connections (between Pin-1 and Pin-2) for a USB PD battery charging application design (**Figure 32** and **Figure 33**) using EZ-PD™ PMG1-B2.

Table 13 External pin connections for USB PD battery charging application

Function	Pin-1	Pin-2	Description
MCU power	IVCC	VDDD	Power for the MCU core and peripherals; connect external bypass capacitor
Input current monitoring	IINMON	IINMON_IN	To enable analog input current monitoring by the MCU; connect external RC filter
Output current monitoring	IOUTMON	IOUTMON_IN	To enable analog output current monitoring by the MCU; connect external RC filter
Error diagnostic flag	EF1	EF1_IN	To enable error monitoring by the MCU; connect external pull-up resistor
Error diagnostic flag	EF1	EF2_IN	To enable error monitoring by the MCU; connect external pull-up resistor
Output current monitoring	SET	PWM_VSET	Analog input referencing for buck-boost output current adjustment by the MCU; connect external RC filter
Buck-boost ON/OFF	PWMI	PWMI_OUT	To control the buck-boost switching by the MCU; connect external pull-down resistor

7 Electrical specifications

7.1 Absolute maximum ratings

Table 14 Absolute maximum ratings

T_J = –40°C to +125°C (unless otherwise specified)

Parameters	Description	Min	Typ	Max	Unit
VDDD_MAX	Max supply voltage relative to VSS	–	–	6	V
VDDIO_MAX	Maximum supply voltage relative to VSS	0.5	–	6	V
V5V_MAX	Max supply voltage relative to VSS	–	–	6	V
V_{GPIO_ABS}	GPIO voltage	–0.5	–	VDDIO+0.5	V
I_{GPIO_ABS}	Current per GPIO	–	–	25	mA
V_{VIN}	Supply input	–0.3	–	60	V
$V_{CC\_PIN\_ABS}$	CC1, CC2 pin voltage	0.5	–	6	V
V_{IVCC}	Internal linear voltage regulator output voltage	–0.3	–	6	V
V_{IVCC_EXT}	External linear voltage regulator input voltage	–0.3	–	6	V
V_{REF}	Voltage reference output	–0.3	–	3.6	V
$V_{LSGD1,2\text{-}PGND1,2}$	Low-side gate driver voltage	–0.3	–	5.5	V
$V_{HSGD1,2\text{-}SWN1,2}$	High-side gate driver voltage	–0.3	–	5.5	V
$V_{SWN1,\ 2}$	Switching node voltage	–1	–	60	V
$V_{BST1,2\text{-}SWN1,2}$	Bootstrap voltage	–0.3	–	6	V
$V_{BST1,\ 2}$	Bootstrap voltage relative to GND	–0.3	–	65	V
V_{SWCS}	Switch current sense input voltage	–0.3	–	0.3	V
V_{SGND}	Switch current sense GND voltage	–0.3	–	0.3	V
$V_{SWCS\text{-}SGND}$	Switch current sense differential voltage	–0.5	–	0.5	V
$V_{PGND1,2}$	Power GND voltage	–0.3	–	0.3	V
$V_{IIN1,\ 2}$	Input current monitor voltage	–0.3	–	60	V
$V_{IIN1\text{-}IIN2}$	Input current monitor differential voltage	–0.5	–	0.5	V
$V_{FBH,\ FBL}$	Feedback error amplifier voltage	–0.3	–	60	V
$V_{FBH\text{-}FBL}$	Feedback error amplifier differential voltage	–0.5	–	0.5	V
$V_{EN/INUVLO}$	Enable/Input undervoltage lockout	–0.3	–	60	V
V_{PWMI}	Digital input voltage	–0.3	–	5.5	V
V_{SYNC}	Synchronization input voltage	–0.3	–	5.5	V
V_{CLKOUT}	Clock output voltage	–0.3	–	5.5	V
$V_{SPREAD\_SPECTRUM}$	Spread spectrum input voltage	–0.3	–	5.5	V
V_{VFB}	Output voltage feedback	–0.3	–	5.5	V
V_{INOVLO}	Input overvoltage lockout	–0.3	–	5.5	V
$V_{EF1,2}$	Error flags output voltage	–0.3	–	5.5	V

Table 14 Absolute maximum ratings *(continued)*

T_J = –40°C to +125°C (unless otherwise specified)

Parameters	Description	Min	Typ	Max	Unit
V_{SET}	Analog control input voltage	–0.3	–	5.5	V
V_{COMP}	Compensation input voltage	–0.3	–	3.6	V
V_{SOFT_START}	Soft start voltage	–0.3	–	3.6	V
V_{FREQ}	Voltage at frequency selection pin	–0.3	–	3.6	V
V_{IINMON}	Voltage at input monitor pin	–0.3	–	3.6	V
$V_{IOUTMON}$	Voltage at output monitor pin	–0.3	–	5.5	V
T_J	Operating junction temperature	–40	–	125	°C
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2 (air discharge for pins CC1 and CC2)	–	–	8	kV
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2 (air discharge for pins CC1 and CC2)	–	–	15	kV
ESD_HBM	Electrostatic discharge human body model	–	–	2	kV
ESD_CDM	Electrostatic discharge charged device model	–	–	0.5	kV

7.2 Device-level specifications

Table 15 Device-level DC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	VDDD	Power supply input voltage	2.7	–	5.5	V	T_J = –40°C to +85°C, UFP modes
SID.PWR#1_A	VDDD	Power supply input voltage	3.0	–	5.5	V	T_J = –40°C to +85°C, DFP / DRP modes
SID.PWR#26	V5V	Power supply for VCONN	4.85	–	5.5	V	T_J = –40°C to +85°C, DFP / DRP modes
SID.PWR24	VCCD	Output voltage for core logic	–	1.8	–	V	–
SID.PWR#4	IDD12	Supply current	–	10	–	mA	V5V = 5 V, T_J = 25°C, CC IO IN Transmit or Receive, no I/O sourcing current, CPU at 24 MHz, two PD ports active
SID.PWR#7	VDDWRITE	Supply voltage for flash write	2.70	–	5.5	V	T_J = –40°C to +85°C, ALL VDDD.
SID.PWR#13	VDDIO	Supply voltage for IO	1.71	–	VDDD	V	T_J = –40°C to +85°C, 2.7 V < VDDD < 5.5 V
SID.PWR#15	C_{EFC}	External regulator voltage bypass for VCCD	80	100	120	nF	X5R ceramic or better
SID.PWR#16	C_{EXC}	Power supply decoupling capacitor for VDDD	0.8	1	–	µF	X5R ceramic or better

Table 15 Device-level DC specifications *(continued)*

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#27	C_{EXV}	Power supply decoupling capacitor for V5V_1 and V5V_2	–	0.1	–	µF	X5R ceramic or better
MCU current consumption in Sleep mode, VDDD =2.7 V to 5.5 V, typical values measured at 5 V and T_J = 25°C							
SID25A	IDD20A	I2C wakeup. WDT on. IMO at 48 MHz	–	2.5	4	mA	VDDD = 5 V, T_J = 25°C, All blocks except CPU are on, CC IO on, no I/O sourcing current
SID25B	IDD20B	I2C wakeup. WDT on. IMO at 48 MHz	–	3	5	mA	VDDD = 5 V, T_J = 25°C, All blocks except CPU are on, CC IO on, no I/O sourcing current for two PD ports
MCU current consumption in Deep Sleep mode, typical values measured at T_J = 25°C							
SID_DS	IDD_DS	VDDD = 5 V. CC wakeup ON	–	5	–	µA	Power Source = VDDD, Type-C Not Attached, CC enabled for wakeup, Rp disabled.
SID_DS1	IDD_DS1	VDDD = 5 V. CC wakeup ON	–	120	–	µA	Power source = VDDD, Type-C Not attached, CC enabled for wakeup, Rp and Rd connected at 70 ms intervals by CPU. Rp, Rd connection should be enabled for both PD ports.
SID34	IDD29	VDDD = 2.7 to 5.5 V. I2C wakeup and WDT ON.	–	50	–	µA	VDDD = 5 V, T_J = 25°C
SID34A	IDD29A	VDDD = 2.7 to 5.5 V. I2C wakeup and WDT ON.	–	60	–	µA	VDDD = 5 V, T_J = 25°C for two PD ports
SID307	IDD_XR	Supply current while XRES asserted	–	2	20	µA	Power Source = VDDD = 5 V, Type-C not attached, T_J = 25°C

Table 16 Device-level AC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#20	t_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	–
SID.PWR#21	$t_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–	µs	–

7.2.1 I/O

Table 17 I/O DC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	T_J = +25°C, all VDDIO
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	T_J = +25°C, all VDDIO
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	T_J = +25°C, 5V VDDIO
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3	7	pF	T_J = –40°C to +85°C, all VDDIO, all package, all I_{OS}
SID.GIO#25	R_{SW}	Switch resistance from port pin to AMUX	–	–	400	Ω	T_J = –40°C to +85°C, all VDDIO, absolute maximum
SID.GIO#26	R_{GND}	Switch resistance from port pin to ground	–	–	400	Ω	T_J = –40°C to +85°C, ALL VDDIO, absolute maximum
SID.GIO#33	V_{OH_3V}	Output voltage high level	VDDIO-0.6	–	–	V	I_{OH} = –4 mA at 3 V VDDIO
SID.GIO#34	$V_{OH\_1.8V}$	Output voltage high level	VDDIO-0.5	–	–	V	I_{OH} = –1 mA at 1.8V VDDIO
SID.GIO#35	$V_{OL\_1.8V}$	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA at 1.8V VDDIO
SID.GIO#36	V_{OL_3V}	Output voltage low level	–	–	0.6	V	I_{OL} = 10 mA (IOL_LED) at 3 V VDDIO
SID.GIO#37	V_{IH_CMOS}	Input voltage high threshold	0.7×VDDIO	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage low threshold	–	–	0.3×VDDIO	V	CMOS input
SID.GIO#39	$V_{IH\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	0.7×VDDIO	–	–	V	–
SID.GIO#40	$V_{IL\_VDDIO2.7-}$	LVTTL input, VDDIO < 2.7 V	–	–	0.3×VDDIO	V	–
SID.GIO#41	$V_{IH\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	2	–	–	V	–
SID.GIO#42	$V_{IL\_VDDIO2.7+}$	LVTTL input, VDDIO ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#43	V_{HYSTTL}	Input hysteresis LVTTL VDDIO > 2.7 V	15	40	–	mV	–
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05×VDDIO	–	–	mV	VDDIO < 4.5 V
SID.GIO#44A	$V_{HYSCMOS55}$	Input hysteresis CMOS	200	–	–	mV	VDDIO > 4.5 V

Table 17 I/O DC specifications *(continued)*

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	–
SID69	I_{DIODE}	Current through protection diode to VDDIO/VSS	–	–	100.0	µA	–

Table 18 I/O AC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	t_{RISEF}	Rise time in fast strong mode	2	–	12	ns	5 V VDDIO, C_{load} = 25 pF
SID71	t_{FALLF}	Fall time in fast strong mode	2	–	12	ns	5 V VDDIO, C_{load} = 25 pF
SID.GIO#46	t_{RISES}	Rise time in slow strong mode	10	–	60	ns	5 V VDDIO, C_{load} = 25 pF
SID.GIO#47	t_{FALLS}	Fall time in slow strong mode	10	–	60	ns	5 V VDDIO, C_{load} = 25 pF
SID.GIO#48	f_{GPIO_OUT1}	GPIO F_{out}; 3.3 V ≤ VDDIO ≤ 5.5 V. Fast strong mode.	–	–	16	MHz	90/10%, 25 pF load
SID.GIO#49	f_{GPIO_OUT2}	GPIO F_{out}; 1.71 V ≤ VDDIO ≤ 3.3 V. Fast strong mode.	–	–	16	MHz	90/10%, 25 pF load
SID.GIO#50	f_{GPIO_OUT3}	GPIO F_{out}; 3.3 V ≤ VDDIO ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load
SID.GIO#51	f_{GPIO_OUT4}	GPIO F_{out}; 1.71 V ≤ VDDIO ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load
SID.GIO#52	f_{GPIO_IN}	GPIO input operating frequency; 1.71 V ≤ VDDIO ≤ 5.5 V	–	–	16	MHz	90/10% V_{IO}

7.2.2 XRES

Table 19 XRES specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.XRES#1	V_{IH_XRES}	Input voltage high threshold on XRES pin	0.7×VDDIO	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage low threshold on XRES pin	–	–	0.3×VDDIO	V	CMOS input
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin	–	–	7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin	–	0.05×VDDIO	–	mV	–

Table 19 XRES specifications *(continued)*

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.XRES#5	t_{XRES}	External reset pulse width	5	–	–	us	T_J = –40°C to +85°C, all VDDIO
SID.XRES#6	t_{XRES_GF}	External reset glitch filter period	–	20	–	ns	T_J = –40°C to +85°C, all VDDIO

7.3 Digital peripherals

7.3.1 Pulse-width-modulation (PWM)

Table 20 PWM DC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	I_{TCPWM1}	Block current consumption at 3 MHz	–	–	45	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2	I_{TCPWM2}	Block current consumption at 8 MHz	–	–	145	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2A	I_{TCPWM3}	Block current consumption at 16 MHz	–	–	160	µA	All modes (Timer/Counter/PWM)

Table 21 PWM AC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	f_c	MHz	f_{cmax} = CLK_SYS. Maximum = 48 MHz
SID.TCPWM.4	$t_{PWMENEXT}$	Input trigger pulse width	$2/f_c$	–	–	ns	For all trigger events[4]
SID.TCPWM.5	t_{PWMEXT}	Output trigger pulse widths	$2/f_c$	–	–	ns	Minimum possible width of overflow, underflow, and CC (counter equals compare value) outputs
SID.TCPWM.5A	t_{CRES}	Resolution of counter	$1/f_c$	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM resolution	$1/f_c$	–	–	ns	Minimum pulse width of PWM output

Note

4. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

7.3.2 I²C

Table 22 I²C DC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	60	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	185	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390	µA	–
SID152	I_{I2C4}	I2C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 23 I²C AC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	f_{I2C1}	Bit rate	–	–	1	Mbps	–

7.3.3 UART

Table 24 UART DC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	125	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	µA	–

Table 25 UART AC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	f_{UART}	Bit rate	–	–	1	Mbps	–

7.3.4 SPI

Table 26 SPI DC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	–

Table 27 SPI AC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	f_{SPI}	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 28 Fixed SPI Master mode AC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID167	t_{DMO}	MOSI valid after SCLK driving edge	–	–	15	ns	–
SID168	t_{DSI}	MISO valid before SCLK capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	t_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge

Table 29 Fixed SPI Slave mode AC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID170	t_{DMI}	MOSI valid before SCLK capturing edge	40	–	–	ns	–
SID171	t_{DSO}	MISO valid after SCLK driving edge	–	–	$48 + 3 \times t_{scb}$	ns	$t_{scb} = t_{cpu} = 1/24$ MHz
SID171A	t_{DSO_EXT}	MISO valid after SCLK driving edge in External Clock mode	–	–	48	ns	–
SID172	t_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$t_{SSELSCK}$	SSEL valid to first SCLK valid edge	100	–	–	ns	–

7.4 Memory

Table 30 Memory size specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#1	FLASH_SIZE	Flash memory size	–	128	–	KB	SONOS flash amount (bytes)
SID.MEM#2	SRAM_SIZE	SRAM memory size	–	8	–	KB	SRAM amount (bytes)

Table 31 Flash macro specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#3	$t_{FLASH\_ROW\_ERASE}$[5]	Row erase time	–	–	13	ms	T_J = –40°C to +85°C, all VDDD
SID.MEM#4	$t_{FLASH\_ROW\_WRITE}$[5]	Row (block) write time (erase and program)	–	–	20	ms	T_J = –40°C to +85°C, all VDDD
SID.MEM#6	FLASH_END	Flash write endurance	100K	–	–	cycles	T_J = –40°C to 55°C, all VDDD
SID.MEM#8	$t_{FLASH\_ROW\_PGM}$[5]	Row program time after erase	–	–	7	ms	T_J = –40°C to 55°C, all VDDD
SID178	$t_{BULKERASE}$[5]	Bulk erase time (128 KB)	–	–	35	ms	–
SID180	$t_{DEVPROG}$[5]	Total device program time	–	–	25	secs	–
SID182	f_{RET1}	Flash retention, $T_J \le 55°C$, 100K P/E cycles	20	–	–	years	–
SID182A	f_{RET2}	Flash retention, $T_J \le 85°C$, 10K P/E cycles	10	–	–	years	–

7.5 System resources

7.5.1 Power-on-reset (POR)

Table 32 Imprecise POR specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID185	$V_{RISEIPOR}$	POR rising trip voltage	0.8	–	1.5	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.7	–	1.4	V	–

Table 33 Precise POR specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	$V_{FALLPPOR}$	Brownout detect (BOD) trip voltage Active/ Sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

7.5.2 SWD interface

Table 34 SWD specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.SWD#1	$f_{SWDCLK1}$	3.3 V ≤ VDDIO ≤ 5.5 V	–	–	14	MHz	–
SID.SWD#2	$f_{SWDCLK2}$	1.8 V ≤ VDDIO ≤ 3.3 V	–	–	7	MHz	–
SID.SWD#3	t_{SWDI_SETUP}	t = 1/f_{SWDCLK}	0.25 × t	–	–	ns	–
SID.SWD#4	t_{SWDI_HOLD}	t = 1/f_{SWDCLK}	0.25 × t	–	–	ns	–
SID.SWD#5	t_{SWDO_VALID}	t = 1/f_{SWDCLK}	–	–	0.50 × t	ns	–
SID.SWD#6	t_{SWDO_HOLD}	t = 1/f_{SWDCLK}	1	–	–	ns	–

7.5.3 Internal main oscillator (IMO)

Table 35 IMO AC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#1	f_{IMO}	IMO frequency	24	–	48	MHz	T_J = –40°C to +85°C, all VDDD
SID.CLK#2	f_{IMO_RES}	IMO frequency resolution	–	0.25	–	%	T_J = –40°C to +85°C, all VDDD
SID.CLK#3	IMO_STL	IMO settling time when trim register is changed	–	–	200	ns	T_J = 25°C, all VDDD, 48 MHz ≥ f_{IMO} ≥ 24 MHz
SID.CLK#4	f_{CPU}	CPU input frequency	0	–	16	MHz	T_J = –40°C to +85°C, all VDDD
SID.CLK#6	SR_POWER_UP	Power supply slew rate during power up	1	–	67	V/ms	T_J = –40°C to +85°C, all VDDD
SID.CLK#13	f_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	2.7 V ≤ VDDD < 5.5 V and –25°C ≤ T_J ≤ 85°C
SID.CLK#14	IMO_HOP_RANGE	f_{IMO} variation range with TRIM registers	–10	–	10	%	T_J = 25°C, all VDDD, 48 MHz ≥ f_{IMO} ≥ 24 MHz
SID218	IMO1	IMO operating current at 48 MHz	–	–	250	µA	–
SID219	IMO2	IMO operating current at 24 MHz	–	–	180	µA	–
SID226	$t_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID228	$t_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–

Note

5. It can take as much as 20 ms to write to flash. During this time the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

7.5.4 Internal low-speed oscillator (ILO)

Table 36 ILO AC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#5	f_{ILO}	ILO frequency	20	40	80	KHz	–
SID231	I_{ILO1}	ILO operating current	–	0.3	1	µA	–
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	–
SID234	$t_{STARTILO1}$	ILO start-up time	–	–	2	ms	–
SID238	ILODUTY	ILO duty cycle	40	50	60	%	–
SID305	EXTCLKFREQ	External clock input frequency	–	–	16	MHz	–
SID306	EXTCLKDUTY	Duty cycle; measured at VDDD/2	45	–	55	%	–
SID262	$t_{CLKSWITCH}$	System clock source switching time	3	–	4	Periods	–

7.5.5 System timers

Table 37 System timer specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TMR#1	SYS_TIM_RES	System timer resolution	–	16	–	bits	T_J = –40°C to +85°C, all VDDD
SID.TMR#2	WDT_RES	Watchdog timer resolution	–	16	–	bits	T_J = –40°C to +85°C, all VDDD

7.5.6 USB power delivery

Table 38 USB PD DC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.1	Rp_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5 A power	166	180	194	µA	–
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0 A power	304	330	356	µA	–
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP dead-battery CC termination on CC1 and CC2	4.08	5.1	6.12	kΩ	Applicable only for packages supporting DRP. Keep the device OFF and apply 1 V on CC1 and CC2 pins to measure the impedance. For DFP, RD1, RD2 will not be bonded to CC1 and CC2.
SID.PD.15	$V_{DROP\_V5V\_CC1}$	Voltage drop from V5V pin to CC1 pin while sourcing 215 mA	–	–	100	mV	–
SID.PD.16	$V_{DROP\_V5V\_CC2}$	Voltage drop from V5V pin to CC2 pin while sourcing 215 mA	–	–	100	mV	–

7.5.7 Analog-to-digital converter (ADC)

Table 39 ADC DC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	bits	–
SID.ADC.2	INL	Integral non-linearity	–1.50	–	1.50	LSB	–
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1	–	1	LSB	–

Table 40 ADC AC specifications

T_J = –40°C to +125°C (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.5	SLEW_MAX	Rate of change of sampled voltage signal	–	–	3	V/ms	–

7.6 Buck-boost controller

Table 41 Buck-boost controller functional range

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_4.2.2	V_{VIN}	Device nominal supply voltage range	4.5	–	55	V	–
P_4.2.5	V_{POW}	Power stage voltage range	4.5	–	55	V	Not subject to production test, specified by design

7.6.1 Buck-boost power supply

Table 42 Power supply DC specifications

VIN = 5 V to 48 V, T_J = –40°C to +125°C, all voltages with respect to EPAD (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_5.3.1	$V_{VIN(ON)}$	Input voltage startup	–	–	4.7	V	VIN increasing; $V_{EN/INUVLO}$ = HIGH; $I_{IVCC} = I_{IVCC\_EXT}$ = 10 mA
P_5.3.14	$V_{VIN(OFF)}$	Input undervoltage switch off	–	–	4.5	V	VIN decreasing; $V_{EN/INUVLO}$ = HIGH; $I_{IVCC} = I_{IVCC\_EXT}$ = 10 mA
P_5.3.2	$I_{VIN(ACTIVE)}$	Device operating current	–	4.4	6	mA	Active mode; CLKOUT freq. 300 kHz; CLKOUT capacitive load 20 pF; V_{PWMI} = 0 V
P_5.3.3	$I_{VIN(SLEEP)}$	VIN Sleep mode supply current	–	–0.1	1.5	µA	$V_{EN/INUVLO}$ = 0 V; VIN = 9 V; $V_{IVCC} = V_{IVCC\_EXT}$ = 0 V

Table 43 EN/INUVLO pin specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_5.3.7	$V_{EN/INUVLOth}$	Input undervoltage falling threshold	1.6	1.75	1.9	V	–
P_5.3.8	$V_{EN/INUVLO(HYST)}$	EN/INUVLO rising hysteresis	–	90	–	mV	Not subject to production test, specified by design
P_5.3.9	$I_{EN/INUVLO(LOW)}$	EN/INUVLO input current LOW	0.45	0.89	1.34	µA	$V_{EN/INUVLO}$ = 0.8 V
P_5.3.10	$I_{EN/INUVLO(HIGH)}$	EN/INUVLO input current HIGH	1.1	2.2	3.3	µA	$V_{EN/INUVLO}$ = 2 V

Table 44 Buck-boost wakeup timing

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_5.3.11	t_{ACTIVE}	Sleep mode to Active time	–	–	0.7	ms	Not subject to production test, specified by design.

7.6.2 Buck-boost control system

Table 45 Feedback control specifications

VIN = 5 V to 48 V, T_J = –40°C to +125°C, all voltages with respect to EPAD (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_6.4.1	$V_{(FBH-FBL)}$	$V_{(FBH-FBL)}$ threshold	145.5	150	154.5	mV	V_{SET} = 2 V; V_{FBH} = 150 mV to 60 V; maximum ±3% deviation
P_6.4.6	$V_{(FBH-FBL)\_10}$	$V_{(FBH-FBL)}$ threshold at analog control 10%	10	15	20	mV	V_{SET} = 0.32 V; V_{FBH} = 150 mV to 60 V
P_6.4.8	I_{FBH_HSS}	FBH bias current with high-side sensing setup	65	110	155	µA	Not subject to production test, specified by design. V_{FBL} = 7 V; $V_{FBH–FBL}$ = 150 mV
P_6.4.9	I_{FBL_HSS}	FBL bias current with high-side sensing setup	17	30	43	µA	Not subject to production test, specified by design. V_{FBL} = 7 V; $V_{FBH–FBL}$= 150 mV
P_6.4.39	I_{FBH_LSS}	FBH bias current with low-side sensing setup	-7.5	-4	-2.5	µA	Not subject to production test, specified by design. V_{FBL} = 0 V; $V_{FBH\ -FBL}$ = 150 mV
P_6.4.40	I_{FBL_LSS}	FBL bias current with low-side sensing setup	-45	-30	-20	µA	Not subject to production test, specified by design. V_{FBL} = 0 V; $V_{FBH\ -FBL}$ = 150 mV
P_6.9.1	$V_{FBH\_HSS\_inc}$	FBH-FBL High Side sensing entry threshold	–	2	–	V	V_{FBH} increasing; Not subject to production test, specified by design.
P_6.9.2	$V_{FBH\_HSS\_dec}$	FBH_FBL High Side sensing exit threshold	–	1.75	–	V	V_{FBH} decreasing; Not subject to production test, specified by design.
P_6.4.10	$IFBx_{gm}$	Output current sense amplifier transconductance (g_m)	–	890	–	µS	Not subject to production test, specified by design.
P_6.4.11	$V_{IOUTMON}$	Output monitor voltage	1.33	1.4	1.47	V	$V_{FBH\ -FBL}$ = 150 mV
P_6.4.12	D_{BOOST_MAX}	Maximum BOOST duty cycle	89	91	93	%	Not subject to production test, specified by design. f_{SW} = 300 kHz
P_6.4.13	$V_{(IIN1-IIN2)\_th}$	Input current sense threshold $V_{IIN1-IIN2}$	46	50	54	mV	V_{IIN1} = $V_{VIN(ON)}$ to 60 V
P_6.4.14	I_{IN_gm}	Input current sense amplifier transconductance (g_m)	–	2.12	–	mS	Not subject to production test, specified by design
P_6.4.15	V_{IINMON}	Input current monitor voltage	0.95	1	1.05	V	Not subject to production test, specified by design. $V_{IIN1–IIN2}$ = 50 mV; V_{IIN1} = $V_{VIN(ON)}$ to 55 V

Table 45 Feedback control specifications *(continued)*

VIN = 5 V to 48 V, T_J = –40°C to +125°C, all voltages with respect to EPAD (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_10.8.15	V_{SWCS_BOOST}	Switch peak overcurrent threshold - BOOST	40	50	60	mV	Not subject to production test, specified by design
P_10.8.16	V_{SWCS_BUCK}	Switch peak overcurrent threshold - BUCK	-60	-50	-40	mV	Not subject to production test, specified by design

Table 46 Soft-start specifications

VIN = 5 V to 48 V, T_J = –40°C to +125°C, all voltages with respect to EPAD (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_6.4.19	$I_{SOFT\_START\_PU}$	Soft start pull-up current	22	26	32	µA	V_{SOFT_START} = 1 V
P_6.4.20	$I_{SOFT\_START\_PD}$	Soft start pull-down current	2.2	2.6	3.2	µA	V_{SOFT_START} = 1 V
P_6.4.21	$V_{SOFT\_START\_LOFF}$	Soft start latch-off threshold	1.65	1.75	1.85	V	–
P_6.4.22	$V_{SOFT\_START\_RESET}$	Soft start reset threshold	0.1	0.2	0.3	V	–
P_6.9.3	$V_{SOFT\_START\_REG}$	Soft start voltage during regulation	1.9	2	2.1	V	Not subject to production test, specified by design. No faults

Table 47 Oscillator specifications

V_{IN} = 5 V to 48 V, T_J = –40°C to +125°C, all voltages with respect to EPAD (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_6.4.23	f_{SW}	Switching frequency	285	300	315	kHz	T_j = 25°C; R_{FREQ} = 37.4 kΩ; +/-5% accuracy
P_6.4.24	f_{SYNC}	SYNC frequency	200	–	700	kHz	–
P_6.4.25	$V_{SYNC,ON}$	SYNC turn-on threshold	2	–	–	V	–
P_6.4.26	$V_{SYNC,OFF}$	SYNC turn-off threshold	–	–	0.8	V	–
P_6.4.62	$I_{SYNC,H}$	SYNC high-input current	15	30	45	µA	V_{SYNC} = 2.0 V
P_6.4.63	$I_{SYNC,L}$	SYNC low-input current	6	12	18	µA	V_{SYNC} = 0.8 V

Table 48 Gate-driver specifications

VIN = 5 V to 48 V, T_J = –40°C to +125°C, all voltages with respect to EPAD (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_6.4.64	$V_{BST1,2}–V_{SWN1,2\_UVth}$	Gate driver undervoltage threshold	3.4	–	4	V	$V_{BST1,2}–V_{SWN1,2}$ decreasing
P_6.4.28	$R_{DS(ON\_PU)HS}$	HSGD1,2 NMOS driver on-state resistance (Gate pull up)	1.4	2.3	3.7	Ω	$V_{BST1,2}–V_{SWN1,2}$ = 5 V; I_{source} = 100 mA
P_6.4.29	$R_{DS(ON\_PD)\ HS}$	HSGD1,2 NMOS driver on-state resistance (Gate pull down)	0.6	1.2	2.2	Ω	$V_{BST1,2}–V_{SWN1,2}$ = 5 V; I_{sink} = 100 mA
P_6.4.30	$R_{DS(ON\_PU)LS}$	LSGD1,2 NMOS driver on-state resistance (Gate pull up)	1.4	2.3	3.7	Ω	V_{IVCC_EXT} = 5 V; I_{source} = 100 mA
P_6.4.31	$R_{DS(ON\_PD)LS}$	LSGD1,2 NMOS driver on-state resistance (Gate pull down)	0.4	1.2	1.8	Ω	V_{IVCC_EXT} = 5 V; I_{sink} = 100 mA
P_6.4.32	$I_{HSGD1,2\_SRC}$	HSGD1,2 Gate driver peak sourcing current	380	–	–	mA	Not subject to production test, specified by design. $V_{HSGD1,2}–V_{SWN1,2}$ = 1 V to 4 V; $V_{BST1,2}–V_{SWN1,2}$= 5 V
P_6.4.33	$I_{HSGD1,2\_SNK}$	HSGD1,2 Gate driver peak sinking current	410	–	–	mA	Not subject to production test, specified by design. $V_{HSGD1,2}–V_{SWN1,2}$ = 4 V to 1 V; $V_{BST1,2}–V_{SWN1,2}$ = 5 V
P_6.4.34	$I_{LSGD1,2\_SRC}$	LSGD1,2 Gate driver peak sourcing current	370	–	–	mA	Not subject to production test, specified by design. $V_{LSGD1,2}$ = 1 V to 4 V; V_{IVCC_EXT} = 5 V
P_6.4.35	$I_{LSGD1,2\_SNK}$	LSGD1,2 Gate driver peak sinking current	550	–	–	mA	Not subject to production test, specified by design. $V_{LSGD1,2}$ = 4 V to 1 V; V_{IVCC_EXT} = 5 V
P_6.4.36	$t_{LSOFF-HSON\_delay}$	LSGD1,2 OFF to HSGD1,2 ON delay (dead-time)	15	30	40	ns	Not subject to production test, specified by design
P_6.4.37	$t_{HSOFF-LSON\_delay}$	HSGD1,2 OFF to LSGD1,2 ON delay (dead-time)	35	60	75	ns	Not subject to production test, specified by design

7.6.3 Buck-boost control inputs

Table 49 Digital control specifications

VIN = 5 V to 48 V, T_J = –40°C to +125°C, all voltages with respect to EPAD (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_7.2.1	$V_{PWMI,ON}$	PWMI turn-on threshold	2	–	–	V	–
P_7.2.2	$V_{PWMI,OFF}$	PWMI turn-off threshold	–	–	0.8	V	–
P_7.2.4	$I_{PWMI,H}$	PWMI high input current	15	30	45	µA	V_{PWMI} = 2.0 V
P_7.2.5	$I_{PWMI,L}$	PWMI low input current	6	12	18	µA	V_{PWMI} = 0.8 V

Table 50 Analog control specifications

VIN = 5 V to 48 V, T_J = –40°C to +125°C, all voltages with respect to EPAD (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_8.3.4	I_{SET_source}	Source current on SET pin	–	–	1	µA	V_{SET} = 0.2 V to 1.4 V

7.6.4 Internal LDO

Table 51 LDO DC specifications

VIN = 5 V to 48 V, T_J = –40°C to +125°C, all voltages with respect to EPAD (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_9.2.1	V_{IVCC}	Output voltage	4.8	5	5.2	V	VIN= 9 V; 0.1 mA ≤ I_{IVCC} ≤ 50 mA
P_9.2.2	I_{LIM}	Output current limitation	70	90	110	mA	V_{IVCC} = 4 V; Not subject to production test, specified by design
P_9.2.3	V_{DR}	Dropout voltage (VIN-V_{IVCC})	–	200	350	mV	VIN = 5 V; I_{IVCC}= 10 mA
P_9.2.4	C_{IVCC}	IVCC buffer capacitor	10	–	–	µF	Not subject to production test, specified by design [6]
P_9.2.5	$V_{IVCC\_EXT\_RTH,D}$	IVCC_EXT undervoltage reset switch OFF threshold	3.7	3.9	4.1	V	V_{IVCC_EXT} decreasing
P_9.2.9	$V_{IVCC\_RTH,D}$	IVCC undervoltage reset switch OFF threshold	3.7	3.9	4.1	V	Selection of external switching MOSFET is crucial. V and V_{min} as worst case V must be considered. V_{IVCC} decreasing
P_9.2.6	V_{IVCCX_HYST}	IVCC and IVCC_EXT undervoltage hysteresis	0.335	0.3365	0.3695	V	V_{IVCC} increasing; V_{IVCC_EXT} increasing
P_9.2.8	V_{REF}	V_{REF} voltage	1.94	2	2.06	V	0 ≤ I_{VREF} ≤ 200 µA

Note

6. Minimum value given is needed for regulator stability; application might need higher capacitance than the minimum. Use capacitors with low ESR.

7.6.5 Fault protections

Table 52 Protection and diagnosis specifications

VIN = 5 V to 48 V, T_J = –40°C to +125°C, all voltages with respect to EPAD (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Short-circuit protection							
P_10.8.1	V_{VFB_S2G}	Short to GND threshold	0.53	0.563	0.59	V	V_{VFB} decreasing
Temperature protection							
P_10.8.4	T_{j_SD}	Overtemperature shutdown	160	175	190	°C	Specified by design; not subject to production test
P_10.8.5	$T_{j\_SD\_HYST}$	Overtemperature shutdown hysteresis	–	10	–	°C	Specified by design; not subject to production test
Output overvoltage protection							
P_10.8.6	V_{VFB_OVth}	VFB overvoltage feedback threshold	1.42	1.46	1.5	V	–
P_10.8.7	$V_{VFB\_OVth,HYS}$	Output overvoltage feedback hysteresis	25	40	58	mV	Output voltage decreasing
Open load and Open feedback diagnostics							
P_10.8.9	$V_{VFB\_OL,RISE}$	Open load rising threshold	1.29	1.34	1.39	V	$V_{FBH-FBL}$ = 0 V
P_10.8.10	$V_{FBH\_FBL\_OL}$	Open load reference voltage $V_{FBH-FBL}$	–	15	22.5	mV	V_{FB}= 1.4 V
P_10.8.11	$V_{VFB\_OL,FALL}$	Open load falling threshold	1.23	1.28	1.33	V	$V_{FBH-FBL}$ = 0 V
Input overvoltage protection							
P_10.8.12	$V_{INOVLOth}$	Input overvoltage rising threshold	1.9	2	2.1	V	–
P_10.8.13	$V_{INOVLO(HYST)}$	Input overvoltage threshold hysteresis	18	40	62	mV	–
Error diagnosis flags							
P_10.8.14	$R_{EF1,2}$	EF1,2 pin output impedance	–	2.1	–	kΩ	Specified by design; not subject to production test. Fault condition[6], I = 100 µA

Note

7. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

7.6.6 Spread spectrum

Table 53 Spread spectrum specifications

VIN = 5 V to 48 V, T_J = –40°C to +125°C, all voltages with respect to EPAD (unless otherwise specified)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
P_11.6.2	f_{dev}	Frequency deviation	–	±16	–	%	SPREAD_SPECTRUM = HIGH; Specified by design; not subject to production test.
P_11.6.3	f_{FM}	Frequency modulation	–	12	–	kHz	SPREAD_SPECTRUM = HIGH; Specified by design; not subject to production test.
SPREAD_SPECTRUM input pin characteristics							
P_11.6.5	$V_{SPREAD\_SPECTRUM,ON}$	SPREAD_SPECTRUM turn-on threshold	2	–	–	V	–
P_11.6.6	$V_{SPREAD\_SPECTRUM,OFF}$	SPREAD_SPECTRUM turn-off threshold	–	–	0.8	V	–
P_11.6.8	$I_{SPREAD\_SPECTRUM,H}$	SPREAD_SPECTRUM high-input current	15	30	45	µA	$V_{SPREAD\_SPECTRUM}$ = 2.0 V
P_11.6.9	$I_{SPREAD\_SPECTRUM,L}$	SPREAD_SPECTRUM low-input current	6	12	18	µA	$V_{SPREAD\_SPECTRUM}$ = 0.8 V
CLKOUT output pin characteristics							
P_11.6.10	$V_{CLKOUT(L)}$	L level output voltage	0	–	0.4	V	I_{CLKOUT}= –2 mA
P_11.6.11	$V_{CLKOUT(H)}$	H level output voltage	V_{IVCC}–0.4 V	–	V_{IVCC}	V	I_{CLKOUT}= 2 mA

8 Performance characteristics

Typical performance characteristics of device

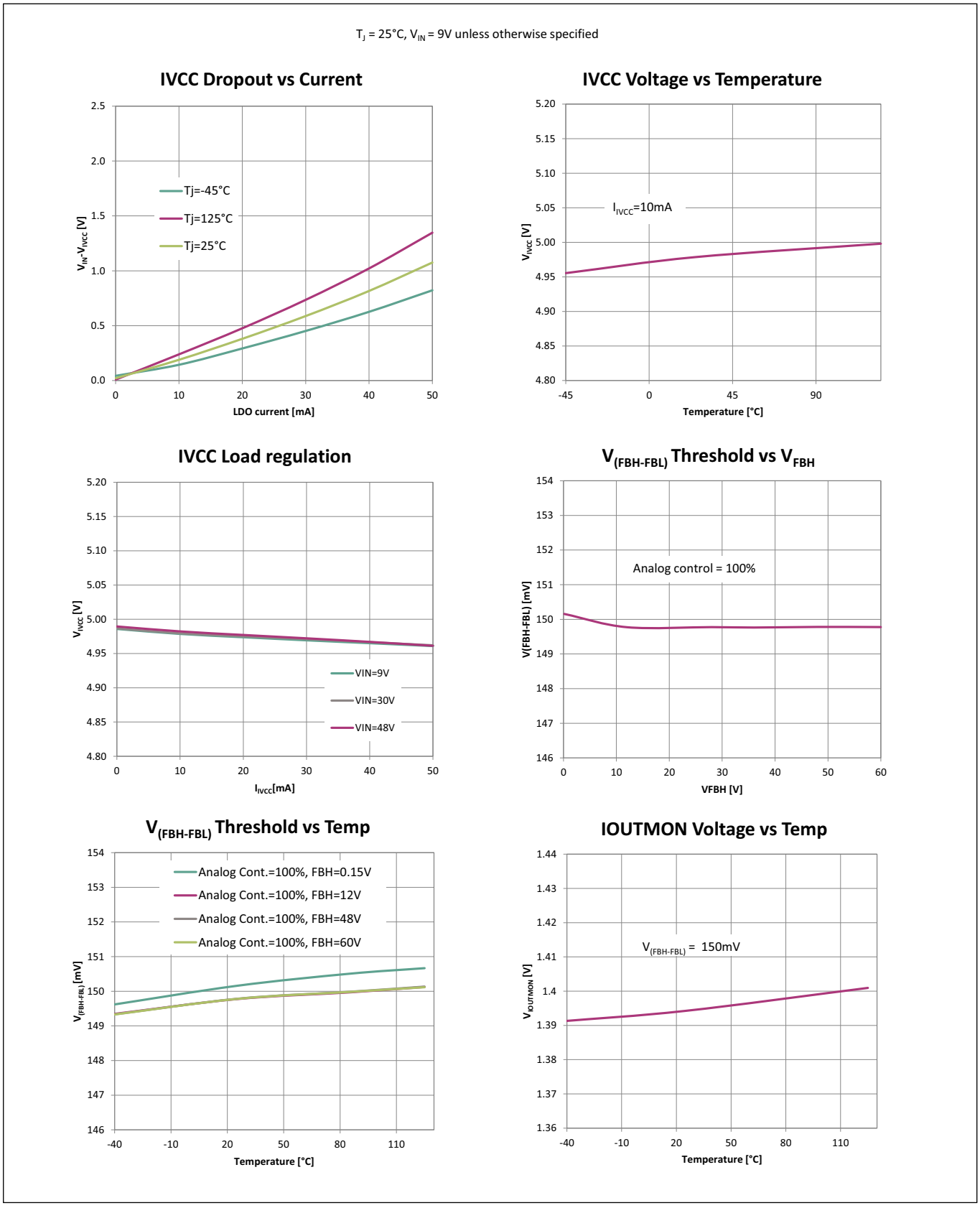


Figure 35 Characterization diagram 1

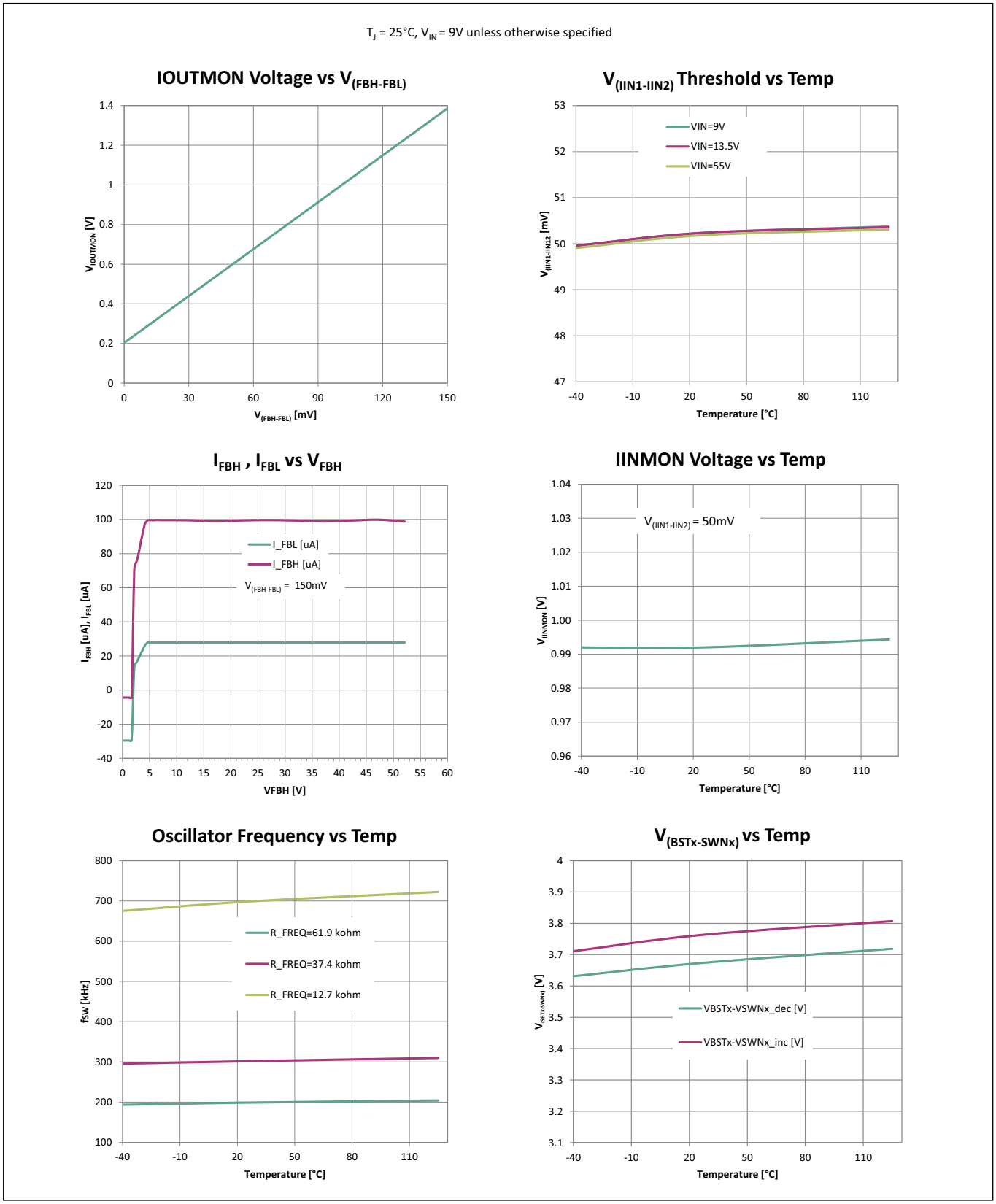


Figure 36 Characterization diagram 2

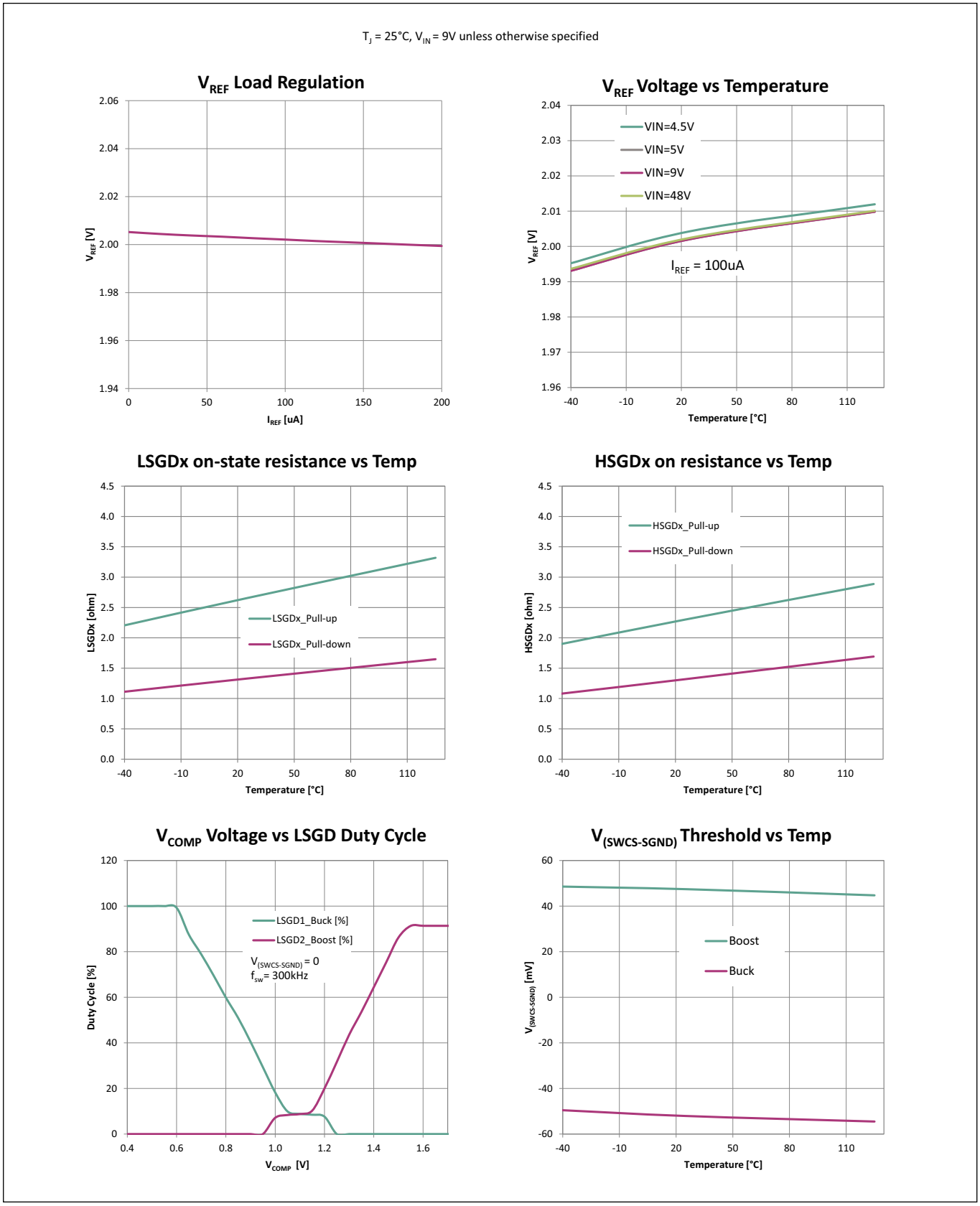


Figure 37 Characterization diagram 3

9 Ordering information

Table 54 lists the EZ-PD™ PMG1-B2 part numbers and features.

Table 54 EZ-PD™ PMG1-B2 ordering information

Product	Termination resistor	Role	Type-C ports	Switching frequency	Package type	Si ID
CYPM1216-68LQXI	R_P, R_D, R_{D-DB}	DRP	1	200 to 700 kHz	68-pin QFN	0x1FA0
CYPM1216-68LQXIT						

9.1 Ordering code definition

Table 55 defines the fields for the part numbers in the form CYPM1ABC-DEFGHIJ.

Table 55 EZ-PD™ PMG1-B2 ordering code definitions

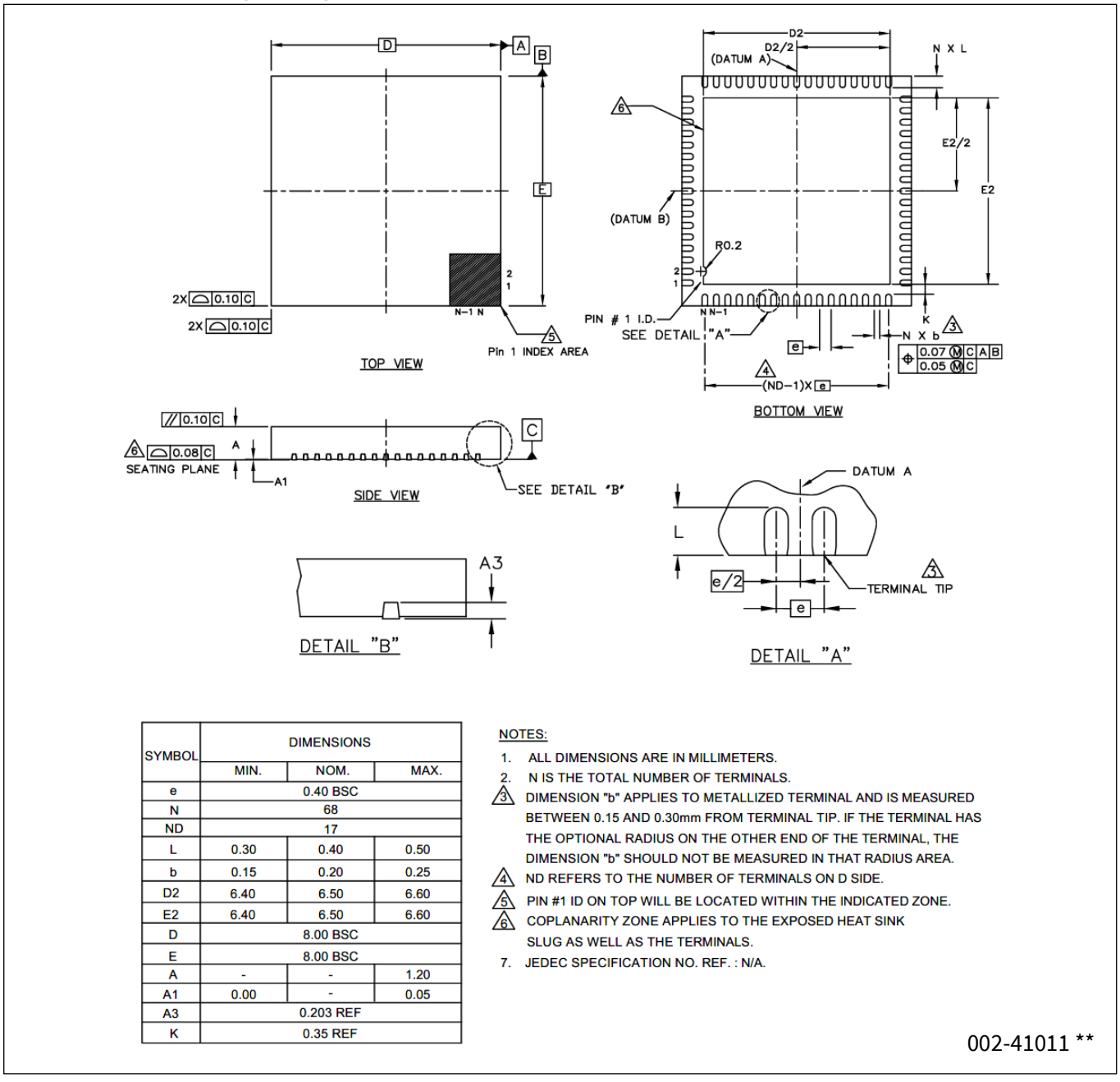
Field	Description	Values	Meaning
CY	Cypress prefix	CY	Company ID, an Infineon company
PM	Marketing code	PM	PM = Power Delivery MCU family
1	MCU family generation	1	Product family generation
A	Family	0	S0
		1	S1, B1
		2	S2, B2
		3	S3
B	PD Ports	1	1-PD port
		2	2-PD port
C	Application specific	5	R_P, R_D (no dead battery support)
		6	R_P, R_D, R_{D-DB} (dead battery support)
DE	Pin	XX	Number of pins in the package
FG	Package code	LQ	QFN
		BZ	BGA
		FN	CSP
H	Lead free	X	Lead: X = Pb-free
I	Temperature range	I	Industrial
J	Only for T&R	T	Tape and reel

10 Packaging

Table 56 Package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_J	Operating junction temperature	–	–40	–	125	°C
T_{JA}	Package θ_{JA}	Specified for JEDEC 2s2p board (JESD 51-7) + natural convection with still air; T_A = 85°C; power dissipation = 1.685 W	–	36	–	°C/W
T_{JB}	Package θ_{JB}		–	5.4	–	°C/W
$T_{JC(TOP)}$	Package θ_{JC} (top)		–	17.6	–	°C/W
$T_{JC(BOT)}$	Package θ_{JC} (bottom)		–	1.4	–	°C/W

10.1 Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.40 BSC	
N		68	
ND		17	
L	0.30	0.40	0.50
b	0.15	0.20	0.25
D2	6.40	6.50	6.60
E2	6.40	6.50	6.60
D		8.00 BSC	
E		8.00 BSC	
A	-	-	1.20
A1	0.00	-	0.05
A3		0.203 REF	
K		0.35 REF	

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-41011 **

Figure 38 68-pin QFN (8.0×8.0×1.2 mm) LT68J, (6.5×6.5 mm) EPAD (Sawn type) (PG-TQFN-68)

11 Acronyms

Table 57 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
Arm®	advanced RISC machine, a CPU architecture
BMC	bi-phase mark coding
CC	constant current
CCM	continuous conduction mode
CPU	central processing unit
CSA	current sense amplifier
DAC	digital-to-analog converter
DRP	dual role power
EMC	electromagnetic compatibility
EMCA	electronically marked cable assembly
EPR	extended power range
ESR	Equivalent series resistance
GPIO	general-purpose input/output
HSDR	high-side driver
I^2C	inter-integrated circuit, a communications protocol
I/O	input/output, see also GPIO
LDO	Low dropout regulator
LSDR	low-side driver
MCU	microcontroller unit
OCP	overcurrent protection
OTA	operational transconductance amplifier
OVLO	overvoltage lockout
OVP	overvoltage protection
PD	power delivery
POR	power-on reset
PWM	pulse-width modulator
RAM	random-access memory
ROM	read only memory
SCP	short-circuit protection
SIP	system-in-package
SPI	serial peripheral interface, a communications protocol
SRAM	static random access memory
SROM	supervisory read only memory
SWD	serial wire debug
TCPWM	timer/counter/PWM
Type-C	a new standard with a slimmer USB connector and a reversible cable
UART	universal asynchronous transmitter receiver, a communications protocol

Table 57 Acronyms used in this document *(continued)*

Acronym	Description
UFP	upstream facing port
UVP	undervoltage protection
USB	Universal Serial Bus
UVLO	undervoltage lockout

12 Document conventions

12.1 Units of measure

Table 58 Units of measure

Symbol	Unit of measure
°C	degrees celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo-ohms
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
µA	microamperes
µF	microfarads
µs	microseconds
µS	microsiemens
µV	microvolts
µW	microwatts
mA	milliamperes
mΩ	milliohms
ms	millisecond
mV	millivolts
nA	nanoamperes
ns	nanoseconds
Ω	ohm
pF	picofarads
ppm	parts per million
ps	picoseconds
s	second
S	siemens
sps	samples per second

Revision history

Document revision	Date	Description of changes
*F	2026-08-07	Public release.

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