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General Description

EZ-PD™ CCG5C is a one-port USB Type-C controller that complies with the latest USB Type-C and Power Delivery (PD) specifications. CCG5C provides a complete USB Type-C and USB PD port control solution for PCs and notebooks. CCG5C includes a 32-bit, 48-MHz Arm® Cortex®-M0 processor with 128-KB flash and integrates a complete Type-C Transceiver including the Type-C termination resistors R_p , R_d , and dead battery R_d termination. CCG5C is available in a 40-pin QFN package.

Applications

- PCs and notebooks
- Thunderbolt, Non-Thunderbolt hosts and devices/docks

Features

USB-PD

- Supports latest USB PD 3.0 Specification
- Fast Role Swap (FRS)
- Extended data messaging

Type-C

- Integrated current sources for DFP^[1] role (R_p)
 - Default current at 500 mA/900 mA
 - 1.5 A
 - 3 A
- Integrated R_d resistor for UFP^[2] role
- Integrated VCONN FETs to power EMCA cables
- Integrated dead battery termination
- Integrated high-voltage protection on CC and SBU pins to protect against accidental shorts to the VBUS pin on the Type-C connector

Legacy Charging

- BCv1.2 (source and sink)
- Apple charging (source only)

Protection

- Configurable hardware controlled VBUS
 - Overvoltage protection (OVP)
 - Undervoltage protection (UVP)
 - Overcurrent protection (OCP)
- Overcurrent protection (OCP) for VCONN
- High-voltage VBUS short protection for SBU & CC pins

Mux

- Integrated USB2.0 analog mux for USB 2.0 HS data and UART data
- Integrated SBU analog mux for alternate modes (Displayport and Thunderbolt)

LDO

- Integrated high-voltage LDO operational up to 21.5 V for dead battery mode operation

CSA

- VBUS high-side Current Sense Amplifier capable of measuring current across 10-mΩ resistance

PFET Gate Drivers

- Gate Drivers tolerant to 24 V to drive external VBUS PFET on the consumer and provider path
- Slew Rate Control

32-bit MCU Subsystem

- 48-MHz Arm Cortex-M0 CPU
- 128-KB Flash
- 12-KB SRAM

Integrated Digital Blocks

- Two integrated timers and counters to meet response times required by the USB-PD protocol
- Four runtime serial communication blocks (SCBs) with reconfigurable I²C, SPI, or UART functionality

Clocks and Oscillators

- Integrated oscillator eliminating the need for an external clock

Operating Range

- V_{SYN} (2.75 V–5.5 V)
- VBUS (4.0 V–21.5 V)

Hot-Swappable I/Os

- I²C pins from SCB1 and CC1, CC2 pins are hot-swappable

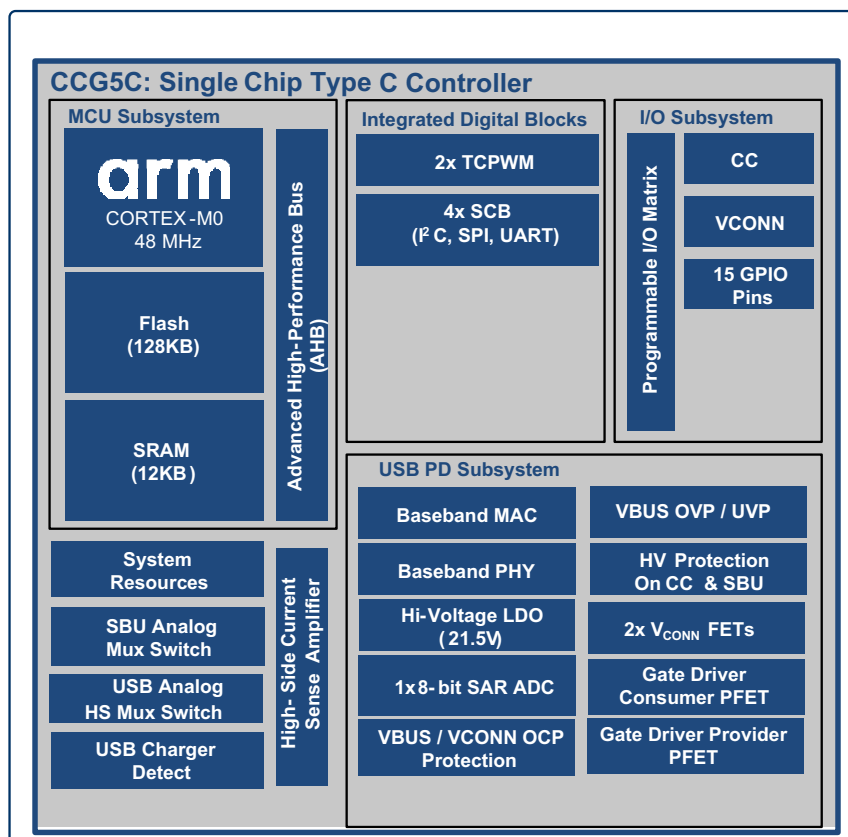
Packages

- 6.0 mm × 6.0 mm, 0.5 mm, 40-pin QFN
- Supports industrial temperature range (–40 °C to +85 °C)

Notes

1. DFP refers to Power Source.
2. UFP refers to Power Sink.

Logic Block Diagram



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Functional Overview

USB-PD Subsystem (SS)

USB-PD Physical Layer

The CCG5C USB-PD subsystem shown in Figure 1 consists of the USB-PD physical layer (PHY) block and supporting circuits. The PHY block consists of a transmitter and receiver that communicates using BMC and 4b/5b encoded/decoded data over the CC channel based on the PD 3.0 specification. All communication is half-duplex. The PHY block practices collision avoidance to minimize communication errors on the channel.

Additionally, the CCG5C USB-PD block includes all termination resistors (R_p and R_d) and their switches as required by the USB Type-C specification. R_p and R_d resistors are required for connection detection, plug orientation detection, and for establishing the USB source/sink roles.

The integrated R_p resistor enables CCG5C to be configured as a downstream facing port (DFP). The R_p resistor is implemented as a current source and can be programmed to support the complete range of current capacity on VBUS defined in the USB Type-C specification.

The R_d resistor is used to identify CCG5C as an upstream facing port (UFP) in a dual-role power (DRP) application. When the device is not powered, the Dead Battery R_d resistor on CC pins is required for dead battery termination detection and charging.

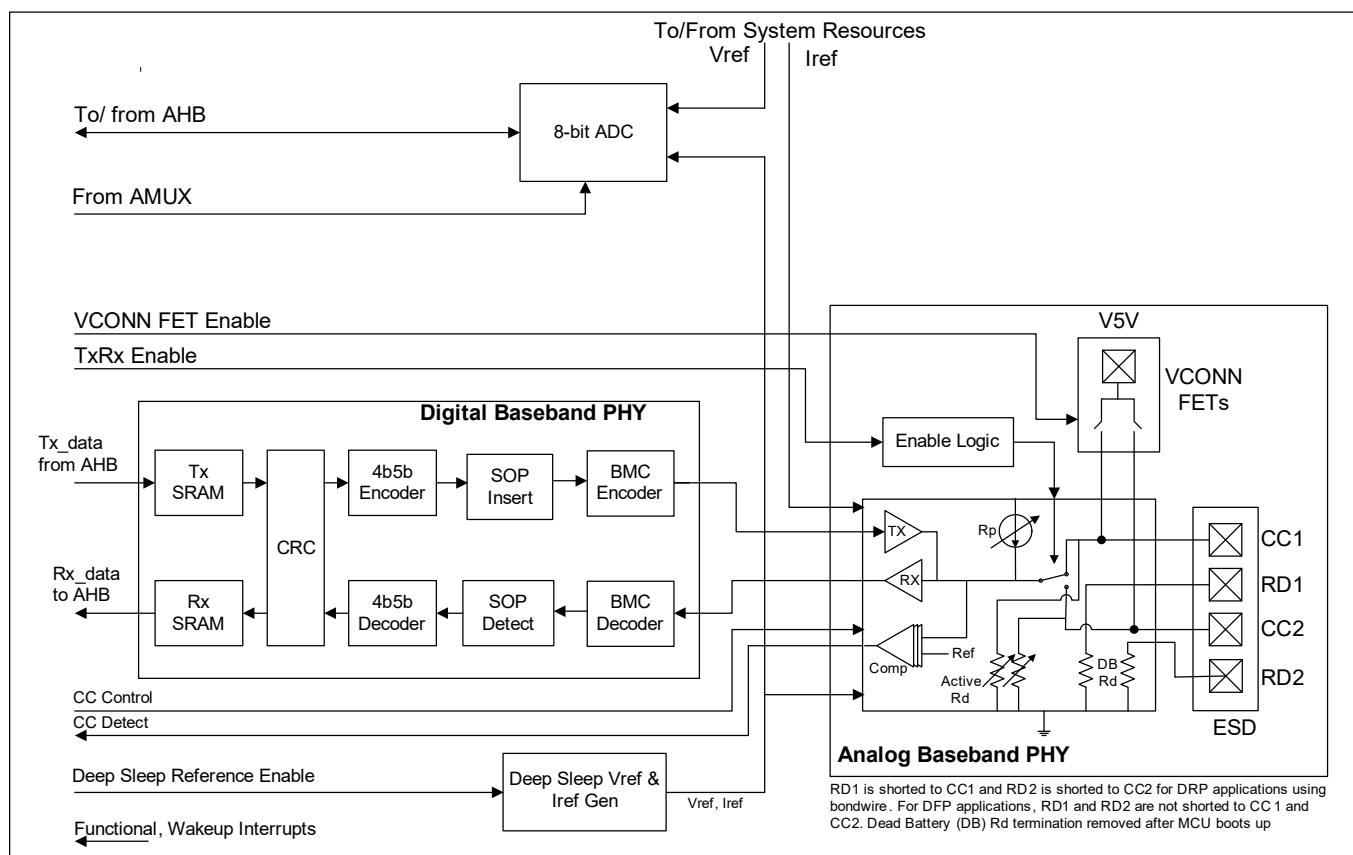
To support the latest USB-PD 3.0 specification, CCG5C includes Fast Role Swap (FRS). The FRS feature enables externally powered docks and hubs to rapidly switch to bus power when their external power supply is removed. CCG5C also supports FRS detection in Deep Sleep mode.

For more details about FRS, refer to Section 6.3.17 in the [USB-PD 3.0 specification](#).

CCG5C is designed to be fully interoperable with revision 3.0 and 2.0 of the USB Power Delivery specification.

CCG5C supports Extended Messages containing data of up to 260 bytes. The Extended Messages will be larger than expected by the USB-PD 2.0 hardware. To accommodate systems based on Revision 2.0, a Chunking mechanism is implemented such that messages are limited to Revision 2.0 sizes unless it is discovered that both systems support longer message lengths.

Figure 1. USB-PD Subsystem



VCONN FET

CCG5C has a power supply input, V5V, for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs to power either CC1 or CC2 pins. These FETs can provide 1.5-W power over VCONN on CC1 and CC2 pins for active EMCA cables. CCG5C also includes overcurrent protection (OCP) on VCONN.

ADC

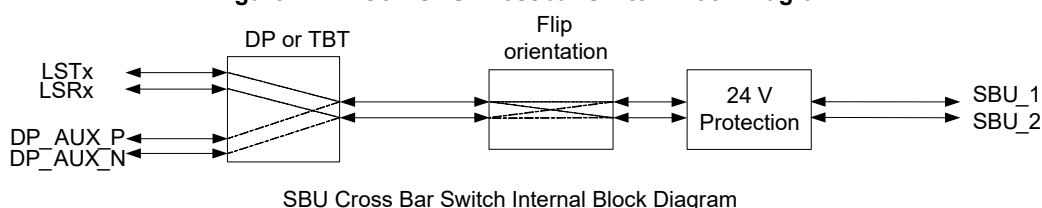
The USB-PD subsystem contains one 8-bit successive approximation register analog-to-digital converter (SAR ADC). The ADC includes an 8-bit digital-to-analog converter (DAC) and a comparator. The DAC output forms the positive input of the

comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses, an internal bandgap voltage, and an internal voltage proportional to the absolute temperature. All GPIOs on the chip have access to the ADC through the chip-wide analog mux bus. CC1 and CC2 pins are not available to connect to the mux bus.

SBU Mux

CCG5C integrates a SBU 4x2 mux that enables selection between the DisplayPort or Thunderbolt alternate mode and Type-C orientation as shown in Figure 2. Type-C facing SBU pins are protected from accidental short to high-voltage VBUS.

Figure 2. CCG5C SBU Crossbar Switch Block Diagram



USB 2.0 Mux

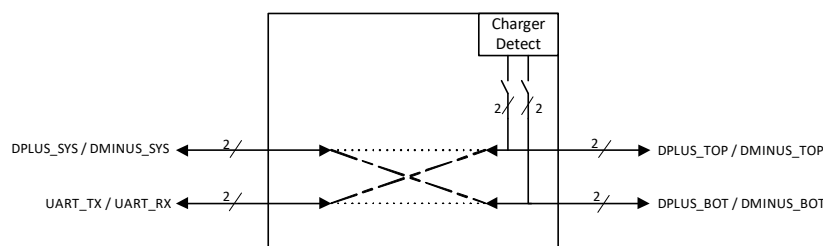
The HS mux contains a 2 × 2 cross bar switch to route the system DPLUS and DMINUS lines to the Type-C top or bottom port based on the CC (Type-C plug) orientation. Unused DPLUS and DMINUS top or bottom lines can be connected to a UART (Debug) port. The maximum operating frequency of UART must be 1 Mbps.

The USB 2.0 mux also contains charger detection/emulation for detecting USB BC 1.2 and Apple terminations. The charger detection block is connected to DPLUS and DMINUS from the system as shown in Figure 3.

To meet the HS eye diagram requirements with sufficient margin, follow these guidelines:

- It is recommended to keep the total USB HS signal trace lengths (USB 2.0 host to CCG5C + CCG5C to Type-C connector pins) to 4 inches.
- Total USB HS signal trace lengths can be increased up to 8 inches by adjusting the drive strength on the USB 2.0 host.
- The differential impedance across the DPLUS/DMINUS signal traces shall be 90 Ω.
- Trace width shall be 6 mils.
- Air Gap (distance between lines) shall be 8 mils.

Figure 3. CCG5C DPLUS/DMINUS Switch Block Diagram



Overvoltage and Undervoltage Protection on VBUS

CCG5C implements an undervoltage/overvoltage (UVOV) detection circuit for the VBUS supply. The threshold for OV and UV detection can be set independently. Both UV and OV detector have programmable thresholds and is controlled by the firmware.

Overcurrent Protection on VBUS

CCG5C integrates a high-side current sense amplifier to detect overcurrent on the VBUS. Overcurrent is detected using an external 10-mΩ sense resistor connected between the CSP and CSN pins. The OCP detector threshold is programmable and controlled by the firmware.

VBUS Discharge

CCG5C also has integrated VBUS discharge circuit. It is used to discharge VBUS to meet the USB-PD specification timing on a detach condition and negative voltage transition.

VBUS Regulator

CCG5C can operate from two power supplies – VSYS and VBUS. CCG5C integrates the regulator (that supports up to 21.5 V) to derive operating supply voltage. The VSYS always takes priority over VBUS. In the absence of VSYS, the regulator powers CCG5C from VBUS.

Gate Driver for VBUS PFET on Consumer and Provider Path

CCG5C has an integrated PFET gate driver to drive external PFETs on the VBUS consumer and provider path. The gate driver can drive only low or high-Z, thus requiring an external pull-up. This pin is VBUS voltage-tolerant.

Charger Detect

CCG5C integrates battery charger emulation and detection for USB BC 1.2 and Apple Charging.

High-Voltage-Tolerant SBU and CC Lines

The chip has high-voltage-tolerant SBU and CC lines. In the case of SBU/CC short to VBUS through connectors, these lines will be protected internally.

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG5C is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG5C has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG5C device has a 128-KB flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver two wait-states (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. A part of the flash module can be used to emulate EEPROM operation if required.

SRAM

A supervisory ROM that contains boot and configuration routines is provided.

SRAM

CCG5C has 12 KB SRAM.

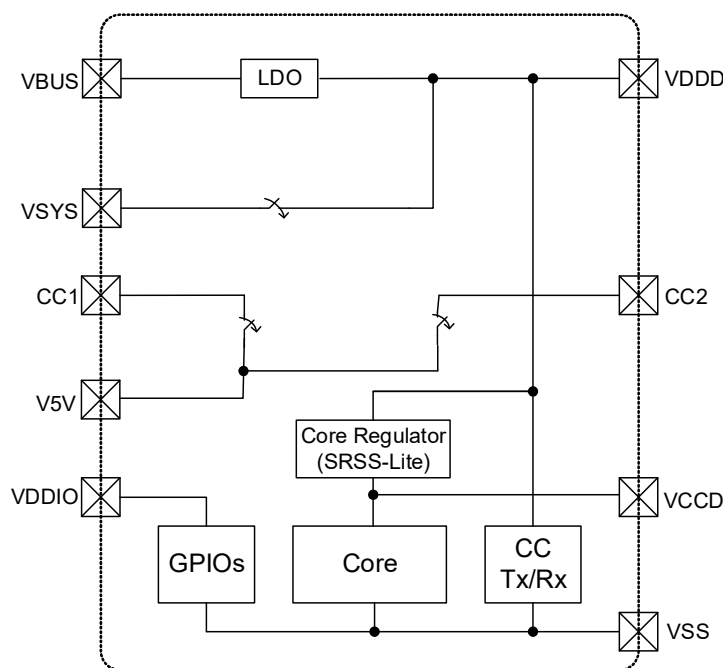
Power System Overview

Figure 4 provides an overview of the EZ-PD CCG5C power system. CCG5C can operate from two possible external supply sources: VBUS (4 to 21.5 V) or VSYS (2.75 to 5.5 V). The VBUS supply is regulated inside the chip with a LDO. The switched supply, V_{DD}, is used directly inside some analog blocks and further regulated down to V_{CCD}, which powers majority of the core. CCG5C has two different power modes: Active and Deep Sleep. Transitions between these power modes are managed by the power system. A separate power domain, VDDIO, is provided for the GPIOs. The VDDD and VCCD pins, both outputs of regulators, are brought out for connecting a 1-μF and 0.1-μF capacitor respectively for the regulator stability only. The VCCD pin is not supported as a power supply. VDDD can source 2 mA (max) for external load. In CCG5C, VDDD shall be shorted to VDDIO on PCB.

Table 1. CCG5C Power Modes

| Mode | Description |
|------------|--|
| RESET | Power is valid and XRES is not asserted. An internal reset source is asserted or Sleep Controller is sequencing the system out of reset. |
| ACTIVE | Power is valid and CPU is executing instructions. |
| DEEP SLEEP | Main regulator and most blocks are shut off. Deep Sleep regulator powers logic, but only low-frequency clock is available. |

Figure 4. EZ-PD CCG5C Power System



Peripherals

CCG5C has four SCBs, which can each implement an I²C, UART, or SPI interface. Among four SCBs SCB4 is configurable in I²C mode only.

I²C Mode: The hardware I²C block implements a full multimaster and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I²C peripheral is compatible with the I²C Standard mode, Fast mode, and Fast Mode Plus devices as defined in the NXP I²C bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes. The I²C bus uses open-drain drivers for clock and data with pull-up resistors on the bus for clock and data connected to all nodes. The required Rise and Fall times for different I²C speeds are guaranteed by using appropriate pull-up resistor values depending on V_{DD}, bus capacitance, and resistor tolerance.

For detailed information on how to calculate the optimum pull-up resistor value for your design, refer to the UM10204 I²C bus specification and user manual (the latest revision is available at www.nxp.com).

CCG5C is not completely compliant with the I²C spec for the following:

- Only SCB1 is overvoltage-tolerant. SCB2, SCB3, and SCB4 GPIO cells are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.
- Fast Mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast mode and Fast Mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

One of the SCB (typically SCB1) blocks is used to implement the Host Processor Interface (HPI) slave which allows an external MCU to control the firmware operation.

The HPI I²C Slave address is configurable using the I2C_CFG_EC pin as shown in below table.

Table 2. I²C Slave Address Configuration

| I2C_CFG_EC configuration | Slave Address |
|--------------------------|---------------|
| Floating | 0x08 |
| Pulled up with 1 kΩ | 0x42 |
| Pulled down with 1 kΩ | 0x40 |

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity error, break

detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

Timer/Counter/PWM Block (TCPWM)

CCG5C has two TCPWM blocks. Each TCPWM block consists of four 16-bit counters with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

GPIO

CCG5C has 15 GPIOs that includes the SCB and SWD pins, which can also be used as GPIOs. The I²C pins from only SCB 1 are overvoltage-tolerant. The GPIO block implements the following:

- Seven drive strength modes:
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL)
- Individual control of input and output buffers enabling/disabling in addition to the drive strength modes
- Hold mode for latching the previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for CCG5C since it has five ports).

Pinouts

Table 3. Pinout for CYPD5126-40LQXIT and CYPD5137-40LQXI

| Group Name | Pin Name | Port | Pin | Description |
|-----------------------------|--------------------------|--------|-----|--|
| USB Type-C | CC1 | Analog | 9 | Connect to Type-C CC1 pin. Filter noise with 390-pF cap to GND. |
| | CC2 | Analog | 7 | Connect to Type-C CC2 pin. Filter noise with 390-pF cap to GND. |
| Mux | DPLUS_SYS | Analog | 23 | Connect to USB 2.0 DP from Host side. |
| | DMINUS_SYS | Analog | 24 | Connect to USB 2.0 DM from Host side. |
| | UART_TX/GPIO | P4.0 | 29 | Connect to Debug port UART_TX (optional) from host side or can be used as GPIO. If unused, leave floating. |
| | UART_RX/GPIO | P4.1 | 30 | Connect to Debug port UART_RX (optional) from host side or can be used as GPIO. If unused, leave floating. |
| | DPLUS_BOT | Analog | 26 | Connect to Type-C DP1 pin. Keep trace length less than 2 inches. |
| | DMINUS_BOT | Analog | 25 | Connect to Type-C DM1 pin. Keep trace length less than 2 inches. |
| | DMINUS_TOP | Analog | 27 | Connect to Type-C DM2 pin. Keep trace length less than 2 inches. |
| | DPLUS_TOP | Analog | 28 | Connect to Type-C DP2 pin. Keep trace length less than 2 inches. |
| | SBU2 | Analog | 34 | Connect to Type-C SBU2 pin. |
| | SBU1 | Analog | 35 | Connect to Type-C SBU1 pin. |
| | AUX_P | Analog | 36 | Connect to Auxiliary Signal P from DisplayPort Controller. If not used, leave floating. |
| | AUX_N | Analog | 37 | Connect to Auxiliary Signal N from DisplayPort Controller. If not used, leave floating. |
| | LSTX | Analog | 38 | Thunderbolt Link Management UART Rx. If not used, leave floating. |
| | LSRX | Analog | 39 | Thunderbolt Link Management UART Tx. If not used, leave floating. |
| VBUS Control | VBUS_P_CTRL | Analog | 11 | Pin for enabling/disabling Provider Side PFET 0: Path ON High-Z: Path OFF |
| | VBUS_C_CTRL | Analog | 12 | Pin for enabling/disabling Consumer Side PFET 0: Path ON High-Z: Path OFF |
| VBUS OCP | CSP | Analog | 1 | Current Sense Positive Input |
| | CSN | Analog | 40 | Current Sense Negative Input |
| GPIOs and Serial Interfaces | SWD_IO/TBT_RST/GPIO | P1.4 | 6 | SWD I/O/GPIO |
| | SWD_CLK/I2C_CFG_EC/ GPIO | P1.0 | 2 | SWD Clock/ I ² C config line. I ² C config line is used to select the I ² C address of HPI interface. The state of line decides the 7 bit I ² C address for HPI. I ² C Config Line Floating: 0x08 Pulled up with 1 k Ω : 0x42 Pulled down with 1 k Ω : 0x40 |
| | I2C_SDA_SCB2_TBT/GPIO | P1.1 | 3 | SCB2 I ² C Data/GPIO |
| | I2C_SCL_SCB2_TBT/GPIO | P1.2 | 4 | SCB2 I ² C Clock/GPIO |
| | I2C_INT_TBT/GPIO | P1.3 | 5 | TBT interrupt/GPIO |

Table 3. Pinout for CYPD5126-40LQXIT and CYPD5137-40LQXI (continued)

| Group Name | Pin Name | Port | Pin | Description |
|-----------------------------|-------------------------------|--------|------|--|
| GPIOs and Serial Interfaces | OVP_TRIP/I2C_SDA_SCB4/GPIO | P2.1 | 14 | VBUS overvoltage output indicator/SCB4 I ² C Data |
| | UV_OCP_TRIP/I2C_SCL_SCB4/GPIO | P2.0 | 13 | VBUS undervoltage or OCP Output Indicator/SCB4 I ² C Clock/GPIO |
| | I2C_SDA_SCB1_EC/GPIO | P5.0 | 16 | SCB1 I ² C Data/GPIO |
| | I2C_SCL_SCB1_EC/GPIO | P5.1 | 17 | SCB1 I ² C Clock/GPIO |
| | I2C_INT_EC/GPIO | P2.2 | 15 | Embedded Controller interrupt/GPIO |
| | HPD/GPIO | P3.0 | 18 | Hot Plug Detect I/O/GPIO |
| | I2C_SDA_SCB3/GPIO/VSEL_2 | P3.1 | 20 | SCB3 I ² C Data or GPIO or voltage selection control for VBUS |
| | I2C_SCL_SCB3/GPIO/VSEL_1 | P3.2 | 21 | SCB3 I ² C Clock or GPIO or voltage selection control for VBUS |
| Reset | XRES | Analog | 10 | Reset input (Active LOW) |
| Power | VBUS | Power | 22 | Supply input (4 V–21.5 V) for VBUS to 3.3-V Regulator. This pin also discharges VBUS using internal pull-down and also has monitors for overvoltage and undervoltage conditions. |
| | VSYS | Power | 19 | Supply input (2.75 V–5.5 V) for PD subsystem and system resources. |
| | VDDD | Power | 31 | Output of VBUS to 3.3-V regulator or connected to VSYS using switch. Bypass with cap to GND. This pin can drive 2-mA external load. |
| | VDDIO | Power | 32 | This pin can be shorted to VDDD or an independent supply can be given. |
| | VCCD | Power | 33 | 1.8-V regulator output for filter capacitor. This pin cannot drive external load. |
| | V5V | Power | 8 | 4.85-V to 5.5-V supply input to power EMCA cables. Connected to CC1 or CC2 using low-impedance switches. |
| Ground | VSS | Ground | EPAD | Ground |

Figure 5. 40-Pin QFN Pin Map (Top View) for CYPD5126-40LQXIT and CYPD5137-40LQXI

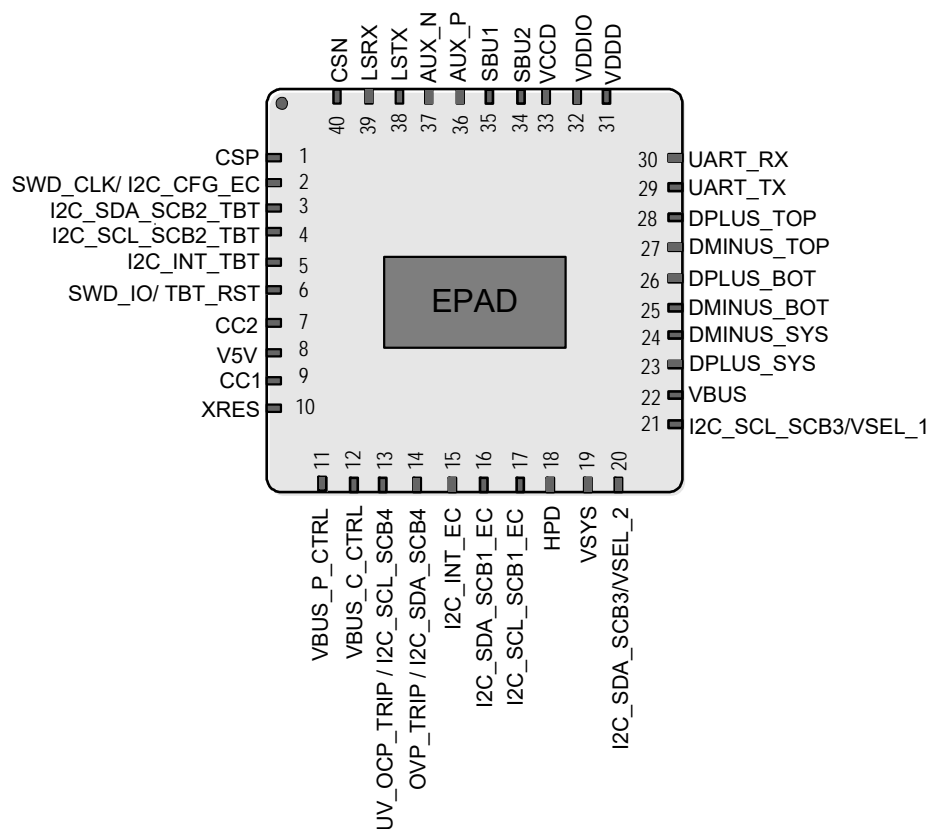


Table 4 through Table 7 provide the various configuration options for the serial interfaces.

Table 4. Serial Communication Block (SCB1) Configuration

| QFN Pin | UART | SPI | I ² C | GPIO Functionality |
|---------|---------------|---------------|------------------|--------------------|
| 16 | UART_RTS_SCB1 | SPI_MOSI_SCB1 | I2C_SDA_SCB1 | GPIO |
| 17 | UART_TX_SCB1 | SPI_MISO_SCB1 | I2C_SCL_SCB1 | GPIO |
| 18 | UART_RX_SCB1 | SPI_CLK_SCB1 | – | HPD/GPIO |
| 15 | UART_CTS_SCB1 | SPI_SEL_SCB1 | – | I2C_INT_EC/GPIO |

Table 5. Serial Communication Block (SCB2) Configuration

| QFN Pin | UART | SPI Master | I ² C Slave | GPIO Functionality |
|---------|---------------|---------------|------------------------|-------------------------|
| 2 | UART_RX_SCB2 | SPI_SEL_SCB2 | – | SWD_CLK/I2C_CFG_EC/GPIO |
| 3 | UART_TX_SCB2 | SPI_MOSI_SCB2 | I2C_SDA_SCB2 | I2C_SDA_SCB2_TBT/GPIO |
| 4 | UART_CTS_SCB2 | SPI_MISO_SCB2 | I2C_SCL_SCB2 | I2C_SCL_SCB2_TBT/GPIO |
| 5 | UART_RTS_SCB2 | SPI_CLK_SCB2 | – | I2C_INT_TBT/GPIO |

Table 6. Serial Communication Block (SCB3) Configuration

| QFN Pin | UART | SPI Master | I ² C Slave | GPIO Functionality |
|---------|---------------|---------------|------------------------|--------------------|
| 20 | UART_CTS_SCB3 | SPI_SEL_SCB3 | I2C_SDA_SCB3 | VSEL_2/GPIO |
| 21 | UART_RTS_SCB3 | SPI_MOSI_SCB3 | I2C_SCL_SCB3 | VSEL_1/GPIO |
| 29 | UART_TX_SCB3 | SPI_MISO_SCB3 | – | UART_TX / GPIO |
| 30 | UART_RX_SCB3 | SPI_CLK_SCB3 | – | UART_RX / GPIO |

Table 7. Serial Communication Block (SCB4) Configuration

| QFN Pin | UART | SPI Master | I ² C Slave | GPIO Functionality |
|---------|------|------------|------------------------|--------------------|
| 13 | – | – | I2C_SCL_SCB4 | GPIO |
| 14 | – | – | I2C_SDA_SCB4 | GPIO |

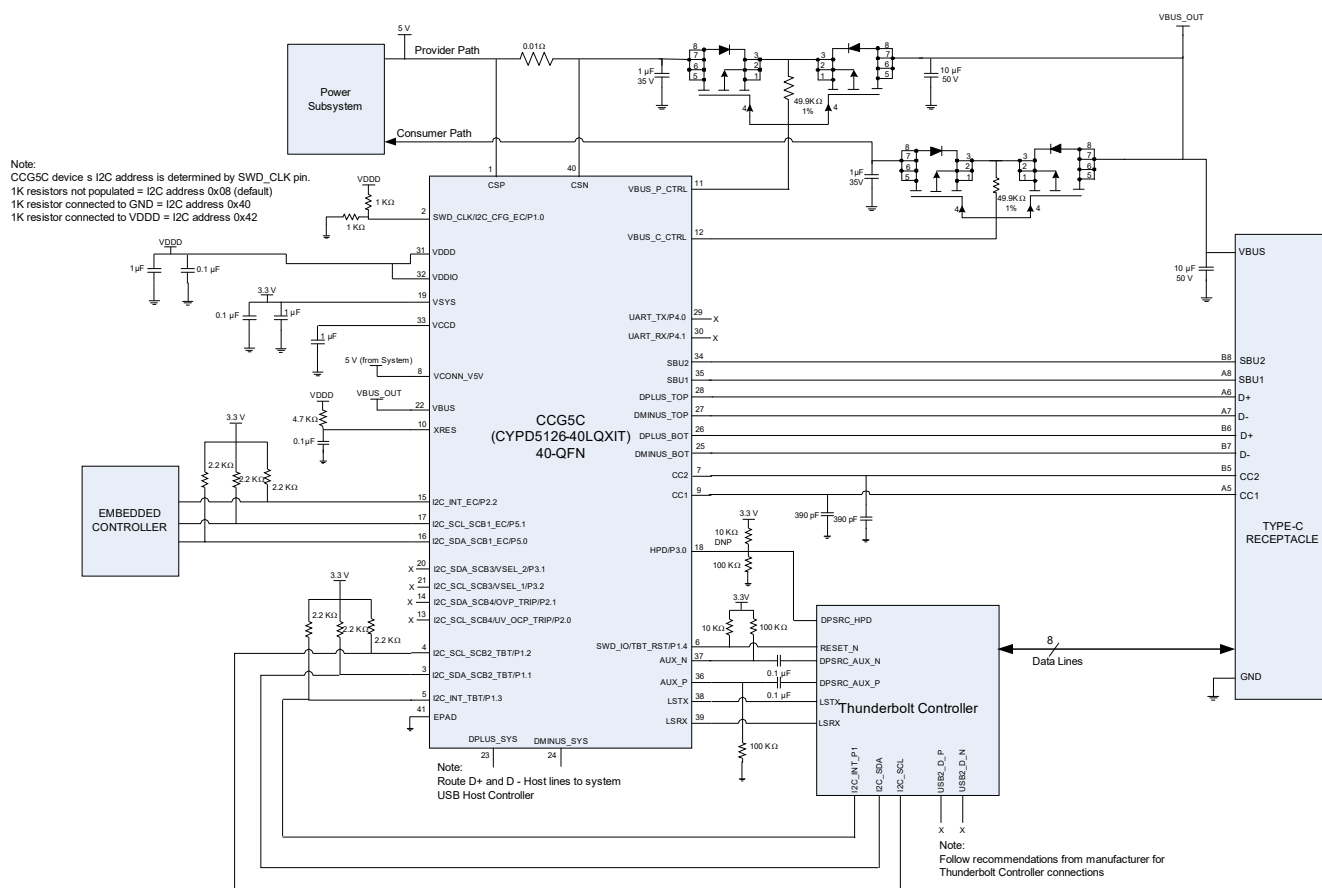
Figure 6 illustrates a Type-C port Thunderbolt notebook DRP application diagram using CCG5C. The Type-C port can be used as a power provider or a power consumer.

The CCG5C device controls the transfer of USB 2.0 DPLUS and DMINUS lines from the top and bottom of the Type-C receptacle to the DPLUS and DMINUS lines of the USB Host controller. CCG5C also handles the routing of SBU1 and SBU2 lines from the Type-C receptacle to the Thunderbolt controller for link management. CCG5C offers VBUS short protection on SBU and CC lines.

The CCG5C device has a integrated VCONN FETs for applications that need to provide power for accessories and cables using the VCONN pin of the Type-C receptacle. VBUS FETs are also used for providing power over VBUS and for consuming power over VBUS. The 10-m Ω resistor between the 5-V supply and provider FETs is used for overcurrent detection on the VBUS. The VBUS_P_CTRL pin of CCG5C has an in-built VBUS monitoring circuit that can detect OV and UV on VBUS.

Figure 6 illustrates a single-port Thunderbolt notebook DRP application diagram using CYPD5126-40LQXIT.

Figure 6. CCG5C in a Single Port Notebook Application using CYPD5126-40LQXIT



Electrical Specifications

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings^[3]

| Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------------------------|--|------|-----|-------------------------|------|--|
| V _{SYS_MAX} | Supply relative to V _{SS} | – | – | 6 | V | – |
| V _{5V_MAX} | Max supply voltage relative to V _{SS} | – | – | 6 | | |
| V _{BUS_MAX} | Max VBUS voltage relative to V _{SS} | – | – | 24 | | |
| V _{DDIO_MAX} | Max supply voltage relative to V _{SS} | – | – | V _{DDD} | | |
| V _{GPIO_ABS} | Inputs to GPIO, DP/DM mux (UART, SYS, DP/DM_top/bot pins), SBU mux (SBU1/2 pins) | –0.5 | – | V _{DDIO} + 0.5 | | |
| I _{GPIO_ABS} | Maximum current per GPIO | –25 | – | 25 | mA | – |
| I _{GPIO_INJECTION} | GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS} | –0.5 | – | 0.5 | | Absolute max, current injected per pin |
| ESD_HBM | Electrostatic discharge human body model | 2200 | – | – | V | – |
| ESD_CDM | Electrostatic discharge charged device model | 500 | – | – | | – |
| LU | Pin current for latch-up | –200 | – | 200 | mA | – |
| VCC_PIN_ABS | Max voltage on CC1 and CC2 pins | – | – | 24 | V | – |
| VSBU_PIN_ABS | Max voltage on SBU1 and SBU2 pins | – | – | 24 | | – |
| VGPI_OVT_ABS | OVT pins (16, 17) voltage | –0.5 | – | 6 | | – |
| ESD_HBM_SBU | Electrostatic discharge human body model for SBU1, SBU2 pins | 1100 | – | – | | Only applicable to SBU1 and SBU2 pins |

Note

3. Usage above the absolute maximum conditions listed in Table 8 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Device-Level Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 120\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 3.0 V to 5.5 V except where noted.

Table 9. DC Specifications (Operating Conditions)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|--|---------------------|--|-------------------------|-----|------------------|------|--|
| SID.PWR#23 | V _{SYS} | – | 2.75 | – | 5.5 | V | UFP applications |
| SID.PWR#23_A | V _{SYS} | – | 3 | – | 5.5 | | DFF/DRP applications |
| SID.PWR#22 | V _{BUS} | – | 4 | – | 21.5 | | – |
| SID.PWR#1 | V _{DDD} | Regulated output voltage when V _{SYS} powered | V _{SYS} – 0.05 | – | V _{SYS} | | – |
| SID.PWR#1_A | V _{DDD} | Regulated output voltage when V _{BUS} powered | 3 | – | 3.65 | | – |
| SID.PWR#26 | V _{5V} | – | 4.85 | – | 5.5 | | – |
| SID.PWR#13 | V _{DDIO} | – | V _{DDD} | – | V _{DDD} | | At system-level, short V _{DDIO} to V _{DDD} |
| SID.PWR#24 | V _{CCD} | Regulated output voltage (for core logic) | – | 1.8 | – | | – |
| SID.PWR#15 | C _{EFC} | Regulator bypass capacitor for V _{CCD} | – | 100 | – | nF | X5R ceramic |
| SID.PWR#16 | C _{EXC} | Regulator bypass capacitor for V _{DDD} | – | 1 | – | μF | |
| Active Mode, V _{SYS} = 2.75 to 5.5 V. Typical values measured at V _{SYS} = 3.3 V | | | | | | | |
| SID.PWR#4 | I _{DD12} | Supply current | – | 10 | – | mA | T _A = 25 °C, CC I/O IN Transmit or Receive, no I/O sourcing current, CPU at 24 MHz, PD port active |
| Deep Sleep Mode, V _{SYS} = 2.75 to 3.6 V | | | | | | | |
| SID34 | I _{DD29} | V _{SYS} = 2.75 to 3.6 V, I ² C, wakeup and WDT on. | – | 150 | – | μA | V _{SYS} = 3.3 V, T _A = 25 °C, |
| SID_DS1 | I _{DD_DS1} | V _{SYS} = 3.3 V, CC wakeup on, Type-C not connected | – | 100 | – | | Power source = V _{SYS} , Type-C not attached, CC enabled for wakeup, Rp and Rd connected at 70-ms intervals by CPU. |
| SID_DS3 | I _{DD_DS2} | V _{SYS} = 3.3 V, CC wakeup on, DP/DM, SBU ON with ADC/CSA/UVOV On | – | 500 | – | | IDD_DS1 + DP/DM, SBU, CC ON, ADC/CSA/UVOV ON |
| XRES Current | | | | | | | |
| SID307 | I _{DD_XR} | Supply current while XRES asserted | – | 130 | – | μA | Power Source = V _{SYS} = 3.3 V, Type-C Not Attached, T _A = 25 °C |

CPU

Table 10. CPU Specifications (Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|------------|------------------------|---|-----|-----|-----|------|--------------------------------|
| SID.CLK#4 | F _{CPU} | CPU input frequency | – | – | 48 | MHz | All V _{DDD} |
| SID.PWR#21 | T _{DEEPSLEEP} | Wakeup from Deep Sleep mode | – | 35 | – | μs | Guaranteed by characterization |
| SYS.XRES#5 | T _{XRES} | External reset pulse width | 5 | – | – | | |
| SYS.FES#1 | T _{PWR_RDY} | Power-up to “Ready to accept I ² C/CC command” | – | 5 | 25 | ms | |

GPIO
Table 11. GPIO DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-------------|---------------------|--|------------------------|-----|-----------------------|------------|---|
| SID.GIO#37 | V_{IH_CMOS} | Input voltage HIGH threshold | $0.7 \times V_{DDIO}$ | — | — | V | CMOS input |
| SID.GIO#38 | V_{IL_CMOS} | Input voltage LOW threshold | — | — | $0.3 \times V_{DDIO}$ | | |
| SID.GIO#39 | $V_{IH_VDDIO2.7-}$ | LVTTL input, $V_{DDIO} < 2.7$ V | $0.7 \times V_{DDIO}$ | — | — | | |
| SID.GIO#40 | $V_{IL_VDDIO2.7-}$ | LVTTL input, $V_{DDIO} < 2.7$ V | — | — | $0.3 \times V_{DDIO}$ | | |
| SID.GIO#41 | $V_{IH_VDDIO2.7+}$ | LVTTL input, $V_{DDIO} \geq 2.7$ V | 2.0 | — | — | | |
| SID.GIO#42 | $V_{IL_VDDIO2.7+}$ | LVTTL input, $V_{DDIO} \geq 2.7$ V | — | — | 0.8 | | |
| SID.GIO#33 | V_{OH} | Output voltage HIGH level | $V_{DDIO} - 0.6$ | — | — | | $I_{OH} = -4$ mA at 3-V V_{DDIO} |
| SID.GIO#34 | V_{OH} | Output voltage HIGH level | $V_{DDIO} - 0.5$ | — | — | | $I_{OH} = -1$ mA at 1.8-V V_{DDIO} |
| SID.GIO#35 | V_{OL} | Output voltage LOW level | — | — | 0.6 | | $I_{OL} = 4$ mA at 1.8-V V_{DDIO} |
| SID.GIO#35A | $V_{OL_I2C_2}$ | Output low voltage | — | — | 0.4 | | $I_{OL} = 3$ mA, $V_{DDIO} > 2$ V |
| SID.GIO#35B | $V_{OL_I2C_3}$ | Output low voltage | — | — | 0.6 ^[4] | | $I_{OL} = 6$ mA, $V_{DDIO} > 1.71$ V |
| SID.GIO#35C | V_{OL1_20mA} | Output low voltage | — | — | 0.4 | | $I_{OL} = 20$ mA for $V_{DDIO} > 3$ V, applicable for overvoltage-tolerant pins only. |
| SID.GIO#36 | V_{OL} | Output voltage LOW level | — | — | 0.6 | | $I_{OL} = 10$ mA (I_{OL_LED}) at 3-V V_{DDIO} |
| SID.GIO#5 | R_{PU} | Pull-up resistor when enabled | 3.5 | 5.6 | 8.5 | k Ω | +25 °C T_A , All V_{DDIO} |
| SID.GIO#6 | R_{PD} | Pull-down resistor when enabled | 3.5 | 5.6 | 8.5 | | |
| SID.GIO#16 | I_{IL} | Input leakage current (absolute value) | — | — | 2 | nA | +25 °C T_A , 3-V V_{DDIO} |
| SID.GIO#17 | C_{PIN} | Max pin capacitance | — | 3 | 7 | pF | — |
| SID.GIO#43 | V_{HYSTTL} | Input hysteresis, LVTTL | 15 | 40 | — | mV | $V_{DDIO} > 2.7$ V. Guaranteed by characterization |
| SID.GIO#44 | $V_{HYSCMOS}$ | Input hysteresis CMOS | $0.05 \times V_{DDIO}$ | — | — | | $V_{DDIO} < 4.5$ V |
| SID.GIO#44A | $V_{HYSCMOS55}$ | Input hysteresis CMOS | 200 | — | — | | |

Table 12. GPIO AC Specifications (Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|------------|------------------|---|-----|-----|-----|------|---------------------------------------|
| SID70 | T_{RISEF} | Rise time in Fast Strong mode | 2 | — | 12 | ns | 3.3-V V_{DDIO} , $C_{load} = 25$ pF |
| SID71 | T_{FALLF} | Fall time in Fast Strong mode | 2 | — | 12 | | |
| SID.GIO#46 | T_{RISES} | Rise time in Slow Strong mode | 10 | — | 60 | | |
| SID.GIO#47 | T_{FALLS} | Fall time in Slow Strong mode | 10 | — | 60 | | |
| SID.GIO#48 | F_{GPIO_OUT1} | GPIO F_{OUT} ; 3.3 V $\leq V_{DDIO} \leq 5.5$ V. Fast Strong mode | — | — | 16 | MHz | 90/10%, 25-pF load |
| SID.GIO#49 | F_{GPIO_OUT2} | GPIO F_{OUT} ; 1.7 V $\leq V_{DDIO} \leq 3.3$ V. Fast Strong mode | — | — | 16 | | |
| SID.GIO#50 | F_{GPIO_OUT3} | GPIO F_{OUT} ; 3.3 V $\leq V_{DDIO} \leq 5.5$ V. Slow Strong mode | — | — | 7 | | |

Note

 4. To drive full bus load at 400 kHz, 6-mA I_{OL} is required at 0.6-V V_{OL} . Parts not meeting this specification can still function, but not at 400 kHz and 400 pF.

Table 12. GPIO AC Specifications (Guaranteed by Characterization) (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|------------|------------------------|---|-----|-----|-----|------|------------------------|
| SID.GIO#51 | F _{GPIO_OUT4} | GPIO F _{OUT} ; 1.7 V ≤ V _{DDIO} ≤ 3.3 V. Slow Strong mode | – | – | 3.5 | MHz | 90/10%, 25-pF load |
| SID.GIO#52 | F _{GPIO_IN} | GPIO input operating frequency; 1.7 V ≤ V _{DDIO} ≤ 5.5 V | – | – | 16 | | 90/10% V _{IO} |

XRES

Table 13. XRES DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|------------|----------------------|------------------------------|-------------------------|--------------------------|-------------------------|------|--------------------------------|
| SID.XRES#1 | V _{IH} | Input voltage HIGH threshold | 0.7 × V _{DDIO} | – | – | V | CMOS input |
| SID.XRES#2 | V _{IL} | Input voltage LOW threshold | – | – | 0.3 × V _{DDIO} | | |
| SID.XRES#3 | C _{IN} | Input capacitance | – | – | 7 | pF | – |
| SID.XRES#4 | V _{HYSXRES} | Input voltage hysteresis | – | 0.05 × V _{DDIO} | – | mV | Guaranteed by characterization |

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 14. PWM AC Specifications (Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|--------------|-----------------------|------------------------------|------------------|-----|----------------|------|--|
| SID.TCPWM.3 | T _{CPWMFREQ} | Operating frequency | – | – | F _c | MHz | F _c max = CLK_SYS. Maximum = 48 MHz |
| SID.TCPWM.4 | T _{PWMENEXT} | Input trigger pulse width | 2/F _c | – | – | ns | For all trigger events |
| SID.TCPWM.5 | T _{PWMEXT} | Output trigger pulse width | 2/F _c | – | – | | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs |
| SID.TCPWM.5A | T _{CRES} | Resolution of counter | 1/F _c | – | – | | Minimum time between successive counts |
| SID.TCPWM.5B | PWM _{RES} | PWM resolution | 1/F _c | – | – | | Minimum pulse width of PWM output |
| SID.TCPWM.5C | Q _{RES} | Quadrature inputs resolution | 1/F _c | – | – | | Minimum pulse width between quadrature-phase inputs |

I²C

Table 15. Fixed I²C AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|------|--------------------|
| SID153 | F _{I2C1} | Bit rate | – | – | 1 | Mbps | – |

UART

Table 16. Fixed UART AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|------|--------------------|
| SID162 | F _{UART} | Bit rate | – | – | 1 | Mbps | – |

SPI

Table 17. Fixed SPI AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|------------------|---|-----|-----|-----|------|--------------------|
| SID166 | F _{SPI} | SPI operating frequency (Master; 6x oversampling) | – | – | 8 | MHz | – |

Table 18. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|------------------|---|-----|-----|-----|------|----------------------------------|
| SID167 | T _{DMO} | MOSI valid after SClock driving edge | – | – | 15 | ns | – |
| SID168 | T _{DSI} | MISO valid before SClock capturing edge | 20 | – | – | | Full clock, late MISO sampling |
| SID169 | T _{HMO} | Previous MOSI data hold time | 0 | – | – | | Referred to slave capturing edge |

Table 19. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|----------------------|--|-----|-----|------------------------------|------|---|
| SID170 | T _{DMI} | MOSI Valid before SClock capturing edge | 40 | – | – | ns | – |
| SID171 | T _{DSO} | MISO Valid after SClock driving edge | – | – | 48 + (3 × T _{CPU}) | | T _{CPU} = 1 / F _{CPU} |
| SID171A | T _{DSO_EXT} | MISO Valid after SClock driving edge in Ext Clk mode | – | – | 48 | | – |
| SID172 | T _{HSO} | Previous MISO data hold time | 0 | – | – | | – |
| SID172A | T _{SSELSCK} | SSEL Valid to first SCK Valid edge | 100 | – | – | | – |

Memory

Table 20. Flash AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------|-------------------------|--|------|-----|-----|--------|--------------------------------------|
| SID.MEM#4 | T _{ROW_WRITE} | Row (Block) write time (erase and program) | – | – | 20 | ms | – |
| SID.MEM#3 | T _{ROW_ERASE} | Row erase time | – | – | 13 | | – |
| SID.MEM#8 | T _{ROWPROGRAM} | Row program time after erase | – | – | 7 | | 25 °C to 55 °C, All V _{DDD} |
| SID178 | T _{BULKERASE} | Bulk erase time (128 KB) | – | – | 35 | | Guaranteed by design |
| SID180 | T _{DEVPROG} | Total device program time | – | – | 25 | s | – |
| SID.MEM#6 | F _{END} | Flash endurance | 100k | – | – | cycles | – |
| SID182 | F _{RET1} | Flash retention, T _A ≤ 55 °C, 100k P/E cycles | 20 | – | – | | – |
| SID182A | F _{RET2} | Flash retention, T _A ≤ 85 °C, 10k P/E cycles | 10 | – | – | | – |

System Resources

Power-on-Reset (POR) with Brown Out

Table 21. Imprecise Power On Reset (IPOR)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|-----------------------|----------------------|------|-----|------|------|--------------------------------|
| SID185 | V _{RISEIPOR} | Rising trip voltage | 0.80 | – | 1.50 | V | Guaranteed by characterization |
| SID186 | V _{FALLIPOR} | Falling trip voltage | 0.70 | – | 1.4 | | |

Table 22. Precise Power On Reset (POR)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------|------------------------|---|------|-----|------|------|--------------------------------|
| SID190 | V _{FALLPPOR} | Brown-out detect (BOD) trip voltage in active/sleep modes | 1.48 | – | 1.62 | V | Guaranteed by characterization |
| SID192 | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep mode | 1.1 | – | 1.5 | | |

SWD Interface

Table 23. SWD Interface Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------|--------------|--|-----------------|-----|-----------------|------|---------------------------------------|
| SID.SWD#1 | F_SWCLK1 | $3.3\text{ V} \leq V_{DDIO} \leq 5.5\text{ V}$ | – | – | 14 | MHz | SWDCLK \leq 1/3 CPU clock frequency |
| SID.SWD#2 | F_SWCLK2 | $1.8\text{ V} \leq V_{DDIO} \leq 3.3\text{ V}$ | – | – | 7 | | SWDCLK \leq 1/3 CPU clock frequency |
| SID.SWD#3 | T_SWDI_SETUP | $T = 1/f_{\text{SWDCLK}}$ | $0.25 \times T$ | – | – | ns | Guaranteed by characterization |
| SID.SWD#4 | T_SWDI_HOLD | $T = 1/f_{\text{SWDCLK}}$ | $0.25 \times T$ | – | – | | |
| SID.SWD#5 | T_SWDO_VALID | $T = 1/f_{\text{SWDCLK}}$ | – | – | $0.50 \times T$ | | |
| SID.SWD#6 | T_SWDO_HOLD | $T = 1/f_{\text{SWDCLK}}$ | 1 | – | – | | |

Internal Main Oscillator

Table 24. IMO AC Specifications

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|------------|-----------------------|---|-----|-----|---------|---------------|--|
| SID.CLK#13 | F _{IMOTOL} | Frequency variation at 48 MHz (trimmed) | – | – | ± 2 | % | $2.7\text{ V} \leq V_{DD} < 5.5\text{ V}$, $-25\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ |
| SID226 | T _{STARTIMO} | IMO start-up time | – | – | 7 | μs | – |
| SID.CLK#1 | F _{IMO} | IMO frequency | – | 48 | – | MHz | – |

Internal Low-speed Oscillator

Table 25. ILO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------|------------------------|-------------------------------|-----|-----|-----|------|--------------------------------|
| SID234 | T _{STARTILO1} | I _{LO} start-up time | – | – | 2 | ms | Guaranteed by characterization |
| SID238 | T _{ILODUTY} | I _{LO} duty cycle | 40 | 50 | 60 | % | |
| SID.CLK#5 | F _{ILO} | I _{LO} frequency | 20 | 40 | 80 | kHz | – |

PD

Table 26. PD DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-------------------|------------------|--|-------|-----|-------|------|----------------------|
| SID.DC.cc_shvt.1 | vSwing | Transmitter Output High Voltage | 1.05 | – | 1.2 | V | – |
| SID.DC.cc_shvt.2 | vSwing_low | Transmitter Output Low Voltage | | – | 0.075 | | – |
| SID.DC.cc_shvt.3 | zDriver | Transmitter output impedance | 33 | – | 75 | Ω | – |
| SID.DC.cc_shvt.4 | zBmcRx | Receiver Input Impedance | 10 | – | | MΩ | Guaranteed by design |
| SID.DC.cc_shvt.5 | Idac_std | Source current for USB standard advertisement | 64 | – | 96 | μA | – |
| SID.DC.cc_shvt.6 | Idac_1p5a | Source current for 1.5 A at 5 V advertisement | 165.6 | – | 194.4 | | – |
| SID.DC.cc_shvt.7 | Idac_3a | Source current for 3 A at 5 V advertisement | 303.6 | – | 356.4 | | – |
| SID.DC.cc_shvt.8 | Rd | Pull-down termination resistance when acting as UFP | 4.59 | – | 5.61 | kΩ | – |
| SID.DC.cc_shvt.9 | Rd_db | Pull-down termination resistance when acting as UFP, with dead battery | 4.08 | – | 6.12 | | – |
| SID.DC.cc_shvt.10 | zOPEN | CC impedance to ground when disabled | 108 | – | | | – |
| SID.DC.cc_shvt.11 | DFP_default_0p2 | CC voltages on DFP side-Standard USB | 0.15 | – | 0.25 | V | – |
| SID.DC.cc_shvt.12 | DFP_1.5A_0p4 | CC voltages on DFP side-1.5 A | 0.35 | – | 0.45 | | – |
| SID.DC.cc_shvt.13 | DFP_3A_0p8 | CC voltages on DFP side-3 A | 0.75 | – | 0.85 | | – |
| SID.DC.cc_shvt.14 | DFP_3A_2p6 | CC voltages on DFP side-3 A | 2.45 | – | 2.75 | | – |
| SID.DC.cc_shvt.15 | UFP_default_0p66 | CC voltages on UFP side-Standard USB | 0.61 | – | 0.7 | | – |
| SID.DC.cc_shvt.16 | UFP_1.5A_1p23 | CC voltages on UFP side-1.5 A | 1.16 | – | 1.31 | | – |
| SID.DC.cc_shvt.17 | Vattach_ds | Deep Sleep attach threshold | 0.3 | – | 0.6 | % | – |
| SID.DC.cc_shvt.18 | Rattach_ds | Deep Sleep pull-up resistor | 10 | – | 50 | kΩ | – |
| SID.DC.cc_shvt.30 | FS_0p53 | Voltage threshold for Fast Swap Detect | 0.49 | – | 0.58 | V | – |

Analog to Digital Converter

Table 27. ADC DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------|------------|---------------------------|--------------------|-----|--------------------|------|--|
| SID.ADC.1 | Resolution | ADC resolution | – | 8 | – | Bits | – |
| SID.ADC.2 | INL | Integral nonlinearity | –1.5 | – | 1.5 | LSB | – |
| SID.ADC.3 | DNL | Differential nonlinearity | –2.5 | – | 2.5 | | – |
| SID.ADC.4 | Gain Error | Gain error | –1.5 | – | 1.5 | | – |
| SID.ADC.5 | VREF_ADC1 | Reference voltage of ADC | V _{DDmin} | – | V _{DDmax} | V | Reference voltage generated from V _{DD} |
| SID.ADC.6 | VREF_ADC2 | Reference voltage of ADC | 1.96 | 2.0 | 2.04 | | Reference voltage generated from bandgap |

Charger Detect

Table 28. Charger Detect Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|--------------|-----------------------|--|-------|-----|-------|------|--------------------|
| DC.CHGDET.1 | V _{DATA_REF} | Data detect voltage in charger detect mode | 250 | – | 400 | mV | – |
| DC.CHGDET.2 | V _{DM_SRC} | DM voltage source in charger detect mode | 500 | – | 700 | | – |
| DC.CHGDET.3 | V _{DP_SRC} | DP voltage source in charger detect mode | 500 | – | 700 | | – |
| DC.CHGDET.4 | I _{DM_SINK} | DM sink current in charger detect mode | 25 | – | 175 | μA | – |
| DC.CHGDET.5 | I _{DP_SINK} | DP sink current in charger detect mode | 25 | – | 175 | | – |
| DC.CHGDET.6 | I _{DP_SRC} | Data contact detect current source | 7 | – | 13 | | – |
| DC.CHGDET.32 | R _{DM_UP} | DP/DM pull-up resistance | 0.9 | – | 1.575 | kΩ | – |
| DC.CHGDET.31 | R _{DM_DWN} | DP/DM pull-down resistance | 14.25 | – | 24.8 | | – |
| DC.CHGDET.29 | R _{DATA_LKG} | Data line leakage on DP/DM | 300 | – | 500 | | – |
| DC.CHGDET.34 | V _{SETH} | Logic Threshold | 1.26 | – | 1.54 | V | – |

V_{BUS} Regulator

Table 29. V_{BUS} Regulator AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------------|--------------------|---|-----|-----|-----|------|---|
| SID.AC.20VREG.1 | T _{START} | Total start up time for the regulator supply output | – | – | 120 | μs | Apply V _{BUS} and measure start time on V _{DDD} pin |
| SID.AC.20VREG.2 | T _{STOP} | Regulator power down time from vreg_en = 0 | – | – | 1 | | Time from assertion of an internal disable signal to load current to decrease from 30 mA to 10 μA |

V_{SYS} Switch

Table 30. V_{SYS} Switch Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------------|-----------|--|-----|-----|-----|------|---|
| SID.DC.VDDDSW.1 | Res_sw | Resistance from supply input to output supply V _{DDD} | – | – | 1.5 | Ω | Measured with a load current of 5 mA to 10 mA on V _{DDD} |

CSA

Table 31. CSA DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------------|--------------|--|-----|-----|-----|------|--|
| OP.CSA_SCP.11 | Rsense | External sense register | – | 10 | – | mΩ | 1% accuracy |
| DC.CSA_SCP.44 | locp_1A | OCP Trip threshold for 1A | – | ±10 | – | % | 1A PD contracts OCP set at 130% of contract value or user programmable |
| DC.CSA_SCP.45 | locp_5A | OCP Trip threshold for 2A, 3A, 4A and 5A contracts | – | ±10 | – | % | 2A, 3A, 4A, and 5A PD contracts OCP set at 130% of contract value OR user programmable |
| DC.rcp_scp.7a | I_csainn_lk | CSP pin input leakage when CSA block is OFF | – | – | 10 | μA | For provider VBUS = 5 V |
| DC.rcp_scp.6a | I_csainp_lk | CSN pin input leakage when CSA block is OFF | – | – | 80 | | |
| DC.sys.3 | I_CSP_CSA_ON | CSP pin current when CSA is ON | – | – | 30 | | |
| DC.sys.4 | I_CSN_CSA_ON | CSN pin current when CSA is ON. | – | – | 100 | | |

V_{BUS} UV/OV

Table 32. V_{BUS} UV/OV Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|--------------|---------------|--|-----|-----|-----|------|--------------------|
| SID.UVOV.1 | $V_{THUVOV1}$ | Voltage threshold accuracy in Active mode using bandgap reference | – | ±3 | – | % | – |
| SID.UVOV.2 | $V_{THUVOV2}$ | Voltage threshold accuracy in Deep Sleep mode using Deep Sleep reference | – | ±5 | – | | |
| SID.COMP_ACC | COMP_ACC | Comparator input offset at 4 s | –15 | – | 15 | mV | |

Consumer and Provider Side PFET Gate Driver

Table 33. Consumer and Provider Side PFET Gate Driver DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------------|-----------|-----------------------------------|-----|-----|-----|------|--------------------|
| SID.DC.PGDO.1 | Rpd | Resistance when “pull_dn” enabled | – | – | 5 | kΩ | – |

Table 34. Consumer and Provider Side PFET Gate Driver AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|---------------|--------------|-------------------------------|-----|-----|-----|------|----------------------|
| SID.AC.PGDO.2 | Tr_discharge | Discharge rate of output node | – | – | 5 | V/μs | Guaranteed by design |

SBU Switch

Table 35. SBU Switch DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------------|-----------------|--|------|-----|------|------|----------------------|
| SID.DC.20sbu.1 | Ron1 | On resistances for Aux switch at 3.3-V input | – | 4 | 7 | Ω | – |
| SID.DC.20sbu.2 | Ron2 | On resistances for Aux switch at 1-V input | – | 3 | 5 | | – |
| SID.DC.20sbu.4 | Ileak1 | Pin leakage current for SBU1, SBU2 | –4.5 | – | 4.5 | μA | – |
| SID.DC.20sbu.5 | Ileak2 | Pin leakage current for LSTX, LSRX, AUX_P, AUX_N | –1 | – | 1 | | – |
| SID.DC.20sbu.6 | Rpu_aux_1 | Pull-up resistance on AUX_P/N | 80 | – | 320 | KΩ | – |
| SID.DC.20sbu.7 | Rpu_aux_2 | Pull-up resistance on AUX_P/N | 0.8 | – | 1.4 | MΩ | – |
| SID.DC.20sbu.8 | Rpd_aux_1 | Pull-down resistance on AUX_P/N | 80 | – | 120 | KΩ | – |
| SID.DC.20sbu.9 | Rpd_aux_2 | Pull-down resistance on AUX_P/N | 0.3 | – | 1.2 | MΩ | – |
| SID.DC.20sbu.10 | Rpd_aux_3 | Pull-down resistance on AUX_P/N | 250 | – | 611 | KΩ | – |
| SID.DC.20sbu.11 | Rpd_aux_4 | Pull-down resistance on AUX_P/N | 0.3 | – | 6.11 | MΩ | – |
| SID.DC.20sbu.16 | OVP_threshold | Over-voltage protection detection threshold above V _{DDIO} | 200 | – | 1200 | mV | – |
| SID.DC.20sbu.17 | Isx_ron_3p3 | On resistances of LSTX/LSRX to SBU1/2 switch at 3.3-V input | – | 8.5 | 17 | Ω | – |
| SID.DC.20sbu.18 | Isx_ron_1 | On resistances of LSTX/LSRX to SBU1/2 switch at 1-V input | – | 5.5 | 11 | | – |
| SID.DC.20sbu.19 | aux_ron_flat_fs | Switch On flat resistances of AUX_P/N to SBU1/2 switch (from 0 to 3.3 V) | – | – | 2.5 | | Guaranteed by design |
| SID.DC.20sbu.20 | aux_ron_flat_hs | Switch On flat resistances of AUX_P/N to SBU1/2 switch (from 0 to 1 V) | – | – | 0.5 | | |
| SID.DC.20sbu.21 | Isx_ron_flat_fs | Switch On flat resistances of LSTX/LSRX to SBU1/2 switch (from 0 to 3.3 V) | – | – | 5 | | |
| SID.DC.20sbu.22 | Isx_ron_flat_hs | Switch On flat resistances of LSTX/LSRX to SBU1/2 switch (from 0 to 1 V) | – | – | 0.5 | | |

Table 36. SBU Switch AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|----------------|--------------------|--|-----|-----|-----|------|----------------------|
| SID.AC.20sbu.1 | Con | Switch On capacitance | – | – | 120 | pF | – |
| SID.AC.20sbu.2 | Coff | Switch Off capacitance - Connector side | – | – | 80 | | – |
| SID.AC.20sbu.3 | Off_isolation | Switch isolation at F=1 MHz | –50 | – | | dB | – |
| SID.AC.20sbu.4 | T _{ON} | SBU Switch turn-on time | – | – | 200 | μs | – |
| SID.AC.20sbu.5 | T _{OFF} | SBU Switch turn-off time | – | – | 400 | | – |
| SID.AC.20sbu.6 | Off_isolation_tran | Coupling on SBU1, 2 terminated to 50 ohm, switch-OFF, Rail-to-rail toggling on LSTX/LSRX | –60 | – | 60 | mV | Guaranteed by design |
| SID.AC.20sbu.7 | X_talk_AC | Crosstalk of switch at F=1 MHz SBU1/2 to SBU2/1 | –50 | – | – | dB | |
| SID.AC.20sbu.8 | X_talk_tran | Check voltage coupling on SBU2(1) when Data is transferred from LSTX (RX) to SBU1 (2) | –70 | – | 70 | mV | |

DP/DM Switch
Table 37. DP/DM Switch DC Specifications (Charger Detect Block is Disconnected from DPLUS_TOP, DMINUS_TOP, DPLUS_BOT, and DMINUS_BOT through Switch)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|----------------|---------------|---|-----|-----|-----|------|----------------------|
| SID.DC.dpdm.1 | RON_HS | DPDM On resistance (0 to 0.5 V) - HS mode | – | – | 8 | Ω | – |
| SID.DC.dpdm.2 | RON_FS | DPDM On resistance (0 to 3.3 V) - FS mode | – | – | 12 | | – |
| SID.DC.dpdm.5 | Con_FS | Switch On capacitance at 6 MHz - FS mode | – | – | 50 | pF | Guaranteed by design |
| SID.DC.dpdm.6 | Con_HS | Switch on capacitance at 240 MHz - HS mode | – | – | 10 | | – |
| SID.DC.dpdm.9 | ileak_pin | Pin leakage at DP/DM connector side and Host side | – | – | 1 | μA | – |
| SID.DC.dpdm.10 | RON_UART | DPDM On resistance for UART lines (0 to 3.3 V) | – | – | 17 | Ω | – |
| SID.DC.dpdm.11 | RON_FLAT_HS | DPDM On Flat resistance in HS mode (0 to 0.4 V) | – | – | 0.5 | | Guaranteed by design |
| SID.DC.dpdm.12 | RON_FLAT_FS | DPDM On flat resistance in FS mode (0 to 3.3 V) | – | – | 4 | | |
| SID.DC.dpdm.13 | RON_FLAT_UART | DPDM UART On Flat resistance (0 to 3.3 V) | – | – | 4 | | |

Table 38. DP/DM Switch AC Specifications (Charger Detect Block is Disconnected from DPLUS_TOP, DMINUS_TOP, DPLUS_BOT, and DMINUS_BOT through Switch)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|----------------|-----------------------|---|-----|-----|-----|------|----------------------|
| SID.AC.dpdm.5 | T _{ON} | DP/DM Switch turn-on time | – | – | 200 | μs | – |
| SID.AC.dpdm.6 | T _{OFF} | DP/DM Switch turn-off time | – | – | 0.4 | | Guaranteed by design |
| SID.AC.dpdm.7 | T _{ON_VPUMP} | DP/DM charge pump startup time | – | – | 200 | | |
| SID.AC.dpdm.8 | Off_isolation_HS | Switch-off isolation for HS | –20 | – | – | db | |
| SID.AC.dpdm.9 | Off_isolation_FS | Switch-off isolation for FS | –50 | – | – | | |
| SID.AC.dpdm.10 | X _{talk} | Crosstalk of Switch from FS to HS at F = 12 MHz | –50 | – | – | | |
| SID.AC.dpdm.11 | uart_coupling | Peak-to-peak coupling of UART signal to DP lines (UART signal 0 to 3.3 V) | – | – | 20 | mV | |

VCONN Switch

Table 39. VCONN Switch DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-------------------|------------------|---|-----|-----|------|------|----------------------|
| SID.DC.20VCONN.1 | R _{on} | Switch ON resistance at V _{5V} = 5 V with 215-mA load current | – | 0.7 | 1.3 | Ω | – |
| SID.DC.20VCONN.9 | I _{OCP} | Overcurrent detection range for CC1/CC2 | 550 | – | – | mA | – |
| SID.DC.20VCONN.10 | OVP_threshold | Overvoltage detection threshold above V _{DD} or V _{5V} , whichever is higher | 200 | – | 1200 | mV | – |
| SID.DC.20VCONN.11 | OVP_hysteresis | Overvoltage detection hysteresis | 50 | – | 200 | | Guaranteed by design |
| SID.DC.20VCONN.12 | OCP_hysteresis | Overcurrent detection hysteresis | 20 | – | 60 | mA | – |
| SID.DC.20VCONN.14 | OVP_threshold_on | Overvoltage detection threshold above V _{5V} of CC1/2, with CC1 or CC2 switch enabled. | 200 | – | 700 | mV | – |

Table 40. VCONN Switch AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|------------------|------------------|----------------------------|-----|-----|-----|------|----------------------|
| SID.AC.20VCONN.1 | T _{ON} | VCONN switch turn-on time | – | – | 200 | μs | – |
| SID.AC.20VCONN.2 | T _{OFF} | VCONN switch turn-off time | – | – | 3 | | Guaranteed by design |

V_{BUS}

Table 41. V_{BUS} Discharge Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/Conditions |
|-----------------|------------------|-------------------------|------|-----|------|------|--------------------|
| SID.VBUS.DISC.1 | R _{on1} | 20-V NMOS ON resistance | 1500 | – | 3000 | Ω | – |
| SID.VBUS.DISC.2 | R _{on2} | 20-V NMOS ON resistance | 750 | – | 1500 | | – |
| SID.VBUS.DISC.3 | R _{on3} | 20-V NMOS ON resistance | 500 | – | 1000 | | – |
| SID.VBUS.DISC.4 | R _{on4} | 20-V NMOS ON resistance | 375 | – | 750 | | – |
| SID.VBUS.DISC.5 | R _{on5} | 20-V NMOS ON resistance | 300 | – | 600 | | – |

Ordering Information

Table 42 lists the EZ-PD CCG5C part numbers and features.

Table 42. EZ-PD CCG5C Ordering Information

| Part Number | Application | Type-C Ports | Dead Battery Termination | Termination Resistor | Role | Package |
|------------------|---------------------|--------------|--------------------------|---------------------------------------|------|------------|
| CYPD5126-40LQXIT | Notebooks, Desktops | 1 | Yes | Rp ^[5] , Rd ^[6] | DRP | 40-pin QFN |
| CYPD5137-40LQXIT | Dock | 1 | No | | | |

Ordering Code Definitions

| | | | | | | | | | | | | |
|----|----|---|---|---|---|---|----|----|---|---|---|--|
| CY | PD | 5 | 1 | X | X | - | XX | LQ | X | I | T | |
| | | | | | | | | | | | | T = Tape and Reel |
| | | | | | | | | | | | | Temperature Grade: I = Industrial |
| | | | | | | | | | | | | Pb-free |
| | | | | | | | | | | | | Package Type: LQ LQ = QFN |
| | | | | | | | | | | | | Number of pins in the package: XX = 40 |
| | | | | | | | | | | | | Application specific X = 6 or 7 |
| | | | | | | | | | | | | Indicates Dead battery termination is supported or not X = 2 or 3 |
| | | | | | | | | | | | | Number of Type-C Ports: 1 = 1 Port |
| | | | | | | | | | | | | Product Type: 5 = Fifth-generation product family, CCG5C |
| | | | | | | | | | | | | Marketing Code: PD = Power Delivery product family |
| | | | | | | | | | | | | Company ID: CY = Cypress |

Notes

5. Termination resistor denoting a downstream facing port.
6. Termination resistor denoting an accessory or upstream facing port.

Packaging

Table 43. Package Characteristics

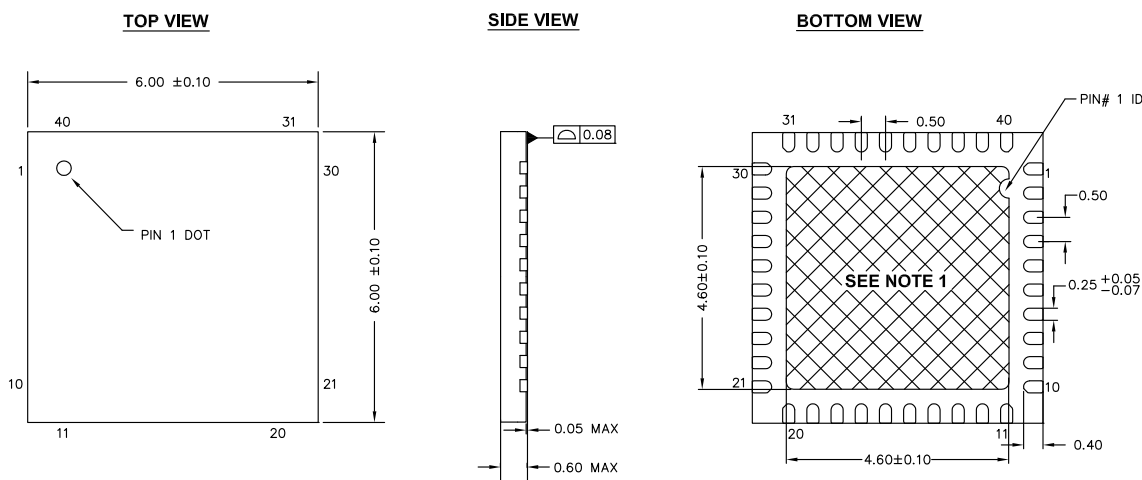
| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------|------------------------------------|------------|-----|-----|------|------|
| T _A | Operating ambient temperature | Industrial | -40 | 25 | 85 | °C |
| T _J | Operating junction temperature | | -40 | 25 | 100 | |
| T _{JA} | Package θ_{JA} (40-pin QFN) | — | — | — | 19.3 | °C/W |
| T _{JC} | Package θ_{JC} (40-pin QFN) | — | — | — | 13.6 | |


Table 44. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Maximum Time within 5 °C of Peak Temperature |
|------------|--------------------------|--|
| 40-pin QFN | 260 °C | 30 seconds |

Table 45. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

| Package | MSL |
|------------|-------|
| 40-pin QFN | MSL 3 |

Figure 7. 40-Pin QFN (6 × 6 × 0.5 mm), LR40A/LQ40A 4.6 × 4.6 E-PAD (Sawn) Package Outline, 001-80659

NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ± 2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

Acronyms

Table 46. Acronyms Used in this Document

| Acronym | Description |
|--------------------------|---|
| ADC | analog-to-digital converter |
| API | application programming interface |
| Arm® | advanced RISC machine, a CPU architecture |
| CC | configuration channel |
| BOD | Brown out Detect |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| CS | current sense |
| DB | dead battery |
| DFP | downstream facing port |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DP | DisplayPort, digital display interface developed by Video Electronics Standards Association. |
| DRP | dual-role power |
| EEPROM | electrically erasable programmable read-only memory |
| EMCA | a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports |
| EMI | electromagnetic interference |
| ESD | electrostatic discharge |
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output |
| IC | integrated circuit |
| IDE | integrated development environment |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| I/O | input/output, see also GPIO |
| LVD | low-voltage detect |
| LVTTTL | low-voltage transistor-transistor logic |
| MCU | microcontroller unit |
| NC | no connect |
| NMI | nonmaskable interrupt |

Table 46. Acronyms Used in this Document *(continued)*

| Acronym | Description |
|---------|--|
| NVIC | nested vectored interrupt controller |
| opamp | operational amplifier |
| OCP | overcurrent protection |
| OVP | overvoltage protection |
| PCB | printed circuit board |
| PD | power delivery |
| PGA | programmable gain amplifier |
| PHY | physical layer |
| POR | power-on reset |
| PRES | precise power-on reset |
| PSoC® | Programmable System-on-Chip™ |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RX | receive |
| SAR | successive approximation register |
| SCL | I ² C serial clock |
| SDA | I ² C serial data |
| S/H | sample and hold |
| SPI | Serial Peripheral Interface, a communications protocol |
| SRAM | static random access memory |
| SWD | serial wire debug, a test protocol |
| TBT | Thunderbolt, hardware interface standard for peripherals developed by Intel. |
| TX | transmit |
| Type-C | a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| USB | Universal Serial Bus |
| USBIO | USB input/output, CCG5C pins used to connect to a USB port |
| XRES | external reset I/O pin |

Document Conventions

Units of Measure

Table 47. Units of Measure

| Symbol | Unit of Measure |
|--------|------------------------|
| °C | degrees Celsius |
| Hz | hertz |
| KB | 1024 bytes |
| kHz | kilohertz |
| kΩ | kilo ohm |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msp | megasamples per second |
| μA | microampere |
| μF | microfarad |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| V | volt |

References and Links to Applications Collateral

Knowledge Base Articles

- Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG5 - KBA210740
- Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG5 Using PSoC® Programmer and MiniProg3 - KBA96477
- CCGX Frequently Asked Questions (FAQs) - KBA97244
- Handling Precautions for CY4501 CCG1 DVK - KBA210560
- Cypress EZ-PD™ CCGx Hardware - KBA204102
- Difference between USB Type-C and USB-PD - KBA204033
- CCGx Programming Methods - KBA97271
- Getting started with Cypress USB Type-C Products - KBA04071
- Type-C to DisplayPort Cable Electrical Requirements
- Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273
- Termination Resistors Required for the USB Type-C Connector – KBA97180
- VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270
- Need for Regulator and Auxiliary Switch in Type-C to DisplayPort (DP) Cable Solution - KBA97274
- Need for a USB Billboard Device in Type-C Solutions – KBA97146
- CCG1 Devices in Type-C to Legacy Cable/Adapter Assemblies – KBA97145
- Cypress USB Type-C Controller Supported Solutions – KBA97179
- Termination Resistors for Type-C to Legacy Ports – KBA97272
- Handling Instructions for CY4502 CCG2 Development Kit – KBA97916
- Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976
- Power Adapter Application Using CCG3 Devices - KBA210975
- Methods to Upgrade Firmware on CCG3 Devices - KBA210974
- Device Flash Memory Size and Advantages - KBA210973
- Applications of EZ-PD™ CCG5 - KBA210739

Application Notes

- AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers
- AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2
- AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2
- AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers
- AN210771 - Getting Started with EZ-PD™ CCG4

Reference Designs

- EZ-PD™ CCG2 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to HDMI/DVI/VGA Adapter Solution
- EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution
- CCG1 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- CCG1 USB Type-C to Legacy USB Device Cable Paddle Card Reference Schematics
- EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle
- EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution
- CCG2 20W Power Adapter Reference Design
- CCG2 18W Power Adapter Reference Design
- EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit

Kits

- CY4501 CCG1 Development Kit
- CY4502 EZ-PD™ CCG2 Development Kit
- CY4531 EZ-PD CCG3 Evaluation Kit
- CY4541 EZ-PD™ CCG4 Evaluation Kit

Datasheets

- CCG1 Datasheet: USB Type-C Port Controller with Power Delivery
- CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C
- CCG2: USB Type-C Port Controller Datasheet
- CCG3: USB Type-C Controller Datasheet
- CCG5: USB Type-C Controller Datasheet

Document History Page

| Document Title: EZ-PD™ CCG5C, USB Type-C Port Controller Document Number: 002-23803 | | | | |
|--|---------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 6164669 | SUDH | 05/17/2018 | New data sheet. |
| *A | 6271142 | SUDH | 08/02/2018 | Changed status from Advance to Preliminary. Updated General Description (description). Updated Features : Updated USB-PD (description). Updated Power System Overview (description). Updated Pinouts : Updated Table 3 : updated description for pin 31. Updated Application Diagram : Updated Figure 6 . Updated Electrical Specifications : Updated Absolute Maximum Ratings : Updated Table 8 : Added ESD_HBM_SBU parameter and its details. Updated System Resources : Updated VCONN Switch : Updated Table 39 : Updated details in "Max" column for I _{OCp} parameter. |
| *B | 6352555 | SUDH | 11/14/2018 | Changed status from Preliminary to Final. Updated Features : Removed "Type-C and USB-PD Support". Added USB-PD . Added Type-C . Added Legacy Charging . Added Protection . Added Mux . Added LDO . Added CSA . Added PFET Gate Drivers . Removed "Low-Power Operation". Added Operating Range . Updated Packages (description). Updated Functional Overview : Updated USB-PD Subsystem (SS) : Updated USB-PD Physical Layer : Updated Figure 1 . Updated USB 2.0 Mux : Updated Figure 3 . Updated Power System Overview : Updated Peripherals : Added Table 2 . Updated Pinouts : Updated Figure 5 . Updated Application Diagram : Updated Figure 6 . |

Document History Page *(continued)*

| Document Title: EZ-PD™ CCG5C, USB Type-C Port Controller Document Number: 002-23803 | | | | |
|--|---------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| *B (cont.) | 6352555 | SUDH | 11/14/2018 | Updated Electrical Specifications : Updated Device-Level Specifications : Updated Table 9 (Changed maximum value of V_{DD} parameter from 3.6 V to 3.65 V corresponding to spec ID SID.PWR#1_A). Updated GPIO : Updated Table 11 (Added $V_{OL_I2C_2}$, $V_{OL_I2C_3}$, V_{OL1_20mA} parameters and their details). Updated System Resources : Updated Power-on-Reset (POR) with Brown Out : Updated Table 21 (Updated table title only). Updated Table 22 (Updated table title only). Updated CSA : Updated Table 31 (Updated entire table). Updated DP/DM Switch : Updated Table 37 (Updated table title only). Updated Table 38 (Updated table title only). Updated VCONN Switch : Updated Table 39 (Updated details in “Description” column corresponding to “OVP_threshold_on” parameter). Updated Ordering Information : Updated Table 42 (Updated part numbers and updated details in “Termination Resistor” column). Removed Note “Termination resistor denoting dead-battery termination.” and its reference. Updated Ordering Code Definitions . Updated Acronyms : Added “DP” and “TBT”. Updated References and Links to Applications Collateral : Updated Datasheets : Added “CCG5”. |
| *C | 6396028 | SUDH | 11/28/2018 | Updated CSA DC Specifications . Updated conditions for $V_{OL_I2C_3}$. |
| *D | 6474710 | SUDH | 02/18/2019 | Updated Features and USB 2.0 Mux . Updated Figure 6 . Updated Copyright information. |

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