EiceDRIVER™ 1EDR314xHQE (1EDR-X3 Compact)

Datasheet

Technical documents
Kits and boards
Support

1EDR314xHQE (1EDR-X3 Compact)

Single-channel isolated gate driver IC

Features

- Single-channel isolated gate driver
- To be used with 600 V/650 V/1200 V/1700 V/2300 V IGBTs, Si and SiC MOSFETs
- +6 A / -6.5 A typical source/sink peak output current
- 40 ns propagation delay with 7 ns skew and 8 ns skew+
- 35 V absolute maximum output supply voltage
- High common-mode transient immunity CMTI > 300 kV/µs
- Separate source and sink outputs with active shutdown and short circuit clamping
- Secondary ground for accurate UVLO monitoring in case of bipolar driving
- Galvanically isolated coreless transformer gate driver
- 3.3 V and 5 V input supply voltage
- Suitable for operation at high ambient temperature and in fast switching applications
- Safety certifications
  - Single protection according to UL 1577 with V_{ISO} = 5.7 kV (rms) for 1 min (E311313)
  - Reinforced insulation according to IEC 60747-17 with V_{IORM} = 1767 V (peak) (planned)

RoHS

Green

AEC Qualified

Potential applications

- On board chargers
- DC/DC converters
- Auxiliary drives
- DC charging stations
- Solar inverters
- Commercial heating, ventilation and air conditioning (HVAC) systems
- DC/AC inverters

Product validation

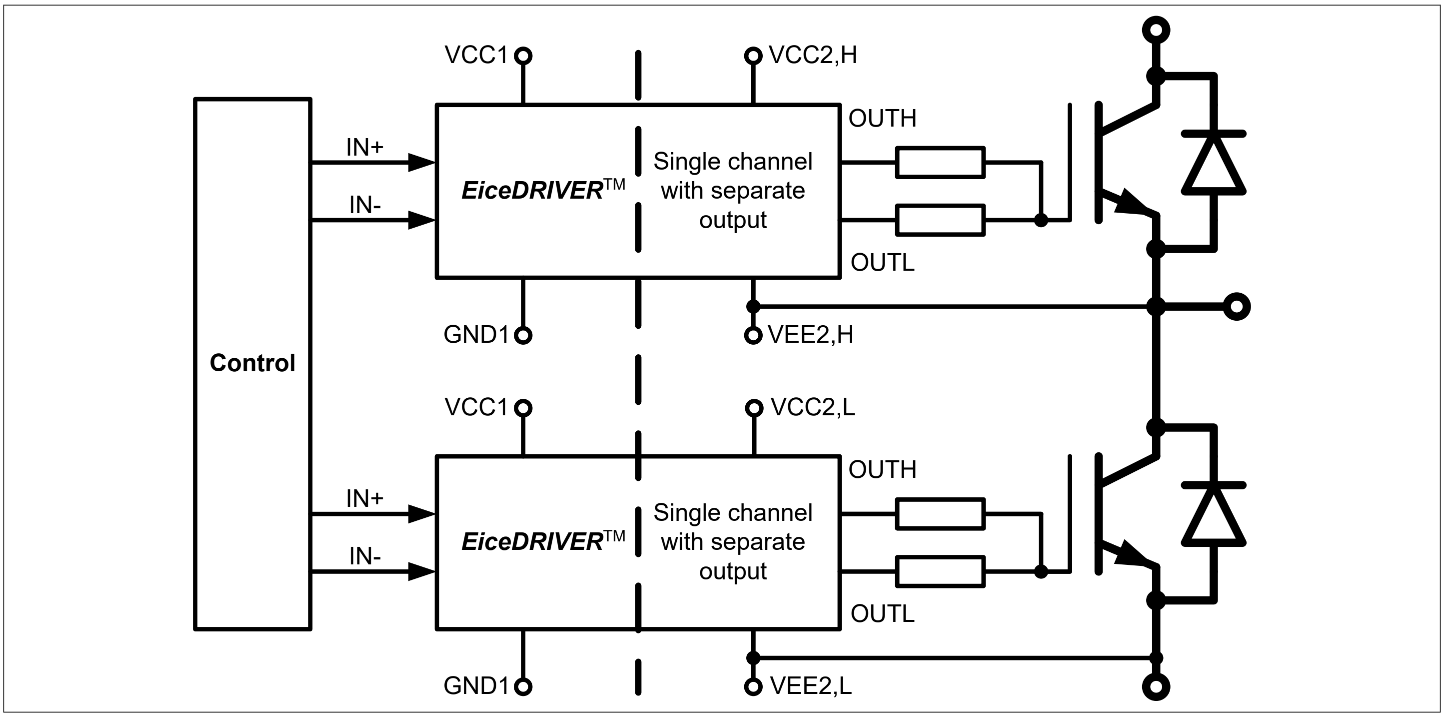
Qualified according to AEC-Q100, rev. H

Description

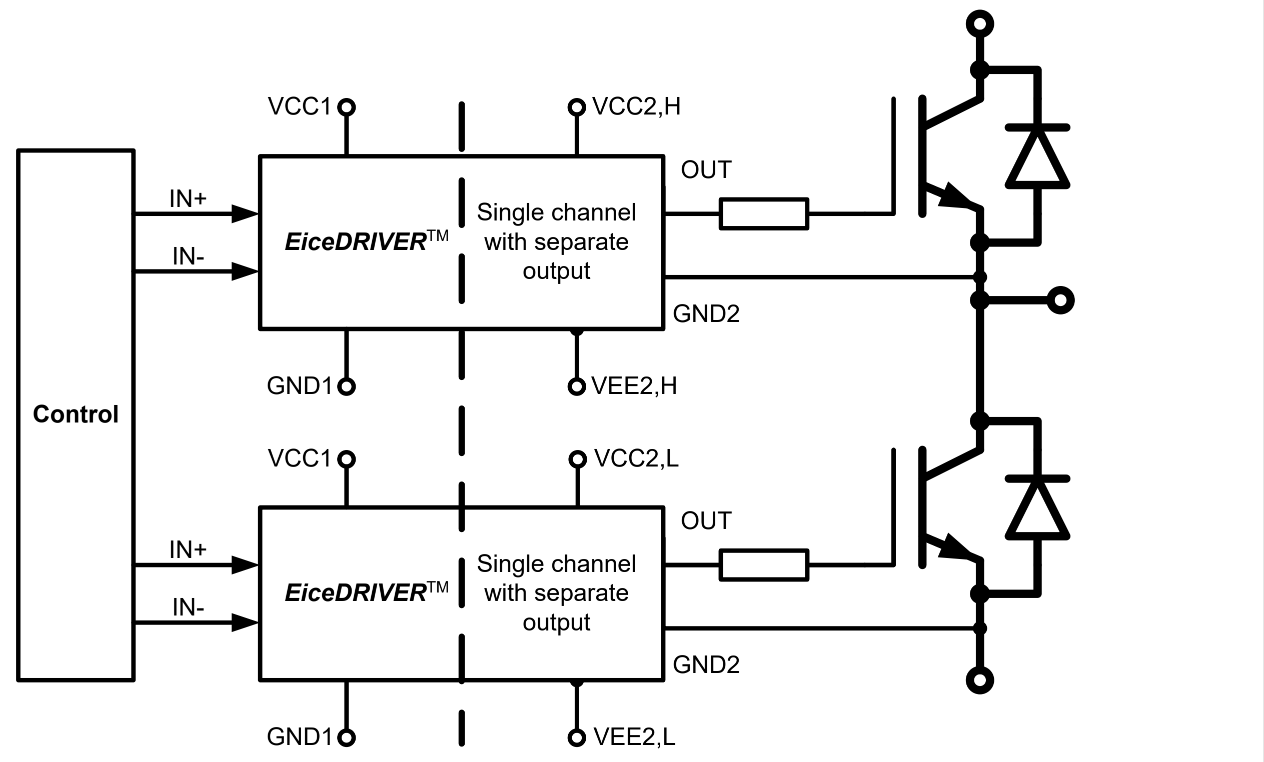
The EiceDRIVER™ 1EDR314xHQE gate driver ICs are high-performance galvanically isolated single-channel gate drivers designed for driving IGBTs, MOSFETs and SiC MOSFETs. They are available in an 8-pin LDSO-8-1 package, with 8 mm input-to-output creepage and reinforced insulation, and they provide a typical output current of 6.5 A.

The 1EDR3140HQE and 1EDR3147HQE are optimized for unipolar driving, providing separate source and sink outputs, while the 1EDR3144HQE and 1EDR3146HQE are targeting bipolar driving, offering a *GND2* pin as secondary ground, to which the output UVLO monitor is connected.

The input logic pins operate on a wide input voltage range of 3 V to 5.5 V using CMOS threshold levels to support 3.3 V microcontrollers. Data transfer across the isolation barrier is realized by the coreless transformer technology. All variants have input and output undervoltage lockout (UVLO) and active shutdown. With excellent common-mode transient immunity (CMTI), low part-to-part propagation delay mismatch, and fast signal propagation, these products are best suited for fast-switching applications.



Typical application diagram for 1EDR3140HQE and 1EDR3147HQE



Typical application diagram for 1EDR3144HQE and 1EDR3146HQE

Table 1 **Ordering information for the 300-mil package**

Product type	Typical UVLO (V_{UVLOL2}/ V_{UVLOH2})	Typical output current source/sink	Output configuration	UL 1577 Certification(single isolation)	IEC 60747-17 Certification (reinforced isolation)	Package marking
1EDR3140HQE	8.5 V / 9.3 V	6 A / 6.5 A	Separate outputs	E311313	(planned)	R3140HQE
1EDR3144HQE	12.5 V / 13.6 V	6 A / 6.5 A	Secondary ground	E311313	(planned)	R3144HQE
1EDR3146HQE	14.75 V / 16.0 V	6 A / 6.5 A	Secondary ground	E311313	(planned)	R3146HQE
1EDR3147HQE	14.75 V / 16.0 V	6 A / 6.5 A	Separate outputs	E311313	(planned)	R3147HQE

Table 2 **Related evaluation boards**

Board name	Gate driver	Power transistor	Short description
EVAL-1EDR3147HQE-SIC	1EDR3147HQE	AIMZH120R060M1T	Half-bridge board with 1EDR3147HQE gate drivers, using unipolar driving voltages and paired with CoolSiC™ devices in TO-247-4 package
EVAL-1EDR3146HQE-SIC	1EDR3146HQE	AIMZH120R060M1T	Half-bridge board with 1EDR3146HQE gate drivers, using bipolar driving voltages and paired with CoolSiC™ devices in TO-247-4 package

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1 Block diagram reference

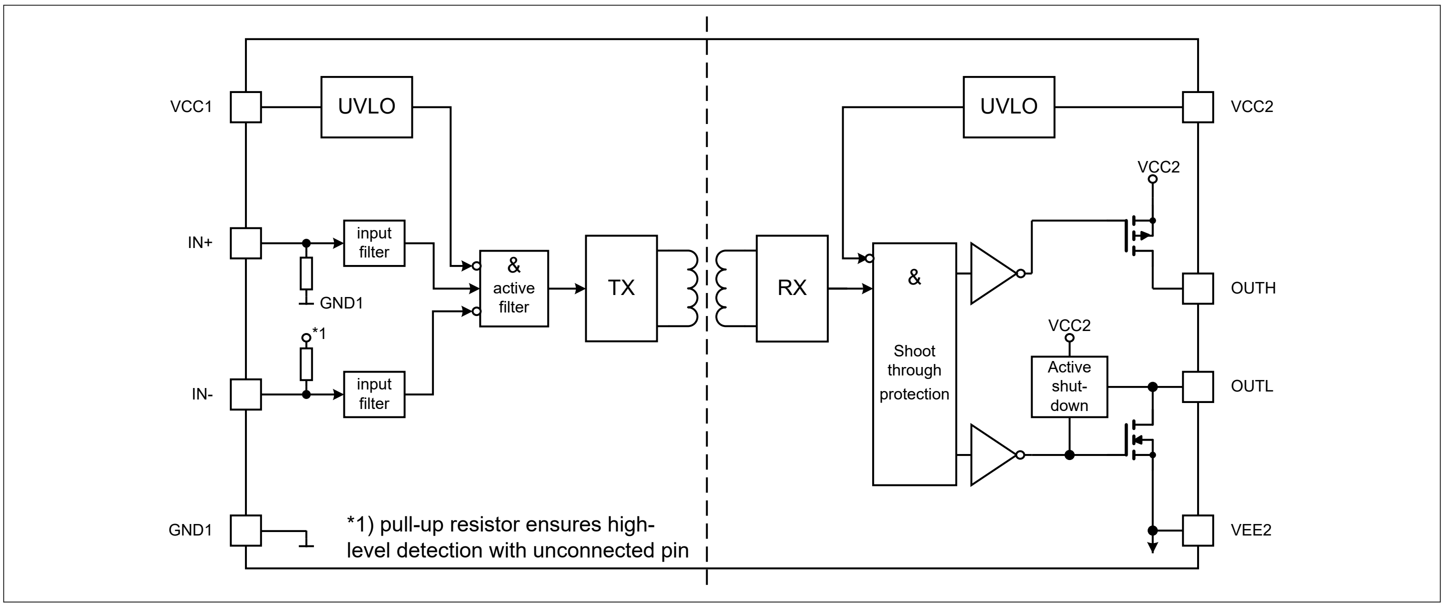


Figure 3 Block diagram for 1EDR3140HQE and 1EDR3147HQE

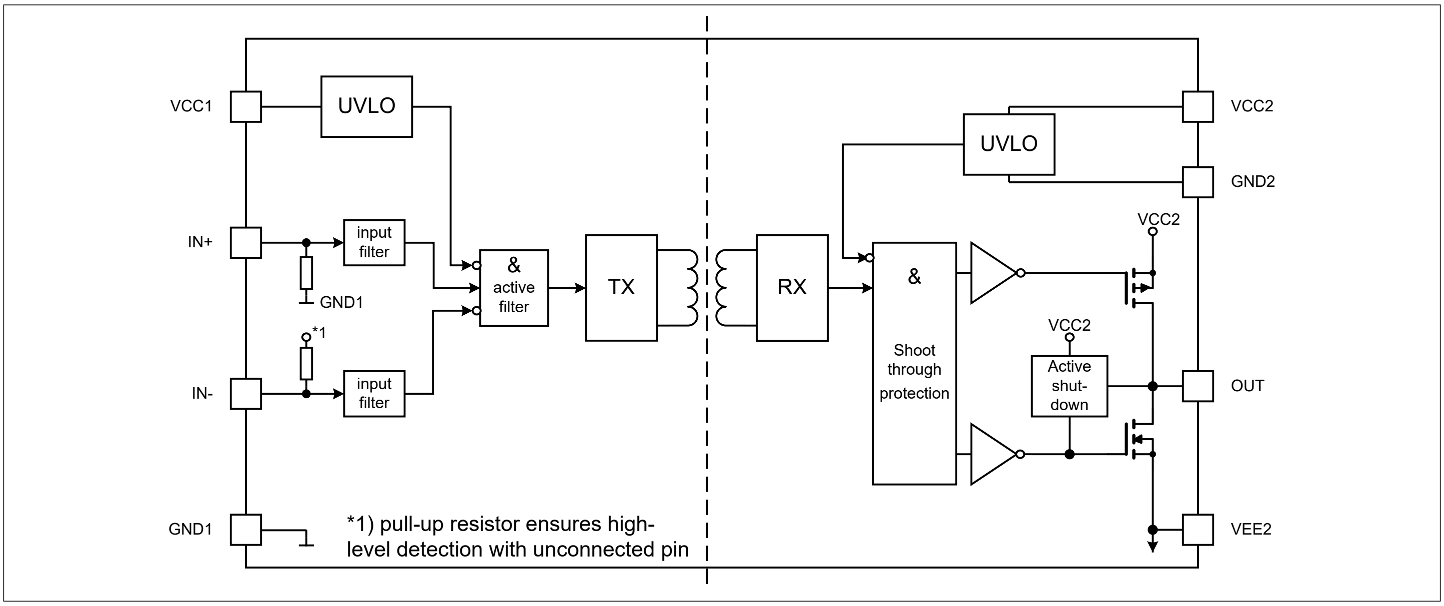


Figure 4 Block diagram for 1EDR3144HQE and1EDR3146HQE

2 Pin configuration and description

Pin configuration and description for 1EDR3140HQE and 1EDR3147HQE

Table 3 **Pin configuration for 1EDR3140HQE and 1EDR3147HQE**

Pin No.	Name	Function
1	*VCC1*	Positive power supply input side
2	*IN+*	Non-inverted driver input (active high)
3	*IN-*	Inverted driver input (active low)
4	*GND1*	Input side ground
5	*VCC2*	Positive power supply output side
6	*OUTH*	Driver sourcing output
7	*OUTL*	Driver sinking output
8	*VEE2*	Output side ground

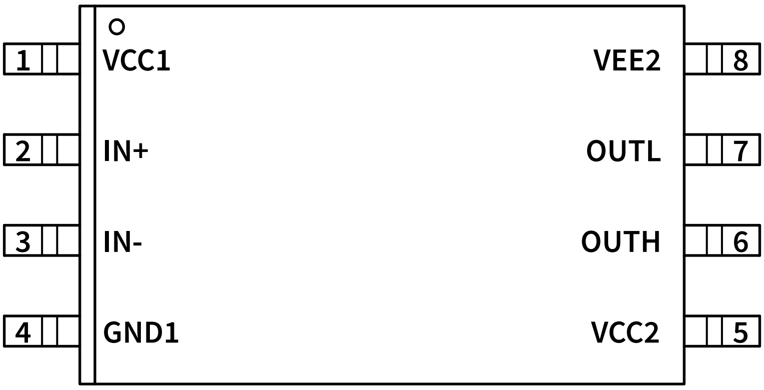


Figure 5 Pin configuration for 1EDR3140HQE and 1EDR3147HQE

Pin description

- *VCC1*: Input supply voltage. Connect to 3.3 V or 5 V and decouple with a capacitor to *GND1*. Use a low-ESR and low-ESL capacitor placed as close to the device as possible
- *GND1*: Input ground. All the input side signals, *VCC1*, *IN+* and *IN-* are referenced to this ground
- *IN+*: Non-inverted control signal for driver output. An internal filter provides robustness against noise at *IN+*. If left open, an internal, weak pull-down resistor pulls this pin to a low state, as shown in Figure 3
- *IN-*: Inverted control signal for driver output. An internal filter provides robustness against noise at *IN-*. If left open, an internal, weak pull-up resistor pulls this pin to a high state, as shown in Figure 3
- *VCC2*: Output positive power supply rail. Connect a decoupling capacitor from this pin to *VEE2*. Use a low-ESR and low-ESL capacitor placed as close to the device as possible
- *VEE2*: Output negative supply rail. For drivers without a *GND2* pin, this is the reference for the output side UVLO levels. In case of a bipolar supply (positive and negative voltage referred to IGBT emitter or MOSFET source), this pin should be connected to the negative supply voltage
- *OUTH*: Driver sourcing output pin used to charge the gate of the external transistor (IGBT or MOSFET). During the ON-state, this output is connected to *VCC2*. This output is controlled by *IN+* and *IN-* and is turned off by an UVLO event
- *OUTL*: Driver sinking output pin used to discharge the gate of the external transistor (IGBT or MOSFET). During the OFF-state, this output is connected to *VEE2*. This output is controlled by *IN+* and *IN-*. In case of an UVLO event, *OUTL* is actively pulled low. If the gate driver output is not supplied, the active shutdown circuit keeps the output voltage at a low level

Pin configuration and description for 1EDR3144HQE and 1EDR3146HQE

Table 4 **Pin configuration for 1EDR3144HQE and 1EDR3146HQE**

Pin No.	Name	Function
1	*VCC1*	Positive power supply input side
2	*IN+*	Non-inverted driver input (active high)
3	*IN-*	Inverted driver input (active low)
4	*GND1*	Input side ground
5	*VCC2*	Positive power supply output side
6	*OUT*	Driver sourcing and sinking output
7	*GND2*	Signal ground output side
8	*VEE2*	Negative power supply output side

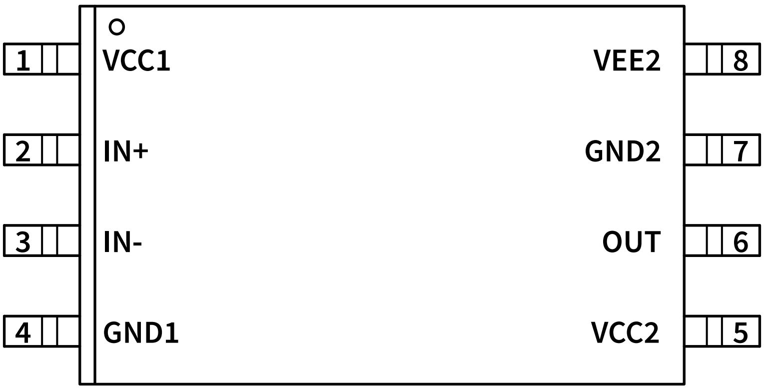


Figure 6 **Pin configuration for 1EDR3144HQE and 1EDR3146HQE**

Pin description

- *VCC1*: Input supply voltage. Connect to 3.3 V or 5 V and decouple with a capacitor to *GND1*. Use a low-ESR and low-ESL capacitor placed as close to the device as possible
- *GND1*: Input ground. All the input side signals, *VCC1*, *IN+* and *IN-* are referenced to this ground
- *IN+*: Non-inverted control signal for driver output. An internal filter provides robustness against noise at *IN+*. If left open, an internal, weak pull-down resistor pulls this pin to a low state, as shown in Figure 4
- *IN-*: Inverted control signal for driver output. An internal filter provides robustness against noise at *IN-*. If left open, an internal, weak pull-up resistor pulls this pin to a high state, as shown in Figure 4
- *VCC2*: Output positive power supply rail. Connect a decoupling capacitor from this pin to *VEE2*. Use a low-ESR and low-ESL capacitor placed as close to the device as possible
- *VEE2*: Output negative supply rail for gate drivers with *GND2* pin. In case of a bipolar supply (positive and negative voltage referred to IGBT emitter or MOSFET source), this pin should be connected to the negative supply voltage
- *OUT*: Combined driver sourcing and sinking output pin used to charge and discharge the gate of the external transistor (IGBT or MOSFET). During the ON-state, this output is connected to *VCC2* and during the OFF- state this output is connected to *VEE2*. The output is controlled by *IN+* and *IN-*. In case of an UVLO event, this output is turned off and the active shut down keeps the output voltage at a low level
- *GND2*: Reference for the output side positive and negative power supply voltages. This pin is connected to the IGBT emitter or the MOSFET Kelvin source. *GND2* is the reference for the output side UVLO levels. In case a unipolar output supply is used, this pin should be connected to *VEE2*

3 Electrical characteristics and parameters

3.1 Absolute maximum ratings

Table 5 Absolute maximum ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Operating the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device reliability may be affected by exposure to absolute-maximum-rated conditions for extended periods of time.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power supply input side voltage	V_{VCC1}	-0.3		17	V	V_{VCC1} - V_{GND1}
Power supply output side voltage	V_{VCC2}	-0.3		35	V	V_{VCC2} - V_{VEE2}
Positive power supply output side voltage	V_{VCC2}	-0.3		35	V	V_{VCC2} - V_{GND2}
Negative power supply output side voltage	V_{VEE2}	-35		0.3	V	V_{VEE2} - V_{GND2}
Gate driver output voltage	V_{OUT}	V_{VEE2} - 0.3		V_{VCC2} + 0.3	V	1EDR3146HQE, 1EDR3144HQE
Gate driver source output voltage	V_{OUTH}	V_{VCC2} - 35		V_{VCC2} + 0.3	V	1EDR3140HQE, 1EDR3147HQE
Gate driver sink output voltage	V_{OUTL}	V_{VEE2} - 0.3		V_{VEE2} + 35	V	1EDR3140HQE, 1EDR3147HQE
Logic input voltages (IN+, IN-)	V_{IN}	-0.3		17	V	
Dynamic logic input voltages (IN+, IN-)	V_{INdyn}	-5		17	V	1) $t_{IN} < 100$ ns, d < 0.01
Input to output offset voltage	V_{OFFSET}			2300	V	2) $V_{OFFSET} = \lvert V_{VEE2} - V_{GND1} \rvert$
ESD robustness - human body model	$\lvert V_{ESD,HBM} \rvert$			4	kV	3)
ESD robustness - charged device model	*ESD,CDM*			TC1500		4)
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{Stg}	-55		150	°C	
Power dissipation (input side)	$P_{D,IN}$			100	mW	5) T_A = 85 °C
Power dissipation (output side)	$P_{D,OUT}$			550	mW	6) T_A = 85 °C
Thermal resistance junction to ambient	$R_{thJA,OUT}$			113	K/W	T_A = 85 °C, 2s2p - no vias, P_J = 550 mW
Characterization parameter junction to package top	Ψ_{Jtop}			5.7	K/W	T_A = 85 °C, 2s2p - no vias, P_J = 550 mW

1) Parameter is not subject to production test - verified by design/characterization

2) for functional operation only

3) According to AEC Q100-002

4) According to AEC Q100-011

5) *IC input-side power dissipation is derated linearly with 8.85 mW/°C above 138.7 °C*

6) *IC output-side power dissipation is derated linearly with 8.85 mW/°C above 88 °C*

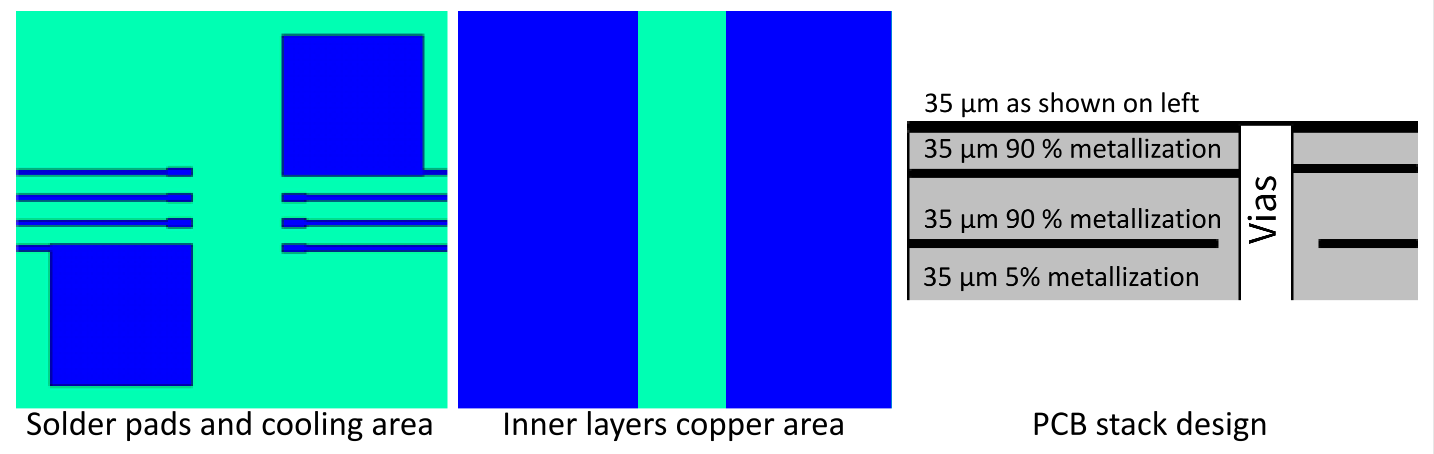


Figure 7 **Reference layout for thermal data**

This PCB layout represents the reference layout used for the thermal characterization.

3.2 Recommended operating conditions

Table 6 **Recommended operating conditions**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power supply input side voltage	V_{VCC1}	3.0		5.5	V	V_{VCC1} - V_{GND1}
Power supply output side voltage	V_{VCC2}	9.6		32	V	V_{VCC2} - V_{VEE2}, 1EDR3140HQE
Power supply output side voltage	V_{VCC2}	14		32	V	V_{VCC2} - V_{VEE2}, 1EDR3144HQE
Power supply output side voltage	V_{VCC2}	16.45		32	V	V_{VCC2} - V_{VEE2}, 1EDR3146HQE
Power supply output side voltage	V_{VCC2}	16.45		32	V	V_{VCC2} - V_{VEE2}, 1EDR3147HQE
Positive power supply output side voltage	V_{VCC2}	14		32	V	V_{VCC2} - V_{GND2}, 1EDR3144HQE
Positive power supply output side voltage	V_{VCC2}	16.45		32	V	V_{VCC2} - V_{GND2}, 1EDR3146HQE
Negative power supply output side voltage	V_{VEE2}	-32		0	V	V_{VEE2} - V_{GND2}, valid only for 1EDR3144HQE and 1EDR3146HQE, V_{VCC2} - V_{GND2} > V_{UVLOH2} for the device to be operational
Logic input voltages (IN+, IN-)	V_{IN}	-0.3		5.5	V	
Ambient temperature	T_A	-40		125	°C	
Junction temperature	T_J	-40		150	°C	

3.3 Electrical characteristics

The electrical characteristics include the spread of values over supply voltages and temperatures within the recommended operating conditions. Electrical characteristics are valid in the -40°C < T_J < 125°C range. Typical values represent the median values measured at V_{VCC1} = 3.3 V, V_{VCC2} - V_{VEE2} = 15 V, and T_J = 25 °C. For 1EDR3144HQE and 1EDR3146HQE V_{VEE2} - V_{GND2} = 0 V. This is valid for all electrical characteristics unless otherwise specified.

3.3.1 Power supply

Table 7 **Power supply**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UVLO threshold input side (on)	V_{UVLOH1}		2.86	3.0	V	V_{VCC1} - V_{GND1}
UVLO threshold input side (off)	V_{UVLOL1}	2.5	2.66		V	V_{VCC1} - V_{GND1}
UVLO hysteresis input side	V_{HYS1}	0.1	0.2		V	V_{UVLOH1} - V_{UVLOL1}
Quiescent current input side	I_{Q1}			1.1	mA	IN+ = Low, IN- = Low
Quiescent current output side, ON state	$I_{Q2,ON}$			1.4	mA	IN+ = High, IN- = Low, , V_{VCC2} - V_{VEE2} = 15 V, V_{GND2} - V_{VEE2} = 0 V
Quiescent current output side, OFF state	$I_{Q2,OFF}$			1.1	mA	IN+ = Low, IN- = High, , V_{VCC2} - V_{VEE2} = 15 V, V_{GND2} - V_{VEE2} = 0 V
1EDR3140HQE						
UVLO threshold output side (on)	V_{UVLOH2}		9.3	9.6	V	V_{VCC2} - V_{VEE2}
UVLO threshold output side (off)	V_{UVLOL2}	8.25	8.55		V	V_{VCC2} - V_{VEE2}
UVLO hysteresis output side	V_{HYS2}		0.75		V	V_{UVLOH2} - V_{UVLOL2}
1EDR3144HQE						
UVLO threshold output side (on)	V_{UVLOH2}		13.6	14	V	V_{VCC2} - V_{GND2}
UVLO threshold output side (off)	V_{UVLOL2}	12.1	12.55		V	V_{VCC2} - V_{GND2}
UVLO hysteresis output side	V_{HYS2}		1.05		V	V_{UVLOH2} - V_{UVLOL2}
1EDR3146HQE						
UVLO threshold output side (on)	V_{UVLOH2}		16	16.45	V	V_{VCC2} - V_{GND2}
UVLO threshold output side (off)	V_{UVLOL2}	14.2	14.75		V	V_{VCC2} - V_{GND2}
UVLO hysteresis output side	V_{HYS2}		1.25		V	V_{UVLOH2} - V_{UVLOL2}
1EDR3147HQE						
UVLO threshold output side (on)	V_{UVLOH2}		16	16.45	V	V_{VCC2} - V_{VEE2}
UVLO threshold output side (off)	V_{UVLOL2}	14.2	14.75		V	V_{VCC2} - V_{VEE2}
UVLO hysteresis output side	V_{HYS2}		1.25		V	V_{UVLOH2} - V_{UVLOL2}

3.3.2 Logic input

Table 8 Logic input

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IN+, IN- low input threshold voltage	$V_{IN,L}$	1.0			V	
IN+, IN- high input threshold voltage	$V_{IN,H}$			2.5	V	
IN+, IN- low/high hysteresis	$V_{IN,HYS}$	0.5	0.8		V	
IN+, IN- input current	I_{IN}			100	µA	V_{VCC1} = 5 V, V_{IN} <= V_{VCC1}
IN+ pull down resistor	$R_{IN,PD}$		75		kΩ	
IN- pull up resistor	$R_{IN,PU}$		75		kΩ	

3.3.3 Gate driver

Table 9 Gate driver

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High level output peak current	I_{OUTH}	3.5	6		A	[1] V_{VCC2} - V_{VEE2} = 15 V, IN+ = High, IN- = Low, C_L = 100 nF
High level output on resistance	$R_{DSON,H}$	0.3	0.9	2.1	Ω	I_{OUTH} = 0.1 A
Low level output peak current	I_{OUTL}	3.5	6.5		A	[1] V_{VCC2} - V_{VEE2} = 15 V, IN+ = Low, IN- = High, C_L = 100 nF
Low level output on resistance	$R_{DSON,L}$	0.2	0.5	1.1	Ω	I_{OUTL} = 0.1 A
Clamp voltage between OUTH and VCC2	V_{CLP_OUTH}			1.0	V	V_{OUTH} - V_{VCC2}, I_{OUTH} = -500 mA, IN+ = High, IN- = Low
Clamp voltage between VEE2 and OUTL	V_{CLP_OUTL}			1.0	V	V_{VEE2}-V_{OUTL}, I_{OUTL} = -500 mA, IN+ = Low, IN- = High

1) Parameter is not subject to production test - verified by design/characterization

3.3.4 Dynamic characteristics

Table 10 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input to output propagation delay ON	t_{PDON}	33	40	50	ns	V_{VCC2} - V_{VEE2} = 15 V, C_L = 100 pF, valid for 1EDR3140
Input to output propagation delay ON	t_{PDON}	33	40	50	ns	V_{VCC2} - V_{VEE2} = 18 V, C_L = 100 pF, valid for 1EDR3144, 1EDR3146 and 1EDR3147
Input to output propagation delay OFF	t_{PDOFF}	33	40	50	ns	V_{VCC2} - V_{VEE2} = 15 V, C_L = 100 pF, valid for 1EDR3140

(table continues...)

Table 10 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input to output propagation delay OFF	t_{PDOFF}	33	40	50	ns	V_{VCC2} - V_{VEE2} = 18 V, C_L = 100 pF, valid for 1EDR3144, 1EDR3146 and 1EDR3147
Input to output propagation delay distortion IN+	$\lvert t_{PDISTO,IN+} \rvert$		0	3	ns	1) $\lvert t_{PDOFF} - t_{PDON} \rvert$
Input to output propagation delay distortion IN-	$\lvert t_{PDISTO,IN-} \rvert$		0	5	ns	1) $\lvert t_{PDOFF} - t_{PDON} \rvert$
Input to output, part to part skew	t_{SKEW}			7	ns	1) 2) C_L = 100 pF, valid for same input pin and edge
Input to output, part to part skew plus	t_{SKEW+}		0	8	ns	1) C_L = 100 pF, valid for opposite output edge and any input combination
Input pulse suppression time (filter time)	t_{INFLT}	15			ns	
Minimum input pulse width	$t_{IN,min}$	30			ns	
Rise time	t_{RISE}			20	ns	V_{VCC2} - V_{VEE2} = 15 V, C_L = 1 nF, valid only for 1EDR3140
Rise time	t_{RISE}			20	ns	V_{VCC2} - V_{VEE2} = 18 V, C_L = 1 nF, valid for 1EDR3144, 1EDR3146 and 1EDR3147
Fall time	t_{FALL}			20	ns	V_{VCC2} - V_{VEE2} = 15 V, C_L = 1 nF, valid for 1EDR3140
Fall time	t_{FALL}			20	ns	V_{VCC2} - V_{VEE2} = 18 V, C_L = 1 nF, valid for 1EDR3144, 1EDR3146 and 1EDR3147
Input-side start-up time	$t_{START,VCC1}$		2.5	10	µs	3) IN+ = High, IN- = Low, V_{VCC2} > V_{UVLOH2}, C_L = 100pF
Input-side deactivation time	$t_{STOP,VCC1}$		2.5	10	µs	3) IN+ = High, IN- = Low, V_{VCC2} > V_{UVLOH2}, C_L = 100pF
Output-side start-up time	$t_{START,VCC2}$		5	10	µs	3) IN+ = High, IN- = Low, V_{VCC1} > V_{UVLOH1}, C_L = 100 pF
Output-side deactivation time	$t_{STOP,VCC2}$	0.5		1.5	µs	3) IN+ = High, IN- = Low, V_{VCC1} > V_{UVLOH1}, C_L = 100 pF
Static common-mode transient immunity	$\lvert CMTI_{Static} \rvert$	300			kV/µs	3) 4) V_{CM} = 1500 V; V_{OUT} = V_{VEE2} or V_{OUT} = V_{VCC2}

1) value at same ambient temperature and operating conditions.
2) this parameter was previously called input to output, part to part propagation delay variation
3) Parameter is not subject to production test - verified by design/characterization
4) Output pin states are generated by connecting the IN+/- pins to either VCC1 or GND1.

3.3.5 Active shut down

Table 11 **Active shut down**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Active shut down voltage	V_{ACTSD}			1.8	V	$V_{OUT/OUTL}$ - V_{VEE2}, $I_{OUT/OUTL}$ = 500 mA, *VCC2* open

3.3.6 Overtemperature protection

Table 12 **Overtemperature protection**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overtemperature protection temperature	T_{OTPOFF}	150	165	175	°C	1)
Overtemperature protection hysteresis	T_{OTPHYS}		10		°C	1)

1) Parameter is not subject to production test - verified by design/characterization

4 Insulation characteristics (IEC 60747-17, UL 1577) for LDSO-8-1 300 mil package

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 13 **Insulation specification for LDSO-8-1 300 mil package**

Description	Symbol	Characteristic	Unit
Safety limiting values			
Maximum ambient safety temperature	T_S	150	°C
Maximum input-side power dissipation at $T_A = 25°C$[1]	P_{SI}	100	mW
Maximum output-side power dissipation at $T_A = 25°C$[2]	P_{SO}	1000	mW
General			
External clearance	CLR	> 8	mm
External creepage	CPG	> 8	mm
Comparative tracking index	CTI	> 600	–
Isolation capacitance	C_{IO}	0.9	pF
Overvoltage category according to IEC 60664-1, Table F.1			–
for rated mains voltage ≤ 150 V (rms)		I-IV	
for rated mains voltage ≤ 300 V (rms)		I-IV	
for rated mains voltage ≤ 600 V (rms)		I-IV	
for rated mains voltage ≤1000 V (rms)		I-III	
Reinforced insulation according to IEC 60747-17 (planned)			
Climatic classification		40/125/21	–
Pollution degree (IEC 60664-1)		2	–
Apparent charge, method a $V_{pd(ini),a} = V_{IOTM}$, $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_{ini} = 1$ min, $t_m = 10$ s	q_{pd}	< 5	pC
Apparent charge, method b $V_{pd(ini),b} = V_{IOTM} \times 1.2$, $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_{ini} = 1$ s, $t_m = 1$ s	q_{pd}	< 5	pC
Isolation resistance at $T_{A,max}$; $V_{IO} = 500\ V_{DC}$, $T_A = 125°C$	R_{IO}	$> 10^{11}$	Ω
Isolation resistance at T_S; $V_{IO} = 500\ V_{DC}$, $T_S = 150°C$	R_{IO_S}	$> 10^9$	Ω
Maximum rated transient isolation voltage	V_{IOTM}	8000	V (peak)
Maximum repetitive isolation voltage	V_{IORM}	1767	V (peak)
Maximum working isolation voltage	V_{IOWM}	1250	V (rms)
		1767	V (DC)
Impulse voltage	V_{IMP}	8000	V (peak)
Maximum surge isolation voltage for reinforced isolation; $V_{TEST} \geq V_{IMP} \times 1.3$	V_{IOSM}	11000	V (peak)
Recognized under UL 1577			
Insulation withstand voltage (60 s)	V_{ISO}	5700	V (rms)
Insulation test voltage (1 s)	$V_{ISO,TEST}$	6840	V (rms)

1) IC input-side power dissipation is derated linearly at 2 mW/°C above 159 °C
2) IC output-side power dissipation is derated linearly at 8 mW/°C above 65 °C

5 Typical characteristics

Unless otherwise noted,the measurements are done with V_{VCC1} = 3.3 V and V_{VCC2} = 15 V, 100 nF capacitor connected between *VCC1* and *GND1*, 4.7 µF capacitor between *VCC2* and *VEE2*.

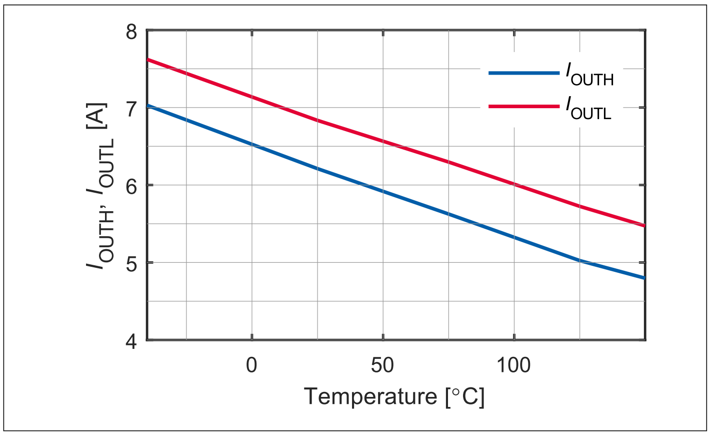


Figure 8 High level output peak current vs. temperature

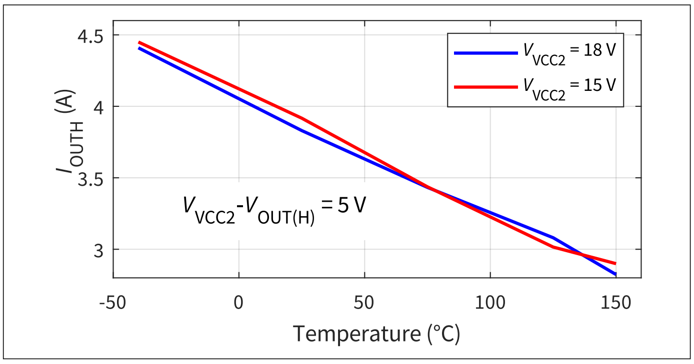


Figure 9 High level output current with V_{VCC2} - V_{OUTH} = 5 V vs. temperature

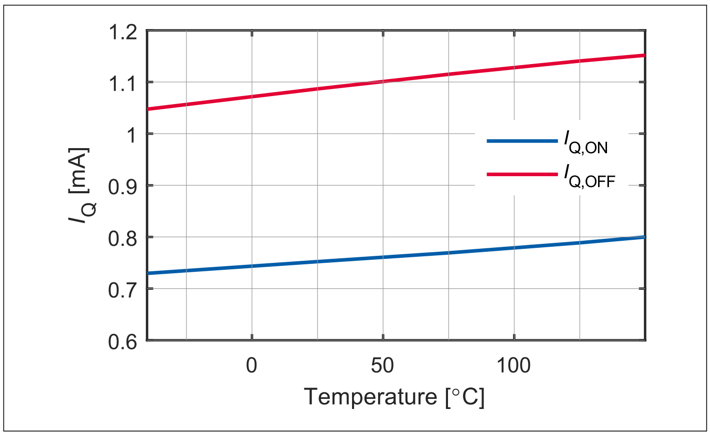


Figure 10 Low level output peak current vs. temperature

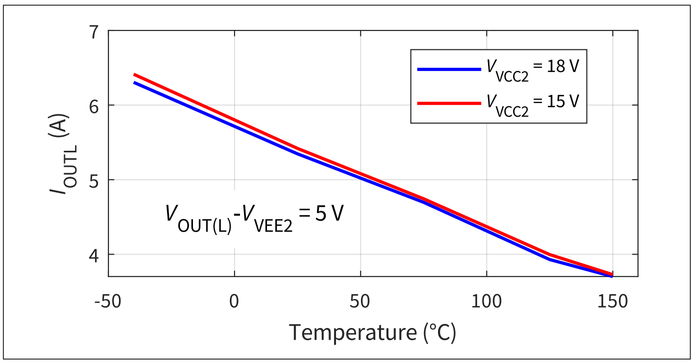


Figure 11 Low level output current with V_{OUTL} - V_{VEE2} = 5 V vs. temperature

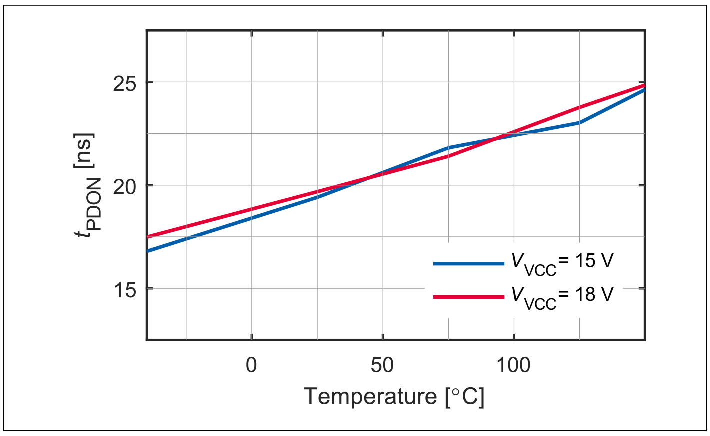


Figure 12 I_{Q1} supply current vs. temperature

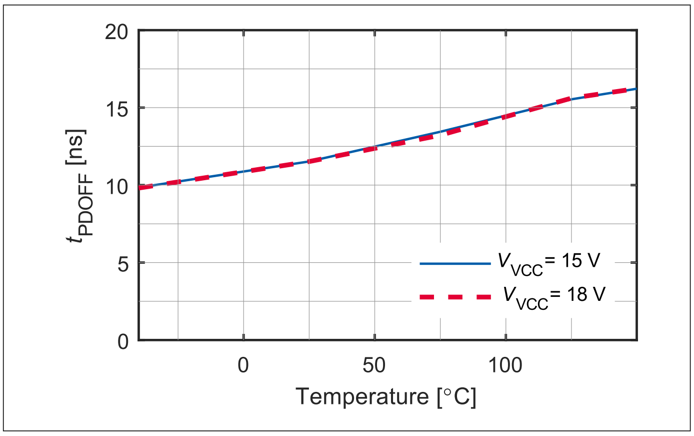


Figure 13 I_{Q1} supply current vs. temperature

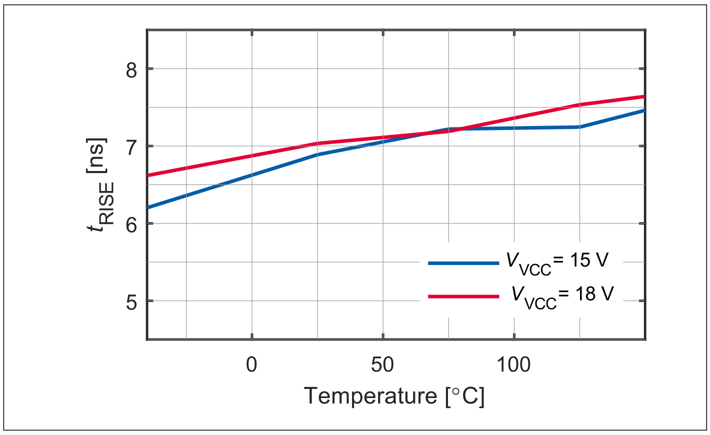


Figure 14 I_{Q1} supply current vs. input frequency

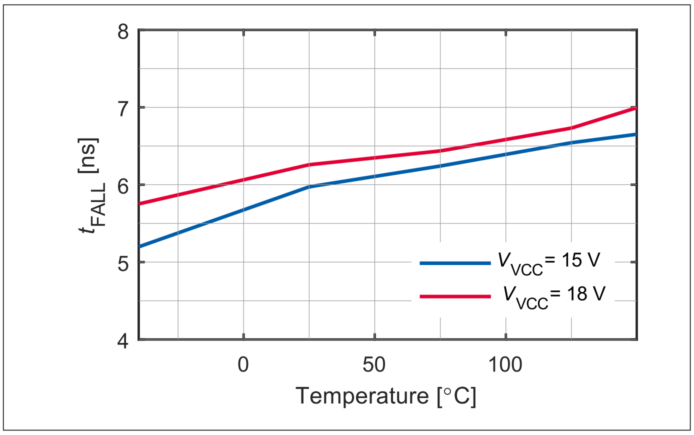


Figure 15 I_{Q2} supply current vs. temperature

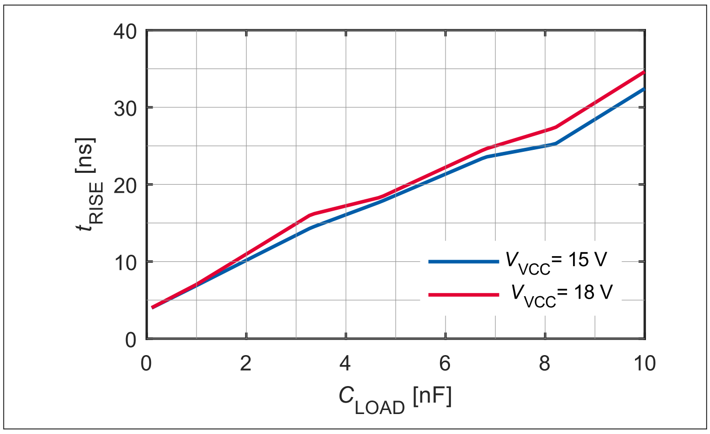


Figure 16 I_{Q2} supply current vs. temperature

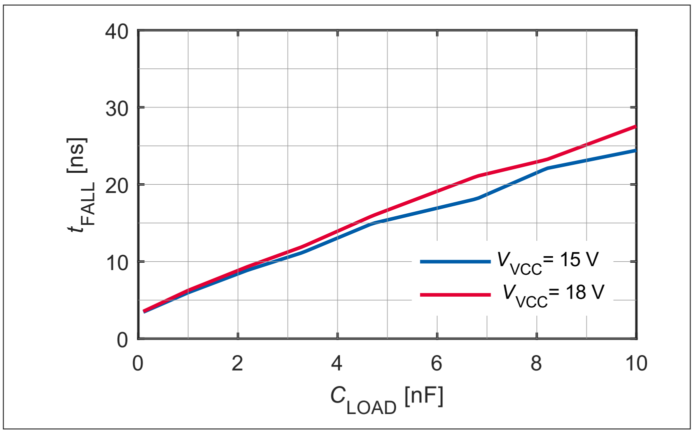


Figure 17 I_{Q2} supply current vs. input frequency

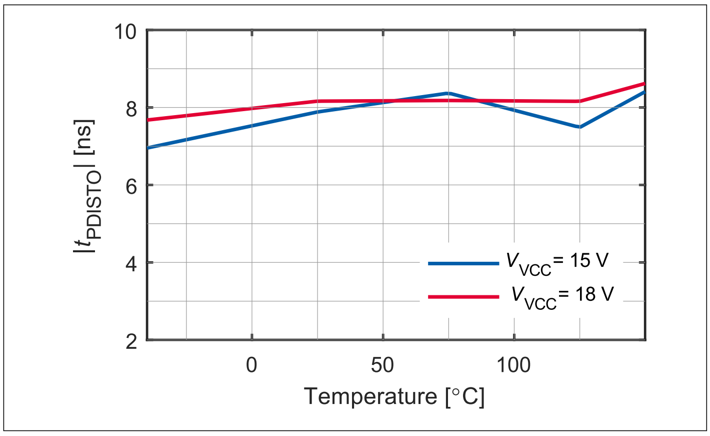


Figure 18 Rise time t_{RISE} vs. temperature

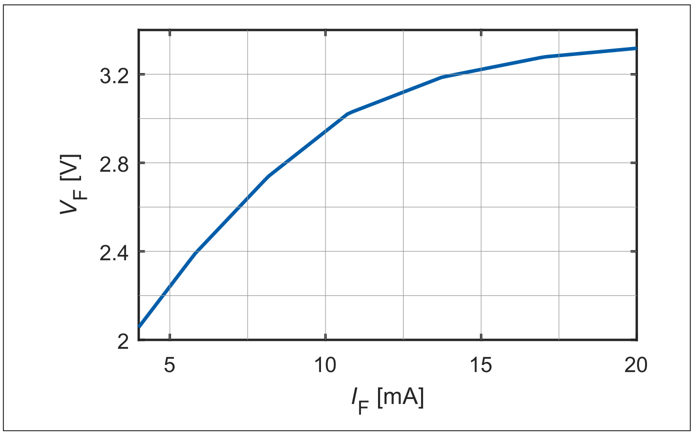
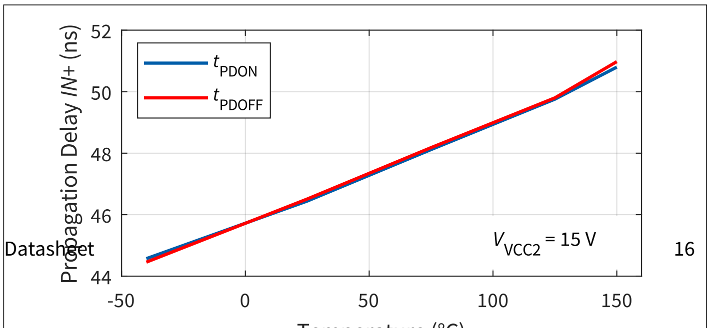
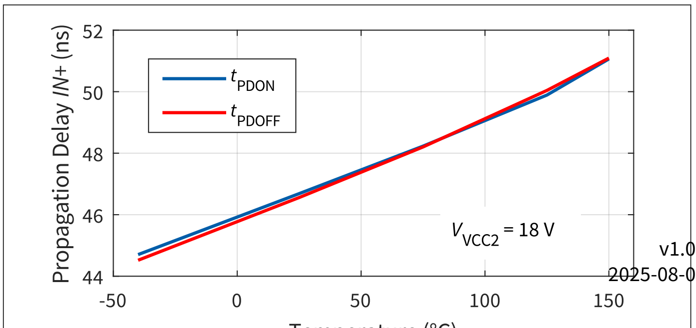


Figure 19 Fall time t_{FALL} vs. temperature





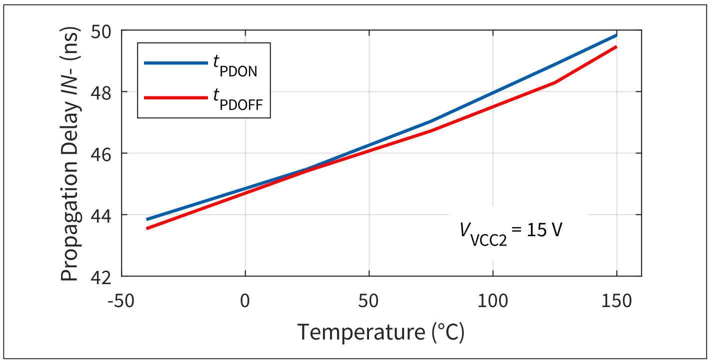


Figure 22 Propagation delay for *IN-* vs. temperature (V_{VCC2} = 15 V)

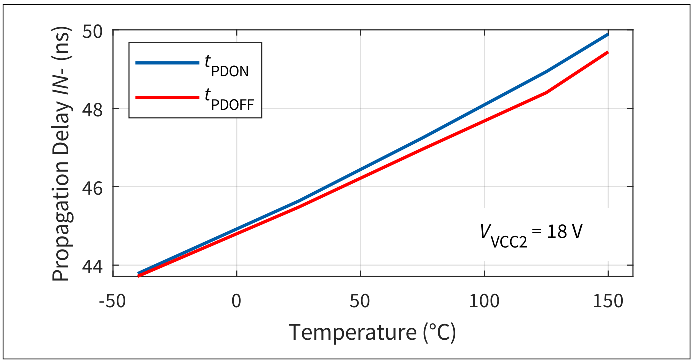


Figure 23 Propagation delay for *IN-* vs. temperature (V_{VCC2} = 18 V)

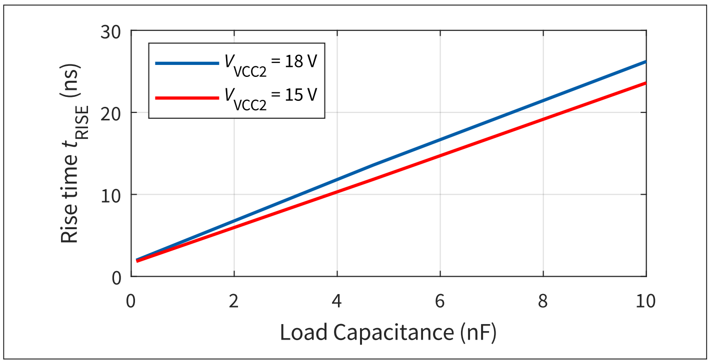


Figure 24 Rise time t_{RISE} vs. load capacitance

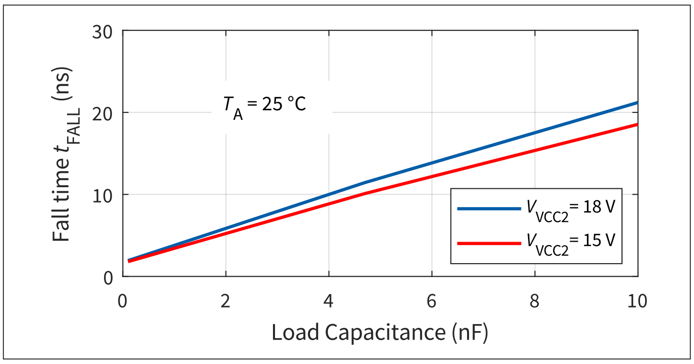


Figure 25 Fall time t_{FALL} vs. load capacitance

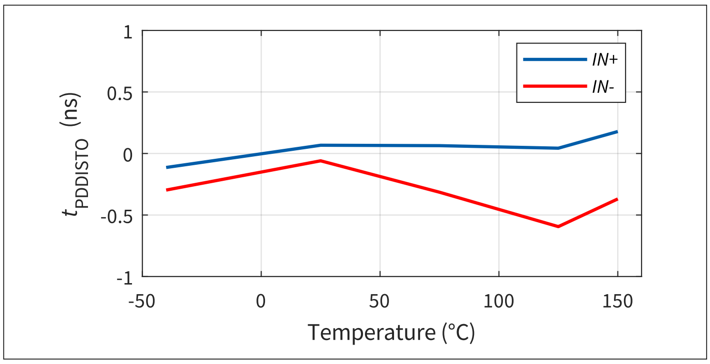


Figure 26 Propagation delay distortion t_{PDISTO} vs. temperature

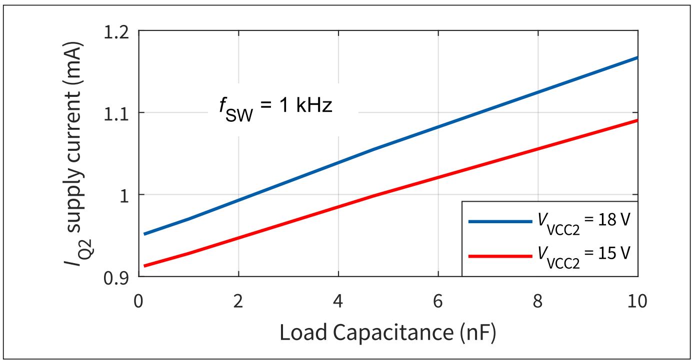


Figure 27 I_{Q2} supply current vs. load capacitance

6 Parameter measurement

6.1 CMTI measurement setup

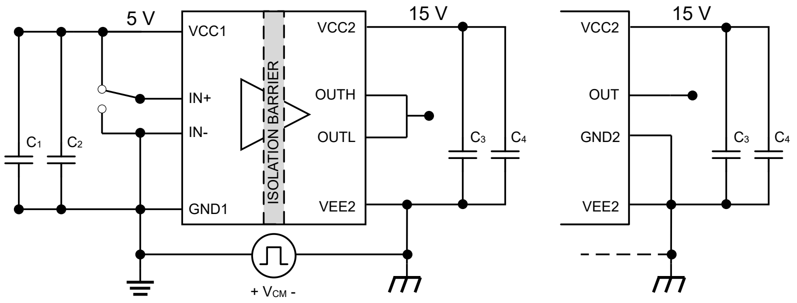


Figure 28 **CMTI test circuits for all the variants**

Figure 28 shows CMTI test setup for the common mode transient immunity measurements.

6.2 Undervoltage lockout (UVLO)

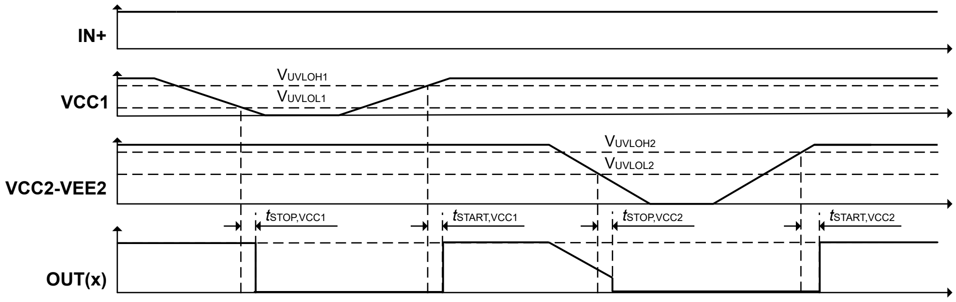


Figure 29 **UVLO behavior of variants with separate source and sink pins**

To ensure correct switching of IGBTs, Si and SiC MOSFETs, the device is equipped with an independent undervoltage lockout for both input and output side. Operation starts only after both supply voltage levels have increased beyond the respective V_{UVLOH} levels.

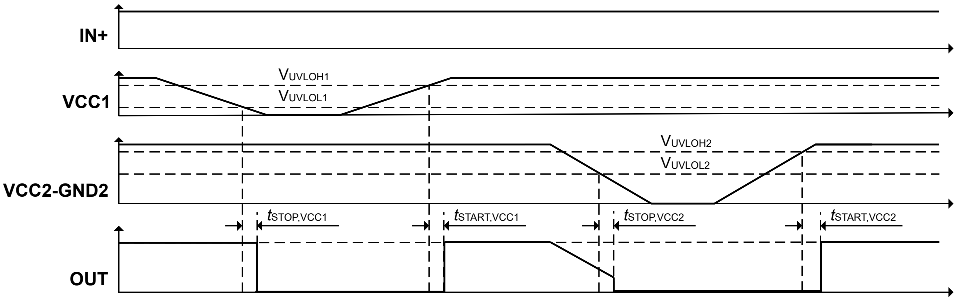


Figure 30 **UVLO behavior of variants with GND2 pin**

If the power supply voltage, V_{VCC1}, of the input chip drops below V_{UVLOL1}, a turn-off signal is sent to the output chip before power-down. The IGBT, Si or SiC MOSFET is switched off and the signals at *IN+* and *IN-* are ignored until V_{VCC1} reaches the power-up voltage, V_{UVLOH1}, again.

If the power supply voltage, V_{VCC2}, of the output chip goes down below V_{UVLOL2}, the IGBT, Si or SiC MOSFET is switched off and signals from the input chip are ignored until V_{VCC2} reaches the power-up voltage, V_{UVLOH2}, again.

6.3 Propagation delay, rise and fall time

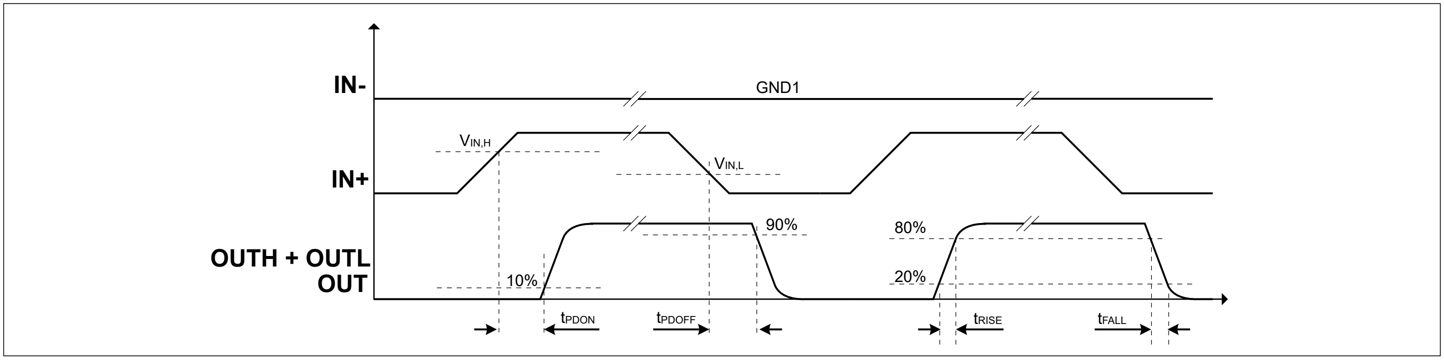


Figure 31 **Propagation delay, rise time and fall time using the non-inverting input**

Figure 31 and Figure 32 show the propagation delays t_{PDON} and t_{PDOFF} for the non-inverting input *IN+* and the inverting input *IN-* including the rise time, t_{RISE}, and fall time, t_{FALL}, diagrams.

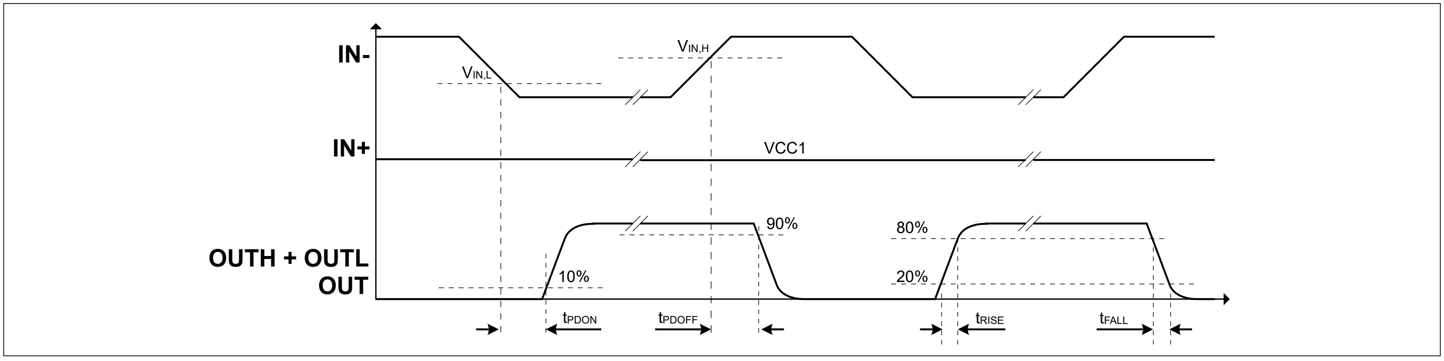


Figure 32 **Propagation delay, rise time and fall time using the inverting input**

Figure 33 and Figure 34 show the input to output, part to part skew, t_{SKEW} measurement with the non-inverting and inverting inputs. This parameter highlights the part to part variation in propagation delay and is relevant when paralleling gate drivers. The parameter is always assuming the same conditions (temperature and supply voltages) between the parts.

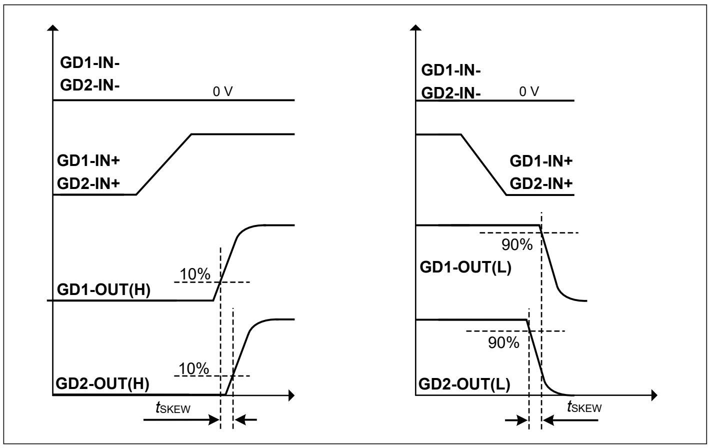


Figure 33 **Input to output, part to part skew using non-inverting input**

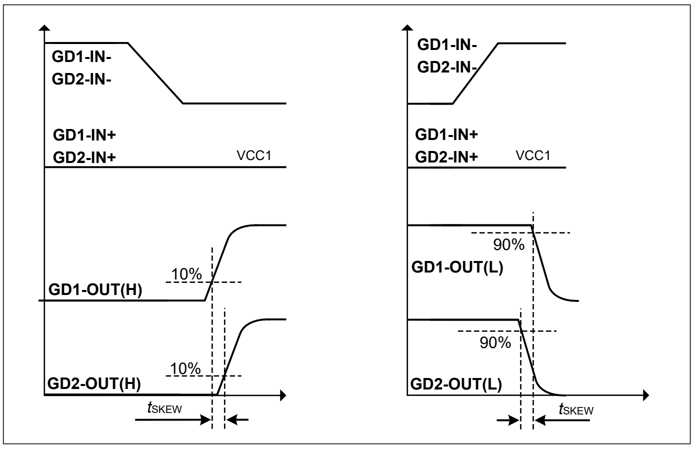


Figure 34 **Input to output, part to part skew using the inverting input**

Figure 35, Figure 36, Figure 37 and Figure 38 show the Skew plus (t_{SKEW+}) using the non-inverting or inverting inputs on the input side under all the possible combinations. The Skew plus parameter is valid at the same temperature and supply voltages. The parameter describes the variation between the turn-on and turn-off propagation delays in a half-bridge, under the previously mentioned conditions and defines the minimum dead time required from the gate driver perspective. This is relevant when driving the gate drivers with complimentary pulses, such as in a half-bridge.

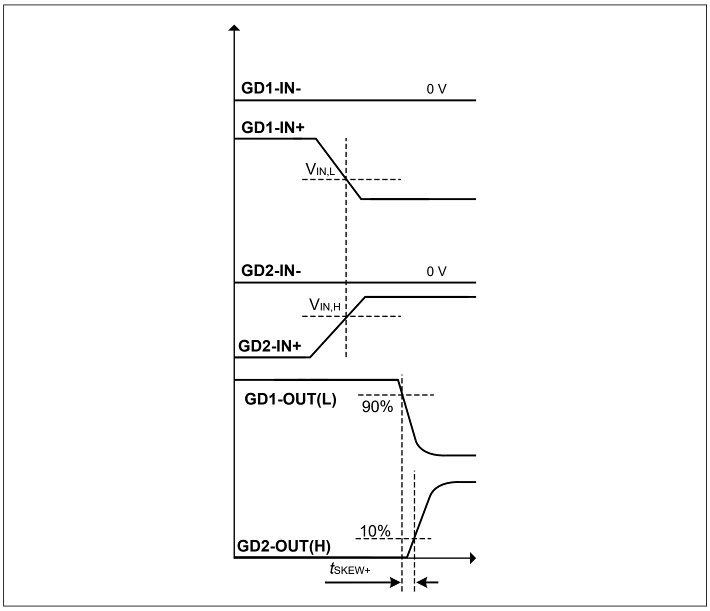


Figure 35 Skew plus using the non-inverting inputs

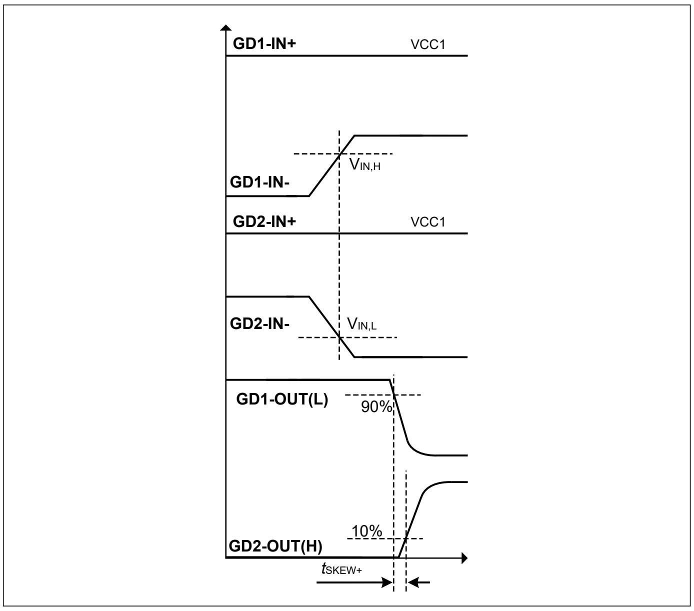


Figure 36 Skew plus using the inverting inputs

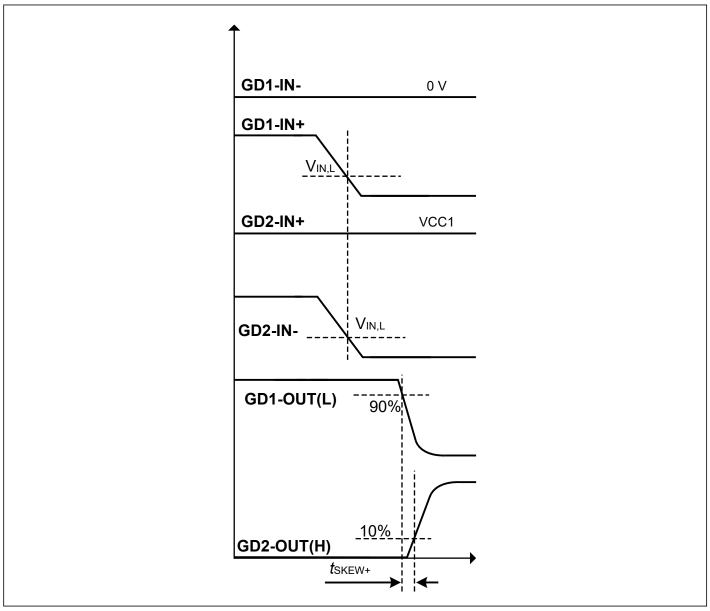


Figure 37 Skew plus using the inverting and non-inverting inputs with falling edges

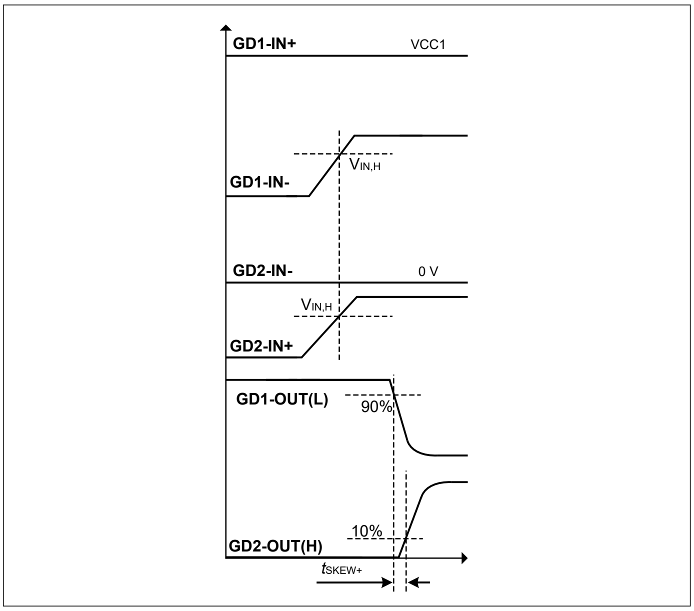


Figure 38 Skew plus using the inverting and non-inverting inputs with rising edges

7 Functional description

7.1 Input features

The input side of the gate driver has two inputs, *IN+* and *IN-*, for the control signals and two power terminals, *VCC1* and *GND1*, for the input chip supply.

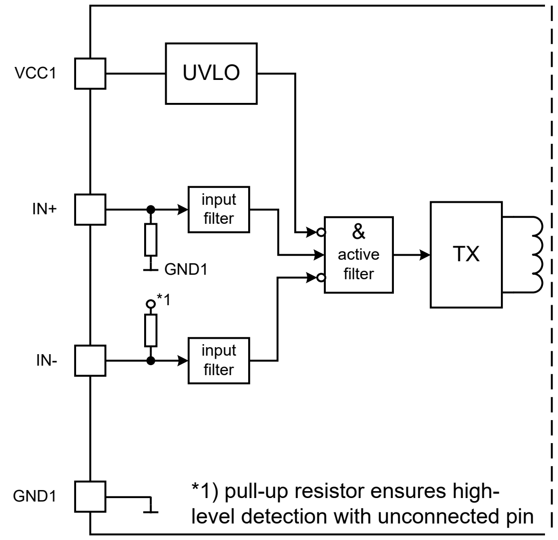


Figure 39 Block diagram of the input section

The gate driver IC input section consists of the following functional blocks:

- Input undervoltage lockout circuit
- Signal filtering
- Pull-up resistor for inverting input
- Pull-down resistor for non-inverting input
- Signal transmission to isolated output section

7.1.1 Input supply and undervoltage lockout (UVLO)

The input supply range has absolute maximum ratings of -0.3 V to 17 V. Static operation beyond the absolute maximum voltage (abs max) damages the internal structures and is, therefore, forbidden.

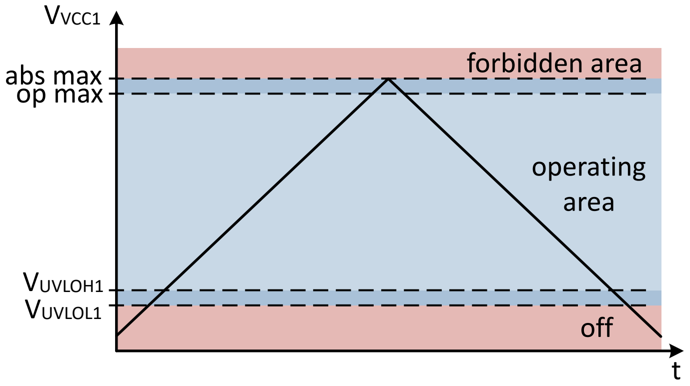


Figure 40 Input supply and UVLO threshold

At a crossing of the turn-on undervoltage lockout threshold, (V_{UVLOH1}), during a positive ramp at *VCC1* pin, the input section starts to operate. It evaluates the input signals *IN+* and *IN-* and transmits their current state to the output section. During V_{VCC1} ramp down and crossing of the turn-off undervoltage lockout threshold, (V_{UVLOL1}), the input section sends a final off signal regardless of the *IN+* or *IN-* state. The hysteresis between the thresholds V_{UVLOL1} and V_{UVLOH1} ensures a stable operation when the supply voltage is close to the threshold levels.

Any voltage overshoot above the absolute maximum voltage (abs max) rating can damage the driver circuits. In this area, the current consumption increases dramatically and results in a violation of the maximum allowed input power dissipation. The operating area is defined between the turn-on undervoltage lockout threshold, (V_{UVLOH1}), and the maximum recommended operating voltage.

7.1.2 Pull-up and pull-down resistors for the input pins

The input pull-up or pull-down resistors ensure an OFF-state in case the corresponding input is not connected. These resistors have a typical value of 75 kΩ. Even with the maximum allowed voltage at the *VCC1* pin, the input current due to these resistors stays below 1 mA.

The pull-up and pull-down resistors are designed to be connected to an external supply or ground potential to permanently activate the individual driver input.

7.1.3 Input signal filtering (deglitch filter)

The input section of the driver IC filters both the input signals to suppress the short pulses triggered by external influences.

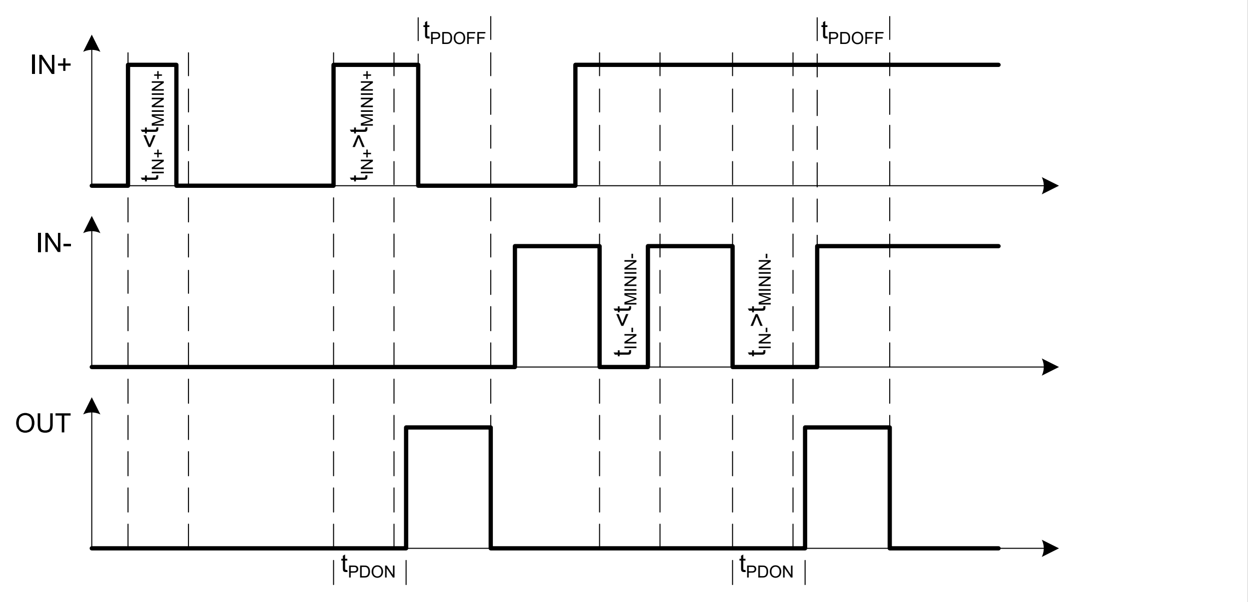


Figure 41 Input pulse suppression and turn-on/turn-off propagation delay

Every pulse at *IN+* or *IN-*, shorter than the input pulse suppression time, t_{INFLT}, will be filtered and will not be transmitted to the output chip. Longer pulses will be sent to the output with the shown propagation delay, t_{PDON} and t_{PDOFF}. This helps the design and an external RC filter for noise suppression will not be needed in most cases.

7.2 Output features

This section describes the output section of the gate drivers. The output features of the gate driver IC include undervoltage lockout for the output supply, shoot-through protection circuitry for the internal output stage and the active shutdown circuitry.

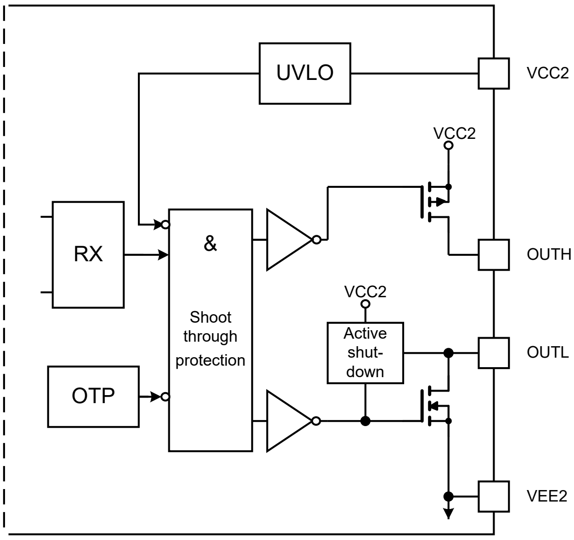


Figure 42 **Block diagram of the output section for variants with separate source and sink pins**

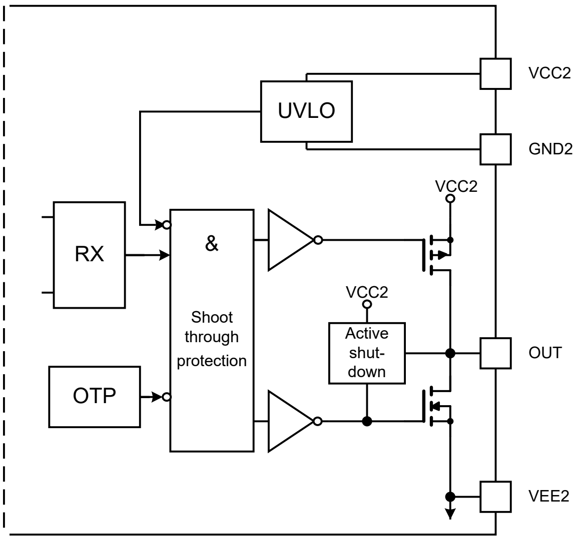


Figure 43 **Block diagram of the output section for variants with GND2 pin**

The output section of the gate driver ICs consists of the following functional blocks:

- Output undervoltage lockout circuit referenced to *VEE2* (1EDR3140HQE and 1EDR3147HQE) or *GND2* (1EDR3144HQE and 1EDR3146HQE)
- Isolated signal receiver from the input section
- Sourcing and sinking output stage
- Active shutdown circuitry
- Overtemperature protection

7.2.1 Driver outputs and supply

The output driver section uses MOSFETs to provide a rail-to-rail output as shown in Figure 42 and Figure 43. This feature allows a tight control of the gate voltage during ON-state and short circuit to be maintained as long as the driver's supply voltage is stable. Due to the low internal voltage drop, switching behavior of the IGBT, Si and SiC MOSFETs is predominantly governed by the gate resistor for as long as the current rating of the gate driver is not exceeded. Furthermore, it reduces the power to be dissipated by the driver as most of the energy is dissipated in the gate resistor.

The current sourcing stage of the gate driver ICs is designed with a PMOS-only MOSFET. The PMOS delivers a strong current, at the beginning of the turn-on process and then sustains a high gate current until the gate reaches *VCC2* rail voltage, ensuring a fast turn-on of the IGBT, Si and SiC MOSFETs. The current sinking stage consists of an NMOS.

7.2.2 Output undervoltage lockout (UVLO)

The output supply range has a positive absolute maximum rating of 35 V for all variants. The gate driver ICs are therefore capable of providing a bipolar gate voltage to a connected power switch.

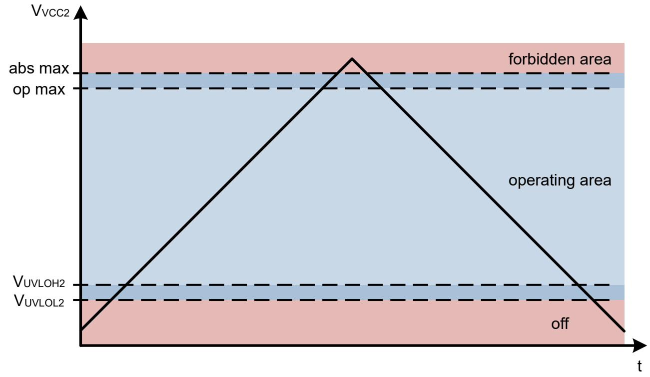


Figure 44 **Output supply and UVLO threshold**

The UVLO feature protects the power switch by preventing the operation when the output supply voltage, V_{VCC2}, is too low. During the positive ramp of the output supply voltage, V_{VCC2}, once the voltage is higher than the UVLO threshold (V_{UVLOH2}), the output stage starts operating by switching the output pins on and off depending on the signals received from the input side of the gate driver. During V_{VCC2} ramp down, once the voltage is lower than the turn-off UVLO threshold, (V_{UVLOL2}), the output section initiates a turn-off command regardless of the signals received from the input section. The hysteresis between the thresholds V_{UVLOL2} and V_{UVLOH2} ensures a stable operation when the supply voltage is close to the threshold levels.

For the variants with separate outputs, the output supply voltage, V_{VCC2}, is measured against the voltage, V_{VEE2}. Therefore, for these variants, the output UVLO monitors the complete rail-to-rail supply voltage. Alternatively, for the variants with *GND2* pin, the V_{VCC2} is measured against the ground pin *GND2*. Hence, for these variants, the UVLO monitors only the positive supply voltage when a bipolar supply voltage is used on the output side and the gate driver prevents the *OUT* pin from turning on when the positive supply voltage is too low. As a result, in applications where bipolar supply voltage is used, the variants with *GND2* pin offer a more effective UVLO protection to the IGBTs and SiC MOSFETs.

7.2.3 Overtemperature protection

Overtemperature protection shuts down the output of the gate driver IC and protects the application from destructive failure when the junction temperature of the IC exceeds the threshold temperature, T_{OTPOFF}. However, it is important to note that this protection activation threshold and the release threshold exceed the absolute maximum junction temperature, T_J, of the IC. Therefore, overtemperature protection does not prevent the damage of the gate driver IC, in case the absolute maximum junction temperature is exceeded.

7.2.4 Active shutdown

The active shutdown function is a protection feature of the driver. It is designed to prevent the free-floating gate of a connected power switch from triggering a turn on.

The active shut down feature ensures a safe IGBT, Si and SiC MOSFET OFF-state in case the output chip is not connected to the power supply or an undervoltage lockout is in effect. The IGBT, Si and SiC MOSFET gate is clamped via the *OUT(L)* pin to *VEE2* .

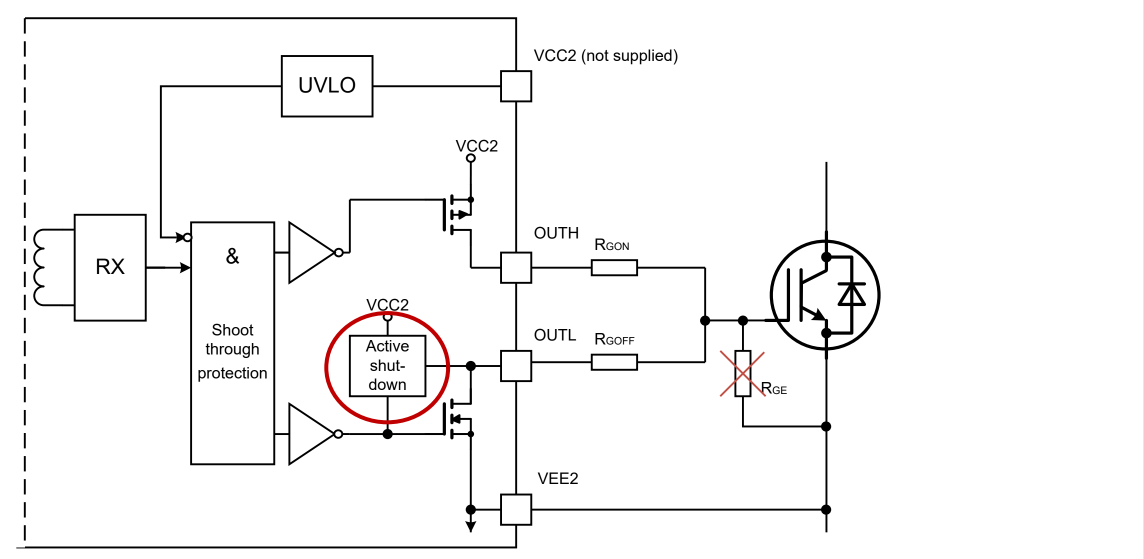


Figure 45 **Block diagram showing active shut down for the variants with separate source and sink pins**

In case of a missing or collapsing power supply at the *VCC2* pin, the output section of the driver operates in the active shutdown mode. In this case, the driver uses the floating voltage of the connected gate to supply this internal circuit. This solution is much stronger than using an external gate to emitter resistor, R_{GE}. At the same time, in the case of fast dV/dt events on the switch that could generate Miller current which can bias the gate, even when the gate driver is not powered on, the active shutdown circuit will use the voltage to power itself and actively pull the gate low. The active shut down feature functions in a similar manner across all the variants.

7.2.5 Short circuit clamping

During short circuit, the gate voltage of the power transistor tends to rise because of the feedback via the Miller capacitance. In this situation, the IC internally clamps the voltage on the *OUT(H)* pin and limits the voltage to a value slightly higher than the supply voltage, V_{VCC2}. A maximum current of 500 mA may be fed back to the supply through this path for 10 µs. If higher currents are expected or tighter clamping is desired, external Schottky diodes should be added between the *OUT(H)* and *VCC2* pins.

8 Application information

Note: Infineon is providing this information as a courtesy only and without acknowledging any legal obligation. Information in the following application chapters is not part of the Infineon component specification, and Infineon does not warrant its accuracy or completeness. Infineon's customers are responsible for determining the suitability of the components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Typical application

This section describes how the gate drivers can be used in an application.

Figure 46 and Figure 47 show a typical application for gate drivers with separated outputs for current sourcing and sinking. For these variants, individual gate resistors can be used for turning a power switch on and off. By having separate sourcing pin, *OUTH*, and sinking pin, *OUTL*, the bill of materials (BOM) can be optimized, saving a bypass Schottky diode for each power switch used.

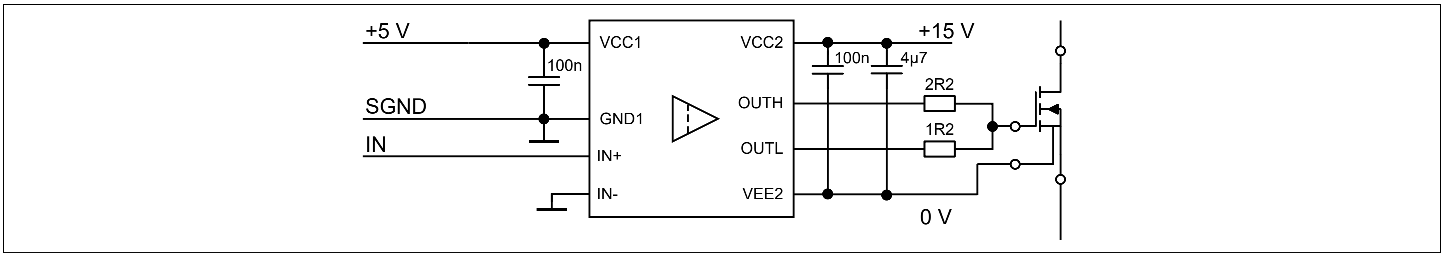


Figure 46 **Circuit example for variants with separate source and sink pins using unipolar power supply driving SiC MOSFET**

When driving the switch with unipolar power supply voltages, the *VEE2* pin should be connected directly to the source or emitter of the power transistor as shown in Figure 46 .

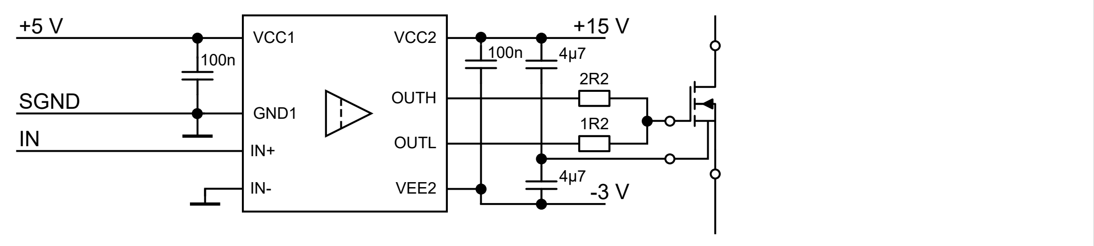


Figure 47 **Circuit example for variants with separate source and sink pins bipolar power supply driving SiC MOSFET**

When driving the switch with bipolar power supply voltages, a virtual ground should be created between the two capacitors connected to the *VCC2* and *VEE2* pins. This virtual ground should then be connected to the source or emitter of the power transistor as shown in Figure 47.

Figure 48 and Figure 49 depict the typical application circuit for the gate drivers with *GND2* pin. For the variants with *GND2* pin, the sourcing and sinking stages of the output are connected internally and the sourcing and sinking gate currents are provided by the *OUT* pin. In case different gate resistances are required for turning the power switch on and off, a separate bypass diode of Schottky type can be used on the sinking path.

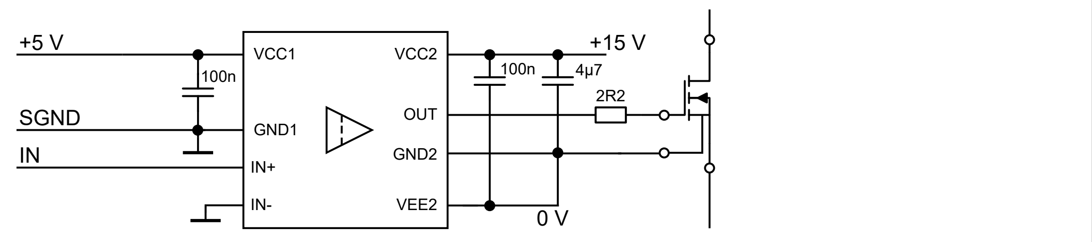


Figure 48 Circuit example for variants with *GND2* pin using unipolar power supply driving SiC MOSFET

When driving the switch with unipolar power supply voltages, the *GND2* pin should be connected directly to the source or emitter of the power transistor as shown in Figure 48. Furthermore, the *VEE2* pin should be connected to the *GND2* pin.

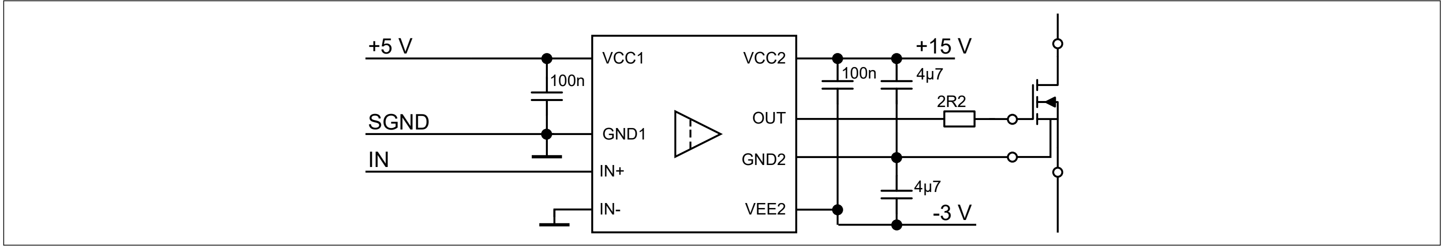


Figure 49 Circuit example for variants with *GND2* pin using bipolar bipolar power supply driving SiC MOSFET

When driving the switch with bipolar power supplies, the *GND2* pin should be connected to the source or emitter of the power transistor as shown in Figure 49.

8.2 Power supply recommendations

The 1EDR314xHQE gate drivers support a wide range of voltages on the input and output side. These devices can operate with unipolar as well as bipolar power supply voltages on the output side for reliable and safe operation in the application.

To ensure that the gate driver operates correctly, it is necessary to place appropriate decoupling capacitors on the power supply pins. On the input side, placing a low ESR, surface mount, multilayer ceramic capacitor of 100 nF between the *VCC1* pin and *GND1* pin is recommended. This capacitor should be placed as close as possible to the pins.

The decoupling capacitors on the output side, in addition to decoupling any disturbance on the power supply, also store the energy necessary to deliver the gate currents required for turning on and off the power transistor. Therefore, these capacitors should be dimensioned appropriately to limit the voltage drop during the power transistor turn-on and turn-off process. When using a unipolar power supply, a low ESR, surface mount, multilayer ceramic capacitor of at least 4.7 µF should be placed between the *VCC2* pin and the *VEE2* pin, in close proximity of the pins. In case of bipolar power supply, using at least 4.7 µF ceramic capacitor between *VCC2* and virtual ground (source or emitter potential of power transistor) or, if applicable *GND2* pin is recommended. Similarly, using a 4.7 µF capacitor between *VEE2* pin and virtual ground or *GND2* pin is recommended. Depending on the gate charge of the power transistor and the peak source and sink gate currents, a higher capacitance may be necessary to limit the voltage drop during power transistor turn-on and turn-off. Finally, a 100 nF decoupling capacitor is recommended between *VCC2* and *VEE2* pins to ensure a short path between them to decouple any high frequency noise.

When selecting the capacitors, it is important to consider the capacitance drop of ceramic capacitors with respect to the applied DC voltage.

8.3 Usage of IN+ and in-

The inverting, *IN-*, and non-inverting, *IN+*, input pins offer multiple possibilities to connect the PWM input and logic signals for various control and protection uses.

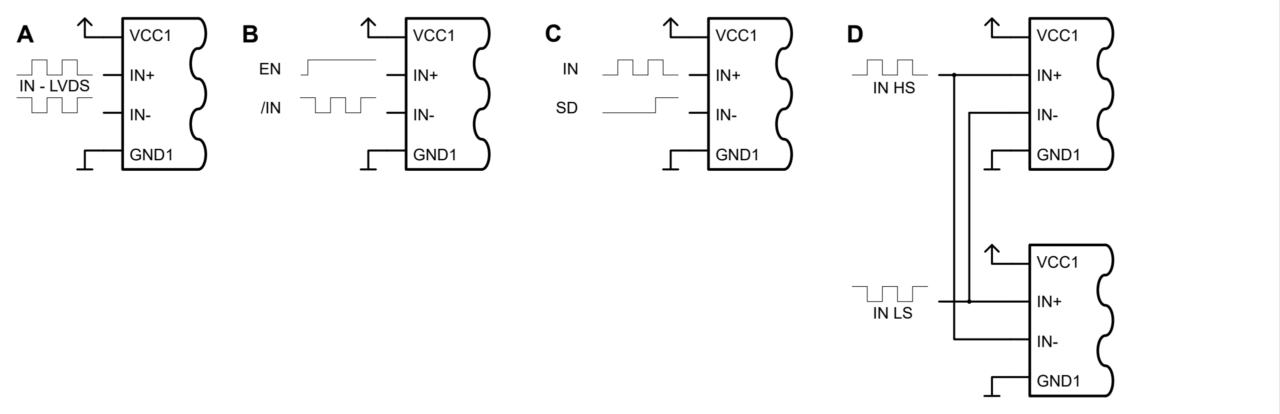


Figure 50 Input ***IN+*** and ***IN-*** usage

Apart from using both inputs with a differential signal (A) (*VCC1* and *GND1* levels), using only one input signal for actual switch control leaves the second input available for functions such as Enable (B), Shutdown (C), or Interlock (D).

A) Differential signal

Applying a logic-level differential signal on both *IN+* and *IN-* with the positive level of *VCC1* pin and the negative level of *GND1* pin improves common-mode noise rejection. However, it is important to note that the input pins *IN+* and *IN-* are not truly differential in nature and the signals on these pins are referenced against the input ground, *GND1*.

B) Enable

Using the *IN+* pin as enable signal leaves the *IN-* to control the output PWM with an inverted logic input signal. The enable signal can then be shared between the gate driver ICs of a complete inverter to start operation with a single control signal.

C) Shutdown

Using the *IN-* pin as shutdown signal leaves the *IN+* to control the output PWM with a non-inverted logic input signal. The shutdown signal can then be shared between the gate driver ICs of a complete inverter to interrupt operation with a single control signal.

D) Interlock

Interlocking is often used in half-bridge configurations to avoid a shoot-through current from the high-voltage DC bus supply. Connecting the following input signal pins of the top and bottom driver ICs together inhibits the static turn on for both channels at the same time:

- Top gate driver's non-inverting input (*IN+*) with the bottom driver inverting input (*IN-*)
- Bottom gate driver's non-inverting input (*IN+*) with the top driver inverting input (*IN-*)

Dynamic turn-on and turn-off characteristics of gate drivers and power switches can still lead to short-term shoot though. To avoid overlapping turn-on times at the power switches, a proper dead time setting for the PWM generation at the microcontroller is recommended.

8.4 Gate resistor selection

The gate resistor is a key component in the gate drive circuit . The gate resistor limits the source and the sink current of the gate driver thereby exercising control over the switching speed of the associated power transistor during both turn-on and turn-off operations. As such, the careful selection of an appropriate gate resistor represents a vital consideration in the design process. Some important considerations for selection of the gate resistance are:

- Optimize the switching losses
- Limit the overshoots and oscillations of the drain source voltage or the collector emitter voltage of the power transistor during turn-off
- Limit the overshoot and oscillations of the drain current or collector current during turn-on
- Damp the oscillations of the gate source or gate emitter voltage caused by parasitic inductances and capacitances in the gate loop

As a starting point in the gate driver selection, the gate resistor used in the datasheet of the power transistor for the characterization of turn-on and turn-off losses can be used. The power supply conditions are rarely the same as the power supply conditions used in power transistor datasheets. Therefore, an adaptation of the power transistor datasheet values is required to obtain a starting point to optimize of the final gate resistor. The method proposed here uses the same peak gate current value for both the actual application and the power transistor datasheet.

The peak gate current as per power transistor datasheet equals to:

$$\begin{aligned} & I_{\mathrm{G,\,pk}} = \frac{\Delta V_{\mathrm{GS}}}{R_{\mathrm{G,\,datasheet}} + R_{\mathrm{G,\,int}}} = \frac{\Delta V_{\mathrm{GS}}}{R_{\mathrm{G,\,application}} + R_{\mathrm{G,\,int}}} \\ & \text{with} \;\; \Delta V_{\mathrm{GS}} = V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}} \end{aligned} \tag{1}$$

Solving this equation for R_G leads to:

$$R_{\mathrm{G}} = \frac{\Delta V_{\mathrm{GS}}}{I_{\mathrm{G,\,pk}}} - R_{\mathrm{G,\,int}} \tag{2}$$

This method results in a starting point for the gate resistor selection. Further evaluations, such as EMI measurements, are required for the final dimensioning of the gate resistors as they have to be adjusted to work with the circuitry inductance, margins and allowed dV/dt transients.

While dimensioning the components for gate resistances, it is necessary to consider the average power dissipation in these resistors due to the switching of the power transistor, as explained in External gate resistor, as well as the pulse power capability of the component.

8.5 Power dissipation estimation

8.5.1 Gate driver

The gate driver's input side losses are dominated by the quiescent losses, which are calculated as:

$$P_{\mathrm{Q1}} = V_{\mathrm{VCC1}} \cdot I_{\mathrm{Q1}} \tag{3}$$

The gate driver's output side losses consist of the quiescent current losses, P_{Q2}, at nominal switching frequency and no load, the sourcing losses, P_{source}, and the sinking losses, P_{sink}:

$$P_{\mathrm{OUT}} = P_{\mathrm{Q2}} + P_{\mathrm{source}} + P_{\mathrm{sink}} \tag{4}$$

The quiescent losses on the output side, P_{Q2}, can be calculated as:

$$P_{\mathrm{Q2}} = \left(V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}\right) \cdot I_{\mathrm{Q2}} \tag{5}$$

The turn-on, P_{source}, and turn-off, P_{sink}, losses can be estimated using the resistive voltage divider between the internal resistance of the gate driver output stage, $R_{\mathrm{DSON,H}}$ or $R_{\mathrm{DSON,L}}$, the external gate resistor, $R_{\mathrm{G,ext}}$, and the internal gate resistance of the power transistor, $R_{\mathrm{G,int}}$, with the application related gate charge, Q_{G}, the total gate driving voltage, V_{VCC2} - V_{VEE2}, and switching frequency, f_{sw}:

$$\begin{aligned} P_{\mathrm{source}} &= \frac{1}{2} Q_G \cdot f_{\mathrm{sw}} \cdot \left(V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}\right) \cdot \frac{R_{\mathrm{DSON,H}}}{R_{\mathrm{DSON,\,H}} + R_{\mathrm{G,}ext\mathrm{,\,ON}} + R_{\mathrm{G,int}}} \\ P_{\mathrm{sink}} &= \frac{1}{2} Q_G \cdot f_{\mathrm{sw}} \cdot \left(V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}\right) \cdot \frac{R_{\mathrm{DSON,L}}}{R_{\mathrm{DSON,L}} + R_{G,ext\mathrm{,\,OFF}} + R_{\mathrm{G,int}}} \end{aligned} \tag{6}$$

Additionally, external components that surround the gate driver can heat up the IC. The mere calculation of losses and the theoretical junction temperature alone are not sufficient for a proven gate driver circuit design. A verification through measurement is required to avoid unexpected effects in the application. It is possible to identify the hotspots, for example, by using an infrared camera.

8.5.2 External gate resistor

The losses in the gate resistor for turn-on, $R_{\mathrm{G,ext,ON}}$ and the gate resistor for turn-off, $R_{\mathrm{G,ext,OFF}}$ can be estimated using the same resistive voltage divider formed by the resistances in the source and the sink path of the gate current as:

$$\begin{aligned} P_{source,\,ext} &= \frac{1}{2} Q_G \cdot f_{\mathrm{sw}} \cdot \left(V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}\right) \cdot \frac{R_{\mathrm{G,}ext\mathrm{,\,ON}}}{R_{\mathrm{DSON,\,H}} + R_{\mathrm{G,}ext\mathrm{,\,ON}} + R_{\mathrm{G,int}}} \\ P_{\mathrm{sink,}\,ext} &= \frac{1}{2} Q_G \cdot f_{\mathrm{sw}} \cdot \left(V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}\right) \cdot \frac{R_{\mathrm{DSON,L}}}{R_{\mathrm{DSON,L}} + R_{G,ext\mathrm{,\,OFF}} + R_{\mathrm{G,int}}} \end{aligned} \tag{7}$$

8.6 Layout guidelines

Having a well-designed PCB layout is crucial to achieve optimal performance of the gate driver. Subsequently, it ensures that the entire power electronic converter operates at its best. Creating a well-designed PCB layout requires a certain level of attention and consideration to specific key factors. The key points that should be considered while designing the PCB layout using 1EDR314xHQE gate drivers are:

- The low-ESR, low-ESL type decoupling capacitor on the input side must be placed close to the *VCC1* and *GND1* pins and connected to the pins such that the decoupling loop is as short as possible. Similarly, the decoupling capacitors on the output side should be placed close to the *VCC2* and *VEE2* pins and connected to the pins with a short connection
- It is crucial to minimize the physical area of the gate current loop that carries the current for charging and discharging the gate of the power transistor. The gate loop contains traces with high dv/dt and di/dt and having a short loop minimizes the noise caused by the turning on and off of the gates of the power transistor. Furthermore, a short loop also minimizes the stray inductance of the gate loop and improves the switching performance. To accomplish a short gate loop, the gate driver should be positioned near the power transistor and the decoupling capacitors that store the energy for high peak currents should be located in close proximity to the gate driver

- To reduce the stray inductance of the gate loop even further, wide traces can be used for the traces in the gate loop. Furthermore, the forward path and the return path of the currents can be routed parallel to each other on the same PCB layer or overlapping each other on adjacent PCB layers to achieve the least amount of stray inductance
- In the case of a unipolar power supply, the *VEE2* pin of the gate driver should be connected to the Kelvin source/emitter pin of the power transistor, if available. Similarly, in the case of a bipolar power supply, the virtual ground between the decoupling capacitors or the *GND2* pin should be connected to the Kelvin source/emitter pin of the power transistor. If the Kelvin pin is not available, then the connection to the source/emitter should be done directly to the pin and not involve any portion of the power trace on the PCB, in order to avoid the high current from the power transistor flowing in the gate loop
- The area below the body of the gate driver package should be kept free of any traces to ensure the integrity of the safety isolation between the input and output side
- It is recommended that the input signals of the gate driver connected to the IN+ and IN- pins be kept away from any noisy traces. Although the 1EDR314xHQE gate drivers come with an integrated input filter that can filter high frequency noise on the input signal, an external RC filter with a small time constant can be placed close to these pins for enhanced filtering. Additionally, a ground plane below the input signal traces is recommended for shielding the signals from noise
- The gate driver IC experiences power dissipation during system operation as explained in the Power dissipation estimation. This heat generated in the device is dissipated mostly via the PCB. Maximizing the copper area connected to the *GND1* and *VEE2* pins is recommended for effectively dissipating the heat from the gate driver on to the PCB

Figure 51, Figure 52, Figure 53 and Figure 54 show examples of PCB layouts for gate drivers with separated output and *GND2* pin. A more detailed layout for all the configurations can be found in the design files of the evaluation boards listed in Table 2.

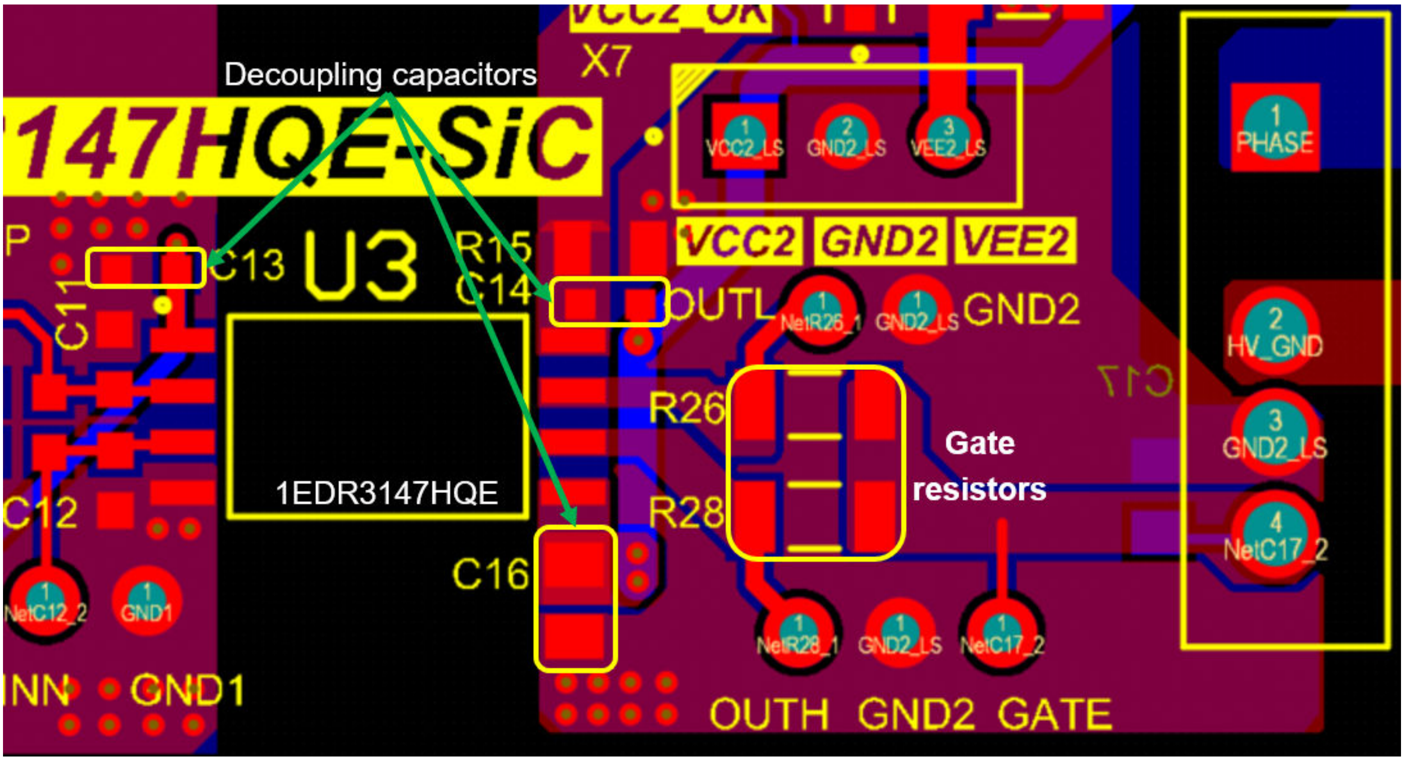


Figure 51 Half-bridge low-side driver sample layout for variants with separate output

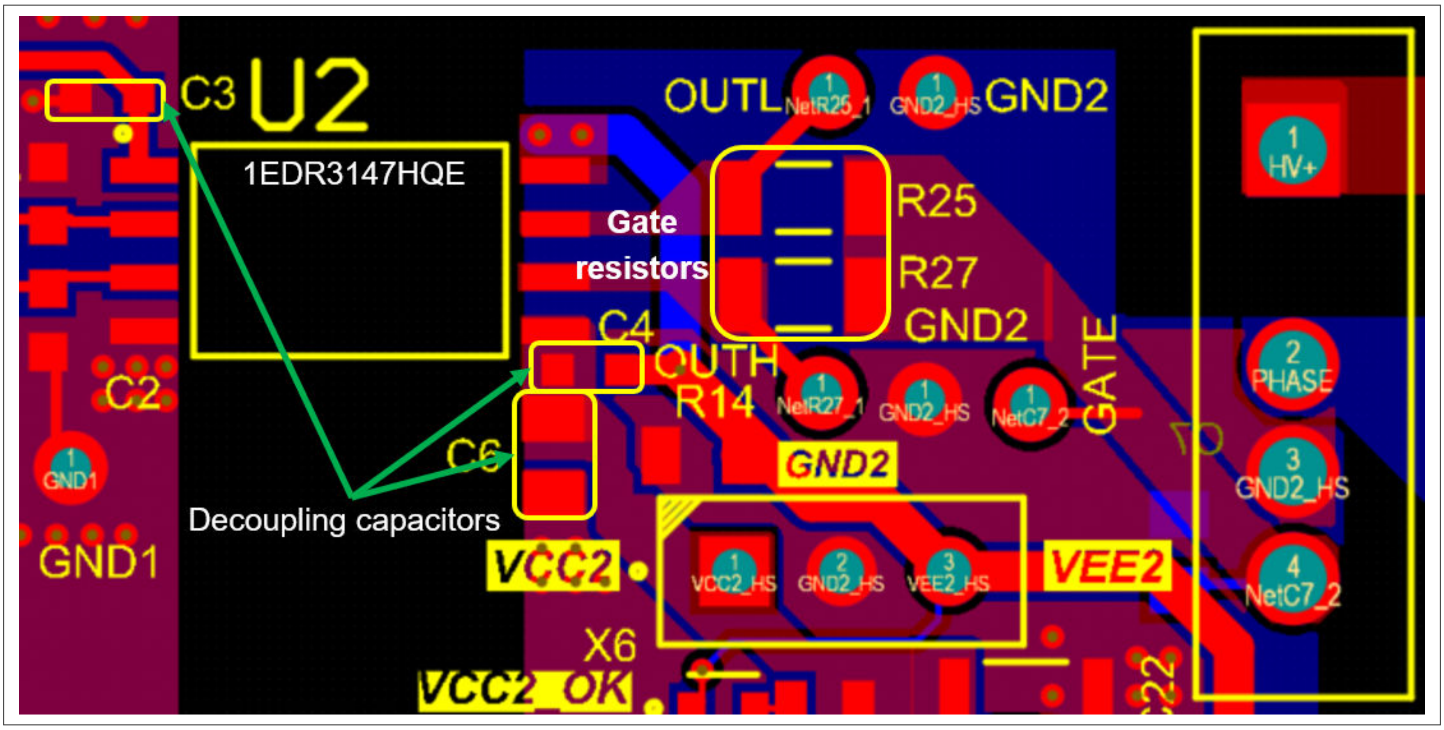


Figure 52 Half-bridge high-side driver sample layout for variants with separate output

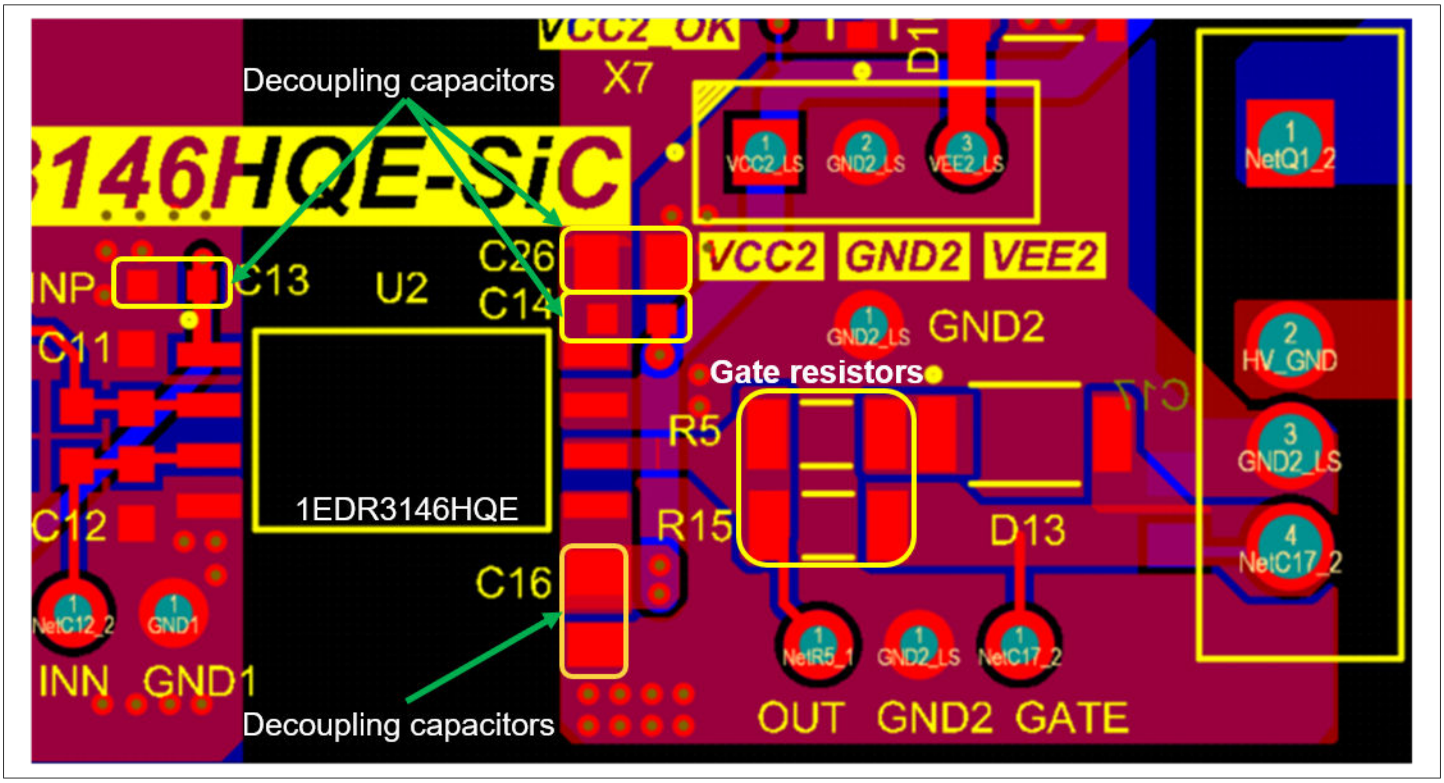


Figure 53 Half-bridge low-side driver sample layout for variants with *GND2* pin

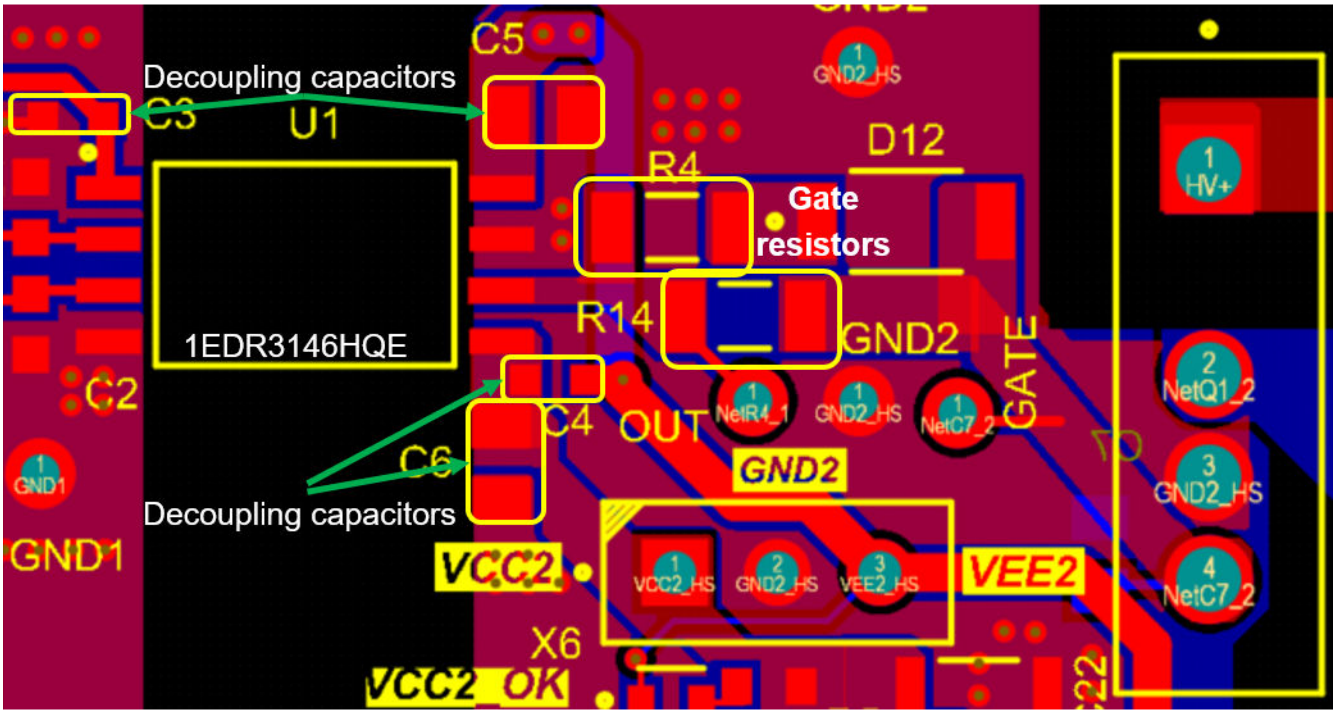


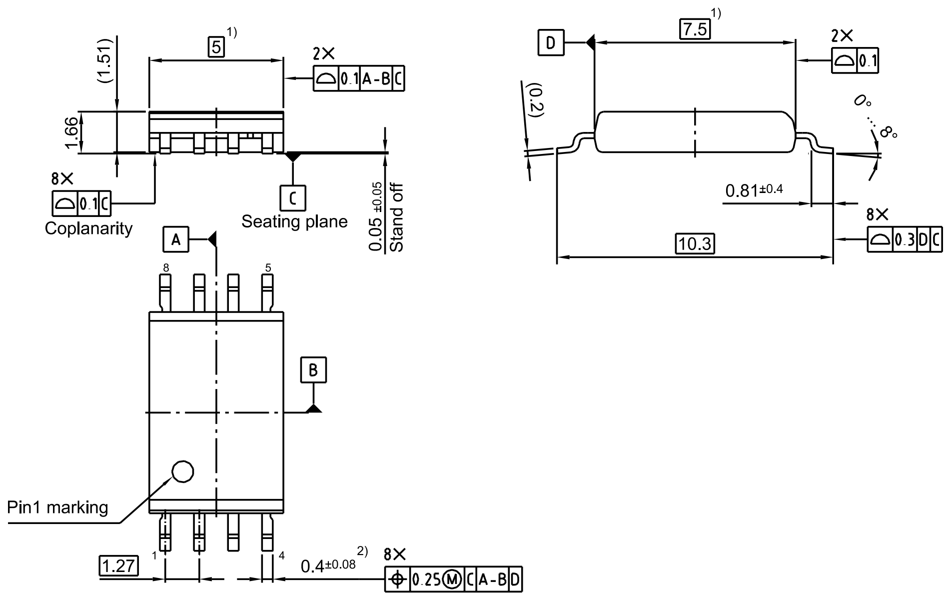
Figure 54 Half-bridge high-side driver sample layout for variants with *GND2* pin

9 Related products

***Note**: Please consider the gate driver IC power dissipation and insulation requirements for the selected power switch and operating condition.*

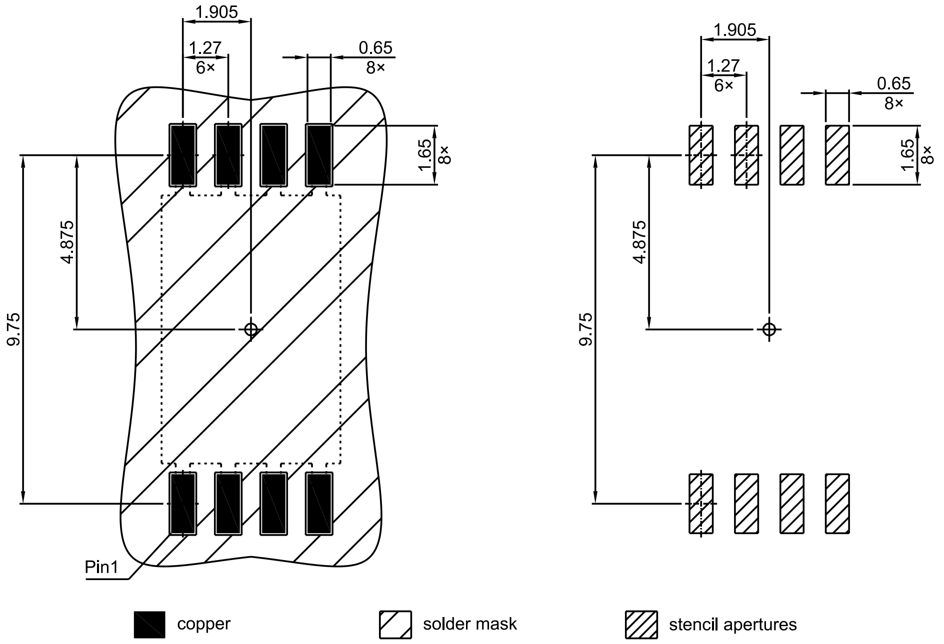
Product group	Product name	Description
TRENCHSTOP™ IGBT Discretes	AIKB30N65DF5	650 V, 30 A automotive IGBT with anti-parallel diode in TO-263-3 (D2PAK) package
	AIKW50N65DF5	650 V, 50 A automotive IGBT with anti-parallel diode in TO-247-3 package
	AIKB50N65DH5	650 V, 50 A automotive IGBT with anti-parallel diode in TO-263-3 package
	AIGW50N65H5	650 V, 50 A automotive IGBT without anti-parallel diode in TO-247-3 package
	AIKBE50N65RF5	650V, 50A automotive fast switching IGBT with SiC diode in TO263-7 (D2PAK) package
CoolSiC™ SiC MOSFET Discretes	AIMCQ120R060M1T	1200 V, 60 mΩ automotive SiC MOSFET in HDSOP-22-3 (Q-DPAK) package
	AIMZHN120R060M1T	1200 V, 60 mΩ automotive SiC MOSFET in TO-247-4 package
	AIMZH120R060M1T	1200 V, 60 mΩ automotive SiC MOSFET in TO-247-4L (thin leads) package
	AIMBG120R060M1	1200 V, 60 mΩ automotive SiC MOSFET in TO-263-7 (D2PAK) package
	AIMZA75R060M1H	750 V, 60 mΩ automotive SiC MOSFET in TO-247-4 package
	AIMDQ75R060M1H	750 V, 60 mΩ automotive SiC MOSFET in HDSOP-22-3 (Q-DPAK) package
	AIMBG75R060M1H	750 V, 60 mΩ automotive SiC MOSFET in TO-263-7 (D2PAK)) package
CoolMOS™ Si MOSFET Discretes	IPDQ65R060CFD7A	650 V, 60 mΩ automotive Si MOSFET in HDSOP-22-3 (Q-DPAK) package
	IPB65R050CFD7A	650 V, 60 mΩ automotive Si MOSFET in TO-263-3 (D2PAK) package
	IPBE65R050CFD7A	650 V, 50 mΩ automotive Si MOSFET in TO-263-7 (D2PAK) package
	IPW65R048CFDA	650 V, 48 mΩ automotive Si MOSFET in TO-247-3 package

10 Package dimensions



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.1 max.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊲⊕]
Drawing according to ISO 8015, general tolerances ISO 2768-mK

Figure 55 LDSO-8-1 300 mil (Plastic dual small outline package, 300 mil)



All dimensions are in units mm
All pads are non-solder mask defined

Figure 56 LDSO-8-1 300 mil recommended footprint

11 Revision history

Document version	Date of release	Description of changes
v1.00	2025-01-07	• Initial official release
v1.01	2025-08-05	• Updated insulation section

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Edition 2025-08-05

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-crr1727785541342

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