

Features

- Single-channel isolated gate driver
- 45 ns input-to-output propagation delay with excellent accuracy (+6/-4 ns)
- Separate low impedance source and sink outputs
- Fast clamping of parasitics-induced output overshoots under UVLO conditions
- Fast start-up times and fast recovery after supply glitches
- Fast start-up times and fast recovery after supply glitches
- Optimized UVLO levels (4 V, 8 V, 12 V, 15 V) for Si, SiC and GaN transistors
- High common-mode transient immunity (CMTI > 300 V/ns)
- Available in 8-pin 150mil DSO package
- Fully qualified according JEDEC for industrial applications

Isolation and safety certificates

- UL 1577 with $V_{ISO} = 3000 V_{RMS}$
- IEC 62368-1 (certification n. CN77761)
- GB 4943.1-2022 (certification n. CQC26001518668)

Potential applications

- Server and Telecom switch-mode power supplies (SMPS)
- EV off-board chargers
- Low-voltage drives and power tools
- Solar micro inverter, solar optimizer
- Industrial power supplies (SMPS, residential UPS)

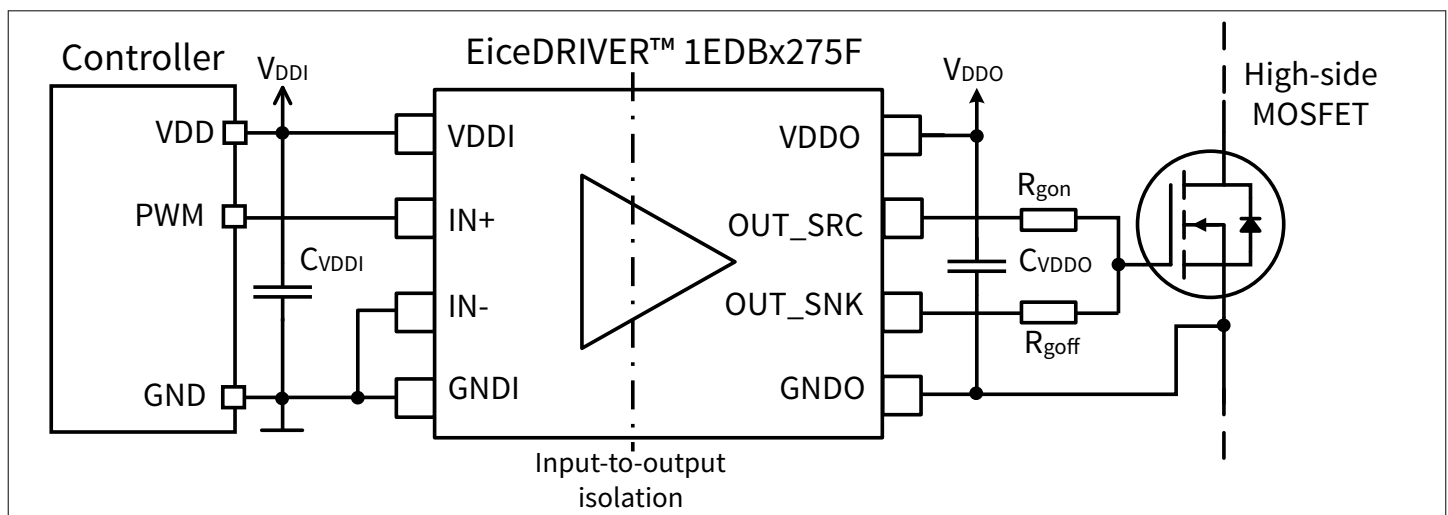
Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22, and J-STD-020.

Description

EiceDRIVER™ 1EDBx275F is a family of single-channel isolated gate driver ICs, designed to drive Si, SiC and GaN power switches. 1EDBx275F is available in an 8-pin DSO package with 4 mm input-to-output creepage distance; it provides isolation by means of on-chip coreless transformer (CT) technology.

With tight timing specifications, 1EDBx275F is designed for fast-switching medium-to-high power systems. Excellent common-mode rejection, low part-to-part skew, fast signal propagation and small package size make 1EDBx275F a superior alternative to high-side driving solutions using optocouplers or pulse transformers.



EiceDRIVER™ 1EDBx275F

Single-channel isolated gate driver ICs in 150 mil DSO package



Description

Table 1 EiceDRIVER™ 1EDBx275F Portfolio

Part number	Peak source/sink current	UVLO ON/OFF	Isolation certification	Package
1EDB7275F	5 A/9 A	4.2 V/3.9 V	UL 1577 ($V_{ISO} = 3000 V_{RMS}$)	PG-DSO-8
1EDB8275F		8.0 V/7.0 V		
1EDB6275F		12.2 V/11.5 V		
1EDB9275F		14.9 V/14.4 V		

Table of contents

	Table of contents	3
1	Pin configuration and description	4
2	Functional description	5
2.1	Block diagram	5
2.2	Power supply and Undervoltage Lockout (UVLO)	5
2.2.1	Input supply voltage	5
2.2.2	Output supply voltage	5
2.2.3	Input stage	6
2.3	Driver output	6
2.4	Output active clamping	7
2.5	CT communication and input to output data transmission	7
3	Electrical characteristics and parameters	8
3.1	Absolute maximum ratings	8
3.2	Thermal characteristics	9
3.3	Operating range	9
3.4	Electrical characteristics	10
3.5	Isolation specifications	14
4	Timing diagrams	16
5	Layout recommendation	18
6	Application notes	19
6.1	Driving 600 V CoolGaN™	19
6.2	Driving 650 V CoolSiC™	20
7	Typical characteristics	21
8	Package outline dimensions	29
8.1	Device numbers and markings	29
8.2	Package PG-DSO-8	29
	Revision history	32
	Disclaimer	33

1 Pin configuration and description

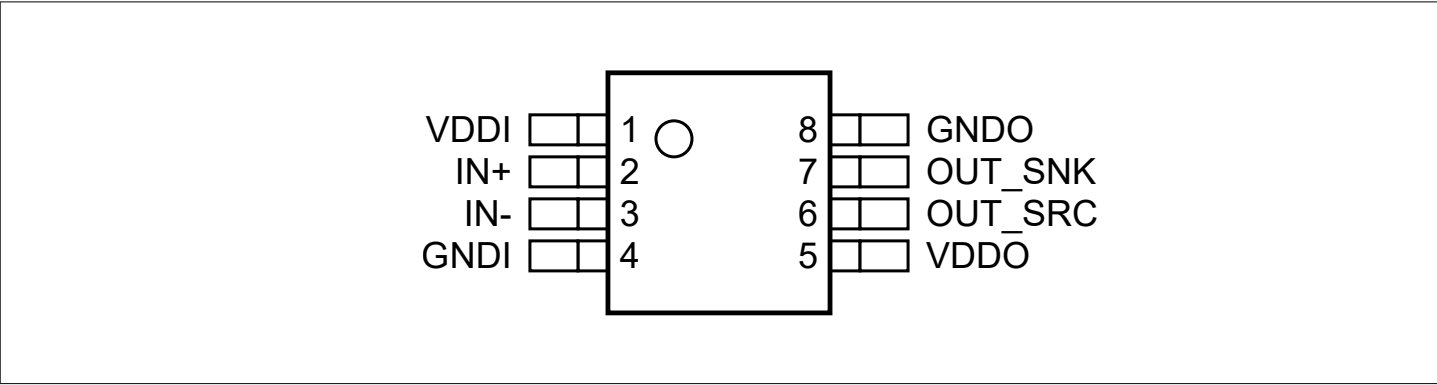


Figure 1 Pin configuration (top side view)

Table 2 Pin description

Pin	Symbol	Description
1	VDDI	Input-side supply voltage (3 V to 15 V)
2	IN+	Non-inverting driver input (active high); if IN+ is low or left open, OUT_SNK is low
3	IN-	Inverting driver input (active low); if IN- is high or left open, OUT_SNK is low
4	GNDI	Input-side ground reference
5	VDDO	Output-side supply voltage (up to 20 V)
6	OUT_SRC	Driver output source, low-impedance switch to VDDO
7	OUT_SNK	Driver output sink, low-impedance switch to GNDO
8	GNDO	Output-side ground reference

For package drawing details see [Chapter 8 Package outline dimensions](#).

2 Functional description

2.1 Block diagram

A simplified functional block diagram for the EiceDRIVER™ 1EDBx275F is given in Figure 2.

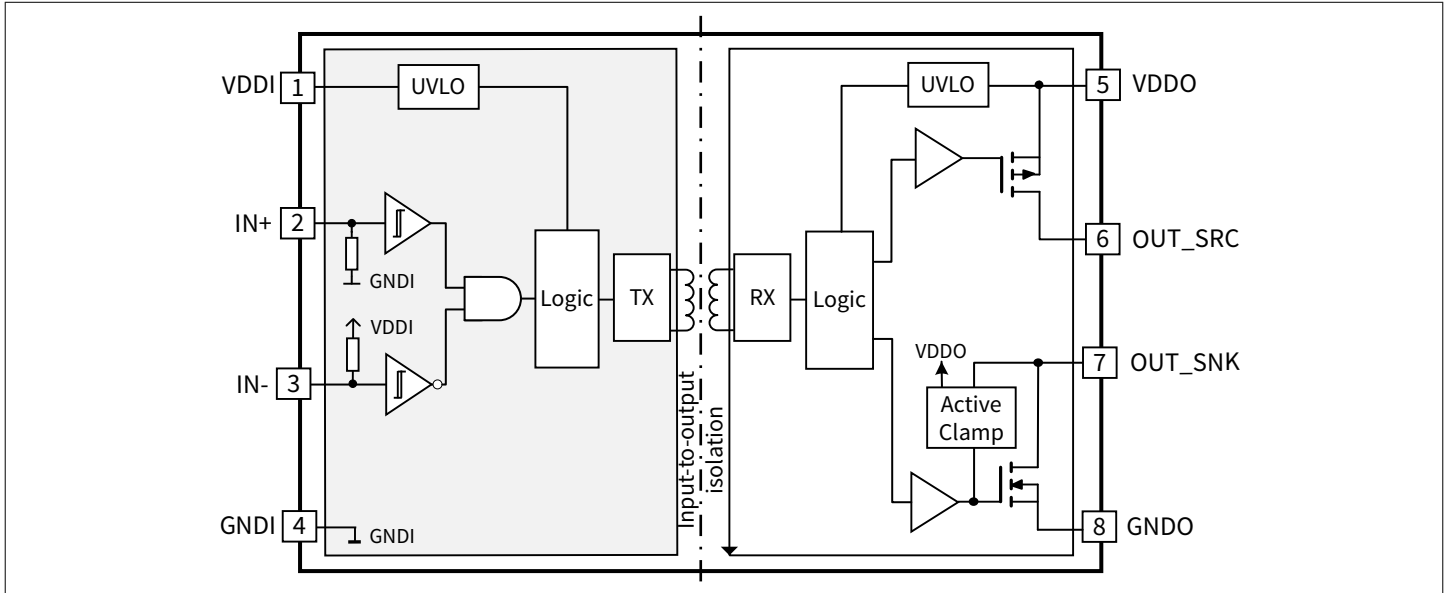


Figure 2 Block diagram

2.2 Power supply and Undervoltage Lockout (UVLO)

Due to the isolation between input and output side, two power domains with independent power management are required. Undervoltage Lockout (UVLO) functions for both input and output supplies ensure a defined startup and robust functionality under all operating conditions.

2.2.1 Input supply voltage

The input die is powered via VDDI and supports a wide supply voltage range from 3 V to 15 V. A ceramic bypass capacitor must be placed between VDDI and GNDI in close proximity to the device; a minimum capacitance of 100 nF is recommended.

Power consumption to some extent depends on switching frequency, as the input signal is converted into a train of repetitive current pulses to drive the coreless transformer. Due to the chosen robust encoding scheme the average repetition rate of these pulses and thus the average supply current depends on the switching frequency, f_{sw} . However, for $f_{sw} < 500$ kHz this effect is very small.

The Undervoltage Lockout function for the input supply VDDI ensures that, as long as VDDI is below UVLO (e.g. in startup), no data is transferred to the output side and the gate driver output is held low (Safety Lock-down at startup). When VDDI exceeds the UVLO level, the PWM input signal is transferred to the output side. If the output side is ready (not in UVLO condition), the output reacts according to the logic input.

2.2.2 Output supply voltage

The output die is powered via VDDO (up to 20 V). A ceramic bypass capacitor must be placed between VDDO and GNDO in close proximity to the device. A minimum capacitance of $20 \times C_{iss}$ (MOSFET input capacitance) is recommended to ensure an acceptable ripple (5% of VDDO) on the supply pin.

The minimum supply voltage is set by the Undervoltage Lockout (UVLO) function. The gate driver output can be switched only, if the output supply voltage (V_{DDO}) exceeds the output-side UVLO. Thus, it can be guaranteed that the switch transistor is not operated, if the driving voltage is too low to achieve a complete and fast transition to the "on" state. Low driving voltage in fact could cause the power MOSFET to enter its saturation (ohmic) region with potentially destructive power dissipation; the output UVLO ensures that the switch transistor always stays within its Safe Operating Area (SOA). Versions with 4 V, 8 V, 12 V, 15 V UVLO thresholds for the output supply are currently available; [Table 3](#) shows the recommended UVLO levels for different Infineon power switch families.

Table 3 Recommended 1EDBx275F UVLO levels for typical use-cases

Switch family	Switch part number example	Recommended 1EDBx275F
Logic level OptiMOS™	BSC010N04LS6, BSZ070N08LS5, ..	1EDB7275F (4 V UVLO)
Normal level OptiMOS™	BSC040N10NS5, BSZ084N08NS5, ..	1EDB8275F (8 V UVLO)
CoolMOS™	IPP60R099C7, IPB60R600P6, ..	1EDB8275F (8 V UVLO)
650 V CoolSiC™	IMZA65R027M1H, IMW65R107M1H, ..	1EDB6275F (12 V UVLO for 15 V V_{GS} driving)
		1EDB9275F (15 V UVLO for 18 V V_{GS} driving)
600 V CoolGaN™	IGOT60R070D1, IGLD60R070D1, ..	1EDB7275F (4 V UVLO)

2.2.3 Input stage

The logic driver output state is equal to the non-inverted or inverted input signal state at pins IN+ or IN-, respectively. The non-inverting input IN+ is internally pulled down to a logic low voltage and the inverting input is internally pulled up to a logic high voltage. This prevents any switching-on during power-up or in other situations with insufficient supply voltage.

The input is compatible with LV-TTL levels and provide a hysteresis of typically 0.9 V. This hysteresis is independent of the supply voltage V_{DDI} .

[Table 4](#) shows the IN+, IN- driver logic in case of sufficiently high supply voltage. Otherwise the outputs of the driver are determined by the Undervoltage Lockout (UVLO) and Output Active Clamping functionalities as shown in [Table 5](#).

Table 4 Logic table in case of sufficient bias power

Inputs		Supplies	Outputs	Note
IN+	IN-	V_{DDI} , V_{DDO}	OUT	
H	L	> UVLO $_{V_{DDX},on}$ (active)	H	–
x	H		L	The output is disabled via IN- (active low)
L	x		L	The output is disabled via IN+ (active high)

2.3 Driver output

The rail-to-rail output stage realized with complementary MOS transistors is able to provide a typical 5.4 A sourcing and 9.8 A sinking peak current for a 15 V supply. The low on-resistance coming together with high driving current is particularly beneficial for fast switching of very large MOSFETs. With a R_{on} of 0.95 Ω for the sourcing pMOS and 0.48 Ω for the sinking nMOS transistor the driver can in most applications be considered as a nearly ideal switch. The p-channel sourcing transistor enables real rail-to-rail behavior without suffering from the voltage drop unavoidably associated with nMOS source follower stages.

In case of floating inputs or insufficient supply voltage not exceeding the UVLO thresholds, the driver output is actively clamped to the "low" level (GNDO).

2.4 Output active clamping

The Undervoltage Lockout (UVLO) ensures no driver operation for supplies below the UVLO thresholds. However, this is not sufficient to guarantee that the output of the driver is kept low. Transient-induced current on the MOSFETs side may pull-up the output node of the driver and the gate voltage causing an unwanted turn-on of the switch; this is particularly critical in systems using bootstrapping since, during start-up, the supply of the high-side channel is delayed, while the low-side MOSFETs is already switching. In resonant topologies (as LLC), the half-bridge switching node may be pulled up after the turn-off of the low-side switch. When this is turned on again, the dv/dt induced increase of the high-side gate voltage cannot be clamped by the drivers $R_{DS(on),sink}$ if the bootstrap supply is not yet available.

With a fast active clamping circuit in the output stage, EiceDRIVER™ 1EDBx275F ensures safe operation in all UVLO situations. This structure allows fast reaction and effective clamping of the output pins (OUT). The exact reaction time depends on the output supply (V_{DDO}) and on the output voltage levels; however, already for very low supply levels (~ 1 V), the active clamping is able to react in some tens of ns.

Undervoltage Lockout together with the Output Active Clamping ensure that the output is actively held low in case of insufficient output-side supply voltage.

Table 5 Logic table in case of insufficient supply voltages

Inputs	Supplies		Output
INx	V_{DDI}	V_{DDO}	OUT
x	$> UVLO_{VDDI,on}$	$1.2\text{ V} < V_{DDO} < UVLO_{VDDO,on}$	L

2.5 CT communication and input to output data transmission

A coreless transformer (CT) based communication module is used for PWM signal transfer between input and output. A proven high-resolution pulse repetition scheme in the transmitter combined with a watchdog timeout at the receiver side enables recovery from communication fails and ensures safe system shutdown in failure cases.

3 Electrical characteristics and parameters

The absolute maximum ratings are listed in Table 6. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.1 Absolute maximum ratings

Table 6 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input supply voltage	V_{DDI}	-0.3	–	17	V	–
Output supply voltage	V_{DDO}	-0.3	–	22	V	–
Voltage at pins IN+, IN-	V_{IN}	-0.3	–	17	V	–
		-5	–	–	V	transient for 50 ns
Voltage at pin OUT_SRC	V_{OUT_SRC}	$V_{DDO} - 24$	–	$V_{DDO} + 0.3$	V	OUT = low, DC
		$V_{DDO} - 24$	–	$V_{DDO} + 2$	V	OUT = low, transient for 200 ns
Voltage at pin OUT_SNK	V_{OUT_SNK}	-0.3	–	24	V	OUT = high, DC
		-2	–	24	V	OUT = high, transient for 200 ns
Reverse current peak at pin OUT_SRC	I_{SRC_rev}	-5	–	–	A_{pk}	transient for 500 ns
Reverse current peak at pin OUT_SNK	I_{SNK_rev}	–	–	5	A_{pk}	transient for 500 ns
Junction temperature	T_J	-40	–	150	°C	–
Storage temperature	T_{STG}	-55	–	150	°C	–
Soldering temperature	T_{SOL}	–	–	260	°C	¹⁾ Reflow/wave soldering
ESD capability	V_{ESD_CDM}	–	–	0.5	kV	²⁾ Charged Device Model (CDM)
	V_{ESD_HBM}	–	–	2	kV	³⁾ Human Body Model (HBM)

1) According to JESD22A111

2) According to ESD-CDM: ANSI/ESDA/JEDEC JS-002

3) According to ESD-HBM: ANSI/ESDA/JEDEC JS-001 (discharging 100 pF capacitor through 1.5 kΩ resistor)

3.2 Thermal characteristics

Table 7 Thermal characteristics at $T_A = 25^\circ\text{C}$

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
¹⁾ Thermal resistance junction-ambient	R_{thJA25}	–	116	–	K/W	200 mW output power
²⁾ Thermal resistance junction-case (top)	R_{thJC25}	–	54	–	K/W	
³⁾ Thermal resistance junction-board	R_{thJB25}	–	45	–	K/W	
⁴⁾ Characterization parameter junction-top	Ψ_{thJT25}	–	9	–	K/W	
⁴⁾ Characterization parameter junction-board	Ψ_{thJB25}	–	36	–	K/W	

- 1) Obtained by simulating a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a
- 2) Obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88
- 3) Obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8
- 4) Estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining R_{th} , using a procedure described in JESD51-2a (sections 6 and 7)

3.3 Operating range

Table 8 Operating range

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input supply voltage	V_{DDI}	3.0	–	15	V	Min. defined by UVLO
Output supply voltage	V_{DDO}	4.5	–	20	V	for 1EDB7275F
		8.5	–	20	V	for 1EDB8275F
		12.8	–	20	V	for 1EDB6275F
		15.5	–	20	V	for 1EDB9275F
Logic input voltage at pins IN+, IN-	V_{IN}	-0.3	–	15	V	–
Junction temperature	T_J	-40	–	150	$^\circ\text{C}$	¹⁾
Ambient temperature	T_A	-40	–	125	$^\circ\text{C}$	–

- 1) Continuous operation above 125°C may reduce lifetime

3.4 Electrical characteristics

Unless otherwise noted the electrical characteristics are given for $V_{DDI} = 3.3\text{ V}$, $V_{DDO} = 12\text{ V}$ ($V_{DDO} = 18\text{ V}$ for 1EDB6275F, 1EDB9275F) and no load.

Typical values are given at $T_J = 25^\circ\text{C}$. Minimum and maximum values are the lower and upper limits valid within the full operating temperature range.

Table 9 Power supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
I_{VDDI} quiescent current	I_{VDDIq}	–	0.85	1	mA	no switching
I_{VDDO} quiescent current	I_{VDDOq}	–	0.65	0.85	mA	OUT = low, no switching, $V_{DDO} = 12\text{ V}$
		–	0.72	1.0	mA	OUT = low, no switching, $V_{DDO} = 18\text{ V}$
		–	0.84	1.0	mA	OUT = high, no switching, $V_{DDO} = 12\text{ V}$

Table 10 Undervoltage Lockout V_{DDI}

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn-on threshold V_{DDI}	$UVLO_{VDDI, on}$	2.7	2.85	3.0	V	–
Undervoltage Lockout (UVLO) turn-off threshold V_{DDI}	$UVLO_{VDDI, off}$	–	2.65	–	V	–
UVLO threshold hysteresis V_{DDI}	$UVLO_{VDDI, hys}$	0.15	0.2	0.25	V	–

Table 11 Undervoltage Lockout V_{DDO} for 1EDB7275F (4 V UVLO option)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold V_{DDO}	$UVLO_{VDDO, on}$	4.0	4.2	4.4	V	–
Undervoltage Lockout (UVLO) turn off threshold V_{DDO}	$UVLO_{VDDO, off}$	–	3.9	–	V	–
UVLO threshold hysteresis V_{DDO}	$UVLO_{VDDO, hys}$	0.2	0.3	0.4	V	–

Table 12 Undervoltage Lockout V_{DDO} for 1EDB8275F (8 V UVLO option)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold V_{DDO}	$UVLO_{VDDO, on}$	7.6	8.0	8.4	V	–
Undervoltage Lockout (UVLO) turn off threshold V_{DDO}	$UVLO_{VDDO, off}$	–	7.0	–	V	–

(table continues...)

Table 12 (continued) Undervoltage Lockout V_{DDO} for 1EDB8275F (8 V UVLO option)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
UVLO threshold hysteresis V_{DDO}	$UVLO_{VDDO, hys}$	0.7	1	1.3	V	–

Table 13 Undervoltage Lockout V_{DDO} for 1EDB6275F (12 V UVLO option)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold V_{DDO}	$UVLO_{VDDO, on}$	11.7	12.2	12.7	V	–
Undervoltage Lockout (UVLO) turn off threshold V_{DDO}	$UVLO_{VDDO, off}$	–	11.5	–	V	–
UVLO threshold hysteresis V_{DDO}	$UVLO_{VDDO, hys}$	0.5	0.7	0.9	V	–

Table 14 Undervoltage Lockout V_{DDO} for 1EDB9275F (15 V UVLO option)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold V_{DDO}	$UVLO_{VDDO, on}$	14.4	14.9	15.4	V	–
Undervoltage Lockout (UVLO) turn off threshold V_{DDO}	$UVLO_{VDDO, off}$	–	14.4	–	V	–
UVLO threshold hysteresis V_{DDO}	$UVLO_{VDDO, hys}$	0.3	0.5	0.7	V	–

Table 15 Logic inputs $IN+$, $IN-$

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{INH}	1.9	2.2	2.5	V	–
Input voltage threshold for transition HL	V_{INL}	1	1.3	1.6	V	–
Input voltage threshold hysteresis	$V_{IN, hys}$	–	0.9	–	V	–
High-level input leakage current at pin $IN+$	$I_{IN+, H}$	–	40	70	μA	$IN+$ tied to V_{DDI}
Low-level input leakage current at pin $IN-$	$I_{IN-, L}$	–55	–40	–	μA	$IN-$ tied to $GNDI$
Input pull-down resistor	$R_{IN, PD}$	–	75	–	$k\Omega$	–
Input pull-up resistor	$R_{IN, PU}$	–	75	–	$k\Omega$	–

Table 16 **Static output characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High-level (sourcing) output resistance	R_{on_SRC}	0.52	0.95	1.70	Ω	$I_{SNK} = 50 \text{ mA}$
Peak sourcing output current	I_{SRC_pk}	–	5	–	A	¹⁾ $V_{DDO} = 12 \text{ V}$, $V_{OUT} = 0 \text{ V}$; see Figure 24; Figure 25
		–	6	–	A	¹⁾ $V_{DDO} = 18 \text{ V}$, $V_{OUT} = 0 \text{ V}$; see Figure 24; Figure 25
Low-level (sinking) output resistance	R_{on_SNK}	0.31	0.48	0.88	Ω	$I_{SRC} = 50 \text{ mA}$
Peak sinking output current	I_{SNK_pk}	–	-9	–	A	$V_{OUT} = V_{DDO} = 12 \text{ V}$; see Figure 24; Figure 25
		–	-10	–	A	$V_{OUT} = V_{DDO} = 18 \text{ V}$; see Figure 24; Figure 25

1) Parameter not subject to production test - verified by design/ characterization

Table 17 **Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
IN+/IN- to output propagation delay	t_{PDOn}, t_{PDOff}	41	45	51	ns	see Figure 3
Part-to-part skew	$\Delta t_{PDOn,p-p}$	–	–	2	ns	¹⁾
	$\Delta t_{PDOff,p-p}$	–	–	2	ns	¹⁾
Pulse width distortion $ t_{PDOff} - t_{PDOn} $	t_{PWD}	–	–	2	ns	²⁾ See Figure 4
Rise time	t_{rise}	–	6.5	12	ns	³⁾ $V_{DDO} = 12 \text{ V}$, $C_{LOAD} = 1.8 \text{ nF}$, see Figure 5
		–	8.3	16	ns	³⁾ $V_{DDO} = 18 \text{ V}$, $C_{LOAD} = 1.8 \text{ nF}$, see Figure 5
Fall time	t_{fall}	–	4.5	8	ns	³⁾ $V_{DDO} = 12 \text{ V}$, $C_{LOAD} = 1.8 \text{ nF}$, see Figure 5
		–	5	9	ns	³⁾ $V_{DDO} = 18 \text{ V}$, $C_{LOAD} = 1.8 \text{ nF}$, see Figure 5
Minimum input pulse width that changes output state	t_{PW}	15	19	23	ns	see Figure 6
Input-side start-up time	$t_{START,VDDI}$	–	3	–	μs	³⁾ See Figure 7
Input-side deactivation time	$t_{STOP,VDDI}$	–	300	–	ns	³⁾ See Figure 7
Output-side start-up time	$t_{START,VDDO}$	–	5	–	μs	³⁾ See Figure 8
Output-side deactivation time	$t_{STOP,VDDO}$	–	125	–	ns	³⁾ See Figure 8

(table continues...)

Table 17 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Activation time of output clamping in UVLO condition	$t_{\text{CLAMP,OUT}}$	–	20	–	ns	³⁾ See Figure 9

- 1) The parameter gives the difference in propagation delay between different samples switching in the same direction under same conditions, including same ambient temperature
- 2) The parameter gives the maximum difference between on and off propagation delay shown from the same sample over the operating temperature range
- 3) Parameter not subject to production test - verified by design/characterization

Table 18 Common Mode Transient Immunity (CMTI)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Static Common Mode Transient Immunity	$ CM_{\text{Static,H}} $	300	–	–	V/ns	^{1) 2)} $V_{\text{CM}} = 1500 \text{ V}$; IN- tied to GNDI, IN+ tied to V_{DDI} (logic high inputs)
	$ CM_{\text{Static,L}} $	300	–	–	V/ns	^{1) 2)} $V_{\text{CM}} = 1500 \text{ V}$; IN- tied to GNDI, IN+ tied to GNDI (logic low inputs)
Dynamic Common Mode Transient Immunity	$ CM_{\text{Dynamic}} $	300	–	–	V/ns	^{1) 3)} $V_{\text{CM}} = 1500 \text{ V}$; IN- tied to GNDI, dynamic IN+ (10 MHz square wave)

- 1) Minimum slew rate of a common mode voltage that is able to cause a wrong output signal
- 2) Verified by characterization according to VDE0884-11 standard definitions and test-methods
- 3) Verified by characterization with ground reference for the common mode pulse generator connected to the coupler input-side ground to reflect real applications requirements

3.5 Isolation specifications

This coupler is suitable for rated insulation only within the given safety limiting values. Compliance with the safety limiting values shall be ensured by means of suitable protective circuits.

Table 19 Input-to-output isolation specifications

Parameter	Symbol	Value	Unit	Note or Test Condition
Nominal input-to-output clearance ¹⁾	CLR	4.0	mm	Shortest distance in air between any input pin and any output pin
Nominal input-to-output creepage ¹⁾	CRP	4.0	mm	Shortest distance over package surface between any input pin and any output pin
Comparative tracking index	CTI	≥ 600	V	According to DIN EN 60112 (VDE 0303-11)
Material group	–	I	–	According to IEC 60112
Pollution degree	–	2	–	According to IEC 60664-1
Overvoltage category per IEC 60664-1	–	I -IV	–	Rated mains voltage ≤ 150 V _{RMS}
	–	I -III	–	Rated mains voltage ≤ 300 V _{RMS}
	–	I -II	–	Rated mains voltage ≤ 600 V _{RMS}
Climatic category	–	40/125/21	–	–

Input-to-output isolation according to UL1577 Edition 5 ²⁾

Input-to-output isolation voltage	V _{ISO}	3000	V _{RMS}	V _{TEST} = V _{ISO} for t = 60 s (qualification); V _{TEST} = 1.2 x V _{ISO} for t = 1 s (100% productive tests)
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Input-to-output isolation according to DIN VDE0884-17 ³⁾

Maximum rated transient isolation voltage	V _{IOTM}	4242	V _{pk}	V _{TEST} = 1.2 x V _{IOTM} for t _{ini} = 1 s
Apparent charge	q _{PD}	< 5	pC	Method b1 V _{PD(ini)} = 1.2 x V _{IOTM} for t _{ini} = 1 s V _{PD(m)} = 2065 V for t _m = 1 s
Maximum surge isolation voltage ⁴⁾	V _{IOSM}	6000	V _{pk}	V _{IOSM_TEST} = 1.3 x V _{IOSM}
Isolation resistance input- to- output ^{5) 6)}	R _{IO}	10 ¹²	Ω	V _{IO} = 500 V _{dc} for t = 60 s, T _A = 25°C
		10 ¹¹	Ω	V _{IO} = 500 V _{dc} for t = 60 s, T _A = 125°C
		10 ⁹	Ω	V _{IO} = 500 V _{dc} for t = 60 s, T _A = T _S = 150°C
Capacitance input-to-output ⁵⁾	C _{IO}	1	pF	f = 1 MHz

1) Creepage and clearance requirements depend on the application and related end-equipment isolation standard. Care should be taken to keep the required creepage and clearance value on printed-circuit-board level

2) See certificate number E509502

3) Parameters are tested according to VDE0884-17 specifications but no safety certification is planned

4) The surge test is performed in insulation oil to determine the intrinsic surge immunity of the insulation barrier

5) The parameters apply to the product converted in a two terminals device with all terminals on side 1 connected together and all terminals on side 2 connected together

6) Parameter verified by characterization on a limited amount of samples previously stressed with a dielectric strength test (V_{ISO})

Table 20 **Safety limiting values**

Parameter	Symbol	Value	Unit	Note or Test Condition
Maximum input power dissipation	P_{S_I}	40	mW	$T_A = 25\text{ °C}, T_J = 150\text{ °C}$
Maximum output power dissipation	P_{S_O}	1380	mW	
Maximum ambient safety temperature	T_S	150	°C	$T_S = T_{J,max}$

4 Timing diagrams

Figure 3 illustrates the input-to-output propagation delays as observed at the capacitively loaded output.

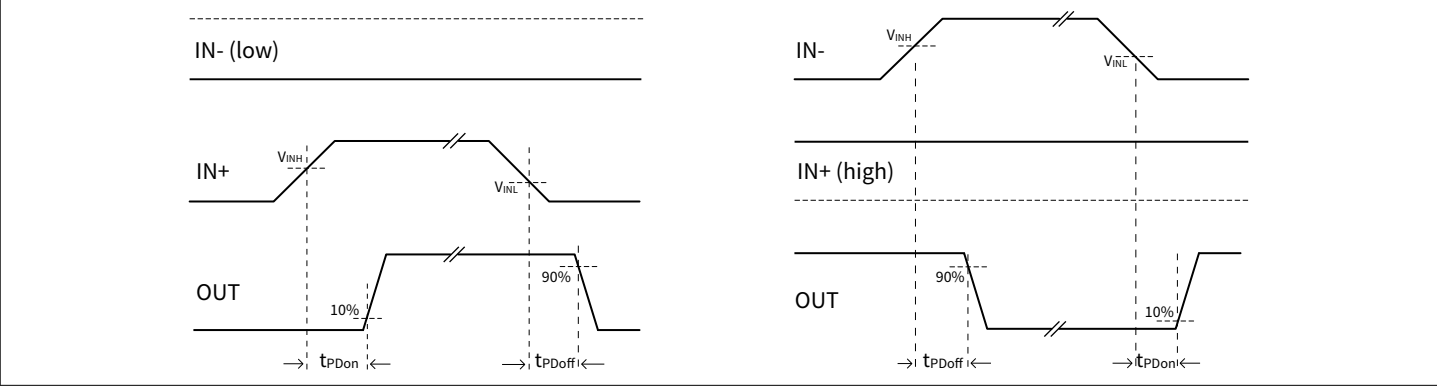


Figure 3 Input-to-output propagation delays (inverting and non-inverting case)

Figure 4 illustrates the pulse width distortion. It depicts the duty cycle distortion of the signal observed at the driver output due to the mismatch between on and off propagation delay.

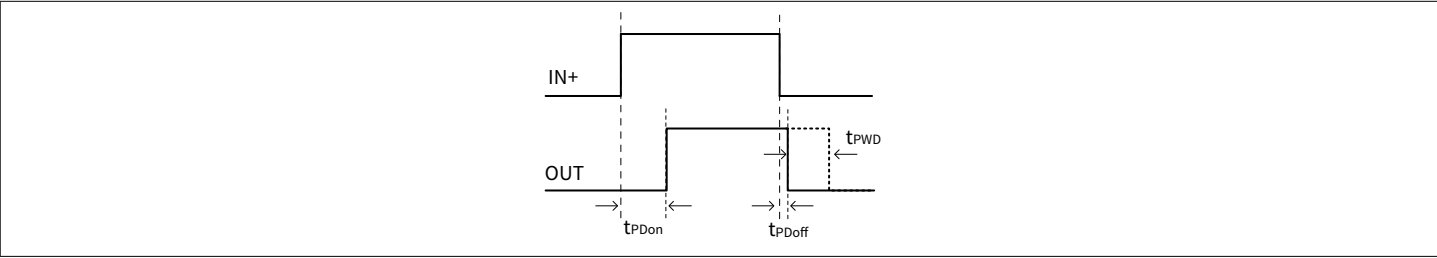


Figure 4 Pulse width distortion (unloaded output)

Figure 5 illustrates the rise and fall time as observed at the capacitively loaded output.

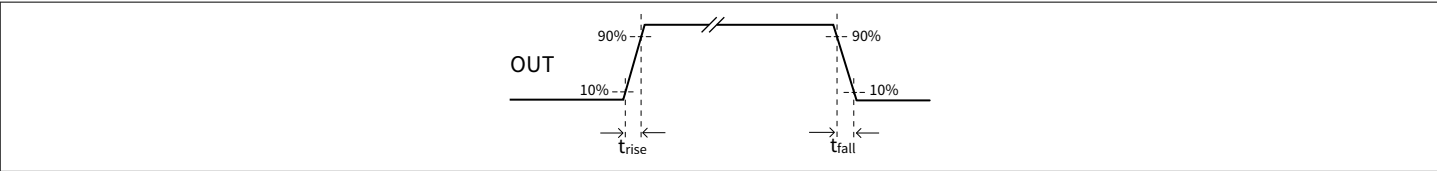


Figure 5 Rise and fall times

Figure 6 illustrates the behavior of the deglitch filter that suppresses input pulses with duration shorter than t_{PWmin} .

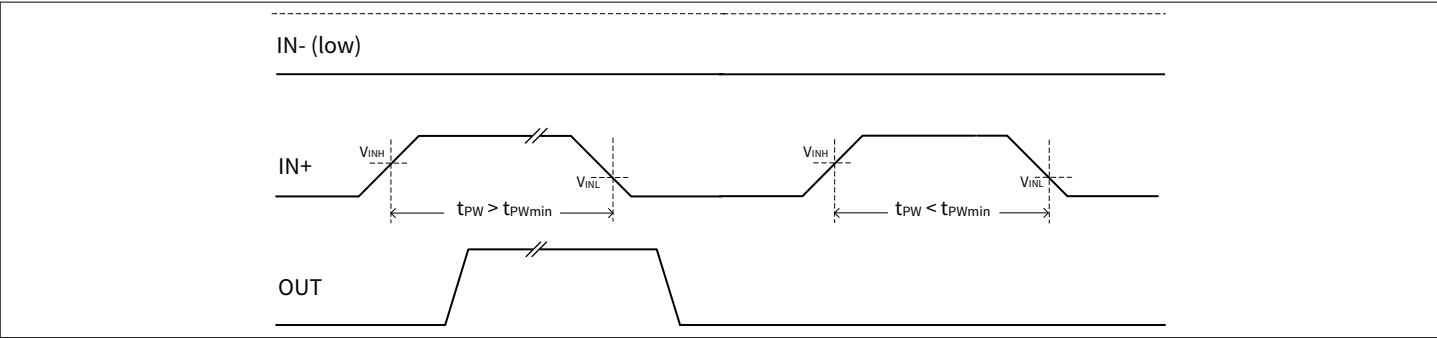


Figure 6 Minimum pulse that changes the output state

4 Timing diagrams

Figure 7 illustrates the input supply UVLO behavior. It depicts the reaction time to UVLO events when V_{DDI} crosses the UVLO thresholds during rising or falling transitions (power-up, power-down, supply noise).

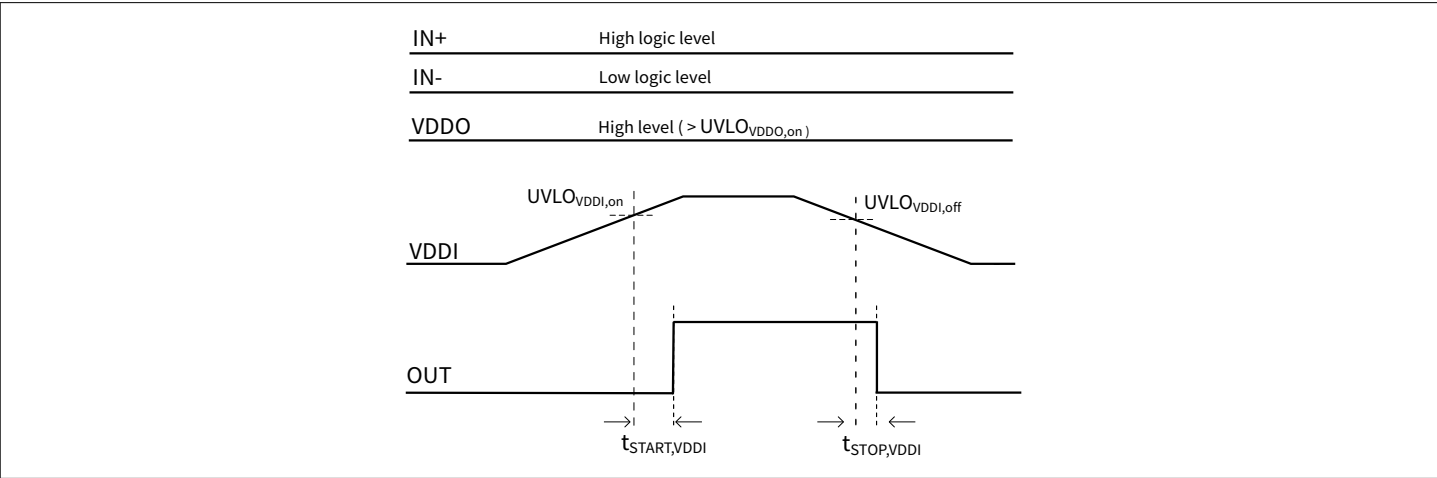


Figure 7 V_{DDI} UVLO behavior, start-up and deactivation time (unloaded output)

Figure 8 illustrates the output supply UVLO behavior. It depicts the reaction time to UVLO events when V_{DDO} crosses the UVLO thresholds during rising or falling transitions (power-up, power-down, supply noise).

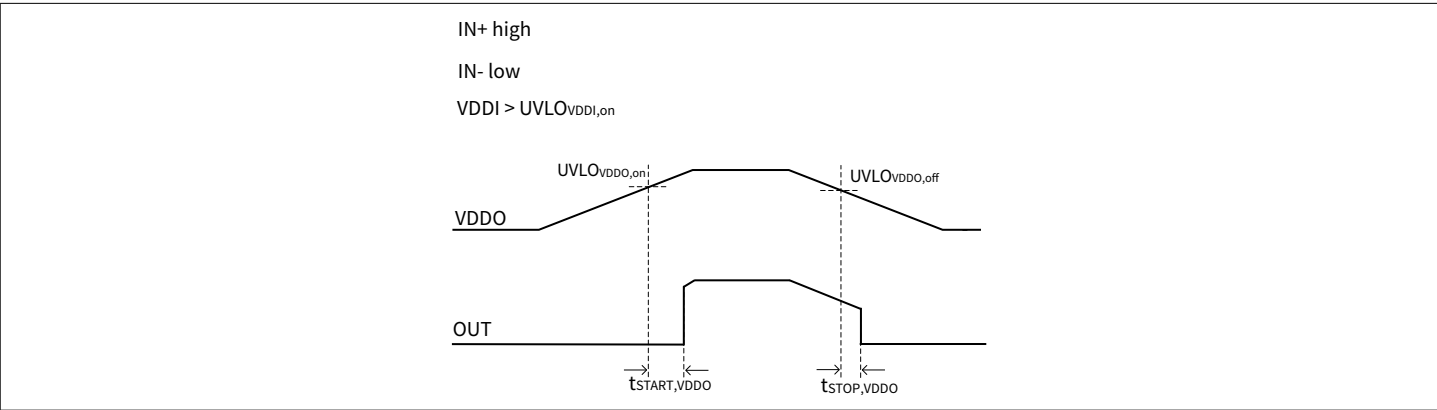


Figure 8 V_{DDO} UVLO behavior, start-up and deactivation time (unloaded output)

Figure 9 illustrates $t_{CLAMP,OUT}$, the time required to clamp potential output induced overshoots in UVLO condition ($V_{DDO} < UVLO_{VDDO,on}$).

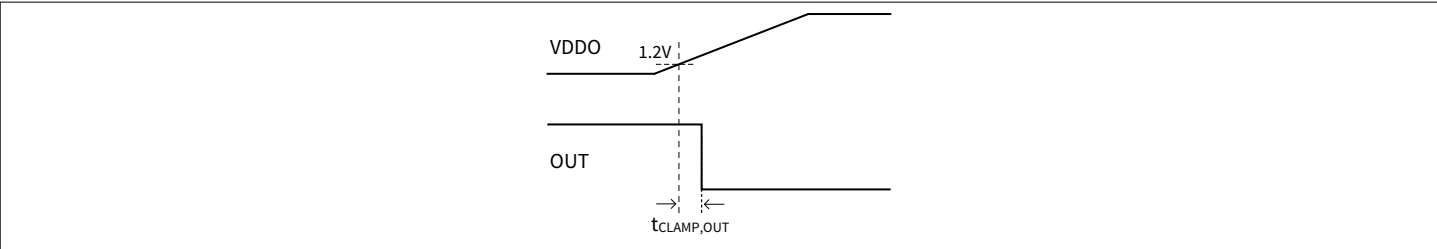


Figure 9 Activation time of output clamping in UVLO conditions (unloaded output)

5 Layout recommendation

For any fast-switching power system the PCB layout is crucial to achieve optimum performance. Among the many existing rules, recommendations, guidelines, tips and tricks, the ones of highest importance are listed as follow.

- Use low-ESR decoupling capacitance (C_{VDDI} , C_{VDDO}) and place them as close as possible to the driver to support high peak currents during switching and to ensure stable supply voltages for the driver. The use of PCB planes at ground potential is also recommended to further reduce the inductance to ground.
- Minimize the gate loop inductance by placing the driver as close as possible to the driven transistor and by ensuring that the gate traces are always placed on top of a PCB plane at ground (GNDO) potential. Minimizing the power loop inductance is the key measure to limit voltage overshoots and enable fast switching.
- In case of bootstrapping, minimize the bootstrap loop inductance to ensure reliable operation and fast bootstrap charge. The bootstrap capacitor is, in fact, charged every cycle through the bootstrap diode and the turned-on low-side transistor and the loop is subject to potential high peak charging currents. When this is not possible, use a split bootstrap capacitor with one part placed in some distance of the driver to avoid induced noise; if big enough, this acts as a stable supply for the high-side driver decoupling capacitance (placed close to the driver).
- Pay attention to keep any source of noise (like half-bridge high-current switching traces) away from the driver to avoid any coupling capacitance.
- According to the application requirements, pay attention to keep the needed input-to-output clearance and creepage on PCB level. To fully benefits from the isolation capabilities of the driver, any trace or plane below the device must be strictly avoided.
- Connect the driver ground pin to proper PCB planes to reduce the junction-to-board resistance and support the spread of heat outside the driver

A layout recommendation for EiceDRIVER™ 1EDBx275F is given in [Figure 10](#).

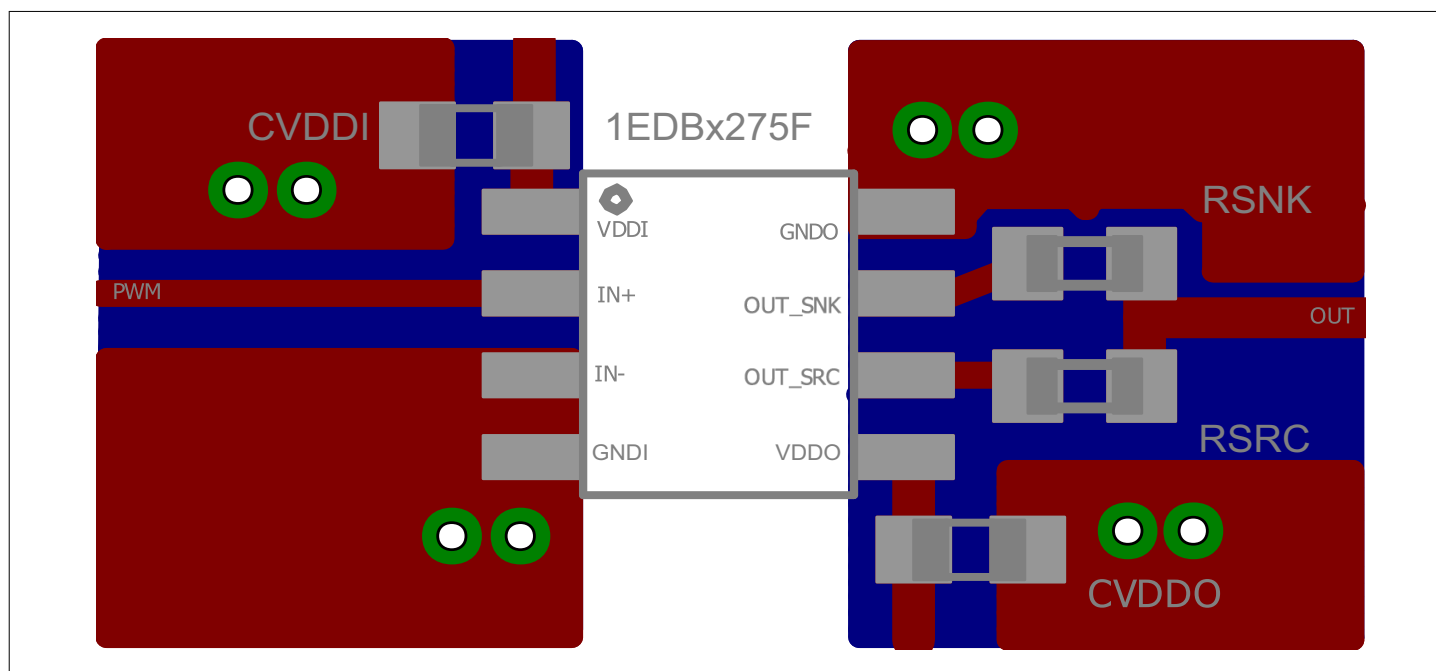


Figure 10 Layout recommendation

Due to the input-to-output isolation, EiceDRIVER™ 1EDBx275F is best suited for use as high-side driver. In particular, the combination with EiceDRIVER™ 1EDN9550B (single-channel gate driver with true differential inputs), is best suited for half-bridge driving due to perfect matching in timing performances and output capability. By making use of the drivers inverting and non-inverting inputs, shoot-through protection can be implemented as depicted in Figure 11; any undesired overlap of low-side and high-side PWM signals is not propagated at the transistors input. This solution is preferable compared to dual-channel gate drivers in case of high-power or high-frequency designs; here minimizing the gate loop may become a critical requirement that can be more easily fulfilled by using single-channel solutions.

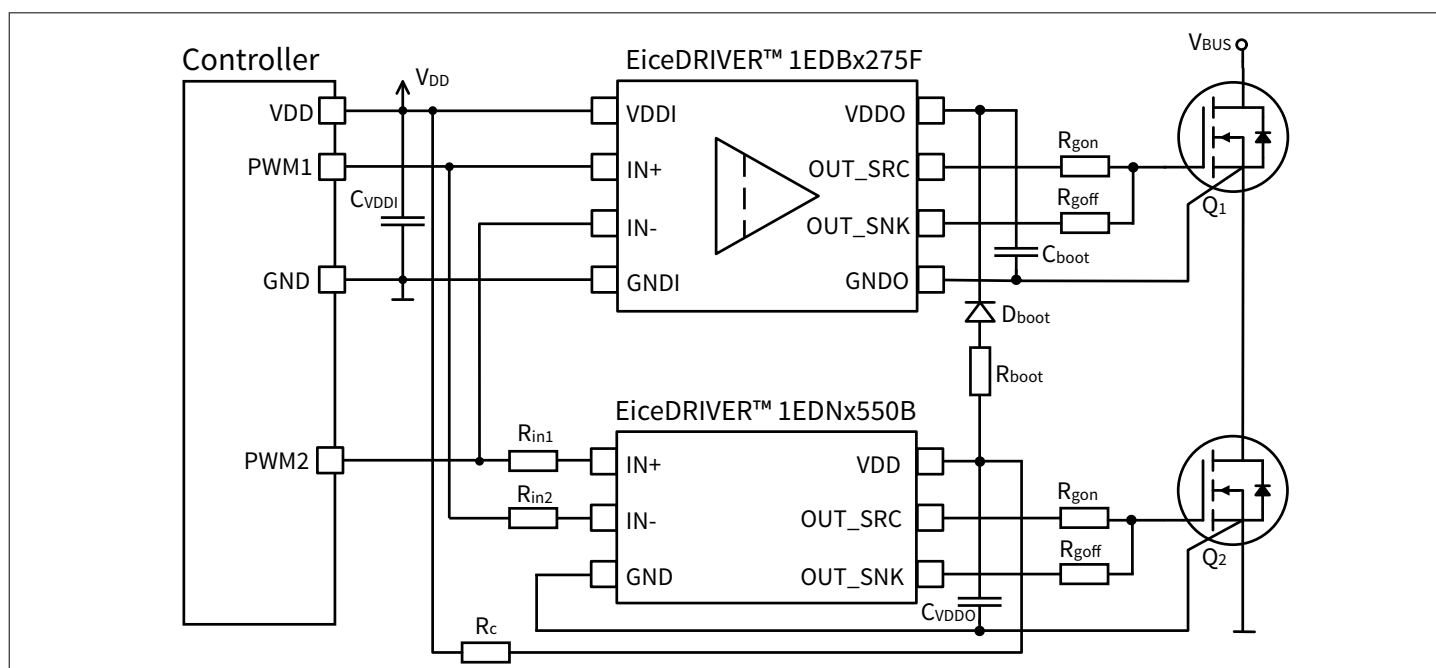


Figure 11 Typical application circuit for half-bridge driving

6.1 Driving 600 V CoolGaN™

Figure 12 depicts a 1EDB7275F typical use case driving Infineon's 600V GaN power switches (CoolGaN™). The example shows a soft-switching topology; here, due to acceptable switching speed, unipolar driving is possible without risk of false triggering of the devices due to switching induced overshoots.

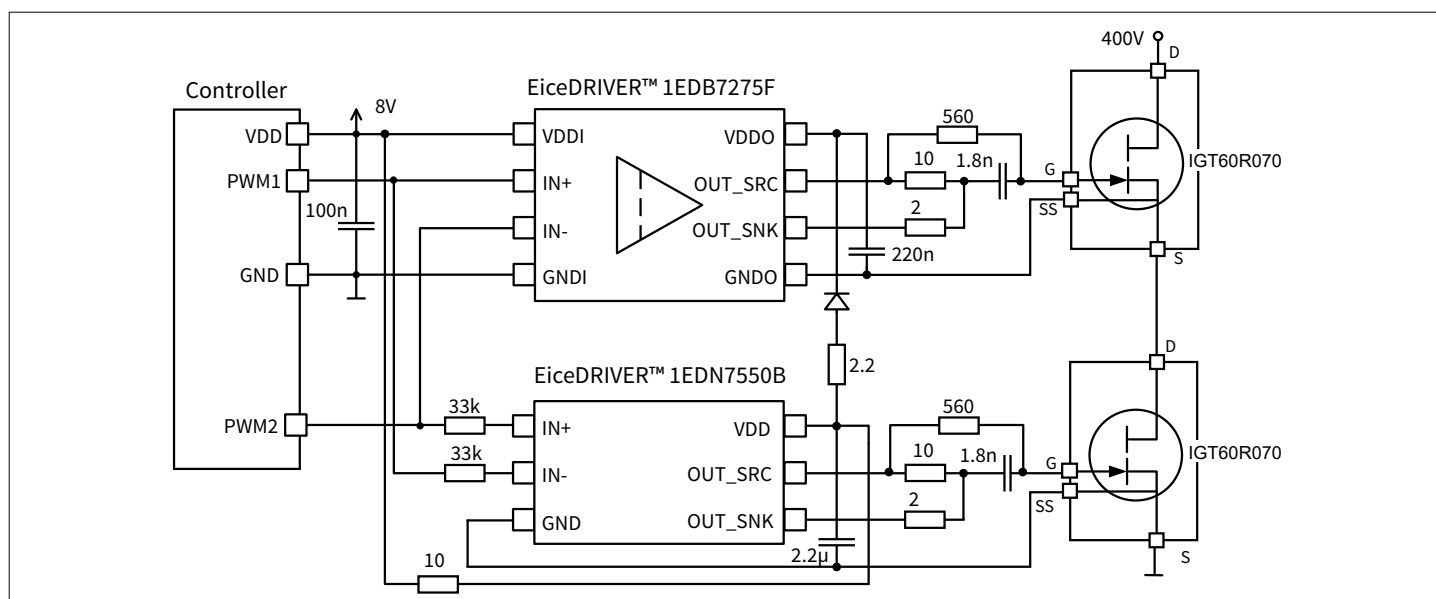


Figure 12 Typical application circuit for 600 V CoolGaN™ driving

6.2 Driving 650 V CoolSiC™

Figure 13 depicts a typical use case for Infineon's 650 V SiC MOSFETs (CoolSiC™) in a so-called "totem-pole" PFC. It consists of a 48 mΩ SiC half-bridge driven by 1EDB9275F and 1EDN9550B EiceDRIVER™ the diode functions indicated in the power path are usually realized with low- $R_{DS(on)}$ MOSFETs operating as synchronous rectifiers. 3.3 kW of power can be handled at very high efficiency (above 99%).

Considering a typical 18 V gate-to-source voltage driving, 1EDB9275F and 1EDN9550B EiceDRIVER™ offer an output UVLO level fitting for 650 V CoolSiC™. With a typical $UVLO_{VDDO,off}$ of 14.4 V, these drivers ensure that even in an unsupplied case the transistor (e.g. IMZA65R048M1H in a 3.3 kW totem-pole PFC) stays within the Safe Operating Area (SOA) with acceptable power dissipation.

In Figure 13 a Schottky diode at the CoolSiC™ gate is recommended to clamp switching induced undershoots on the gate terminal which may cause a potential drift in the gate threshold voltage $V_{gs,th}$ over lifetime.

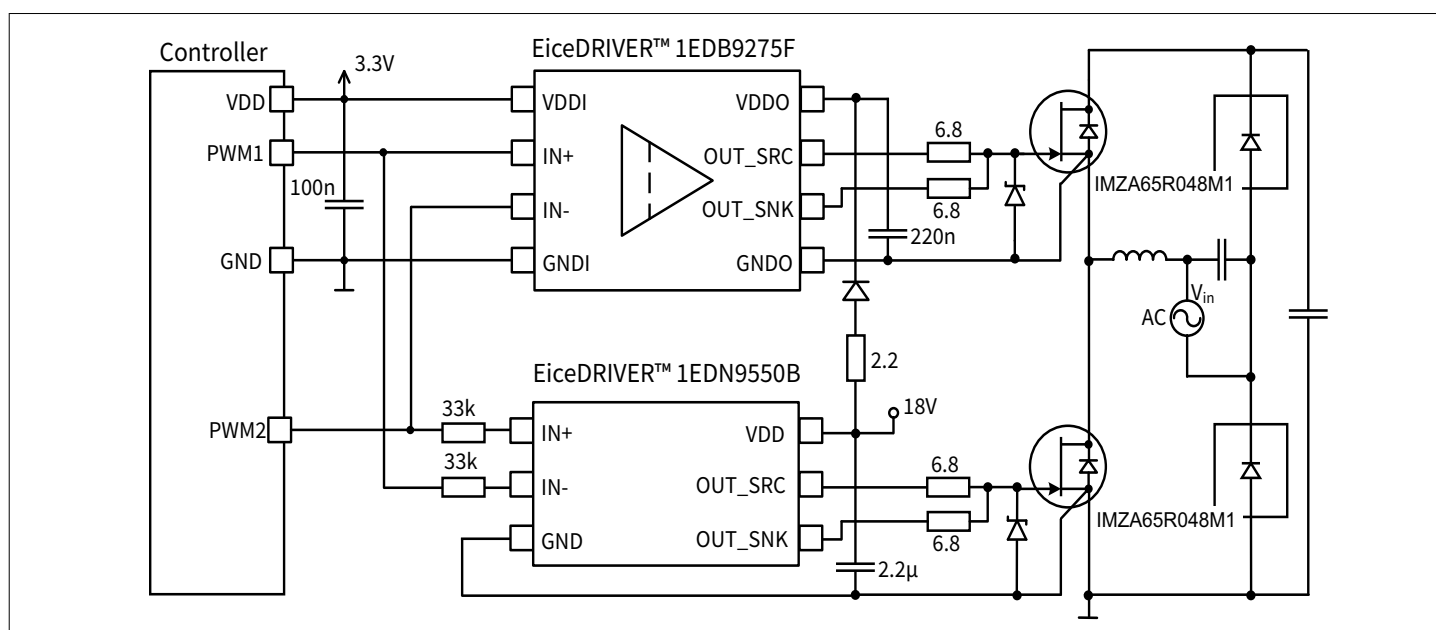


Figure 13 Typical application circuit for 650 V CoolSiC™ driving

7 Typical characteristics

$V_{DDI} = 3.3\text{ V}$, $V_{DDO} = 12\text{ V}$, $T_A = 25^\circ\text{C}$, $f_{sw} = 1\text{ MHz}$, no load unless otherwise noted.

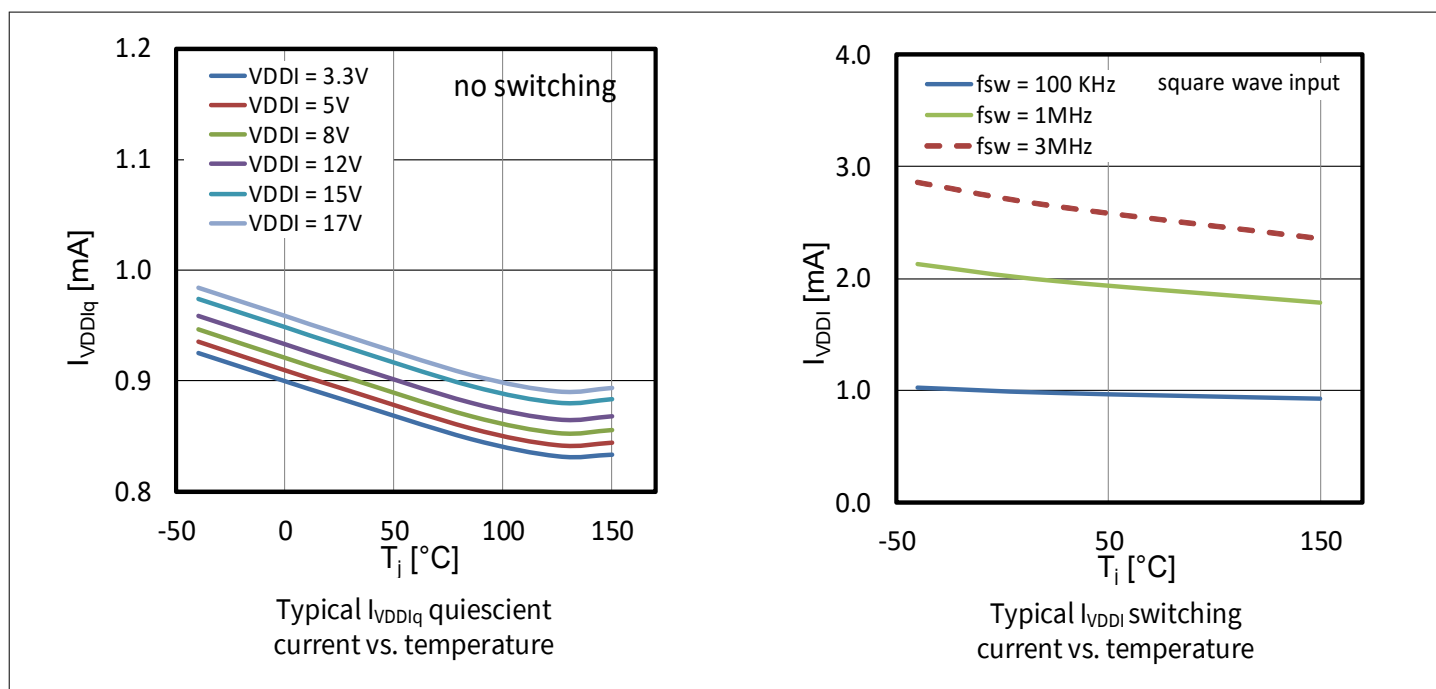


Figure 14 Input-side supply current I_{VDDI} (quiescent and switching current) with temperature

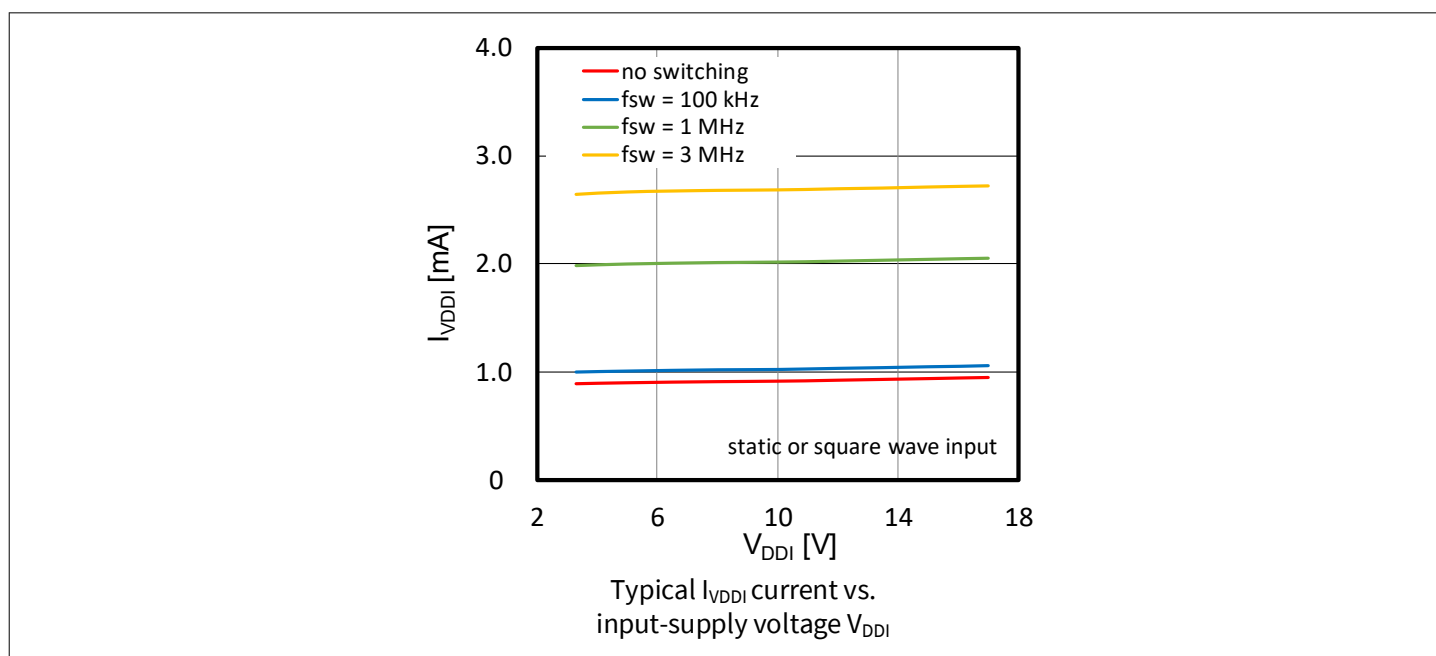


Figure 15 Input-side supply current I_{VDDI} (quiescent and switching current) with V_{DDI}

7 Typical characteristics

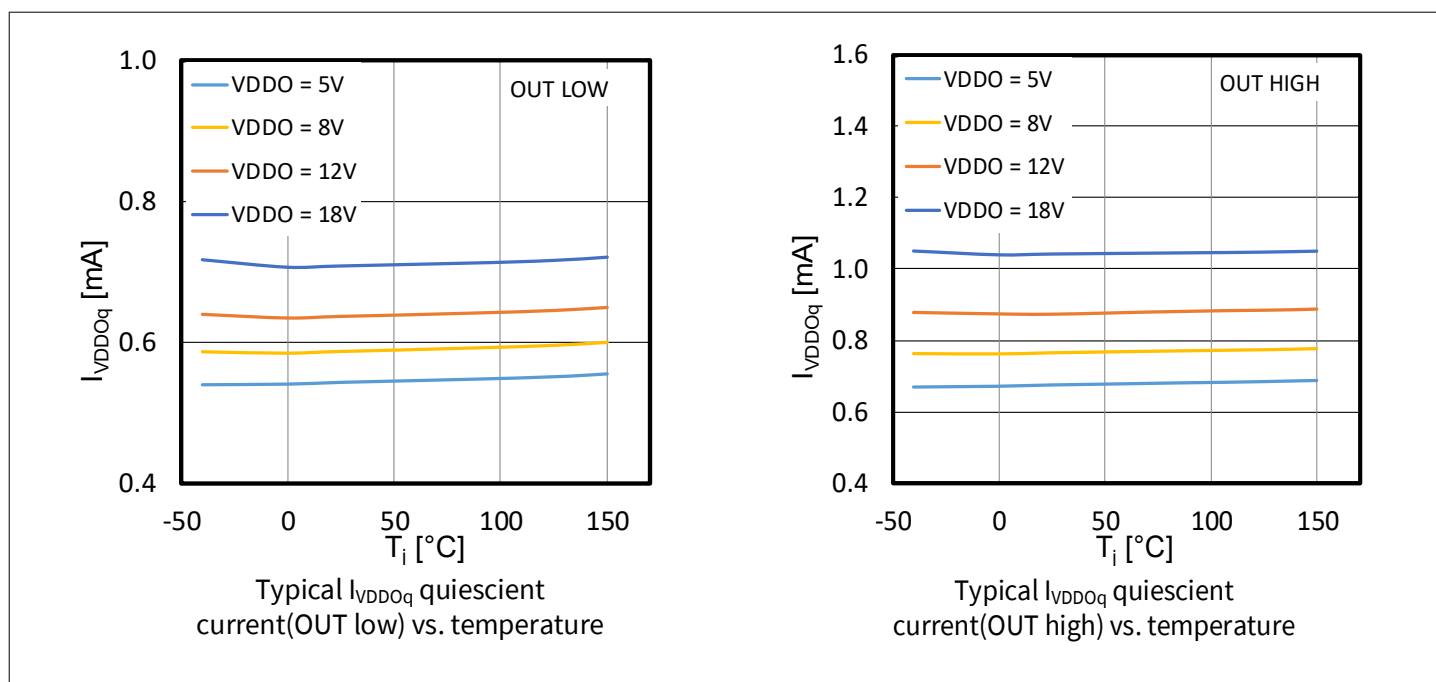


Figure 16 Output-side supply current I_{VDDOq} (quiescent current) with temperature

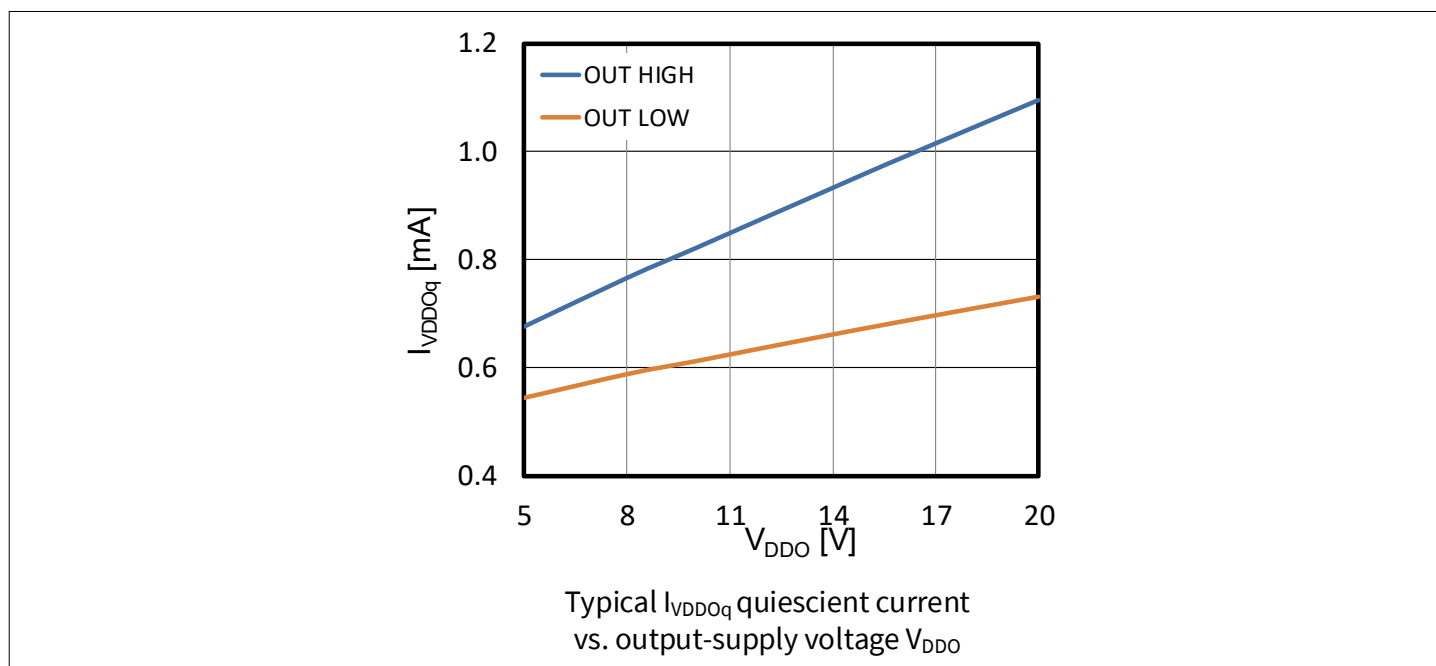


Figure 17 Output-side supply current I_{VDDOq} (quiescent current) with V_{DDO}

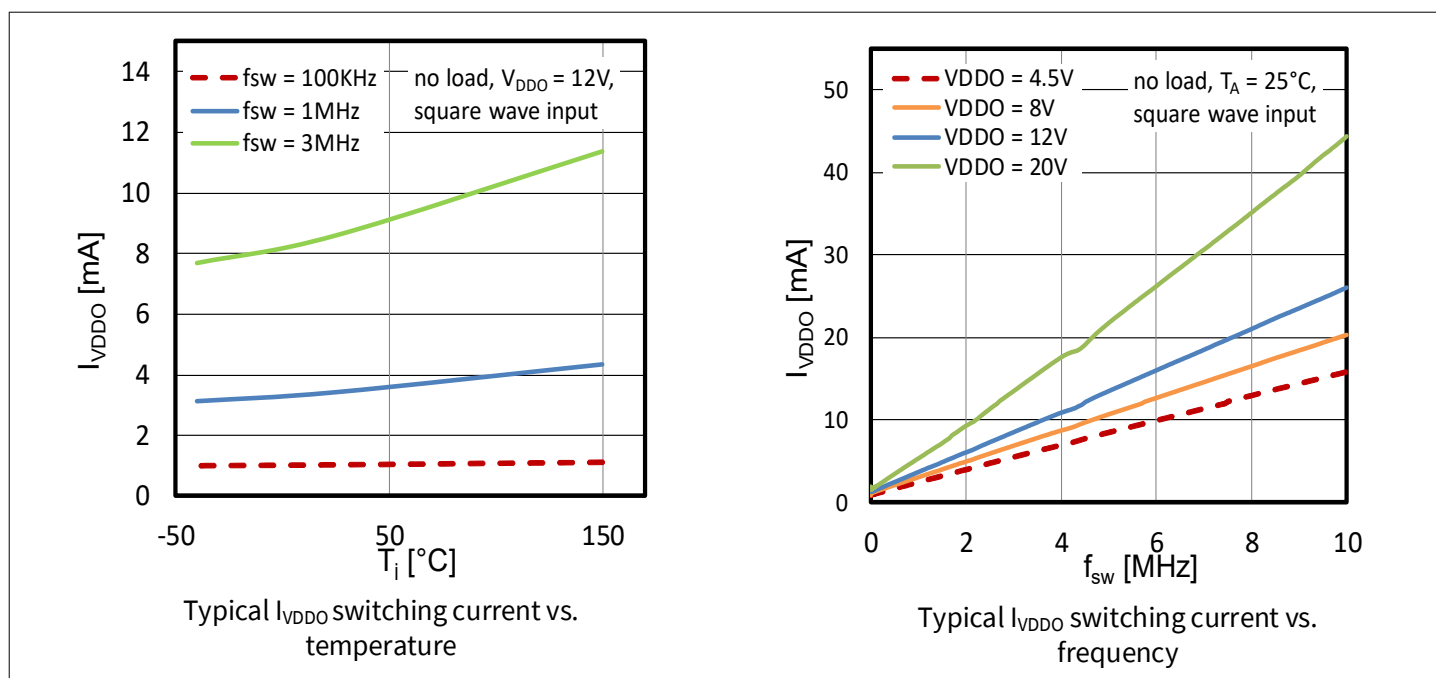


Figure 18 Output-side supply current I_{VDDO} (switching current without load) with temperature

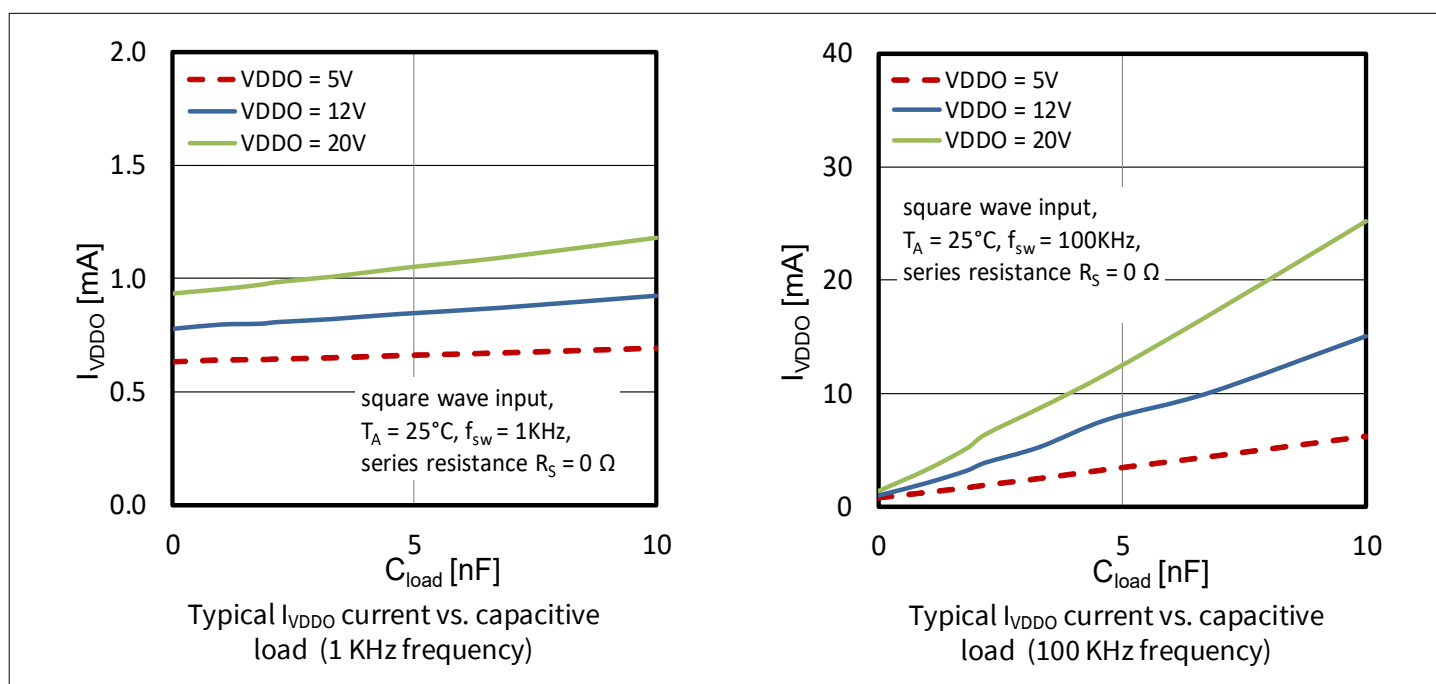


Figure 19 Output-side supply current I_{VDDO} (switching current with load) with temperature

7 Typical characteristics

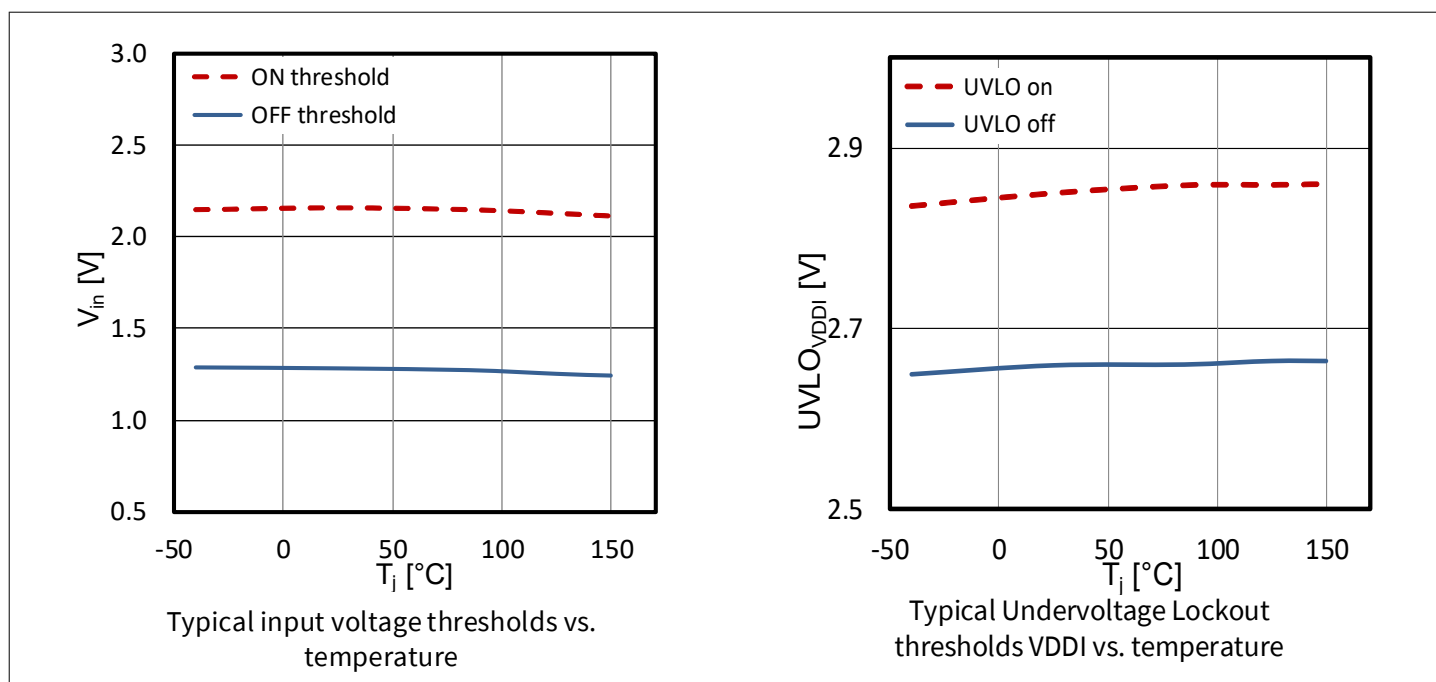


Figure 20 Logic input thresholds and V_{DDI} UVLO thresholds with temperature

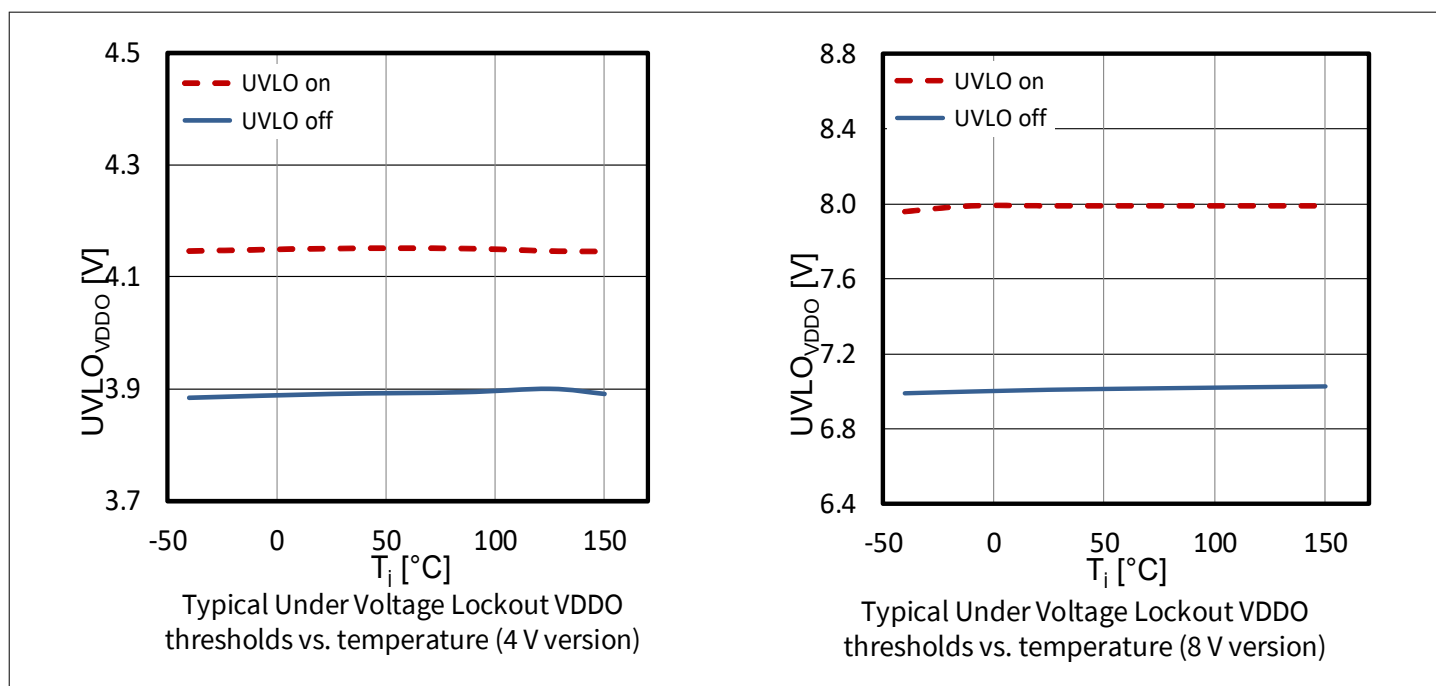


Figure 21 V_{DDO} UVLO thresholds (4 V, 8 V options) with temperature

7 Typical characteristics

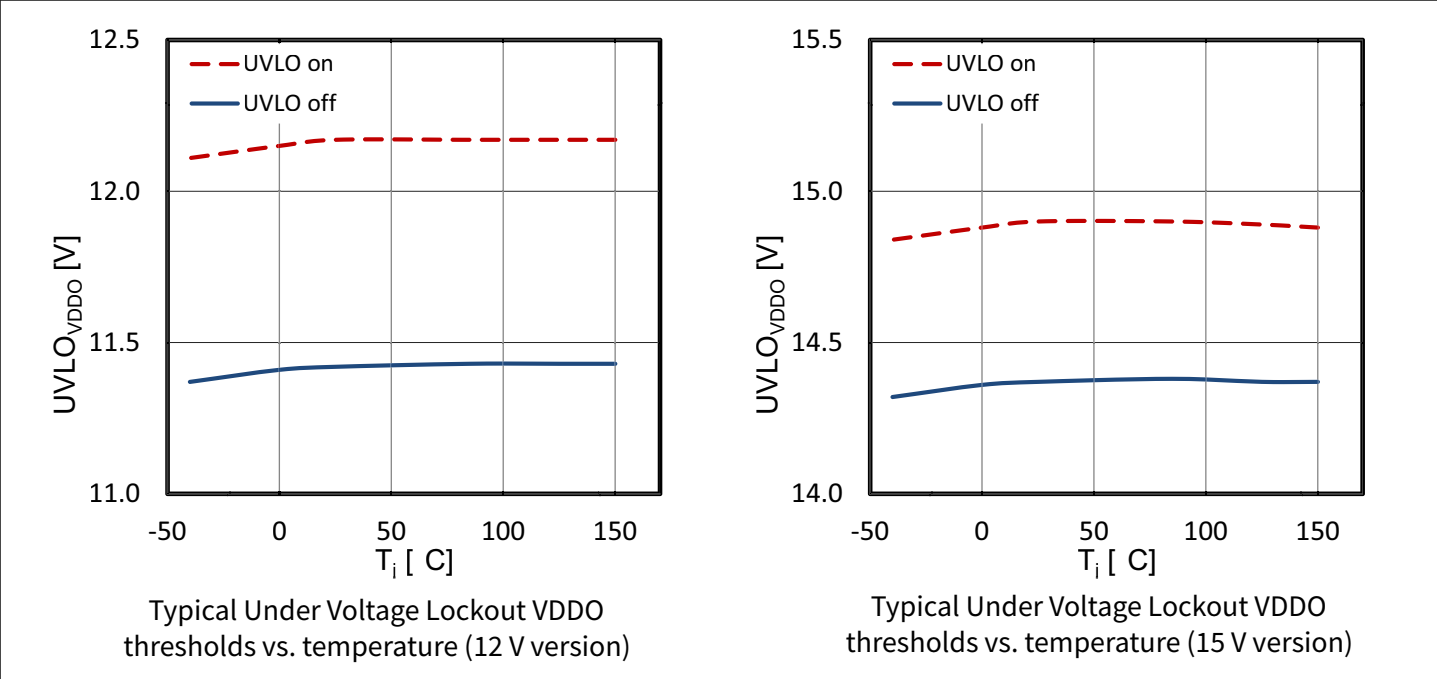


Figure 22 V_{DDO} UVLO thresholds (12 V, 15 V options) with temperature

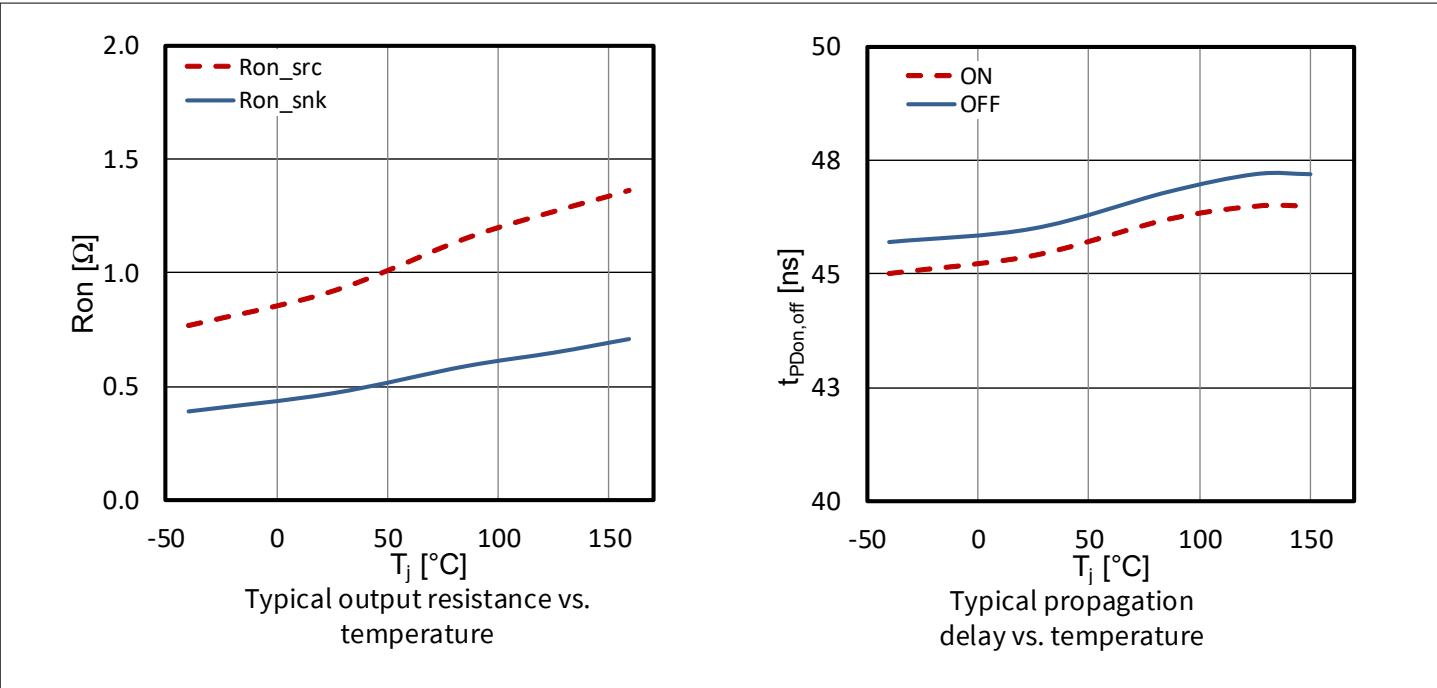


Figure 23 Output resistance and propagation delay with temperature

7 Typical characteristics

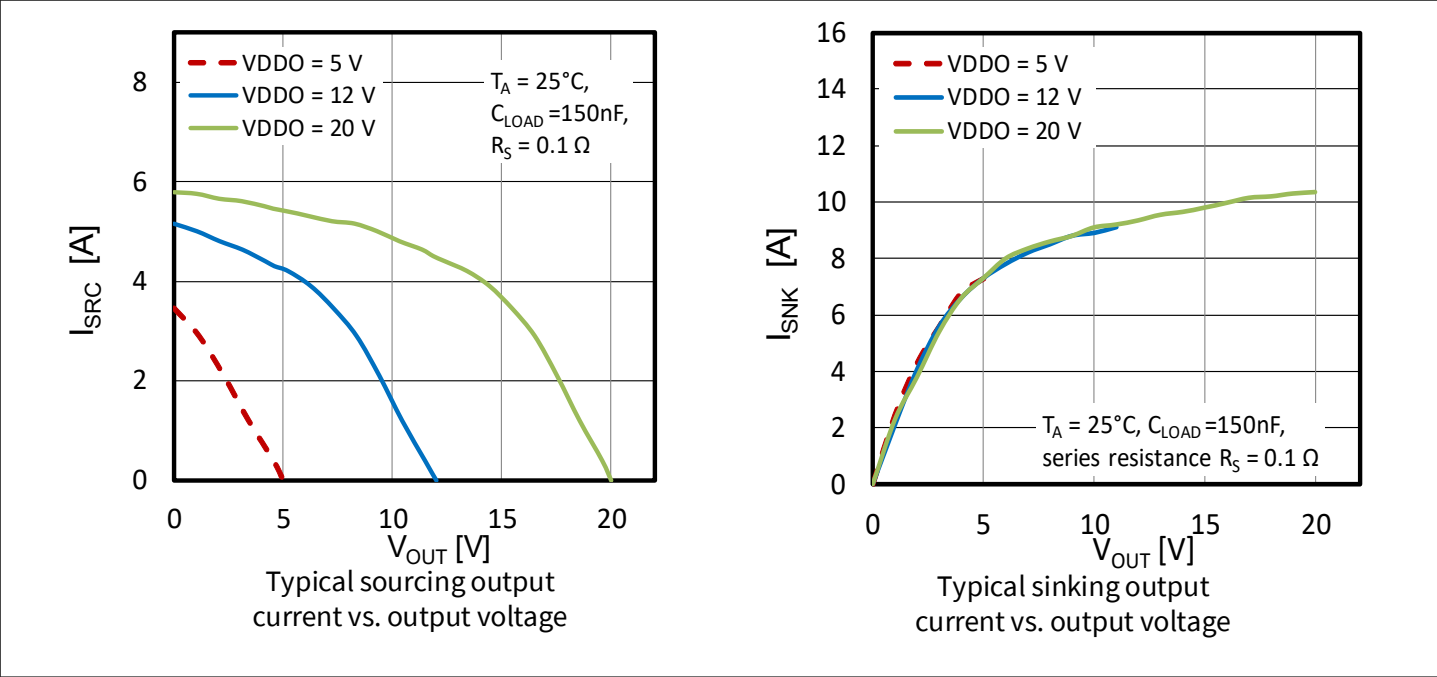


Figure 24 Source and sink current with output voltage

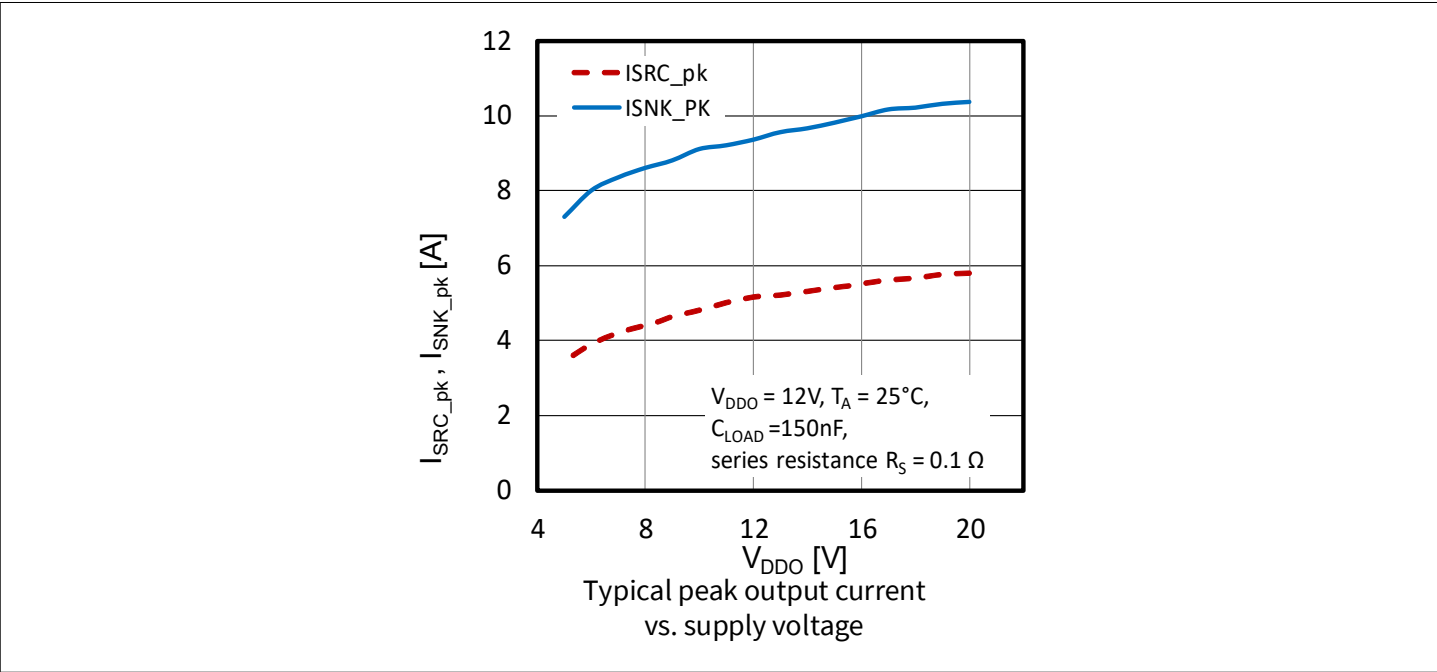


Figure 25 Peak source and sink current with supply voltage

7 Typical characteristics

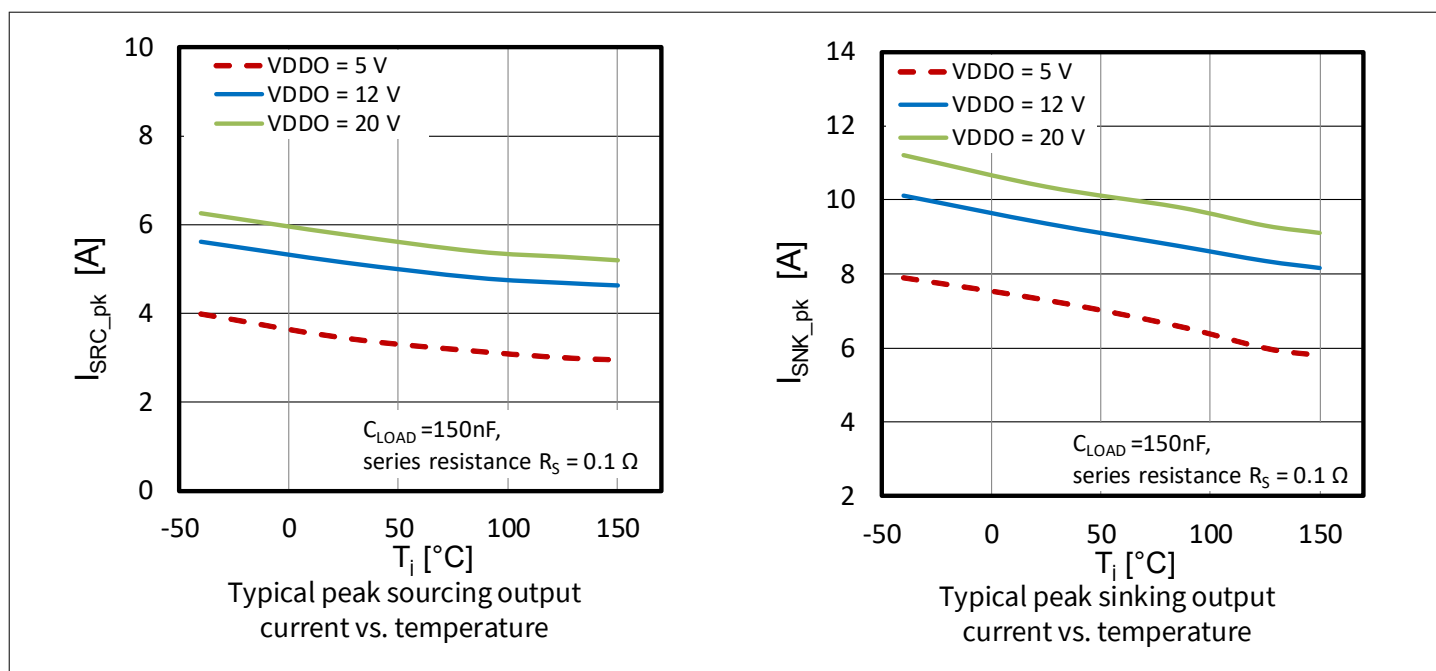


Figure 26 Peak source and sink current with temperature

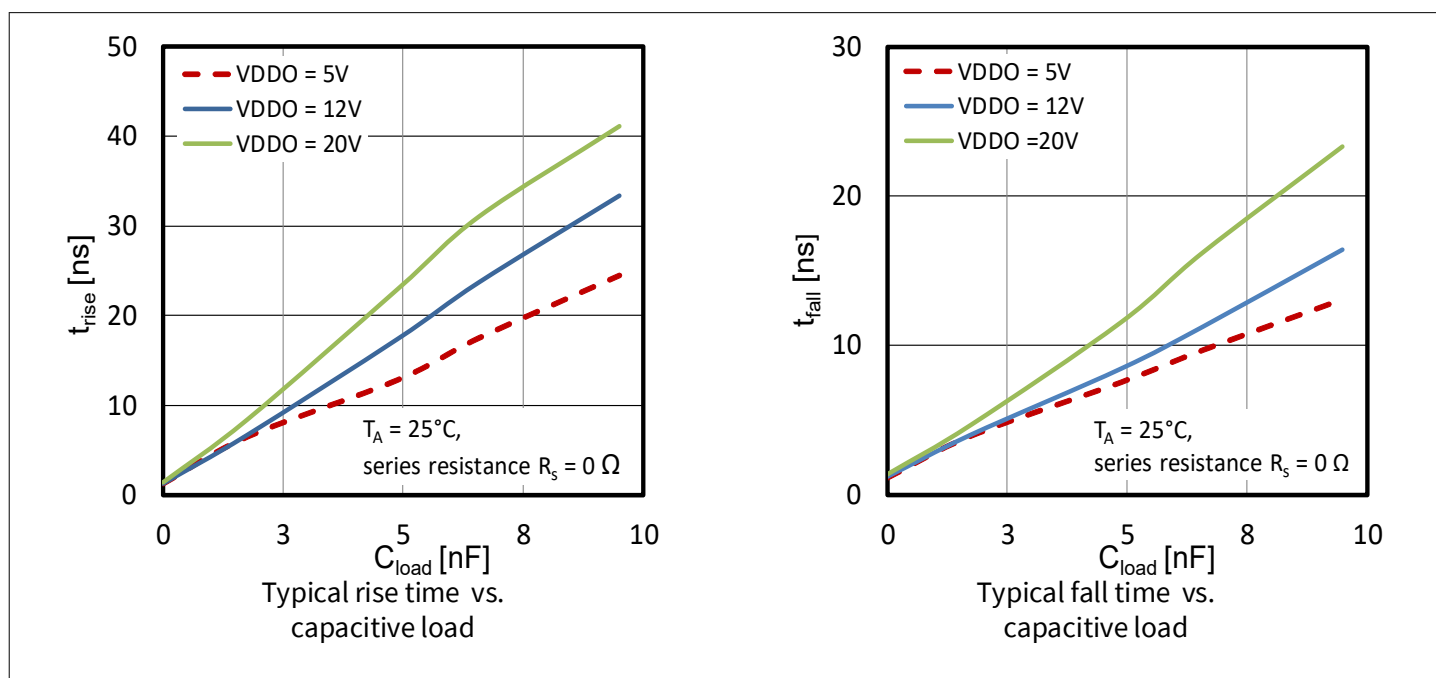


Figure 27 Rise and fall times with capacitive load

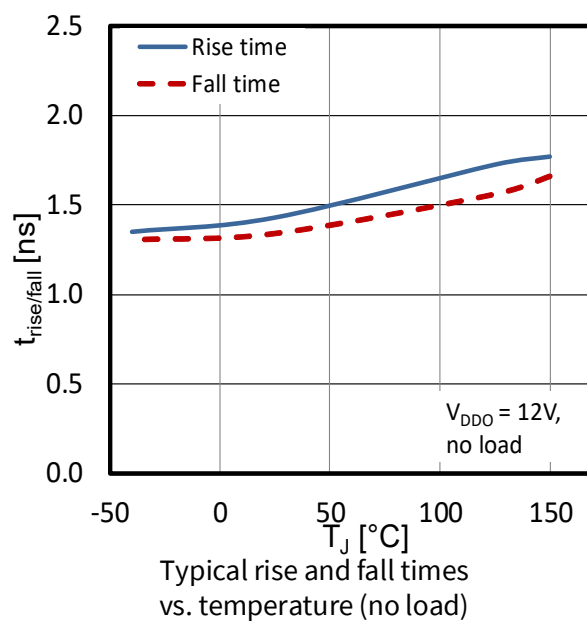


Figure 28 Rise and fall times with temperature

8 Package outline dimensions

8.1 Device numbers and markings

Table 21 Device numbers and markings

Part number	Orderable part number (OPN)	Device marking
1EDB6275F	1EDB6275FXUMA1	1B6275A
1EDB7275F	1EDB7275FXUMA1	1B7275A
1EDB8275F	1EDB8275FXUMA1	1B8275A
1EDB9275F	1EDB9275FXUMA1	1B9275A

8.2 Package PG-DSO-8

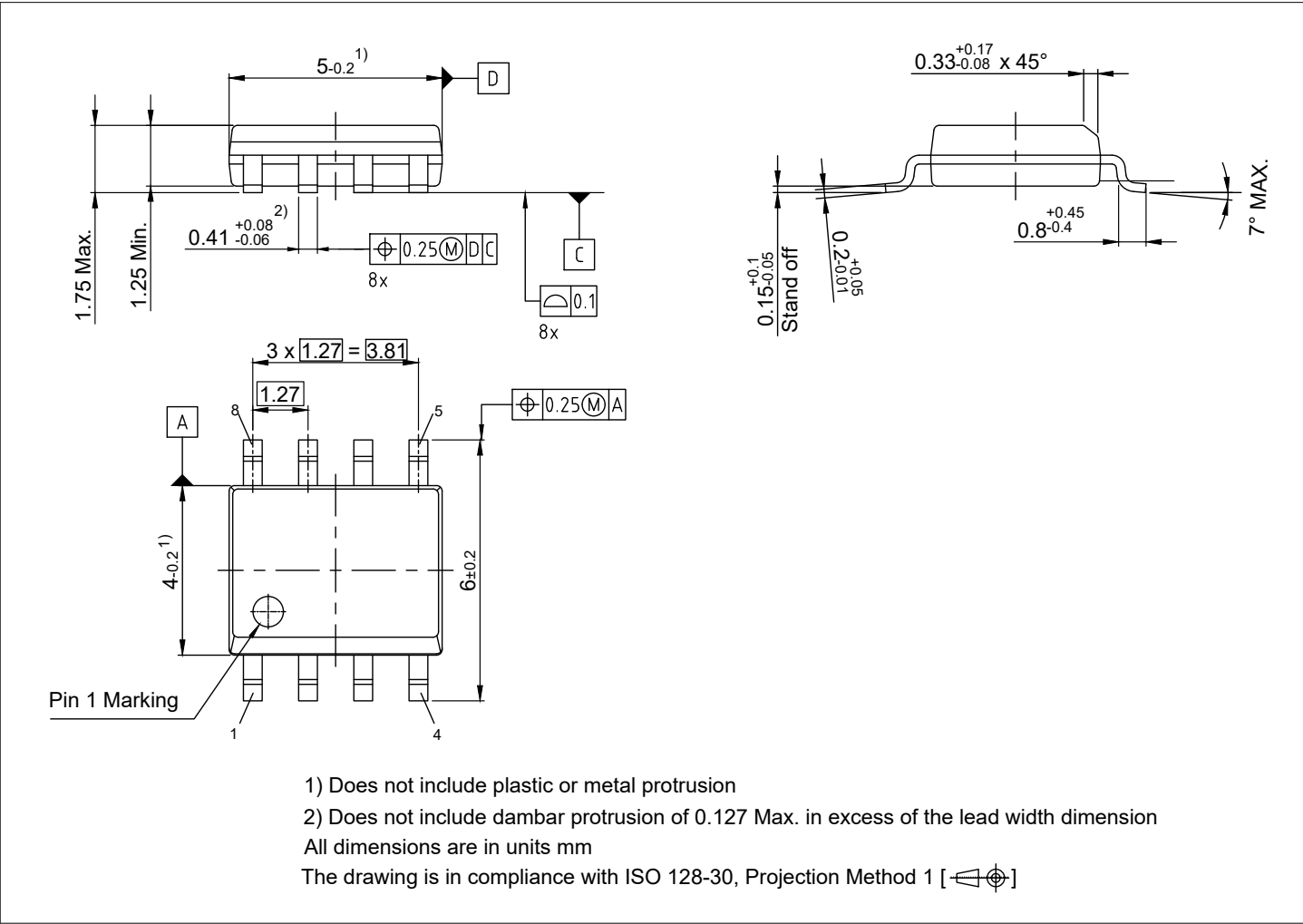


Figure 29 PG-DSO-8 outline

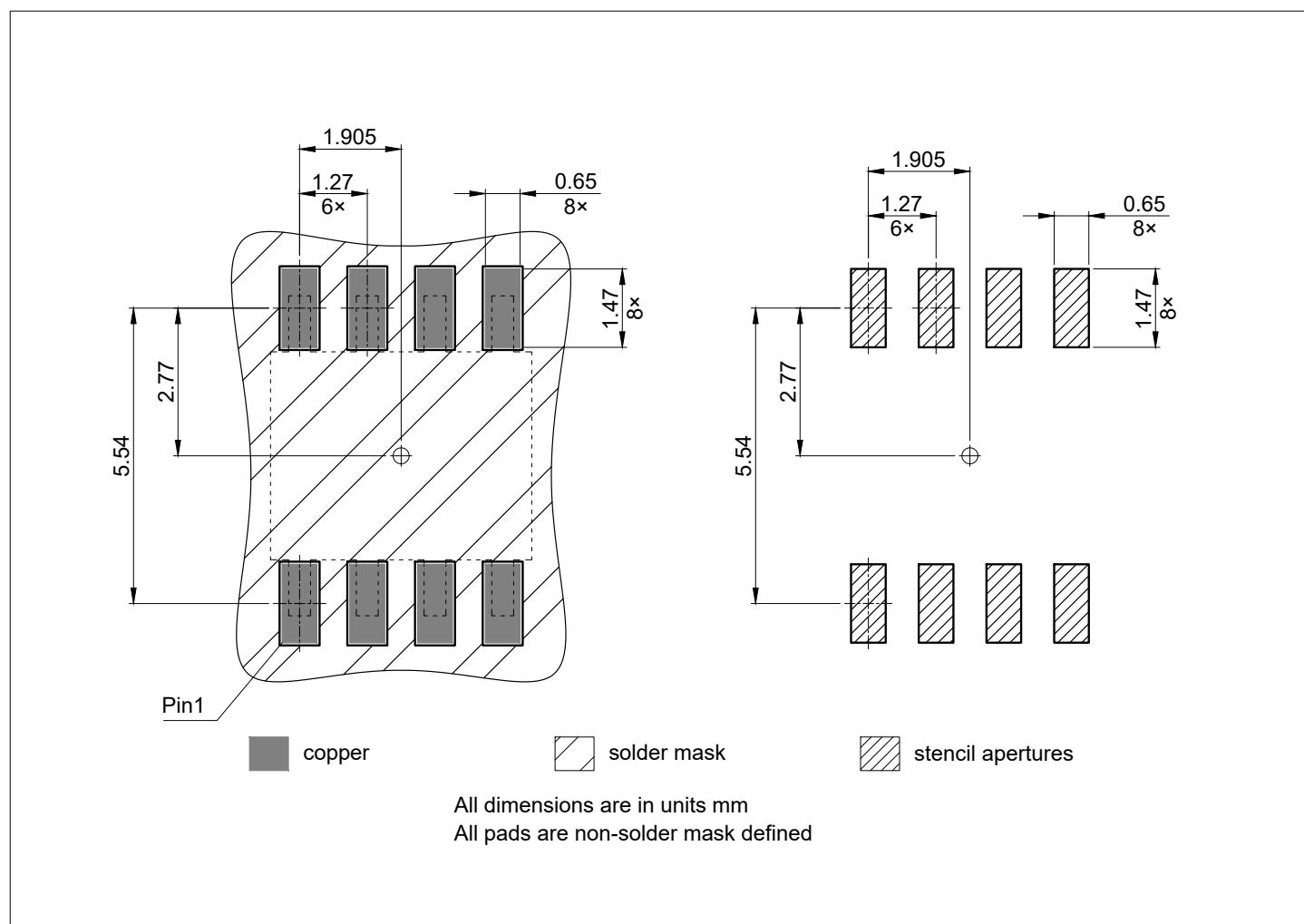
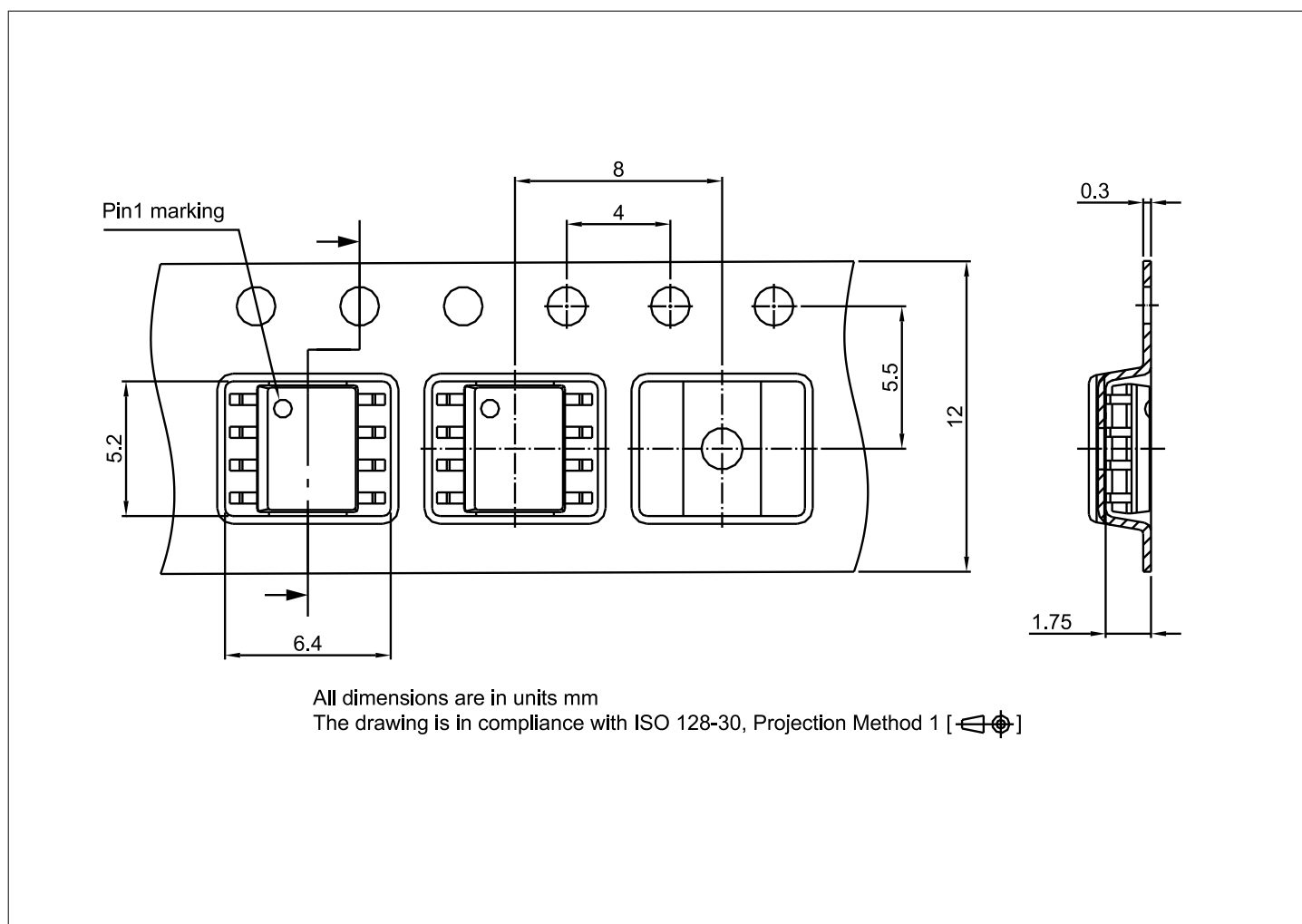


Figure 30 **PG-DSO-8 footprint**

**Figure 31 PG-DSO-8 packaging****Green Product (RoHS-compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

<https://www.infineon.com/packages>

Revision history

Document version	Date of release	Description of changes
Rev.2.4	2026-10-15	Front cover: Isolation certificates added
Rev.2.3	2025-10-23	- Template update and editorial changes - Table 19: Updated “Comparative tracking index” values - Table 19: Updated “Material group” value - Table 19: Updated VDE0884-11 → VDE0884-17 - Figure 30: Update
Rev.2.2	2021-11-04	- Front cover: Editorial updates - Table 16: Output current values are rounded - Table 8: Fixed typo (OUT does not follow V_{DDI} shape) - Figure 11: Fixed typo (OUT_SRC and OUT_SNK flipped) - Figure 14: Updated typical application circuit for 650 V CoolSiC™ updated with the new 1EDN9550B EiceDRIVER™ to drive the low-side MOSFET - Figure 15: Added new V_{DDI} data points for typical input-side quiescent current I_{VDDIq} vs. temperature - Figure 16: Added typical input-side current I_{VDDI} vs. V_{DDI} - Figure 17: Added new V_{DDO} data points for typical output-side quiescent current I_{VDDOq} vs. temperature - Figure 18: Added typical output-side quiescent current I_{VDDOq} vs. V_{DDO}
Rev.2.1	2021-04-21	- Whole document: Removed “UL1577 certification pending” because certification has been issued - Table 1; Table 3; Table 21: Added 1EDB6275F 12 V UVLO variant - Table 1; Table 21: Modified UVLO values for 1EDB9275F - Table 7: Fixed typo in R_{thJB25} - Table 17: Increased propagation delay max (49 ns → 51 ns) - Table 19: Added pollution degree, climatic category and emulated VDE0884-11 parameters - Table 20: Added safety limiting values table - Table 23: Updated VDDO UVLO vs. temperature graph for 1EDB9275F, added graph for 1EDB6275F
Rev.2.0	2020-04-08	Final datasheet created

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