EiceDRIVER™ 1ED301xMC12I Opto-emulator gate driver IC

Datasheet

Technical documents
Kits and boards
Support

1ED3010MC12I, 1ED3011MC12I, 1ED3012MC12I

Single-channel isolated gate driver IC with opto-emulator input

Features

- Single-channel isolated gate driver with opto-compatible input
- Pin-to-Pin compatible, drop-in replacement and upgrade for opto-isolated gate drivers
- For use with IGBTs, Si and SiC MOSFETs
- Up to 6.5 A typical peak output current
- Pure-PMOS sourcing stage for optimal turn-on efficiency
- 40 ns propagation delay with 10 ns part-to-part matching (skew)
- 17 ns part to part matching for complementary edges (skew+)
- 35 V absolute maximum output supply voltage
- High common-mode transient immunity CMTI > 300 kV/µs
- Single output with active shutdown and short circuit clamping
- Galvanically isolated coreless transformer gate driver
- Suitable for operation at high ambient temperature and in fast switching applications
- Safety certification:
  - UL 1577 (File E311313) with $V_{\mathrm{ISO,test}}$ = 6840 V (rms) for 1 s, V_{ISO} = 5700 V (rms) for 60 s
  - Reinforced insulation according to IEC 60747-17 (planned) with V_{IORM} = 1767 V (peak)

✓ RoHS

Green

Potential applications

- Industrial motor drives
- EV charging
- Energy storage systems
- Solar inverters
- Server and telecom switched mode power supplies (SMPS)
- UPS-systems
- Commercial air-conditioning (CAC)
- High voltage DC-DC converter and DC-AC inverter

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22, and J-STD-020.

Description

The 1ED301xMC12I gate driver ICs are opto-compatible, galvanically isolated single channel gate drivers for IGBT, Si or SiC MOSFET in LDSO-6 300 mil package. They provide a typical output current of up to 6.5 A.

The exceptional common mode transient immunity, low propagation delay with outstanding part-to-part skew and very small pulse width distortion are performance parameters vastly above those of standard opto-coupler based gate drivers. This makes these gate drivers a perfect fit for high performance applications using SiC MOSFETs, while pin-to-pin compatibility offers a simple alternative in IGBT applications with increased reliability.

Data transfer across the isolation barrier is realized by the coreless transformer technology. All variants have output undervoltage lockout (UVLO) and active shutdown.

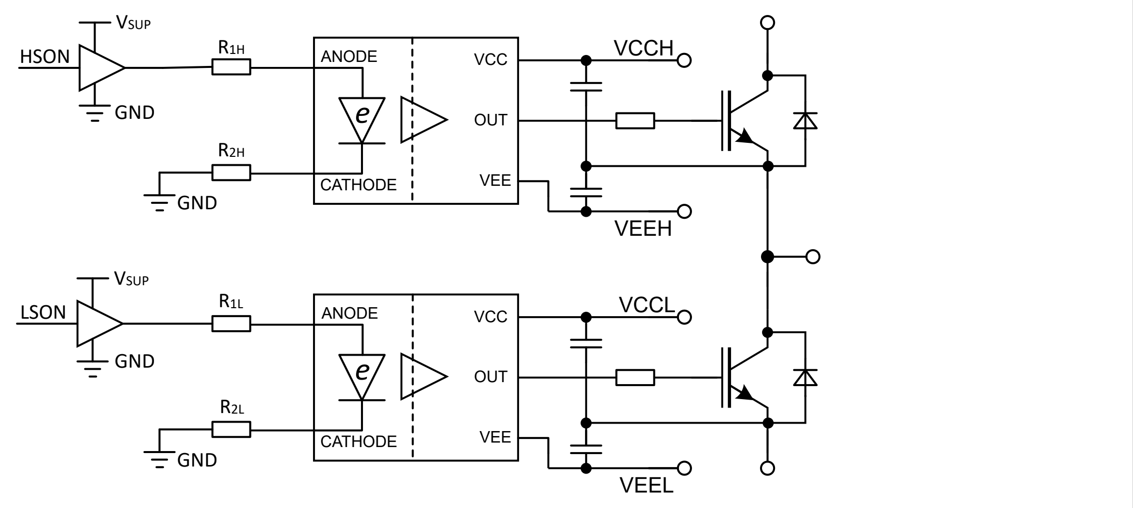

Table 1 **Ordering information**

Product type	Typical UVLO (V_{UVLOL2}/V_{UVLOH2})	Typical output current source/sink	UL 1577 Certification	IEC 60747-17 Certification	Package marking
1ED3010MC12I	8.5 V/9.3 V	6 A/6.5 A	File E311313	planned	13010MC12I
1ED3011MC12I	11.0 V/12.0 V	6 A/6.5 A	File E311313	planned	13011MC12I
1ED3012MC12I	12.5 V/13.6 V	6 A/6.5 A	File E311313	planned	13012MC12I

Table 2 **Related evaluation board**

Board name	Gate driver	Power transistor	Short description
EVAL-1ED3012MC12I-SIC	1ED3012MC12I	IMZC120R017M2H	Half-bridge evaluation board with 1ED3012MC12I gate drivers paired with IMZC120R017M2H CoolSiC™ in TO247-4 package

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1 Block diagram reference

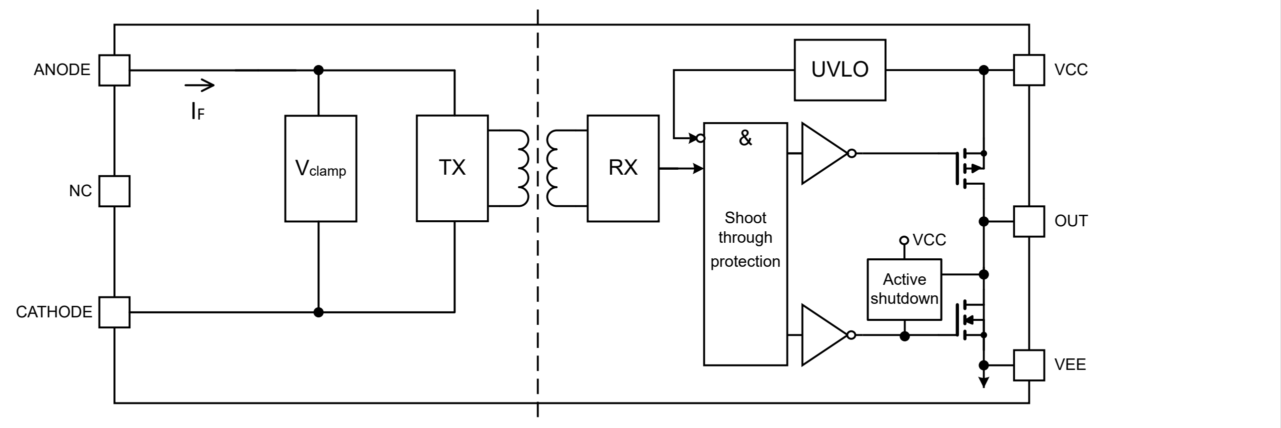


Figure 1 Block diagram

2 Pin configuration and description

Pin configuration

Table 3 **Pin configuration**

Pin No.	Name	Function
1	*ANODE*	Anode connection of opto-emulator input
2	*NC*	Not connected
3	*CATHODE*	Cathode connection of opto-emulator input
4	*VEE*	Output side ground
5	*OUT*	Driver output
6	*VCC*	Positive power supply output side

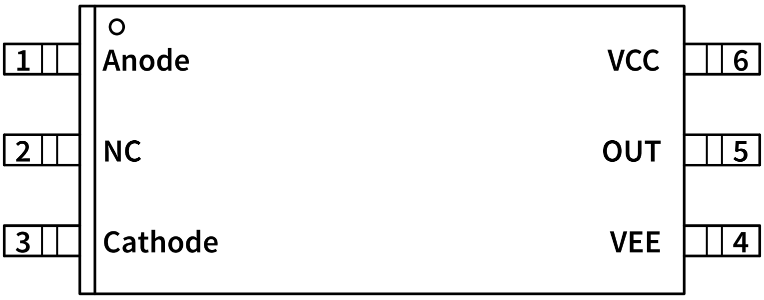


Figure 2 **LDSO-6 300 mil (top view)**

Pin description

- *ANODE*: Anode connection of the input emulated diode. When forward current above a given threshold is flowing through this emulated diode, the OUTPUT is pulled high
- *CATHODE*: Cathode connection of the input emulated diode. When forward current above a given threshold is flowing through this emulated diode, the OUTPUT is pulled high
- *VCC*: Output positive power supply rail. Connect a decoupling capacitor from this pin to *VEE*. Use a low ESR and ESL capacitor placed as close to the device as possible
- *VEE*: Output ground. All the output side signals, *VCC* and *OUT*, are referenced to this ground. In case of a bipolar supply (positive and negative voltage referred to IGBT emitter or MOSFET source), this pin should be connected to the negative supply voltage
- *OUT*: Driver output pin used to charge and discharge the gate of the external transistor (IGBT or MOSFET). During ON-state this output is connected to *VCC*. During OFF-state this output is connected to *VEE*. This output is controlled by the current flow between *ANODE* and *CATHODE*. In case of an UVLO event *OUT* will be actively pulled low. For cases where the gate driver output is not supplied, the active shutdown circuit keeps the output voltage at a low level

3 Electrical characteristics and parameters

3.1 Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Operating the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device reliability may be affected by exposure to absolute-maximum-rated conditions for extended periods of time.

Parameter	**Symbol**	**Values**			**Unit**	**Note or condition**
		Min.	**Typ.**	**Max.**		
Average input current	$I_{F(AVG)}$			20	mA	
Peak transient input current	$I_{F(TRAN)}$			1	A	<1 µs pulse width, 300 pps
Reverse input voltage	$V_{R(MAX)}$			18	V	
Power supply output side voltage	V_{VCC}	-0.3		35	V	V_{VCC} - V_{VEE}
Gate driver output voltage	V_{OUT}	V_{VEE} - 0.3		V_{VCC} + 0.3	V	
Input to output offset voltage	V_{OFFSET}			2300	V	1) $V_{OFFSET} = \|V_{VEE} - V_{CATHODE}\|$
ESD robustness - human body model	$\|V_{ESD,HBM}\|$			8	kV	2)
ESD robustness - charged device model	*ESD,CDM*			TC1500		3)
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{Stg}	-55		150	°C	

1) for functional operation only
2) According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor)
3) According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = test condition in volt)

3.2 Thermal parameters

Table 5 Thermal parameters

Parameter	**Symbol**	**Values**			**Unit**	**Note or condition**
		Min.	**Typ.**	**Max.**		
Power dissipation (input side)	$P_{D,IN}$			100	mW	1) 2) T_A = 85 °C
Power dissipation (output side)	$P_{D,OUT}$			380	mW	2) 3) T_A = 85 °C
Thermal resistance junction to ambient	R_{THJA}			152	K/W	2) T_A = 85 °C, $P_{D,IN}$ = 100 mW, $P_{D,OUT}$ = 380 mW
Characterization parameter junction to package top	Ψ_{Jtop}			18.3	K/W	2) T_A = 85 °C, $P_{D,IN}$ = 100 mW, $P_{D,OUT}$ = 380 mW

1) *IC input-side power dissipation is derated linearly with 6.58 mW/°C above 134.5 °C*
2) According to the JESD 51-7 standard, 2s2p and a metallization of 70 / 35 / 35 / 70 [µm]
3) *IC output-side power dissipation is derated linearly with 6.58 mW/°C above 85 °C*

3.3 Recommended operating conditions

Table 6 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power supply output side voltage	V_{VCC}	9.6		32	V	V_{VCC} - V_{VEE}, 1ED3010
Power supply output side voltage	V_{VCC}	12.35		32	V	V_{VCC} - V_{VEE}, 1ED3011
Power supply output side voltage	V_{VCC}	14		32	V	V_{VCC} - V_{VEE}, 1ED3012
Input diode forward current (Diode "ON")	$I_{F(ON)}$	5.5		15	mA	
Input voltage (Diode "OFF")	$V_{F(OFF)}$	-15		0.9	V	
Ambient temperature	T_A	-40		125	°C	
Junction temperature	T_J	-40		150	°C	

3.4 Electrical characteristics

The electrical characteristics include the spread of values over supply voltages, input currents and temperatures within the recommended operating conditions (T_J = -40 °C to 150 °C, $I_{F(ON)}$ = 5.5 mA to 15 mA, $V_{F(OFF)}$ = -15 V to 0.9 V). Electrical characteristics are tested in production at T_A = 25 °C. Typical values represent the median values measured at V_{VCC} - V_{VEE} = 15 V and T_A = 25 °C unless otherwise specified. Minimum and maximum values in characteristics are verified by characterization/design. This is valid for all electrical characteristics unless otherwise specified.

3.4.1 Power supply

Table 7 Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Quiescent current output side, ON state	$I_{Q,ON}$			1.35	mA	I_F=$I_{F(ON)}$, V_{VCC} - V_{VEE} = 15 V
Quiescent current output side, OFF state	$I_{Q,OFF}$			1.0	mA	V_F = 0 V, V_{VCC} - V_{VEE} = 15 V
1ED3010						
UVLO threshold output side (on)	V_{UVLOH}		9.3	9.6	V	V_{VCC} - V_{VEE}
UVLO threshold output side (off)	V_{UVLOL}	8.25	8.55		V	V_{VCC} - V_{VEE}
UVLO hysteresis output side	V_{HYS}		0.75		V	V_{UVLOH} - V_{UVLOL}
1ED3011						
UVLO threshold output side (on)	V_{UVLOH}		12	12.35	V	V_{VCC} - V_{VEE}
UVLO threshold output side (off)	V_{UVLOL}	10.7	11.05		V	V_{VCC} - V_{VEE}
UVLO hysteresis output side	V_{HYS}		0.95		V	V_{UVLOH} - V_{UVLOL}
1ED3012						
UVLO threshold output side (on)	V_{UVLOH}		13.6	14	V	V_{VCC} - V_{VEE}
UVLO threshold output side (off)	V_{UVLOL}	12.15	12.55		V	V_{VCC} - V_{VEE}
UVLO hysteresis output side	V_{HYS}		1.05		V	V_{UVLOH} - V_{UVLOL}

3.4.2 Input

Table 8 Input

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Threshold input forward current low to high	I_{FLH}			4.5	mA	$V_{OUT} > 5$ V, $C_L = 1$ nF
Input forward voltage	V_F		2.35	2.65	V	$I_F = 5.5$ mA
Input forward voltage	V_F	2.65	3.2		V	$I_F = 15$ mA
Threshold input voltage high to low	V_{FHL}	0.9			V	$V_{OUT} < 5$ V, $C_L = 1$ nF
Temperature coefficient of input forward voltage	$\Delta V_F/\Delta T$	-1.5		1.5	mV/°C	1)
Input reverse breakdown voltage	V_R	20			V	$I_R = 10$ µA

1) Parameter is not subject to production test - verified by design/characterization.

3.4.3 Gate driver

Table 9 Gate driver

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High level output peak current	I_{OUTH}	3.5	6		A	1) $V_{VCC} - V_{VEE} = 15$ V, $I_F = I_{F(ON)}$, $C_L = 100$ nF
High level output on resistance	$R_{DSON,H}$	0.3	0.9	2.1	Ω	$I_{OUTH} = 0.1$ A
Low level output peak current	I_{OUTL}	3.5	6.5		A	1) $V_{VCC} - V_{VEE} = 15$ V, $V_F = 0$ V, $C_L = 100$ nF
Low level output on resistance	$R_{DSON,L}$	0.2	0.5	1.1	Ω	$I_{OUTL} = 0.1$ A
Short circuit clamp voltage between OUT and VCC	$V_{CLP,OUT}$			1.0	V	$V_{OUT} - V_{VCC}$, $I_{OUT(H)} = -500$ mA, $t < 10$ µs, $I_F = I_{F(ON)}$
Clamp voltage between VEE and OUT	$V_{CLP,OUT}$			1.0	V	$V_{VEE} - V_{OUT}$, $I_{OUT} = -500$ mA, $t < 10$ µs, $V_F = 0$ V

1) Parameter is not subject to production test - verified by design/characterization

3.4.4 Dynamic characteristics

Table 10 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input to output propagation delay ON	t_{PDON}	19	32	40	ns	$V_{VCC} - V_{VEE} = 15$ V, $C_L = 100$ pF, valid for 1ED3010 and 1ED3011 only

(table continues...)

Table 10 **(continued) Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input to output propagation delay ON	t_{PDON}	19	32	40	ns	V_{VCC} - V_{VEE} = 18 V, C_{L} = 100 pF, valid for 1ED3012 only
Input to output propagation delay OFF	t_{PDOFF}	15	25	30	ns	V_{VCC} - V_{VEE} = 15 V, C_{L} = 100 pF, valid for 1ED3010 and 1ED3011 only
Input to output propagation delay OFF	t_{PDOFF}	15	25	30	ns	V_{VCC} - V_{VEE} = 18 V, C_{L} = 100 pF, valid for 1ED3012 only
Input to output propagation delay distortion	$\lvert t_{\mathrm{PDISTO}}\rvert$		7	15	ns	[1] $\lvert t_{\mathrm{PDOFF}} - t_{\mathrm{PDON}}\rvert$, t_{ON} > 100 ns and t_{OFF} > 100 ns
Input to output, part to part skew	t_{SKEW}			10	ns	[1] [2] C_{L} = 100 pF, same input signal
Input to output, part to part skew plus	$t_{\mathrm{SKEW+}}$			17	ns	[1] [2] C_{L} = 100 pF, complementary input signals
Rise time	t_{RISE}			15	ns	V_{VCC} - V_{VEE} = 15 V, C_{L} = 1 nF, valid for 1ED3010 and 1ED3011 only
Rise time	t_{RISE}			15	ns	V_{VCC} - V_{VEE} = 18 V, C_{L} = 1 nF, valid for 1ED3012 only
Fall time	t_{FALL}			15	ns	V_{VCC} - V_{VEE} = 15 V, C_{L} = 1 nF, valid for 1ED3010 and 1ED3011 only
Fall time	t_{FALL}			15	ns	V_{VCC} - V_{VEE} = 18 V, C_{L} = 1 nF, valid for 1ED3012 only
Output-side start-up time	$t_{\mathrm{START,VCC}}$		5	10	µs	[2] $I_{\mathrm{F}} = I_{\mathrm{F(ON)}}$, C_{L} = 100 pF
Output-side deactivation time	$t_{\mathrm{STOP,VCC}}$	0.5		1.5	µs	[2] $I_{\mathrm{F}} = I_{\mathrm{F(ON)}}$, C_{L} = 100 pF
High-level common-mode transient immunity	$\lvert CM_{\mathrm{H}}\rvert$	300			kV/µs	[2] V_{CM} = 1500 V, $I_{\mathrm{F}} = I_{\mathrm{F(ON)}}$
Low-level common-mode transient immunity	$\lvert CM_{\mathrm{L}}\rvert$	300			kV/µs	[2] V_{CM} = 1500 V, V_{F} = 0 V

1) Value at same ambient temperature and supply voltage
2) Parameter is not subject to production test - verified by design/characterization

3.4.5 Active shut down

Table 11 **Active shut down**

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Active shut down voltage	V_{ACTSD}			1.8	V	V_{OUT} - V_{VEE}, I_{OUTL} = 500 mA, *VCC* open

4 Insulation characteristics (IEC 60747-17, UL 1577) for LDSO-6 300 mil package

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 12 Insulation specification for LDSO-6 300 mil package

Description	Symbol	Characteristic	Unit
Safety limiting values			
Maximum ambient safety temperature	T_S	150	°C
Maximum input-side power dissipation at $T_A = 25°C$[1]	P_{SI}	100	mW
Maximum output-side power dissipation at $T_A = 25°C$[2]	P_{SO}	750	mW
General			
External clearance	*CLR*	> 8	mm
External creepage	*CPG*	> 8	mm
Comparative tracking index	*CTI*	> 600	–
Isolation capacitance	C_{IO}	< 1	pF
Overvoltage category according to IEC 60664-1, Table F.1			–
for rated mains voltage ≤ 150 V (rms)		I-IV	
for rated mains voltage ≤ 300 V (rms)		I-IV	
for rated mains voltage ≤ 600 V (rms)		I-IV	
for rated mains voltage ≤1000 V (rms)		I-III	
Reinforced insulation according to IEC 60747-17 planned			
Climatic classification		40/125/21	–
Pollution degree (IEC 60664-1)		2	–
Apparent charge, method a $V_{pd(ini),a} = V_{IOTM}$, $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_{ini} = 1$ min, $t_m = 10$ s	q_{pd}	< 5	pC
Apparent charge, method b $V_{pd(ini),b} = V_{IOTM} \times 1.2$, $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_{ini} = 1$ s, $t_m = 1$ s	q_{pd}	< 5	pC
Isolation resistance at $T_{A,max}$; $V_{IO} = 500\ V_{DC}$, $T_A = 125°C$	R_{IO}	$> 10^{11}$	Ω
Isolation resistance at T_S; $V_{IO} = 500\ V_{DC}$, $T_S = 150°C$	R_{IO_S}	$> 10^9$	Ω
Maximum rated transient isolation voltage	V_{IOTM}	8000	V (peak)
Maximum repetitive isolation voltage	V_{IORM}	1767	V (peak)
Maximum working isolation voltage	V_{IOWM}	1250	V (rms)
		1767	V (DC)
Impulse voltage	V_{IMP}	8000	V (peak)
Maximum surge isolation voltage for reinforced isolation; $V_{TEST} \geq V_{IMP} \times 1.3$	V_{IOSM}	11000	V (peak)
Recognized under UL 1577 File E311313			
Insulation withstand voltage (60 s)	V_{ISO}	5700	V (rms)
Insulation test voltage (1 s)	$V_{ISO,TEST}$	6840	V (rms)

1) IC input-side power dissipation is derated linearly with 6.1 mW/°C above 133 °C
2) IC output-side power dissipation is derated linearly at 6.1 mW/°C above 25 °C

5 Typical characteristics

Unless otherwise noted,the measurements are done with V_{VCC} = 15 V and a 4.7 μF capacitor between *VCC2* and *VEE2*.

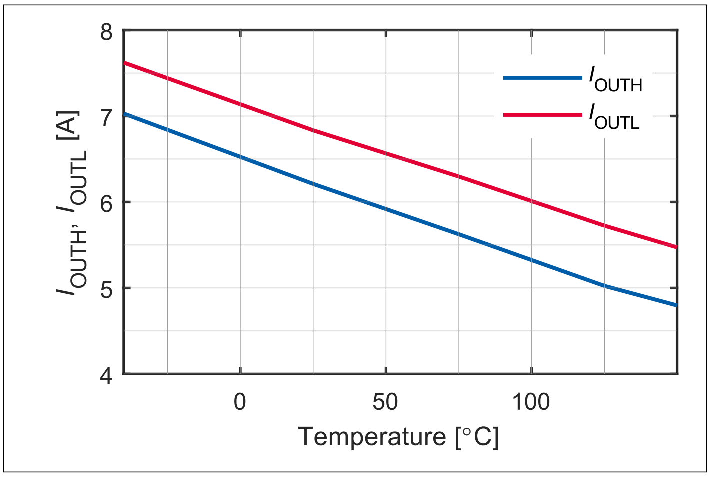


Figure 3 **Output peak current vs. temperature**

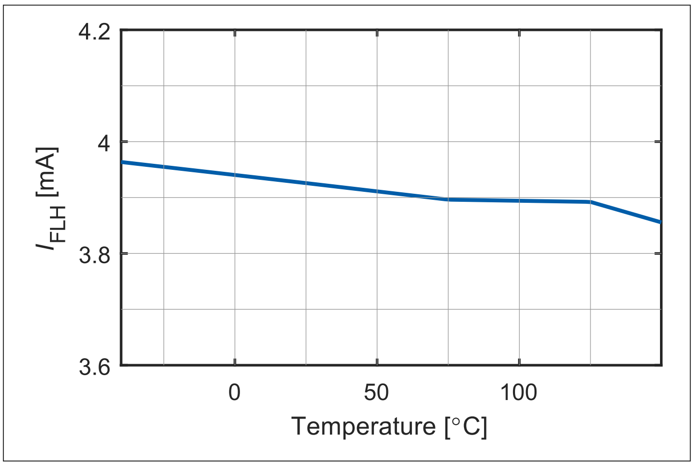


Figure 4 **Forward threshold current vs. temperature**

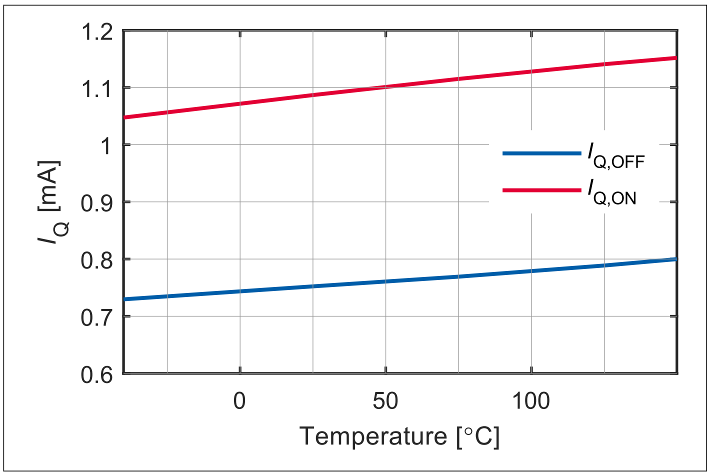


Figure 5 **Supply current vs. temperature**

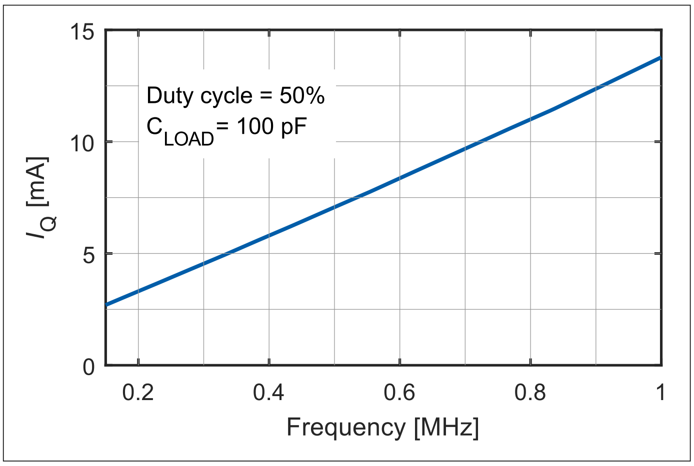


Figure 6 **Supply current vs. frequency**

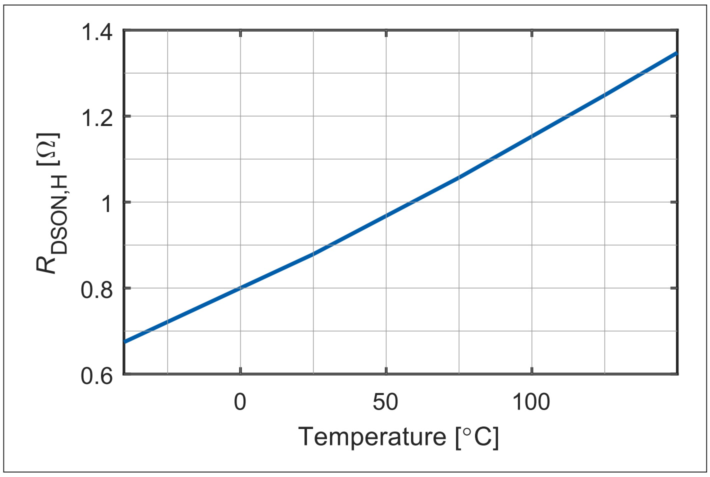


Figure 7 **High level output on resistance vs. temperature**

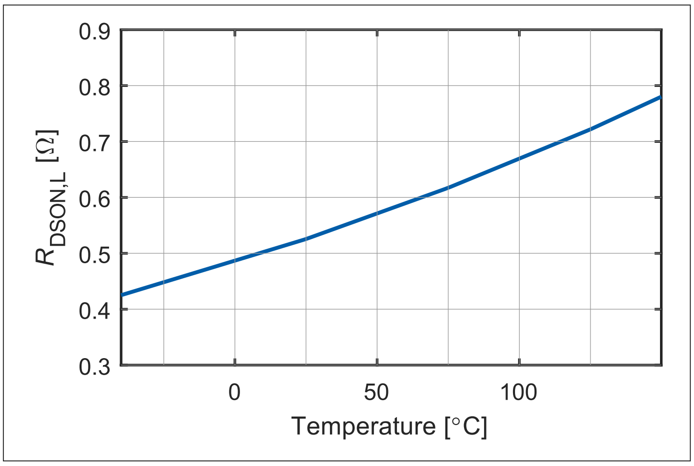


Figure 8 **Low level output on resistance vs. temperature**

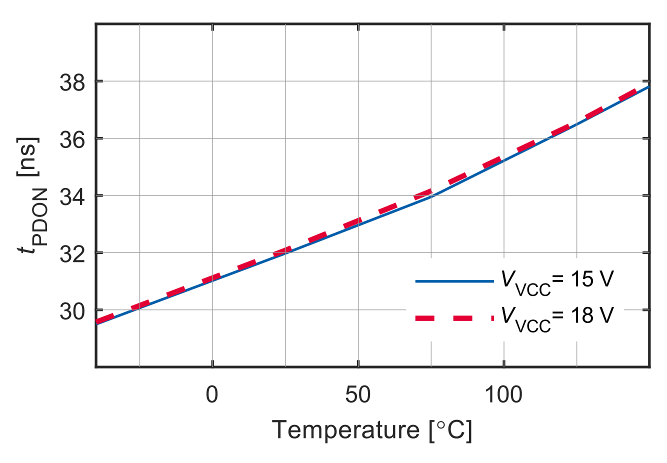


Figure 9 Propagation delay ON vs. temperature

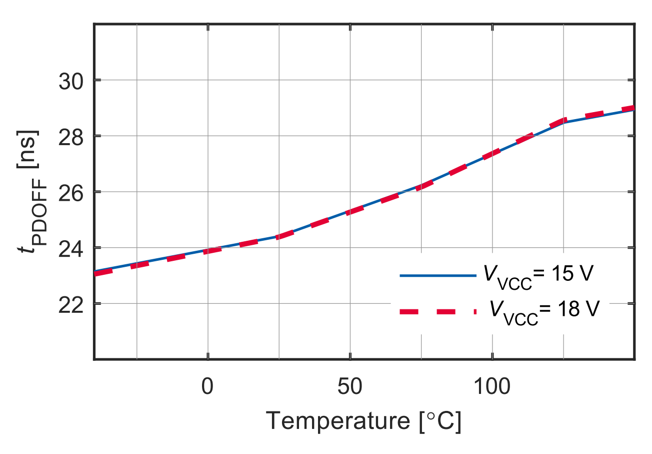


Figure 10 Propagation delay OFF vs. temperature

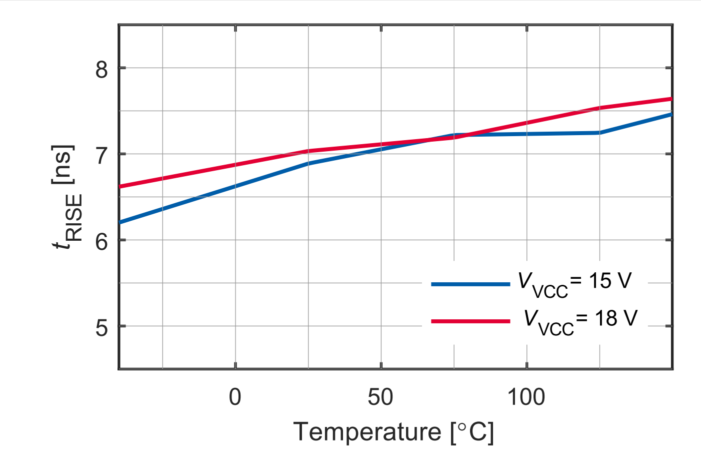


Figure 11 Rise time vs. temperature

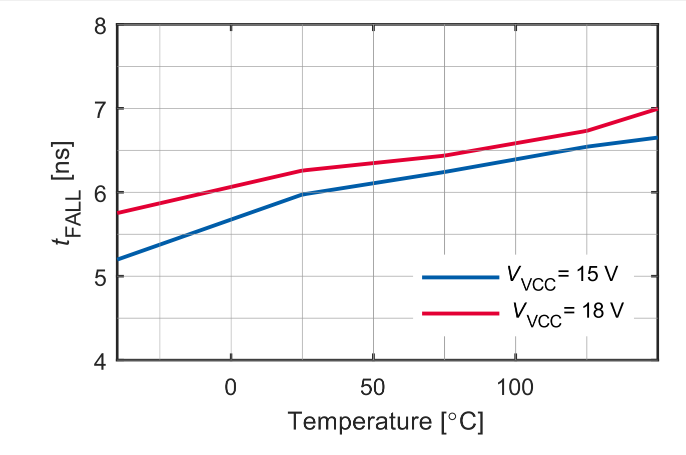


Figure 12 Fall time vs. temperature

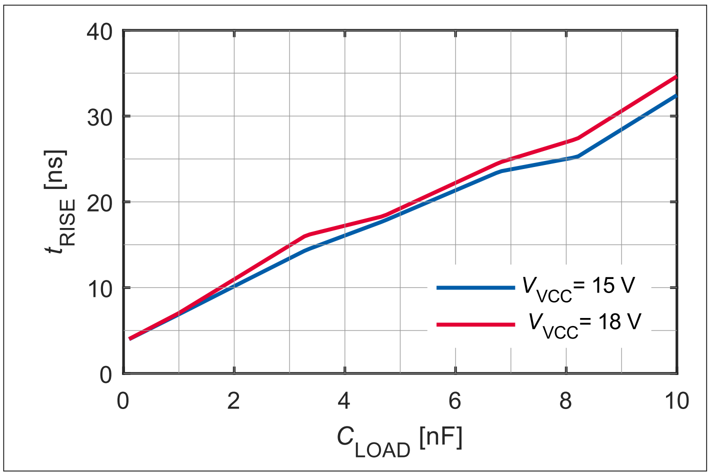


Figure 13 Rise time vs. load capacitance

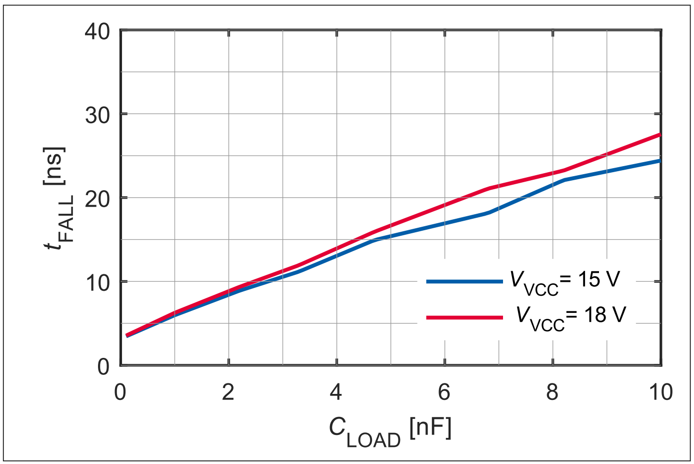


Figure 14 Fall time vs. load capacitance

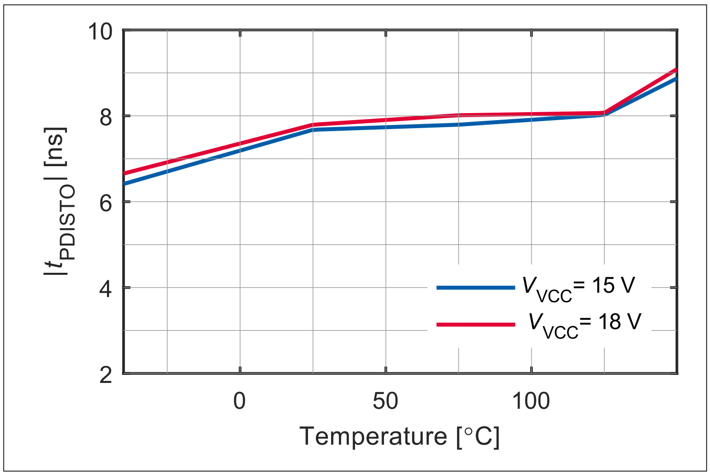


Figure 15 **Propagation delay distortion vs. temperature**

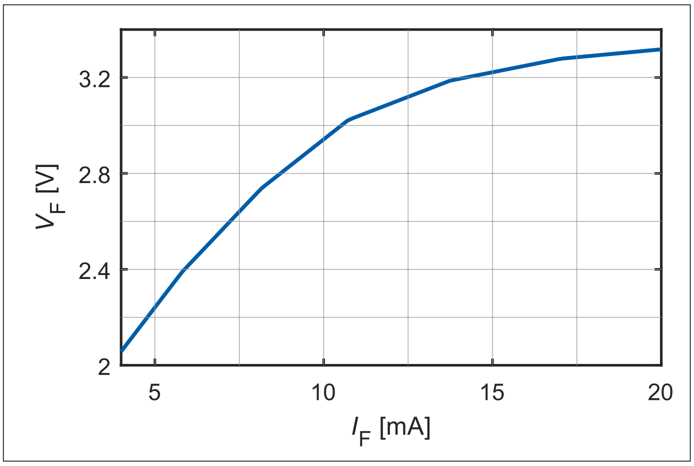


Figure 16 **Input forward voltage vs. input forward current**

6 Parameter measurement

6.1 Propagation delay, rise and fall time

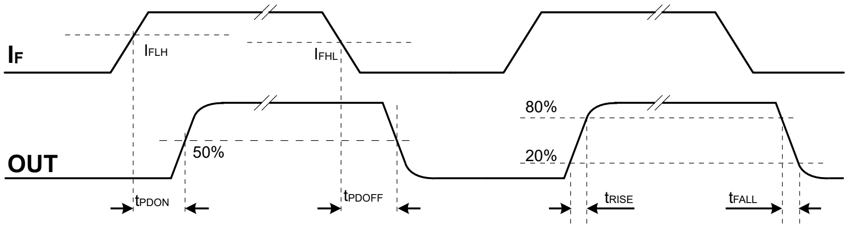


Figure 17 Propagation delay, rise time and fall time

6.2 Part to part skew and skew+

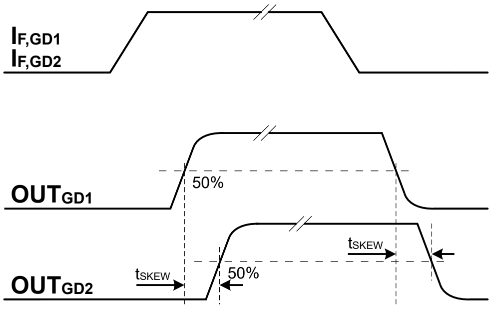


Figure 18 Input to output, part to part skew

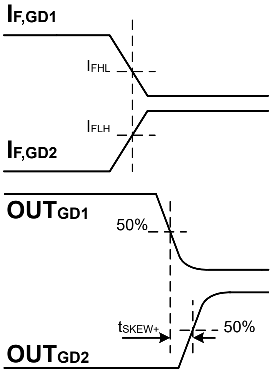


Figure 19 Input to output, part to part skew+

6.3 Undervoltage lockout (UVLO)

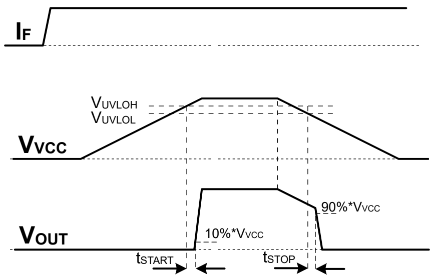


Figure 20 **UVLO Behavior**

To ensure correct switching of the IGBT, Si or SiC MOSFET, the device is equipped with an undervoltage lockout for the output side. Operation starts only after the supply voltage level has increased beyond the V_{UVLOH} level.

If the power supply voltage V_{VCC} of the output chip goes down below V_{UVLOL} the IGBT, Si or SiC MOSFET is switched off and signals from the input chip are ignored until V_{VCC} reaches the power-up voltage V_{UVLOH} again.

***Note**: V_{VCC} is always referred to VEE and does not differentiate between unipolar or bipolar supply.*

6.4 CMTI measurement setup

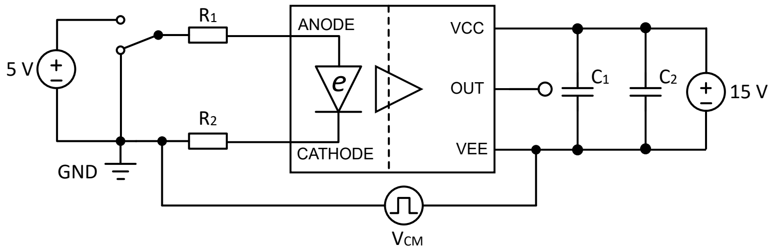


Figure 21 **CMTI Test circuit**

7 Functional description

The EiceDRIVER™ 1ED301xMC12I gate driver ICs are compact, general purpose gate drivers for IGBTs and MOSFETs. They are offered in an industry standard 6 pin (SO6) package with >8 mm creepage and clearance and are pin compatible with standard opto-isolated gate drivers. They offer basic control and protection features enabling fast and easy design of highly reliable systems.

The integrated galvanic isolation via coreless transformer, between the input control side and the driving output stage, provides reinforced isolation and moreover offers best-in-class common mode transient immunity of >300 kV/µs.

The input stage of the 1ED301xMC12I family uses an emulated diode which does not use light emission to transmit signals across the isolation barier and is therefore providing several advantages over standard opto-isolated gate drivers:

- Best in class common mode transient immunity
- Best in class propagation delay and part to part matching (skew and skew+)
- Best in class pulse distortion and part to part skew in the propagation delay, making the design suitable for high performance applications using SiC MOSFETs
- Superior reliability and aging characteristics to those of standard opto-isolated gate drivers who use light emission for their operation

7.1 Input features

The input stage of the gate driver is made to emulate a diode and therefore has two connections: the *ANODE* (Pin 1) and the *CATHODE* (Pin 3).

When the emulated diode is forward biased, meaning a positive voltage is applied between *ANODE* and *CATHODE*, a forward current I_F flows through it. If this current is above the threshold I_{FLH}, the transmitter is activated and this leads to the gate driver output being driven high. An external resistor is recommended in order to limit the forward current to a range within the recommended values. If the *ANODE* to *CATHODE* voltage goes below the threshold V_{FHL} or if the *ANODE* is reversed biased with respect to the *CATHODE*, the gate driver output is driven low. The large allowable reverse voltage enables the gate driver to be operated in interlock architecture.

The gate driver IC input section consists of the following functional blocks:

- reverse voltage blocking element
- forward voltage clamping element
- isolated signal transmitter to the output section

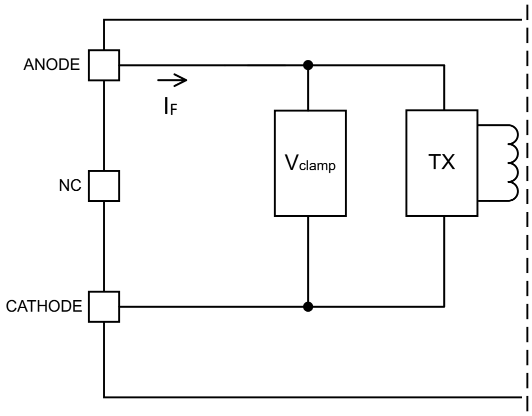


Figure 22 **Block diagram of input section**

7.2 Output features

This section describes the gate driver output sections. The output features of the gate driver IC include undervoltage lockout for the output supply, shoot through protection circuitry for the internal output stage and the active shutdown circuitry.

The current sourcing stage design of the gate driver ICs is designed with a PMOS-only MOSFET. The PMOS will deliver a strong current, not only at the beginning, but constantly all the way up to the *VCC* rail, ensuring a fast turn-on of the IGBT, Si or SiC MOSFET.

The gate driver IC output section consists of the following functional blocks:

- output undervoltage lockout circuit
- isolated signal receiver from the input section
- sourcing and sinking output stage
- active shutdown circuitry

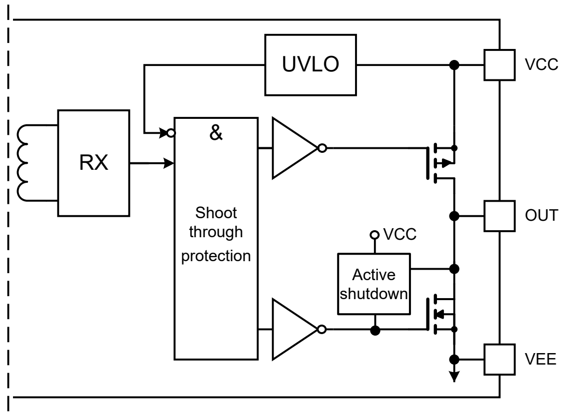


Figure 23 **Block diagram of output section**

7.2.1 Output undervoltage lockout (UVLO)

The output supply range has a positive absolute maximum rating of 35 V for all variants. The gate driver ICs are therefore capable of providing a bipolar gate voltage to a connected power switch.

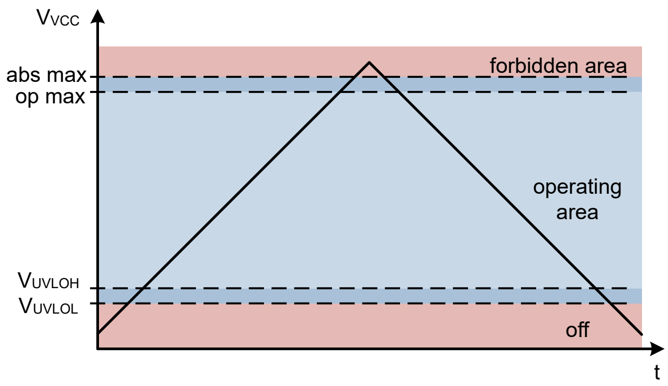


Figure 24 **Output supply and UVLO threshold**

At a crossing of the turn on undervoltage lockout threshold (V_{UVLOH}) during a positive ramp at *VCC* pin in relation to the *VEE* pin, the output section starts operating. The commands from the input side of the gate driver are received and evaluated at the output side. During V_{CC} ramp down and crossing of the turn-off undervoltage lockout threshold (V_{UVLOL}), the output section will initiate a turn-off command regardless of the commands received from the input section. The hysteresis between the thresholds V_{UVLOL} and V_{UVLOH} ensures stable operation when the supply voltage is close to the threshold levels.

Any voltage overshoot above the absolute maximum voltage rating can damage the driver circuits. The operating area is defined between the turn-on undervoltage lockout threshold (V_{UVLOH}) and the maximum recommended operating voltage.

7.2.2 Active shutdown

The active shutdown function is a protection feature of the driver. It is designed to avoid a free-floating gate of a connected power switch to trigger a turn-on.

The active shutdown feature ensures a safe IGBT, Si or SiC MOSFET off-state in case the output chip is not connected to the power supply or an undervoltage lockout is in effect. The IGBT, Si or SiC MOSFET gate is clamped via the *OUT*-pin to *VEE*.

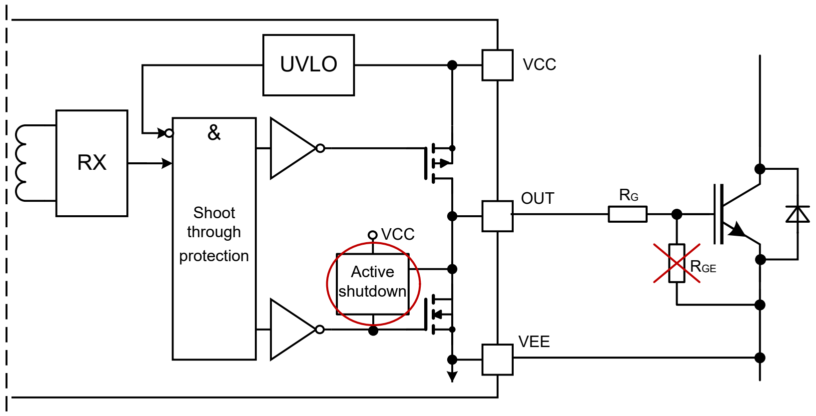


Figure 25 **Block diagram showing active shutdown**

In case of a missing or collapsing power supply at the *VCC* pin, the output section of the driver operates in the active shutdown mode. In this case the driver uses the floating voltage of the connected gate to supply this internal circuit. This solution is by far stronger than using an external R_{GE}. At the same time, in case of fast dV/dt events on the switch which are generating Miller currents that could bias the gate, even when the gate driver is not powered on, the active shutdown circuit will self power and actively pull the gate low.

7.2.3 Driver outputs and supply

The output driver section uses MOSFETs to provide a rail-to-rail output. This feature allows a well defined gate voltage during ON-state and short circuit which is maintained as long as the driver's supply voltage is stable. Due to the low internal voltage drop, the switching behavior of the IGBT, Si or SiC MOSFET is predominantly governed by the gate resistor for as long as the current rating of the gate driver is not exceeded. Furthermore, it reduces the power to be dissipated by the driver as most of the energy is dissipated in the gate resistor.

When driving the switch with unipolar power supplies, the *VEE* pin should be connected directly to the source or emitter of the power transistor as shown in Figure 26.

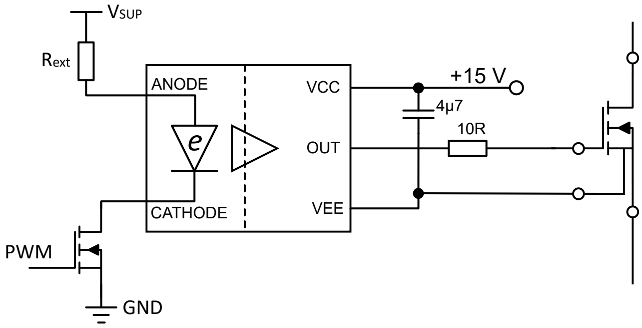


Figure 26 **Circuit example for unipolar power supply driving SiC MOSFET**

When driving the switch with bipolar power supplies, a virtual ground should be created between two capacitors connected to the *VCC* and *VEE* pins. This virtual ground should then be connected to the source or emitter of the power transistor as shown in Figure 27.

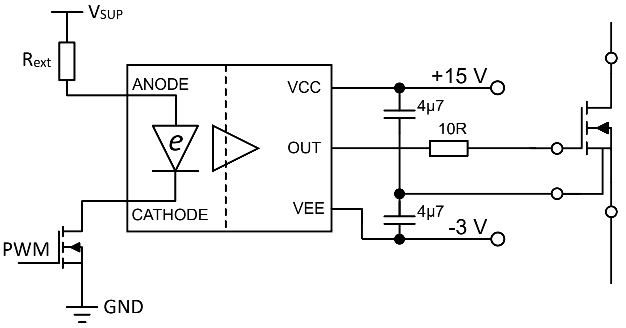


Figure 27 **Circuit example for bipolar power supply driving SiC MOSFET**

8 Application information

Note: Infineon is providing this information as a courtesy only and without acknowledging any legal obligation. Information in the following application chapters is not part of the Infineon component specification, and Infineon does not warrant its accuracy or completeness. Infineon's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality

8.1 Input resistor selection

The input resistor limits the current through the emulated diode when it is forward biased and ensures that the forward current, when the emulated diode is on, stays inside the recommended operating range.

There are several design aspects that need to be taken into consideration when selecting the input resistor:

- Supply voltage V_{SUP} variation
- Emulated diode forward voltage drop variation
- Manufacturer's tolerance for the resistor

In order to calculate the maximum allowed resistor value for a V_{SUP} = 3.3 V nominal, the following assumptions are made:

- the supply voltage is 5% below the nominal value of 3.3 V
- the forward voltage drop of the emulated diode is at its maximum value for 5.5 mA

The maximum allowed resistor value will therefore be given by:

$$R_{\mathrm{in,\,max}} = \frac{V_{SUP,\,\mathrm{min}} - V_{F,\,\mathrm{max}}}{I_{F,\,\mathrm{min}}} = \frac{3.135V - 2.65V}{5.5mA} \approx 88\Omega \tag{1}$$

In order to calculate the minimum allowed resistor value for a V_{SUP} = 3.3 V nominal, the following assumptions are made:

- the supply voltage is 5% above the nominal value of 3.3 V
- the forward voltage drop of the emulated diode is at its minimum value for 15 mA

The minimum allowed resistor value will therefore be given by:

$$R_{\mathrm{in,\,min}} = \frac{V_{SUP,\,\mathrm{max}} - V_{F,\,\mathrm{min}}}{I_{F,\,max}} = \frac{3.465V - 2.65V}{15mA} \approx 55\Omega \tag{2}$$

The chosen input resistor value, taking into account tolerances as well, should be between these limit values:

$$R_{\mathrm{in,\,min}} \leq R_{\mathrm{in,\,chosen}} \leq R_{\mathrm{in,\,max}} \tag{3}$$

For a supply voltage on the input side of 3.3 V nominal, a 68 Ω resistor with 1% tolerance is recommended. This value does not take into consideration any resistance of the buffer or the transistor used to drive the input stage of the gate driver. In case this resistance is significant compared to the total external resistance, it should be subtracted from the chosen value for the external resistor.

8.2 Gate resistor selection

The gate resistor is a key component in the gate drive circuit. The gate resistor defines the source and the sink current of the gate driver thereby controlling the switching speed of the associated power transistor during both turn-on and turn-off operations. As such, selecting an appropriate gate resistor represents an important step in the design process. Key aspects to be considered when selecting the gate resistance are to:

- Optimize the switching losses
- Limit the overshoots and oscillations of the drain source voltage or the collector emitter voltage of the power transistor during turn-off

- Limit the overshoot and oscillations of the drain current or collector current during turn-on
- Damp the oscillations of the gate source or gate emitter voltage caused by parasitic inductances and capacitances in the gate loop

As a starting point in the gate driver selection, the gate resistor used in the datasheet of the power transistor for the characterization of turn-on and turn-off losses can be used. The power supply conditions are rarely the same as the power supply conditions used in power transistor datasheets. Therefore, an adaptation of the power transistor datasheet values is required to obtain a starting point in the selection of the final gate resistor. The method proposed here assumes the same peak gate current value for both the actual application and the power transistor datasheet.

The peak gate current as per power transistor datasheet equals to:

$$I_{\mathrm{G,\,pk}} = \frac{\Delta V_{\mathrm{GS,datasheet}}}{R_{\mathrm{G,\,datasheet}} + R_{\mathrm{G,\,int}}} = \frac{\Delta V_{\mathrm{GS,application}}}{R_{\mathrm{G,\,application}} + R_{\mathrm{G,\,int}}}$$
$$\text{with} \quad \Delta V_{\mathrm{GS}} = V_{\mathrm{VCC}} - V_{\mathrm{VEE}} \tag{4}$$

Solving this equation for R_G leads to:

$$R_{\mathrm{G,application}} = \frac{\Delta V_{\mathrm{GS,application}}}{I_{\mathrm{G,\,pk}}} - R_{\mathrm{G,\,int}} \tag{5}$$

This method provides a starting point for the gate resistor selection. Further evaluations, such as EMI measurements, are required for the final dimensioning of the gate resistors as they have to be adjusted to work with the circuitry inductance, margins and allowed dV/dt transients.

8.3 Power supply recommendations

The EiceDRIVER™ 1ED301x gate drivers support a wide range of voltages on the output side. These devices can operate with unipolar as well as bipolar power supply voltages on the output side for reliable and safe operation in the application. To ensure that the gate driver operates correctly, it is necessary to place appropriate decoupling capacitors on the power supply pins.

The decoupling capacitors on the output side, in addition to decoupling any disturbance on the power supply, also store the energy necessary to deliver the gate currents required for turning on and off the power transistor. Therefore, these capacitors should be dimensioned appropriately to limit the voltage drop during the power transistor turn-on and turn-off process.

When using a unipolar power supply, a low ESR, surface mount, multilayer ceramic capacitor of proper value should be placed between the *VCC* pin and the *VEE* pin, in close proximity of the pins.

In case of bipolar power supply, using a ceramic capacitor of proper value between *VCC* and virtual ground (source or emitter potential of power transistor) is recommended. Similarly, using a capacitor between *VEE* pin and virtual ground is recommended. Depending on the gate charge of the power transistor and the peak source and sink gate currents, a higher capacitance may be necessary to limit the voltage drop during power transistor turn-on and turn-off. Finally, a 100 nF decoupling capacitor is recommended between the *VCC* and *VEE* pins to ensure a short path between them to decouple any high frequency noise.

When selecting the capacitors, it is important to consider the capacitance drop of ceramic capacitors with respect to the applied DC voltage.

8.4 Power dissipation estimation

The gate driver output side losses consist of the quiescent current losses P_Q at nominal switching frequency and no load, the sourcing losses P_{source} and the sinking losses P_{sink}:

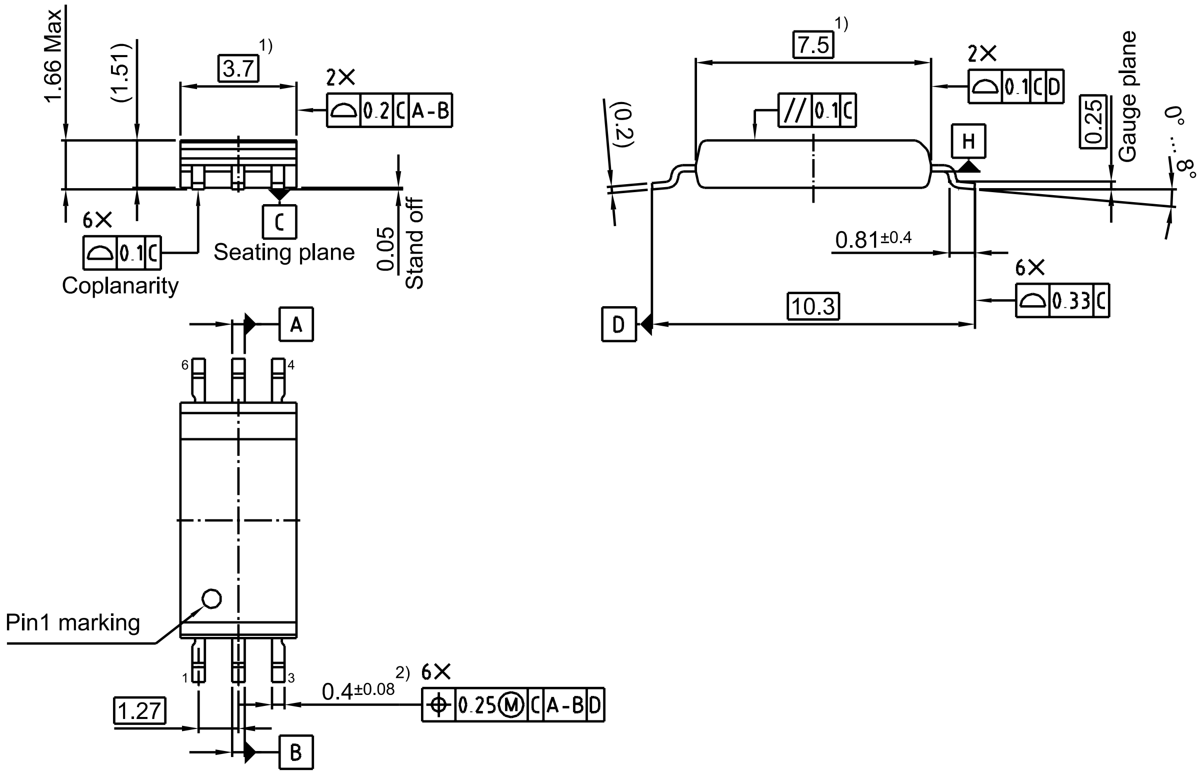
$$P_{\mathrm{OUT}} = P_{\mathrm{Q}} + P_{\mathrm{source}} + P_{\mathrm{sink}} \tag{6}$$

The turn-on, P_{source}, and turn-off, P_{sink}, losses can be estimated using the inner gate driver resistance, $R_{\text{DSON,H}}$ or $R_{\text{DSON,L}}$, the external gate resistor, $R_{\text{G,ext}}$ and, if applicable, the internal gate resistor of the switch $R_{\text{G,int}}$, the application related gate charge, Q_{G}, the total gate driving voltage, V_{VCC} - V_{VEE}, and switching frequency, f_{sw}:

$$\begin{aligned} P_{\text{source}} &= \frac{1}{2} Q_G \cdot f_{\text{sw}} \cdot (V_{\text{VCC}} - V_{\text{VEE}}) \cdot \frac{R_{\text{DSON,H}}}{R_{\text{DSON, H}} + R_{\text{G,ext, ON}} + R_{\text{G,int}}} \\ P_{\text{sink}} &= \frac{1}{2} Q_G \cdot f_{\text{sw}} \cdot (V_{\text{VCC}} - V_{\text{VEE}}) \cdot \frac{R_{\text{DSON,L}}}{R_{\text{DSON,L}} + R_{\text{G,ext, OFF}} + R_{\text{G,int}}} \end{aligned} \tag{7}$$

Additionally, external components that surround the gate driver can heat up the IC. The mere calculation of losses and the theoretical junction temperature alone are not sufficient for a proven gate driver circuit design. A verification by measurement is needed to avoid unexpected effects in the application. The identification of hot spots is possible, for example, by using an infrared camera.

9 Package dimensions



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.15 max.
3) Datum A & B to be determined at datum H.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊲⊕]
Drawing according to ISO 8015, general tolerances ±0.05 / ±1°

Figure 28 LDSO-6 300 mil (low profile dual small outline package wide form factor, 300 mil)

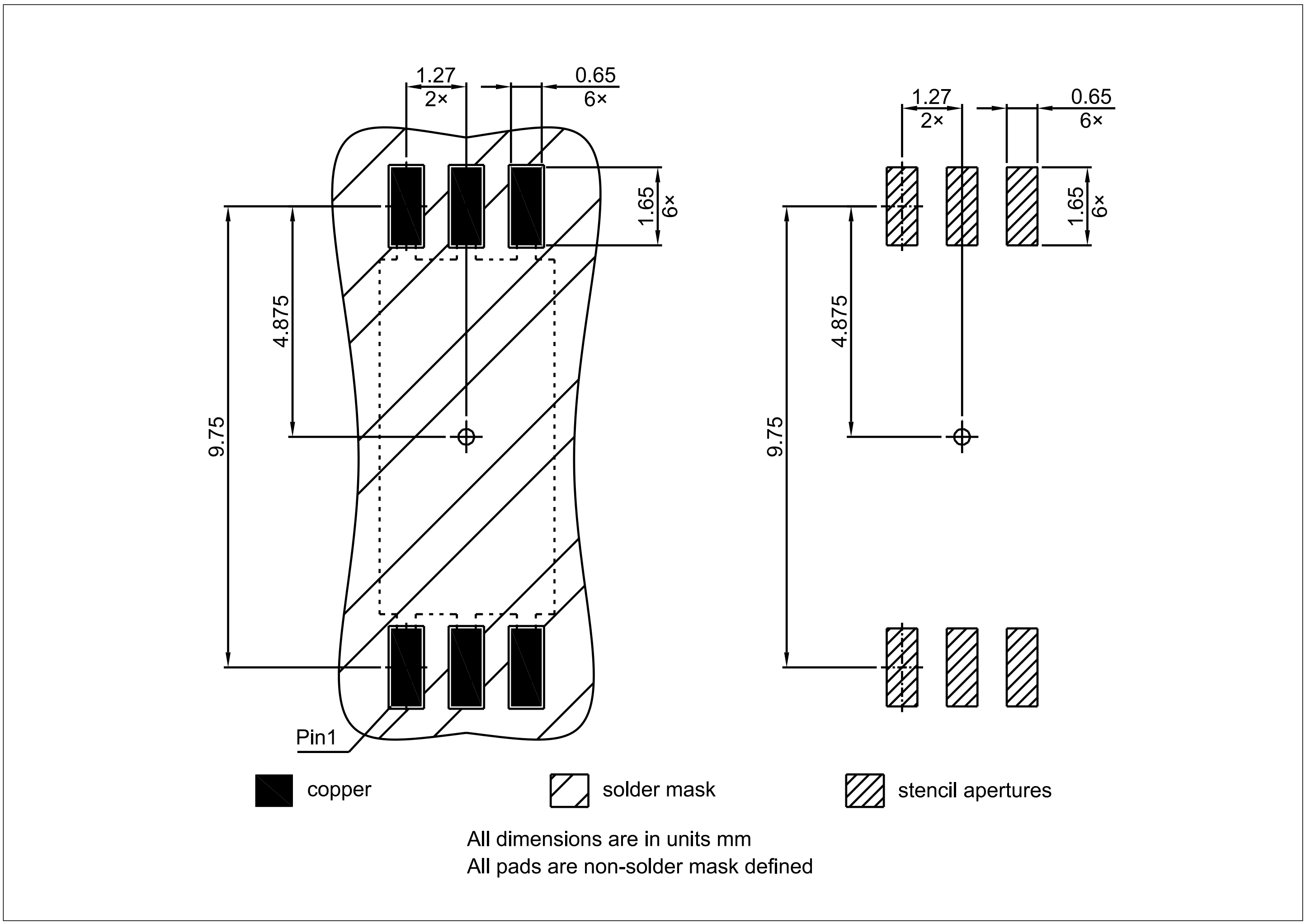


Figure 29 LDSO-6 300 mil recommended footprint

Revision history

Document version	Date of release	Description of changes
v 1.00	2025-08-11	• initial release
v 1.10	2025-11-30	• Updated the UL 1577 certification status

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