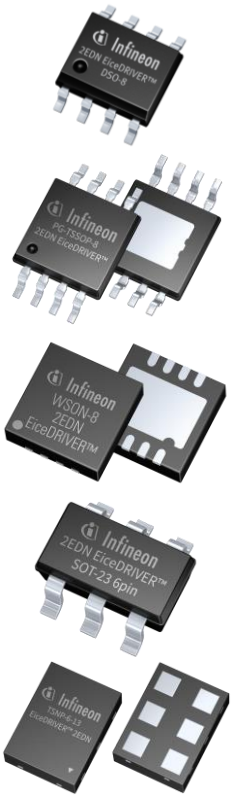
EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x

Dual-channel low-side 5 A gate driver ICs with low output resistance and excellent timing accuracy



Features

- ±5 A source/sink currents
- 19 ns typ. propagation delay
- +6/-4 ns propagation delay accuracy
- 1.8 µs Undervoltage lockout (UVLO) start-up time
- 500 ns UVLO shut-down time
- Fast active output voltage clamping (1.2 V/20 ns)
- -12 V input robustness
- 5 A reverse current robustness
- 4 V and 8 V UVLO options

Potential applications

- Switch-mode power-supplies
- DC-DC power converters
- Synchronous rectification stages
- Power factor correction systems

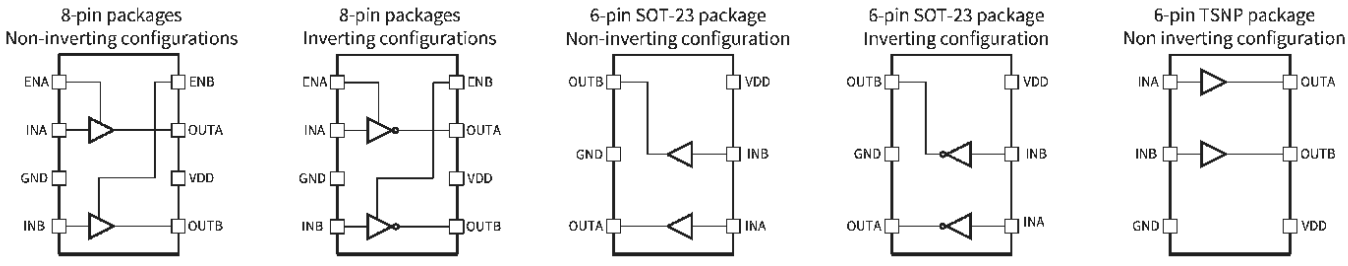
Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Description

The EiceDRIVER™ 2EDN family is offered in 8-pin DSO, TSSOP and WSON packages as well as in small and versatile 6-pin SOT23 and TSNP packages. High output current capability together with active output voltage clamping, tight timing specifications, and optimized start-up and shut-down times, make the 2EDN family the first choice for fast-switching applications.

Available device configurations



Peak output current	Input Config.	8-pin DSO		8-pin TSSOP		8-pin WSON	6-pin SOT23	6-pinTSNP
		4V UVLO	8V UVLO	4V UVLO	8V UVLO	4V UVLO	4V UVLO	4V UVLO
5 A	non-inverting	2EDN7534F	2EDN8534F	2EDN7534R	2EDN8534R	2EDN7534G	2EDN7534B	2EDN7534U
	inverting	2EDN7533F	2EDN8533F	2EDN7533R	2EDN8533R	-	2EDN7533B	-
4 A	non-inverting	2EDN7434F	-	2EDN7434R	-	-	-	-

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1 Product versions

The EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x are available in two different logic configurations (direct and inverting), two different undervoltage lockout levels (4 V and 8 V) and five package versions.

1.1 Logic configuration versions

The two input logic configurations are identified by the "x" variable in the product code EiceDRIVER™ 2EDN753x/ 2EDN853x/2EDN743x:

- x = 3: inverting input logic
- x = 4: non-inverting/direct input logic

Table 1 and Table 2 describe the logic dependence of the output state from undervoltage lockout (UVLO), enable and input pins for the 8-pin and 6-pin variants respectively. If the enable pin ENA (or ENB) is either driven high or left open, the associated gate driver output depends on the respective input pin. If the enable pin ENA (or ENB) is low, the associated OUT pin is low, independent of the input signal. If a UVLO event is triggered, both OUTA and OUTB are kept in a low state, regardless of the input and enable pins status. The functional description is in Chapter 3 Block diagram and Chapter 4 Functional description.

Table 1 Logic table for DSO-8, TSSOP-8, WSON-8 pin package

Inputs					Inverting output		Direct output	
ENA	ENB	INA	INB	UVLO[1)]	OUTA	OUTB	OUTA	OUTB
x	X	X	X	Active	L	L	L	L
L	L	X	X	inactive	L	L	L	L
H	L	L	X	inactive	H	L	L	L
H	L	H	X	inactive	L	L	H	L
L	H	X	L	inactive	L	H	L	L
L	H	X	H	inactive	L	L	L	H
H	H	L	L	inactive	H	H	L	L
H	H	H	L	inactive	L	H	H	L
H	H	L	H	inactive	H	L	L	H
H	H	H	H	inactive	L	L	H	H

1) *Inactive UVLO: V_{DD} is above $UVLO_{ON}$ voltage threshold and control logic drives the output stage. Active UVLO: an undervoltage lockout event has been triggered*

Table 2 Logic table for DSO-8, TSSOP-8, WSON-8 pin package

Inputs			Inverting output		Direct output	
INA	INB	UVLO[1)]	OUTA	OUTB	OUTA	OUTB
X	X	Active	L	L	L	L
L	L	inactive	H	H	L	L
H	L	inactive	L	H	H	L
L	H	inactive	H	L	L	H
H	H	inactive	L	L	H	H

1) *Inactive UVLO: V_{DD} is above $UVLO_{ON}$ voltage threshold and control logic drives the output stage. Active UVLO: an undervoltage lockout event has been triggered*

1.2 Package versions

The EiceDRIVER™ 2EDN family is available in five different package versions. The package type is identified by the last character in the product code:

- the standard PG-DSO-8 is designated by “F” (e.g. 2EDN753xF)
- the small leaded PG-TSSOP-8 is designated by “R” (e.g. 2EDN753xR)
- the leadless PG-WSON-8 is designated by “G” (e.g. 2EDN753xG)
- the tiny PG-SOT23-6 is designated by “B” (e.g. 2EDN753xB)
- the ultra-tiny PG-TSNP-6 is designated by “U” (e.g. 2EDN7534U)

Package drawings are available in Package outlines Chapter 9

2 Pin configuration and description

2.1 Input configuration for PG-DSO-8 package

The pin configuration for all input versions of EiceDRIVER™ 2EDN7534F, 2EDN7434F, 2EDN7533F, 2EDN8534F and 2EDN8533F in the PG-DSO-8 package is shown in the figure below. Diagrams can be viewed in Chapter 9.2 PG-DSO-8.

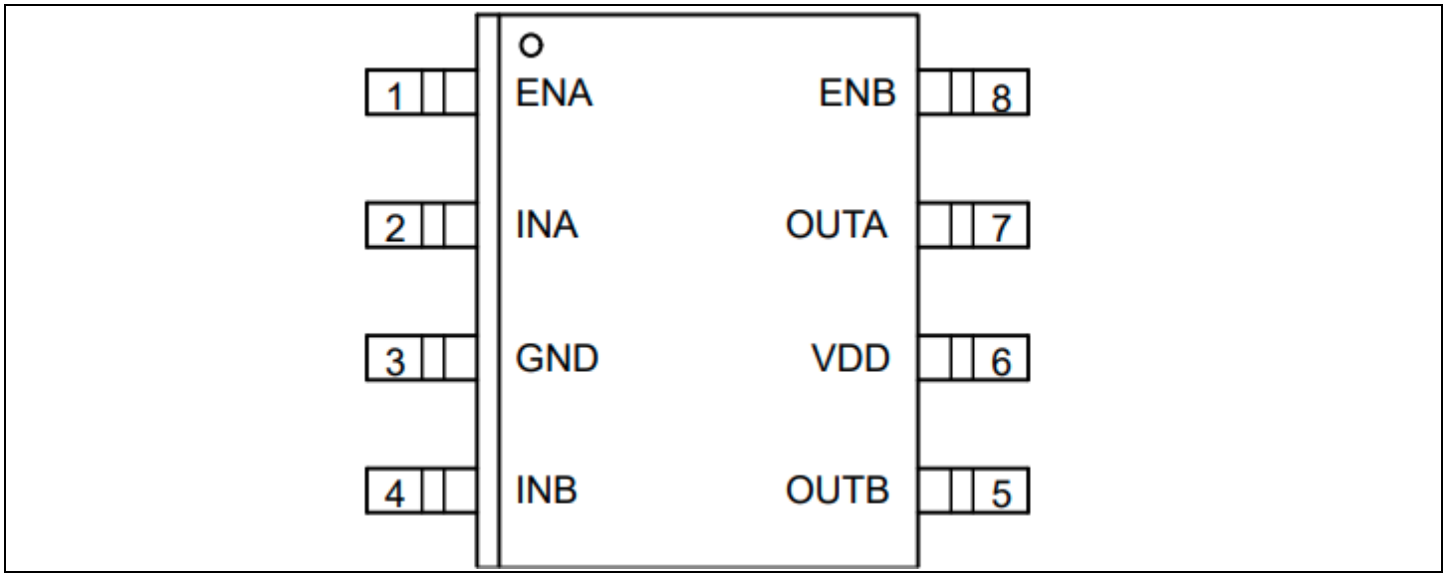

Figure 1 Pin Configuration PG-DSO-8. Top view

Table 3 Pin configuration for PG-DSO-8 package

Pin number	Symbol	Description
1	ENA	**Enable input channel A** Logic input. If ENA is high or left open, OUTA is controlled by INA. ENA low causes OUTA low
2	INA	**Input signal channel A** Logic input, controlling OUTA (inverting or non-inverting)
3	GND	**Ground** Gate driver reference ground
4	INB	**Input signal channel B** Logic input, controlling OUTB (inverting or non-inverting)
5	OUTB	**Driver output channel B** Low-impedance output with source and sink capability
6	VDD	**Positive supply voltage** Operating range 4.5 V/8.6 V to 20 V
7	OUTA	**Driver output channel A** Low-impedance output with source and sink capability
8	ENB	**Enable input channel B** Logic Input. If ENB is high or left open, OUTB is controlled by INB. ENB low causes OUTB low

2.2 Input configuration for PG-TSSOP-8 package

The pin configuration for all input versions of EiceDRIVER™ 2EDN7534R, 2EDN7434R, 2EDN7533R, 2EDN8534R, 2EDN8533R in the PG-TSSOP-8 package is shown in the figure below. Diagrams can be viewed in Chapter 9.3 PG-TSSOP-8.

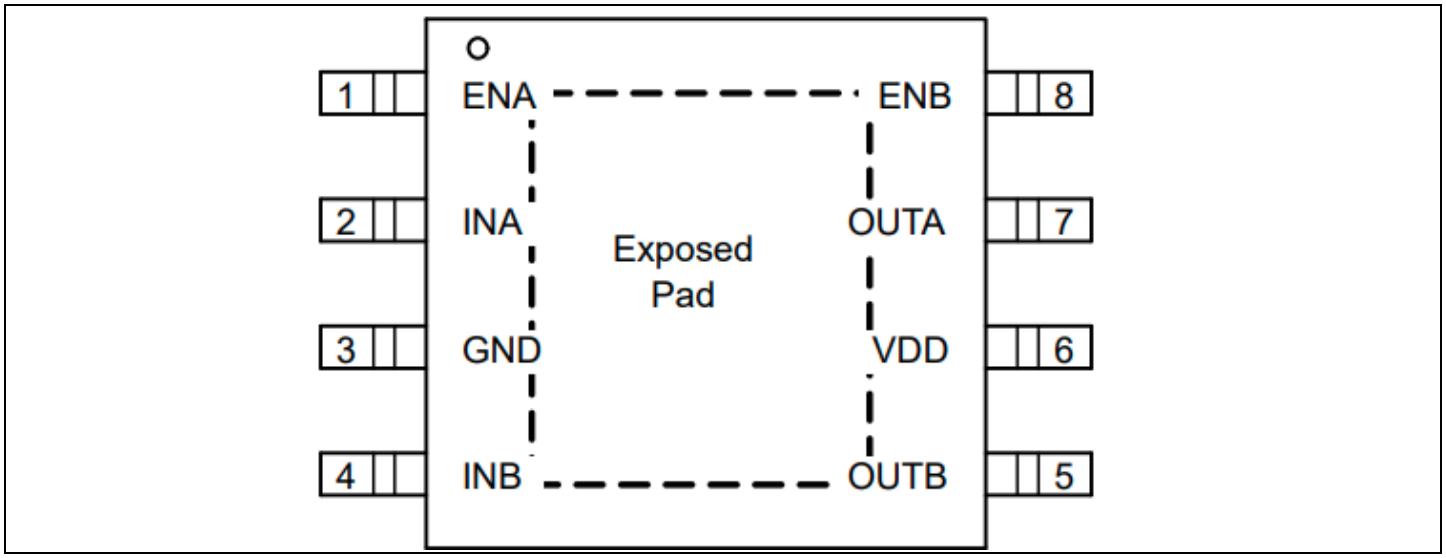

Figure 2 Pin Configuration PG-TSSOP-8, top view

Table 4 Pin configuration for PG-TSSOP-8 package

Pin number	Symbol	Description
1	ENA	**Enable input channel A** Logic input. If ENA is high or left open, OUTA is controlled by INA. ENA low causes OUTA low
2	INA	**Input signal channel A** Logic input, controlling OUTA (inverting or non-inverting)
3	GND	**Ground**[1)] Gate driver reference ground
4	INB	**Input signal channel B** Logic input, controlling OUTB (inverting or non-inverting)
5	OUTB	**Driver output channel B** Low-impedance output with source and sink capability
6	VDD	**Positive supply voltage** Operating range 4.5 V/8.6 V to 20 V
7	OCTA	**Driver output channel A** Low-impedance output with source and sink capability
8	ENB	**Enable input channel B** Logic Input. If ENB is high or left open, OUTB is controlled by INB. ENB low causes OUTB low

1) *Exposed pad sink of PG-TSSOP-8 packages has to be connected to GND pin*

2.3 Input configuration for PG-WSON-8 package

The pin configuration of EiceDRIVER™ 2EDN7534G in the PG-WSON-8 package is shown in the figure below. Diagrams can be viewed in Chapter 9.4 PG-WSON-8.

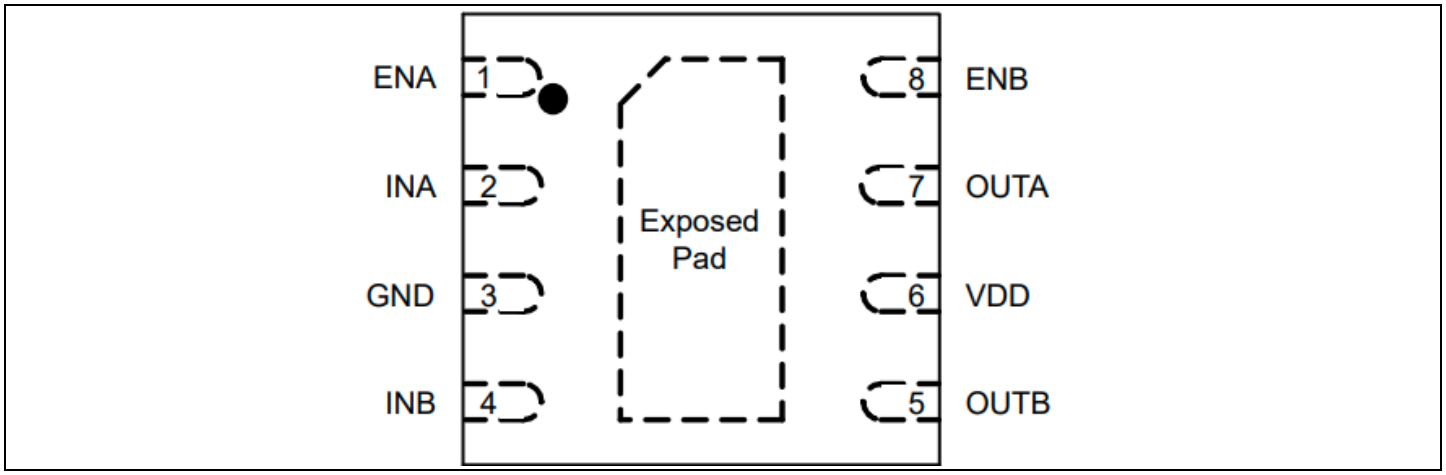

Figure 3 Pin Configuration PG-WSON-8, top view

Table 5 Pin configuration for PG-WSON-8 package

Pin number	Symbol	Description
1	ENA	**Enable input channel A** Logic input. If ENA is high or left open, OUTA is controlled by INA. ENA low causes OUTA low
2	INA	**Input signal channel A** Logic input, controlling OUTA (inverting or non-inverting)
3	GND	**Ground**[1)] Gate driver reference ground
4	INB	**Input signal channel B** Logic input, controlling OUTB (inverting or non-inverting)
5	OUTB	**Driver output channel B** Low-impedance output with source and sink capability
6	VDD	**Positive supply voltage** Operating range 4.5 V/8.6 V to 20 V
7	OUTA	**Driver output channel A** Low-impedance output with source and sink capability
8	ENB	**Enable input channel B** Logic Input. If ENB is high or left open, OUTB is controlled by INB. ENB low causes OUTB low

1) *Exposed pad of PG-WSON-8 packages has to be connected to GND pin*

2.4 Input configuration for PG-SOT23-6 package

The pin configuration of EiceDRIVER™ 2EDN7534B and 2EDN7533B in the PG-SOT23-6 package is shown in the figure below. Drawings can be viewed in Chapter 9.5 PG-SOT23-6.

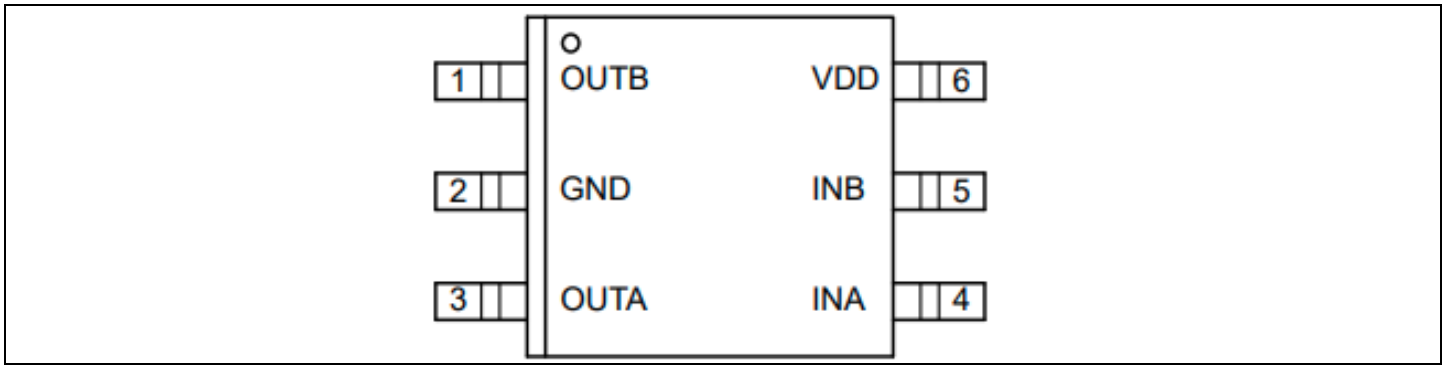

Figure 4 Pin Configuration PG-SOT23-6 top view

Table 6 Pin configuration for PG-SOT23-6 package

Pin number	Symbol	Description
1	OUTB	**Driver output channel B** Low-impedance output with source and sink capability
2	GND	**Ground** Gate driver reference ground
3	OUTA	**Driver output channel A** Low-impedance output with source and sink capability
4	INA	**Input signal channel A** Logic input, controlling OUTA (non-inverting)
5	INB	**Input signal channel B** Logic input, controlling OUTB (non-inverting)
6	VDD	**Positive supply voltage** Operating range 4.5 V/8.6 V to 20 V

2.5 Input configuration for PG-TSNP-6 package

The pin configuration of EiceDRIVER™ 2EDN7534U in the PG-TSNP-6 package is shown in the figure below. Drawings can be viewed in Chapter 9.6 PG-TSNP-6.

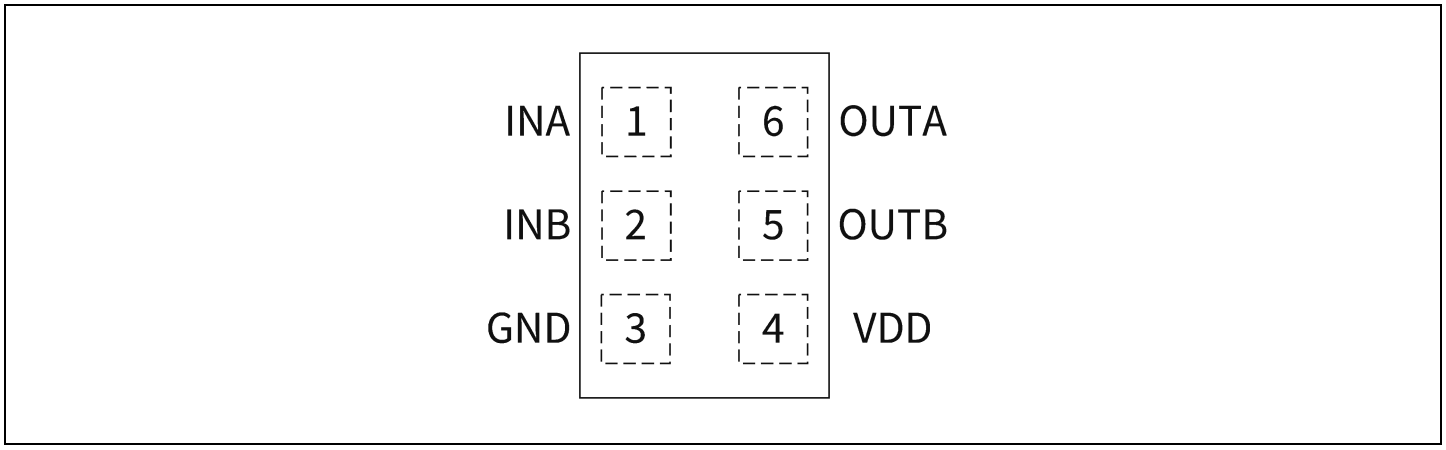

Figure 5 Pin Configuration PG-TSNP-6 top view

Table 7 Pin configuration for PG-TSNP-6 package

Pin number	Symbol	Description
1	INA	**Input signal channel A** Logic input, controlling OUTA (non-inverting)
2	INB	**Input signal channel B** Logic input, controlling OUTB (non-inverting)
3	GND	**Ground** Gate driver reference ground
4	VDD	**Positive supply voltage** Operating range 4.5 V to 20 V
5	OUTB	**Driver output channel B** Low-impedance output with source and sink capability
6	OUTA	**Driver output channel A** Low-impedance output with source and sink capability

3 Block diagram

Simplified functional block diagrams for the PG-DSO-8, PG-TSSOP-8, PG-WSON-8 package variants are given in Figure 6 and Figure 7. Block diagrams for the PG-SOT23-6 and PG-TSNP-6 package variants are shown in Figure 8 and Figure 9. Please refer to functional description in Chapter 4.

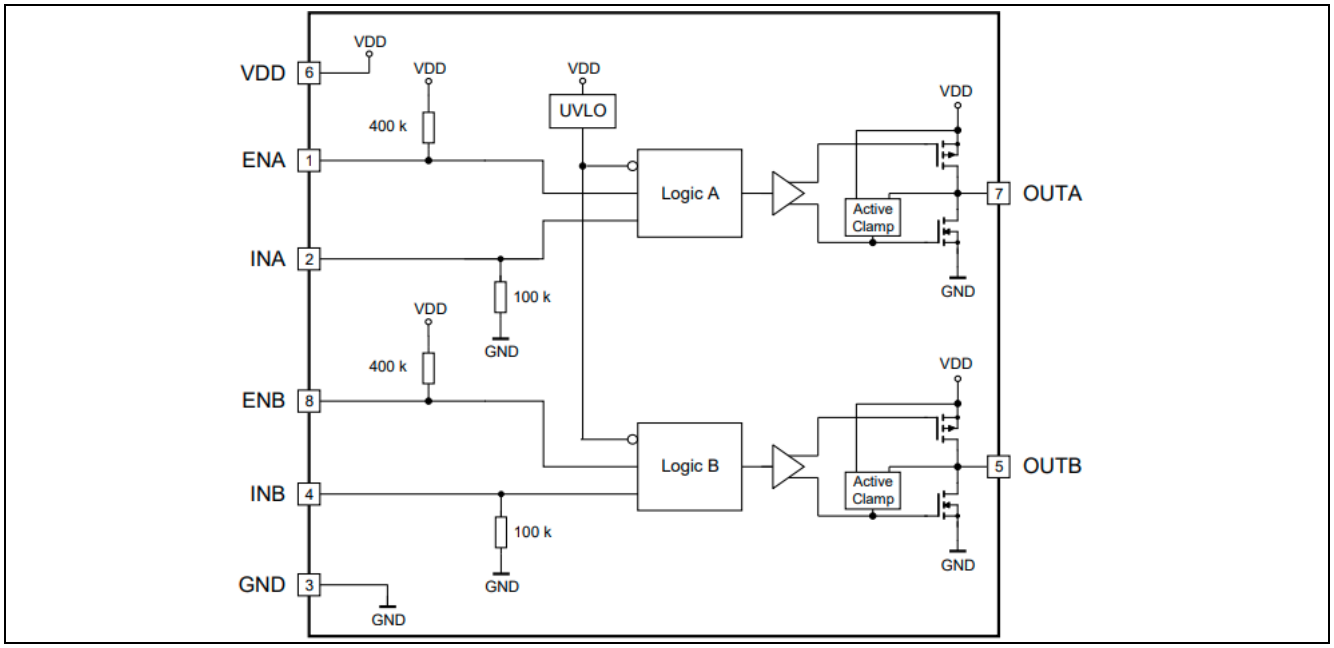

Figure 6 Simplified block diagram for direct/non-inverting input configuration, 8-pin packages

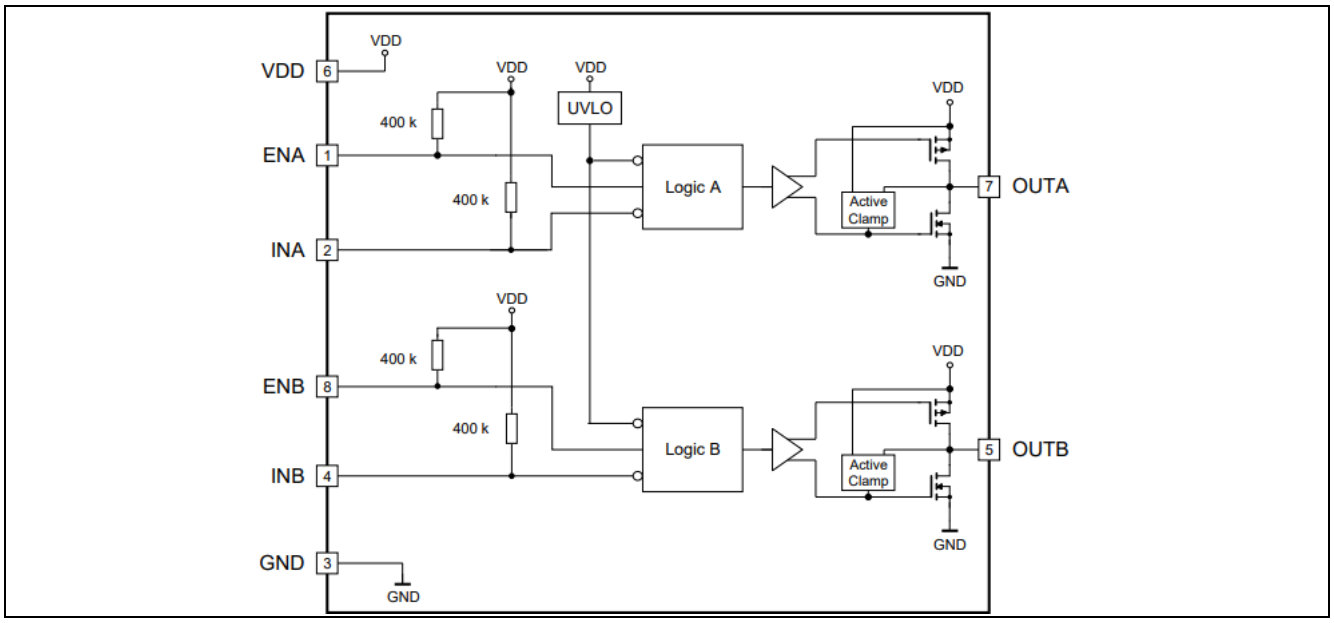

Figure 7 Simplified block diagram for inverting input configuration, 8-pin packages

Block diagram

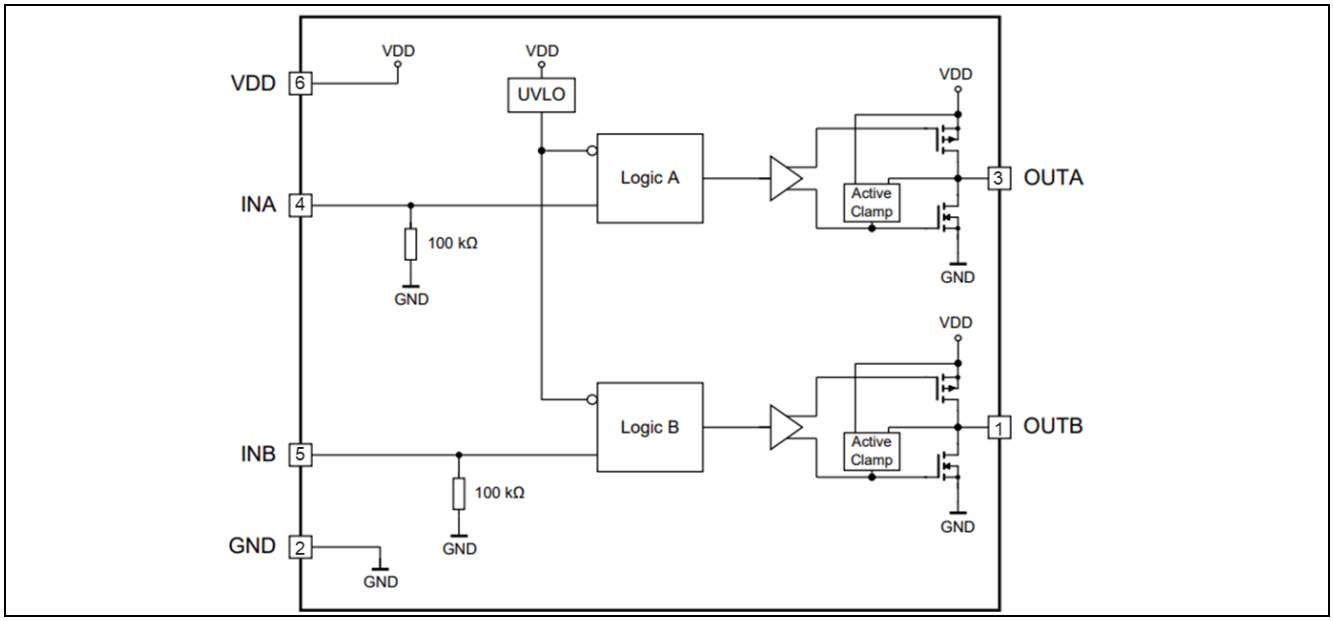

Figure 8 Simplified block diagram for direct/non-inverting input configuration, 6-pin packages PG-SOT23-6

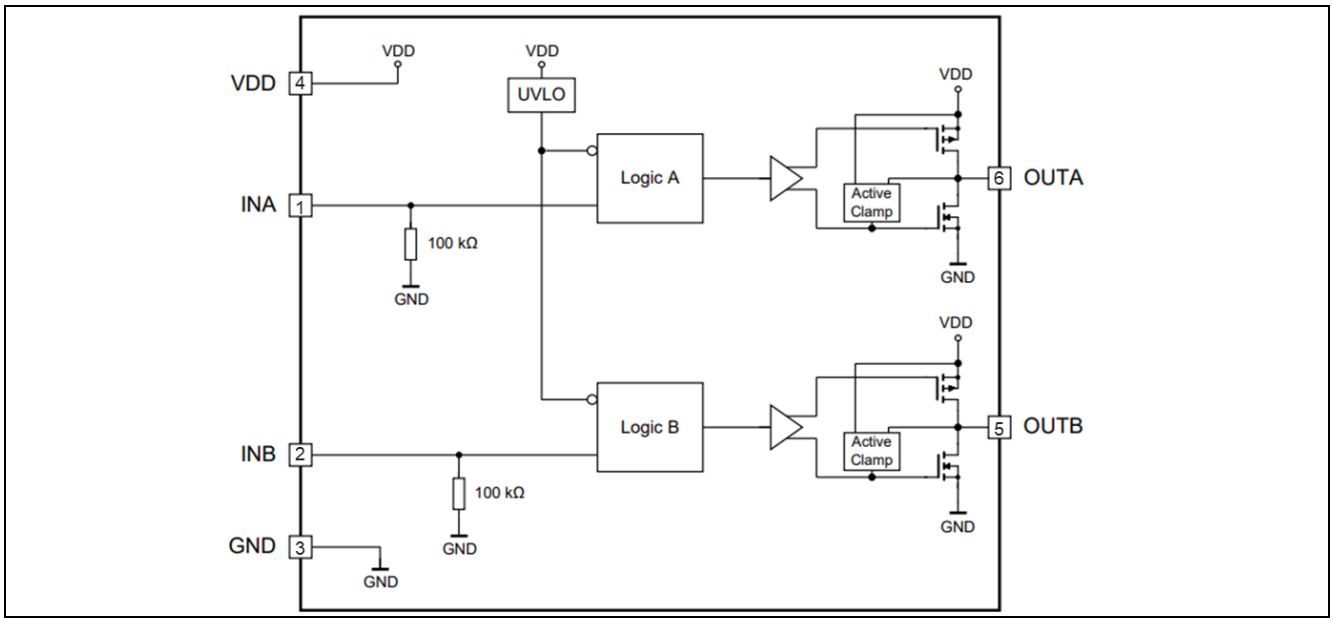

Figure 9 Simplified block diagram for inverting input configuration, 6-pin packages TSNP

4 Functional description

4.1 Introduction

The EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x is a fast dual-channel driver for low-side switches. Two true rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure high flexibility and cover a high variety of applications.

An extended negative voltage range protects input pins against ground shifts. No current flows over the ESD structure in the IC during a negative input level. All outputs are robust against reverse current. During the interaction with the power MOSFET, reverse reflected power is handled by the internal output stage.

All inputs are compatible with LV-TTL signal levels. The threshold voltages have a typical hysteresis of 0.9 V, that is constant over the supply voltage range.

EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x ensure optimal performance in fast-switching applications because of the low delays and rise/fall times. The maximum skew between Channel A and Channel B is 2 ns.

4.2 Supply voltage

The maximum operating supply voltage is 20 V. This high voltage is valuable in order to exploit the full current capability of EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x when driving low R_{DSON} MOSFETs. The minimum operating supply voltage is set by the undervoltage lockout function to a typical default values of 4.2 V for the 4 V-UVLO variant and 8 V for the 8 V-UVLO variant.

4.3 Undervoltage lockout (UVLO) function

The undervoltage lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. This protects power MOSFETs from running into linear mode, preventing excessive power dissipation if the voltage is not enough to completely turn on the switches. The UVLO level is set to a typical value of 4.2 V or 8 V (with hysteresis). UVLO of 4.2 V is normally used for logic level MOSFETs. For standard and high voltage superjunction MOSFETs, a UVLO voltage of typical 8 V is available.

Table 8 UVLO turn-on and turn-off thresholds

Nominal UVLO level	UVLO turn-on threshold(typ.)	UVLO turn-on threshold(typ.)
4.2 V	4.2 V	3.9 V
8.0 V	8.0 V	7.0 V

4.4 Input configurations

As described in Chapter 1, EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x are available in two different configurations with respect to the logic of the input pins.

The enable inputs are internally pulled up to a logic high voltage, i.e. the driver is enabled with these pins left open. The direct PWM inputs are internally pulled down to a logic low voltage. This prevents a switch-on event during power up and a not driven input condition. Version with inverted PWM input have an internal pull up resistor to prevent unwanted switch-on.

All inputs are compatible with LV-TTL levels and provide a hysteresis of 0.9 V typ. This hysteresis is independent of the supply voltage.

All input pins have a negative extended voltage range. This prevents cross-current over single wires during GND shifts between signal source (controller) and driver input.

4.5 Driver outputs

The two rail-to-rail output stages realized with complementary MOS transistors are able to provide a maximum sinking/sourcing current of 5 A (4 A output current versions are also available). This driver output stage has a shoot-through protection and current limiting behavior. After a switching event, current limitation is raised up to achieve the typical current peak for an excellent fast reaction time of the following power MOS transistor.

The output impedances for the sourcing p-channel MOS have typical values of 0.8 Ω for 2EDN753x and 2EDN853x and 1.0 Ω for 2EDN743x. The output impedances for the sinking n-channel MOS transistor have typical values of 0.6 Ω for 2EDN753x and 2EDN853x and 0.8 Ω for 2EDN743x. The use of a p-channel sourcing transistor is crucial for achieving true rail-to-rail behavior and avoiding a source follower's voltage drop.

Gate drive outputs are kept actively low in case of floating ENx or INx inputs, or during startup or power down if the supply voltage is below the UVLO threshold.

4.6 Active output voltage clamping

The undervoltage lockout (UVLO) protection ensures no driver operation when the supply voltage is below the UVLO threshold. However, this is not sufficient to keep output low when V_{DD} is far below the UVLO threshold. As a result, fast dv/dt of the switches could trigger undesired V_{gs} of the driven device, leading to abnormal turn-ons.

The fast active output voltage clamping of EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x is intended to actively keep the driver output low when the V_{DD} voltage is between 1.2V and $UVLO_{ON}$ threshold, overcoming the unwanted turnon issue listed above and ensuring safe off state before device operation.

This structure allows fast reaction and effective clamping of the output pins (OUTx). The exact reaction time depends on the power supply (V_{DD}) and on the output voltage levels. Undervoltage Lockout together with the output active clamping ensure that the output is actively held low in case of insufficient supply voltage.

Table 9 UVLO turn-on and turn-off thresholds

Inputs	Supplies	Output
INx	V_{DD}	OUTx
x	1.2 V < V_{DD} < $UVLO_{VDD,ON}$	L

5 Electrical characteristics

Note: *The absolute maximum ratings are listed in Table 10. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability*

5.1 Absolute maximum ratings

Table 10 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Positive supply voltage	V_{DD}	-0.3	-	22	V	1)
Voltage at pins INA, INB, ENA, ENB	V_{IN}	-12	-	22	V	-
Voltage at pins OUTA, OUTB	V_{OUT}	-0.3	-	V_{DD} +0.3	V	2)
		-2	-	V_{DD} +2	V	3) Repetitive pulse <200 ns
Reverse current peak at pins OUTA, OUTB	I_{SNKREV} I_{SRCREV}	-5 -	-	- 5	A_{pk}	<500 ns
Junction temperature	T_J	-40	-	150	°C	-
Storage temperature	T_S	-55	-	150	°C	-
ESD capability	V_{ESD}	-	-	0.5	kV	4) Charged Device Model (CDM)
ESD capability	V_{ESD}	-	-	2.0	kV	5) Human Body Model (HBM)

1) Maximum positive supply voltage already complies with derating requirements
2) Voltage spikes resulting from reverse current peaks are allowed
3) Values are verified by characterization on bench
4) According to JESD22-002
5) According to JESD22-A114-B (discharging 100 pF capacitor through 1.5 kΩ resistor)

5.2 Thermal characteristics

Table 11 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
PG-DSO-8, Tamb = 25°C						
Thermal resistance junction-ambient	R_{thJA25}	-	111	-	K/W	1)
Thermal resistance junction-case (top)	R_{thJC25}	-	66	-	K/W	2)
Thermal resistance junction-board	R_{thJB25}	-	59	-	K/W	3)
Characterization parameter junction-top	Ψ_{thJC25}	-	12	-	K/W	4)
Characterization parameter junction-board	Ψ_{thJB25}	-	57	-	K/W	5)
PG-TSSOP-8, Tamb = 25°C						
Thermal resistance junction-ambient	R_{thJA25}	-	48	-	K/W	1) 6)
Thermal resistance junction-case (top)	R_{thJP25}	-	74	-	K/W	2)
Thermal resistance junction-board	R_{thJB25}	-	22.5	-	K/W	3) 6)
Characterization parameter junction-top	Ψ_{thJC25}	-	3	-	K/W	4) 6)
Characterization parameter junction-board	Ψ_{thJB25}	-	21	-	K/W	5) 6)
PG-WSON-8, Tamb = 25°C						
Thermal resistance junction-ambient	R_{thJA25}	-	46	-	K/W	1) 6)
Thermal resistance junction-case (top)	R_{thJP25}	-	73	-	K/W	2)
Thermal resistance junction-board	R_{thJB25}	-	18	-	K/W	3) 6)
Characterization parameter junction-top	Ψ_{thJC25}	-	2	-	K/W	4) 6)
Characterization parameter junction-board	Ψ_{thJB25}	-	17.5	-	K/W	5) 6)
PG-SOT23-6, Tamb =25°C						
Thermal resistance junction-ambient	R_{thJA25}	-	163	-	K/W	1)
Thermal resistance junction-case(top)	R_{thJC25}	-	69	-	K/W	2)
Thermal resistance junction-board	R_{thJB25}	-	36	-	K/W	3)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Characterization parameter junction-case (top)	Ψ_{thJC25}	-	13	-	K/W	4)
Characterization parameter junction-board	Ψ_{thJB25}	-	36	-	K/W	5)
PG-TSNP-6, Tamb=25°C						
Thermal resistance junction-ambient	R_{thJA25}	-	140	-	K/W	1)
Thermal resistance junction-case(top)	R_{thJC25}	-	80	-	K/W	2)
Thermal resistance junction-board	R_{thJB25}	-	50	-	K/W	3)
Characterization parameter junction-case (top)	Ψ_{thJC25}	-	1.6	-	K/W	4)
Characterization parameter junction-board	Ψ_{thJB25}	-	35	-	K/W	5)

1)The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a

2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88

3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8

4) The characterization parameter junction-top, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Rth , using a procedure described in JESD51-2a (sections 6 and 7)

5) The characterization parameter junction-board, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Rth , using a procedure described in JESD51-2a (sections 6 and 7)

6) Characterization done on a JEDEC 2s2p PCB with thermal via array connected to the first inner copper layer under the exposed pad

5.3 Operating range

Table 12 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	4.5	-	20	V	1) Min. defined by UVLO
Logic input voltage	V_{IN}	-10	-	20	V	-
Junction temperature	T_J	-40	-	150	°C	2)

1) Maximum positive supply voltage already complies with derating requirements
2) Continuous operation above 125°C may reduce life time

5.4 General electric characteristics

Unless otherwise noted, min./max. values of characteristics are the lower and upper limits respectively. They are valid within the full operating range. The supply voltage is V_{DD} = 12 V. Typical values are given at T_J = 25°C.

Table 13 Power supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
V_{DD} quiescent current	I_{VDDQU1}	0.5	0.9	1.2	mA	OUT = high, V_{DD} = 12 V
V_{DD} quiescent current	I_{VDDQU2}	0.3	0.5	0.7	mA	OUT = low, V_{DD} = 12 V

Table 14 Undervoltage lockout for logic level MOSFET

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{ON}$	-	4.2	4.5	V	-
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{OFF}$	3.6	3.9	-	V	-
UVLO threshold hysteresis	$UVLO_{HYS}$	0.25	0.3	0.35	V	-

Table 15 Undervoltage lockout for standard and superjunction MOSFET version

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{ON}$	-	8.0	8.6	V	-
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{OFF}$	6.5	7.0	-	V	-
UVLO threshold hysteresis	$UVLO_{HYS}$	0.8	1.0	1.2	V	-

Table 16 Logic inputs INA, INB, ENA, ENB

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{INH}	1.9	2.1	2.3	V	-
Input voltage threshold for transition HL	V_{INL}	1.0	1.2	1.4	V	-
Input pull up resistor	R_{INH}	-	400	-	kΩ	1)
Input pull down resistor	R_{INL}	-	100	-	kΩ	2)

1) Inputs with initial high logic level
2) Inputs with initial low logic level

Table 17 Static output characteristics for 2EDN753x, 2EDN853x

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level (sourcing) output resistance	R_{ONSRC}	0.4	0.8	1.4	Ω	I_{SRC} = 50 mA
High level (sourcing) output current	$I_{SRCPEAK}$	-	5.0	-	A	1)
Low level (sinking) output resistance	R_{ONSNK}	0.35	0.6	1.2	Ω	I_{SNK} = 50 mA
Low level (sinking) output current	$I_{SNKPEAK}$	-	-5.0	-	A	1)

1) Parameter is not subject to production test - verified by design/characterization

Table 18 Static output characteristics for 2EDN743x

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level (sourcing) output resistance	R_{ONSRC}	0.5	1.0	1.7	Ω	I_{SRC} = 50 mA
High level (sourcing) output current	$I_{SRCPEAK}$	-	4.0	-	A	1)
Low level (sinking) output resistance	R_{ONSNK}	0.4	0.8	1.45	Ω	I_{SNK} = 50 mA
Low level (sinking) output current	$I_{SNKPEAK}$	-	-4.0	-	A	1)

1) Parameter is not subject to production test - verified by design/characterization

Table 19 Dynamic Characteristic (see Figure 10, Figure 11, Figure 12, Figure 13)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input/Enable to output propagation delay	t_{PDlh}	15	19	25	ns	C_{LOAD} = 1.8 nF, V_{DD} = 12 V; Low to high transition at Input/Enable
Input/Enable to output propagation delay	t_{PDhl}	15	19	25	ns	C_{LOAD} = 1.8 nF, V_{DD} = 12 V High to low transition at Input/Enable
Input/Enable to output propagation delay mismatch between the two channels on the same IC	Δt_{PD}	-	-	2	ns	-
Rise time	t_{RISE}	-	8.6	15	ns	[1] C_{LOAD} = 1.8 nF, V_{DD} = 12 V
Fall time	t_{FALL}	-	6	13	ns	[1] C_{LOAD} = 1.8 nF, V_{DD} = 12 V
Minimum input pulse width that changes output state	t_{PW}	-	-	15	ns	[1] C_{LOAD} = 1.8 nF, V_{DD} = 12 V
V_{DD} start-up time from $UVLO_{ON}$ to OUT_x	t_{START}	-	1.8	-	µs	[1] V_{DD} rising to 12 V; see Figure 12
V_{DD} deactivation time from $UVLO_{OFF}$ to OUT_x	t_{STOP}	-	500	-	ns	[1] V_{DD} falling from 12 V; see Figure 12
Activation time of output clamping in UVLO condition	$t_{CLAMP,OUT}$	-	30	-	ns	[1] see Figure 14

1) Parameter is not subject to production test-verified by component verification

6 Timing diagrams

Figure 10 shows the definition of rise, fall and delay times for the inputs of the non-inverting/direct version (with enable pin high or open).

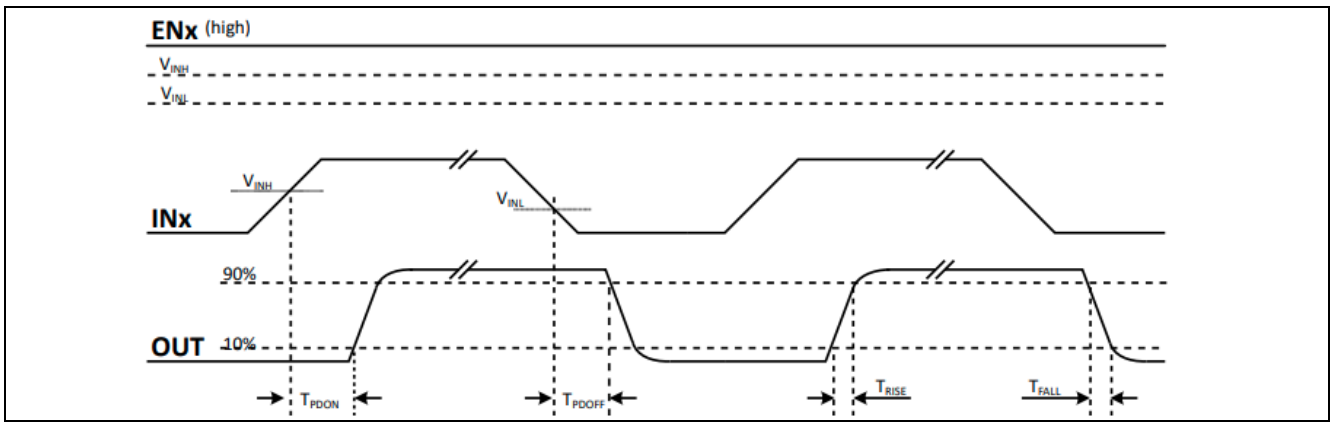

Figure 10 Propagation delay, rise and fall time definition for the direct/non-inverting configuration

Figure 11 shows the definition of rise, fall and delay times for the inputs of the inverting version (with enable pins high or open).

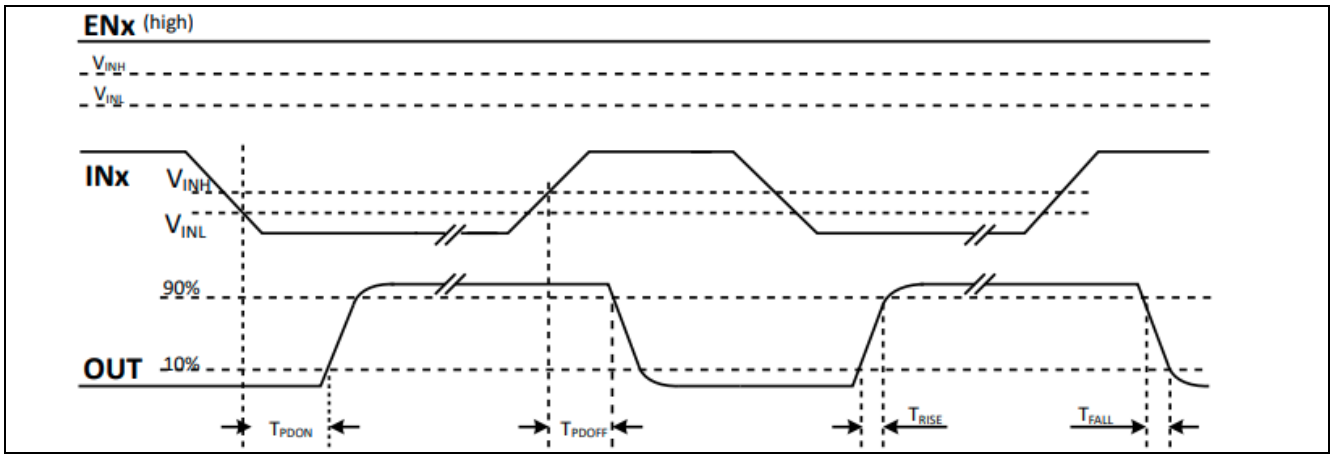

Figure 11 Propagation delay, rise and fall time definition for the inverting configuration

Figure 12 illustrates the undervoltage lockout function.

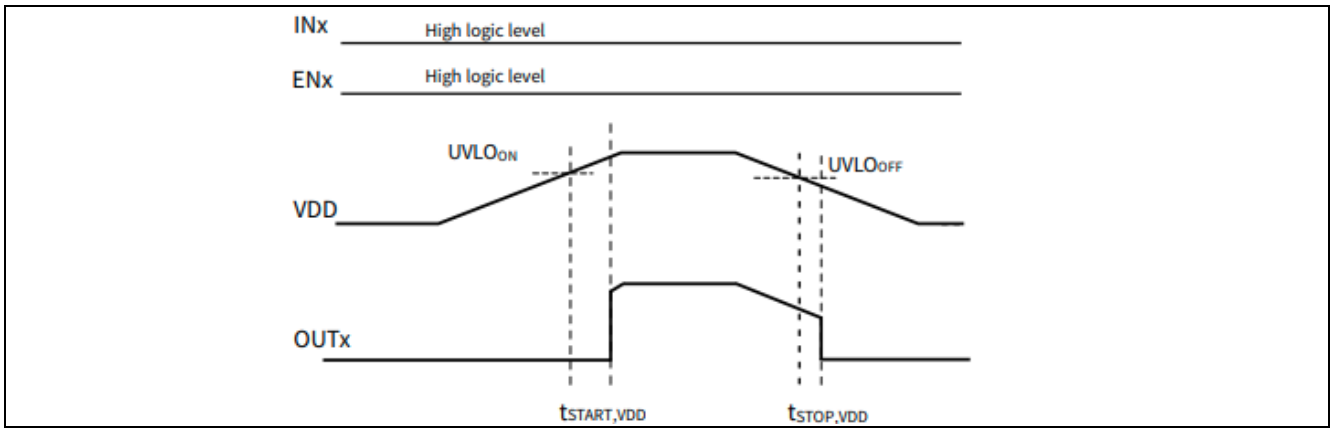

Figure 12 UVLO behaviour, input ENx and INx drives OUTx normally high

Figure 13 illustrates the minimum input pulse width that changes output state.

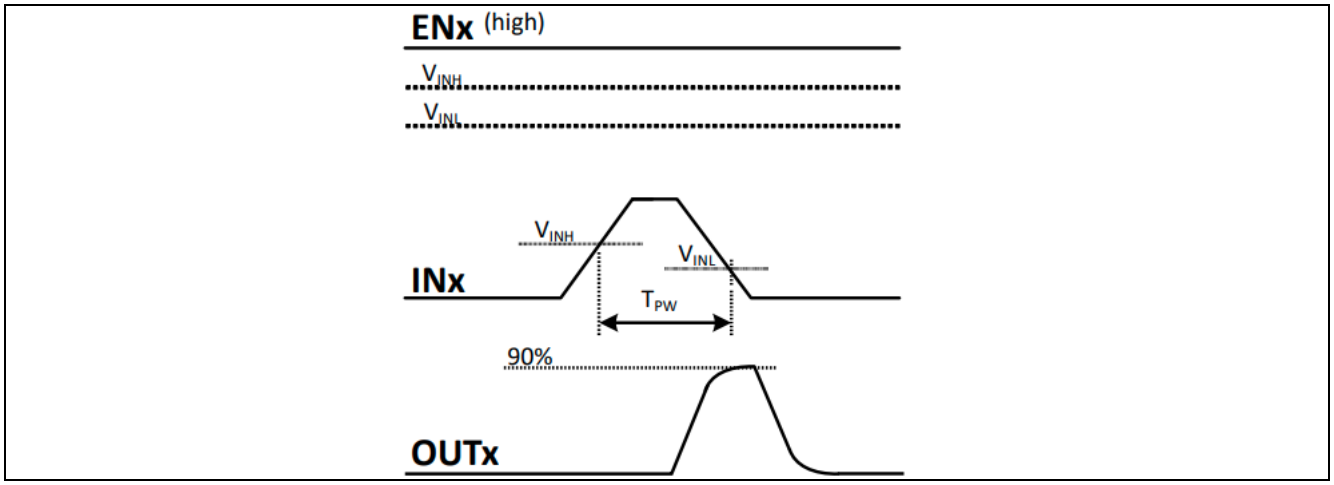

Figure 13 Minimum input pulse width definition

Figure 14 illustrates $t_{CLAMP,OUT}$, the time required to clamp potential output induced overshoots in UVLO condition (V_{DD} < $UVLO_{ON}$)

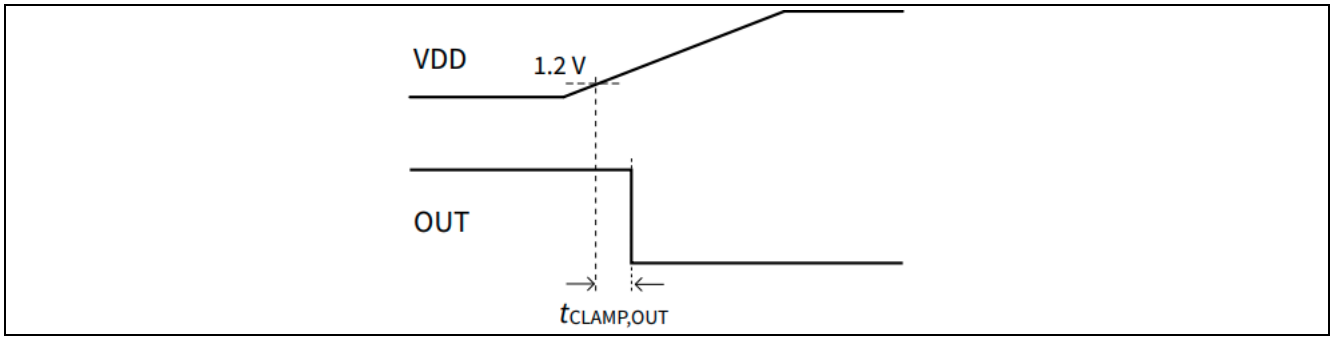

Figure 14 Activation time of output clamping in UVLO conditions (unloaded output)

7 Typical characteristics

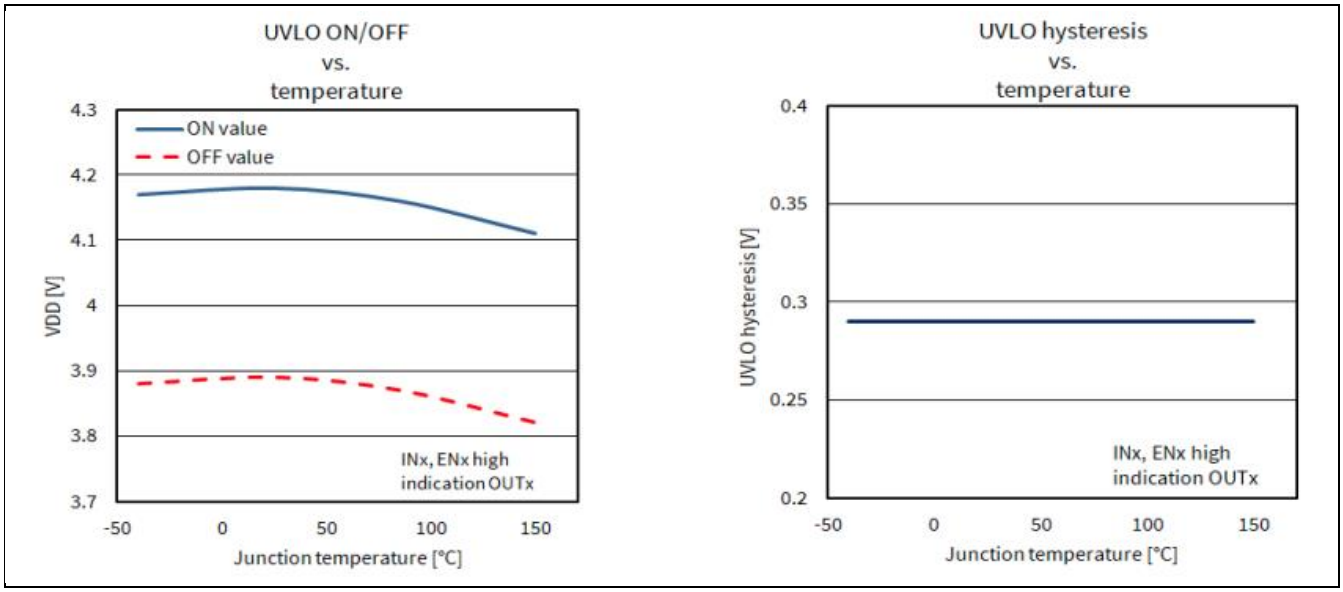

Figure 15 Typical undervoltage lockout behavior vs. temperature for 2EDN7x (4 V)

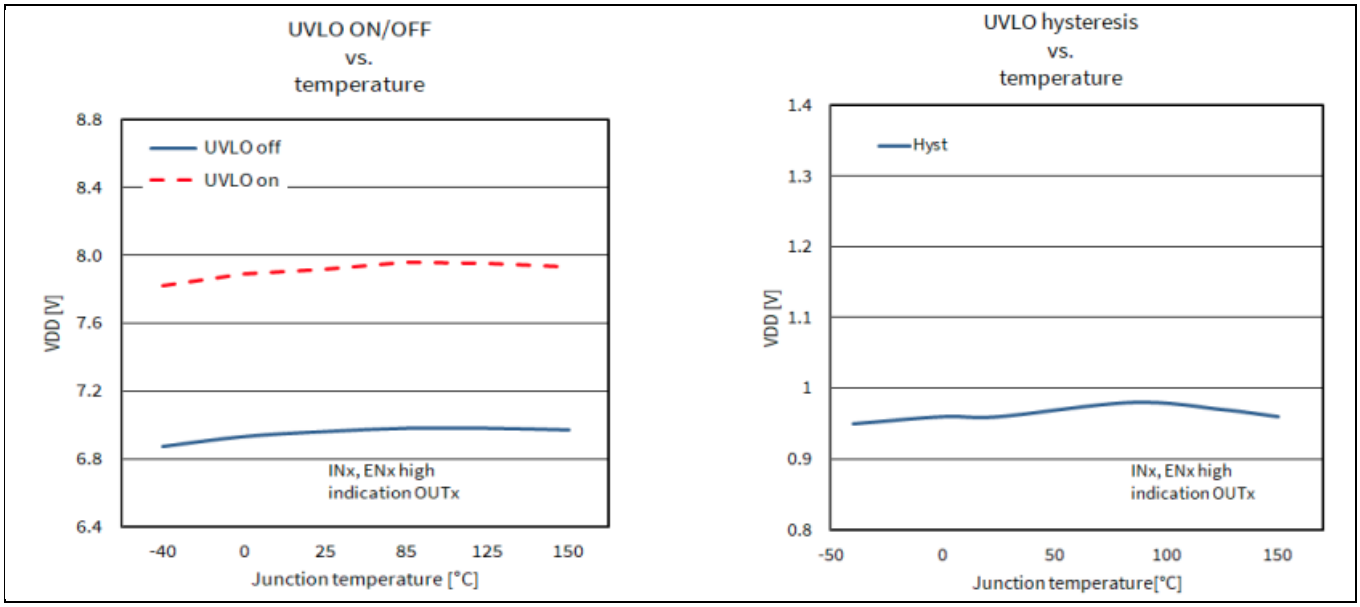

Figure 16 Typical undervoltage lockout behavior vs. temperature for 2EDN8x (9 V)

Typical characteristics

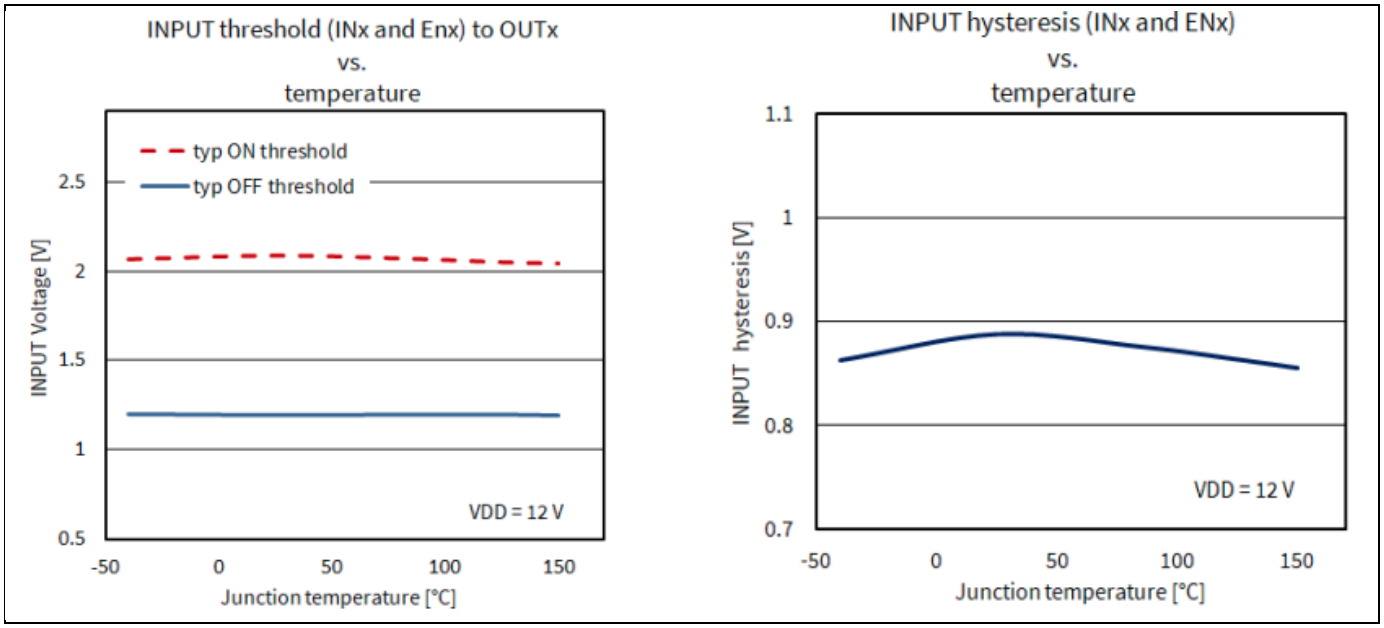

Figure 17 Input characteristics (Inx and ENx)

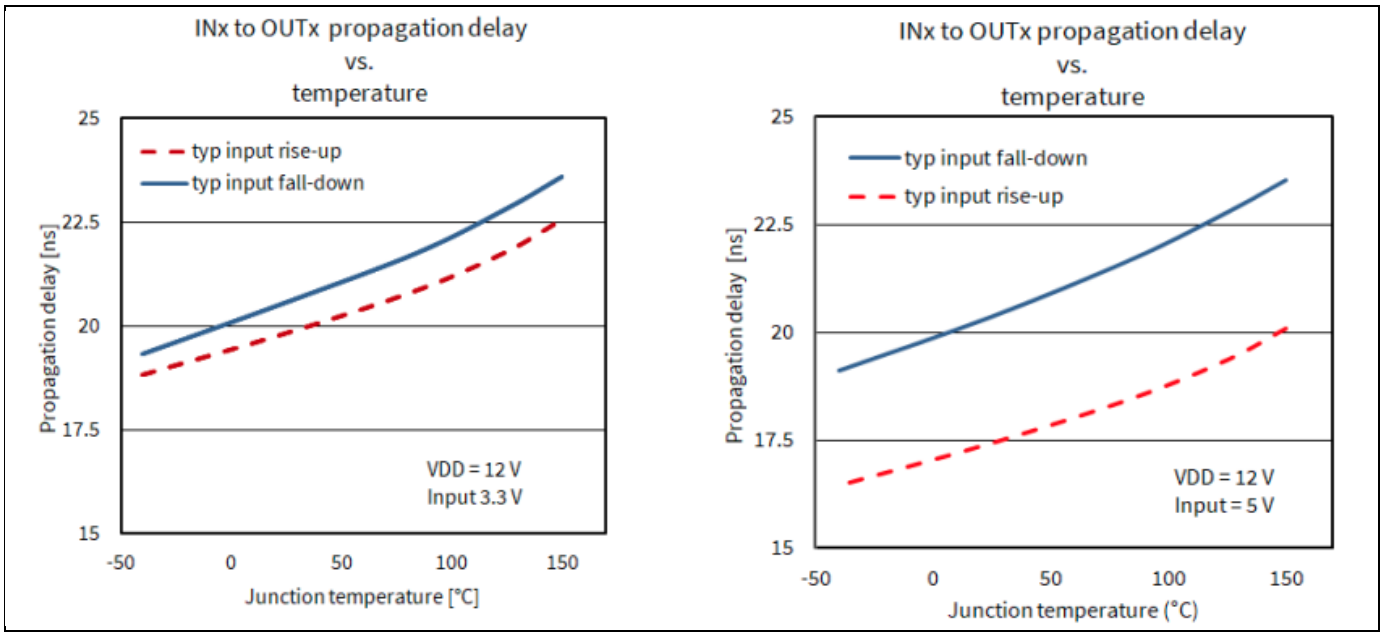

Figure 18 Propagation delay (INx) on different input logic levels (see Figure 10)

Typical characteristics

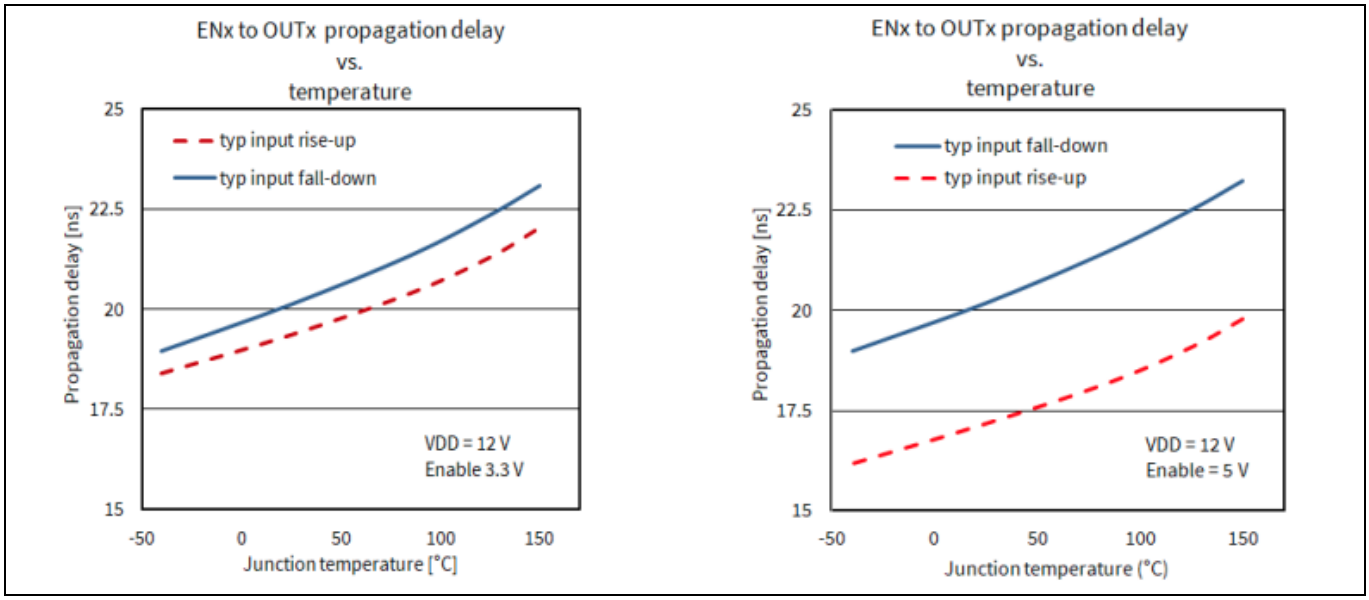

Figure 19 Propagation delay (ENx) on different input logic levels (see Figure 11)

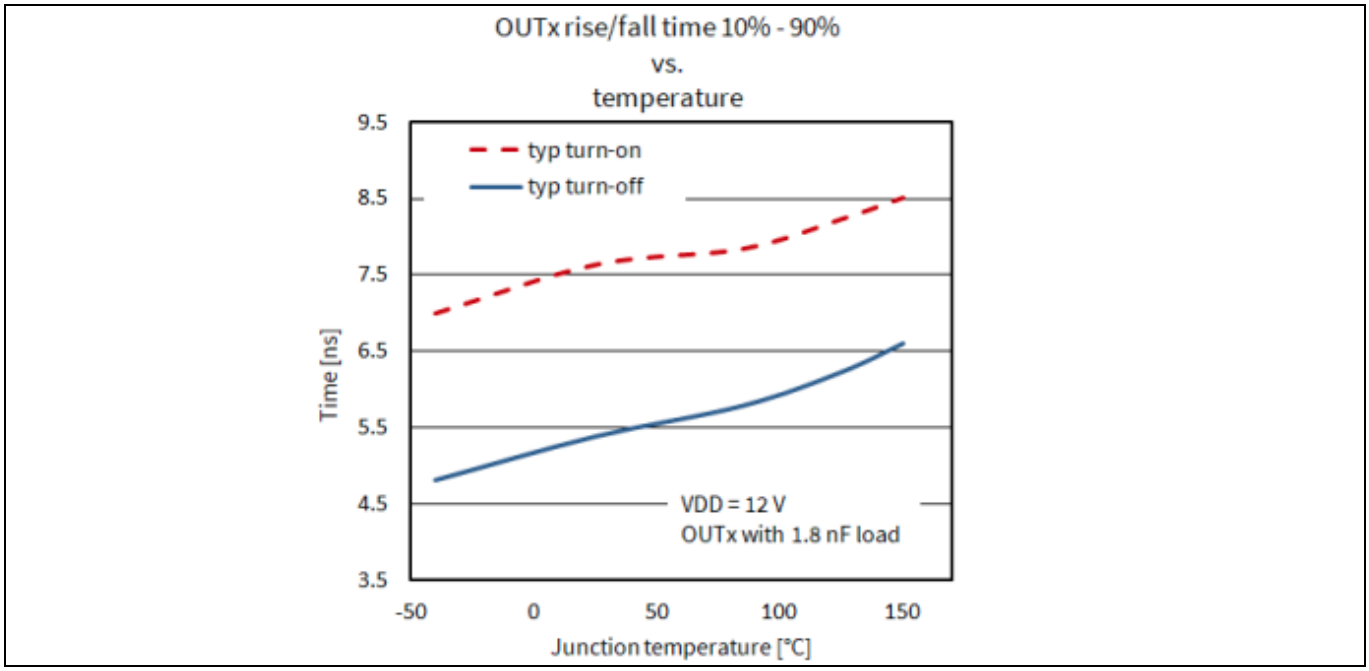

Figure 20 Rise/fall times with load on output(see Figure 10)

Typical characteristics

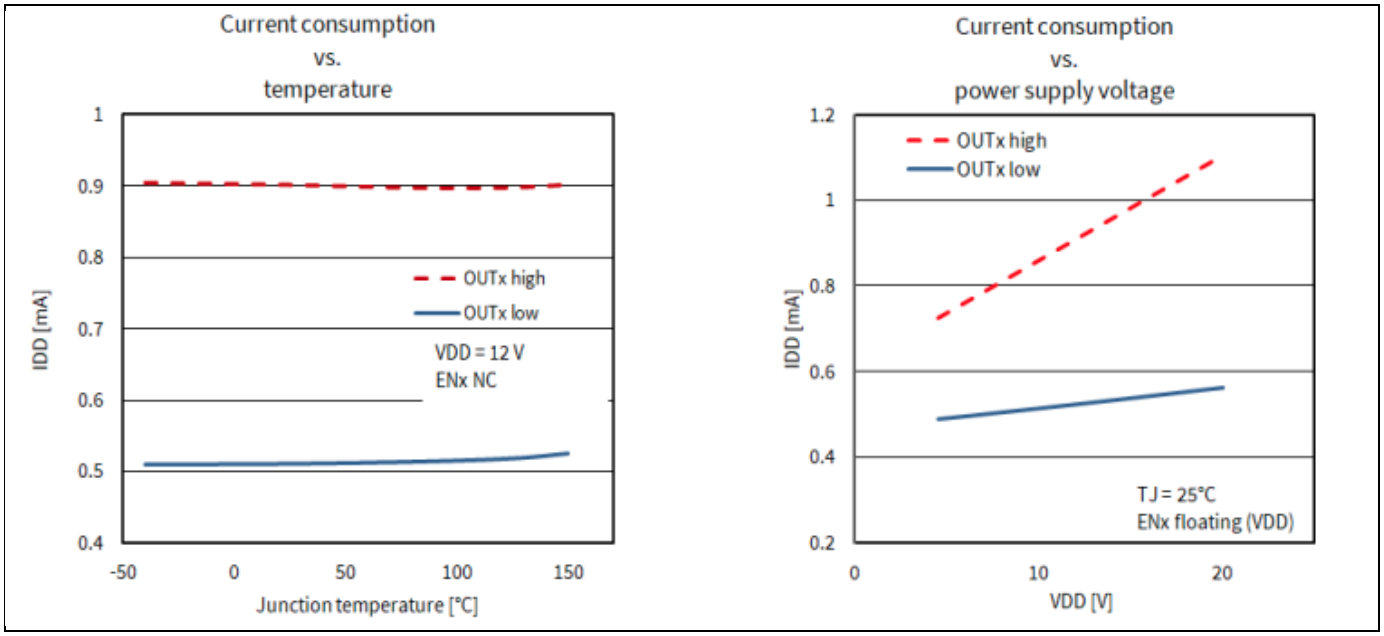

Figure 21 Power consumption related to temperature and power supply

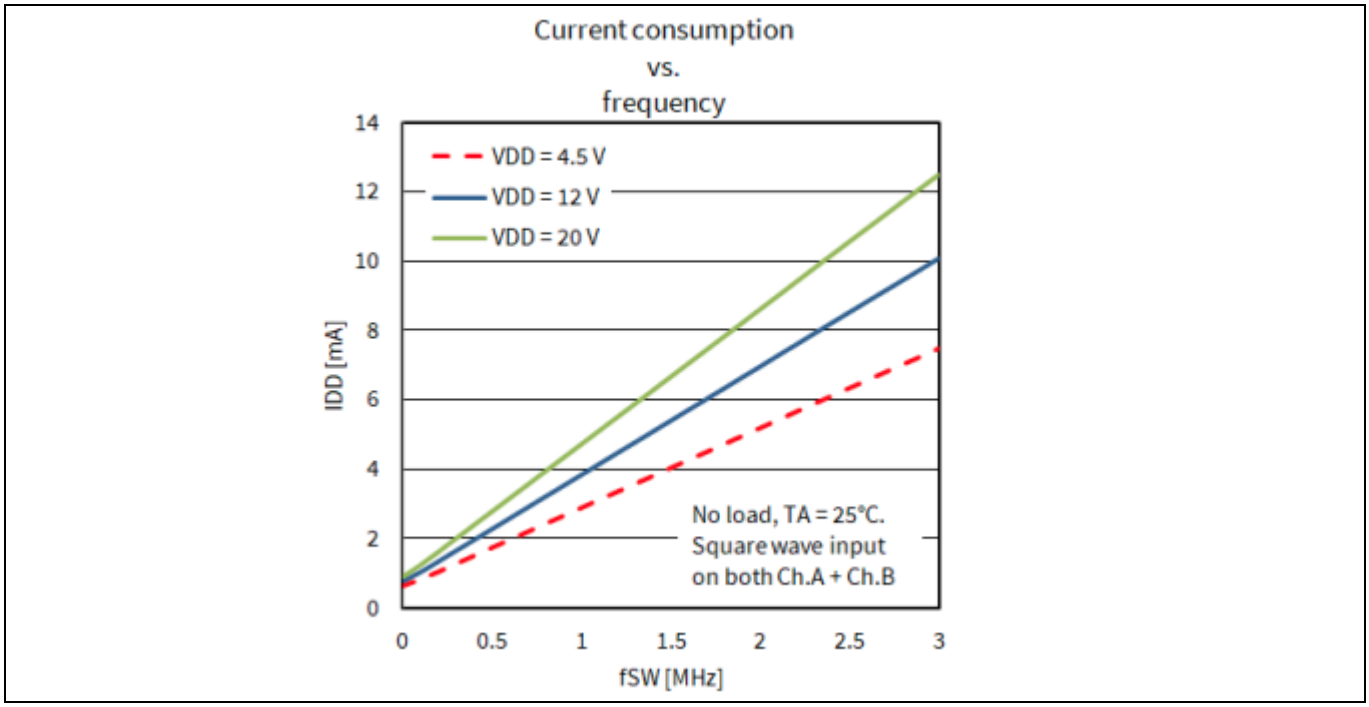

Figure 22 Current consumption versus frequency

8 Application and implementation

Note: *The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device*

8.1 Typical application

The EiceDRIVER™ 2EDN753x/2EDN853x/2EDN743x is a fast and high-performance dual-channel driver designed for low-side switches. Each output channel can sink and source 5 A currents, thanks to its true rail-to-rail stage. This results in very low on-resistance values and lower power dissipation.

The tight channel-to-channel delay matching of 1 ns (typical) allows for parallel use of the two channels, providing a combined source and sink capability of 10 A. However, when using the channels in parallel mode, be aware that there may be differences in the input threshold voltage level between the two channels, which can cause delays and shoot-through in the output, especially when slow dV/dt input signals are used. To avoid cross-conduction currents in the device output stages, the rise and fall times of the input signals must be less than 100 ns (10 to 90 percent). This ensures optimal performance and reliability when using the 2EDN dual-channel driver.

Figure 23 and Figure 24 show typical applications for the 8-pin and 6-pin package versions respectively.

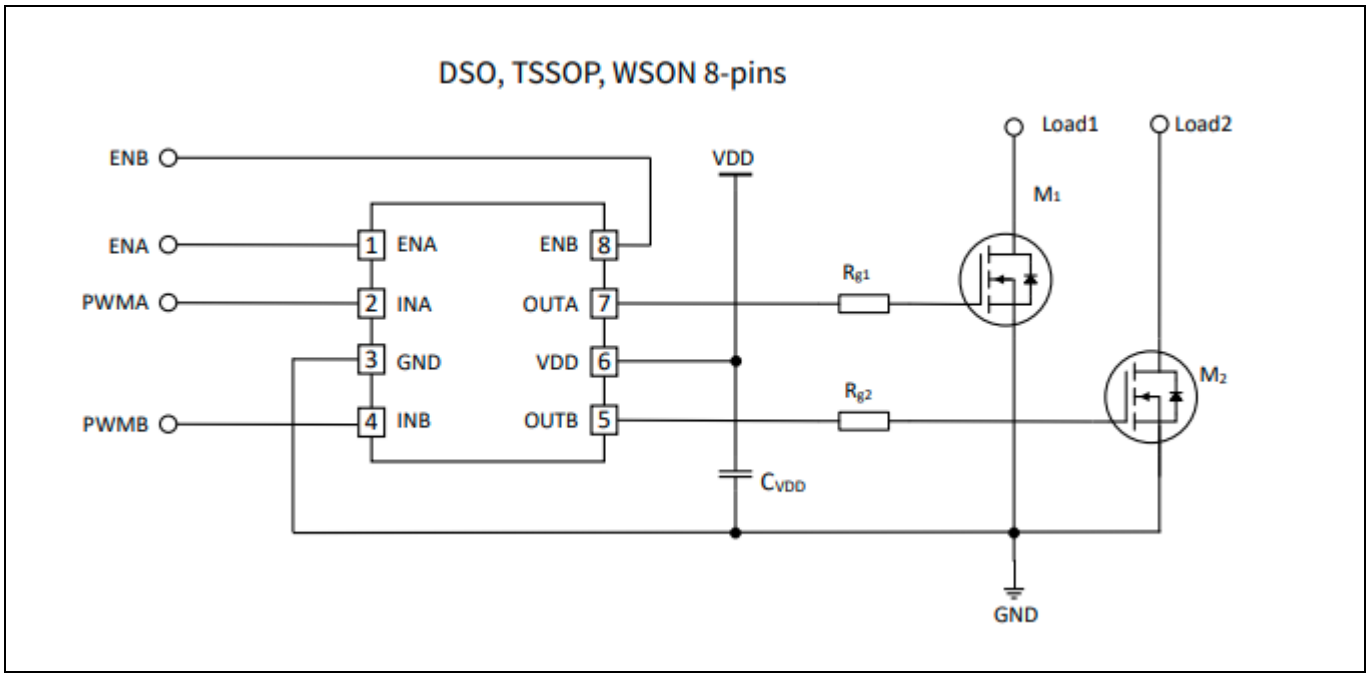

Figure 23 Typical application for 8-pin packages

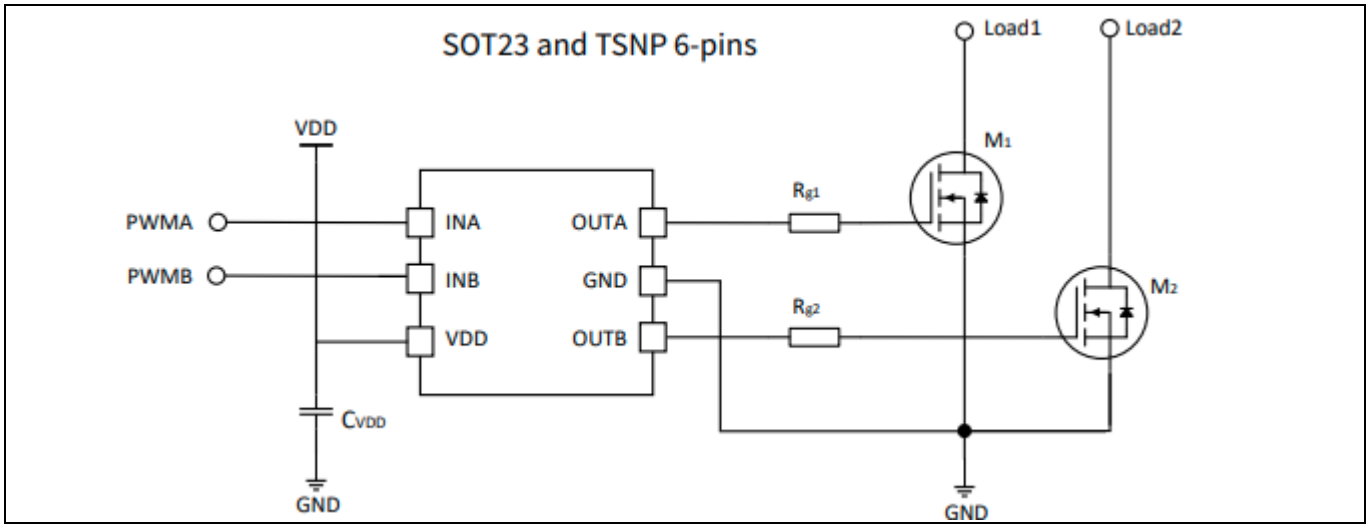

Figure 24 Typical application for 6-pin packages

8.2 PCB layout recommendations

Good PCB layout is essential for high-current, fast-switching devices to ensure optimal functioning of the design along with providing robustness during transient events. Due to the powerful output stages of the 2EDN, it is capable of delivering large current peaks with very fast rise and fall times at the gate of the power MOSFET to facilitate very fast voltage transitions. However, the high di/dt can cause significant ringing if the trace lengths and impedances are beyond recommended limits.

The following layout guidelines are recommended to prevent any issues:

- The driver should be placed as close as possible to switching MOSFET in order to minimize the length of any high-current traces between the driver output pins and the gate of MOSFET.
- The V_{DD} bypass capacitors between V_{DD} and GND should be as close as possible to the driver with minimal trace lengths to improve the noise filtering. These capacitors support high peak current being drawn from V_{DD} during turn-on of MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (MOSFET driver, MOSFET and V_{DD} bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops during turn-on and turn-off transients, which will induce significant voltage transients on the output pin of the driver device and the gate of the MOSFET.
- Parallel the source and return traces, taking advantage of flux cancellation, if feasible, while routing the tracks. Separate power traces and signal traces, such as output and input signals.
- Use a ground plane to provide noise shielding. Fast rise and fall times at the output may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can act as a heatsink and assist in power dissipation.
- In noisy environments, connect the input of an unused channel of the 2EDN to GND (using short traces) to ensure that the output of that channel is disabled and prevent noise from causing malfunction in that output. This is particularly necessary when testing the capabilities of each channel individually.

8.3 Thermal considerations

The 2EDN family of gate drivers is designed for various application requirements, with their performance being influenced by the load's power requirements and the device package's thermal characteristics. The strong output stage of these drivers contributes to their ability to operate at lower temperatures.

To ensure effective operation over a specific temperature range, the gate driver package must facilitate efficient heat removal while maintaining the junction temperature within the rated limits. The 2EDN family comes in different packages to accommodate diverse application needs. The TSSOP-8 and WSON-8 packages dissipate heat from the semiconductor junction through the bottom of the package, featuring an exposed thermal pad at the base.

This thermal pad is soldered to the copper on the printed circuit board (PCB) directly beneath the device package, significantly reducing thermal resistance and improving heatsinking. It is generally recommended to connect the exposed pad to GND in the PCB layout for better electromagnetic interference (EMI) immunity.

In summary, the 2EDN family of gate drivers offers various package options to address a wide range of application requirements, with the TSSOP-8 and WSON-8 packages providing efficient heat removal and improved thermal performance

9 Package outlines

Note: *For further information on package types, recommendation for board assembly, please go to:* www.Infineon.com.

9.1 Device numbers and markings

Table 20 Product versions

Part number	Orderable part number (OPN)	Device marking
2EDN7534F	2EDN7534FXTMA1	2N7534AF EiceDRIV XXHYYWW
2EDN7434F	2EDN7434FXTMA1	2N7434AF EiceDRIV XXHYYWW
2EDN7533F	2EDN7533FXTMA1	2N7533AF EiceDRIV XXHYYWW
2EDN8534F	2EDN8534FXTMA1	2N8534AF EiceDRIV XXHYYWW
2EDN8533F	2EDN8533FXTMA1	2N8533AF EiceDRIV XXHYYWW
2EDN7534R	2EDN7534RXTMA1	2N7534 AR HYYWW
2EDN7434R	2EDN7434RXTMA1	2N7434 AR HYYWW
2EDN7533R	2EDN7533RXTMA1	2N7533 AR HYYWW
2EDN8534R	2EDN8534RXTMA1	2N8534 AR HYYWW
2EDN8533R	2EDN8533RXTMA1	2N8533 AR HYYWW

Part number	Orderable part number (OPN)	Device marking
(table continues...)		
2EDN7534G	2EDN7534GXTMA1	2N7534 AG HYYWW
2EDN7534B	2EDN7534BXTSA1	[1] YW 754
2EDN7533B	2EDN7533BXTSA1	[1] YW 753
2EDN7534U	2EDN7534UXTSA1	[1] YW 54

1) The date code digits "Y" and "W" in device marking for the SOT23-6 package are explained in Table 21 and Table 22

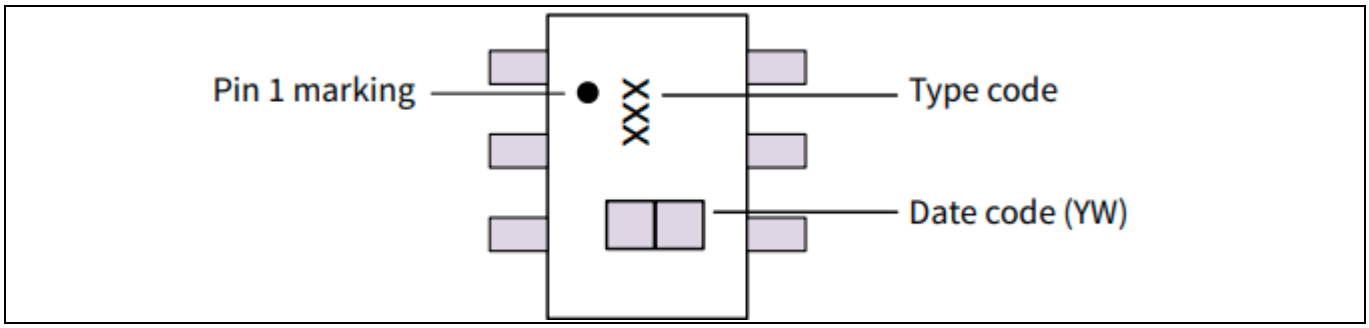

Figure 25 Package marking (PG-SOT23-6)

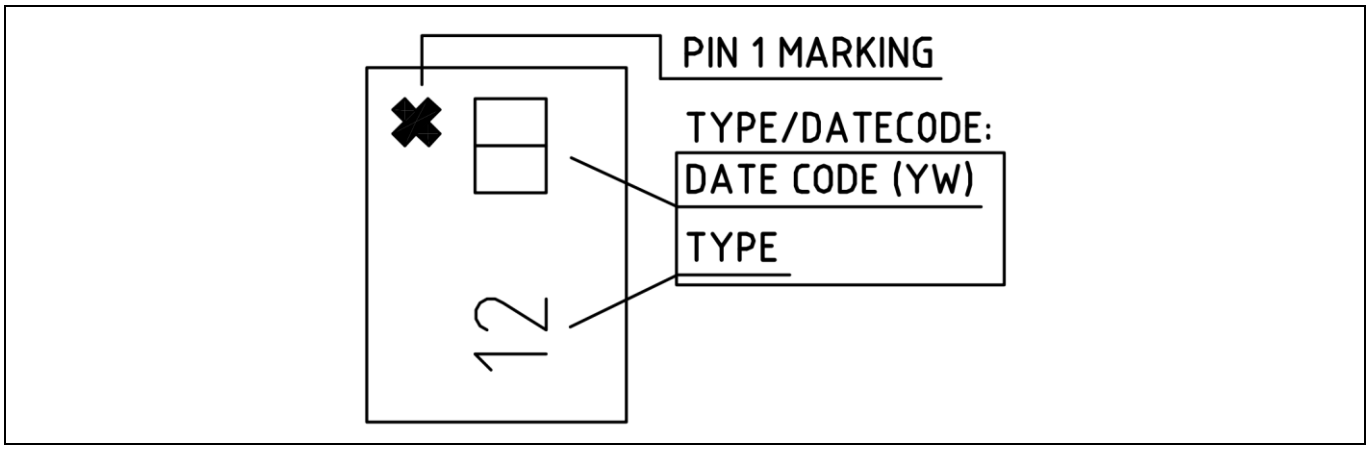

Figure 26 Package marking (PG-TSNP-6)

Table 21 Year date code marking - digit "Y"

Year	Y	Year	Y	Year	Y
2000	0	2010	0	2020	0
2001	1	2011	1	2021	1
2002	2	2012	2	2022	2
2003	3	2013	3	2023	3
2004	4	2014	4	2024	4
2005	5	2015	5	2025	5
2006	6	2016	6	2026	6
2007	7	2017	7	2027	7
2008	8	2018	8	2028	8
2009	9	2019	9	2029	9

Table 22 Week date code marking - digit "W"

Week	W	Week	W	Week	W	Week	Year	Week	W
1	A	12	N	23	4	34	h	45	V
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	*25*	6	*36*	k	*47*	*Y*
4	D	15	R	*26*	7	*37*	l	*48*	*Z*
5	E	16	S	*27*	a	*38*	n	*49*	*8*
6	F	17	T	*28*	b	*39*	p	*50*	*9*
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	-	-
10	K	21	Y	32	f	43	t	-	-
11	L	22	Z	33	g	44	u	-	-

9.2 PG-DSO-8

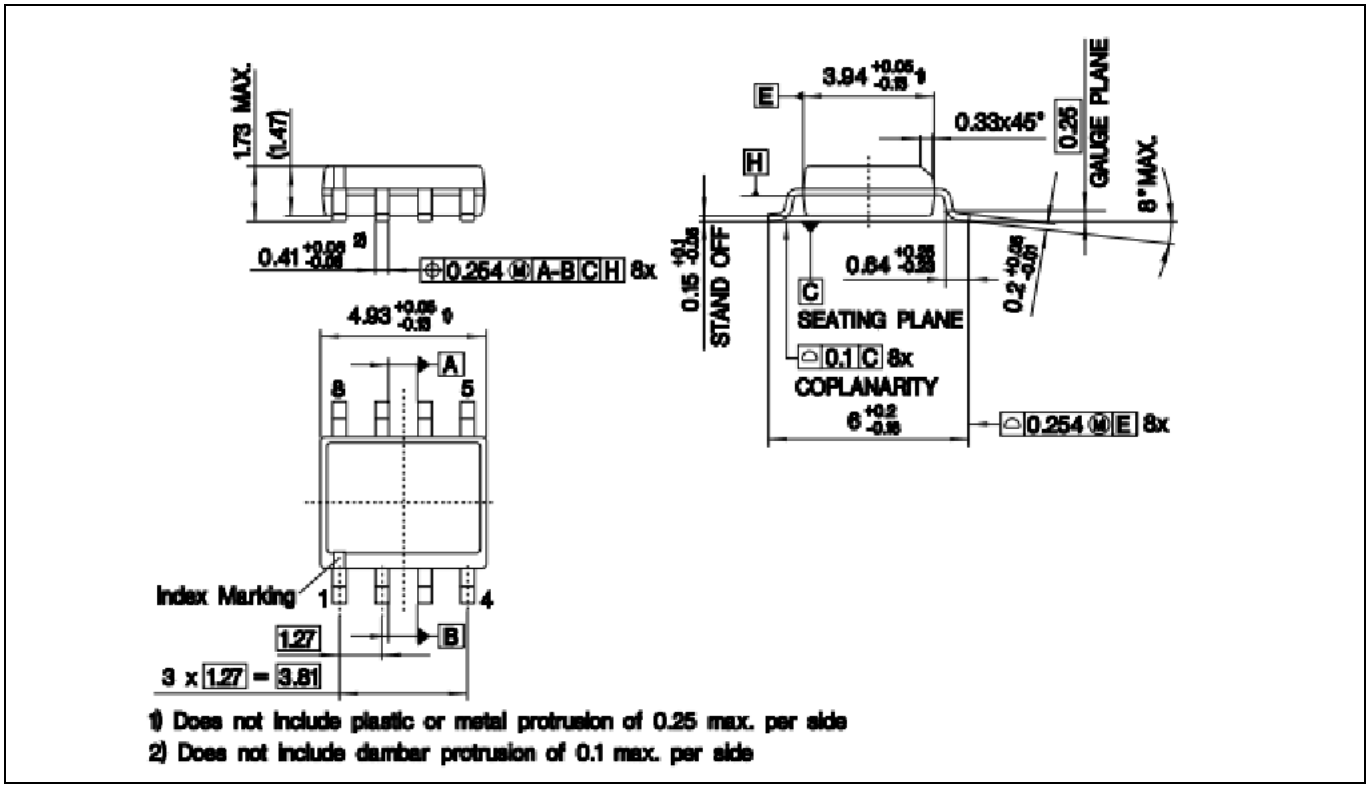

Figure 27 Package marking (PG-TSNP-6)

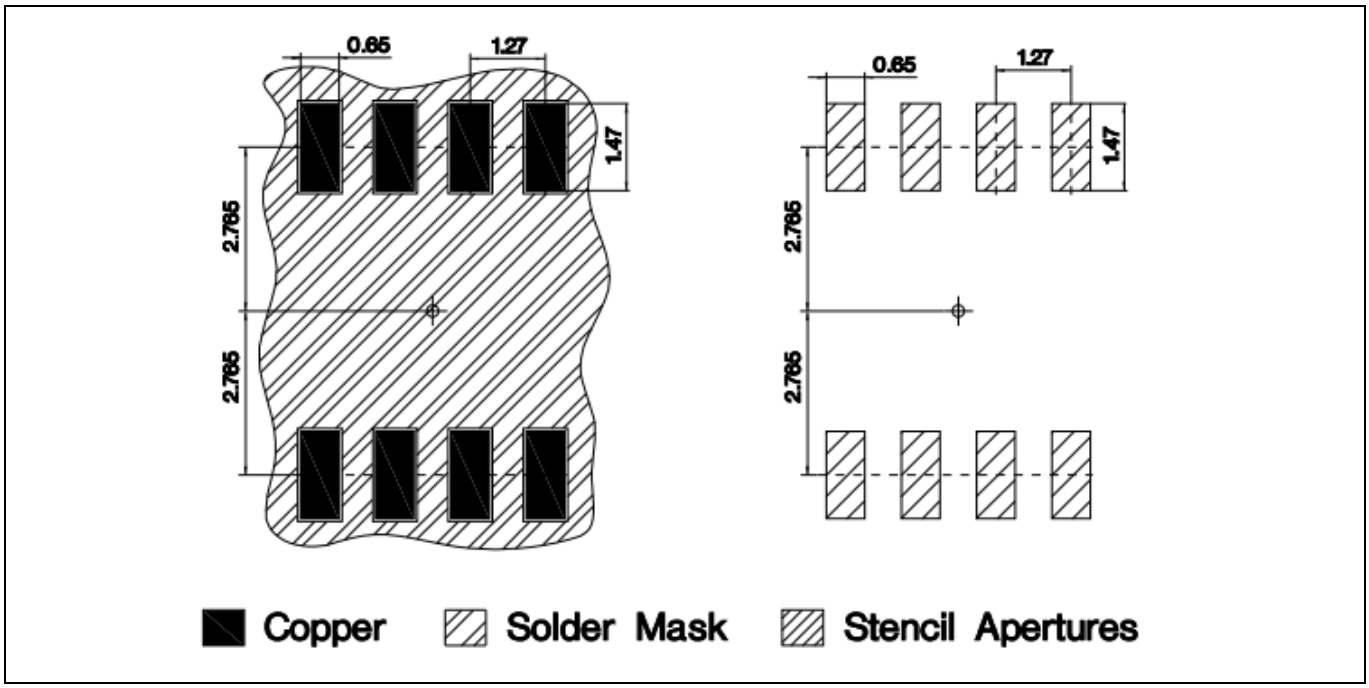

Figure 28 PG-DSO-8 footprint

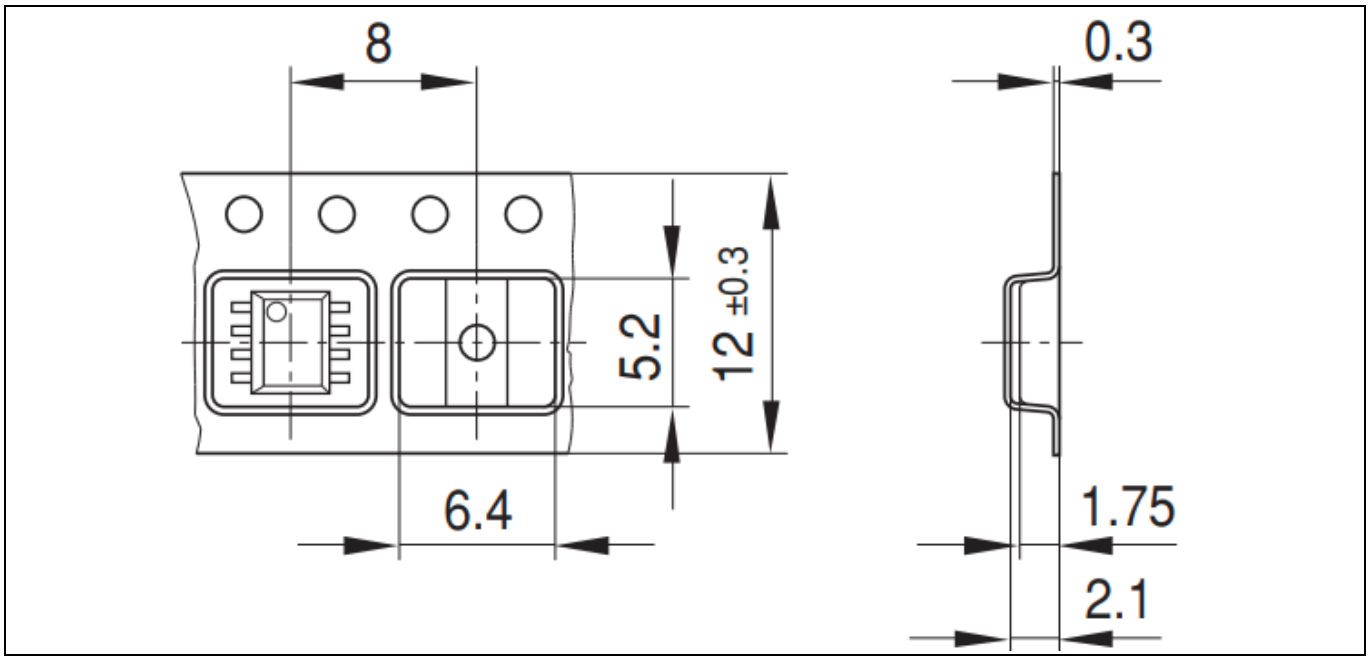

Figure 29 PG-DSO-8 packaging

9.3 PG-TSSOP-8

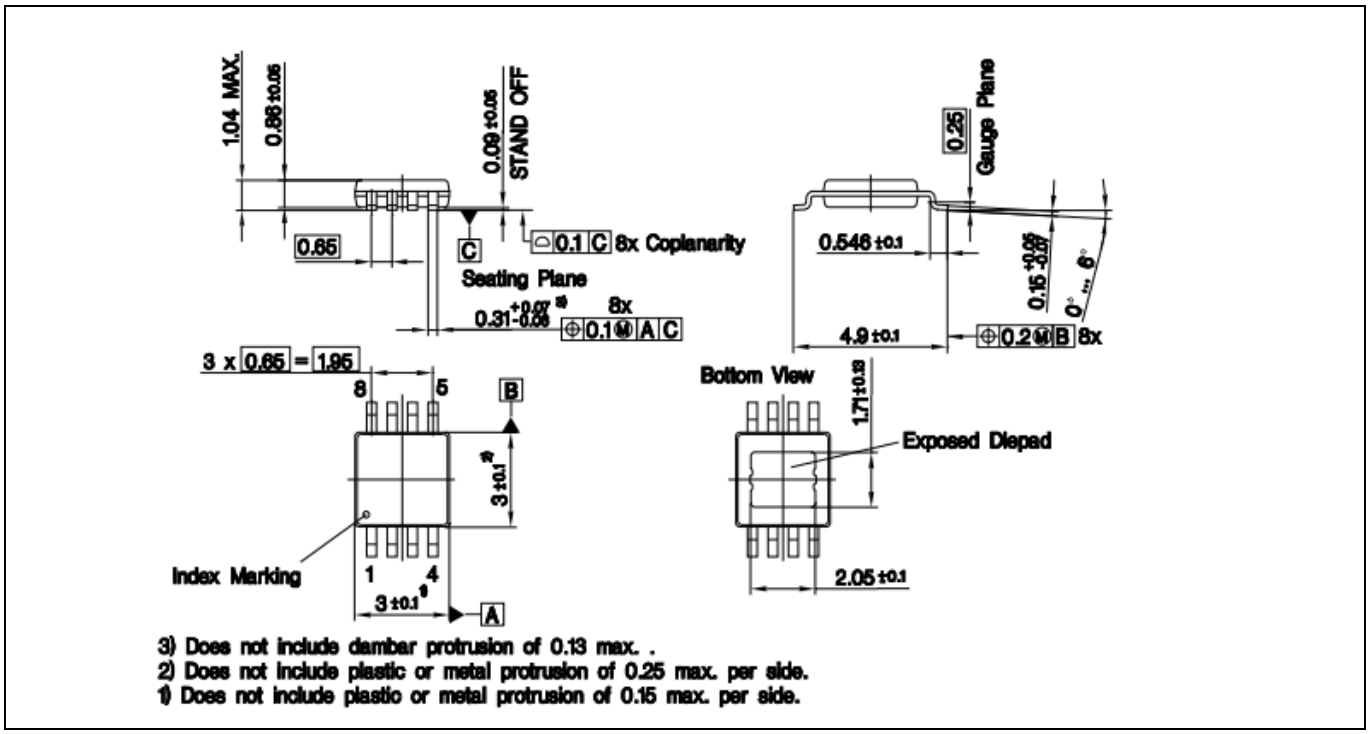

Figure 30 PG-TSSOP-8 outline

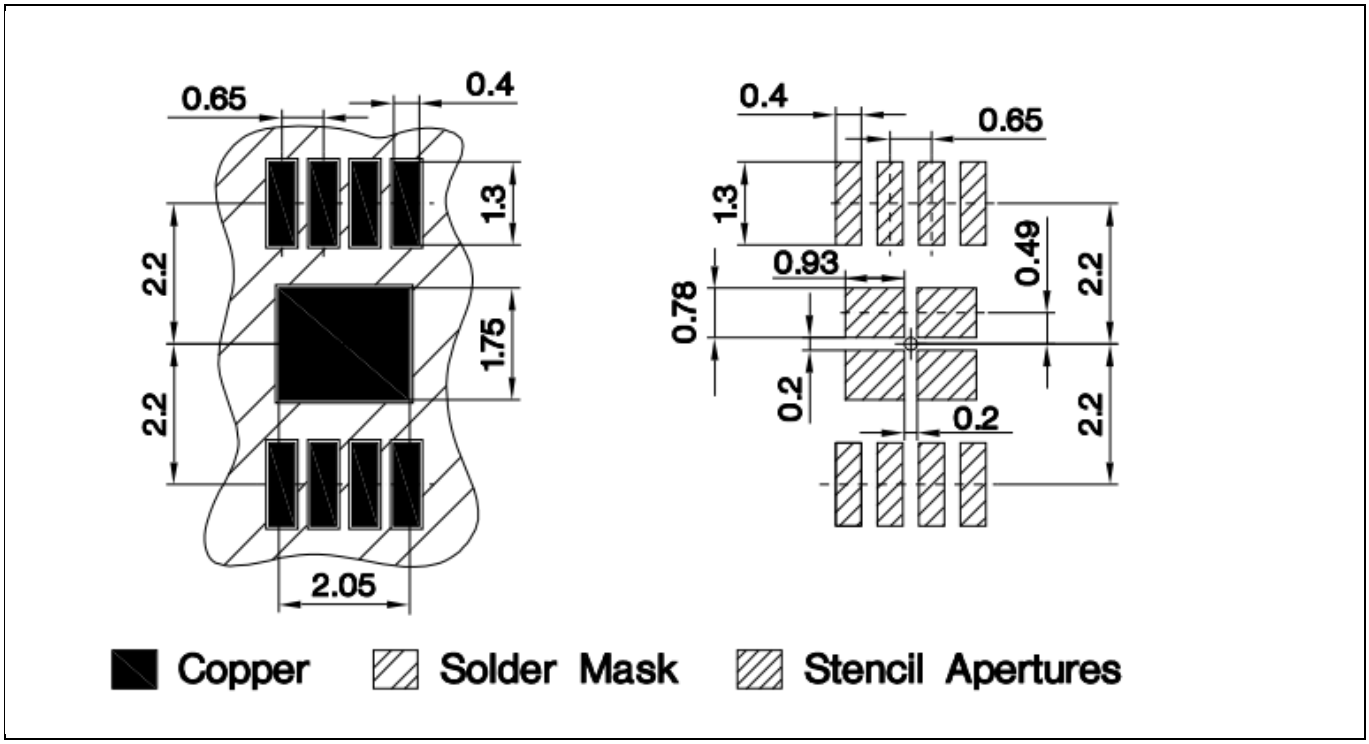

Figure 31 PG-TSSOP-8 footprint

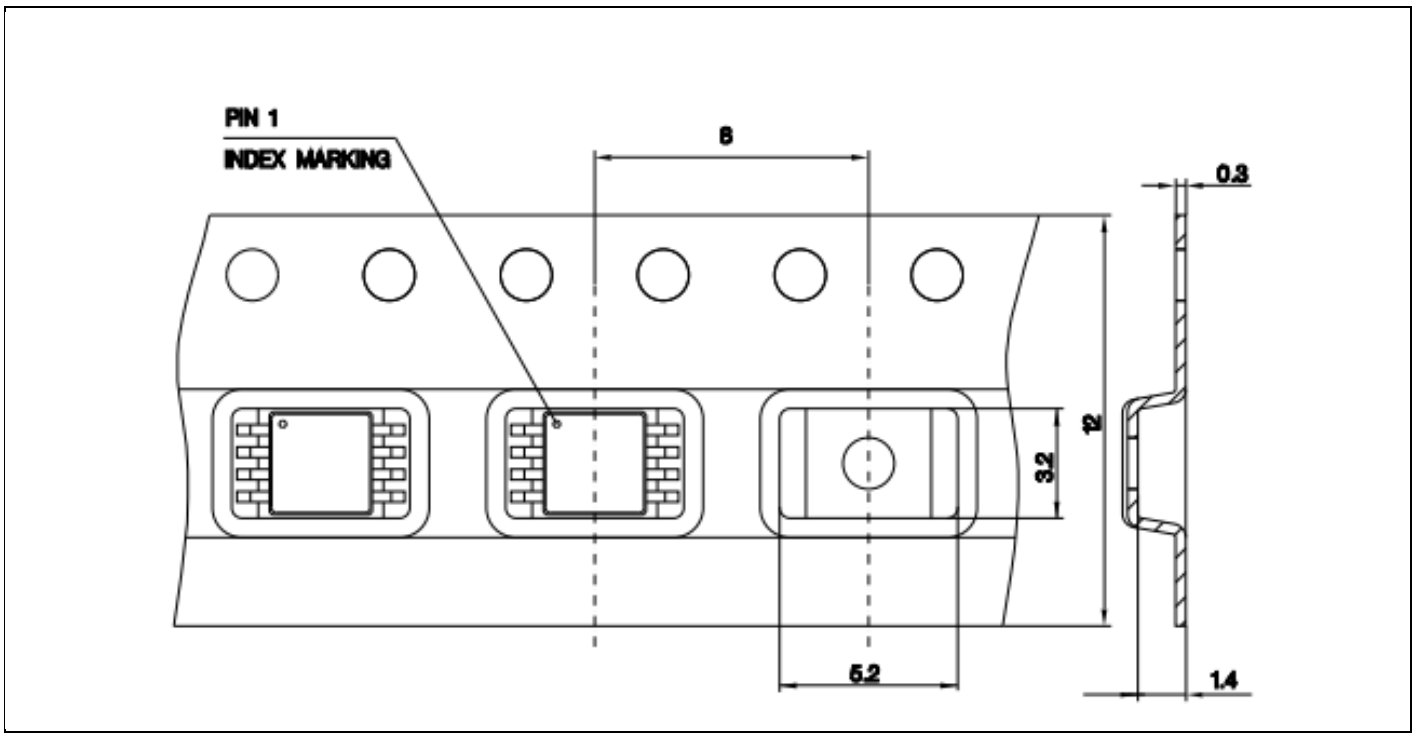

Figure 32 PG-TSSOP-8 packaging

9.4 PG-WSON-8

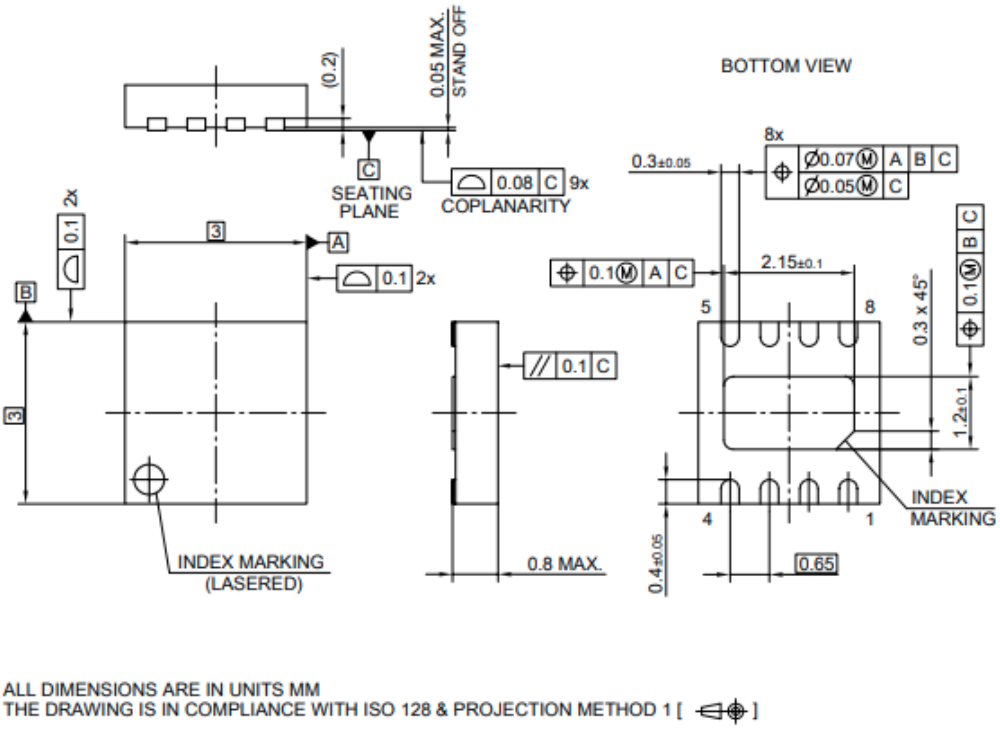

Figure 33 PG-WSON-8 outline

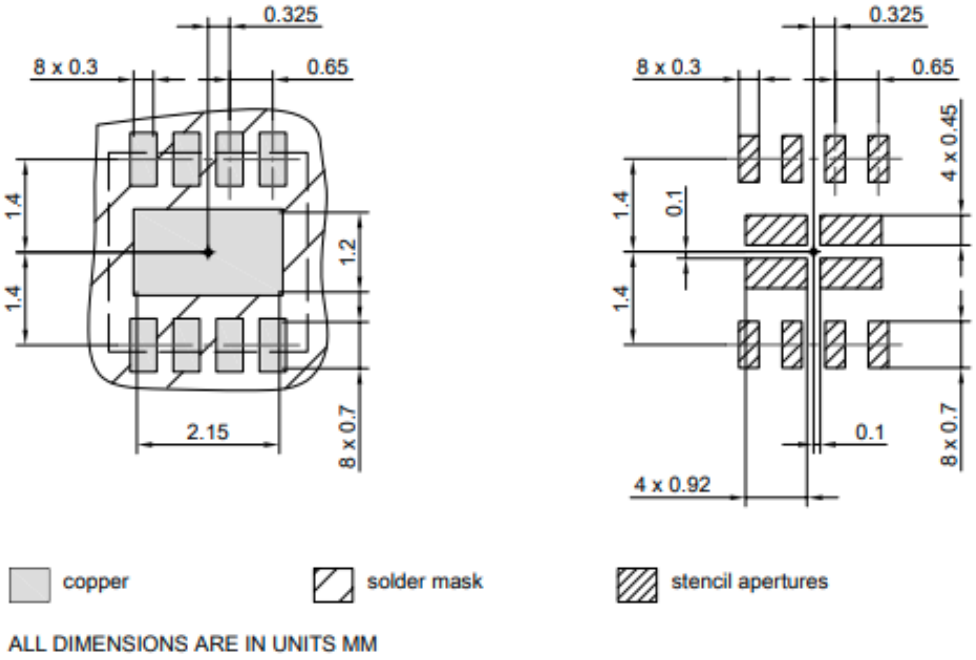

Figure 34 PG-WSON-8 footprint

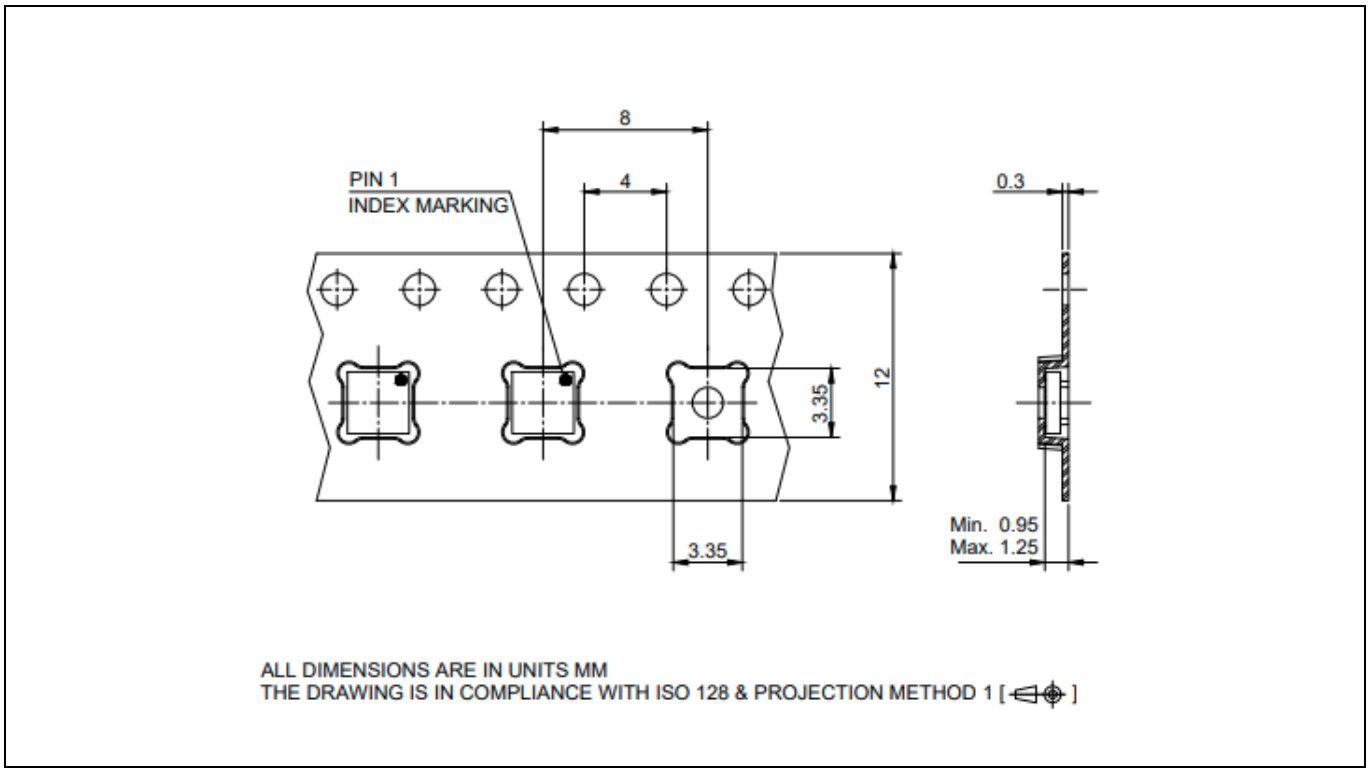

Figure 35 PG-WSON-8 packaging

9.5 PG-SOT23-6

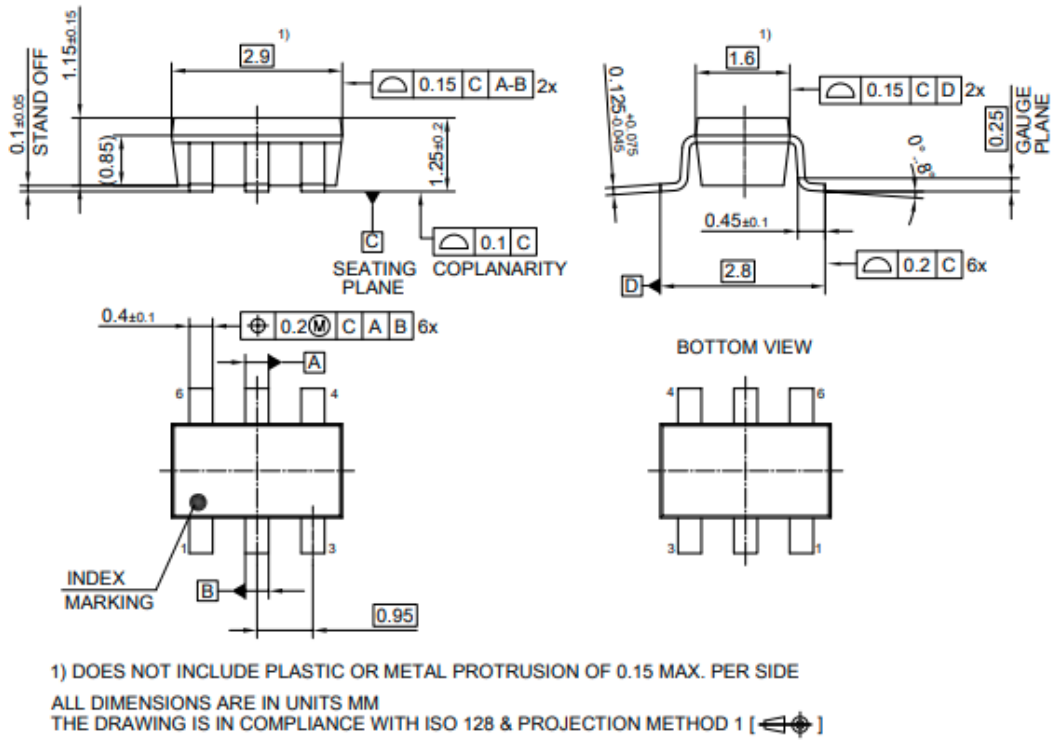

Figure 36 PG-SOT23-6 outline

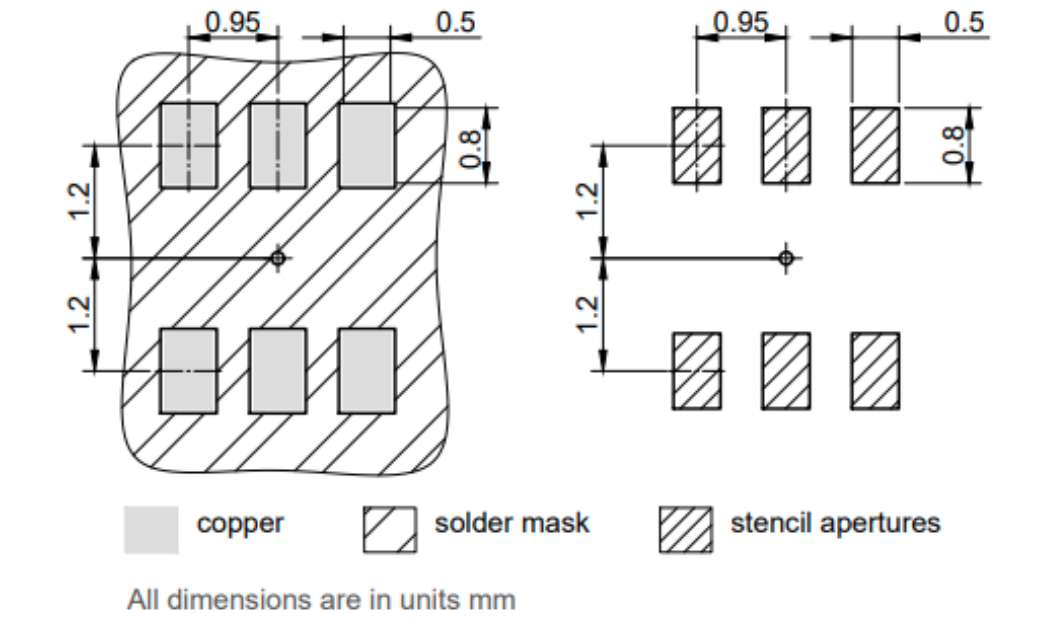

Figure 37 PG-SOT23-6 footprint

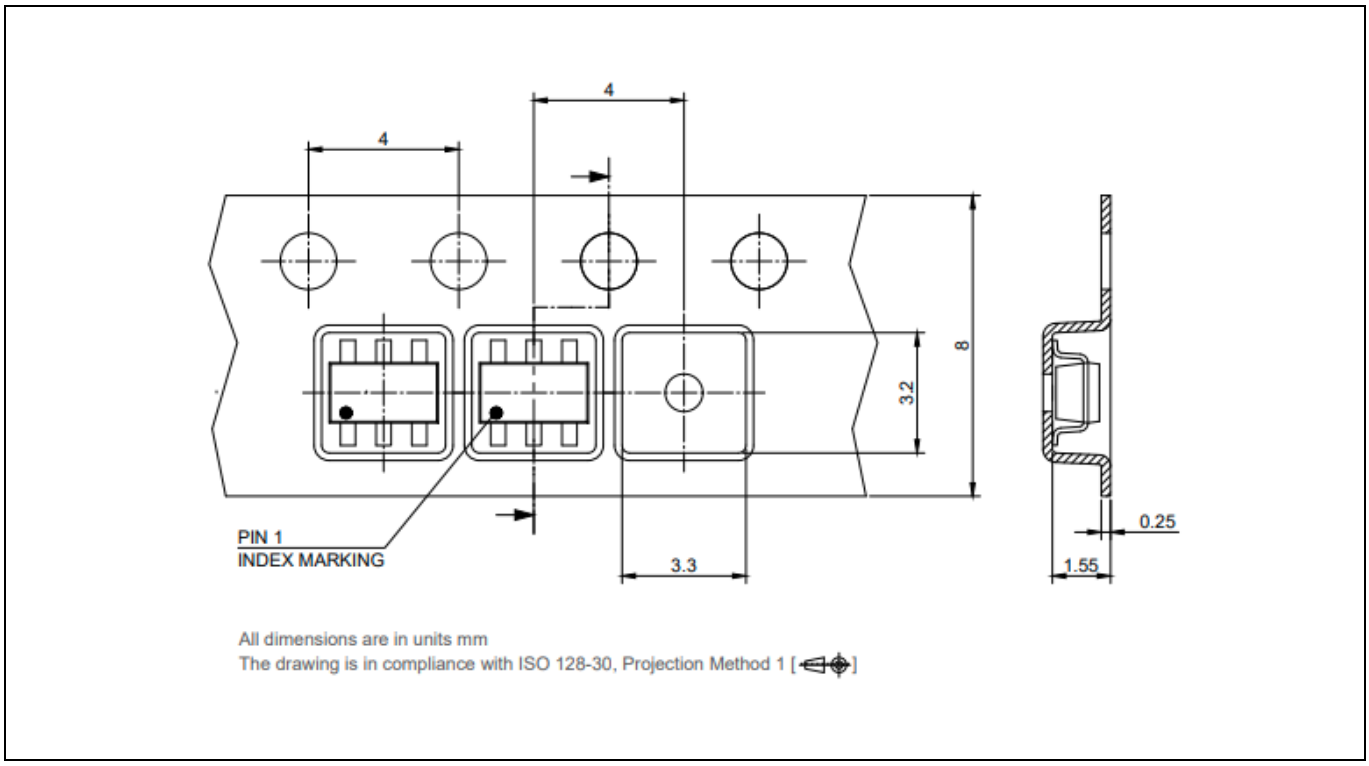

Figure 38 PG-SOT23-6 packaging

9.6 PG-TSNP-6

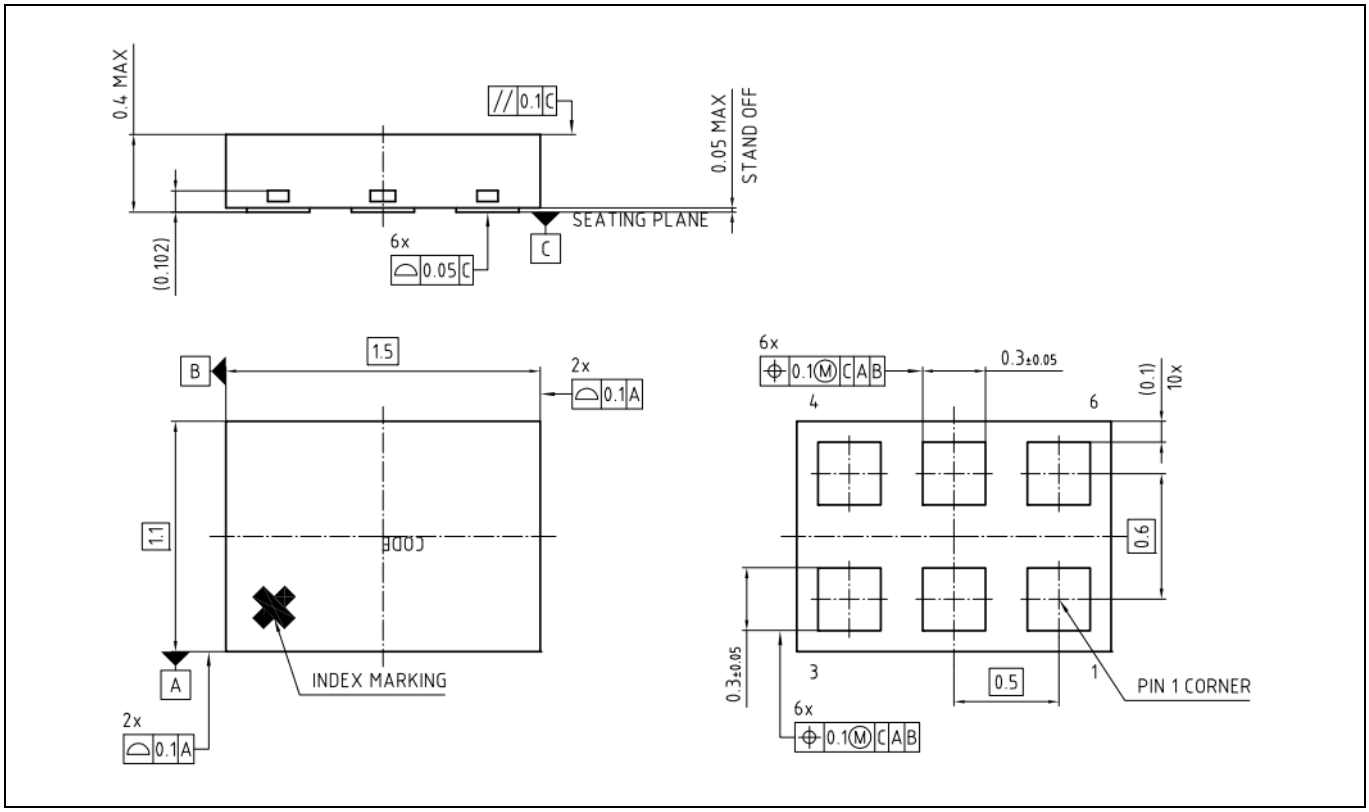

Figure 39 PG-TSNP-6 outline

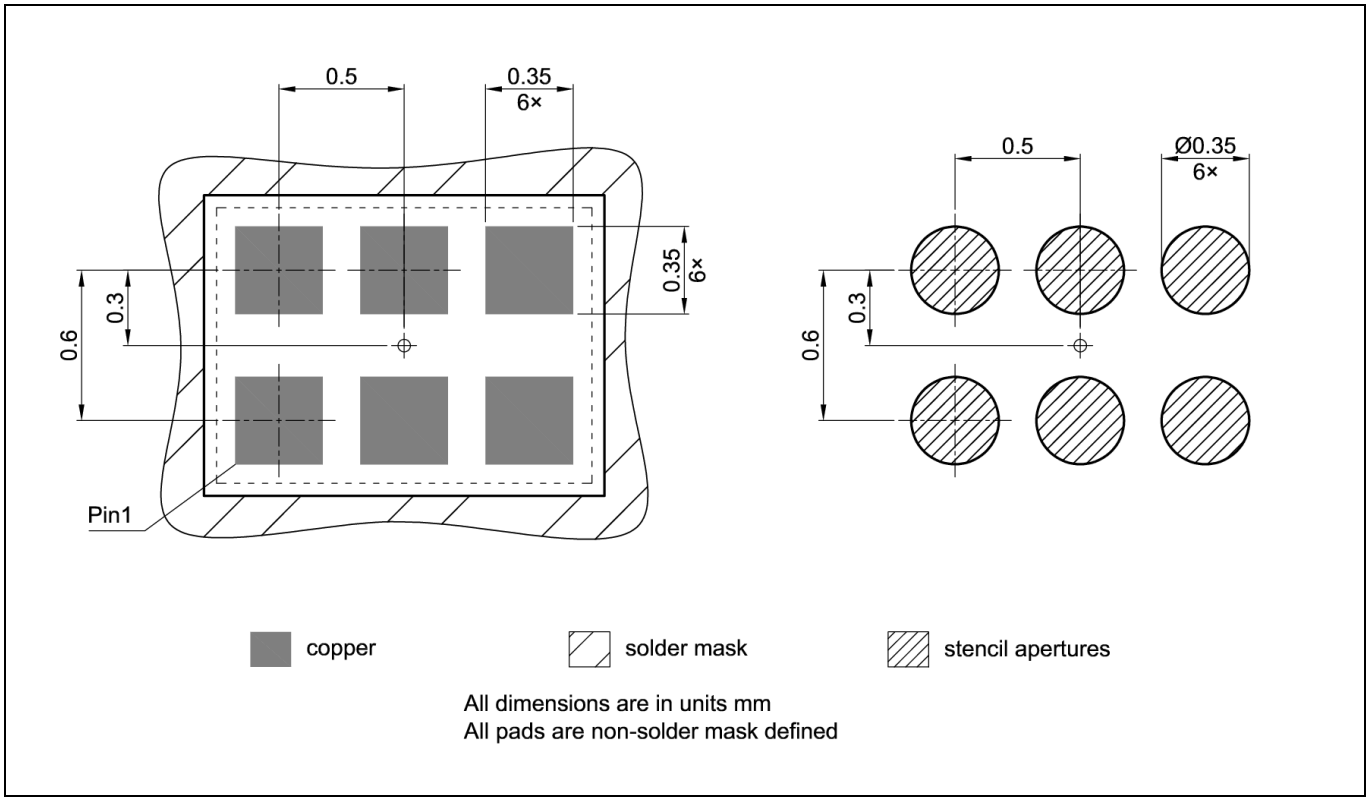

Figure 40 PG-TSNP-6 footprint

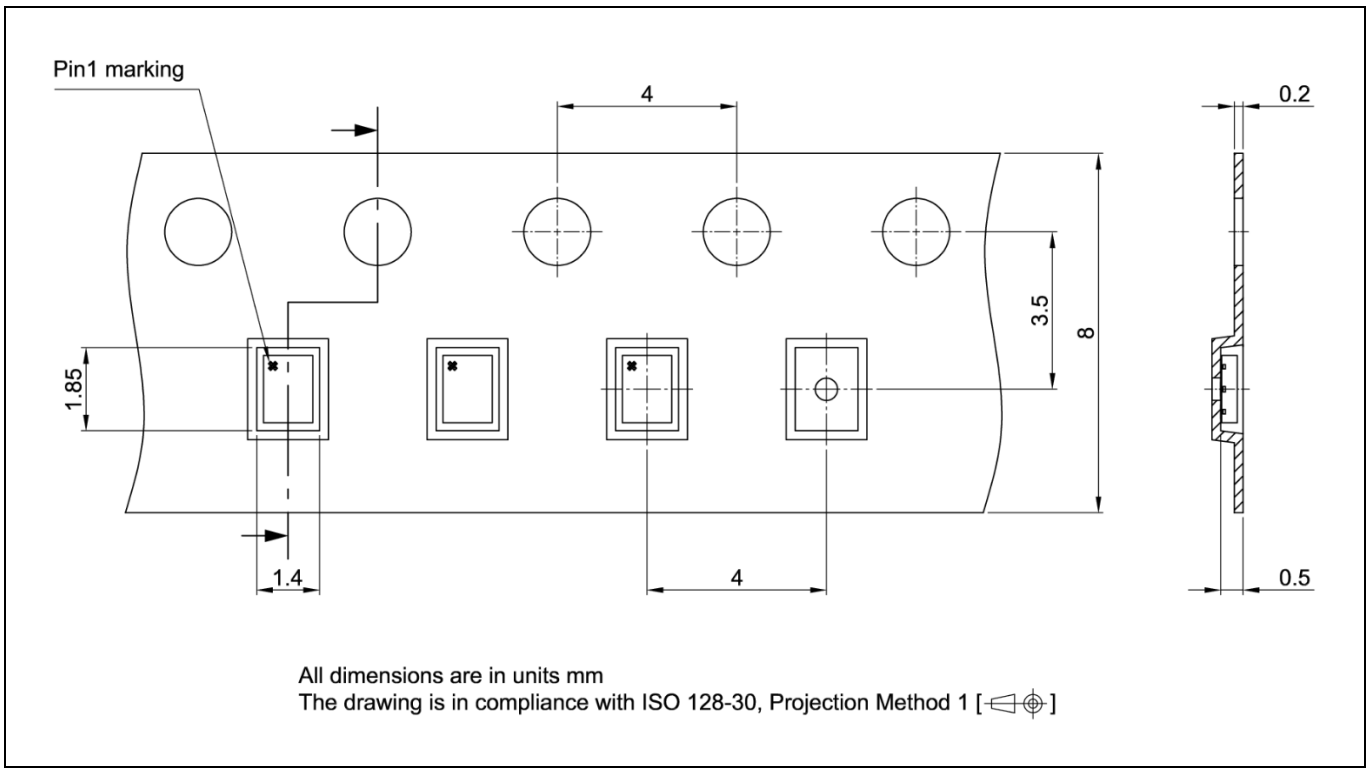

Figure 41 PG-TSNP-6 packaging

10 Revision history

Version	Date	Changes
Rev.1.3	2026-01-22	Update Figure 26, 39, 40, 41 Update Table 11 (TSNP-6 RthJB25 parameter)
Rev.1.2	2025-07-21	6-pin TPSON pinout update Figures 8, 9, 24 update TPSON thermal resistances update Device configuration figure update
Rev.1.1	2025-05-20	Template update and editorial changes Added 2EDN7534U Added Footnote 1 in Table 10 and Table 12 Updated Parameter "Minimum input pulse width that changes output state” in Table 19 Added Chapter 8.1, Chapter 8.2, Chapter 8.3
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