EZ-PD™ PMG1-B1: 2 to 5-cell Battery Charge Controller with USB-C PD MCU

General description

EZ-PD™ PMG1-B1 is a highly integrated Buck boost battery charge controller with USB Type-C Power Delivery (PD) microcontroller in a single chip designed to charge 2 to 5-cell Li-ion batteries via USB-C PD interface. It complies to the latest USB Type-C and PD specifications. EZ-PD™ PMG1-B1 has integrated gate drivers for VBUS NFET on the consumer path for sink application. It also includes hardware-controlled protection features on the VBUS.

EZ-PD™ PMG1-B1 has on-chip 32-bit Arm® Cortex®-M0 processor, 128-KB flash, 16-KB RAM and 32-KB ROM for user application programmability. It also includes analog and digital peripherals such as ADC, PWMs and timers.

Applications

- Cordless power tool charger
- Wireless speakers
- Portable electronics
- Cordless home appliance

Features

- **Buck-boost controller with battery charging support**
  - Switching frequency: 150 kHz to 600 kHz
  - Input: 4 V to 24 V, 40 V tolerant
  - Output: 3.3 to 21.5 V (ideal for 2 to 5-cell Li-Ion batteries)
  - ±3% charge current regulation
  - Maximum output current: 6.5 A (with 5 mΩ sense resistor)
  - Soft start
  - Constant voltage and constant current modes
  - Selectable pulse skipping mode (PSM) and forced continuous conduction mode (FCCM)
  - Programmable spread spectrum frequency modulation for low EMI
  - Hardware protections for OVP, UVP, OCP, and SCP
  - Configurable safety timers and thermal shutdown
  - Peak load efficiency of up to 96%
- **Type-C/USB-PD**
  - TID: 8934
  - One USB Type-C PD port with a baseband transceiver
  - Integrated USB power-delivery (USB PD) v3.2 complaint
  - Supports PPS and SPR AVS PDOs for Source & Sink
  - Slew rate control to limit the inrush current on the gate drivers configured to be used in VBUS provider or consumer path
  - Supports up to 20 V on VBUS path (tolerant to 24 V)
  - Configurable VBUS overvoltage protection (OVP), overcurrent protection (OCP), short-circuit protection (SCP) and reverse-current (RCP) protection
  - VBUS to CC short protection
  - Overtemperature protection through integrated ADC circuit and internal temperature sensor
  - VBUS high-side current sense amplifier capable of measuring current across 5 mΩ series resistance
  - Integrated 100 mW VCONN power supply and control
  - Configurable termination resistors R_P and R_D and $R_{D\text{-}DB}$ ($R_{D\text{-}DB}$ available only in CYPM1116)

  - One legacy/proprietary charging block with Apple charging 2.4 A and USB BC 1.2 support
- **32-bit MCU subsystem**
  - 48-MHz Arm® Cortex®-M0 CPU
  - 128-KB Flash
  - 16-KB SRAM
  - 32-KB ROM
- **Power supply**
  - VIN: 4 to 24 V
  - VBUS: 4 to 21.5 V
  - Integrated LDO for system power: 5 V, 75 mA
  - Integrated low-power standby regulator: 3 V, 10 mA
- **Peripherals and GPIOs**
  - Up to 21 GPIOs including two fail-safe GPIOs
  - Two 8-bit SAR ADC
  - One 12-bit SAR ADC
  - Eight 16-bit timer/counter pulse-width modulators (TCPWM)
  - Three run-time reconfigurable serial communication blocks (SCB) configurable as I2C, SPI, UART, or LIN
- **Package**
  - 48-pin QFN
  - Supports ambient temperature range (-40°C to +105°C) with 125°C operating junction temperature
- **Software tool**
  - ModusToolbox™

Block diagram

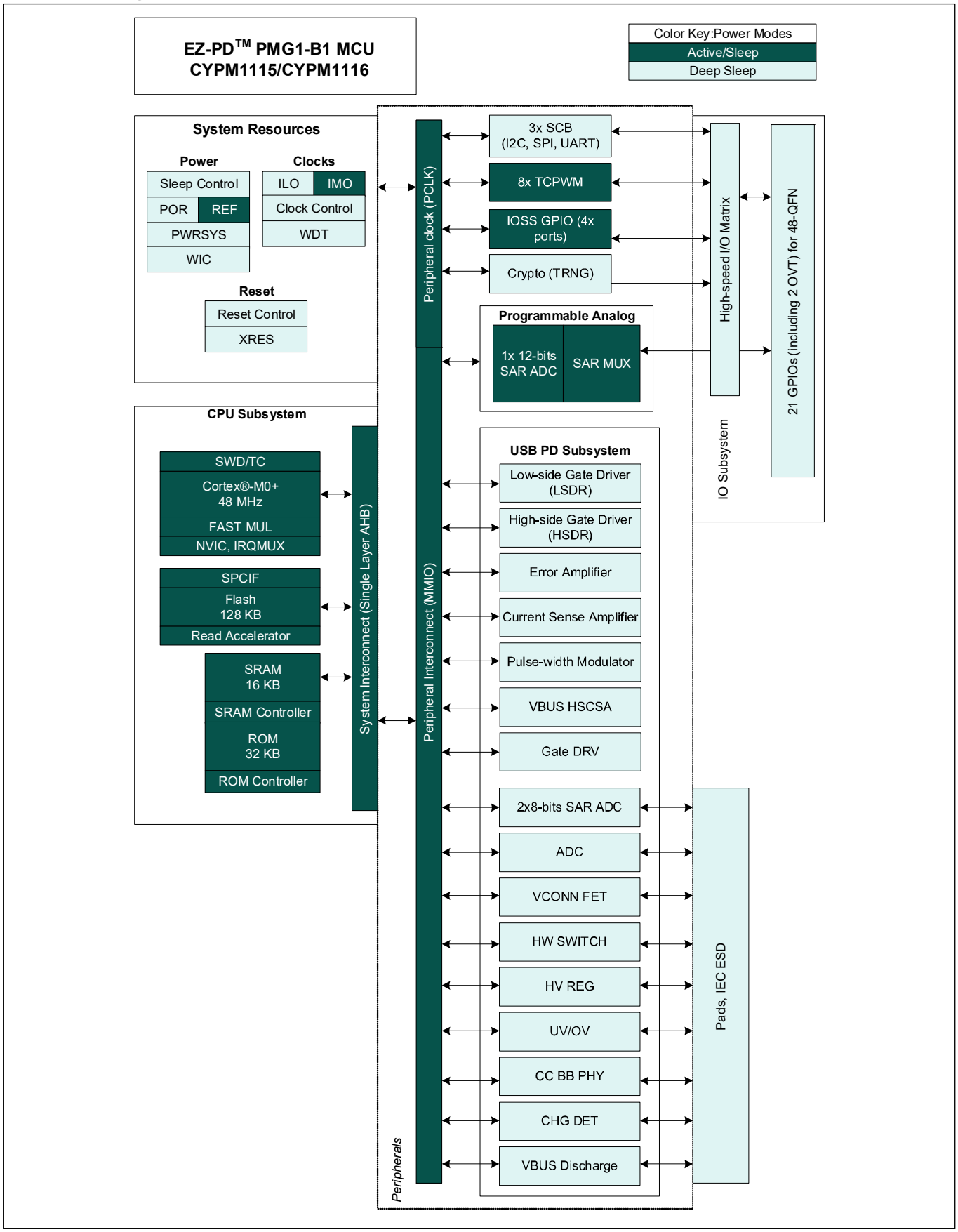

Table of contents

1 Development support

The EZ-PD™ PMG1 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit **USB-C High Voltage Microcontrollers**.

1.1 Documentation

A suite of documentation supports the EZ-PD™ PMG1 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

ModusToolbox™ documentation: A step-by-step guide for using ModusToolbox™. The software user guide shows you how ModusToolbox™ build process works in detail, how to use source control with ModusToolbox™, and much more.

Component datasheets: The flexibility of EZ-PD™ PMG1 allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all the information needed to select and use a particular component, including functional description, API documentation, example codes, and AC/DC specifications.

Application notes: This includes the Getting Started application note and the hardware design guidelines.

Technical reference manual: The technical reference manual (TRM) contains all the technical detail you need to use a EZ-PD™ PMG1 device, including a complete description of all EZ-PD™ PMG1 registers. The TRM is available in the Documentation section at **USB-C High Voltage Microcontrollers**.

1.2 Online

In addition to print documentation, the **Infineon community forums** helps connect you with fellow users and experts in PMG1 from around the world, 24 hours a day, 7 days a week.

1.3 Tools

With the industry standard cores, programming, and debugging interfaces, the EZ-PD™ PMG1 family is part of a development tool ecosystem.

Visit us at **ModusToolbox™ software** for the latest information on the revolutionary, easy to use ModusToolbox™ IDE, supported third party compilers, programmers, debuggers, and development kits.

1.4 ModusToolbox™ IDE and the EZ-PD™ PMG1 SDK

ModusToolbox™ is an Eclipse-based development environment on Windows, macOS, and Linux platforms that includes the ModusToolbox™ IDE and the EZ-PD™ PMG1 SDK. The ModusToolbox™ IDE brings together several device resources, middleware, and firmware to build an application. Using ModusToolbox™, you can enable and configure device resources and middleware libraries, write C/C++/assembly source code, and program and debug the device.

The PMG1 SDK is the software development kit for the EZ-PD™ PMG1 MCU. The SDK makes it easier to develop firmware for supported devices without the need to understand the intricacies of the device resources.

For additional details on using the ModusToolbox™, refer to the **Getting started with EZ-PD™ PMG1 MCU on ModusToolbox™ software** application note and the documentation and help integrated into ModusToolbox™.

2 Functional overview

2.1 MCU subsystem

2.1.1 CPU

The Cortex®-M0 in EZ-PD™ PMG1-B1 devices is a 32-bit MCU, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. It also includes a hardware multiplier, which provides a 32-bit result in one cycle. It includes an interrupt controller (the NVIC block) with 32 interrupt inputs and a wakeup interrupt controller (WIC), which can wake the processor up from Deep Sleep mode.

2.1.2 Flash, ROM and SRAM

EZ-PD™ PMG1-B1 devices have 128-KB flash and 32-KB ROM for non-volatile storage. ROM stores libraries for authentication and device drivers such as I^2C, SPI, and so on. Flash provides the flexibility to store code for any customer feature and allows firmware upgrades to meet the latest USB power delivery specifications and application needs.

The 16-KB RAM is used under software control to store the temporary status of system variables and parameters. A supervisory ROM that contains boot and configuration routines is provided.

2.2 System resources

2.2.1 Watchdog timer (WDT)

EZ-PD™ PMG1-B1 devices have a WDT running from the internal low-speed oscillator (ILO). This allows watchdog operation during Deep Sleep and generate a watchdog reset (WDR) if not serviced before the timeout occurs. The WDR is recorded in the Reset Cause register.

2.2.2 Reset

EZ-PD™ PMG1-B1 devices can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is preserved through reset and allows application firmware to determine the cause of the reset. XRES pin is the dedicated pin for asserting an external hardware reset.

2.2.3 Clock system

EZ-PD™ PMG1-B1 devices have a fully integrated clock with no external crystal required. EZ-PD™ PMG1-B1 device's clock system is responsible for providing clocks to all sub-systems that require clocks (SCB and PD) and for switching between different clock sources.

The HFCLK signal can be divided down as shown to generate synchronous clocks for the digital peripherals. The clock dividers have 8-bit, 16-bit and 16-bit fractional divide capability. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values. The clock dividers generate either enabled clocks (that is, 1 in N clocking where N = Divisor) or an approximately 50% duty cycle clock (exactly 50% for even divisors, one clock difference in the high and low values for odd divisors).

In **Figure 1**, PERXYZ_CLK represents the clocks for different peripherals.

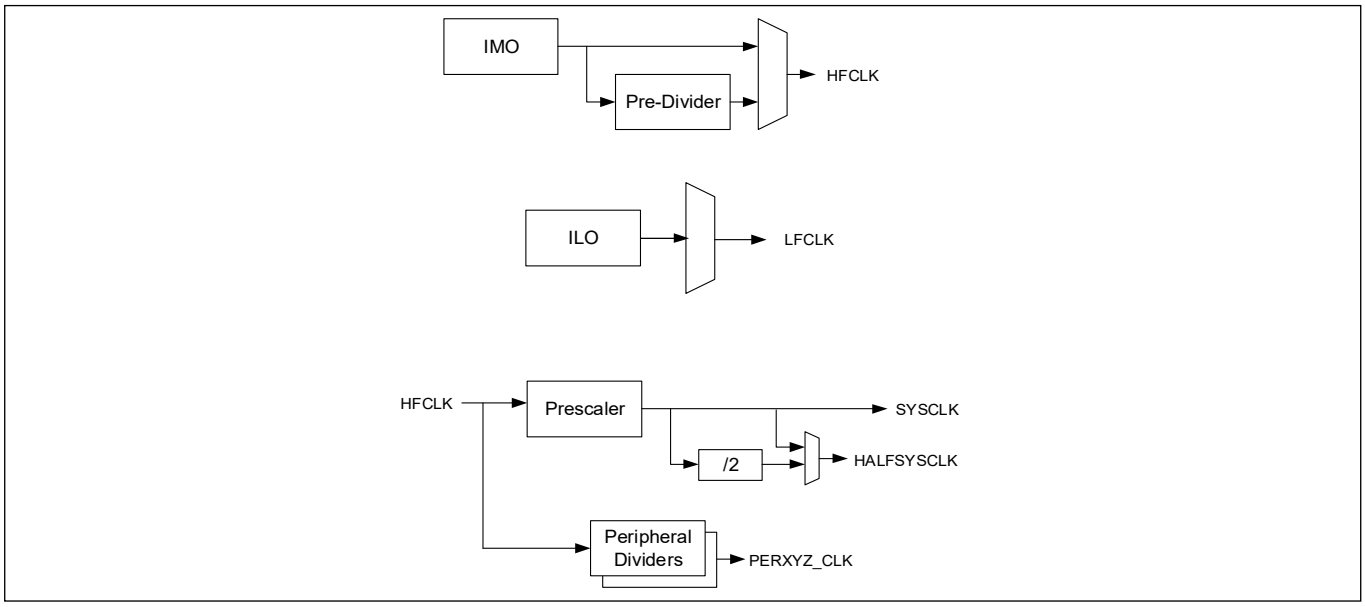

Figure 1 Clocking architecture of EZ-PD™ PMG1-B1 devices

Internal main oscillator (IMO) clock source

The IMO is the primary source of internal clocking in EZ-PD™ PMG1-B1 devices. IMO default frequency for EZ-PD™ PMG1-B1 devices is 48 MHz±2%.

Internal low-power oscillator (ILO) clock source

The ILO is a very low power, relatively inaccurate, oscillator, which is primarily used to generate clocks for peripheral operation in USB Suspend (Deep Sleep) mode. It is a 40 kHz oscillator with untrimmed accuracy of –50 to +100%.

2.3 USBPD subsystem

This subsystem provides the interface to the Type-C USB port.

2.3.1 USBPD physical layer

The USBPD physical layer consists of a transmitter and receiver block that communicate BMC encoded data over the CC channel per the USBPD 3.1 standard. All communication is half-duplex. The physical layer or PHY implements collision avoidance to minimize communication errors on the channel. The USBPD block includes all termination resistors (R_p and R_d) and their switches as required by the USB Type-C spec. R_p and R_d resistors are required to implement connection detection, plug orientation detection and for the establishment of the USB source/sink roles. EZ-PD™ PMG1-B1 devices support R_p under HW control in unconnected (standby) state to minimize standby power.

The PMG1-B1 device family along with the accompanying firmware is fully complaint with latest revision 3.x of the USB Power delivery specification. The device supports programmable power supply (PPS) operation at all valid voltages from 5 to 21 V.

2.3.2 VCONN Power

EZ-PD™ PMG1-B1 internal LDO voltage regulator is capable of powering a 100 mW VCONN supply for electronically marked cable assemblies (EMCA), VCONN-powered devices (VPD), and VCONN-powered accessories (VPA) as defined in the USB Type-C specification. PMG1-B1 also has VCONN FETs with OCP protection inbuilt. In the event the VCONN current exceeds the VCONN OCP limit, EZ-PD™ PMG1-B1 can be configured to shut down the Type-C port after a certain number of user configurable retries. The port can be re-enabled after a physical disconnect.

2.3.3 VBUS load switch controller

EZ-PD™ PMG1-B1 devices have an integrated high-side load switch controller to drive the gate of an external high-side NFET on the VBUS consumer path. The gate driver has an optional slow turn-on feature also which reduces the high-current spikes on the output. For a typical gate capacitance of 3 nF, a slow turn-on time of 2 to 10 ms is configurable using firmware. The load switch controller has following functions:

- **Overvoltage and undervoltage on protection on VBUS**
  The chip implements an undervoltage/overvoltage (UV/OV) detection circuit for the VBUS supply. The thresholds for both UV and OV are programmable.
- **Overcurrent and Short-circuit protection for VBUS**
  EZ-PD™ PMG1-B1 supports the detection of over-current and short-circuit faults via integrated high side current amplifiers on the VBUS provider path using external shunt resistor (5 mΩ or 10 mΩ).
- **VBUS discharge**
  EZ-PD™ PMG1-B1 has an integrated high voltage (21.5 V) VBUS discharge circuitry. After cable removal detection, the chip will discharge the residual charge and bring the floating VBUS back to vSafe0V within the time specified by USB PD spec.

2.3.4 Legacy charge detection and support

EZ-PD™ PMG1-B1 implements battery charger emulation and detection (source and sink) for USB BC.1.2, legacy Apple charging. The charger detection block connected to the DP/DM pins allows EZ-PD™ PMG1-B1 to detect conventional battery chargers.

2.3.5 VBUS to CC short protection

EZ-PD™ PMG1-B1 supports high voltage tolerant CC lines. In case of CC lines short to VBUS through connectors, these lines will be protected internally. In the event, an overvoltage is detected on the CC pin, it can be configured to shut down the Type-C port completely. The port will resume normal operation once the CC voltage detected is within normal range.

2.4 Analog blocks

2.4.1 8-bit SAR ADC

EZ-PD™ PMG1-B1 has two 8-bit SAR ADCs, these ADCs are available for general purpose A-D conversion applications in the chip. This ADC is used by USB PD block for VBUS measurements. The ADC can be accessed for external usage from all the GPIOs through the on-chip analog mux.

2.4.2 12-bit SAR ADC

EZ-PD™ PMG1-B1 has one 12-bit SAR ADC coupled with a SAR MUX. The 12-bit 1 MS/second SAR ADC operates at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion. The ADC clock input is derived by dividing the CPU clock rate by an integer value. This means that at 48 MHz CPU clock rate, the highest allowable clock rate for the ADC is 16 MHz. The 16 MHz clock rate allows 10-bit conversions to be performed at 1 MS/second (a 10-bit conversion takes a minimum of 16 clocks). Using integer dividers also means that 12-bit ADC performance is 890 samples/s at 48 MHz and its peak of 1 MS/s is at 18 or 36 MHz. The ADC requires an approximately 50% duty cycle clock and this is provided for all integer divider values.

The ADC is connected to fixed set of pins (Port1) through an 8-input sequencer (SARMUX). The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (i.e., aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The ADC input can also be fed through any GPIO through on-chip analog mux.

2.4.3 Temperature sensor

EZ-PD™ PMG1-B1 has an on-chip temperature sensor which consists of a diode biased by a current source. The diode is calibrated during production to achieve ±5% maximum deviation from accuracy (typical ±1%). Since the measured temperature is the on-chip temperature of the diode, the diode is placed in close proximity to the 12-bit SAR ADC to allow more accurate measurement.

2.4.4 Analog multiplexed buses

EZ-PD™ PMG1-B1 has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (8-bit and 12-bit SAR ADCs) to connect to any pin on the I/O Ports.

2.5 Fixed-function digital

2.5.1 Serial communication block (SCB)

EZ-PD™ PMG1-B1 devices have three SCB blocks that can be configured for I^2C, SPI, UART or LIN.

I^2C mode: SCB block implement full multi-master and slave I^2C interfaces capable of multi-master arbitration. This I^2C implementation is compliant with the standard Philips I^2C specification v3.0. These blocks operate at speeds of up to 1 Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU. The SCB blocks support 8-byte deep FIFOs for receive and transmit, which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The I^2C port I/Os for SCB0 are fail-safe.

UART mode: This is a full-feature UART operating at up to 1 Mbps. In addition, it supports the 9-bit multi-processor mode which allows address of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported.
SPI mode: The SPI mode supports full Motorola SPI as well as TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI) variants. The SPI block can also utilize the FIFO.

2.5.2 Timer, counter, pulse-width modulator (TCPWM)

The timer/counter/PWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. Each TCPWM counter has start, stop, count, reload and capture inputs. In PWM mode, the kill input can be used to force outputs to a pre-determined state; this is used in motor drive systems for instance when an over-current state is indicated and the PWMs driving the FETs need to be shut-off immediately with no time for software intervention.
The TCPWM block of EZ-PD™ PMG1-B1 devices support eight timers or counters or pulse-width modulators. These timers are available for internal timer use by firmware or for providing PWM-based functions on the GPIOs.

2.5.3 I/O subsystem

The EZ-PD™ PMG1-B1 devices have 21 GPIOs including the I^2C and SWD pins which can also be used as GPIOs. The GPIO block implements the following:

- Eight output drive modes
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Disabled
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control
- Fail-safe on one pair of GPIOs

During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals such as USB Type-C port are also fixed in order to reduce internal multiplexing complexity. Data output registers and pin state register store, respectively, the values to be driven on the pins and the states of the pins themselves.
The configuration of the pins can be done by the programming of registers through software for each digital I/O port. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

The I/O ports can retain their state during Deep Sleep mode or remain ON. If the operation is restored using reset, then the pins shall go the high-Z state. If operation is restored by an interrupt event, then the pin drivers shall retain their state until firmware chooses to change it. The IOs (on data bus) do not draw current on power down.

Fail-safe GPIOs

EZ-PD™ PMG1-B1 has two pins which are fail-safe GPIOs. These are P3.0 and P3.1, which are the I2C pins for SCB0. The fail-safe feature ensures that, in the absence of VBUS/VSYS power, a logic high level on these pins due to I2C line activity will not back-power the MCU.

2.6 Buck-boost battery charger subsystem

The buck-boost subsystem in EZ-PD™ PMG1-B1 devices can be configured to operate in buck-boost mode, buck-only mode or boost-only mode. While buck-boost mode requires four external switching FETs, buck-only and boost-only modes require only two FETs. **Figure 2** shows the buck-boost subsystem's main external components and connections.

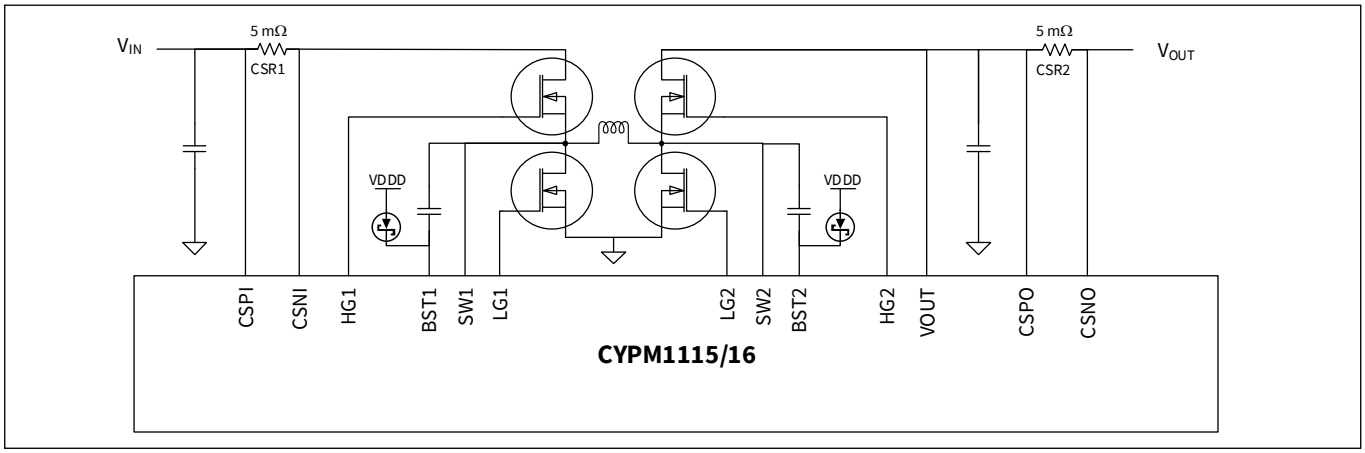

Figure 2 Buck-boost schematic showing external components

Buck-boost subsystem in EZ-PD™ PMG1-B1 devices have the following key functional blocks:

- High-side (cycle-by-cycle) CSA
- High-side and low-side gate driver
- Pulse-width modulator (PWM)
- Error amplifier (EA)

2.6.1 High-side (cycle-by-cycle) CSA

EZ-PD™ PMG1-B1 device's buck-boost controller implements peak current control in both boost and buck modes. A high-side CSA is used for peak current sensing through an external resistor (5 mΩ; see CSR1 in **Figure 2**) placed in series with the buck control FET. This CSA has a high bandwidth and a very wide common mode range. This CSR is connected to the CSA block through pins CSPI and CSNI as shown in **Figure 2**. This block implements slope compensation to avoid sub-harmonic oscillation for the internal current loop. In addition to peak current sensing, it provides a current limit comparator for shutting off the buck-boost converter if the current hits an upper threshold which is programmable.

2.6.2 High-side gate driver and low-side gate driver (HG/LG)

EZ-PD™ PMG1-B1' buck-boost controller provides four N-channel MOSFET gate drivers: two floating high-side gate drivers at the HG1 and HG2 pins, and two ground referenced low-side drivers at the LG1 and LG2 pin. The high-side gate drivers drive the high-side external FET with a nominal VGS of 5 V. The high-side gate driver has a programmable drive strength to drive external FET. An external capacitor and schottky diode form a bootstrap network to collect and store the high voltage source (VIN + ~5 V for HG1 and VOUT + ~5 V for HG2) needed to drive the high-side FET. The low-side gate driver drives the low-side external FET with a nominal VGS of 5 V using energy sourced from EZ-PD™ PMG1-B1' internal LDO regulator and stored in the capacitor between PVDD and PGND. Low-side gate driver has programmable drive strength to drive external FET. In addition to drive strength, the high-side gate driver and the low-side gate driver have programmable options for deadtime control and zero-crossing levels. High-side gate driver and low-side gate driver blocks include zero-crossing detector (ZCD) to implement discontinuous-conduction mode (DCM) mode with diode emulation.

The gate drivers for the switching FETs function at their nominal drive voltage levels (5 V) provided the VIN voltage is between 4.5 V and 24 V.

2.6.3 Error amplifier (EA)

EZ-PD™ PMG1-B1' buck-boost controller contains two EAs for output voltage and current regulation. The EA is a trans-conductance type amplifier with single compensation pin (COMP) to ground for both the voltage and current loops. In voltage regulation, the output voltage is compared with the internal reference voltage and the output of EA is fed to the PWM block. In current regulation, the average current is sensed by VOUT high-side CSA through the external resistor. The output of the VOUT CSA is compared with an internal reference in EA block and EA output is fed to the PWM block. EZ-PD™ PMG1-B1 firmware configures and controls the integrated programmable EA circuit for achieving the required VOUT voltage output from the power section.

2.6.4 Pulse-width modulator (PWM)

EZ-PD™ PMG1-B1 device family's PWM block generates the control signals for the gate drivers driving the external FETs in peak current mode control. There are many programmable options for minimum/maximum pulse width, minimum/maximum period, frequency and pulse skip levels to optimize the system design.

EZ-PD™ PMG1-B1 devices have two firmware-selectable operating modes to optimize efficiency and reduce losses under light load conditions: PSM and FCCM.

Pulse skipping mode (PSM)

In pulse skipping mode, the controller reduces the total number of switching pulses without reducing the active switching frequency by working in "bursts" of normal nominal-frequency switching interspersed with intervals without switching. The output voltage thus increases during a switching burst and decreases during a quiet interval. This mode results in minimal losses at the cost of higher output voltage ripple. When in this mode, EZ-PD™ PMG1-B1 devices monitor the voltage across the buck or boost sync FET to detect when the inductor current reaches zero; when this occurs, the EZ-PD™ PMG1-B1 devices switch off the buck or boost sync FET to prevent reverse current flow from the output capacitors (i.e. diode emulation mode). Several parameters of this mode are programmable through firmware, allowing the user to strike their own balance between light load efficiency and output ripple.

Forced continuous conduction mode (FCCM)

In FCCM mode, the nominal switching frequency is maintained at all times, with the inductor current going below zero (i.e. "backwards" or from the output to the input) for a portion of the switching cycle as necessary to maintain the output voltage and current. This keeps the output voltage ripple to a minimum at the cost of light-load efficiency.

2.6.5 Buck-boost controller operation regions

EZ-PD™ PMG1-B1's buck boost controller can operate in 3 modes- buck, boost, and buck-boost region depending on the input and output voltage ranges. The switching time/period of the four gate drivers (HG1, LG1, HG2, LG2) depends upon the region in which the block is operating as well as the mode such as DCM or FCCM. The exact VIN vs VOUT thresholds for transitions into and out of each region are adjustable in firmware including the hysteresis.

Buck region operation (VIN >> VOUT)

When the VIN voltage is significantly higher than the required VOUT voltage, EZ-PD™ PMG1-B1 devices operate in the buck region. In this region, the boost side FETs are inactivated, with the boost control FET (connected to LG2) turned off and the boost sync FET (connected to HG2) turned on. The buck side FETs are controlled as a buck converter with synchronous rectification as shown in **Figure 3**.

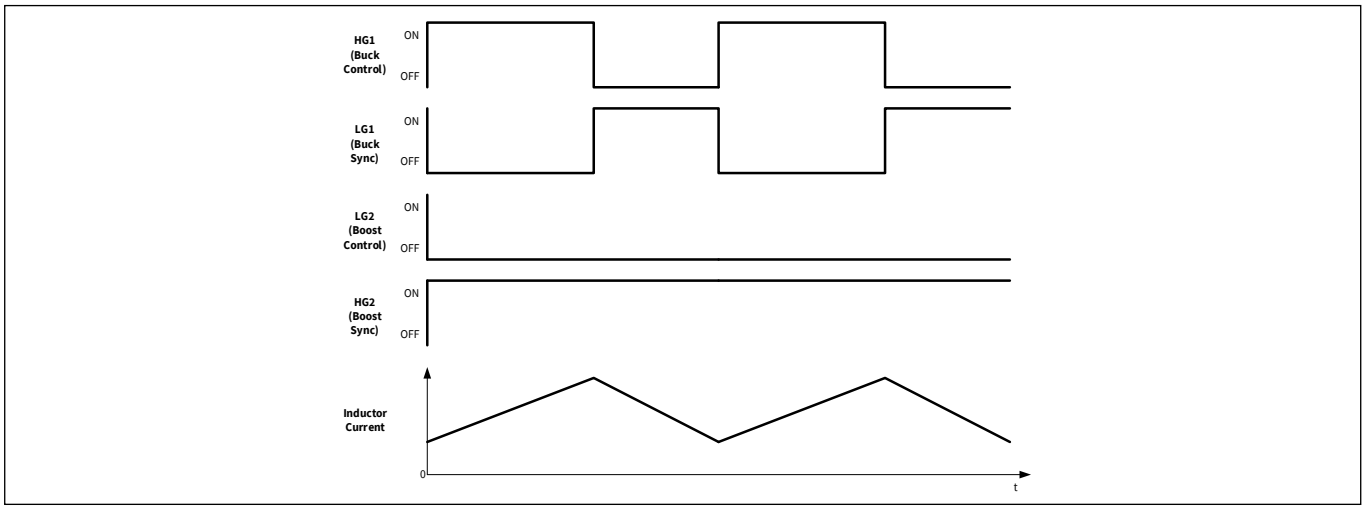

Figure 3 Buck operation waveforms

Boost region operation (VIN << VOUT)

When the VIN voltage is significantly lower than the required VOUT voltage, EZ-PD™ PMG1-B1 devices operate in the boost region. In this region, the buck side FETs are inactivated, with the sync FET turned off and the buck control FET turned on. The boost side FETs are controlled as a boost converter with synchronous rectification as shown in **Figure 4**.

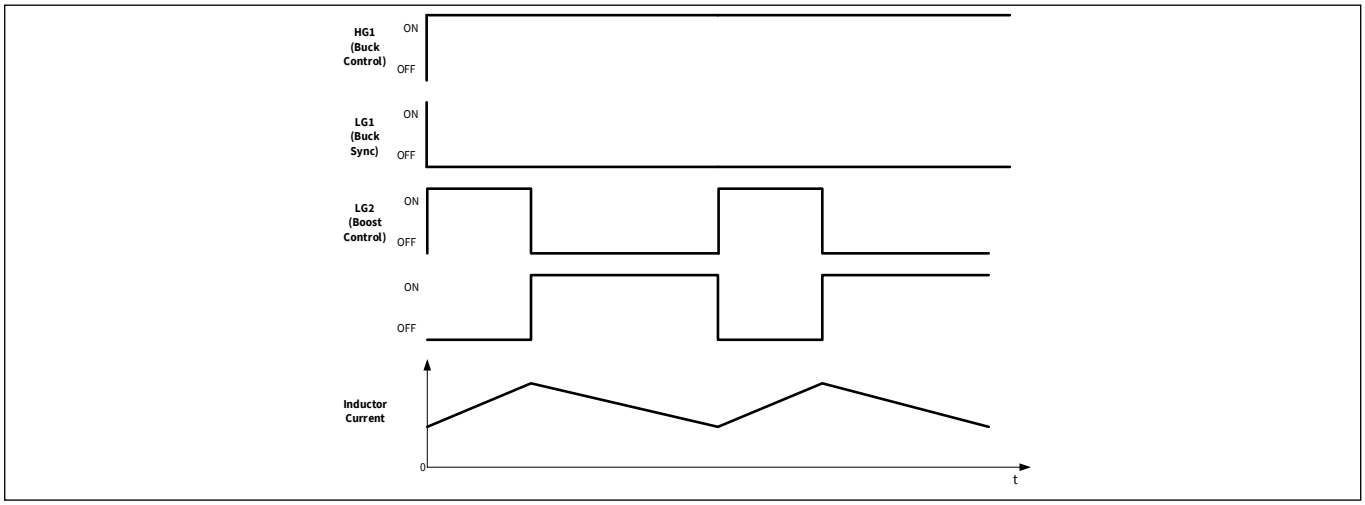

Figure 4 Boost operation waveforms

Buck-boost region 1 operation (VIN ~> VOUT)

When the VIN voltage is slightly higher than the required VOUT voltage, EZ-PD™ PMG1-B1 devices operate in the buck-boost region 1. In this region, the boost side works at a fixed 20% duty cycle (programmable) while the buck side (LG1 / HG1) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in **Figure 5**.

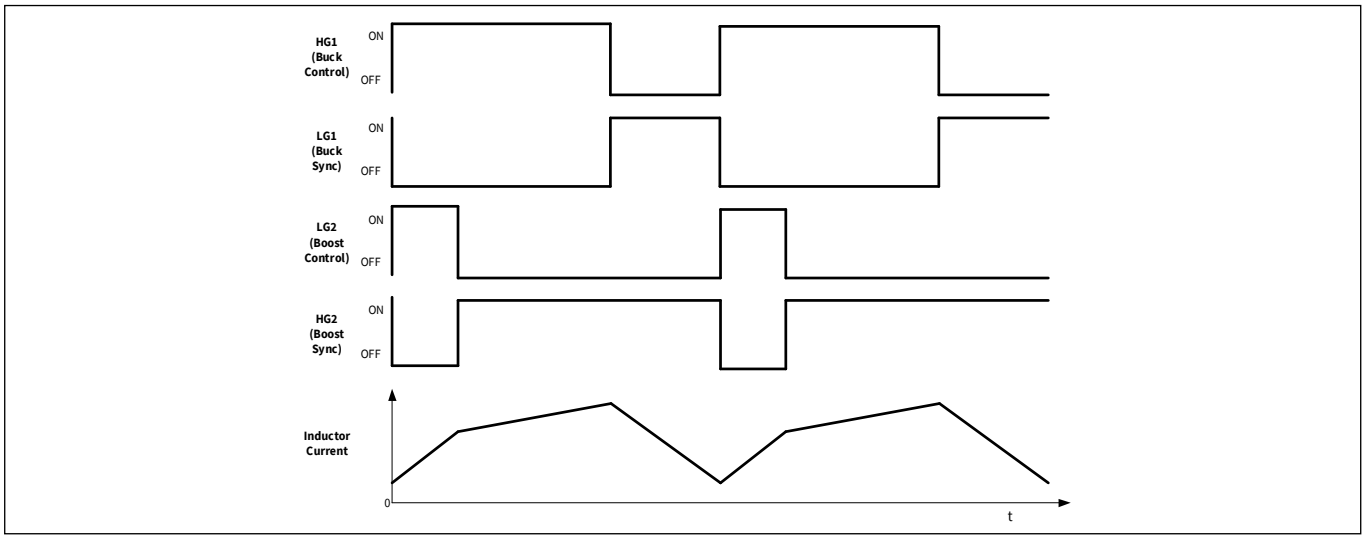

Figure 5 Buck-boost region 1 (VIN ~> VOUT) operation waveforms

Buck-boost region 2 operation (VIN ~< VOUT)

When the VIN voltage is slightly lower than the required VOUT voltage, EZ-PD™ PMG1-B1 devices operate in the buck-boost region 2. In this region, the buck side works at a fixed 80% duty cycle (programmable) while the boost side (LG2) duty cycle is modulated to control the output voltage. All four FETs are switching every cycle in this operating region as shown in **Figure 6**.

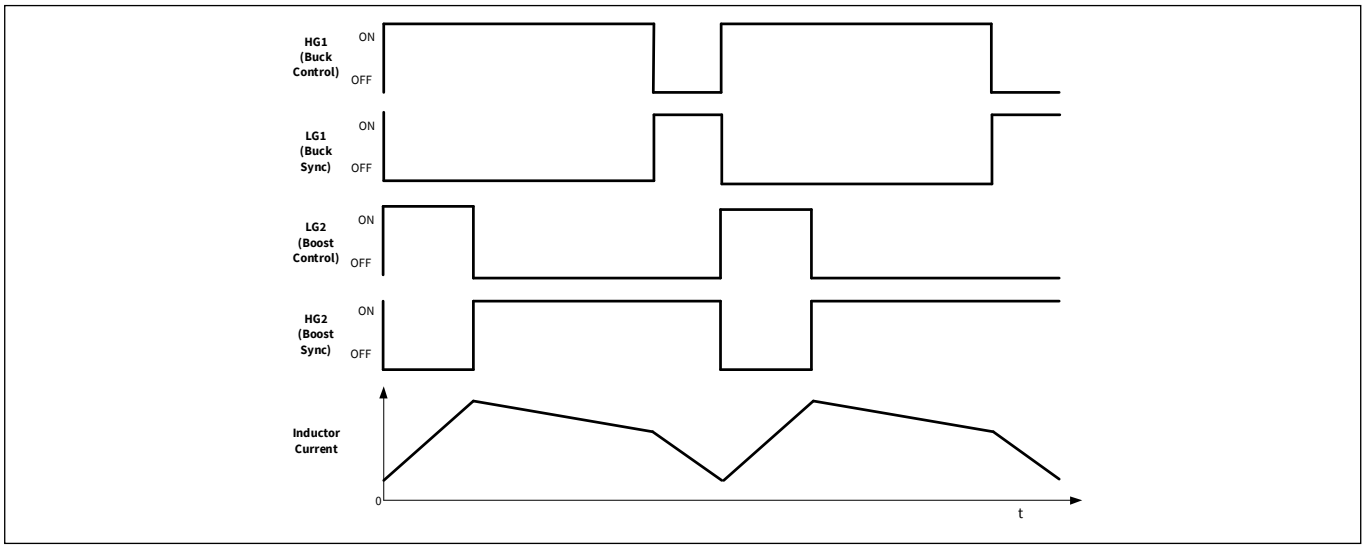

Figure 6 Buck-boost region 2 (VIN ~< VOUT) operation waveforms

2.6.6 Switching frequency and spread spectrum

EZ-PD™ PMG1-B1's buck-boost controller devices offer programmable switching frequency between 150 kHz and 600 kHz. The controller supports spread spectrum clocking within the operating frequency range in all operating modes. Spread spectrum is essential for charging applications to meet EMC/EMI requirements by spreading emissions caused by switching over a wide spectrum instead of a fixed frequency, thereby reducing the peak energy at any particular frequency. Both the switching frequency and the spread spectrum span are firmware programmable.

2.6.7 Protections

Overvoltage and undervoltage protections

EZ-PD™ PMG1-B1 MCU utilizes dedicated UVOV block to monitor the buck-boost output, VOUT, during the operation. This block provides hardware-based protection against overvoltage and undervoltage conditions and immediately cuts-off buck-boost output upon detection of battery overvoltage (OV). In a DRP design, EZ-PD™ PMG1-B1 MCU can also cut-off source mode and prevent the battery from over-discharging if a undervoltage (UV) is detected.

Overcurrent and short-circuit protections

At the output of buck-boost, VOUT, overcurrent and short-circuit faults are monitored using internal CSAs using an external shunt resistor. The OCP and SCP fault thresholds and response times are configurable via firmware. In the event of OCP or SCP, PMG1-B1 can be configured to shut down the buck-boost controller.

Battery charging safety timers

EZ-PD™ PMG1-B1 MCU has inbuilt safety timers, which runs on ILO clock, to prevent an extended charging cycle in case of abnormal battery conditions. Two firmware configurable timers, Pre-charge and Normal charge timers, monitor the charge time independently and cut-off the charging if limits are crossed detecting an abnormal battery pack.

2.6.8 Battery charging

The buck-boost controller can be used for 2 to 5-cell battery charging in constant current, constant voltage, pre-charge, and trickle charge mode. **Figure 7** shows a typical battery charging application using EZ-PD™ PMG1-B1. The smart battery charging algorithm provided with PMG1-B1 devices can be used to configure the charging mode, voltage and current via the firmware.

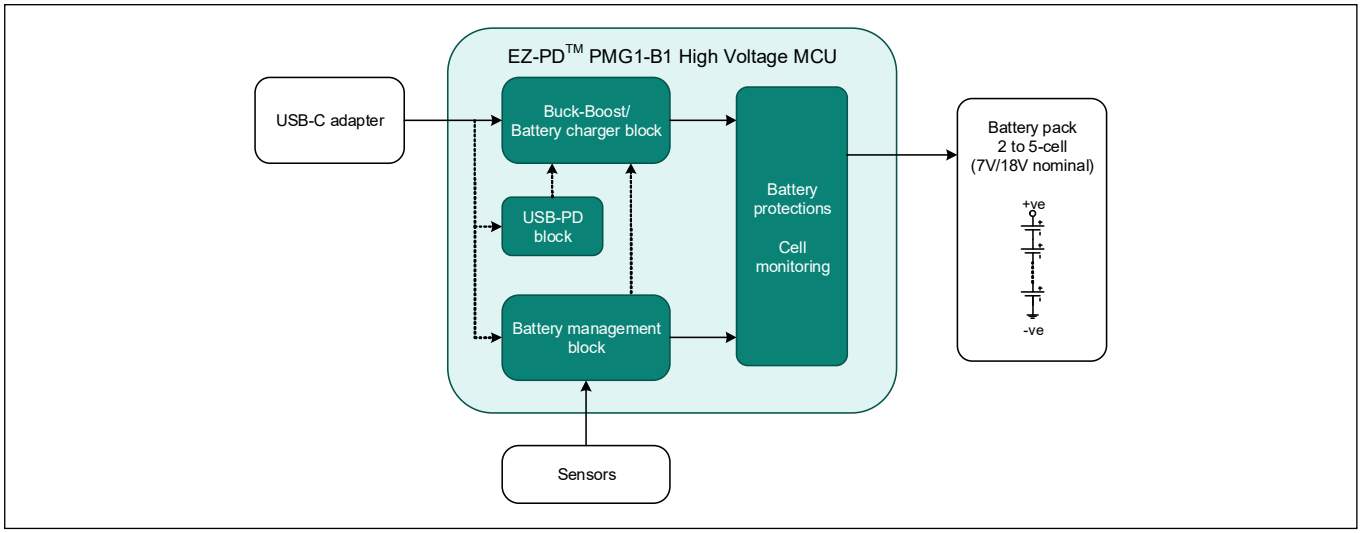

Figure 7 EZ-PD™ PMG1-B1 based USB-C battery charger system

Multi-stage constant current mode charging

In constant current (CC) mode, a fixed current is used to charge the battery continuously. Implementing a multi-stage constant current battery charging algorithm provides better utilization of the battery capacity. After the battery voltage reaches the specified cut-off voltage, the charging current can be reduced to 40%, 20%, and 6% (these % current steps can be customized) of the rated current respectively when the terminal voltage reaches the specified cut-off voltage.

Figure 8 shows an EZ-PD™ PMG1-B1 MCU-based multi-stage battery charging profile of a 5-cell Li-ion battery with support for the smart charging algorithm.

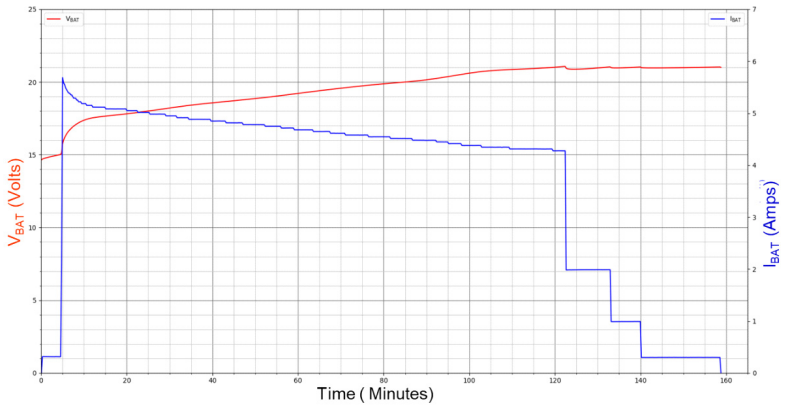

Figure 8 Multistage constant current battery charging profile for a 5-cell 10 Ah Li-ion battery

Mixed constant current and constant voltage mode charging

In this method, the charging starts with constant current (CC) mode and when the battery terminal voltage reaches the maximum safe threshold value, the charging mode transfers to the constant voltage (CV) charging method. The charging process is complete when the charging current goes below the cut-off threshold.

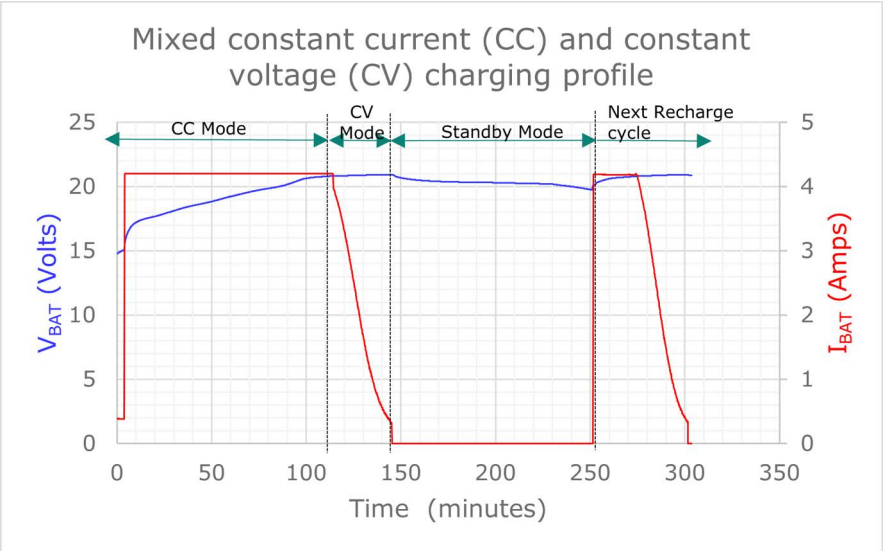

Figure 9 Constant current (CC) and constant voltage (CV) modes charging profile for a 5-cell 10 Ah Li-ion battery

The default EZ-PD™ PMG1-B1 MCU firmware supports the mixed constant current and constant voltage mode charging. The firmware can be modified to support the multi-stage constant current mode or other algorithms preferred by the manufacturer of the battery charging device.

2.6.9 Buck-boost efficiency

The buck-boost controller efficiency is measured on the EVAL_PMG1_B1_DRP board, which has below component on the power path:

- MOSFETs: Infineon BSZ063N04LS6 (6.3 mΩ, 40 V)
- Inductor: KEMET MPX1D1040L6R8 (6.8 µH, 24.1 mΩ)
- Output capacitor: 220 µF 35 V Electrolyte & 2x 10 µF 25 V Ceramic

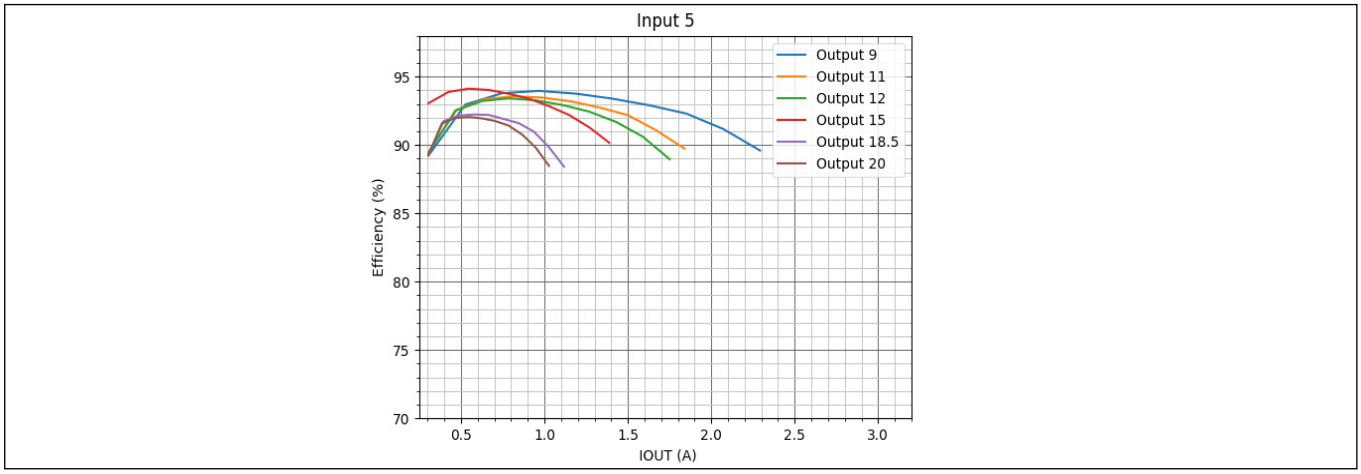

Figure 10 Efficiency at 5 VDC (VBUS) input

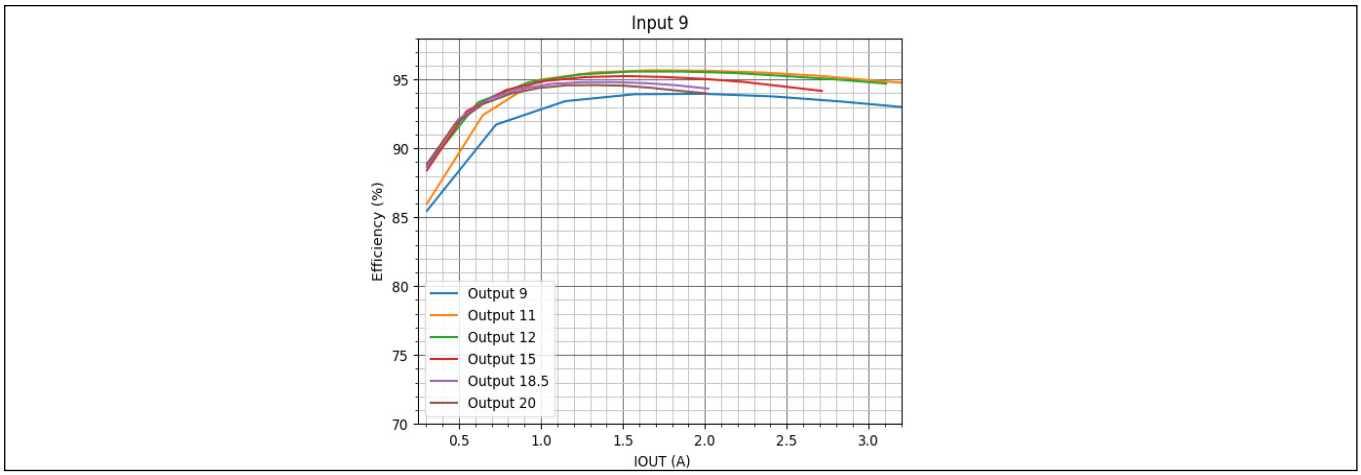

Figure 11 Efficiency at 9 VDC (VBUS) input

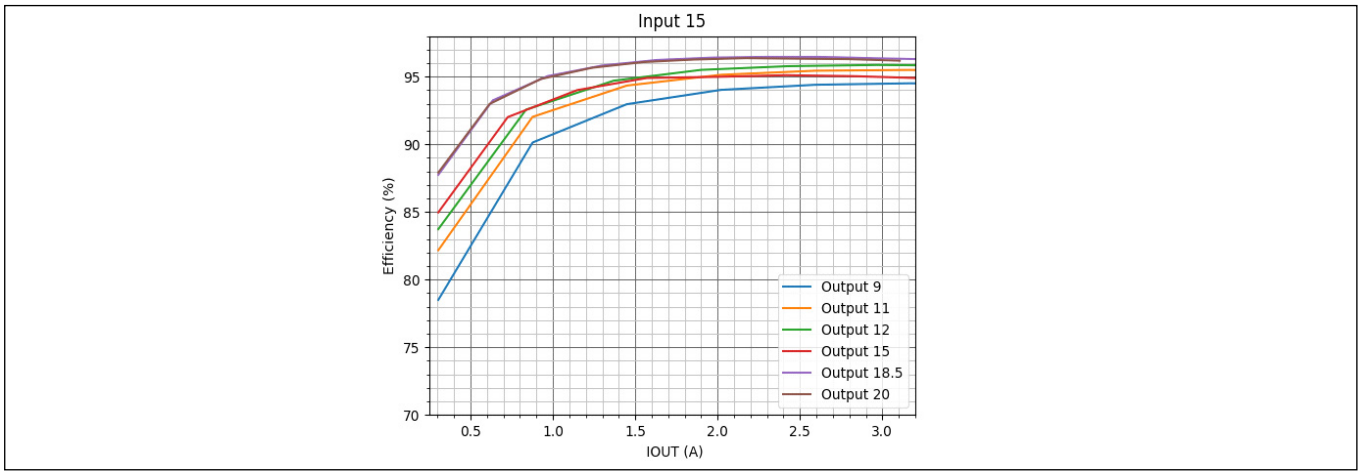

Figure 12 Efficiency at 15 VDC $_{(VBUS)}$ input

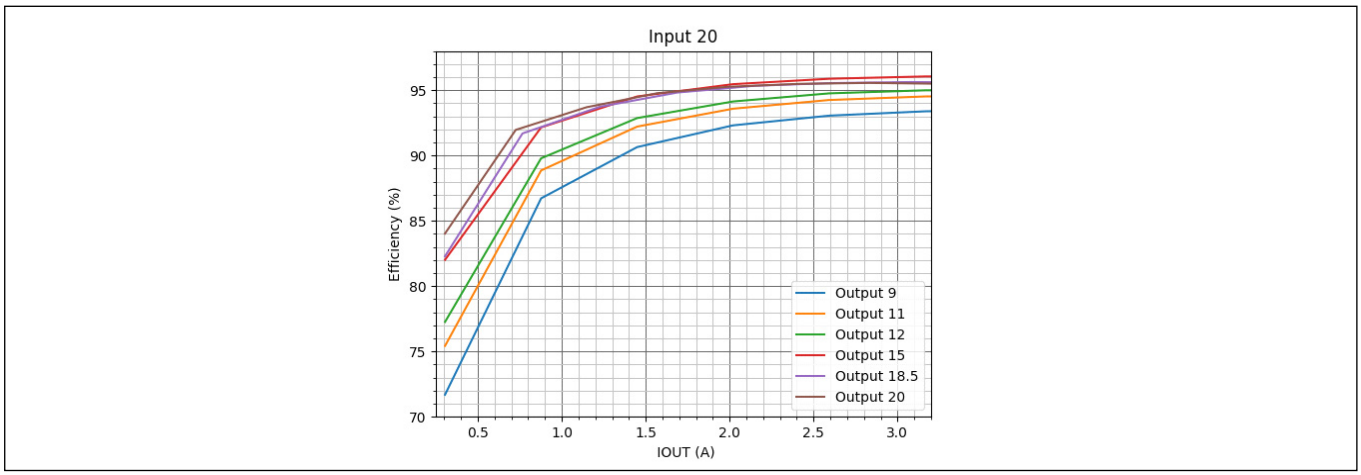

Figure 13 Efficiency at 20 VDC $_{(VBUS)}$ input

3 Power systems overview

Figure 14 shows an overview of the power subsystem architecture for EZ-PD™ PMG1-B1 devices. The power subsystem of EZ-PD™ PMG1-B1 devices operate from VIN supply which can vary from 4 V to 24 V. The V_{DDD} pin, the output of an internal 5 V LDO, gets input from VIN supply. The chip can be also powered from CSN0 pin (used in case of battery powered applications) via the standby regulator provides 3 V to VDDD. The current capability of the VDDD pin is up to 75 mA including internal as well as external loads (applicable only if supply is from VIN).

EZ-PD™ PMG1-B1 devices have two different power modes: Active and Deep Sleep, transitions between which are managed by the power system. The VCCD pin, the output of the core (1.8 V) regulator, is brought out for connecting a 0.1 µF capacitor for the regulator stability only. This pin is not supported as a power supply for external load.

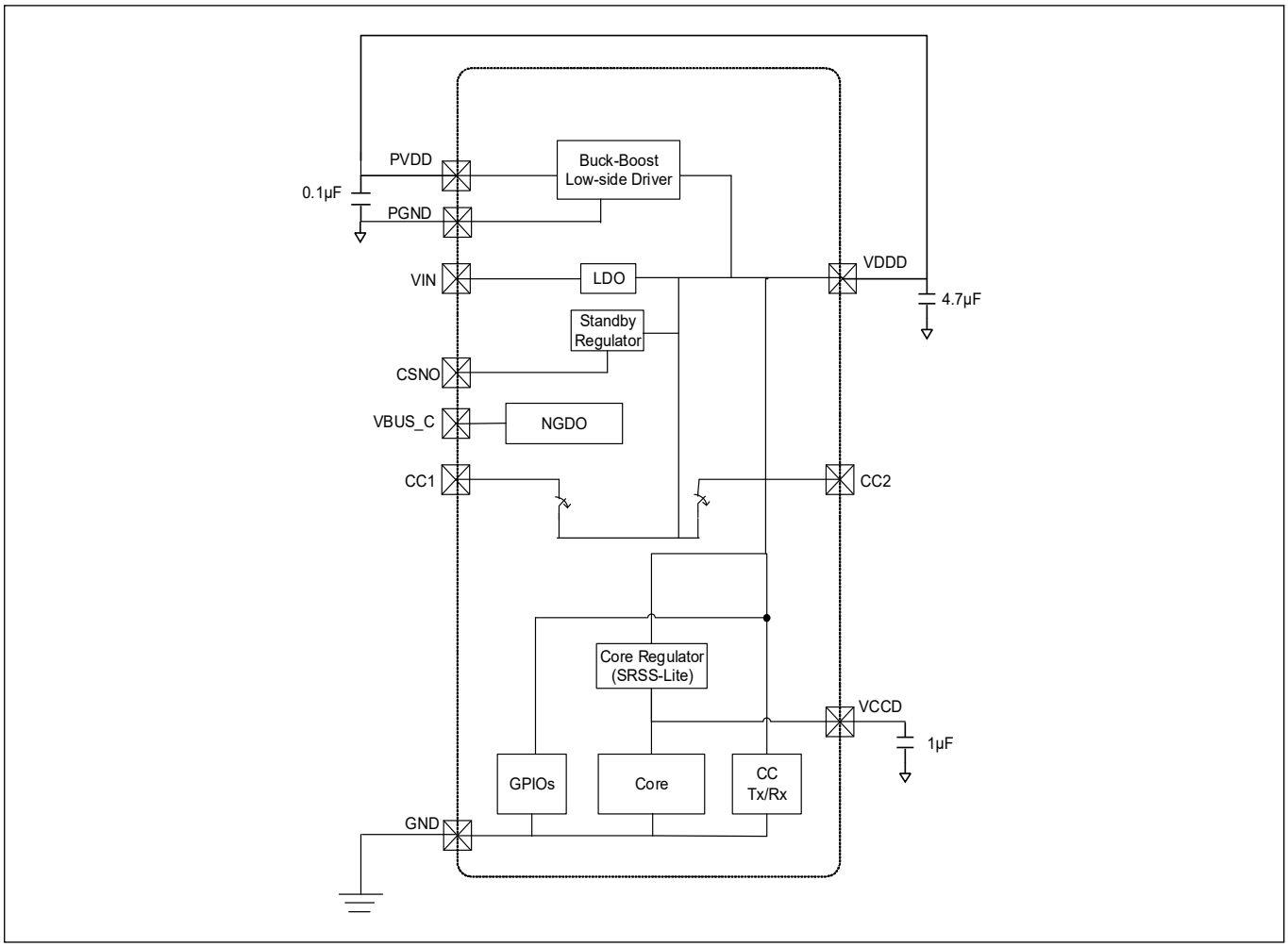

Figure 14 Power system requirement block diagram[1]

Note

1. It is recommended to tie PGND and GND together in the layout for better EMI performance.

3.1 VIN under-voltage lockout (UVLO)

EZ-PD™ PMG1-B1 supports UVLO to allow the device to shut down when the input voltage is below the reliable level. It guarantees predictable behavior when the device is up and running.

3.2 Using external VDDD supply

By default, external VDDD is not supported for EZ-PD™ PMG1-B1 devices. However, usage of external VDDD supply can be enabled using firmware. The prerequisite for enabling external forcing of VDDD is to always maintain VIN higher than VDDD.

3.3 Power modes

The power modes of the device accessible and observable by the user are listed in **Table 1**.

Table 1 Power modes

Mode	Description
RESET	Power is valid and XRES is not asserted. An internal reset source is asserted or Sleep controller is sequencing the system out of reset
ACTIVE	Power is valid and CPU is executing instructions.
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most hard-IP are shut off. Deep Sleep regulator powers logic, but only low-frequency clock is available.
XRES	Power is valid and XRES is asserted. Core is powered down.

4 Pinouts

Table 2 Pin list for PMG1-B1 CYPM1115-48LQXI and CYPM1116-48LQXI

Group	Pin No	Alternate functions (HSIOM_PORT_SEL)										Description
		Pin name	Analog	ACT#0	ACT#1	ACT#2	ACT#3	DS#0	DS#1	DS#2	DS#3	
Buck-Boost controller	1	BST1	–	–	–	–	–	–	–	–	–	Bootstrap capacitor node (buck)
	2	HG1	–	–	–	–	–	–	–	–	–	Buck high-side gate driver output
	3	SW1	–	–	–	–	–	–	–	–	–	Buck high-side gate driver negative power rail
	4	LG1	–	–	–	–	–	–	–	–	–	Buck low-side gate driver output
	5	PGND	–	–	–	–	–	–	–	–	–	Low-side gate driver ground, short to GND
	6	PVDD	–	–	–	–	–	–	–	–	–	Low-side gate driver supply, short to VDDD
	7	LG2	–	–	–	–	–	–	–	–	–	Boost low-side gate driver output
	8	VOUT	–	–	–	–	–	–	–	–	–	Buck-boost converter output
	9	SW2	–	–	–	–	–	–	–	–	–	Boost high-side gate driver negative power rail
	10	HG2	–	–	–	–	–	–	–	–	–	Boost high-side gate driver output
	11	BST2	–	–	–	–	–	–	–	–	–	Bootstrap capacitor node (boost)
	13	COMP	–	–	–	–	–	–	–	–	–	Error Amplifier(EA) output pin for compensation network
	15	VOUT_EA	–	–	–	–	–	–	–	–	–	Output voltage feedback for EA
	16	CSNO	–	–	–	–	–	–	–	–	–	Output CSA negative input
	17	CSPO	–	–	–	–	–	–	–	–	–	Output CSA positive input
	47	CSPI	–	–	–	–	–	–	–	–	–	Input CSA positive input
	48	CSNI	–	–	–	–	–	–	–	–	–	Input CSA negative input
USB PD Type-C	12	VBUS_CTRL	–	–	–	–	–	–	–	–	–	VBUS NFET gate driver output
	14	VBUS_C	–	–	–	–	–	–	–	–	–	USB PD VBUS
	18	CC2	–	–	–	–	–	–	–	–	–	USB PD configuration channel 2
	19	CC1	–	–	–	–	–	–	–	–	–	USB PD configuration channel 1

Table 2 Pin list for PMG1-B1 CYPM1115-48LQXI and CYPM1116-48LQXI

Group	Pin No	Alternate functions (HSIOM_PORT_SEL)										Description
		Pin name	Analog	ACT#0	ACT#1	ACT#2	ACT#3	DS#0	DS#1	DS#2	DS#3	
GPIO	20	P0.0/DM	–	–	–	–	–	–	–	scb2_spi_miso	–	GPIO, Legacy charging charge detect positive, SCB
	21	P0.1/DM	–	–	–	–	–	–	–	scb2_spi_clk	–	GPIO, Legacy charging charge detect negative, SCB
	23	P0.2/CSP	–	tcpwm0_line	tcpwm0_comp_match	–	tcpwm0_tr_overflow	tcpwmx_tr_in0	–	scb2_spi_mosi	–	GPIO, VBUS CSA positive input, TCPWM, SCB
	24	P0.3/CSN	–	tcpwm1_line	tcpwm1_comp_match	–	tcpwm1_tr_overflow	tcpwmx_tr_in1	–	scb2_spi_select	–	GPIO, VBUS CSA negative input, TCPWM, SCB
	25	P0.5	–	tcpwm2_line	tcpwm2_comp_match	–	tcpwm2_tr_overflow	tcpwmx_tr_in2	–	–	usbpd_fault0	GPIO, TCPWM, USB PD fault output
	26	P0.6	–	tcpwm0_line	tcpwm0_comp_match	–	–	tcpwmx_tr_in3	–	–	–	GPIO, TCPWM
	27	P0.7	–	tcpwm1_line	tcpwm1_comp_match	–	–	tcpwmx_tr_in4	–	–	–	GPIO, TCPWM
	28	P2.0	–	tcpwm2_line	tcpwm2_comp_match	–	–	tcpwmx_tr_in5	–	–	–	GPIO, TCPWM
	29	P2.1	–	tcpwm6_line	tcpwm6_comp_match	scb2_uart_cts	–	–	–	–	–	GPIO, TCPWM, SCB
	30	P1.7	sarmux_7	tcpwm5_line	tcpwm5_comp_match	scb2_uart_rts	–	–	–	–	–	GPIO, TCPWM, SCB, SAR MUX input
	31	P1.6	sarmux_6	tcpwm4_line	tcpwm4_comp_match	scb2_uart_rx	–	–	–	–	–	GPIO, TCPWM, SCB, SAR MUX input
	32	P1.5	sarmux_5	tcpwm3_line	tcpwm3_comp_match	scb2_uart_tx	–	–	–	–	–	GPIO, TCPWM, SCB, SAR MUX input
	33	P1.4	sarmux_4	tcpwm7_line	tcpwm7_comp_match	scb1_uart_rts	tcpwm7_tr_overflow	tcpwmx_tr_in7	–	scb1_spi_select	usbpd_fault1	GPIO, TCPWM, SCB, SAR MUX input, USB PD fault output
	34	P1.3	sarmux_3	tcpwm6_line	tcpwm6_comp_match	scb1_uart_rx	tcpwm6_tr_overflow	swd_clk(alt)	–	scb1_spi_clk	scb1_i2c_scl	GPIO, TCPWM, SCB, SAR MUX input, SWD Clock alternate
	35	P1.2	sarmux_2	tcpwm5_line	tcpwm5_comp_match	scb1_uart_tx	tcpwm5_tr_overflow	swd_data(alt)	–	scb1_spi_miso	scb1_i2c_sda	GPIO, TCPWM, SCB, SAR MUX input, SWD Data alternate
	36	P1.1	sarmux_1	tcpwm4_line	tcpwm4_comp_match	scb0_uart_rts	tcpwm4_tr_overflow	swd_clk	–	scb0_spi_select	scb2_i2c_scl	GPIO, TCPWM, SCB, SAR MUX input, SWD Clock
	37	P1.0	sarmux_0	tcpwm3_line	tcpwm3_comp_match	scb0_uart_cts	tcpwm3_tr_overflow	swd_data	–	scb0_spi_mosi	scb2_i2c_sda	GPIO, TCPWM, SCB, SAR MUX input, SWD Data
	38	P2.2	sar_ext_vref	ext_clk1	–	scb1_uart_cts	–	tcpwmx_tr_in6	–	scb0_spi_miso	–	GPIO, TCPWM, SCB, ADC reference voltage, external clock input
	39	P2.3	–	tcpwm7_line	tcpwm7_comp_match	–	–	–	–	–	–	GPIO, TCPWM
	41	P3.0	–		–	scb0_uart_tx			–	scb1_spi_mosi	scb0_i2c_sda	GPIO, SCB
	42	P3.1	–	ext_clk	–	scb0_uart_rx	–	–	–	scb0_spi_clk	scb0_i2c_scl	GPIO, SCB, external clock input

Table 2 Pin list for PMG1-B1 CYPM1115-48LQXI and CYPM1116-48LQXI

Group	Pin No	Alternate functions (HSIOM_PORT_SEL)										Description
		Pin name	Analog	ACT#0	ACT#1	ACT#2	ACT#3	DS#0	DS#1	DS#2	DS#3	
Power	46	VIN	–	–	–	–	–	–	–	–	–	Input supply (4 - 24V)
	22	VDDD	–	–	–	–	–	–	–	–	–	5-V LDO output for filter capacitor
	44		–	–	–	–	–	–	–	–	–	
	40	XRES	–	–	–	–	–	–	–	–	–	External reset (active low)
	45	VCCD	–	–	–	–	–	–	–	–	–	1.8-V core LDO output for filter capacitor, this pin can not drive external loads.
	43	GND	–	–	–	–	–	–	–	–	–	Ground
	EPAD	GND	–	–	–	–	–	–	–	–	–	Ground, Connect directly to pin 36 and pin 22.

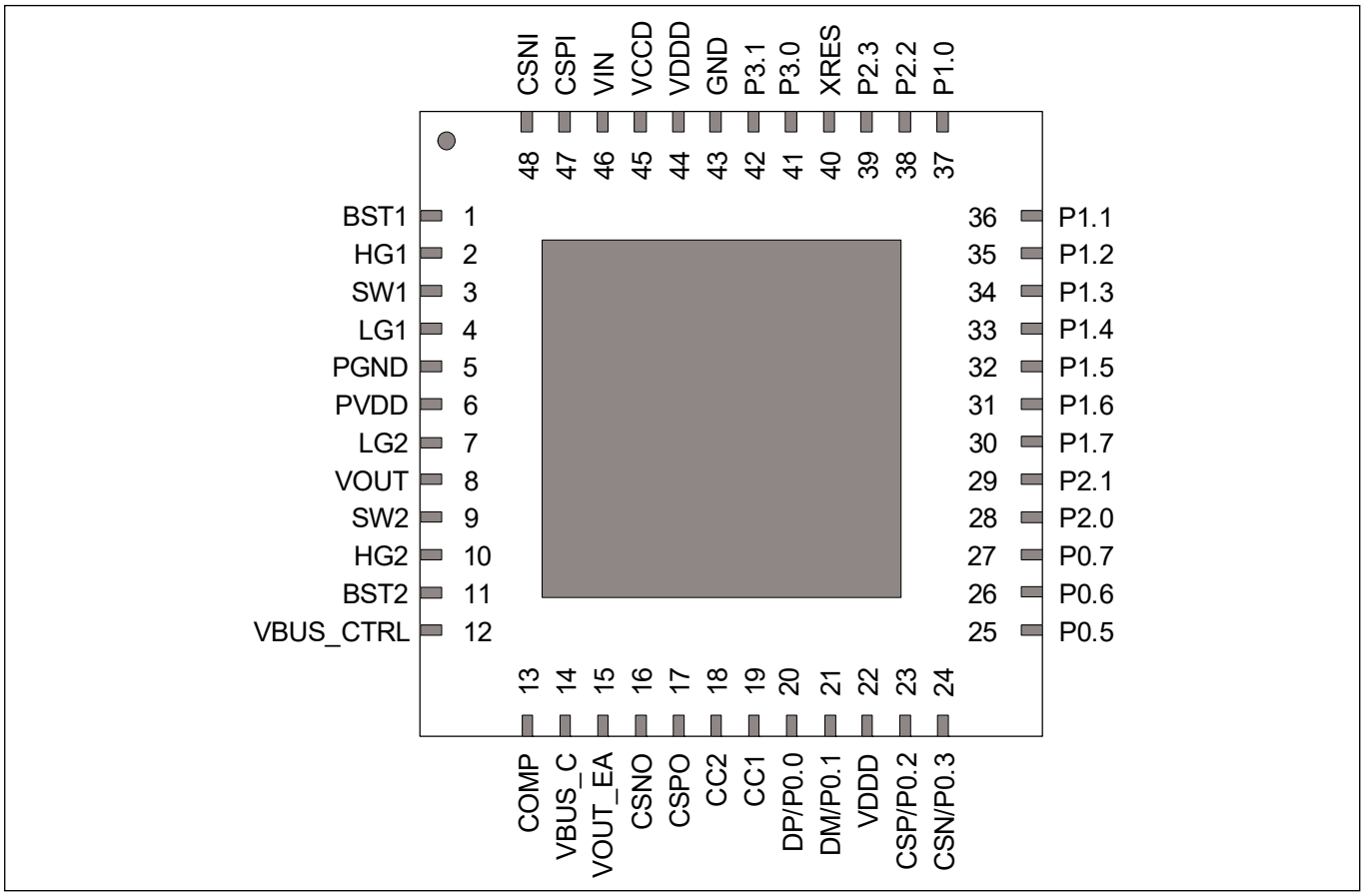

Figure 15 CYPM1311-48LDXI: single-port 48-pin QFN

5 Applications

Figure 16, **Figure 17**, and **Figure 18** shows the typical battery charging application for 2 to 5-cell application for USB PD sink and DRP applications.

1. Battery charging - Sink only operation

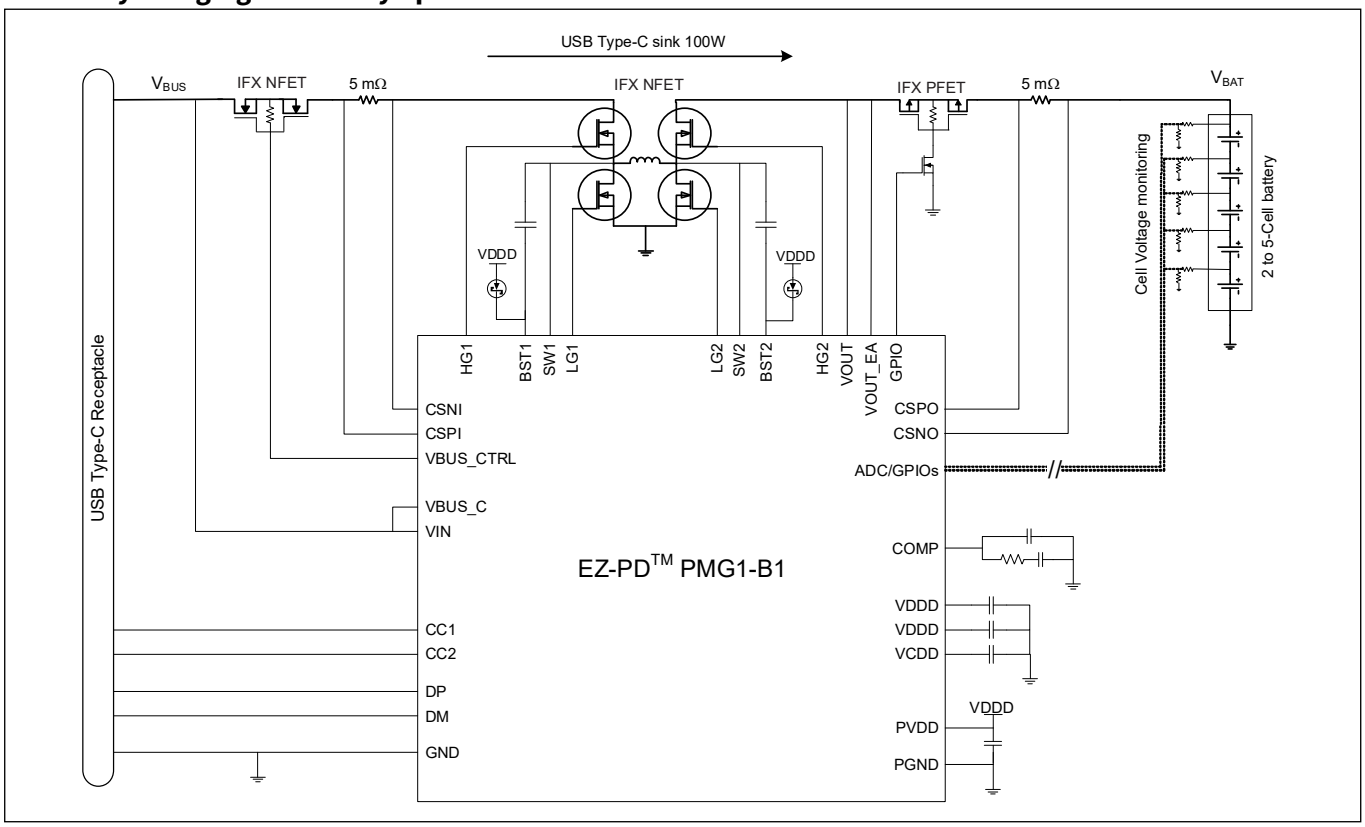

Figure 16 EZ-PD™ PMG1-B1 battery pack charging solution diagram

2. Battery charging - DRP operation with 100W sink and 27W source

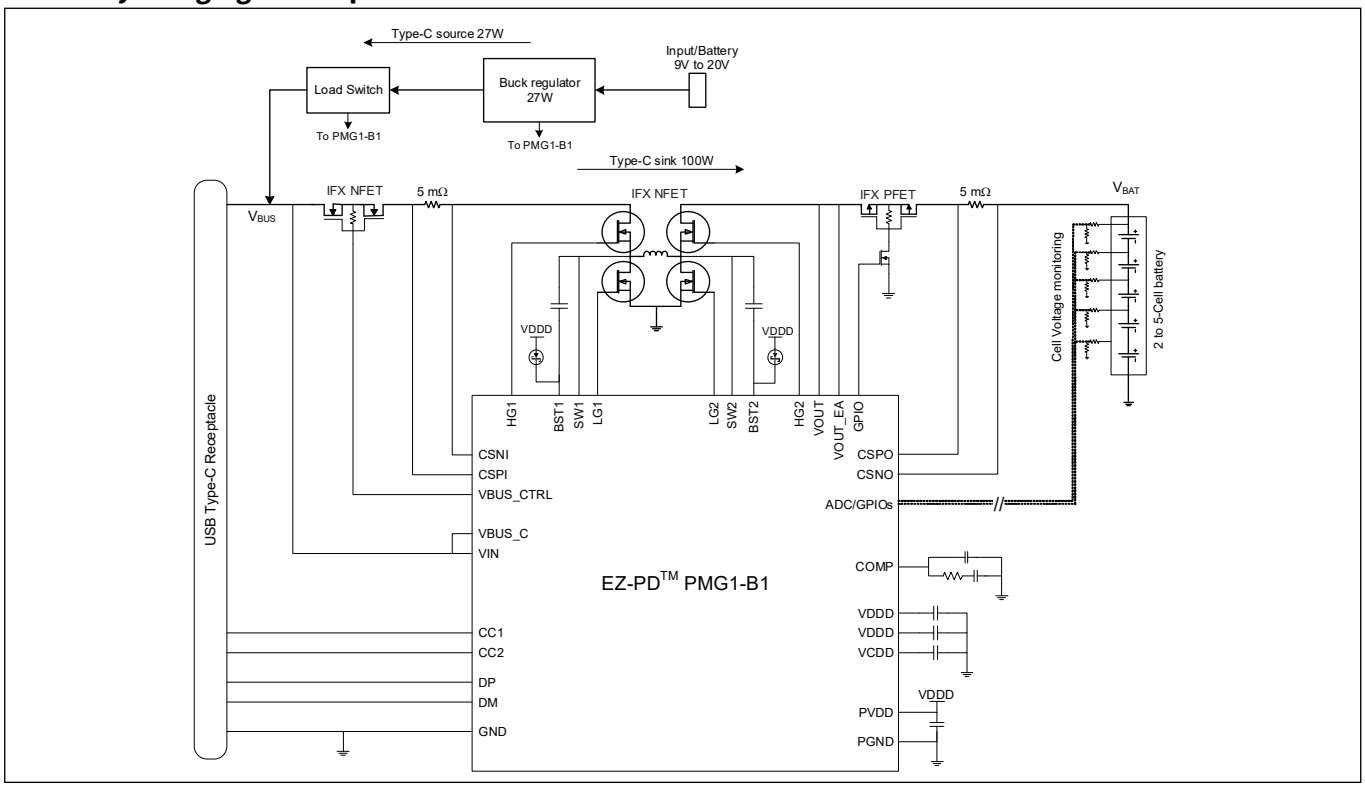

Figure 17 EZ-PD™ PMG1-B1 DRP battery charging 27 W

3. Battery charging - 100W DRP Bi-directional operation

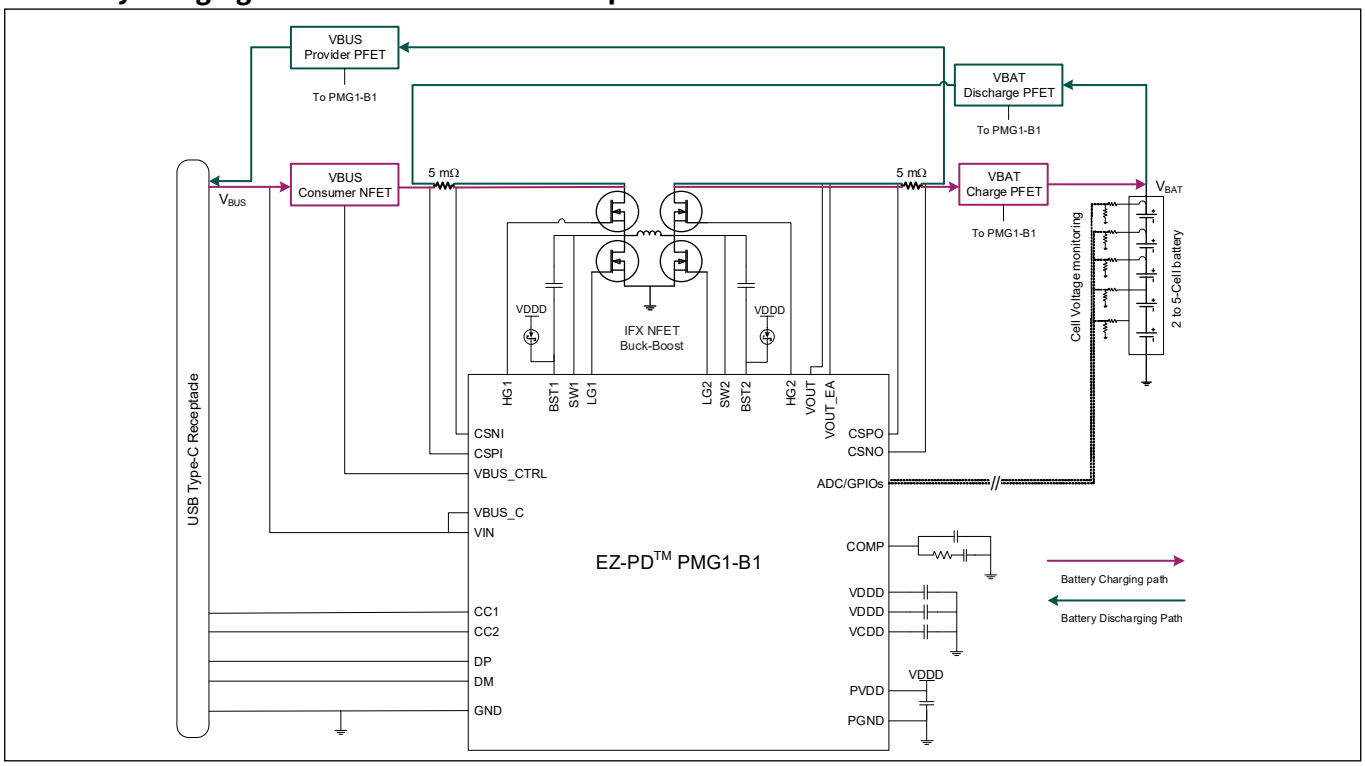

Figure 18 EZ-PD™ PMG1-B1 DRP battery charging 100 W

6 Electrical specifications

6.1 Absolute maximum ratings

Table 3 Absolute maximum ratings[2]

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
V_{IN_MAX}	Maximum input supply voltage	–	–	40	V	–
V_{DDD_MAX}	Maximum supply voltage relative to V_{SS}			6		
V_{5V_MAX}	Maximum supply voltage relative to V_{SS}					
$V_{BUS\_C\_MAX}$	Max V_{BUS_C} (P0/P1) voltage relative to V_{SS}			24		
$V_{CC\_PIN\_ABS}$	Max voltage on CC1 and CC2 pins					
V_{GPIO_ABS}	Inputs to GPIO	–0.5		V_{DDD} + 0.5		
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage			6		
I_{GPIO_ABS}	Maximum current per GPIO	–25		25	mA	
$I_{GPIO\_INJECTION}$	GPIO injection current, max for $V_{IH} > V_{DDD}$, and min for $V_{IL} < V_{SS}$	–0.5		0.5		Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2000		–	V	All pins
ESD_CDM	Electrostatic discharge charged device model	500				Charged device model ESD
LU	Pin current for latch-up	–100		100	mA	–
T_J	Junction temperature	–40		125	°C	

Table 4 Pin-based absolute maximum ratings

Pin no	Pin name	Absolute minimum (volts)[3]	Absolute maximum (volts)[3]	Remarks
1	BST1	–0.5	40	Maximum voltage not to exceed SW1 + PVDD
2	HG1			
3	SW1	–0.5	35	–
4	LG1	–0.5	6	–
5	PGND	–	–	–
6	PVDD	–	6	Short to VDDD at board level
7	LG2	–0.5	6	–
8	VOUT	–	24	–
9	SW2	–0.3	24	–
10	HG2	–0.5	32	Maximum voltage not to exceed SW2 + PVDD
11	BST2			
13	COMP	–0.5	6	–
15	VOUT_EA	–0.3	24	–
16	CSNO	–0.3	24	–
17	CSPO			–

Notes

2. Usage above the absolute maximum conditions listed in **Table 3** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
3. All voltages are measured with respect to GND.

Table 4 Pin-based absolute maximum ratings

Pin no	Pin name	Absolute minimum (volts)[3]	Absolute maximum (volts)[3]	Remarks
47	CSPI	–0.3	40	–
48	CSNI			–
12	VBUS_CTRL	–0.5	32	–
14	VBUS_C	–	24	–
18	CC2	–0.5	24	–
19	CC1			–
20	P0.0/DP	–0.5	6	Maximum voltage not to exceed VDDD + 0.5
21	P0.1/DM			
23	P0.2/CSP			
24	P0.3/CSN			
25	P0.5			
26	P0.6			
27	P0.7			
28	P2.0			
29	P2.1			
30	P1.7			
31	P1.6			
32	P1.5			
33	P1.4			
34	P1.3			
35	P1.2			
36	P1.1			
37	P1.0			
38	P2.2			
39	P2.3			
41	P3.0			
42	P3.1			
46	VIN	–0.5	40	–
22	VDDD	–	6	–
44				
40	XRES	–0.5	6	Maximum voltage not to exceed VDDD + 0.5
45	VCCD	–	–	–
43	GND	–	–	–
EPAD				

Notes

2. Usage above the absolute maximum conditions listed in **Table 3** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, high temperature storage life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
3. All voltages are measured with respect to GND.

6.2 Device-level specifications

All specifications are valid for –40°C ≤ T_A ≤ 105°C and T_J ≤ 125°C, except where noted. Specifications are valid for 3.0 to 5.5 V except where noted.

6.2.1 DC specifications

Table 5 DC Specifications (operating conditions)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	V_{IN}	Input supply voltage	4.0	–	24	V	–
SID.PWR#1A	V_{IN_BB}	Buck-boost operating input supply voltage	4.5				
SID.PWR#2	V_{DDD_REG}	VDDD output with VIN 5.5 to 24 V, max load = 75 mA	4.6		5.5		
SID.PWR#2A	V_{DDD_BYPASS}	VDDD output with VIN 4.5 to 5.5 V, max load = 75 mA	V_{IN} -0.7				
SID.PWR#3	V_{DDD_MIN}	VDDD output with VIN 4 to 4.5 V, max load = 20 mA	V_{IN} - 0.2		–		
SID.PWR#20	VBUS	VBUS_C valid range	3.3		21.5		
SID.PWR#5	V_{CCD}	Regulated output voltage (for core logic)	–	1.8	–		
SID.PWR#16	C_{EFC_VCCD}	External regulator voltage bypass for VCCD	80	100	120	nF	X5R ceramic
SID.PWR#17	C_{EXC_VDDD}	Power supply decoupling capacitor for V_{DDD}	–	10	–	µF	
SID.PWR#18	C_{EXV}	Bootstrap supply capacitor (BST1, BST2)		0.1			
SID.PWR#24	I_{DD_ACT}	Supply current at 0.4 MHz switching frequency		50		mA	T_A = 25°C, VIN = 12 V. CC IO IN transmit or receive, no I/O sourcing current, No VCONN load current, CPU at 24 MHz, PD port active. Buck-boost converter on, 3-nF gate driver capacitance.
Deep Sleep mode							
SID_DS1	I_{DD_DS1}	V_{IN} = 12 V. CC wakeup on, Type-C not connected, Source mode.	–	80	–	µA	Type-C not attached, CC enabled for wakeup. R_p connection should be enabled for the PD port. T_A = 25°C.
SID_DS2	I_{DD_DS2}	V_{IN} = 12 V, GPIO wake-up		50			USBPD disabled. Wake-up from GPIO. T_A = 25°C. All faults disabled.

6.2.2 CPU

Table 6 CPU specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#4	F_{CPU}	CPU input frequency	–	–	48	MHz	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.PWR#19	$T_{DEEPSLEEP}$	Wake-up from Deep Sleep mode		35	–	µs	–
SYS.XRES#5	T_{XRES}	External reset pulse width	5	–			
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to Accept I^2C/CC command”	–	5	25	ms	

6.2.3 GPIO

Table 7 GPIO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#9	V_{IH_CMOS}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID.GIO#10	V_{IL_CMOS}	Input voltage low threshold	–		0.3 × V_{DDD}		
SID.GIO#11	V_{IH_TTL}	LVTTL input	2.0		–		–40°C ≤ TA ≤ +105°C
SID.GIO#12	V_{IL_TTL}	LVTTL input	–		0.8		
SID.GIO#7	V_{OH_3V}	Output voltage high level	V_{DDD} – 0.6		–		I_{OH} = –4 mA, –40°C ≤ T_A ≤ +105°C
SID.GIO#8	V_{OL_3V}	Output voltage low level	–		0.6		I_{OL} = 10 mA, –40°C ≤ T_A ≤ +105°C
SID.GIO#2	Rpu	Pull-up resistor when enabled	3.5	5.6	8.5	kΩ	–40°C ≤ T_A ≤ +105°C
SID.GIO#3	Rpd	Pull-down resistor when enabled	3.5	5.6	8.5		
SID.GIO#4	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, 3-V V_{DDD}
SID.GIO#5	C_{PIN_A}	Max pin capacitance			22	pF	–40°C ≤ T_A ≤ +105°C, capacitance on DP, DM pins
SID.GIO#6	C_{PIN}	Max pin capacitance		3	7		–40°C ≤ T_A ≤ +105°C, all V_{DDD}, all other I/Os
SID.GIO#13	V_{HYSTTL}	Input hysteresis, LVTTL, V_{DDD} > 2.7 V	100	–	–	mV	V_{DDD} > 2.7 V
SID.GIO#14	$V_{HYSCMOS}$	Input hysteresis CMOS	0.1 × V_{DDD}				–

Table 8 GPIO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#16	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	C_{load} = 25 pF, –40°C ≤ T_A ≤ +105°C
SID.GIO#17	T_{FALLF}	Fall time in fast strong mode					
SID.GIO#18	T_{RISES}	Rise time in slow strong mode	10		60		
SID.GIO#19	T_{FALLS}	Fall time in slow strong mode					
SID.GIO#20	F_{GPIO_OUT1}	GPIO F_{OUT}; 3.0 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–		16	MHz	
SID.GIO#21	F_{GPIO_OUT2}	GPIO F_{OUT}; 3.0 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.			7		
SID.GIO#22	F_{GPIO_IN}	GPIO input operating frequency; 3.0 V ≤ V_{DDD} ≤ 5.5 V.			16		–40°C ≤ T_A ≤ +105°C

Table 9 GPIO fail-safe DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT_GIO#4	GPIO_20VT_I_LU	GPIO_20VT latch up current limits	-140		140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply
SID.GPIO_20VT_GIO#5	GPIO_20VT_RPU	GPIO_20VT pull-up resistor value	3.5		8.5	kΩ	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.GPIO_20VT_GIO#6	GPIO_20VT_RPD	GPIO_20VT pull-down resistor value			8.5		
SID.GPIO_20VT_GIO#16	GPIO_20VT_IIL	GPIO_20VT input leakage current (absolute value)	–		2	nA	+25°C T_A, 3-V V_{DDD}
SID.GPIO_20VT_GIO#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance			10	pF	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.GPIO_20VT_GIO#33	GPIO_20VT_Voh	GPIO_20VT output voltage high level	VDDD-0.6	–	–	V	I_{OH} = -4 mA
SID.GPIO_20VT_GIO#36	GPIO_20VT_Vol	GPIO_20VT output voltage low level	–		0.6		I_{OL} = 8 mA
SID.GPIO_20VT_GIO#41	GPIO_20VT_Vih_LVTTL	GPIO_20VT LVTTL input	2		–		–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.GPIO_20VT_GIO#42	GPIO_20VT_Vil_LVTTL	GPIO_20VT LVTTL input	–		0.8		
SID.GPIO_20VT_GIO#43	GPIO_20VT_Vhysttl	GPIO_20VT input hysteresis LVTTL	100		–	mV	
SID.GPIO_20VT_GIO#45	GPIO_20VT_ITOT_GPIO	GPIO_20VT maximum total sink pin current to ground	–		95	mA	V (GPIO_20VT pin) > V_{DDD}

Table 10 GPIO fail-safe AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO_20VT_70	GPIO_20VT_TriseF	GPIO_20VT rise time in fast strong mode	1	–	15	ns	All V_{DDD}, C_{load} = 25 pF
SID.GPIO_20VT_71	GPIO_20VT_TfallF	GPIO_20VT fall time in fast strong mode					
SID.GPIO_20VT_GIO#46	GPIO_20VT_TriseS	GPIO_20VT rise time in slow strong mode	10		70		
SID.GPIO_20VT_GIO#47	GPIO_20VT_TfallS	GPIO_20VT fall time in slow strong mode					
SID.GPIO_20VT_GIO#48	GPIO_20VT_FGPIO_OUT1	GPIO_20VT GPIO Fout; 3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–		33	MHz	
SID.GPIO_20VT_GIO#50	GPIO_20VT_FGPIO_OUT3	GPIO_20VT GPIO Fout; 3 V≤V_{DDD}≤5.5V. Slow strong mode.			7		
SID.GPIO_20VT_GIO#52	GPIO_20VT_FGPIO_IN	GPIO_20VT GPIO input operating frequency; 3 V ≤ V_{DDD} ≤ 5.5 V			8		All V_{DDD}

6.2.4 XRES

Table 11 XRES DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.XRES#1	V_{IH_XRES}	Input voltage high threshold on XRES pin	0.7 × V_{DDD}	–	–	V	CMOS input
SID.XRES#2	V_{IL_XRES}	Input voltage low threshold on XRES pin	–		0.3 × V_{DDD}		
SID.XRES#3	C_{IN_XRES}	Input capacitance on XRES pin			7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis on XRES pin		0.05 × V_{DDD}	–	mV	

6.3 Digital peripherals

6.3.1 Pulse-width modulation (PWM) for GPIO pins

Table 12 PWM AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS
SID.TCPWM.3	T_{PWMEXT}	Output trigger pulse width	2/Fc		–	ns	Minimum possible width of overflow, underflow, and CC (counter equals compare value) outputs
SID.TCPWM.4	T_{CRES}	Resolution of counter	1/Fc				Minimum time between successive counts
SID.TCPWM.5	PWM_{RES}	PWM resolution					Minimum pulse width of PWM output

6.3.2 I^2C

Table 13 Fixed I^2C AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

6.3.3 UART

Table 14 Fixed UART AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

6.3.4 SPI

Table 15 Fixed SPI AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	–

Table 16 Fixed SPI master mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID167	T_{DMO}	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO valid before SClock capturing edge	20		–		Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0				Referred to slave capturing edge

Table 17 Fixed SPI slave mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO valid after Sclock driving edge	–		48 + (3 × T_{CPU})		$T_{CPU} = 1/F_{CPU}$
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in ext clk mode			48		–
SID172	T_{HSO}	Previous MISO data hold time	0		–		
SID172A	$T_{SSELSCK}$	SSEL valid to first SCK valid edge	100				

6.3.5 Memory

Table 18 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#2	FLASH_WRITE	Row (block) write time (Erase and program)	–	–	20	ms	–40°C ≤ T_A ≤ +85°C, all V_{DDD}
SID.MEM#1	FLASH_ERASE	Row erase time			15.5		
SID.MEM#5	FLASH_ROW_PGM	Row program time after erase			7		
SID178	$T_{BULKERASE}$	Bulk erase time (32 KB)			35		–
SID180	$T_{DEVPROG}$	Total device program time			7.5	s	
SID.MEM#6	FLASH_$_{ENPB}$	Flash write endurance	100k		–	cycles	25°C ≤ T_A ≤ 55°C, all V_{DDD}
SID182	F_{RET1}	Flash retention, T_A ≤ 55°C, 100K P/E cycles	20			years	–
SID182A	F_{RET2}	Flash retention, T_A ≤ 85°C, 10K P/E cycles	10				

6.4 System resources

6.4.1 Power-on and brown-out reset

Table 19 Power-on reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID185	$V_{RISEIPOR}$	Power-on reset (POR) rising trip voltage	0.80	–	1.50	V	–40°C ≤T_A ≤ +105°C, all V_{DDD}
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70		1.4		

Table 20 Brown-out reset (BOR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	$V_{FALLPPOR}$	Brown-out detect (BOD) trip voltage in Active/Sleep modes	1.48	–	1.62	V	–40°C ≤T_A ≤ +105°C, all V_{DDD}
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1		1.5		

6.4.2 SWD interface

Table 21 SWD interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.SWD#1	F_SWDCLK1	3.0 V ≤ V_{DDIO} ≤ 5.5 V	–	–	14	MHz	–
SID.SWD#2	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T		–	ns	–
SID.SWD#3	T_SWDI_HOLD						
SID.SWD#4	T_SWDO_VALID		–		0.50 × T		
SID.SWD#5	T_SWDO_HOLD		1		–		

6.4.3 Internal main oscillator

Table 22 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 48 MHz (trimmed)	–	–	±2	%	3.0 V ≤ V_{DDD} < 5.5 V. –40°C ≤ T_A ≤ 105°C
SID226	$T_{STARTIMO}$	IMO start-up time			7	µs	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID.CLK#1	F_{IMO}	IMO frequency	24		48	MHz	

6.4.4 Internal low-speed oscillator

Table 23 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234	$T_{STARTILO1}$	ILO start-up time	–	–	2	ms	–40°C ≤ T_A ≤ +105°C, all V_{DDD}
SID238	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	
SID.CLK#5	F_{ILO}	ILO frequency	20	40	80	kHz	–

6.4.5 USB PD

Table 24 PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.cc_shvt.1	vSwing	Transmitter output high voltage	1.05		1.2	V	
SID.DC.cc_shvt.2	vSwing_low	Transmitter output low voltage	–		0.075		
SID.DC.cc_shvt.3	zDriver	Transmitter output impedance	33		75	W	
SID.DC.cc_shvt.4	zBmcRx	Receiver input impedance	10			MΩ	
SID.DC.cc_shvt.5	Idac_std	Source current for USB standard advertisement	64		96	µA	
SID.DC.cc_shvt.6	Idac_1p5a	Source current for 1.5A at 5 V advertisement	166		194		
SID.DC.cc_shvt.7	Idac_3a	Source current for 3A at 5 V advertisement	304		356		
SID.DC.cc_shvt.8	Rd	Pull down termination resistance when acting as UFP (upstream facing port)	4.59		5.61	kΩ	
SID.DC.cc_shvt.10	zOPEN	CC impedance to ground when disabled	108	–			–
SID.DC.cc_shvt.11	DFP_default_0p2	CC voltages on DFP side-standard USB	0.15		0.25	V	
SID.DC.cc_shvt.12	DFP_1.5A_0p4	CC voltages on DFP side-1.5A	0.35		0.45		
SID.DC.cc_shvt.13	DFP_3A_0p8	CC voltages on DFP side-3A	0.75		0.85		
SID.DC.cc_shvt.14	DFP_3A_2p6	CC voltages on DFP side-3A	2.45		2.75		
SID.DC.cc_shvt.15	UFP_default_0p66	CC voltages on UFP side-standard USB	0.61		0.7		
SID.DC.cc_shvt.16	UFP_1.5A_1p23	CC voltages on UFP side-1.5A	1.16		1.31		
SID.DC.cc_shvt.17	Vattach_ds	Deep Sleep attach threshold	0.3		0.6	%	
SID.DC.cc_shvt.18	Rattach_ds	Deep Sleep pull-up resistor	10		50	kΩ	
SID.DC.cc_shvt.19	VTX_step	TX drive voltage step size	80		120	mV	

6.4.6 Analog-to-digital converter

Table 25 8-bit SAR ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap.
SID.ADC.3	DNL	Differential non-linearity	–2.5		2.5		Reference voltage generated from V_{DDD}.
SID.ADC.4	Gain Error	Gain error	–1.5		1.5		Reference voltage generated from bandgap.
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	V_{DDDmin}		V_{DDDmax}	V	Reference voltage generated from V_{DDD}.
SID.ADC.6	VREF_ADC2		1.96	2.0	2.04		Reference voltage generated from Deep Sleep reference.

Table 26 12-bit SAR ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC12.DC.2	A_RES_1	Resolution	–	–	12	bits	IMO/HFCLK at 48 MHz
SID.ADC12.DC.3	A_CHNLS_S	Number of channels - single ended			8		8 full speed
SID.ADC12.DC.4	A-CHNKS_D	Number of channels - differential			4		Differential inputs use adjacent I/O.
SID.ADC12.DC.5	A-MONO	Monotonicity			–		Yes
SID.ADC12.DC.6	A_GAINERR	Gain error			±0.1	%	With external reference.
SID.ADC12.DC.7	A_OFFSET	Input offset voltage			2	mV	Measured with 1 V reference.
SID.ADC12.DC.8	A_ISAR	Current consumption			1	mA	–
SID.ADC12.DC.9	A_VINS	Input voltage range - single ended	V_{SS}		V_{DDD}	V	
SID.ADC12.DC.10	A_VIND	Input voltage range - differential					
SID.ADC12.DC.11	A_INRES	Input resistance	–		2.2	kΩ	
SID.ADC12.DC.12	A_INCAP	Input capacitance			10	pF	

Table 27 12-bit SAR ADC AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC12.AC.1	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID.ADC12.AC.2	A_CMRR	Common mode rejection ratio	66				Measured at 1 V.
SID.ADC12.AC.3	A_SAMP_1	Sample rate with external reference bypass cap.	–		1	Msps	–
SID.ADC12.AC.4	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}.			500	Ksps	
SID.ADC12.AC.5	A_SAMP_3	Sample rate with no bypass cap. Internal reference.			100		
SID.ADC12.AC.6	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65		–	dB	Fin = 10 kHz
SID.ADC12.AC.7	A_BW	Input bandwidth without aliasing	–		A_samp/2	kHz	–
SID.ADC12.AC.8	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 1 Msps	-1.7		2	LSB	Vref = 1 to V_{DD}
SID.ADC12.AC.9	A_INL	Integral non linearity. V_{DDD} = 1.71 to 3.6, 1 Msps	-1.5		1.7		Vref = 1.71 to V_{DD}
SID.ADC12.AC.10	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 500 ksps					Vref = 1 to V_{DD}

6.4.7 VCONN switch

Table 28 VCONN switch DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DC.VCONN.1	VCONN_OUT	VCONN output voltage with 20 mA load current	4.5	–	5.5	V	–
DC.VCONN.2	I_{LEAK}	Connector side pin leakage current	–		10	µA	
DC.VCONN.3	I_{OCP}	VCONN overcurrent protection threshold	22.5	30	42.5	mA	

Table 29 VCONN switch AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
AC.VCONN.1	T_{ON}	VCONN switch turn-on time	–	–	600	µs	–
AC.VCONN.2	T_{OFF}	VCONN switch turn-off time			10		

6.4.8 VBUS discharge

Table 30 VBUS discharge specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.VBUS.DISC.1	R1	20-V NMOS ON resistance for DS = 1	500	–	2000	Ω	Measured at 0.5 V.
SID.VBUS.DISC.2	R2	20-V NMOS ON resistance for DS = 2	250		1000		
SID.VBUS.DISC.3	R4	20-V NMOS ON resistance for DS = 4	125		500		
SID.VBUS.DISC.4	R8	20-V NMOS ON resistance for DS = 8	62.5		250		
SID.VBUS.DISC.5	R16	20-V NMOS ON resistance for DS = 16	31.25		125		
SID.VBUS.DISC.6	Vbus_stop_error	Error percentage of final VBUS value from setting	–		10	%	When VBUS is discharged to 5 V.

6.4.9 Voltage regulator

Table 31 Voltage regulation DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.DC.VR.1	VOUT	CSNO output voltage range	3.3	–	21.5	V	–
SID.DC.VR.2	VR	CSNO voltage regulation accuracy	–	±3	±5	%	
SID.DC.VR.3	VIN_UVLO	VIN supply below which chip will get reset	1.7	–	3.0	V	
SID.VREG.1	T_{START}	Total startup time for the regulator supply outputs	–	–	200	µs	

6.4.10 VBUS gate driver

Table 32 VBUS gate driver DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.1	GD_VGS	Gate to source overdrive during ON condition	4.5	5	10	V	NFET driver is ON
SID.GD.2	GD_RPD	Resistance when pull-down enabled	–	–	2	kΩ	Applicable on VBUS_CTRL to turn off external NFET.
SID.GD.5	GD_drv	Programmable typical gate current	0.3		9.75	µA	–

Table 33 VBUS gate driver AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GD.3	T_{ON}	VBUS_CTRL low to high (1V to VBUS + 1 V) with 3 nF external capacitance	2	5	10	ms	CSNO = 5 V
SID.GD.4	T_{OFF}	VBUS_CTRL high to low (90% to 10%) with 3 nF external capacitance	–	7	–	µs	CSNO = 21.5 V

6.4.11 Thermal

Table 34 Thermal specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.OTP.1	OTP	Thermal shutdown	120	125	130	°C	–

6.4.12 Buck boost controller

Table 35 HS CSA DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.HSCSA.1	Csa_Acc1	CSA accuracy 5 mV < Vsense < 10 mV	–15	–	15	%	Active mode
SID.HSCSA.2	Csa_Acc2	CSA accuracy 10 mV < Vsense < 15 mV	–10		10		
SID.HSCSA.3	Csa_Acc3	CSA accuracy 15 mV < Vsense < 25 mV	–5		5		
SID.HSCSA.4	Csa_Acc4	CSA accuracy 25 mV < Vsense	–3		3		
SID.HSCSA.7	Csa_SCP_Acc1	CSA SCP at 6A with 5-mΩ sense resistor	–10		10		
SID.HSCSA.8	Csa_SCP_Acc2	CSA SCP at 10A with 5-mΩ sense resistor					
SID.HSCSA.9	Csa_OCP_1A	CSA OCP at 1A with 5-mΩ sense resistor	104	130	156		
SID.HSCSA.10	Csa_OCP_5A	CSA OCP for 5A with 5-mΩ sense resistor	123		137		

Table 36 HS CSA AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.HSCSA.AC.1	T_{SCP_GATE}	Delay from SCP threshold trip to external NFET power gate turn off	–	3.5	–	µs	1 nF NFET gate
SID.HSCSA.AC.2	$T_{SCP\_GATE\_1}$	Delay from SCP threshold trip to external NFET power gate turn off		8			3 nF NFET gate

Table 37 Buck-boost PWM controller specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
PWM.1	F_{SW}	Switching frequency	150	–	600	kHz	–
PWM.2	FSS	Spread spectrum frequency dithering span	–	10	–	%	
PWM.3	Ratio_buck_BB	Buck to buck boost ratio		1.16		V/V	
PWM.4	Ratio_boost_BB	Boost to buck boost ratio		0.84			

Table 38 Buck-boost NFET gate driver specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
DR.1	R_HS_PU	Top-side gate driver on-resistance-gate pull-up	–	2	–	Ω	–
DR.2	R_HS_PD	Top-side gate driver on-resistance-gate pull-down		1.5			
DR.3	R_LS_PU	Bottom-side gate driver on-resistance-gate pull-up		2			
DR.4	R_LS_PD	Bottom-side gate driver on-resistance-gate pull-down		1.5			
DR.5	Dead_HS	Dead time before high-side rising edge		30		ns	
DR.6	Dead_LS	Dead time before low-side rising edge		30			
DR.7	Tr_HS	Top-side gate driver rise time		25			
DR.8	Tf_HS	Top-side gate driver fall time		20			
DR.9	Tr_LS	Bottom-side gate driver rise time		25			
DR.10	Tf_LS	Bottom-side gate driver fall time		20			

Table 39 LS-SCP DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.LSSCP.DC.1	SCP_6A	Short circuit current detect @ 6A	5.4	6	6.6	A	Using differential inputs (CSP_GPIO2, CSN_GPIO3)
SID.LSSCP.DC.1A	SCP_6A_SE	Short circuit current detect @ 6A	4.5	6	7.5		Using single ended inputs (CSP_GPIO2) and internal ground
SID.LSSCP.DC.2	SCP_10A	Short circuit current detect @10A	9	10	11		Using differential inputs (CSP_GPIO2, CSN_GPIO3)
SID.LSSCP.DC.2A	SCP_10A_SE	Short circuit current detect @10A	7.5	10	12.5		Using single ended inputs (CSP_GPIO2) and internal ground

Table 40 UV/OV specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.UVOV.1	VTHOV1	Overvoltage threshold accuracy, 4 to 11 V	–3	–	3	%	Active mode
SID.UVOV.2	VTHOV2	Overvoltage threshold accuracy, 11 to 21.5 V	–3.2		3.2		
SID.UVOV.3	VTHUV1	Undervoltage threshold accuracy, 3 to 3.3 V	–4		4		
SID.UVOV.4	VTHUV2	Undervoltage threshold accuracy, 3.3 to 4.0 V	–3.5		3.5		
SID.UVOV.5	VTHUV3	Undervoltage threshold accuracy, 4.0 to 21.5 V	–3		3		

7 Ordering information

Table 41 lists the EZ-PD™ PMG1-B1 part numbers and features.

Table 41 EZ-PD™ PMG1-B1 ordering information

MPN	Termination resistor	Role	Switching frequency	Package type	Silicon ID
CYPM1115-48LQXI	R_P, R_D	Sink and DRP	150 to 600 kHz	48-pin QFN	0x3A2011CA
CYPM1116-48LQXI	R_P, R_D, R_{D-DB}				0x3A2111CA

7.1 Ordering code definition

The part numbers are of the form CYPM1ABC-DEFGHIJ where the fields are defined as follows.

Table 42 EZ-PD™ PMG1-B1 ordering code definitions

Field	Description	Values	Meaning
CY	CYPRESS prefix	CY	Company ID
PM	Marketing code	PM	PM = Power Delivery MCU family
1	MCU family generation	1	Product family generation
A	Family	0	S0
		1	S1, B1
		2	S2
		3	S3
B	PD Ports	1	1-PD port
		2	2-PD port
C	Application specific	5	R_P, R_D (no dead battery support)
		6	R_P, R_D, R_{D-DB} (dead battery support)
DE	Pin	XX	Number of pins in the package
FG	Package code	LQ	QFN
		BZ	BGA
		FN	CSP
H	Lead free	X	Lead: X = Pb-free
I	Temperature range	I	Industrial
J	Only for T&R	T	Tape and reel

8 Packaging

Table 43 Package characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_J	Operating junction temperature	–	-40	25	125	°C
T_{JA}	Package θ_{JA}		–	–	18.81	°C/W
T_{JC}	Package θ_{JC}				10.1	

8.1 Package diagram

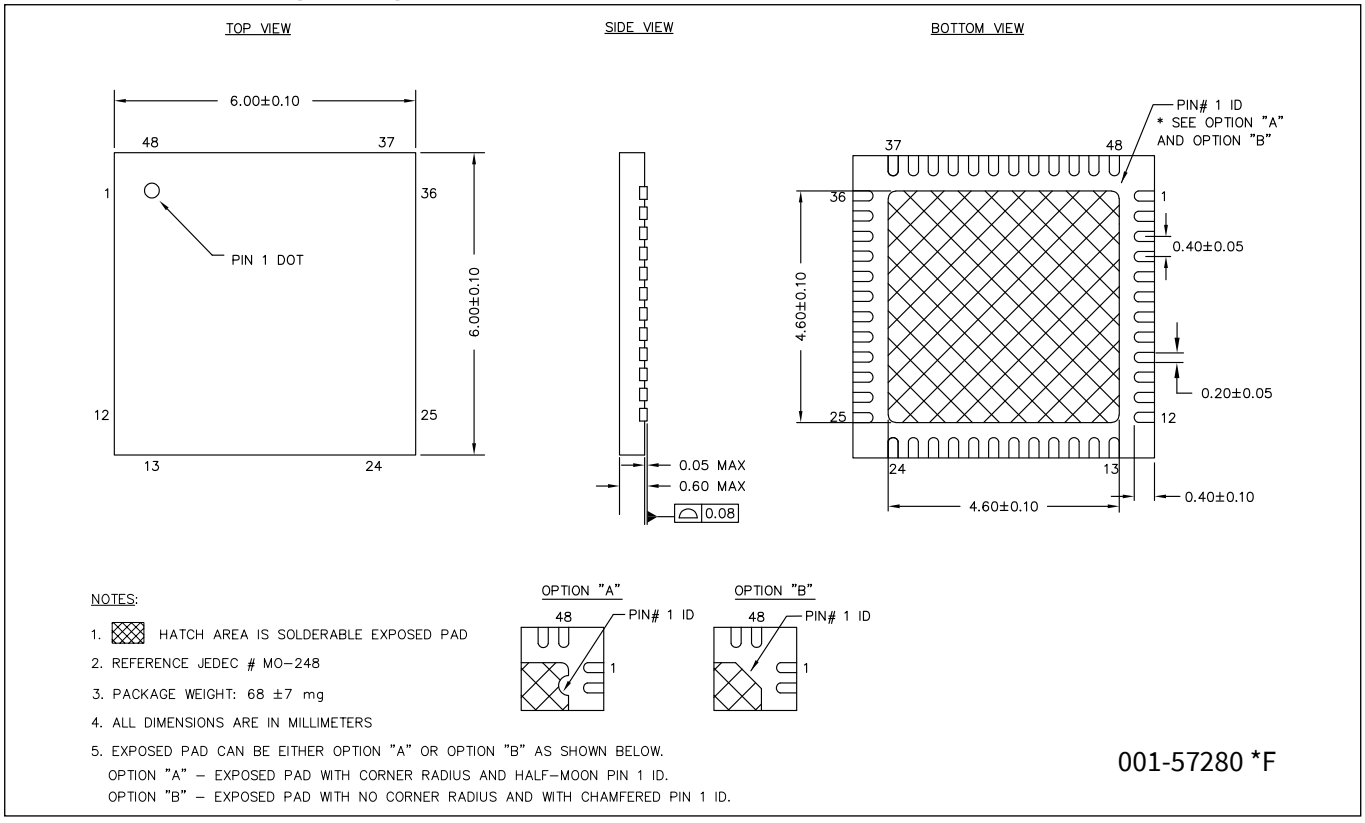

Figure 19 48-QFN package outline (PG-VQFN-48)

9 Acronyms

Table 44 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
AFC	Samsung adaptive fast charging
Arm®	advanced RISC machine, a CPU architecture
CPU	central processing unit
CSA	current sense amplifier
DAC	digital-to-analog converter
FCCM	forced continuous current/conduction mode
GPIO	general-purpose input/output
HSDR	high-side driver
I^2C, or IIC	inter-integrated circuit, a communications protocol
IDAC	current DAC
I/O	input/output, see also GPIO
LSDR	low-side driver
MCU	microcontroller unit
OCP	overcurrent protection
OVP	overvoltage protection
PD	power delivery
POR	power-on reset
PSM	pulse skipping mode
PWM	pulse-width modulator
RAM	random-access memory
SPI	serial peripheral interface, a communications protocol
SRAM	static random access memory
TCPWM	timer/counter/PWM
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	universal asynchronous transmitter receiver, a communications protocol
UFP	upstream facing port
UVP	undervoltage protection
USB	universal serial bus
UVLO	under-voltage lockout
VPA	VCONN powered accessories
ZCD	zero crossing detector

10 Document conventions

10.1 Units of measure

Table 45 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mΩ	milliohm
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second

Revision history

Document revision	Date	Description of changes
*D	2022-12-19	Publish to web.
*E	2025-09-15	Updated title from “EZ-PD™ PMG1-B1 USB Type-C Buck-boost controller” to “EZ-PD™ PMG1-B1: 2 to 5-cell battery charge controller with USB-C PD MCU”. Updated **General description**, **Applications**, **Features**, **Block diagram**, **Functional overview**, **Pinouts**, and **Applications**. Added **Development support**. Updated **Figure 7**, and **Figure 15**. Added **Table 4**. Added **Buck boost controller**. Updated **Table 41**. Updated package diagram 001-57280 (Rev. *E to *F) in **Figure 19**.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-09-15
Published by

Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Email:
erratum@infineon.com

Document reference
002-35400 Rev. *E

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”).

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.