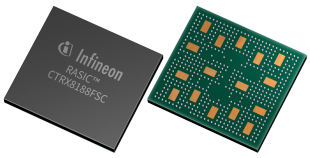
76-81 GHz Radar Transceiver with Antenna Feed in Package



AEC Qualified

RoHS

ISO 26262 compliant

Features

- Eight transmit channels and eight receive channels in form of waveguide ports
- Radio Frequency (RF) range from 76 GHz to 81 GHz, with fast chirp modulation up to 200 MHz/µs and maximum chirp bandwidth of 4 GHz
- RF performance: TX output power of 13.5 dBm, TX phase noise of -100 dBc/Hz at 1 MHz, and RX noise figure (10 MHz) of 10 dB
- Scalability by cascading of several transceivers
- Highly flexible sequencer with built-in memory for execution of user defined ramp scenarios
- Digital Phase Locked Loop (DPLL) enables complex ramp scenario and fast modulation adaptation
- Industry leading RX input linearity (P_{1dB} min. -2.5 dBm)
- Widely configurable Intermediate Frequency (IF) signal
- Optimized for low power consumption
- Configurable Camera Serial Interface 2 (MIPI CSI-2) Interface
- Control and configure via Serial Peripheral Interface (SPI) (up to 50 Mbps)
- Built-in calibration and monitoring functionalities for safety applications
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL B
- RoHS-compliant Flip Chip Ball Grid Array (FCBGA) package with 0.5 mm ball pitch

Potential applications

- Automatic Emergency Braking (AEB)
- Highway Assist/Pilot including Adaptive Cruise Control (ACC)
- Lane-Change Assistant (LCA)
- Traffic Jam Assist/Pilot (TJA)

Product validation

Product validation according to AEC-Q100 Grade 1, qualified for automotive applications.

Description

Infineon's RASIC™ CTRX8188F is a 77GHz radar transceiver for automotive ADAS applications featuring eight transmit and eight receive channels. This radar MMIC achieves high output power at low power consumption and industry leading noise figure ensuring market leading SNR. High channel count allows for optimum coverage in both the azimuth plane and elevation enabling more complex scenarios for ADAS radars. The flexible configurable CSI-2 interface provides full compatibility to available processing solutions while also enabling connection of the device via a single CSI-2 interface.

The device has been designed using the latest automotive qualified RF technology and is housed inside an automotive qualified FCBGA package.

Product type	Package	Marking
CTRX8188F	PG-TF2BGA-457-1	CTRX8188F

***Note**:* • *The full datasheet for this product is available under NDA.*

Table of contents

1 Device configurations

The CTRX8188F can be used as STAND-ALONE, PRIMARY or SECONDARY MMIC enabling a cascaded setup.

STAND-ALONE configuration:

In this configuration, the device does not use the CLKIN/CLKOUT or LOIN/LOOUT ports. Instead, the reference oscillator interface (XIN/XOUT) is employed: a crystal is connected across XIN and XOUT, or an external active clock source is applied to XIN. The internal clock and LO are derived from the selected reference.

PRIMARY configuration:

In this configuration, the device acts as the system reference source. The reference oscillator interface (XIN/XOUT) is used: a crystal is connected across XIN and XOUT, or an external active clock source is applied to XIN. From this reference, the device derives and outputs the LO at LOOUT and a clock at CLKOUT, along with a trigger to initiate a frequency ramp scenario. In PRIMARY configuration, CLKOUT and LOOUT must be fed back to the CLKIN and LOIN pins, respectively (self-feeding). Internal clock and the LO path are derived from CLKIN and LOIN.

SECONDARY configuration:

In this configuration, the device is synchronized to a PRIMARY MMIC. It accepts the reference clock and ramp trigger at CLKIN and receives the LO at one of the two LOIN inputs. The XIN/XOUT, CLKOUT, and LOOUT ports are not used in this mode. Internal clock is derived from CLKIN, and the LO path is driven by the selected LOIN input.

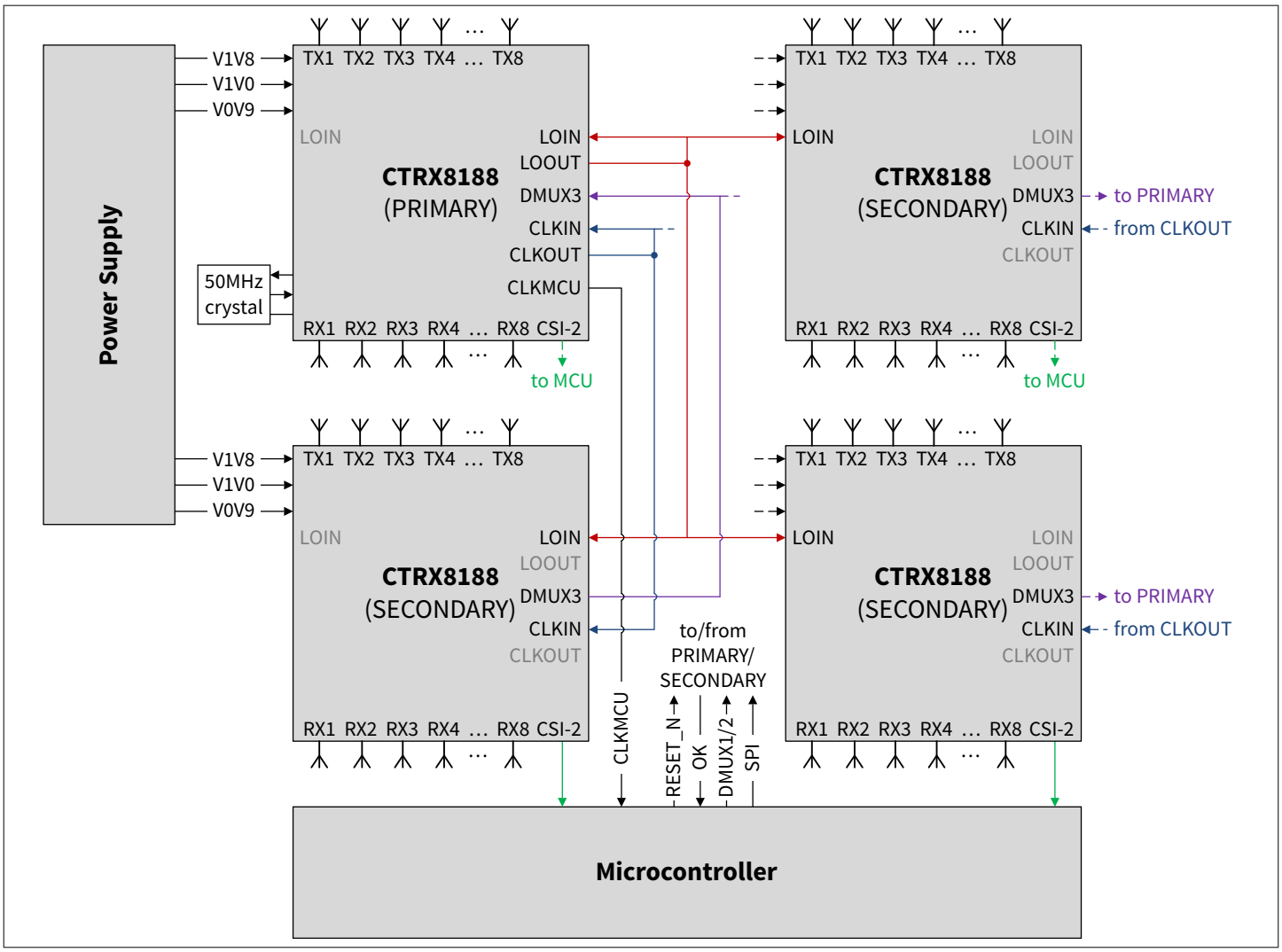


Figure 1 Application example for 4 cascaded MMIC

2 Block diagram

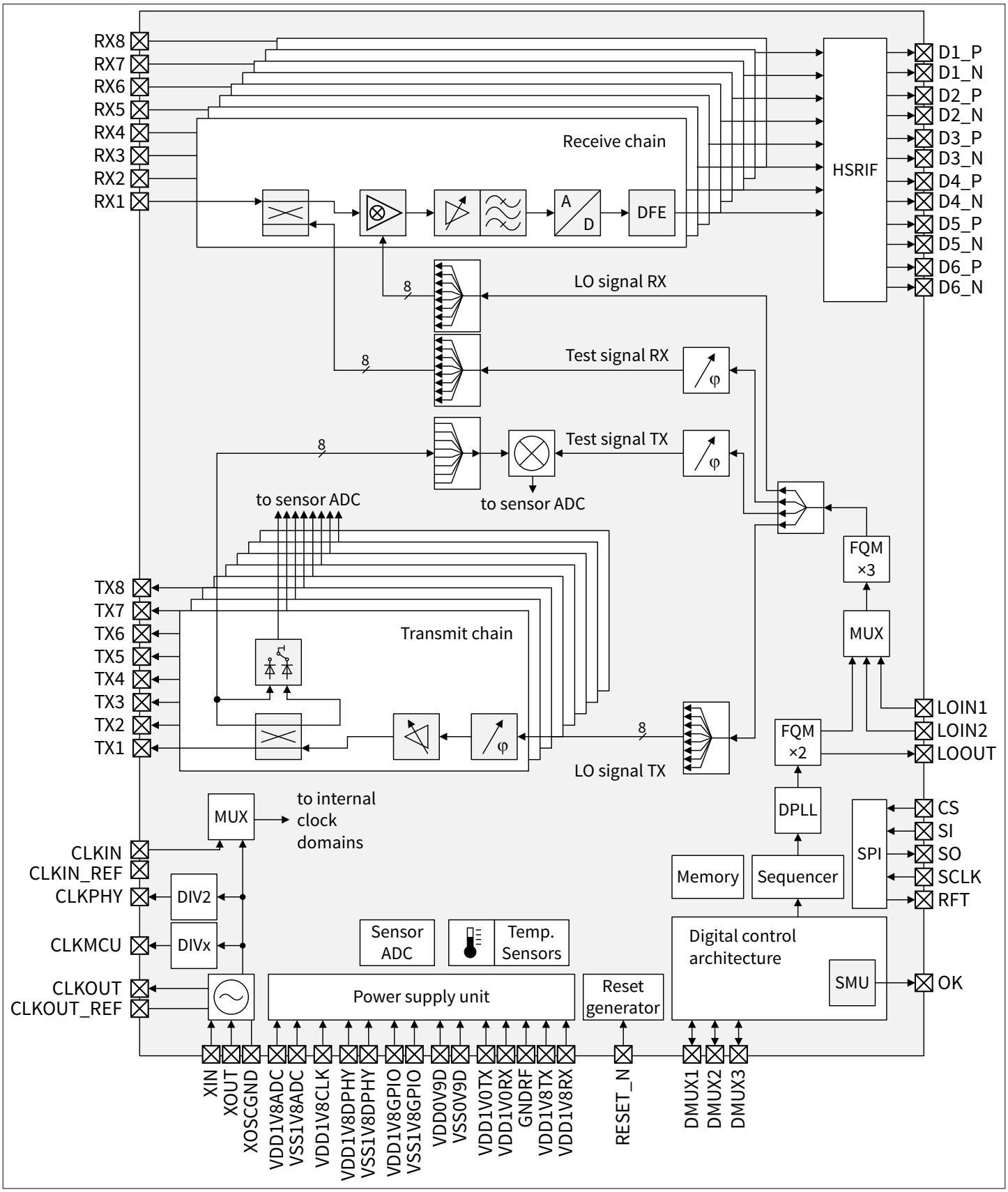


Figure 2 Block diagram

3 Product characteristics

Table 1 Average power consumption of typical application use cases

Parameter	Description	Typ. Value	Unit	Condition
Average power consumption	Radar cycle 40 ms each (averaged over 2 cycles): 20 ms acquisition, 1.5 ms monitoring, 14 ms low power state, 4.5 ms calibration. TX/RX monitoring spread across 2 cycles, TX/RX calibration done every 10th cycle.	2.2	W	3 TX (at max. power), 8 RX
		2.4	W	4 TX (at max. power), 8 RX
		2.6	W	5 TX (at max. power), 8 RX
		2.8	W	6 TX (at max. power), 8 RX
		3.0	W	7 TX (at max. power), 8 RX
		3.2	W	8 TX (at max. power), 8 RX

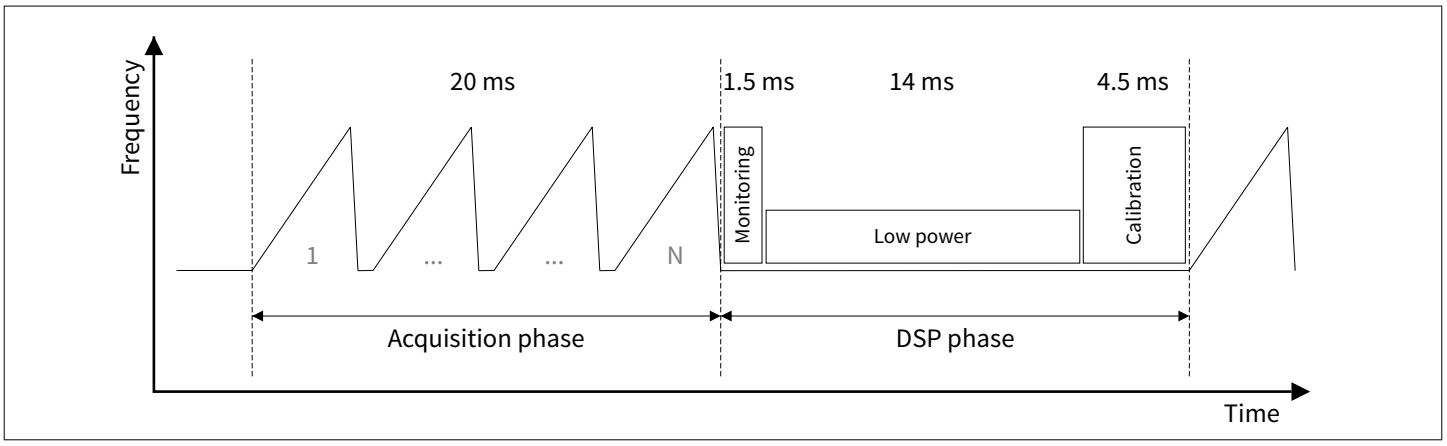


Figure 3 Example use case for average power consumption

Table 2 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Operating temperature	T_J	-40	–	135	°C	On-chip temperature sensor read values. Ambient temperature not below -40°C according to AEC-Q100 grade 1.
RF operating frequency	f_{RF}	76	–	81	GHz	–
Channel to channel isolation	ISO	–	40	–	dB	Applicable for an Infineon reference footprint.
IF bandwidth	f_{IF}	0.001	–	22.5	MHz	–
Output sample rate	R_{OSR}	–	–	50	MS/s	Effective output sample rate after decimation

(table continues...)

Table 2 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
CSI-2 data rate	R_{CSI-2}	800	–	1200	Mbps	–
Transmitter						
RF output power at maximum setting	P_{out}	–	13.5	–	dBm	Maximal output power setting of a single TX channel.
TX phase noise @ 1 MHz, RF range 1	$N_{\varphi\_1M\_RF1}$	–	-100	–	dBc/Hz	Valid for 76 ≤ f_{RF} ≤ 77 GHz. Continuous wave (CW) mode. f_{offset} = 1 MHz.
TX phase noise @ 1 MHz, RF range 2	$N_{\varphi\_1M\_RF2}$	–	-98	–	dBc/Hz	Valid for 77 GHz < f_{RF} ≤ 81 GHz. Continuous wave (CW) mode. f_{offset} = 1 MHz.
TX phase noise @ 10 MHz, RF range 1	$N_{\varphi\_10M\_RF1}$	–	-121	–	dBc/Hz	Valid for 76 ≤ f_{RF} ≤ 77 GHz. Continuous wave (CW) mode. f_{offset} = 10 MHz.
TX phase noise @ 10 MHz, RF range 2	$N_{\varphi\_10M\_RF2}$	–	-120	–	dBc/Hz	Valid for 77 GHz < f_{RF} ≤ 81 GHz. Continuous wave (CW) mode. f_{offset} = 10 MHz.
Receiver						
Total RX SSB noise figure @ 10 MHz (TX OFF) for ultra low noise operation mode, RF range 1	$N_{SSB\_NB\_10M\_1\_1}$	–	10	–	dB	Valid for 76 ≤ f_{RF} ≤ 77 GHz. No blocker. All TX turned off. RX gain step G_{step}: +3 dB. f_{cutoff_AHP}: 300 kHz.
Total RX SSB noise figure @ 10 MHz (TX OFF) for ultra low noise operation mode, RF range 2	$N_{SSB\_NB\_10M\_1\_2}$	–	10.8	–	dB	Valid for 77 < f_{RF} ≤ 81 GHz. No blocker. All TX turned off. RX gain step G_{step}: +3 dB. f_{cutoff_AHP}: 300 kHz.
RX input P1dB, stop band	P_{1dB_SB}	-2.5	–	–	dBm	RX gain step G_{step}: -18 dB. f_{cutoff_AHP}: 300 kHz. IF tone frequency: 300 kHz × 0.05.

(table continues...)

Table 2 (continued) Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Nominal RX conversion gain for ultra low noise operation mode	G_{nom_ULN}	–	44.5	–	dB FS/mW	Unit is given in dB (FS/mW) (FS .. ADC Full Scale). Valid from the RX RF reference plane to CSI-2 output. RX gain step G_{step}: +3 dB. f_{cutoff_AHP}: 300 kHz. IF tone frequency: 2.0 MHz. Valid for source impedance mismatch better -15 dB.
Nominal RX conversion gain for low noise operation mode	G_{nom_LN}	–	41.5	–	dB FS/mW	Unit is given in dB (FS/mW) (FS .. ADC Full Scale). Valid from the RX RF reference plane to CSI-2 output. RX gain step G_{step}: 0 dB. f_{cutoff_AHP}: 300 kHz. IF tone frequency: 2.0 MHz. Valid for source impedance mismatch better -15 dB.
PLL						
TX settling time	t_{TX_set}	–	–	1.5	µs	Time from begin of chirp (t_{ref} = 0) until ramp linearity requirement (deviation from ideal ramp) is met.
Flyback time to reach start frequency of following chirp	$t_{flyback}$	–	–	1	µs	Time until frequency meets start frequency within ±500 kHz starting from chirp end frequency with 4 GHz frequency step.
Measurement ramp slope	$\lvert S_{ramp} \rvert$	3	–	200	MHz/µs	Valid for up- and down-ramp. Parameter ideal ramp deviation error need to be fulfilled.

4 Package outline

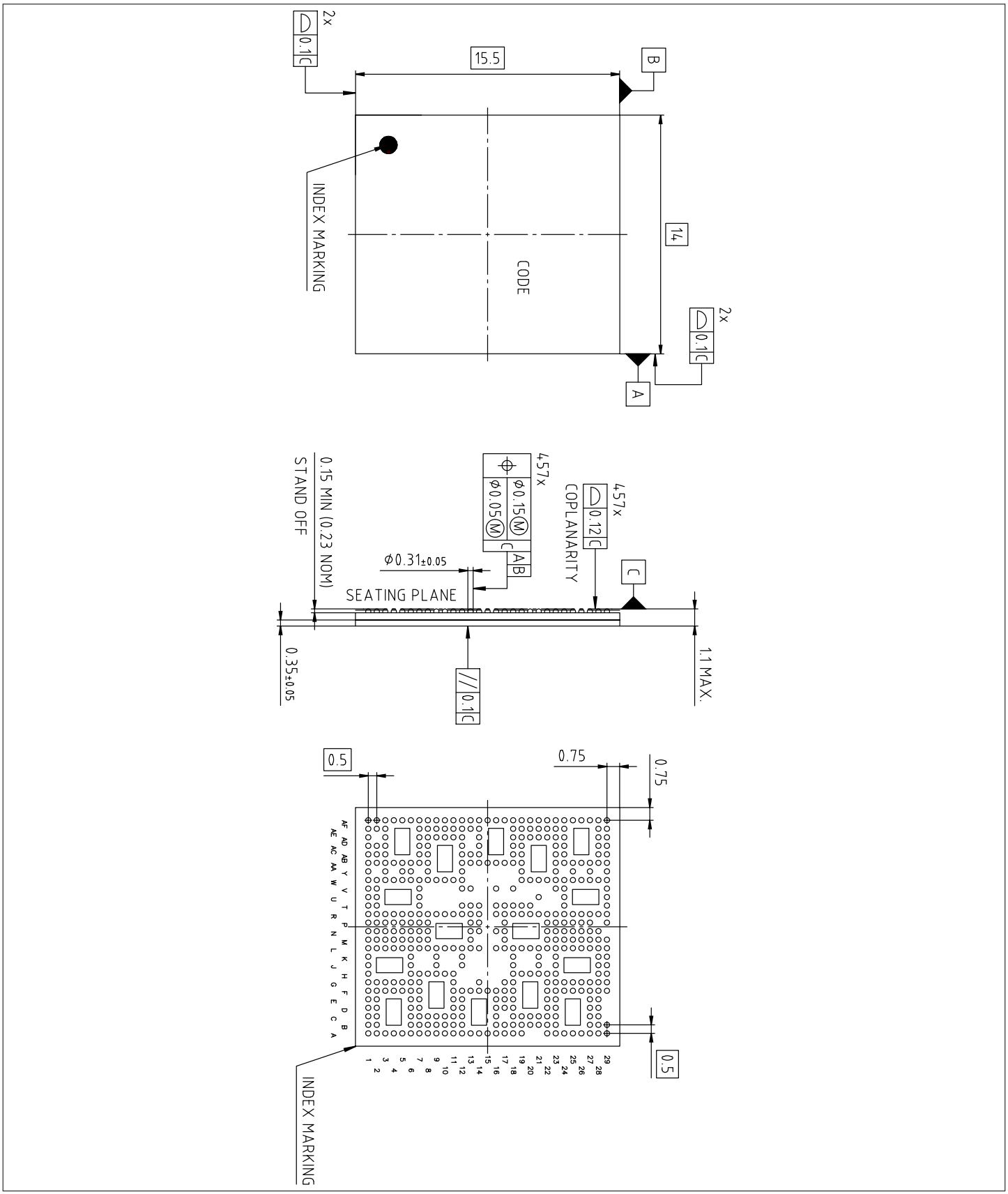


Figure 4 Drawing of FCBGA package; dimensions in mm

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