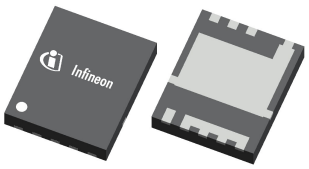
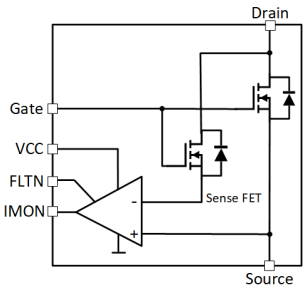
Power-transistor with integrated current sensor, 40 V





Features

- Bi-directional, loss-less, high-accuracy current sensing with 15 µA/A
- Very low on-resistance, $R_{DS(on)}$
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Overcurrent and overtemperature fault detection
- Dedicated fault-reporting pin
- Pb-free lead plating; RoHS-compliant
- Halogen-free according to IEC61249-2-21
- Rated for 150°C

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	0.9	mΩ
I_D	287	A
Q_{oss}	87	nC
Q_G(0V...10V)	79	nC
Current-sense gain	15	µA/A
Current-sense range (max.)	±220	A
Current-sense accuracy	±3	%
OCP level	160	A
OTP level	145	°C

Potential applications

- Low-voltage motor drive applications
- Battery-powered applications
- 3-phase BLDC and PMSM motor drives
- Power tools and gardening tools
- E-bikes, robotics, RC toys, drones, and multi-copters
- Pumps and fans

Product	Package	Body size	Features
CSF04ISCH90LT1	PG-TISON-9-1	5 mm × 6 mm	L-160 A OCP threshold, T-OTP enabled
CSF04ISCH90XT1	PG-TISON-9-1	5 mm × 6 mm	X-OCP disabled, T-OTP enabled

Product validation

Fully qualified according to JEDEC for industrial applications.

Description

A current-sense FET (CSFET) adds accurate and fast real-time sensing to a power MOSFET in a single package. The loss-less current sensing enables total system-loss reduction compared to discrete implementations, reduces the external component count, and shrinks the system footprint. The CSFET provides a high current-measurement accuracy with an error of less than ± 3% over a current range of 10% to 120% of the nominal current and detects overcurrent fault when the threshold is exceeded. The current-source output allows easy customization of the voltage range via an external resistor divider which is tied to the system's reference voltage. The device also has a built-in temperature sensor which detects overtemperature fault when the maximum junction temperature is exceeded. The main MOSFET is rated for 40 V and has an $R_{DS(on)}$ of less than 0.9 mΩ.

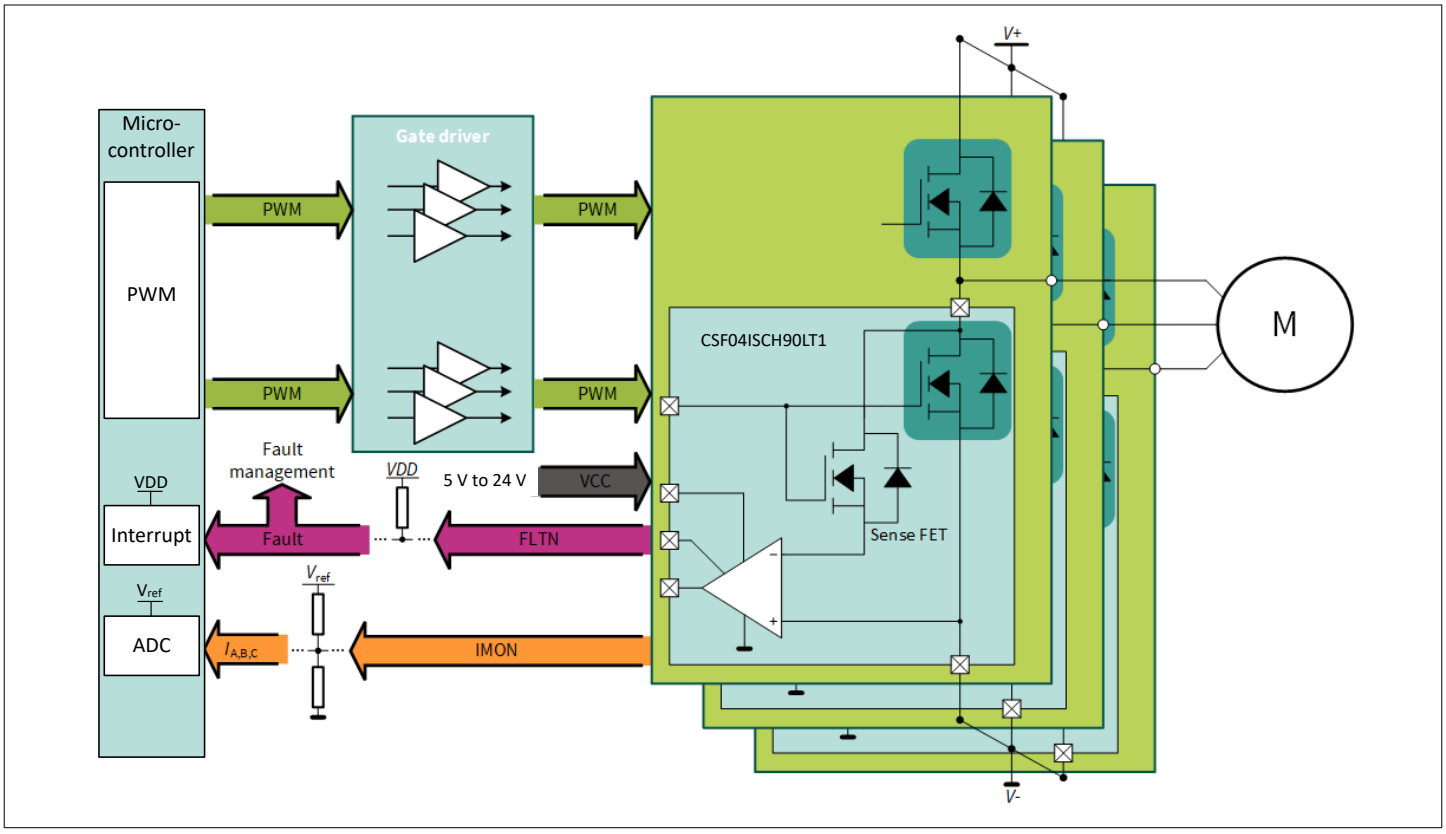


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1 Pin configuration and functions

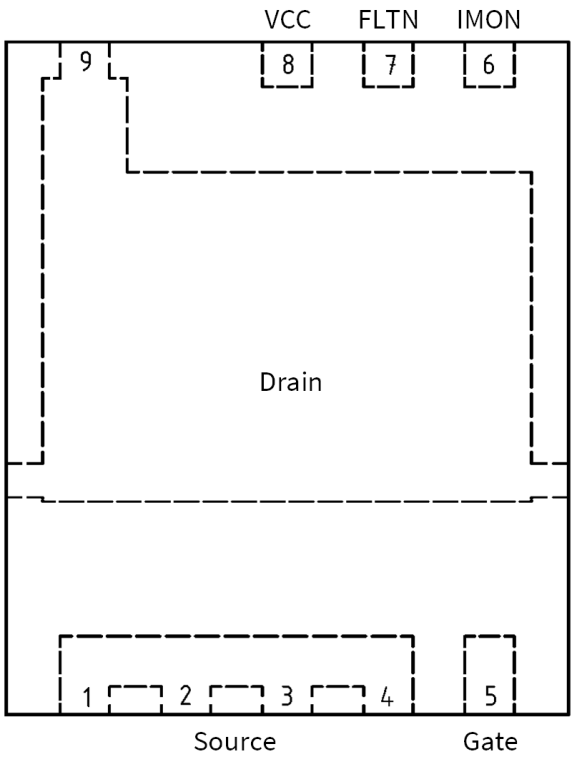


Figure 3 Pinout

Table 3 Pin description

Pin	Symbol	Function
1,2,3,4	Source	MOSFET source pins
5	Gate	MOSFET gate pin
6	IMON	Current-sense output
7	FLTN	Open-drain active-low fault output
8	VCC	Power supply for current sense
9	Drain	MOSFET drain

2 Block diagram

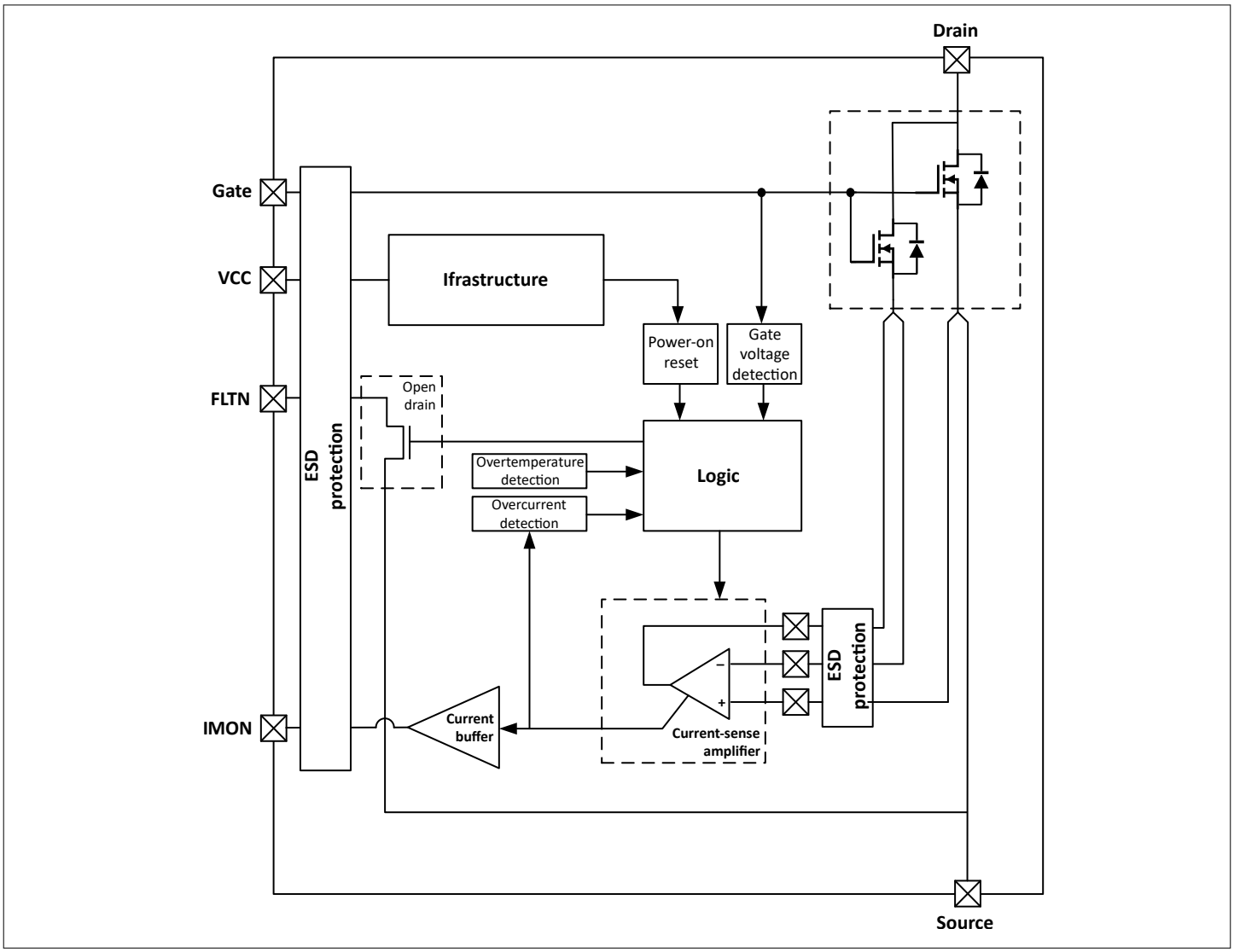


Figure 4 CSFET block diagram

3 Functional description

3.1 Fault handling and diagnostics

The device has integrated fault-handling and diagnostic features covering overcurrent protection (OCP), overtemperature protection (OTP) and V_{CC} undervoltage protection (UVLO). Faults are reported on the FLTN pin, and the signal is typically consumed by a microcontroller. The FLTN pin is an open-drain output, and an external pull-up resistor must be placed. When faults are present, the FLTN pin is pulled to the source of the device, meaning the FLTN signal goes low. 1

3.1.1 Overcurrent detection

The device contains an internal comparator to detect overcurrent events. This comparator includes a deglitch filter to eliminate spurious overcurrent events. The current measurement and overcurrent detection are only active when the gate of the device is on. If the current $|I_D|$ exceeds the threshold I_{D_OC} for longer than the deglitch time $t_{OC_FLT_deglitch}$, an overcurrent fault is detected and the FLTN pin is pulled to source to report the fault. The FLTN pin remains pulled to source until t_{FLT_extend} has expired. If no other faults are present, the FLTN pin then switches to an high-impedance state and is pulled high through the external resistor. If any faults other than overcurrent are already present, the FLTN pin continues to be pulled to source for the duration of that fault. If $|I_D|$, exceeds I_{D_OC} for less than $t_{OC_FLT_deglitch}$, it is considered a glitch, in which case the FLTN pin remains in a high-impedance state and is pulled high by the external resistor.

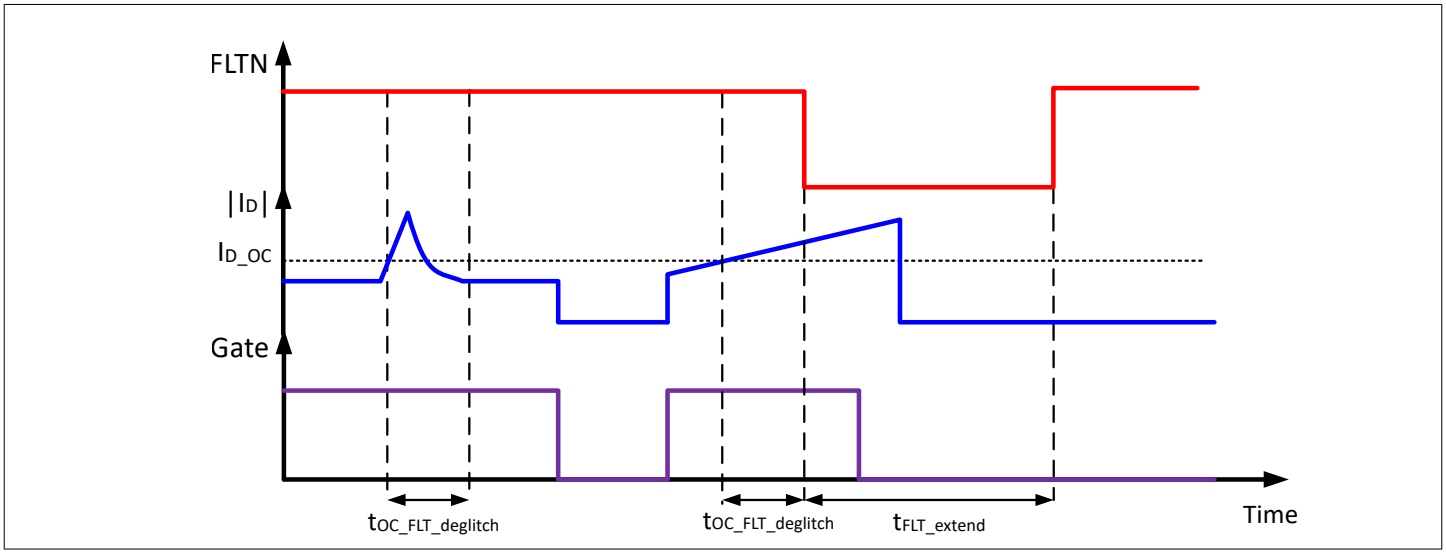


Figure 5 Overcurrent detection and reporting

3.1.2 Overtemperature detection

The device contains an internal temperature monitor, with the temperature sensor embedded in the current-sense IC. If the IC temperature T_{IC} exceeds the threshold T_{OT} for more than the deglitch time, $T_{OT_FLT_deglitch}$, an overtemperature fault is detected and the FLTN pin is pulled to source. If the duration of the overtemperature event is less than $T_{OT_FLT_deglitch}$, it is considered a glitch, in which case the FLTN pin remains in a high-impedance state and is pulled high by the external resistor. An overtemperature fault is cleared when the temperature T_{IC} drops below the threshold minus the hysteresis $T_{OT} - T_{OT_HYS}$, and the deglitch time $T_{OT_FLT_deglitch}$ has expired. Once the fault is cleared, the FLTN pin switches to a high-impedance state and is pulled high by the external resistor.

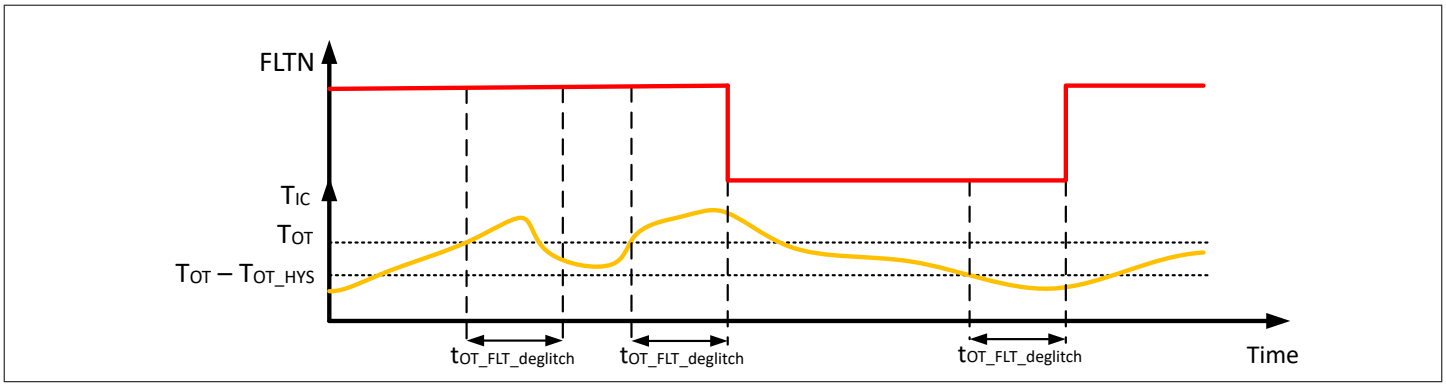


Figure 6 Overtemperature detection and reporting

3.1.3 Undervoltage detection (UVLO)

The device contains a linear regulator on the VCC pin to power the internal circuitry. An undervoltage lockout (UVLO) is provided to avoid undefined behavior due to low-voltage situations. The amplifier turns on as soon as the V_{CC} supply crosses the UVLO rising threshold VTH_{VCC_R}, and is ready to report the current on IMON after the start-up time t_{START} has expired. During start-up, the FLTN pin is pulled to the source of the device but enters a high-impedance state upon successful completion of a start-up sequence. The only way to turn off the amplifier is when V_{CC} drops below $VTH_{VCC_R} - V_{HYS_VCC}$ for more than t_{UVLO}. When the amplifier is off, the FLTN pin is pulled to the source of the device. The device restarts according to the normal start-up sequence once V_{CC} crosses the UVLO threshold and the FLTN pin enters high impedance, indicating no fault, after t_{START} has expired. If the start-up sequence is not successful, the FLTN pin is latched low as long as voltage is applied to V_{CC}. This condition may be cleared by a power cycle if there is no permanent damage to the amplifier. If the internal supplies do not generate the intended voltage levels, it can compromise the current-sense accuracy, and hence the FLTN pin is pulled low to indicate such a situation. The FLTN pin goes back to high impedance state as soon as the internal supplies generate the intended voltage levels.

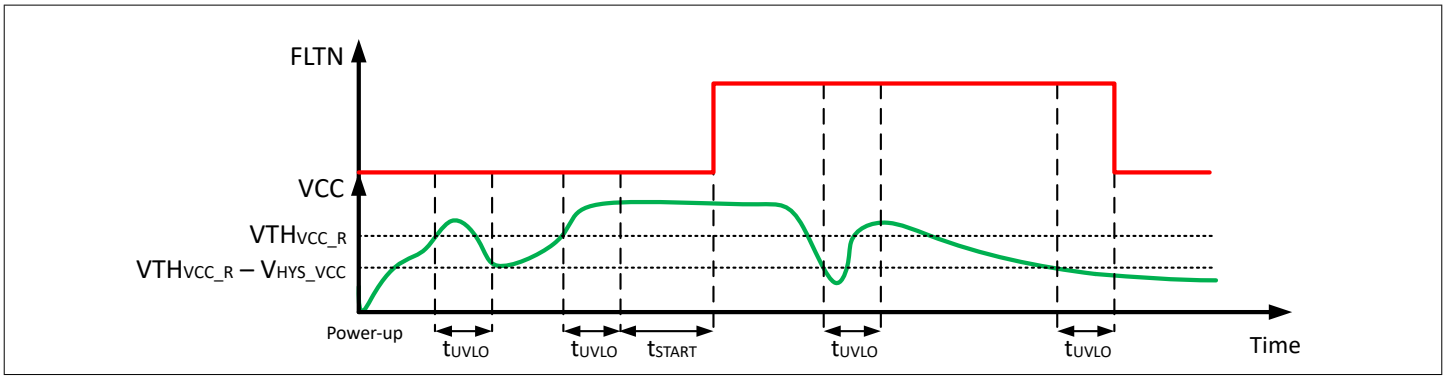


Figure 7 Undervoltage detection and reporting

3.1.4 Fault pin summary table

The FLTN pin functions are summarized in Table 4.

Table 4 FLTN pin functions

Operating conditions	V_{CC}	Gate	T_{IC}	I_D	FLTN pin
Normal operation	$V_{CC} > VTH_{VCC_R}$ and t_{START} has expired	Don't care	$T_{IC} < T_{OT}$	Don't care	High impedance

(table continues...)

Table 4 (continued) FLTN pin functions

Operating conditions	V_{CC}	Gate	T_{IC}	I_D	FLTN pin
V_{CC} undervoltage after entering normal operation	$V_{CC} < VTH_{VCC_R} - V_{HYS_VCC}$	Don't care	Don't care	Don't care	Pulled to source
V_{CC} undervoltage after power-up	$V_{CC} < VTH_{VCC_R}$ and t_{START} has expired	Don't care	Don't care	Don't care	Pulled to source
Overtemperature	$V_{CC} > VTH_{VCC_R}$ and t_{START} has expired	Don't care	$T_{IC} > T_{OT}$ and $t_{OT_FLT_degltich}$ has expired Until $T_{IC} < T_{OT} - T_{OT_HYS}$ and $t_{OT_FLT_degltich}$ has expired	$\lvert I_D \rvert < I_{D_OC}$	Pulled to source
Overcurrent	$V_{CC} > VTH_{VCC_R}$ and t_{START} has expired	On	$T_{IC} \leq T_{OT}$	$\lvert I_D \rvert > I_{D_OC}$ and $t_{OT_FLT_degltich}$ has expired Until $\lvert I_D \rvert < I_{D_OC}$ and t_{FLT_extend} has expired	Pulled to source

3.2 FLTN interface for a port pin

The FLTN pin utilizes an open-drain architecture, requiring a pull-up resistor R_{FLTN_PU} as shown in Figure 8. This pull-up resistor must be supplied by the same voltage rail as the microcontroller's I/O $V_{I/O}$. When a fault is active, the FLTN pin is pulled to the source of the device, causing the FLTN signal to go low. If the power device continues to switch high currents while the FLTN pin is asserted (for example during the time from fault assertion to system shutdown), voltage spikes may be observed on the FLTN signal. The amplitude and width of these spikes are highly dependent on the PCB layout and device operation. To prevent stressing the microcontroller's GPIO port, it is recommended to implement a clamp-and-filter circuit between the CSFET and the microcontroller, as shown in Figure 8. To clamp negative spikes on the FLTN signal, a Schottky diode (D) should be placed between the FLTN pin and the source of the device. This diode ensures that the FLTN signal cannot drop below DGND minus the forward voltage of the diode. To attenuate positive spikes on the FLTN signal, a filter consisting of R_{FLTN} and C_{FLTN} should be placed on the FLTN pin and connected to the ground used by the microcontroller's GPIO port (DGND). The filter's attenuation must be sufficient to prevent spurious fault assertions. Consult the microcontroller's GPIO port specifications and size D, R_{FLTN}, and C_{FLTN} accordingly to ensure that the GPIO port's maximum ratings are not exceeded. Note that adding a filter to the FLTN signal introduces delay to the FLTN signal chain, which can affect the overall FLTN response time of the system.

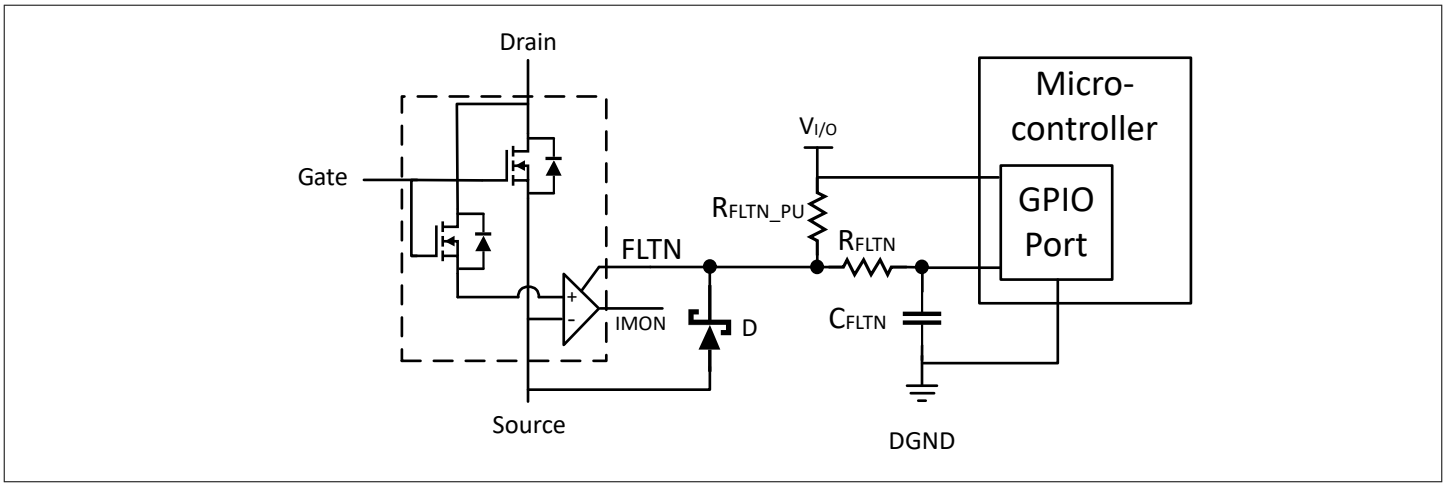


Figure 8 Interfacing the FLTN signal to a microcontroller's port pin

3.3 IMON interface for an ADC

The device features an accurate current-mirror architecture, which outputs the real-time current information on the IMON pin. The IMON output is a current source with a gain of A_{CS}. The IMON current-sense signal is translated into a voltage and level-shifted for the ADC, using an external resistive divider as shown in Figure 9. For a ratiometric measurement, the pull-up voltage for the resistive divider should be the reference for the microcontroller's ADC, V_{REF}. For the optimal signal-to-noise ratio, the ground for the resistive divider, AGND, should be shared with the ADC as well. The resistor values R_{IMON_H} and R_{IMON_L} should be selected to provide a symmetrical swing, meaning R_{IMON_H} = R_{IMON_L} = R_{IMON} with 0 A load current represented as the voltage center point of the resistive divider $V_{REF}/2$. The sizes of R_{IMON_H} and R_{IMON_L} determine the scaling of V_{IMON}. Larger resistors produce a higher voltage swing (lower dynamic range) for a given current range. Likewise, smaller resistors produce a lower voltage swing (higher dynamic range) for the same current range. Through selection of R_{IMON_H} and R_{IMON_L}, it must be ensured, that the minimum and maximum voltages of V_{IMON} are never violated. Below the minimum voltage on V_{IMON} and above the maximum voltage, the amplifier continues to report I_{MON}, but saturation effects reduce the measurement accuracy significantly.

A current-source signal tends to have better immunity from noise and EMI than a voltage-source signal. For best performance, it is recommended to keep the IMON PCB trace as a current signal all the way to the ADC of the micro-controller. This is implemented by placing the resistive divider physically close to the ADC. To decouple the ADC's sample-hold circuit, a capacitor, $C_{S/H}$, should be placed close to the ADC and across R_{IMON_L}. The size of the capacitor must be sufficient to decouple the ADC's sample-hold capacitor of the ADC. Consult the specification of the ADC and select an appropriate size for $C_{S/H}$. Note that placing a capacitor on the IMON signal can affect the settling time and stability of the amplifier.

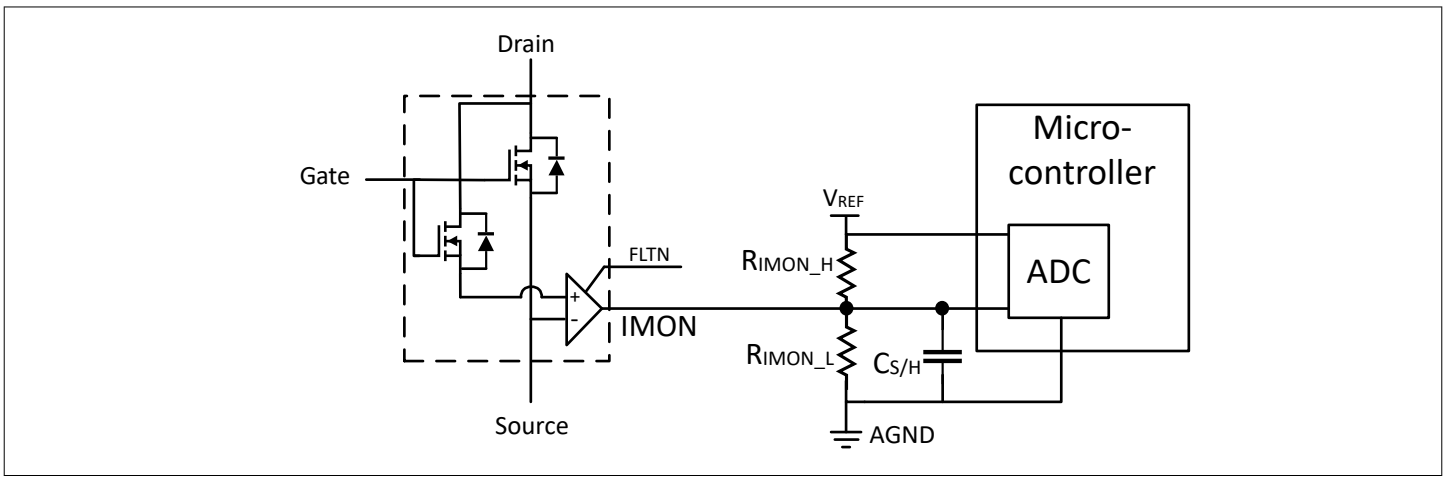


Figure 9 Interfacing the IMON signal to a microcontroller's ADC

3.4 VIMON scaling and dynamic range

Table 5 shows the relationship between the direction of system level currents and sensing signals. Positive load current I_{LOAD}, is defined to flow into the motor winding. With a positive I_{LOAD} the current of the low-side CSFET is negative, meaning that the current flows from the source to the drain. A positive I_{LOAD} results in a positive I_{MON}, meaning that the current flows out of the I_{MON} pin and represented as $V_{IMON} > V_{REF}/2$. Similar, a negative I_{LOAD} results in a negative I_{MON}, meaning that the current flows into the IMON pin and represented as a voltage $< V_{REF}/2$. $I_{LOAD} = 0$ A is represented as as the center-point voltage $V_{IMON} = V_{REF}/2$.

Table 5 Current directions and sensing signals

I_{LOAD}	Motor winding current	CSFET current	IMON current	V_{IMON} voltage
Positive	Positive (flowing into winding)	Negative (flowing from source to drain)	Positive (out of IMON pin)	$> V_{REF}/2$
Negative	Negative (flowing out of winding)	Positive (flowing from drain to source)	Negative (into IMON pin)	$< V_{REF}/2$

The relationship between I_{MON} and V_{IMON} is shown in Figure 10. As an example, assume a positive load current $I_{LOAD,pos}$ flowing into the motor. The CSFET represents the load current as $I_{MON,pos}$ by scaling $I_{LOAD,pos}$ by A_{CS}. $I_{MON,pos}$ is translated into a voltage $V_{IMON,pos}$ through a resistive divider with the equivalent resistance of $R_{PAR,nom}$. The resistive value of R_{PAR} sets the gain of V_{IMON}. A lower resistance, $R_{PAR,low}$, increases the dynamic range, and a higher resistance, $R_{PAR,high}$, decreases the dynamic range.

When selecting resistance values for the resistive divider, ensure that the maximum current to be measured does not bring V_{IMON} beyond $V_{IMON,max}$. Likewise, ensure that the minimum current to be measured does not bring V_{IMON} below $V_{IMON,min}$.

In Figure 10, the precision sense range is shown as the blue part of the A_{CS} line. To avoid saturating the current-sense amplifier, any sensed current must result in a V_{IMON} that satisfies $V_{IMON,min} < V_{IMON} < V_{IMON,max}$ (the blue rectangle in the upper left quadrant). If V_{IMON} falls outside the precision sense range, lower sensing accuracy must be expected.

The device offers extended low sense range below 10% of I_{NOM} (absolute value), which is indicated by the yellow areas in the graphic. As the load current approaches 0 A, uncalibrated offsets and nonlinearities become more dominant, and the highest sensing accuracy cannot be maintained. Currents from 120% of I_{NOM} to the OCP threshold (absolute value) fall in the extended high sense range, which is shown in green in Figure 10. In this range, saturation effects of the amplifier start to affect accuracy because V_{IMON} approaches $V_{IMON,max}$ or $V_{IMON,min}$. For precision sensing accuracy beyond 120% I_{NOM} or if sensing beyond the OCP limit is required, the resistors of the I_{MON} divider can be redesigned. A lower resistance (higher dynamic range) brings the V_{IMON} voltage back into the precision sense range (blue rectangle in the lower left quadrant). When extending the sensing range, be careful to never exceed the maximum sink and source capabilities of I_{MON}, indicated as $I_{MON,max}$ and $I_{MON,min}$ in Figure 10.

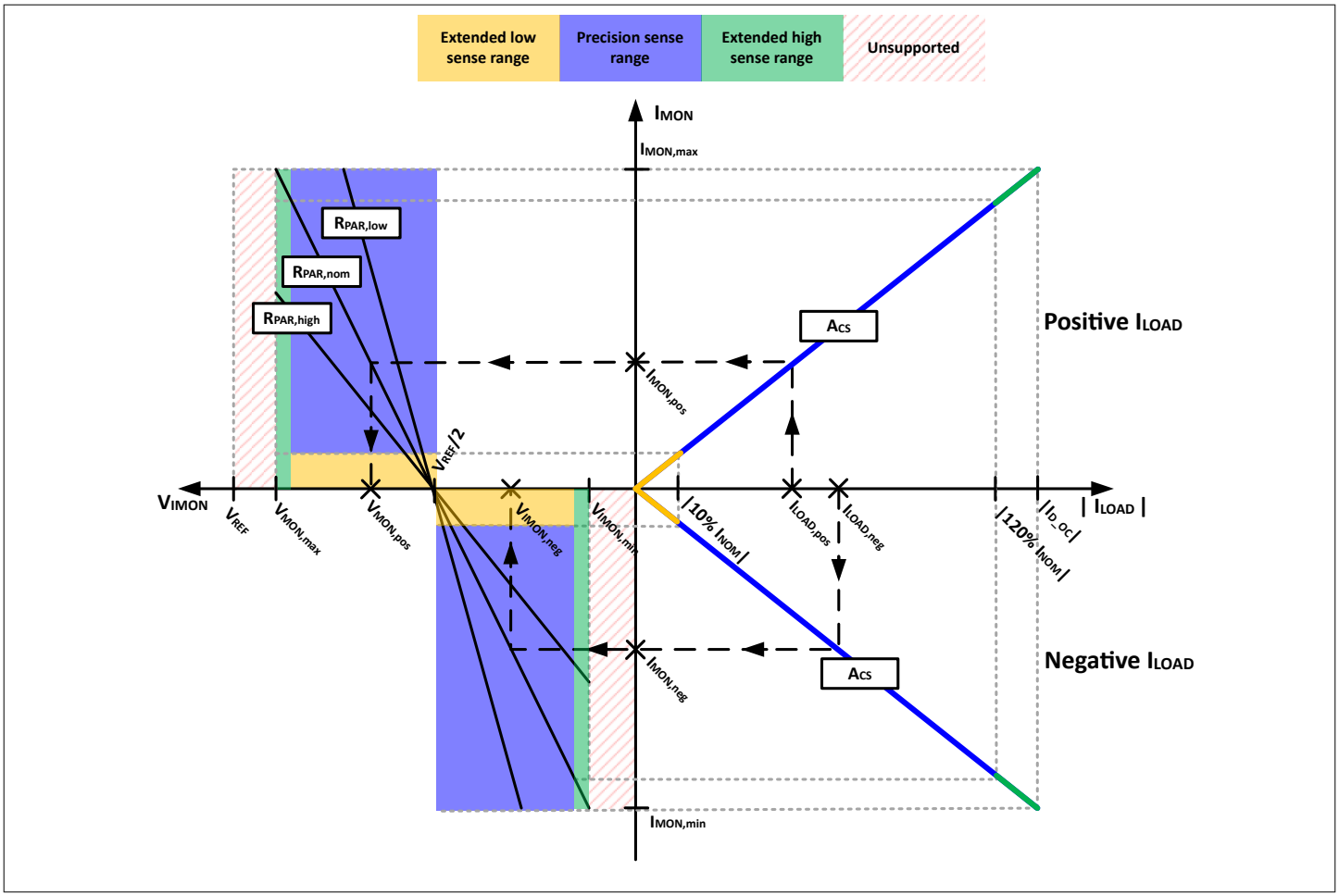


Figure 10 Translation of I_{MON} into a voltage signal, V_{IMON}

Table 6 Legend

Parameter	Description
A_{CS}	Current-sense gain.
I_{LOAD}	Load current. Currents flowing into the motor winding are defined as positive (source-to-drain of low-side FET).
I_{NOM}	Nominal load current.
I_{D_OC}	Overcurrent protection threshold.
I_{MON}	Sensed current on the IMON pin.
$I_{MON,min}$	Maximum current that can be sinked by the IMON pin.
$I_{MON,max}$	Maximum current that can be sourced by the IMON pin.
$R_{PAR,low}$, $R_{PAR,nom}$, $R_{PAR,high}$	Equivalent parallel resistance of resistor divider on IMON pin. The low resistance value results in a high dynamic range, the nominal value in a nominal dynamic range, and the high value in a low dynamic range.. $R_{PAR,low} < R_{PAR,nom} < R_{PAR,high}$.
V_{IMON}	Voltage on the IMON pin.

(table continues...)

Table 6 (continued) Legend

Parameter	Description
$V_{IMON,min}$	Minimum acceptable voltage on the IMON pin.
$V_{IMON,max}$	Maximum acceptable voltage on the IMON pin.
V_{ref}	Pull-up voltage for resistor divider on the IMON pin. Typically 3.3 V.
$I_{LOAD,neg}$	Example current where I_{LOAD} < 0 A.
$I_{LOAD,pos}$	Example current where I_{LOAD} > 0 A.
$I_{MON,neg}$	IMON current corresponding to $I_{LOAD,neg}$.
$I_{MON,pos}$	IMON current corresponding to $I_{LOAD,pos}$.
$V_{IMON,neg}$	Voltage on IMON pin corresponding to $I_{LOAD,neg}$.
$V_{IMON,pos}$	Voltage on IMON pin corresponding to $I_{LOAD,pos}$.

3.4.1 VIMON scaling example

I_{MON} is a current output that generates a voltage swing on the center tap of the resistor divider as shown in Figure 9. The resistor divider design depends on the amplitude of the current to measure, the level of the supply for the resistive divider, and the V_{IMON} operating voltage range. To ensure that measurement accuracy is maintained across the measurement range, the resistor values need to be selected such that the voltage swing created on the IMON pin, in response to the measured current, does not exceed the V_{IMON} operating range. For a symmetrical voltage swing on the center tap of the resistor divider, the resistors must be of the same size:

$$R_{IMON_H} = R_{IMON_L} = R_{IMON} \tag{1}$$

The equivalent resistance of the voltage divider is the parallel connection of the resistors:

$$R_{PAR} = R_{IMON} \times R_{IMON} / (R_{IMON} + R_{IMON}) \tag{2}$$

$$R_{PAR} = 0.5 \times R_{IMON} \tag{3}$$

The current that is sinked or sourced on the IMON pin is related to the load current I_{LOAD} through the sense gain, A_{CS}:

$$I_{MON} = I_{LOAD} \times A_{CS} \tag{4}$$

The voltage on the IMON pin V_{IMON} is:

$$V_{IMON} = R_{PAR} \times I_{MON} + 0.5 \times V_{REF} \tag{5}$$

Replacing the I_{MON} and R_{PAR} values in the above equation:

$$V_{IMON} = 0.5 \times R_{IMON} \times I_{LOAD} \times A_{CS} + 0.5 \times V_{REF} \tag{6}$$

Based on this, R_{IMON} is expressed as a function of V_{IMON} and I_{LOAD} :

$$R_{IMON} = (2 \times V_{IMON} - V_{REF})/(I_{LOAD} \times A_{CS}) \quad (7)$$

As an example, assume a system where the maximum load current to be measured is I_{LOAD} = ±160 A. To maintain accuracy across the range, the voltage swing on the IMON pin must fall within the range 0.4 V < V_{IMON} < 2.9 V. In this example, I_{LOAD} = 160 A should map to V_{IMON} = 2.9 V, and I_{LOAD} = –160 A should map to V_{IMON} = 0.4 V. Assume the reference voltage for the ADC and the pull-up voltage for the resistive divider, V_{REF}, is 3.3 V, and that the current sense gain A_{CS} is 15 µA/A. At I_{LOAD} = 160 A, R_{IMON} is calculated as:

$$\begin{aligned} R_{IMON} &= (2 \times V_{IMON} - V_{REF})/(I_{LOAD} \times A_{CS}) \\ R_{IMON} &= (2 \times 2.9V - 3.3V)/(160A \times 15\mu A/A) \\ R_{IMON} &= 1042\Omega \end{aligned} \quad (8)$$

The voltage swing is symmetrical, so a similar result is found at I_{LOAD} = –160 A:

$$\begin{aligned} R_{IMON} &= (2 \times 2.9V - 3.3V)/(-160A \times 15\mu A/A) \\ R_{IMON} &= 1042\Omega \end{aligned} \quad (9)$$

To avoid exceeding the V_{IMON} range, the R_{IMON} resistance value should be rounded down to the next standard size. For this example, R_{IMON} = 1 kΩ is the recommended size and the equivalent parallel resistance of the resistive divider is R_{PAR} = 500 Ω.
With R_{IMON} = 1 kΩ and an example I_{LOAD} = 50 A , I_{MON} is calculated using equation 4:

$$\begin{aligned} I_{MON} &= 50A \times 15\mu A/A \\ I_{MON} &= 0.75mA \end{aligned} \quad (10)$$

V_{IMON} is calculated using equation 5 :

$$\begin{aligned} V_{IMON} &= 0.5 \times 1k\Omega \times 50A \times 15\mu A/A + 0.5 \times 3.3V \\ V_{IMON} &= 2.025V \end{aligned} \quad (11)$$

Similarly, with R_{IMON} = 1 kΩ and I_{LOAD} = –60 A the resulting I_{MON} is:

$$\begin{aligned} I_{MON} &= -60A \times 15\mu A/A \\ I_{MON} &= -0.9mA \end{aligned} \quad (12)$$

And, V_{IMON} is calculated using the Equation :

$$\begin{aligned} V_{IMON} &= 0.5 \times 1k\Omega \times -60A \times 15\mu A/A + 0.5 \times 3.3V \\ V_{IMON} &= 1.2V \end{aligned} \quad (13)$$

The example used here is illustrated in Figure 11.

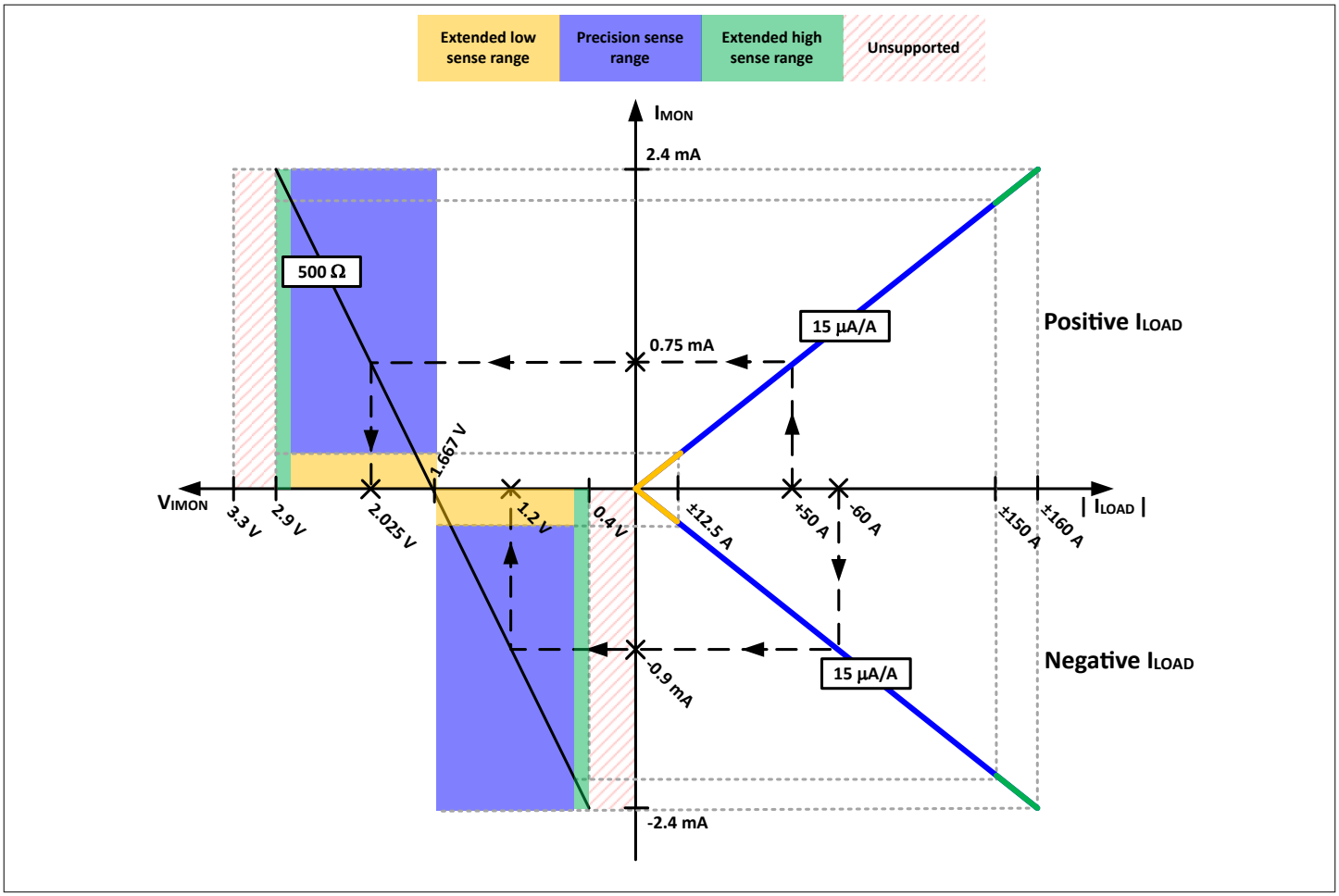


Figure 11 Scaling example with R_{IMON} = 1 kΩ

3.5 Power supply

The device only requires a single external supply, V_{CC}, to operate. From V_{CC}, the device generates all internal power supply rails for the current-sense IC. Current consumption on the supply pin I_{CC} depends on:

- The drain current level
- The state (on or off) of the gate of the device

V_{CC} supplies the internal IC, including the current sinked or sourced by the IMON pin. This makes I_{CC} dependent on the on the drain current level. IMON is only valid when the gate is on, which makes I_{CC} dependent on the state of the gate of the device. With the pulsating nature of I_{CC}, two decoupling capacitors of 1 µF and 100 nF, respectively, must be placed close to the device as shown in Figure 12. The device supports a V_{CC} voltage range from 5 V to 24 V. In systems with a DC bus voltage not exceeding 24 V, V_{CC} can be sourced directly from the DC bus. If the system has an auxiliary supply of 5 V or greater, that rail can be used to supply the CSFET. The supply current I_{CC} is independent of the voltage supplied on the V_{CC} pin. The power consumption of the device is minimized by supplying it with a voltage close to the minimum required. In applications where power consumption is less of a concern, a supply sourced directly from the DC bus can be an attractive low-cost option.

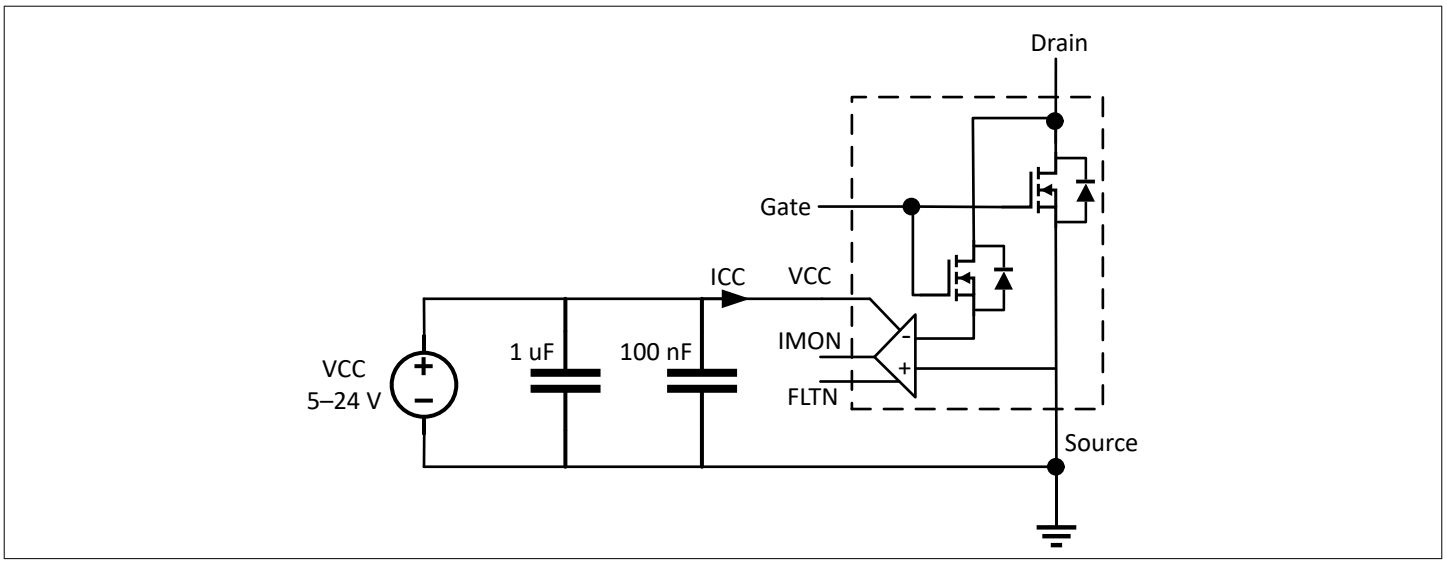


Figure 12 V_{CC} supply and decoupling

3.6 Operating devices in parallel

CSFET devices can be operated in parallel to support higher currents. The I_{MON} signals are current-source outputs and can be shorted to represent the sum of the current through the parallel devices. The summed I_{MON} signal is translated into a voltage, V_{IMON}, with a single resistive divider. Similar to the operations of a single device, the supported voltage range on V_{IMON} must be observed to maintain sensing accuracy. If the summed I_{MON} is double that of a single device, the R_{IMON} resistance should be halved to maintain the same voltage swing.

4 General product characteristics

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions. Exposure to conditions rated as absolute maximums for extended periods may affect device reliability.

4.1 Absolute maximum ratings

Table 7 Absolute maximum ratings

At T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
MOSFET						
Continuous drain current	I_D	–	–	287	A	V_{GS} = 10 V, T_C = 25°C [1]
Continuous drain current	I_D	–	–	182	A	V_{GS} = 10 V, T_C = 100°C [1]
Continuous drain current	I_D	–	–	41	A	V_{GS} = 10 V, T_A = 25°C, R_{thJA} = 50°C/W [2]
Pulsed drain current	$I_{D,pulse}$	–	–	1148	A	T_A = 25°C Pulsed drain current with 287 A < $I_{D,pulse}$ ≤ 350 A is allowed for an accumulated time of up to 50 seconds during the life of the device. Pulsed drain current with 350 A < $I_{D,pulse}$ ≤ 1148 A is allowed up to 20 times during the life of the device [3]
Avalanche energy, single pulse	E_{AS}	–	–	477	mJ	I_D = 50 A, R_{GS} = 25 Ω [4]
Gate-to-source voltage	V_{GS}	–3	–	20	V	
Power dissipation	P_{tot}	–	–	125	W	T_C = 25°C
Power dissipation	P_{tot}	–	–	2.5	W	T_A = 25°C, R_{thJA} = 50°C/W [2]
Amplifier						
Input supply voltage	V_{CC}	–0.3	–	27	V	Referenced to source.
IMON pin voltage	V_{IMON}	–0.3	–	3.6	V	Referenced to source.
FLTN pin voltage	V_{FLTN}	–0.3	–	6	V	Referenced to source.

(table continues...)

Table 7 (continued) Absolute maximum ratings

At T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Temperature						
Storage temperature	T_{stg}	–55	–	150	°C	
Operating temperature	T_J	–40	–	150	°C	Operation at junction temperatures from 150°C to 175°C is allowed for up to 10 ms.

1) The absolute maximum ratings apply only to the product itself. They are valid only if the product operates with a case temperature T_A as specified. For maximum ratings under other case temperatures, see the drain current diagram in Chapter 5 for detailed information. De-rating is required based on the actual environmental conditions.
2) Device on 40 mm × 40 mm × 1.5 mm epoxy PCB FR4 with 6 cm^2 copper area (one layer, 70 µm thick) for drain connection. PCB is in a vertical position in still air.
3) See the safe operating area diagram in Chapter 5 for detailed information.
4) See avalanche characteristics diagram in Chapter 5 for detailed information.

4.2 ESD ratings

Table 8 ESD Ratings

Symbol	Description	Value	Unit	Notes or conditions
HBM	Human Body Model sensitivity as per ANSI/ESDA/JEDEC JS-001	2000	V	For source, gate, IMON, FLTN, and drain (pins 1...4, 5, 6, 7, and 9)
HBM	Human Body Model sensitivity as per ANSI/ESDA/JEDEC JS-001	1500	V	For VCC (pin 8)
CDM	Charge Device Model sensitivity as per ANSI/ESDA/JEDEC JS-001	1000	V	For source, gate, IMON, FLTN, VCC and drain (pins 1...4, 5, 6, 7, 8, and 9)

4.3 Recommended operating conditions

Table 9 Recommended operating conditions

Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input supply voltage	V_{CC}	5	–	24	V	Referenced to source.

(table continues...)

Table 9 (continued) Recommended operating conditions

Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted).

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input supply voltage slew rate	$V_{CC,SLEW}$	–	–	1	V/µs	
Gate pin voltage	V_{GATE}	8	–	15	V	Referenced to source.
FLTN pin voltage range	V_{FLTN}	–0.3	–	5.5	V	Active low.

4.4 Thermal characteristics

Table 10 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance, junction–case, bottom	$R_{thJC(bot)}$	–	–	1	°C/W	
Thermal resistance, junction–case, top	$R_{thJC(top)}$	–	–	28.5	°C/W	
Thermal resistance, junction–ambient	R_{thJA}	–	–	50	°C/W	Device on PCB, 6 cm^2 cooling area.

4.5 Electrical characteristics

Table 11 MOSFET electrical characteristics

Condition: T_j = 25°C, unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Drain–source breakdown voltage	$V_{(BR)DSS}$	40	–	–	V	V_{GS} = 0 V, I_D = 1 mA
Gate threshold voltage	$V_{GS(th)}$	1.8	2.3	2.8	V	V_{DS} = V_{GS}, I_D = 890 µA

(table continues...)

Table 11 (continued) MOSFET electrical characteristics

Condition: T_j = 25°C, unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Nominal current	I_{NOM}	–	125	–	A	
Zero gate voltage drain current	I_{DSS}	–	0.1	1	µA	V_{DS} = 40 V, V_{GS} = 0 V, T_j=25°C
Zero gate voltage drain current	I_{DSS}	–	10	100	µA	V_{DS} = 40 V, V_{GS} = 0 V, T_j = 125°C
Gate–source leakage current	I_{GSS}	–	45	90	µA	V_{GS} = 15 V, V_{DS} = 0 V
Drain-source on–state resistance	$R_{DS(on)}$	–	–	0.9	mΩ	V_{GS} = 10 V, I_D = 50 A
Drain–source on-state resistance	$R_{DS(on)}$	–	–	1.05	mΩ	V_{GS} = 6 V, I_D = 50 A
Gate resistance	R_G	–	0.85	–	Ω	
Transconductance	g_{fs}	138	276	–	S	$\|V_{DS}\| \geq 2 \times \|I_D\| \times R_{DS(on),max}$, I_D = 50 A

Table 12 Current-sense amplifier electrical characteristics

Condition: T_j = 25°C, V_{in} = 18 V, R_{IMON} = 1 kΩ (equivalent to 500 Ω load on IMON), V_{GS} = 12 V, V_{CC} = 5 V, V_{REF} = 3.3 V, unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply and UVLO						
VCC UVLO rising threshold	VTH_{VCC_R}	–	–	4.5	V	
VCC UVLO hysteresis	V_{HYS_VCC}	–	350	500	mV	
VCC UVLO filtering time	t_{UVLO}	–	–	5	µs	
VCC quiescent current	$I_{CC,Q}$	–	7.3	–	mA	At gate off.
VCC current at no load	I_{CC}	–	9.2	–	mA	At gate on and I_{LOAD} = 0 A.

(table continues...)

Table 12 (continued) Current-sense amplifier electrical characteristics

Condition: T_j = 25°C, V_{in} = 18 V, R_{IMON} = 1 kΩ (equivalent to 500 Ω load on IMON), V_{GS} = 12 V, V_{CC} = 5 V, V_{REF} = 3.3 V, unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VCC current at maximum drian–source current	I_{CC}	–	12.4	–	mA	At gate on and 150 A flowing from drain to source.
VCC current at minimum drain–source current	I_{CC}	–	13.9	–	mA	At gate on and -150 A flowing from drain to source.
Start-up time	t_{START}	–	0.025	1	ms	VCC UVLO released.
IMON						
IMON voltage range	V_{IMON}	0.4	–	2.9	V	The accuracy is only achieved if the resistor divider and its supply are designed so as not to violate this voltage range. The resistor divider and its supply must be designed to represent the maximum continuous drain current. Short-term operation beyond voltage limits is allowed for up to 10ms per event.
IMON current range	I_{MON}	–3.4	–	3.4	mA	The sensing accuracy is only guaranteed for -2.4 mA ≤ IMON ≤ 2.4 mA
Current-sense gain	A_{CS}	–	15	–	µA/A	Current flow from drain to source will cause the measured current to flow into the IMON pin (sink). Current flow from source to drain will cause the measured current to flow out of the IMON pin (source).
Current-measurement accuracy	$\Delta I/I$	–12	–	12	%	$\lvert I_D \rvert$ = 3 A [1) 2) 3)]
Current-measurement accuracy	$\Delta I/I$	–5	–	5	%	6.25 A < $\lvert I_D \rvert$ ≤ 12.5 A [1) 2) 3)]
Current-measurement accuracy	$\Delta I/I$	–3	–	3	%	12.5 A < $\lvert I_D \rvert$ ≤ 150 A [1) 2) 3)]

(table continues...)

Table 12 (continued) Current-sense amplifier electrical characteristics

Condition: T_j = 25°C, V_{in} = 18 V, R_{IMON} = 1 kΩ (equivalent to 500 Ω load on IMON), V_{GS} = 12 V, V_{CC} = 5 V, V_{REF} = 3.3 V, unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Current-measurement accuracy	$\Delta I/I$	–10	–	10	%	150 A < $\lvert I_D \rvert$ ≤ 160 A 1) 2) 3) 4)
Output common-mode rejection ratio	$CMRR_{IMON}$	–	–	–60	dB	Reference voltage 0.5 V to 2.5 V. Up to 1 MHz frequency.
Output power supply rejection ratio	$\Delta I_{MON}/V_{CC}$	–	–	–166	dBA/V	V_{CC} = 20 V Up to 1 MHz frequency.
Amplifier						
Unity gain bandwidth	GBW	5	–	–	MHz	
Minimum gate on time	t_{PW}	100	–	–	ns	Full current accuracy is achieved after $t_{settling}$.
Settling time without capacitive load	$t_{settling}$	–	–	350	ns	Settling time of VIMON with a capacitive load of 0 pF.
Settling time with capacitive load	$t_{settling}$	–	–	1	us	Settling time of VIMON with a capacitive load of 270 pF.
FLTN						
FLTN pull-down resistance	R_{FLTN}	–	–	250	Ω	Pull-up resistance on this pin has to be more than 10 kΩ.
Overcurrent detection						
Overcurrent fault level	I_{D_OC}	145	160	176	A	
Overcurrent fault detection filter time	$t_{OC_FLT_deglitch}$	–	300	–	ns	
FLTN pin overcurrent fault duration	t_{FLT_extend}	–	350	–	µs	FLTN pin stays LOW for t_{FLT_extend} after the fault is detected.
Overtemperature detection						
Overtemperature fault detection threshold	T_{OT}	140	145	150	°C	

(table continues...)

Table 12 (continued) Current-sense amplifier electrical characteristics

Condition: T_j = 25°C, V_{in} = 18 V, R_{IMON} = 1 kΩ (equivalent to 500 Ω load on IMON), V_{GS} = 12 V, V_{CC} = 5 V, V_{REF} = 3.3 V, unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overtemperature detection hysteresis	T_{OT_HYS}	–	15	–	°C	
Overtemperature fault detection filter time	$t_{OT_FLT_deglitch}$	–	500	–	ns	

1) Current accuracy is specified at T_j = –40°C to 150°C and after $t_{settling}$ has passed.
2) Current accuracy is specified with R_{IMON} = 1 kΩ (equivalent to 500 Ω load on IMON).
3) Current-sense accuracy is specified at a gate voltage range of 8 V < V_{GS} < 15 V.
4) Operation above the overcurrent threshold is considered to be unsafe or lifetime-limiting. When overcurrents are detected in the system or on FLTN, the system must shut down the MOSFET.

Table 13 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	–	5506	–	pF	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz 1)
Output capacitance	C_{oss}	–	1779	–	pF	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz 1)
Reverse transfer capacitance	C_{rss}	–	35	–	pF	V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz 1)
Turn-on delay time	$t_{d(on)}$	–	15.1	–	ns	V_{DD} = 20 V, V_{GS} = 10 V, I_D = 50 A, $R_{G,ext}$ = 3 Ω
Rise time	t_r	–	4.0	–	ns	V_{DD} = 20 V, V_{GS} = 10 V, I_D = 50 A, $R_{G,ext}$ = 3 Ω
Turn-off delay time	$t_{D(off)}$	–	47.9	–	ns	V_{DD} = 20 V, V_{GS} = 10 V, I_D = 50 A, $R_{G,ext}$ = 3 Ω
Fall time	t_f	–	10.4	–	ns	V_{DD} = 20 V, V_{GS} = 10 V, I_D = 50 A, $R_{G,ext}$ = 3 Ω

1) Not subject to production test; specified by design.

Table 14 Gate-charge characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Gate-to-source charge	Q_{gs}	–	18.7	–	nC	V_{DD} = 20 V, I_D = 50 A, V_{GS} = 0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	–	12.7	–	nC	V_{DD} = 20 V, I_D = 50 A, V_{GS} = 0 to 10 V

(table continues...)

Table 14 (continued) Gate-charge characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Gate-to-drain charge	Q_{gd}	–	11	–	nC	V_{DD} = 20 V, I_D = 50 A, V_{GS} = 0 to 10 V [1]
Switching charge	Q_{sw}	–	17	–	nC	V_{DD} = 20 V, I_D = 50 A, V_{GS} = 0 to 10 V
Gate charge total	Q_g	–	79	–	nC	V_{DD} = 20 V, I_D = 50 A, V_{GS} = 0 to 10 V [1]
Gate plateau voltage	$V_{plateau}$	–	3.4	–	V	V_{DD} = 20 V, I_D = 50 A, V_{GS} = 0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	–	75	–	nC	V_{DS} = 0.1 V, V_{GS} = 0 to 10 V
Output charge	Q_{oss}	–	87	–	nC	V_{DD} = 20 V, V_{GS} = 0 V [1]

1) Not subject to production test; specified by design.

Table 15 Reverse diode

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	–	–	121	A	T_C = 25°C
Diode pulse current	$I_{S,pulse}$	–	–	1148	A	T_C = 25°C Pulsed diode current with 287 A < $I_{S,pulse}$ ≤ 350 A is allowed for an accumulated time of up to 50 seconds during the life of the device. Pulsed diode current with 350 A < $I_{S,pulse}$ ≤ 1148 A is allowed up to 20 times during the life of the device.
Diode forward voltage	V_{SD}	–	0.8	1.0	V	V_{GS} = 0 V, I_F = 50 A, T_j = 25°C
Reverse recovery time	t_{rr}	–	36.7	–	ns	V_R = 20 V, I_F = 25 A, di_F/dt = 400 A/µs [1]
Reverse recovery charge	Q_{rr}	–	157.2	–	nC	V_R = 20 V, I_F = 25 A, di_F/dt = 400 A/µs

1) Not subject to production test; specified by design.

5 MOSFET electrical characteristic diagrams

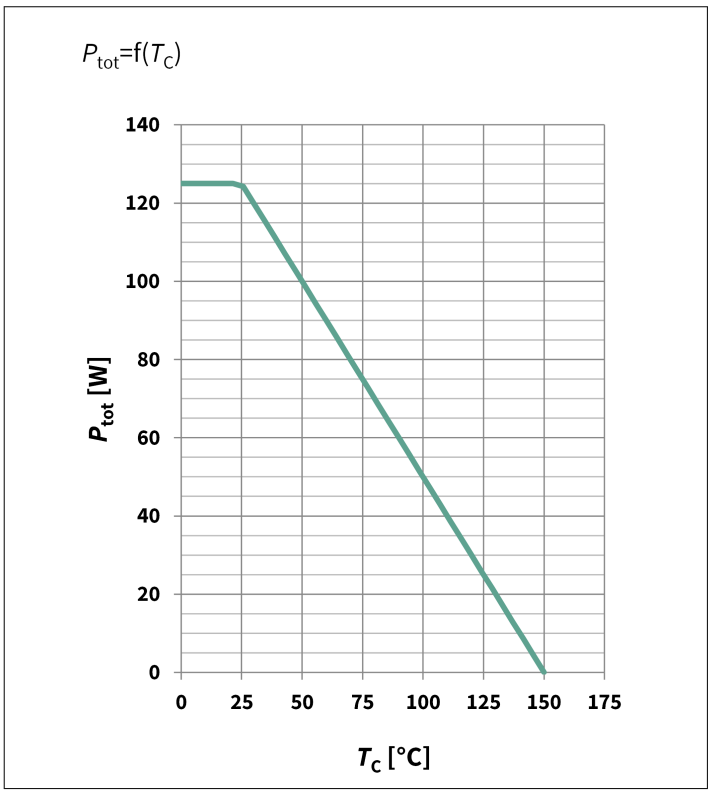


Figure 13 Power dissipation

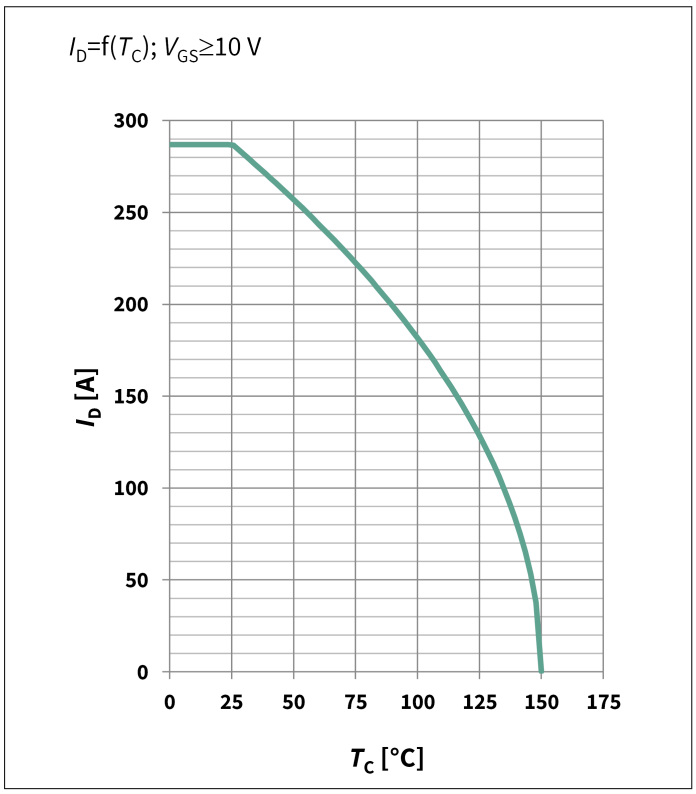


Figure 14 Drain current

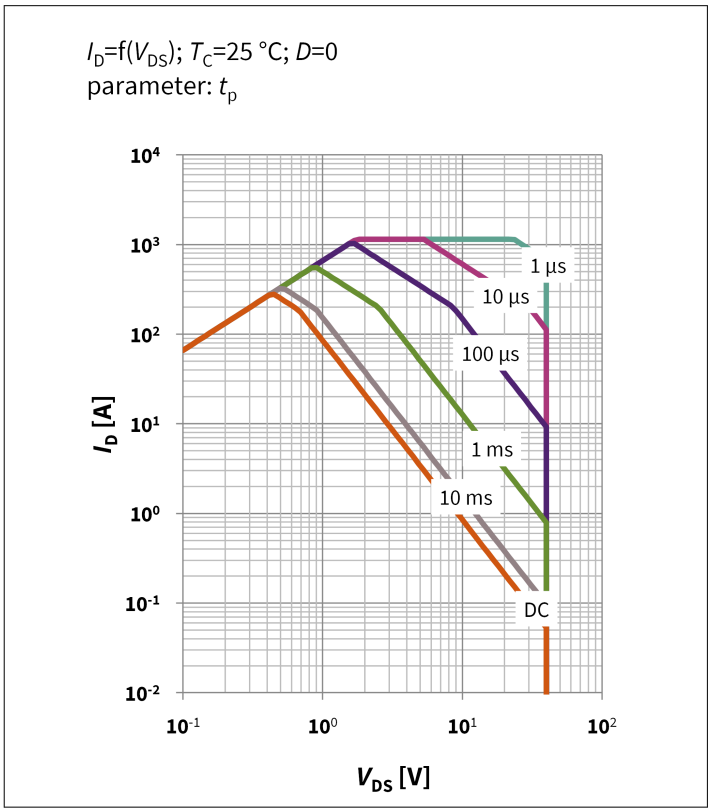


Figure 15 Safe operating area (see Note)

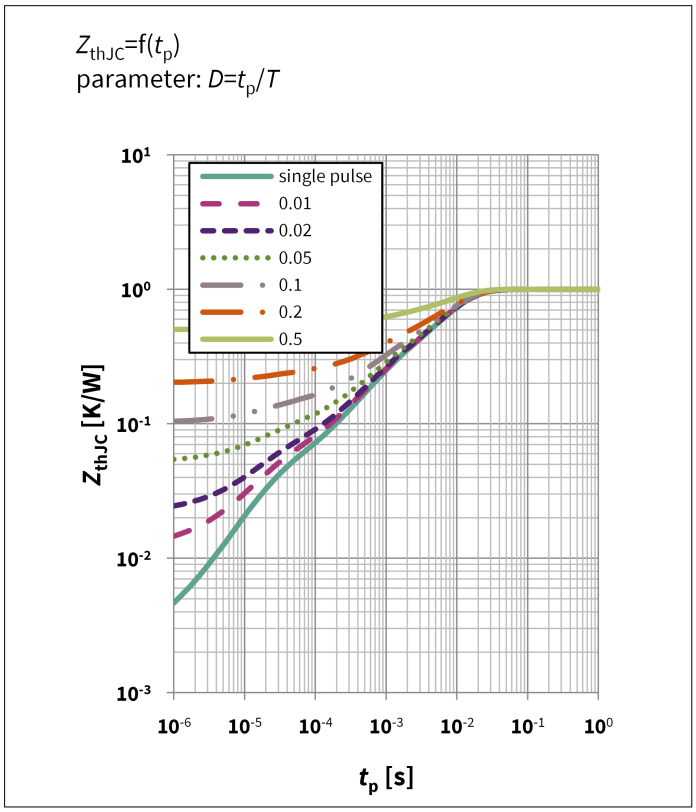


Figure 16 Maximum transient thermal impedance

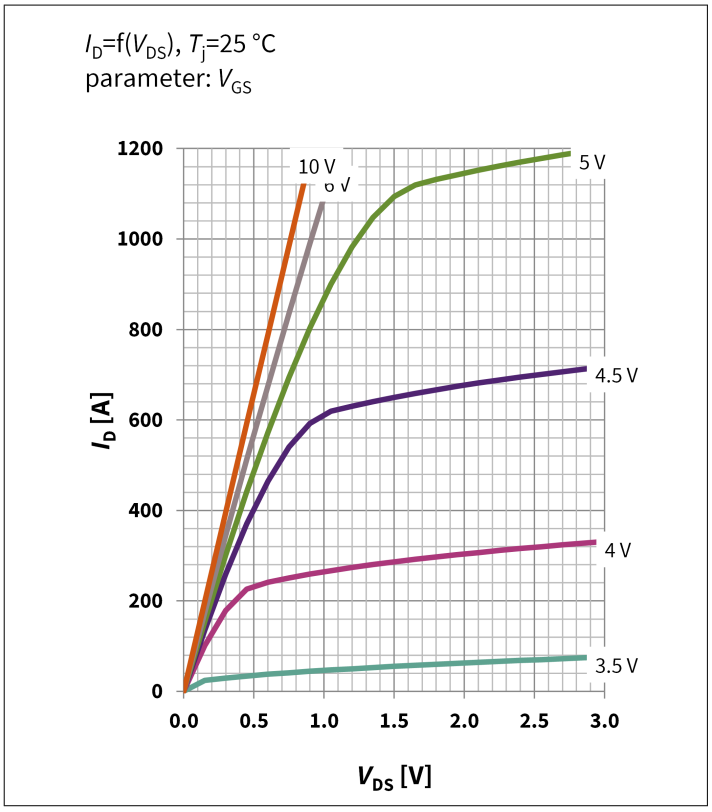


Figure 17 **Typical output characteristics**

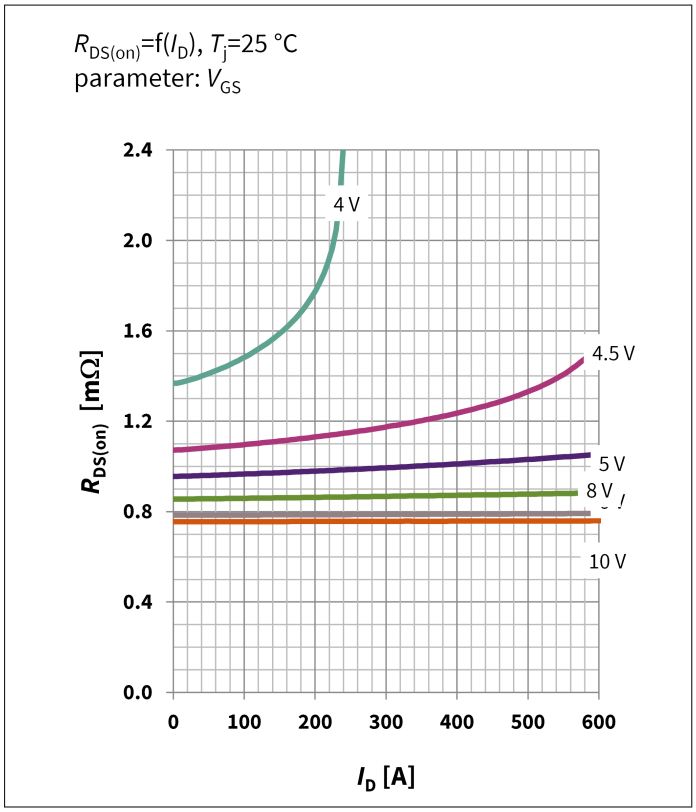


Figure 18 **Typical drain–source on resistance**

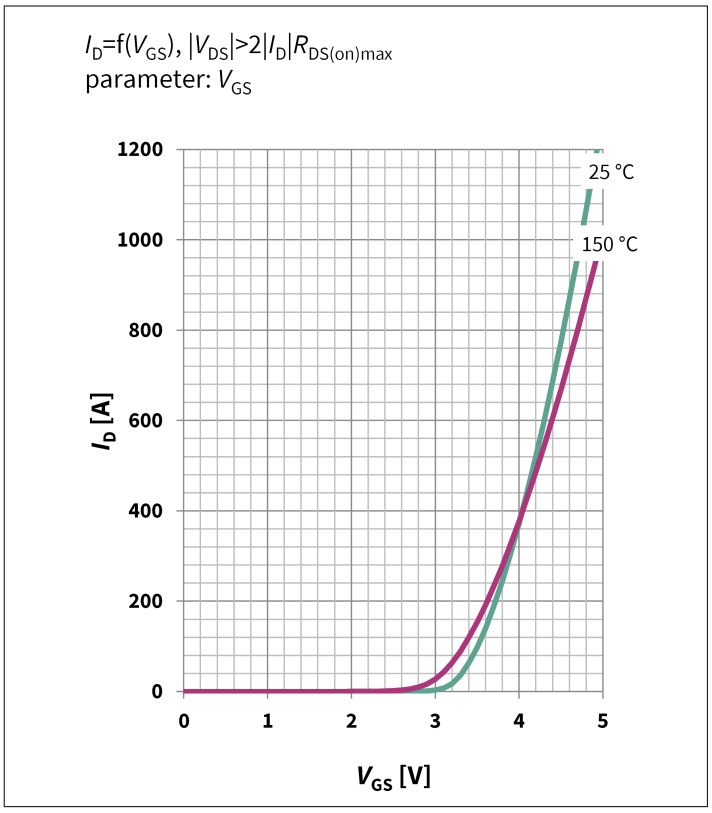


Figure 19 **Typical transfer characteristics**

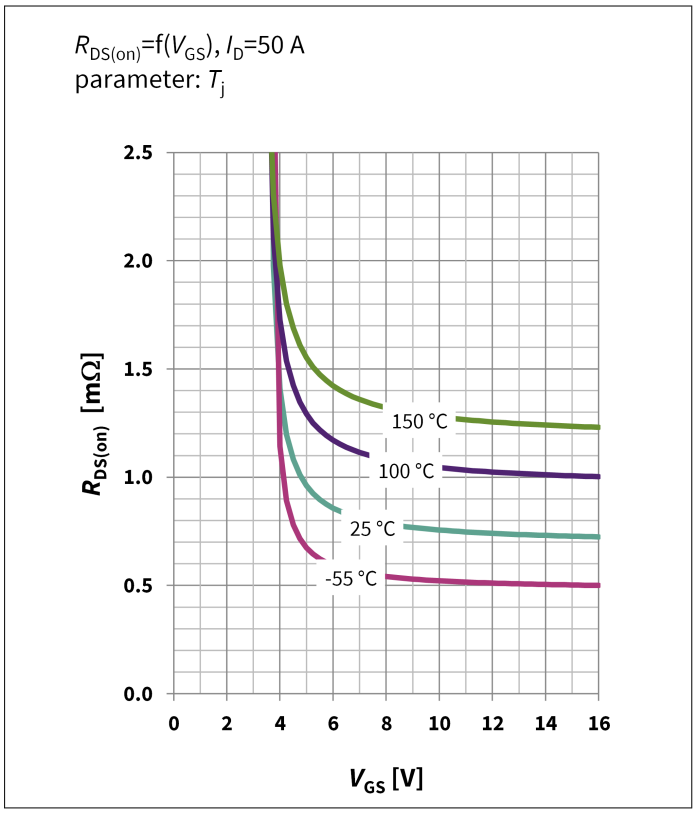


Figure 20 **Typical drain–source on resistance**

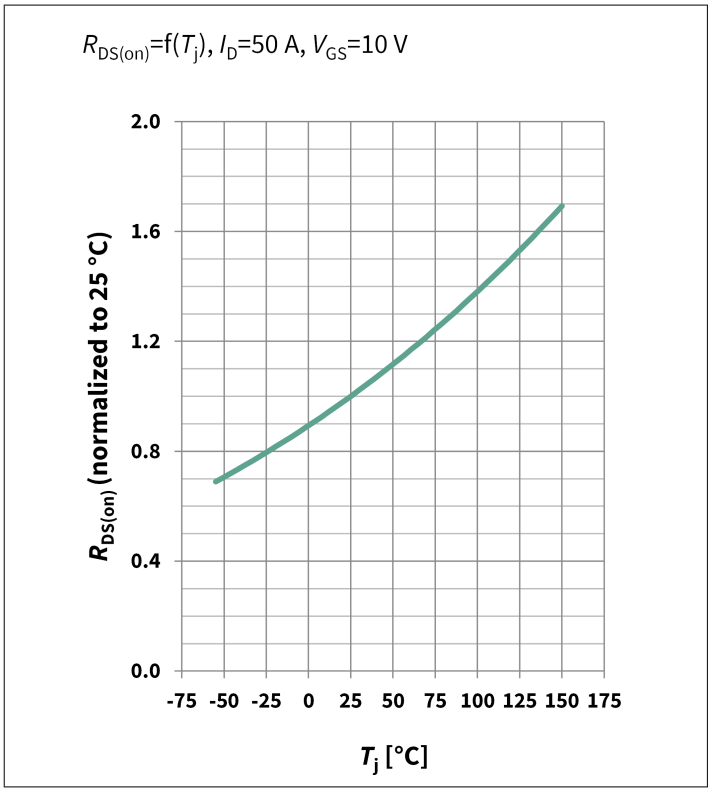


Figure 21 **Normalized drain–source on resistance**

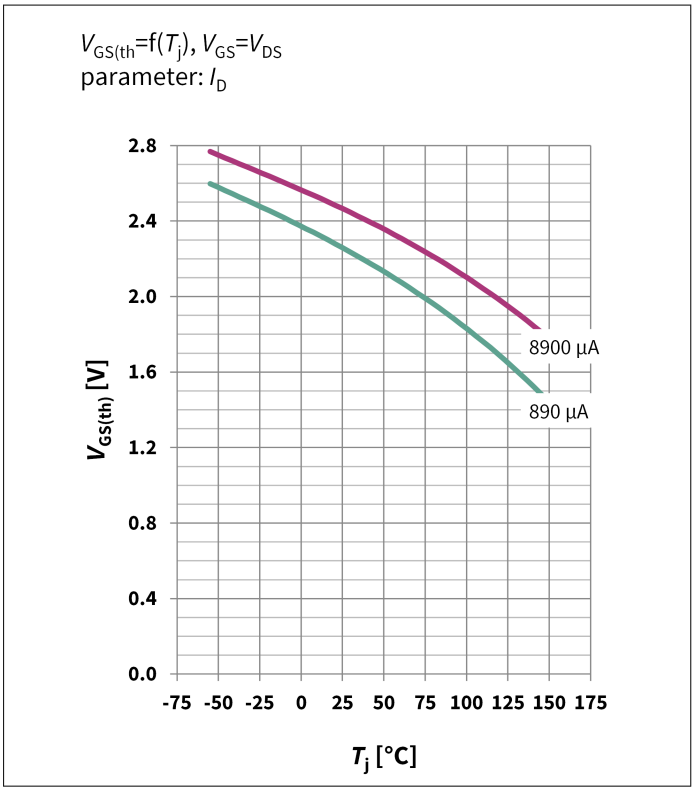


Figure 22 **Typical gate threshold voltage**

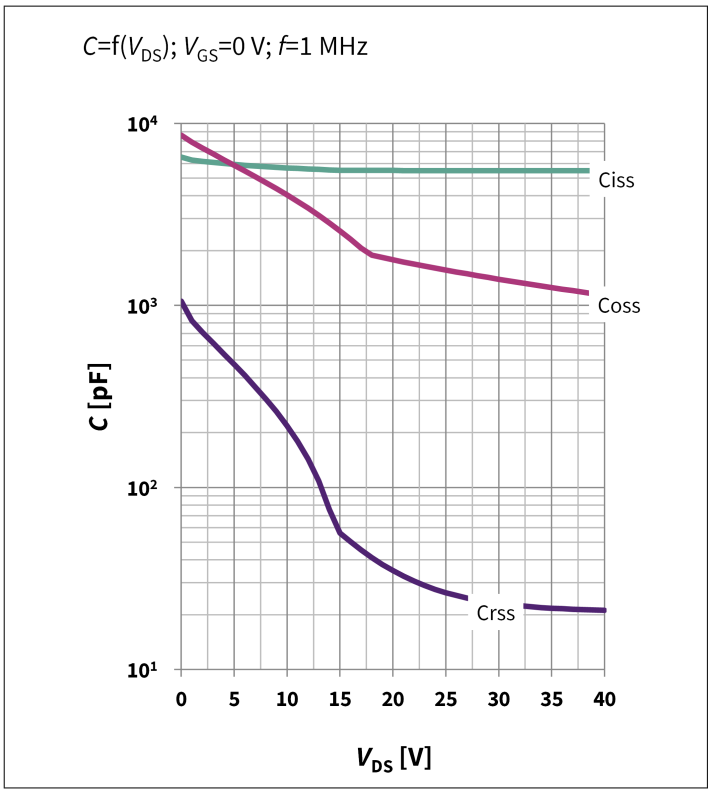


Figure 23 **Typical capacitances**

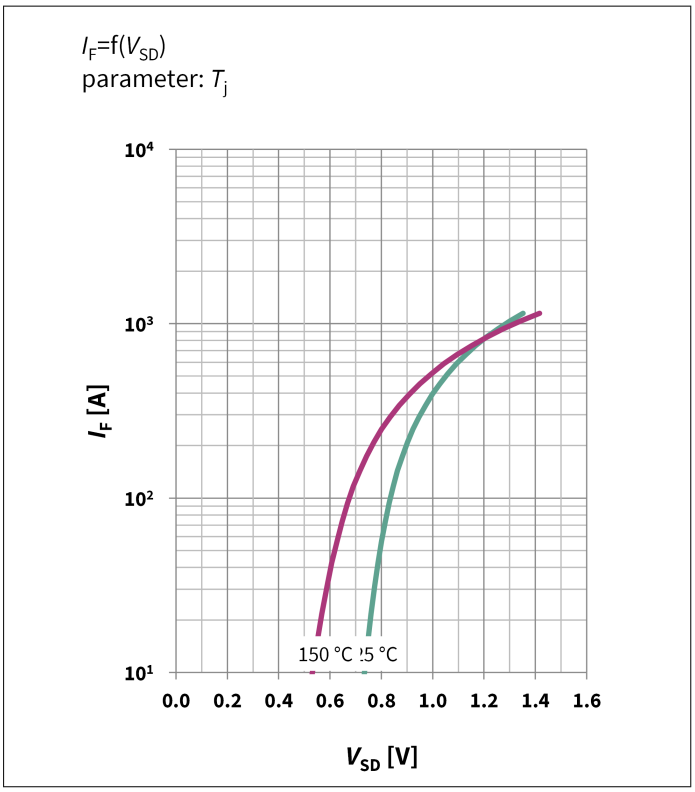


Figure 24 **Typical forward characteristics of reverse diode**

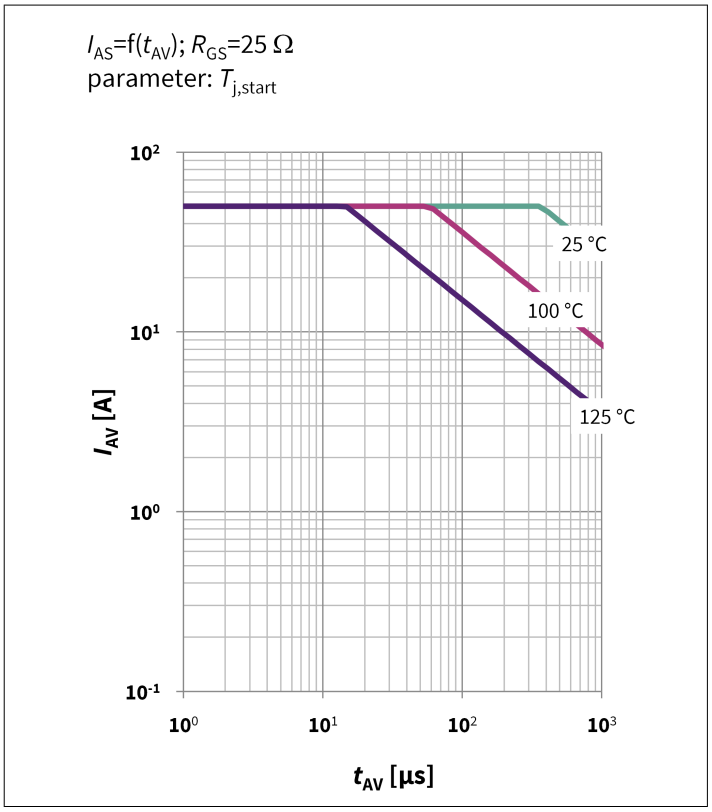


Figure 25 Avalanche characteristics

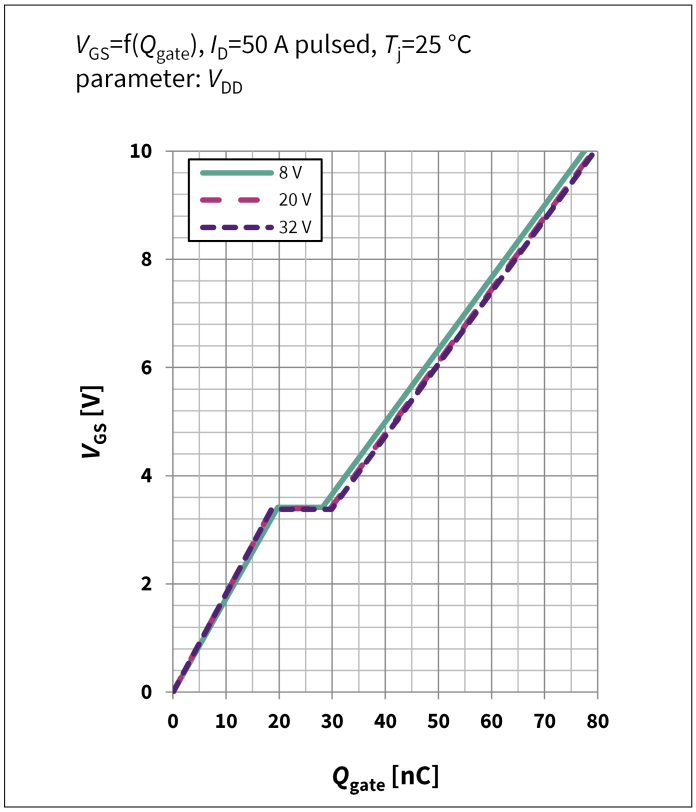


Figure 26 Typical gate charge

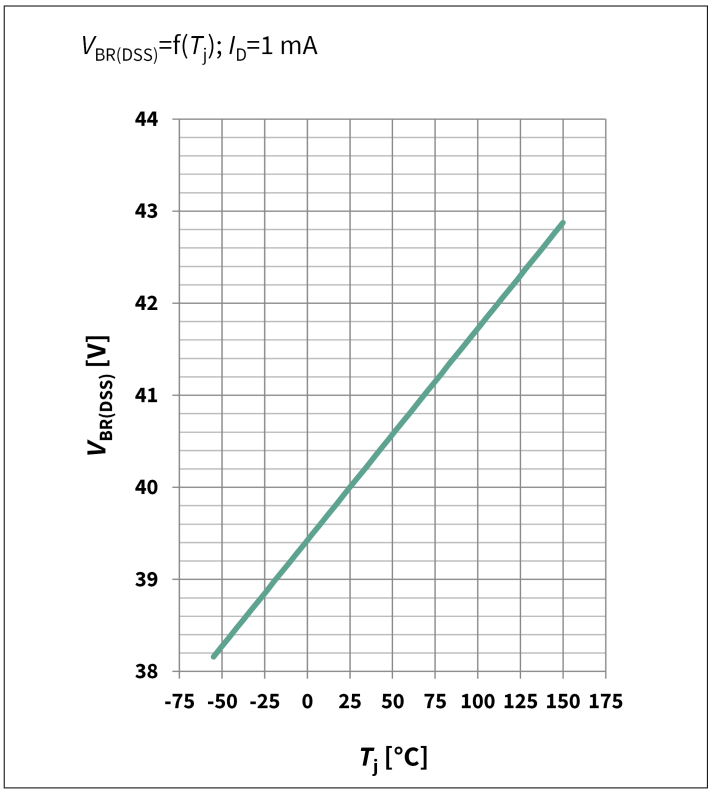


Figure 27 Minimum drain–source breakdown voltage

***Note**: For safe operating area diagram, a pulsed drain current with 287 A < $I_{D,pulse}$ ≤ 350 A is allowed for an accumulated time of up to 50 seconds during the life of the device. Pulsed drain current with 350 A < $I_{D,pulse}$ ≤ 1148 A is allowed up to 20 times during the life of the device.*

6 Package information

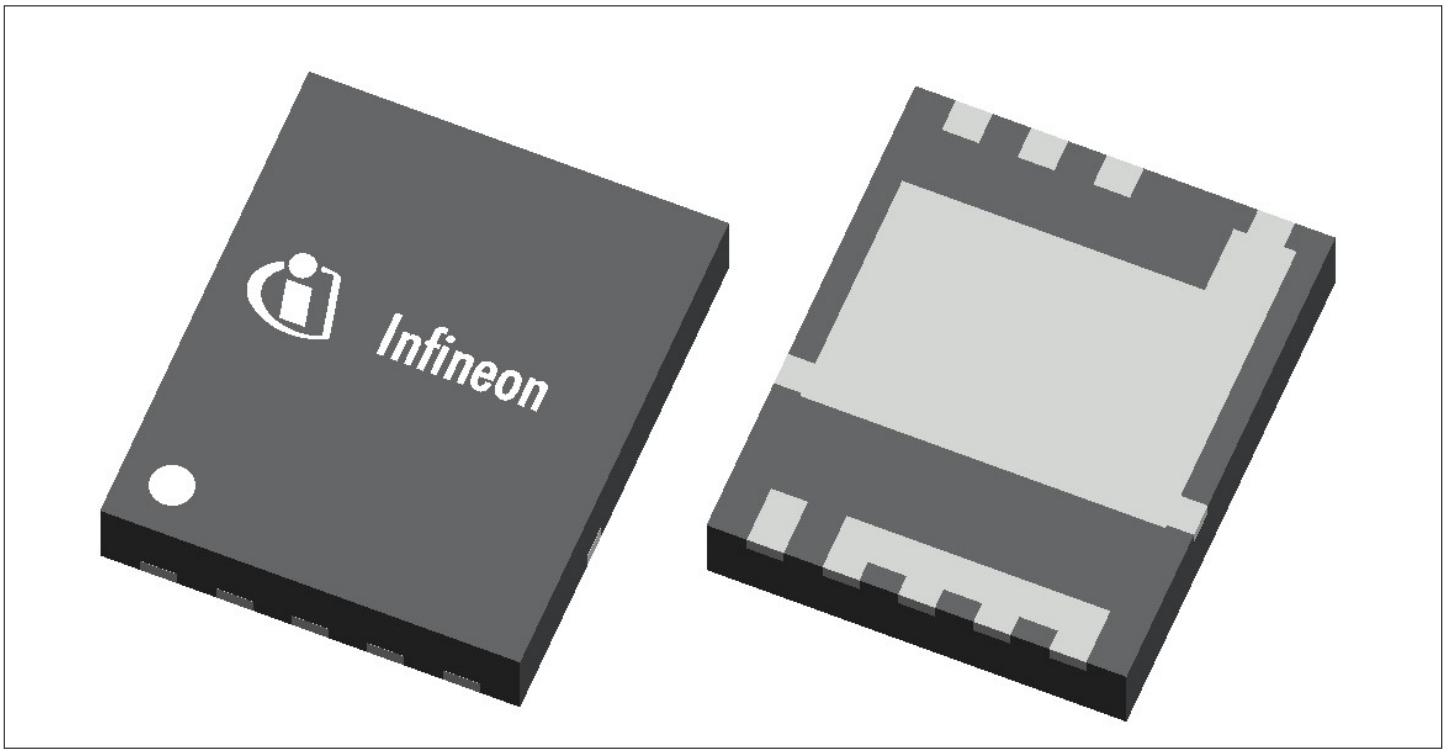


Figure 28 5 mm × 6 mm package

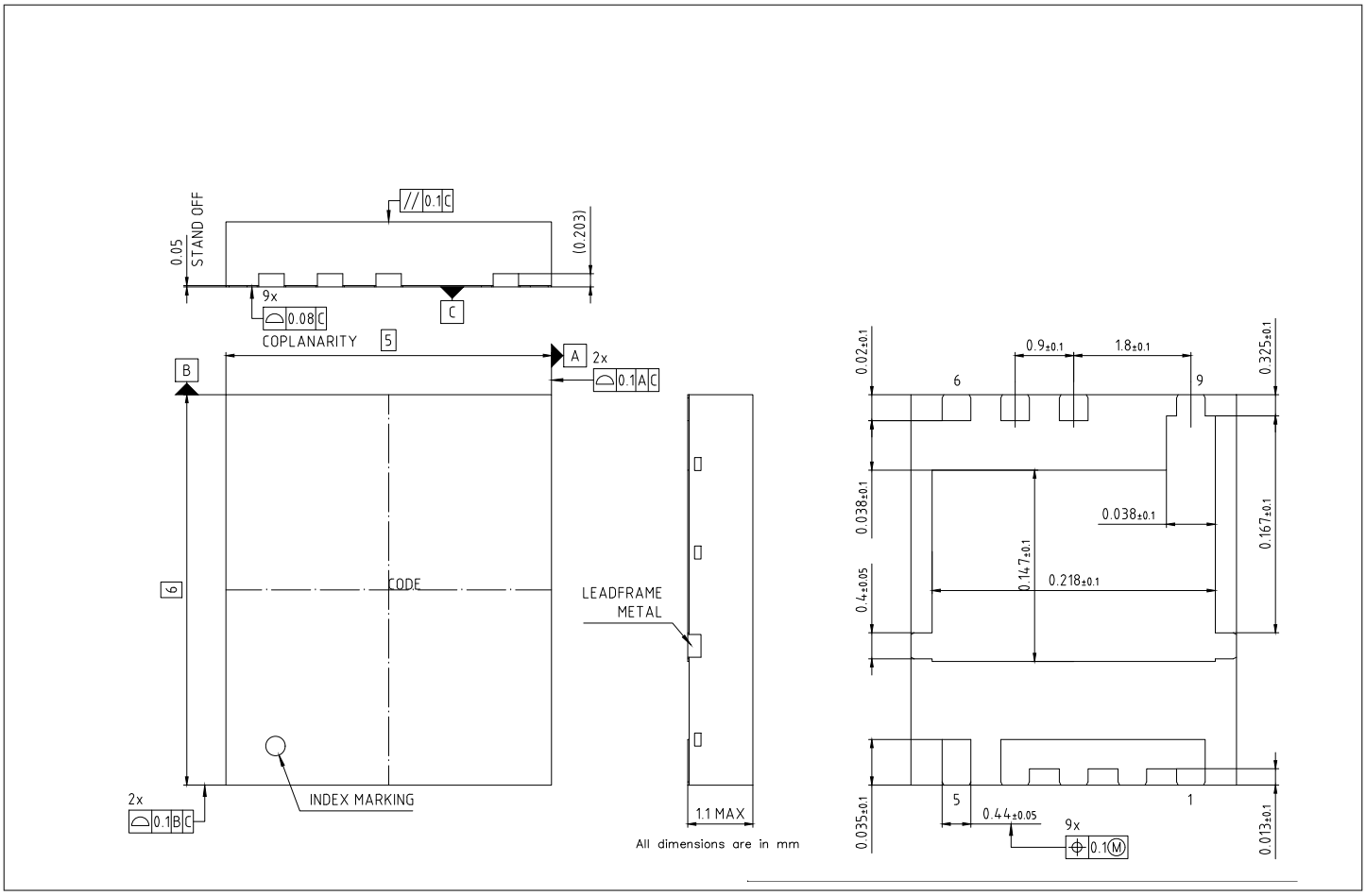


Figure 29 Package outline dimensions

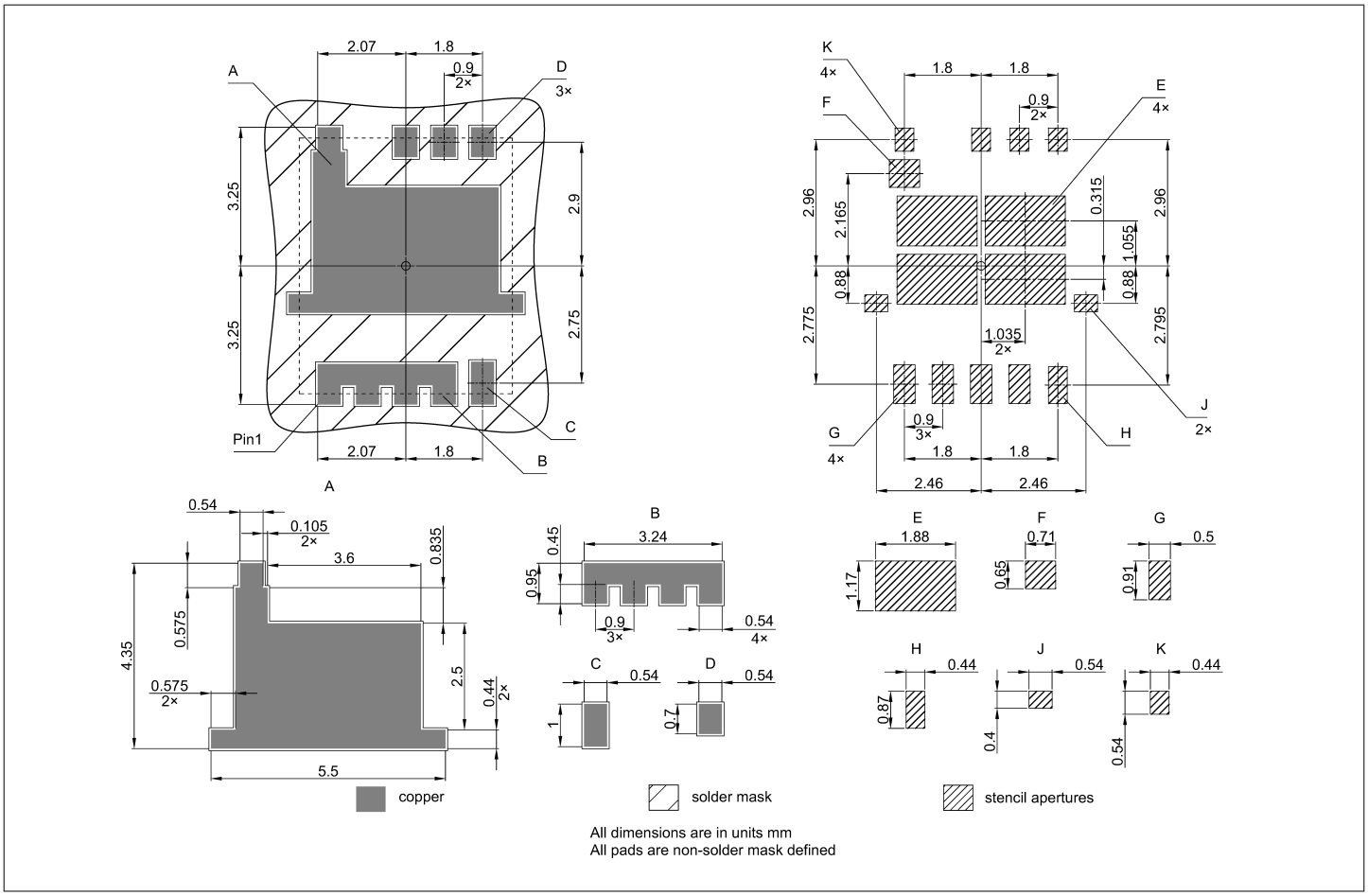


Figure 30 Footprint dimensions

Green Product (RoHS compliant)

To meet the worldwide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: https://www.infineon.com/packages

7 Revision history

Revision	Date	Change description
Rev 1.0	2026-07-14	Initial release

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