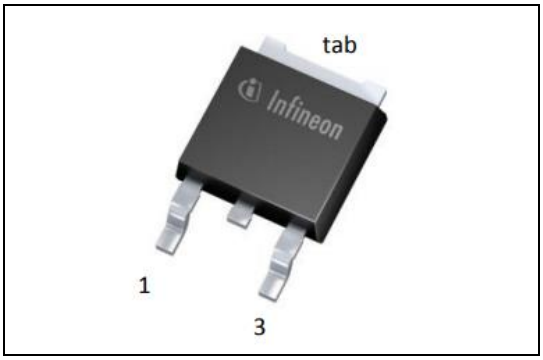
60V p-channel Radiation Tolerant power MOSFET

BUP06CP038F-01



Features

- Low $R_{DS(on)}$
- Single Event Effect (SEE) tolerant
- Total Ionisation Dose (TID) tolerant
  30 kRad approved
- P-channel

Product validation

Qualified for space applications according to the relevant tests of AEC-Q101

Electrical parameters in Table 4 are guaranteed pre- and post-irradiation.

Description

Table 1 Product information

Type	Comment	Pin Configuration			Package
		1	2 (tab)	3	
BUP06CP038F-01		G	D	S	DPAK (TO252)

Table of contents

1 Maximum ratings

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain source voltage	V_{DS}	-	-	-60	V	
Gate source voltage	V_{GS}	-20	-	20	V	static
Drain gate voltage	V_{DG}	-	-	-60	V	
Continuous drain current [1]	I_D	- -	- -	-35 -28	A	T_C= 25 °C T_C= 100 °C
Continuous source current	I_S	-	-	-35	A	
Drain current pulsed	I_{DM}	-	-	-140	Apk	
Total power dissipation [2]	P_{tot}	-	-	125	W	$T_C \leq 25$ °C
Operating temperature	T_{op}	-55	-	175	°C	
Junction temperature	T_j	-55	-	175	°C	
Storage temperature	T_{stg}	-55	-	175	°C	
Avalanche energy	E_{AS}	-	-	500	mJ	I_D= -35A, R_{GS}= 25 Ω

[1] Limited by junction temperature

[2] For T_C > 25°C derating is required.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th,JC}$	-	-	1.2	K/W	
Thermal resistance, junction - ambient	$R_{th,JA}$	-	-	75	K/W	Device on 40mm*40mm *1.5mm epoxy PCB FR4 with 6cm^2 (one layer, 70µm thickness) copper area for drain connection. PCB is vertical without air stream cooling
Soldering temperature	T_{sol}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

3 Electrical characteristics

at T_A=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	BV_{DSS}	-60	-	-	V	I_D= 1 mA, V_{GS}= 0V
Gate threshold voltage	$V_{GS(th)}$	-2	-3	-5	V	I_D= -1.7mA, V_{DS} = V_{GS}
Gate to source leakage current	I_{GSS}	-	-10	-100	nA	V_{DS}= 0V, V_{GS}= +/- 20V
Zero gate voltage drain current	I_{DSS}	- -	-0.1 -10	-1 -100	µA	V_{DS}= -48V, V_{GS}= 0V, T_A= 25°C V_{DS}= -48V, V_{GS}= 0V, T_A= 125°C
Drain source on-state resistance [1]	$R_{DS(ON)}$	-	32	38	mΩ	V_{GS}= -10V, I_D= -35A
Diode forward voltage	V_{SD}	-	-1.2	-1.6	V	V_{GS}= 0V, I_S= -35A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Turn-on delay time	$t_{d(ON)}$	-	16	-	ns	V_{DD}= -30V, V_{GS}= -10V, I_D= -17.5A, R_G= 1.6Ω
Rise time	t_r	-	19	-	ns	V_{DD}= -30V, V_{GS}= -10V, I_D= -17.5A, R_G= 1.6Ω
Turn-off delay time	$t_{d(OFF)}$	-	47	-	ns	V_{DD}= -30V, V_{GS}= -10V, I_D= -17.5A, R_G= 1.6Ω
Fall time	t_f	-	19	-	ns	V_{DD}= -30V, V_{GS}= -10V, I_D= -17.5A, R_G= 1.6Ω
Reverse recovery time	t_{rr}	-	63	-	ns	V_{DD} = -30V, I_F= I_S, di_F/dt= 100A/µs
Common source input capacitance	C_{iss}	-	2.5	-	nF	V_{DS}= -30V, V_{GS}= 0V, f= 1.0MHz
Common source output capacitance	C_{oss}	-	0.36	-	nF	V_{DS}= -30V, V_{GS}= 0V, f= 1.0MHz
Common source reverse transfer capacitance	C_{rss}	-	83	-	pF	V_{DS}= -30V, V_{GS}= 0V, f= 1.0MHz
Total gate charge	Q_G	-	63	-	nC	V_{DD}= -30V, V_{GS}= 0 to -10V, I_D= -35A

[1] Pulsed measurement: Pulse Width < 300µs, Duty Cycle <2.0%.

4 Electrical characteristics diagrams

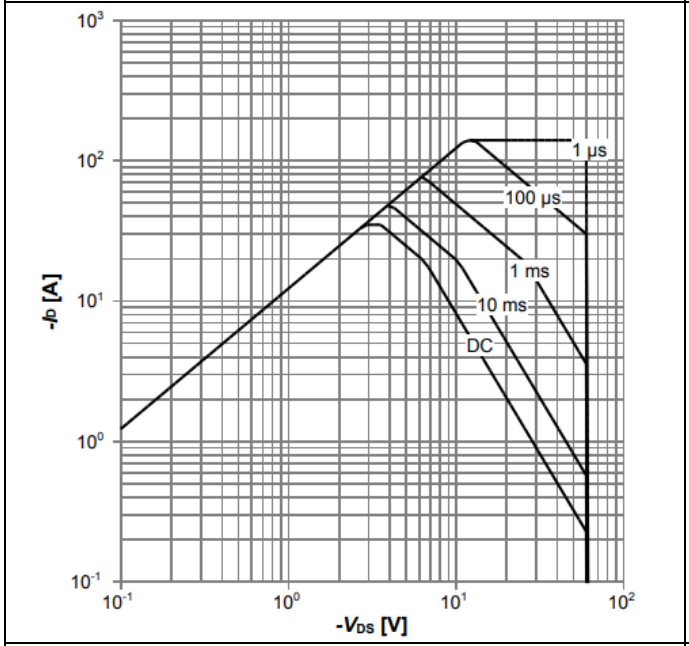
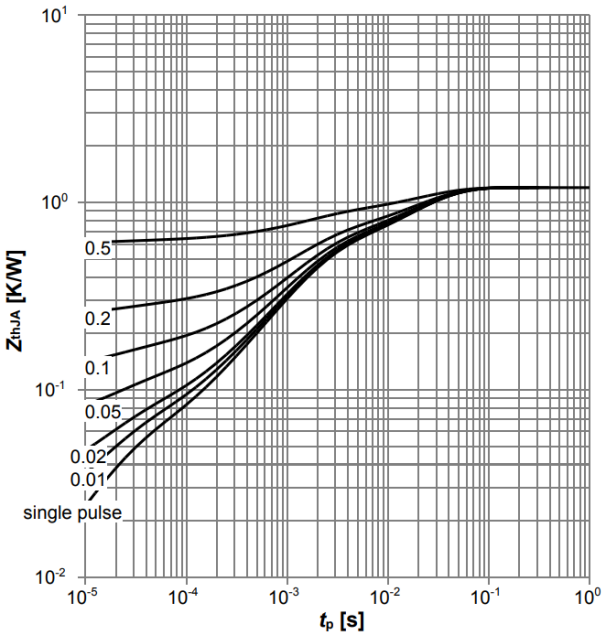
Diagram 1: Safe operating area	Diagram 2: Max. transient thermal impedance
	
$I_D = f(V_{DS})$; $T_C = 25°C$; D=0; parameter: t_p	$Z_{thJC} = f(t_p)$; parameter: $D = t_p/T$

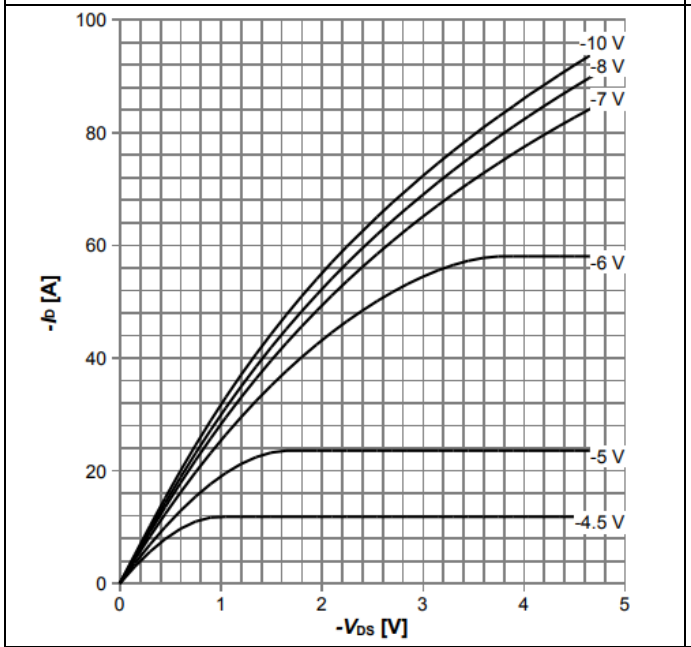
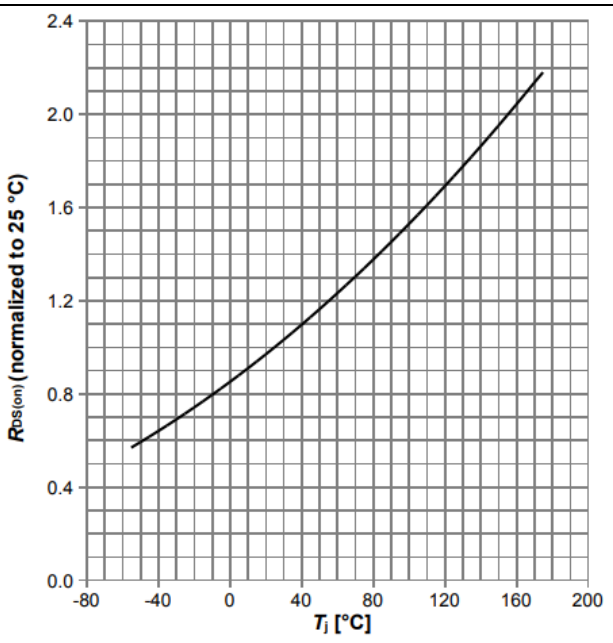
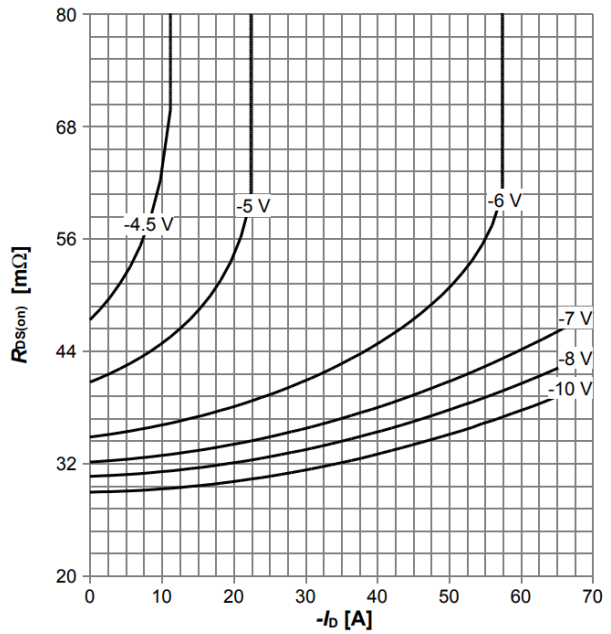
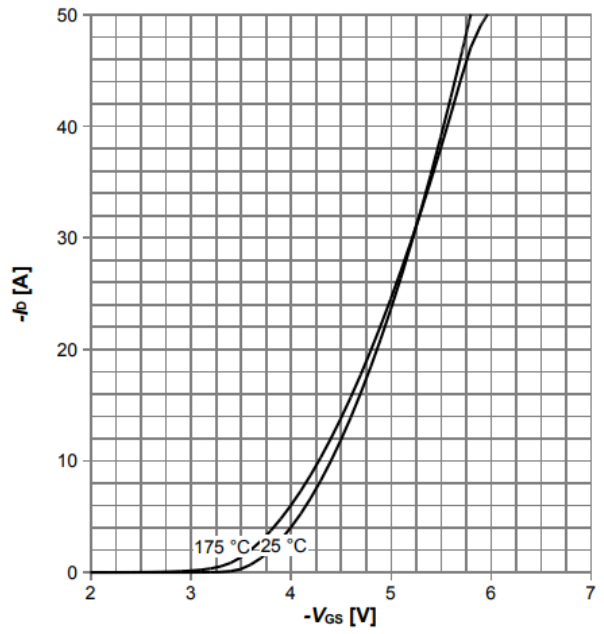
Diagram 3: Typ. output characteristics	Diagram 4: Typ. drain-source on-state resistance
	
$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}	$R_{DS(on)} = f(T_j)$; I_D=-35A; V_{GS}= -10V

Diagram 5: Typ. drain-source on-state resistance



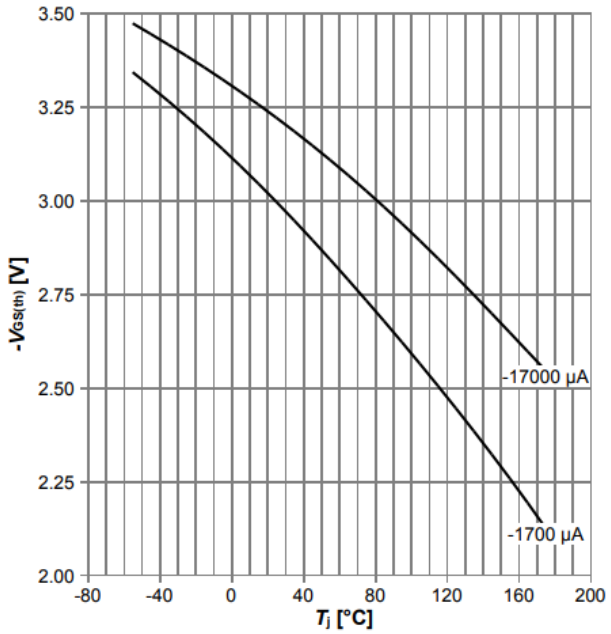
$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: V_{GS}

Diagram 6: Typ. transfer characteristics



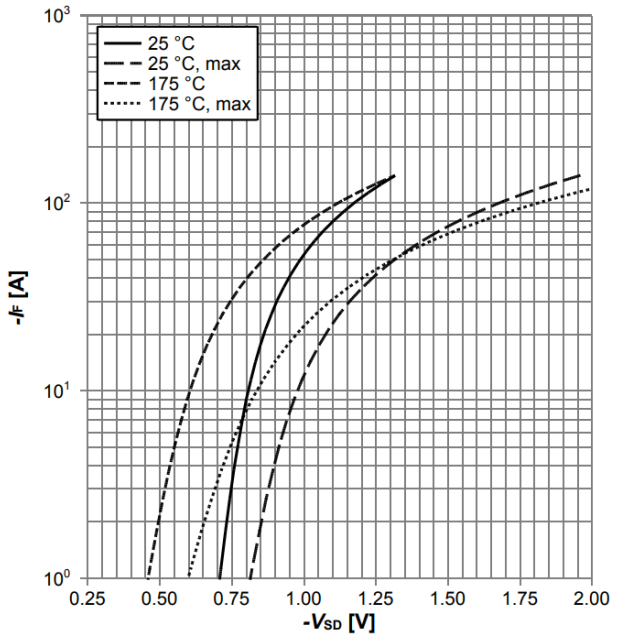
$I_D = f(V_{GS})$, $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$; parameter: T_j

Diagram 7: Typ. gate threshold voltage



$I_D = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D

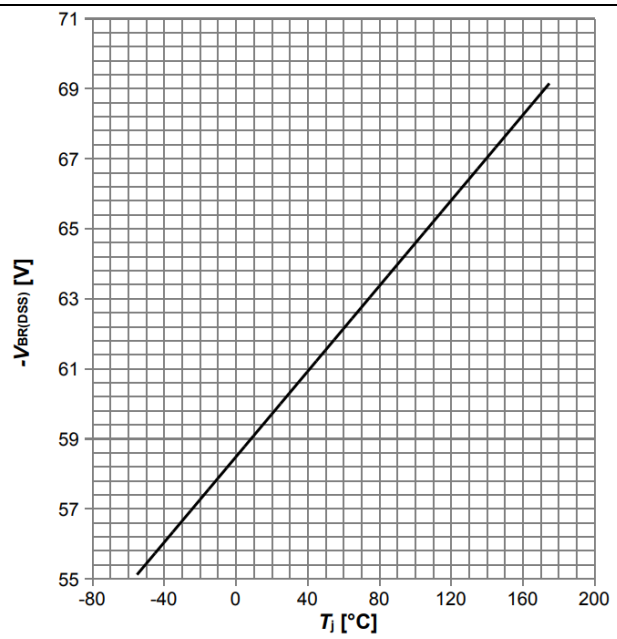
Diagram 8: Forward characteristics of reverse diode



$I_F = f(V_{SD})$; parameter: T_j

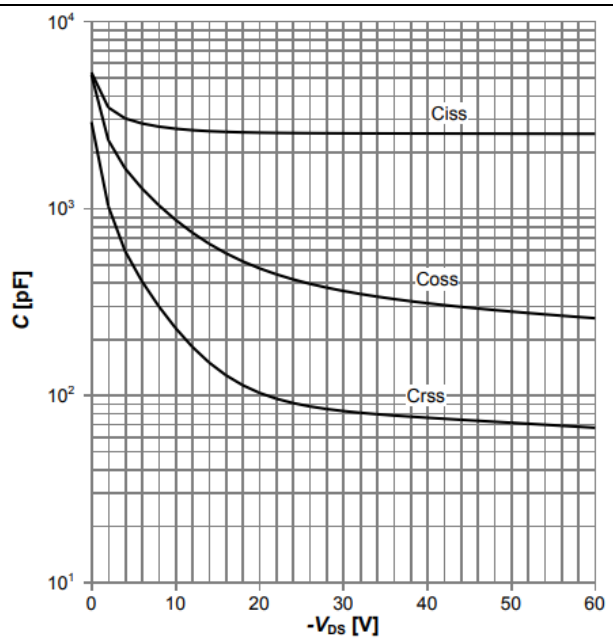
Electrical characteristics diagrams

Diagram 9: Drain-source breakdown voltage



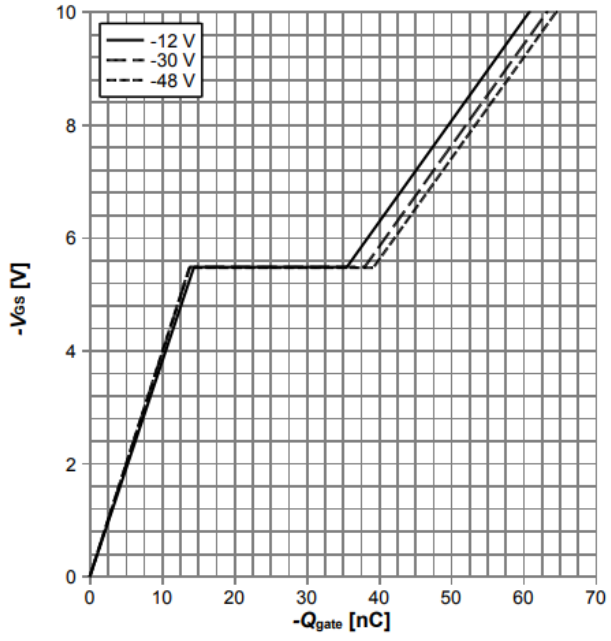
$BV_{DSS} = f(T_j)$; I_D = -250µA

Diagram 10: Typ. capacitances



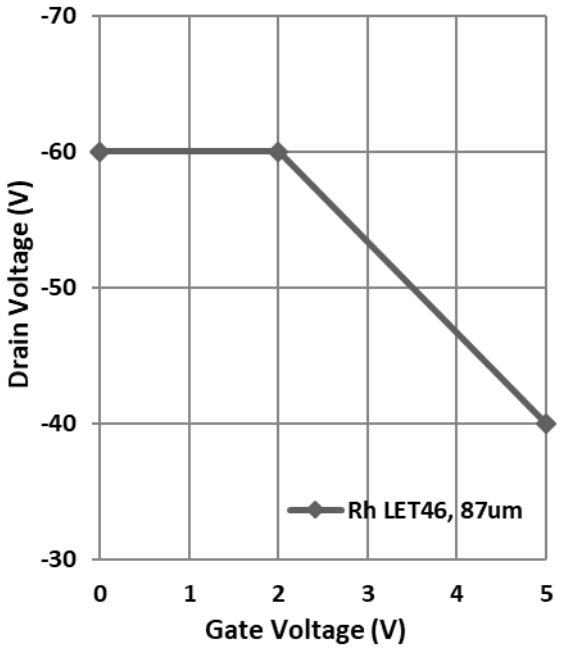
$C = f(V_{DS})$; V_{GS} = 0 V; f = 1 MHz

Diagram 11: Typ. gate charge

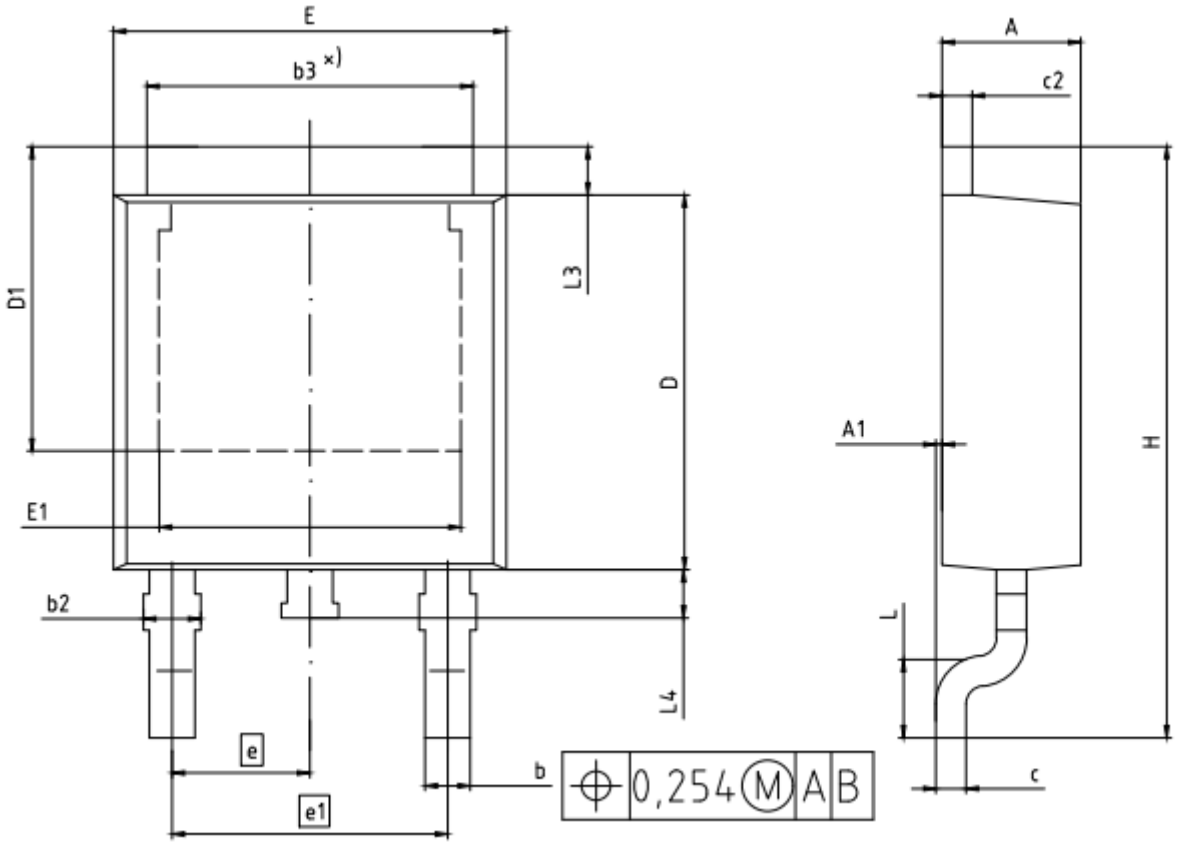


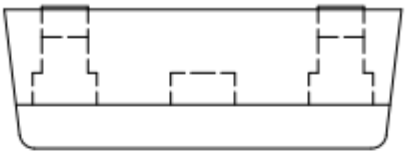
$V_{GS} = f(Q_{gate})$; I_D = -35.0 A pulsed; parameter: V_{DD}

Diagram 12: SEE – Safe operating area



5 Package outlines





NOTES:

1. INDUSTRIAL QUALITY GRADE
2. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	4,95	5.50	0.195	0.217
c	0.46	0.61	0.018	0.024
c2	0.40	0.98	0.016	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.35	6.73	0.250	0.265
E1	4.32	5.21	0.185	0.205
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57 (BSC)		0.180 (BSC)	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.78	0.046	0.070
L3	0.89	1.27	0.035	0.050
L4	0.51	1.02	0.020	0.040

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