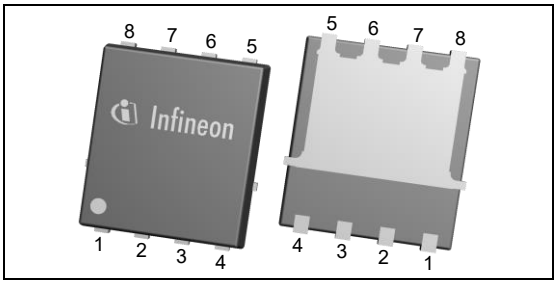
30V p-channel radiation tolerant power MOSFET

BUP03CP010C-02



Features

- Low $R_{DS(on)}$
- Single Event Effect (SEE) tolerant up to Linear Energy Transfer (LET) = 45 MeVcm^2/mg
- Total Ionisation Dose (TID) tolerant up to 50 kRad(Si)
- P-channel

RoHS

Product validation

Qualified for space applications according to the relevant tests of JEDEC[1]

TID irradiation according to ESCC 22900 standard[2]

Description

Table 1 Product information

Type	Comment	Pin Configuration			Package
		1-3	4	5-8	
BUP03CP010C-02		S	G	D	SuperSO8 (PG-TDSON-8)

[1] J-STD20 and JESD22

[2] TID irradiation testing for this device conforms to the ESCC 22900 standard. Parameters specified in this datasheet reflect post irradiation performance only. Rad report can be provided by request. Please contact sales to request a report.

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1 Maximum ratings

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain source voltage	V_{DS}	-	-	-30	V	
Gate source voltage	V_{GS}	-20	-	20	V	static
Drain gate voltage	V_{DG}	-	-	-30	V	
Continuous drain current [1]	I_D	- -	- -	-100 -64	A	T_C = 25 °C T_C = 100 °C
Continuous source current	I_S	-	-	-100	A	
Drain current pulsed	I_{DM}	-	-	-200	Apk	
Total power dissipation [2]	P_{tot}	-	-	83	W	$T_C \leq 25$ °C
Operating temperature	T_{op}	-55	-	150	°C	
Junction temperature	T_j	-55	-	150	°C	
Storage temperature	T_{stg}	-55	-	150	°C	
Avalanche energy	E_{AS}	-	-	135	mJ	I_D = -50 A, R_{GS} = 25 Ω

[1] Limited by junction temperature

[2] For T_C > 25 °C derating is required.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th,JC}$	-	-	1.5	K/W	
Thermal resistance, junction - ambient	$R_{th,JA}$	-	-	50	K/W	Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thickness) copper area for drain connection. PCB is vertical without air stream cooling
Soldering temperature	T_{sol}	-	-	260	°C	1.6 mm (0.063 in.) from case for 10 s

3 Electrical characteristics

at T_A=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	BV_{DSS}	-30	-	-	V	I_{D+} = -250 µA, V_{GS+} = 0 V
Gate threshold voltage	$V_{GS(th)}$	-2	-	-5.5	V	I_{D+} = -150 µA, V_{DS} = V_{GS}
Gate to source leakage current	I_{GSS}	-	-	-10	µA	V_{DS} = 0 V, V_{GS} = +/- 20 V
Zero gate voltage drain current	I_{DSS}	- -	- -	-1 -100	µA	V_{DS} = -24 V, V_{GS} = 0 V, T_A = 25 °C V_{DS} = -24 V, V_{GS} = 0 V, T_A = 125 °C
Drain source on-state resistance [1]	$R_{DS(ON)}$	-	-	10	mΩ	V_{GS} = -10 V, I_D = -50 A
Diode forward voltage	V_{SD}	-	-	-1.1	V	V_{GS} = 0 V, I_S = -50 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Turn-on delay time	$t_{d(ON)}$	-	15	-	ns	V_{DD} = -15 V, V_{GS} = -10 V, I_D = -50 A, R_G = 6 Ω
Rise time	t_r	-	139	-	ns	V_{DD} = -15 V, V_{GS} = -10 V, I_D = -50 A, R_G = 6 Ω
Turn-off delay time	$t_{d(OFF)}$	-	66	-	ns	V_{DD} = -15 V, V_{GS} = -10 V, I_D = -50 A, R_G = 6 Ω
Fall time	t_f	-	34	-	ns	V_{DD} = -15 V, V_{GS} = -10 V, I_D = -50 A, R_G = 6 Ω
Reverse recovery time	t_{rr}	-	51	-	ns	V_{DD} = -15 V, I_F = I_S, di_F/dt = 100 A/µs
Common source input capacitance	C_{iss}	-	4.5	-	nF	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz
Common source output capacitance	C_{oss}	-	2.1	-	nF	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz
Common source reverse transfer capacitance	C_{rss}	-	150	-	pF	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz
Total gate charge	Q_G	-	61	-	nC	V_{DD} = -15 V, V_{GS} = 0 to -10 V, I_D = -50 A

[1] Pulsed measurement: Pulse Width < 300 µs, Duty Cycle < 2.0%.

4 Electrical characteristics diagrams

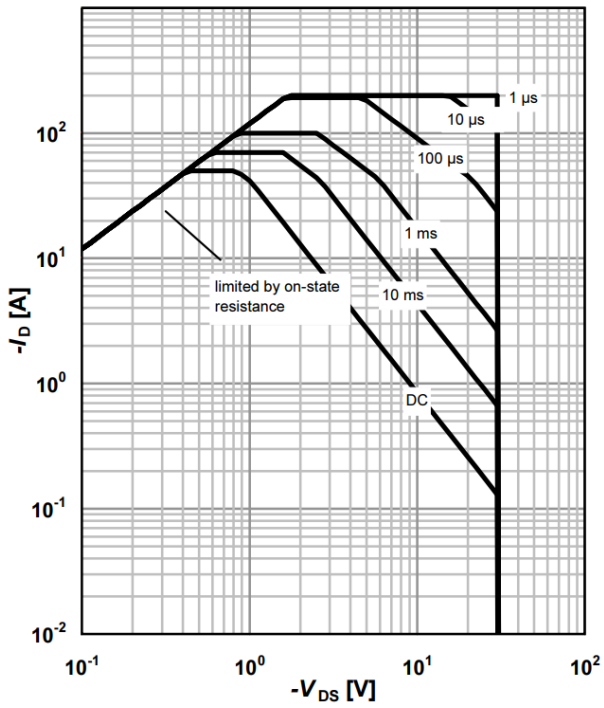
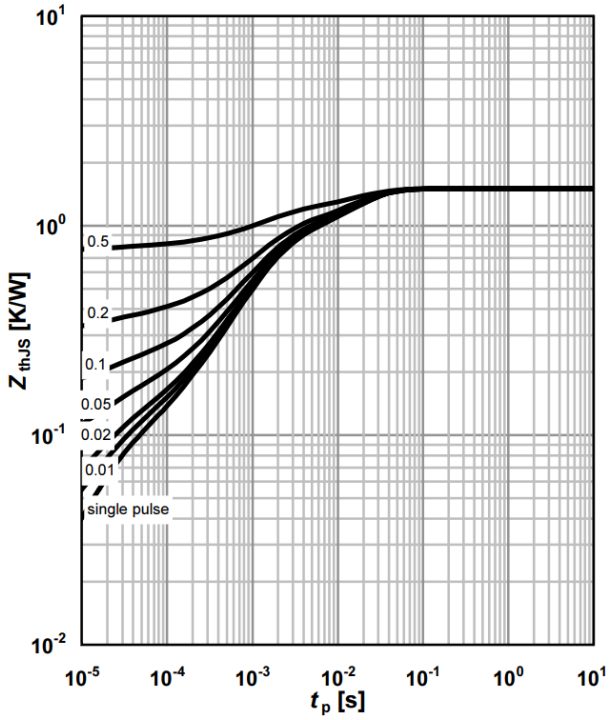
Diagram 1: Safe operating area	Diagram 2: Max. transient thermal impedance
	
$I_D = f(V_{DS})$; $T_C = 25°C$; D=0; parameter: t_p	$Z_{thJC} = f(t_p)$; parameter: $D = t_p/T$

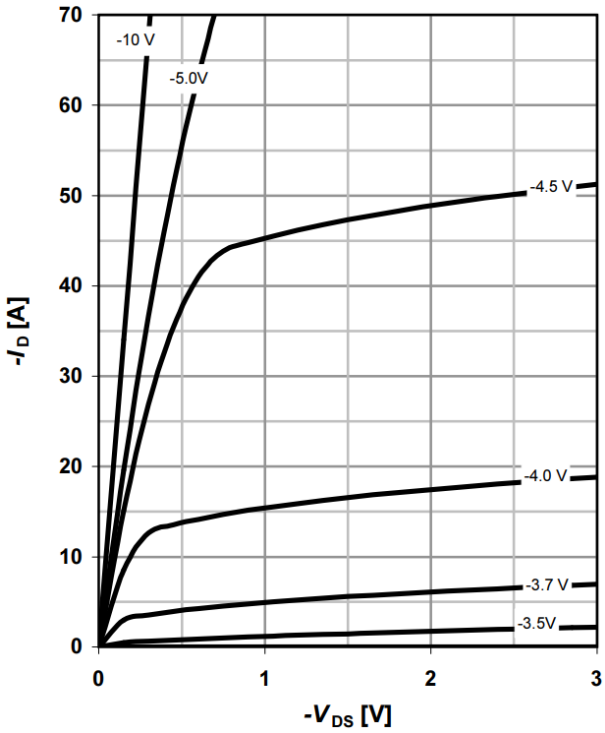
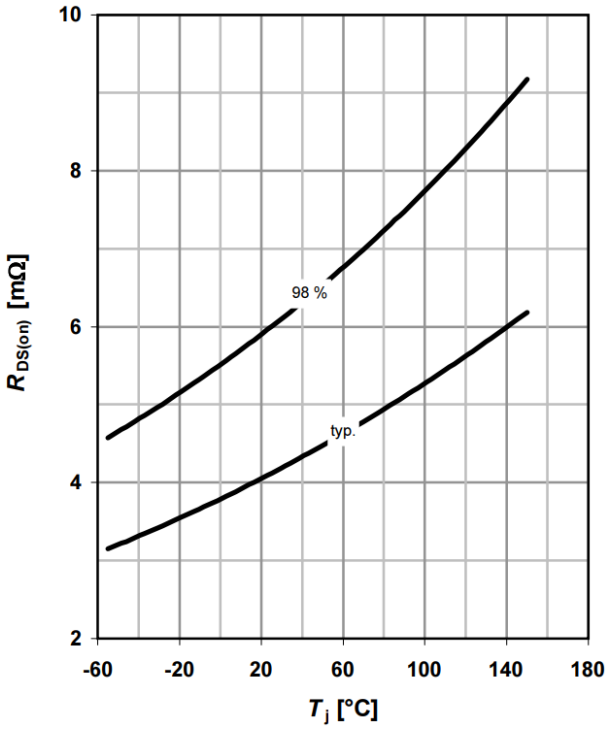
Diagram 3: Typ. output characteristics	Diagram 4: Typ. drain-source on-state resistance
	
$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}	$R_{DS(on)} = f(T_j)$; I_D=-50A; V_{GS}= -10V

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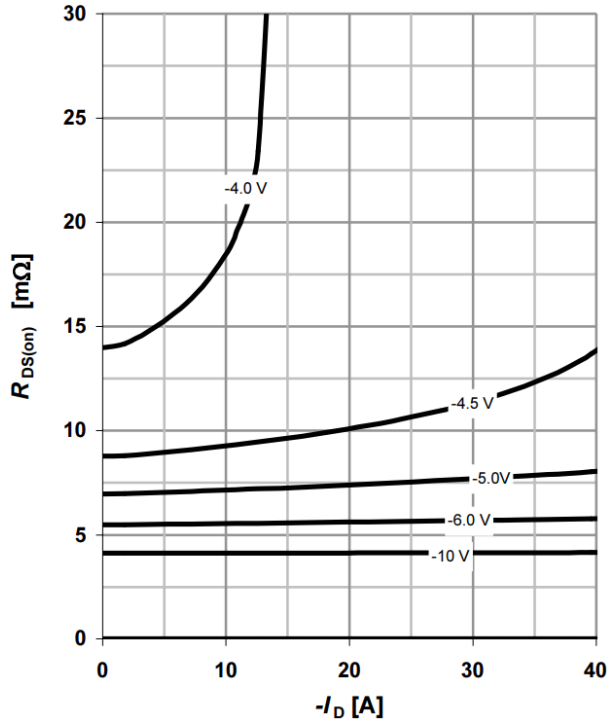
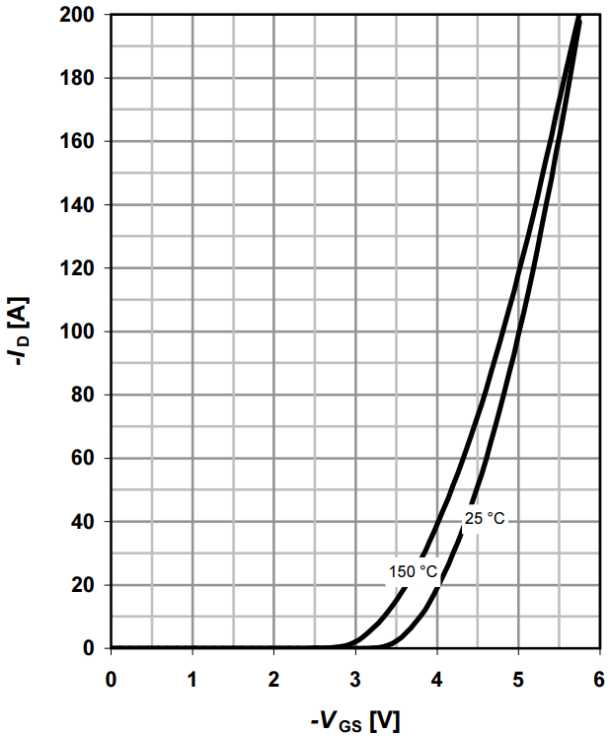
Diagram 5: Typ. drain-source on-state resistance	Diagram 6: Typ. transfer characteristics
	
$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: V_{GS}	$I_D = f(V_{GS})$, $V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$; parameter: T_j

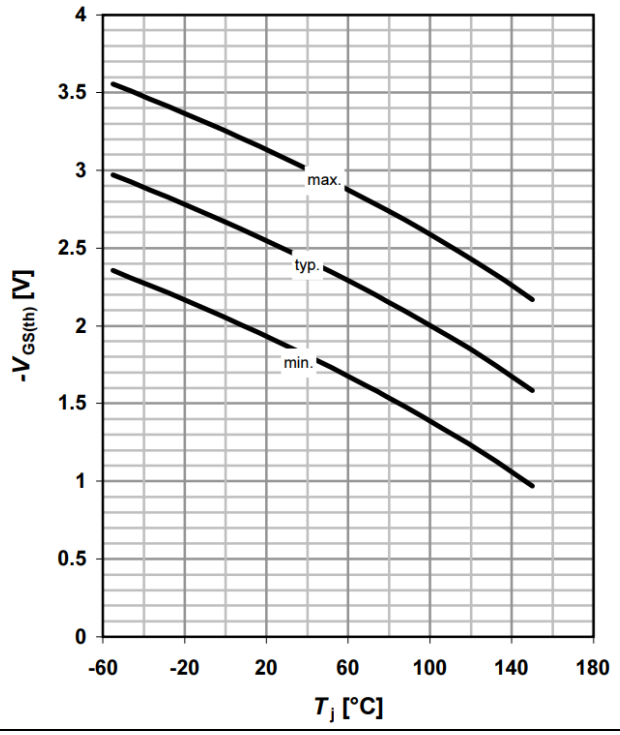
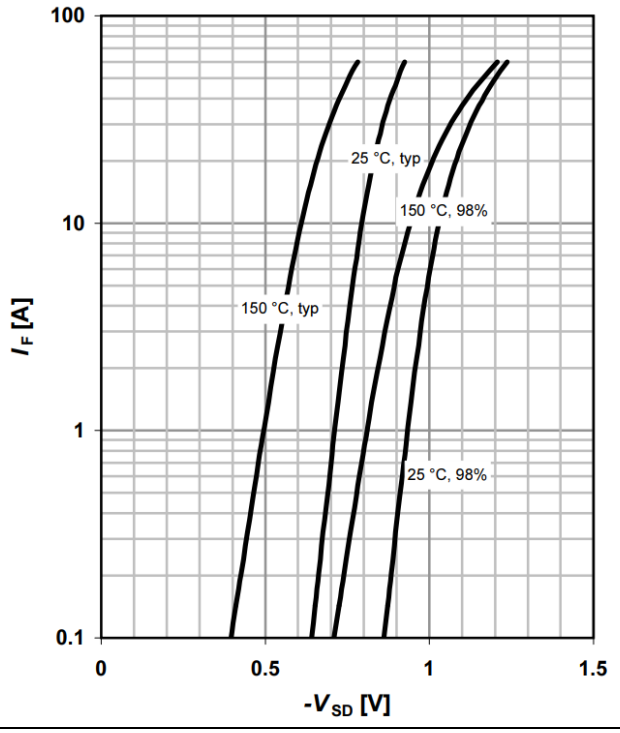
Diagram 7: Typ. gate threshold voltage	Diagram 8: Forward characteristics of reverse diode
	
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = -150µA	$I_F = f(V_{SD})$; parameter: T_j

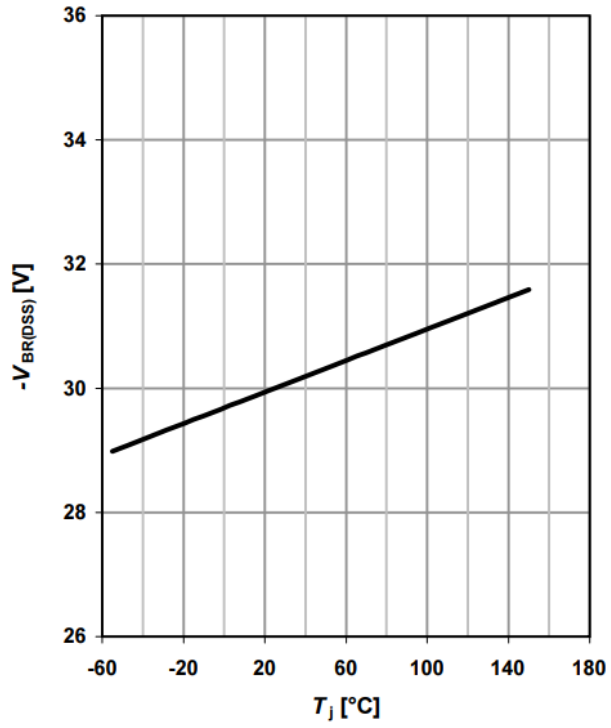
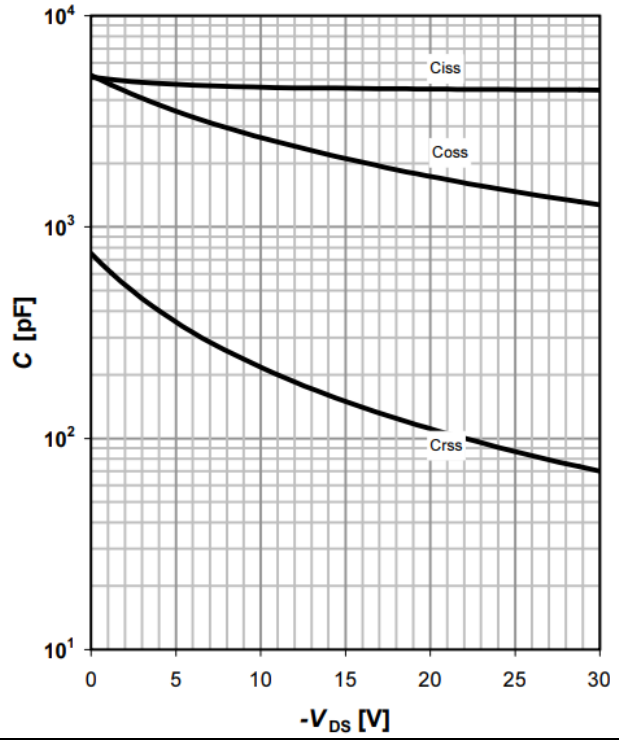
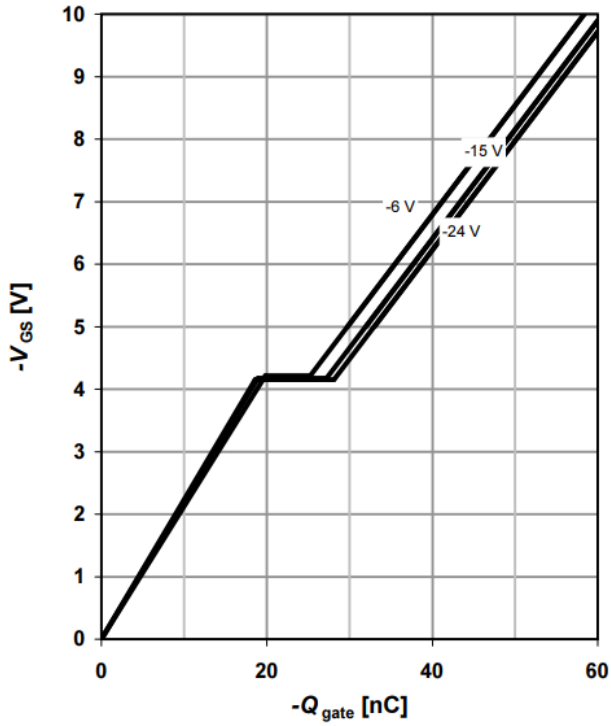
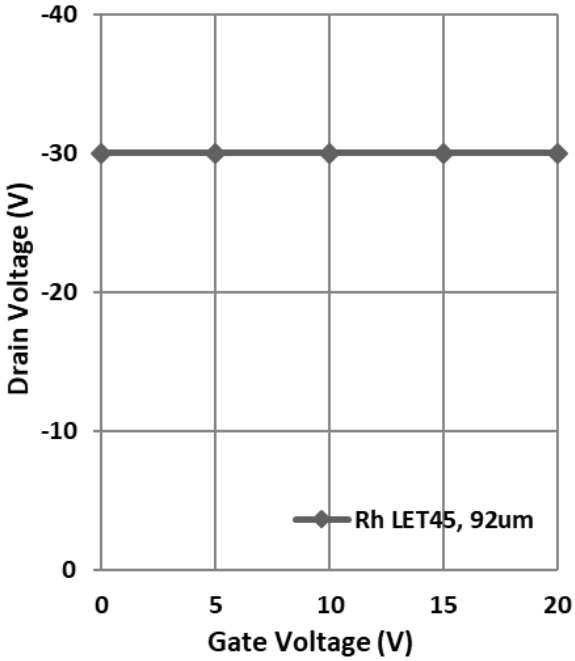
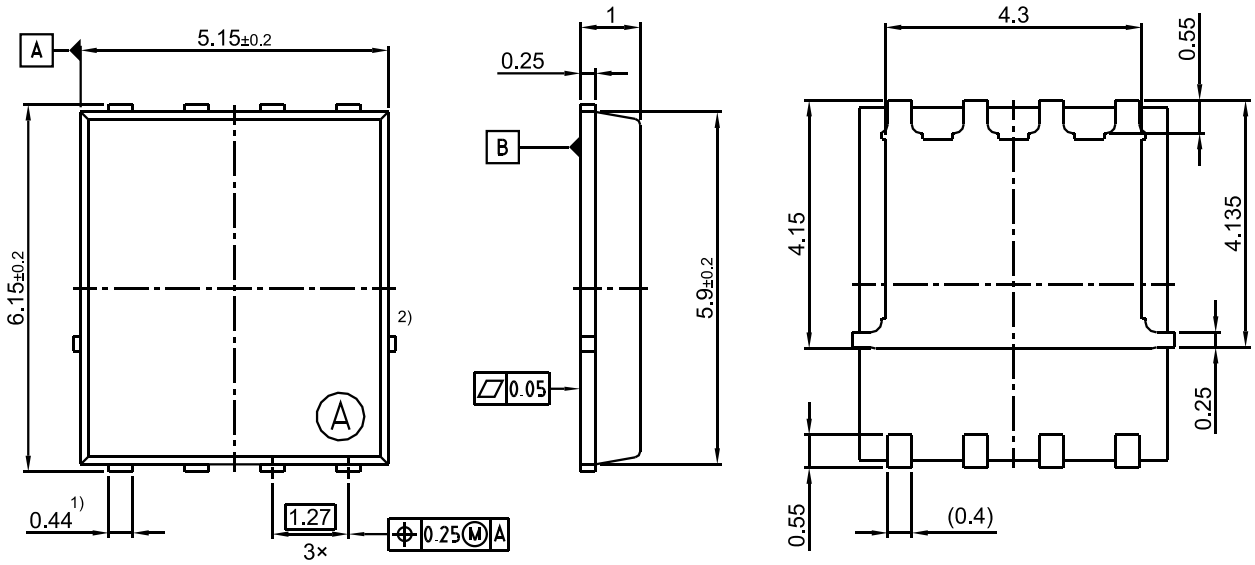
Diagram 9: Drain-source breakdown voltage	Diagram 10: Typ. capacitances
	
$BV_{DSS} = f(T_j)$; I_D = -250µA	$C = f(V_{DS})$; V_{GS} = 0 V; f = 1 MHz

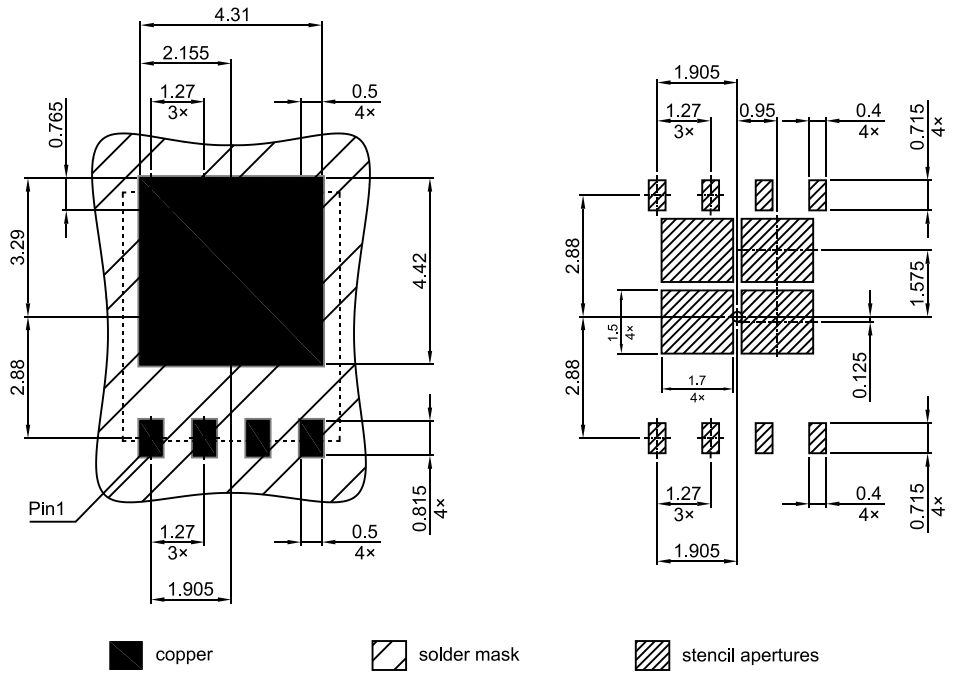
Diagram 11: Typ. gate charge	Diagram 12: SEE – Safe operating area
	
$V_{GS} = f(Q_{gate})$; I_D = -50 A pulsed; parameter: V_{DD}	

5 Package outlines and footprint



1) Exclude mold flash
2) Removal on mold gate, Intrusion 0.1mm
Protrusion 0.1mm

All metal surfaces are plated except area of cut
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊕]
Drawings according to ISO 8015, general tolerances ±0.1 / 1°30'



All dimensions are in units mm
All pads are solder mask defined

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Edition 1.1, April 2026
Published by
Infineon Technologies AG
81726 München, Germany

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