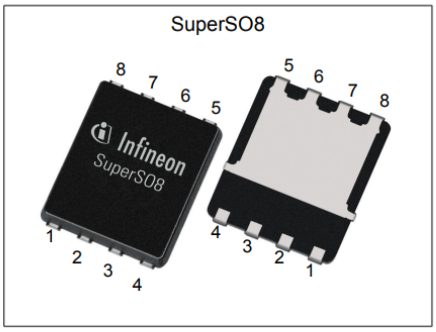
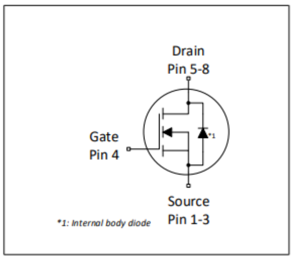
英飞凌MOSFET功率晶体管

英飞凌BSC105N15LS5 OptiMOS™5 150 V 功率晶体管



特性

- N沟道，逻辑电平
- 极低的导通电阻 $R_{DS(on)}$
- 卓越的耐热性
- 100% 雪崩测试
- 无铅镀层；符合RoHS标准
- 符合 IEC61249-2-21 标准的无卤素



产品验证

完全符合 JEDEC 工业应用标准

表 1 主要性能参数

Parameter	Value	Unit
V_{DS}	150	V
$R_{DS(on),max}$	10.5	mΩ
I_D	76	A
Q_{oss}	81	nC
Q_G (0V...10V)	34	nC

Type / Ordering Code	Package	Marking	Related Links
BSC105N15LS5	PG-TDSON-8	105N15LS	-

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目录

1 最大额定值

除非另有规定， $T_A = 25$ °C

表 2 最大额定值

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - - -	- - - -	76 48 41 10.7	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10V,T_A=25°C,R_{thJA}=50°C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	304	A	T_C=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	62	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	125 2.5	W	T_C=25 °C T_A=25 °C, R_{THJA}=50 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

2 热特性

表3 热特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	1.0	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area[2]	R_{thJA}	-	-	50	°C/W	-

[1]额定值指产品仅具有数据表指定的绝对最大值，保持外壳温度符合规定要求。其他外壳温度请参见图 2。需要根据实际环境条件降低额定值。

[2] 器件安装在 40 mm x 40 mm x 1.5 mm环氧树脂印刷电路板 FR4 上，漏极连接用铜面积为 6 cm² （一层，70 µm厚）。印刷电路板垂直放置在静止空气中。

[3]详细信息请参见图 3

[4]详细信息请参见图 13

3 电气特性

除非另有规定， $T_j = 25$ °C

表4 静态特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.3	1.8	2.3	V	V_{DS}=V_{GS}, I_D=91 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1.0 100	µA	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C V_{DS}=120 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	8.8 10.9	10.5 14	mΩ	V_{GS}=10 V, I_D=40 A V_{GS}=4.5 V, I_D=20 A
Gate resistance	R_G	-	0.9	1.35	Ω	-
Transconductance	g_{fs}	-	70	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=40 A

表 5 动态特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2300	3000	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	580	750	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	17	30	pF	V_{GS}=0 V, V_{DS}=75 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	6.4	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=40 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	2.3	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=40 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	17.8	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=40 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	3.4	-	ns	V_{DD}=75 V, V_{GS}=10 V, I_D=40 A, $R_{G,ext}$=1.6 Ω

表6 栅极电荷特性[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	7.5	-	nC	V_{DD}=75 V, I_D=40 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	4.1	-	nC	V_{DD}=75 V, I_D=40 A, V_{GS}=0 to 4.5 V
Gate to drain charge[1]	Q_{gd}	-	6.9	10.4	nC	V_{DD}=75 V, I_D=40 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	10.3	-	nC	V_{DD}=75 V, I_D=40 A, V_{GS}=0 to 4.5 V
Gate charge total[1]	Q_g	-	18.1	23.0	nC	V_{DD}=75 V, I_D=40 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	3.3	-	V	V_{DD}=75 V, I_D=40 A, V_{GS}=0 to 4.5 V
Gate charge total[1]	Q_g	-	34	43	nC	V_{DD}=75 V, I_D=40 A, V_{GS}=0 to 10 V
Output charge[1]	Q_{oss}	-	81	108	nC	V_{DS}=75 V, V_{GS}=0 V

[1)]由设计标定，不受制于生产测试。
[2)] 参数定义请参见“栅极电荷波形”

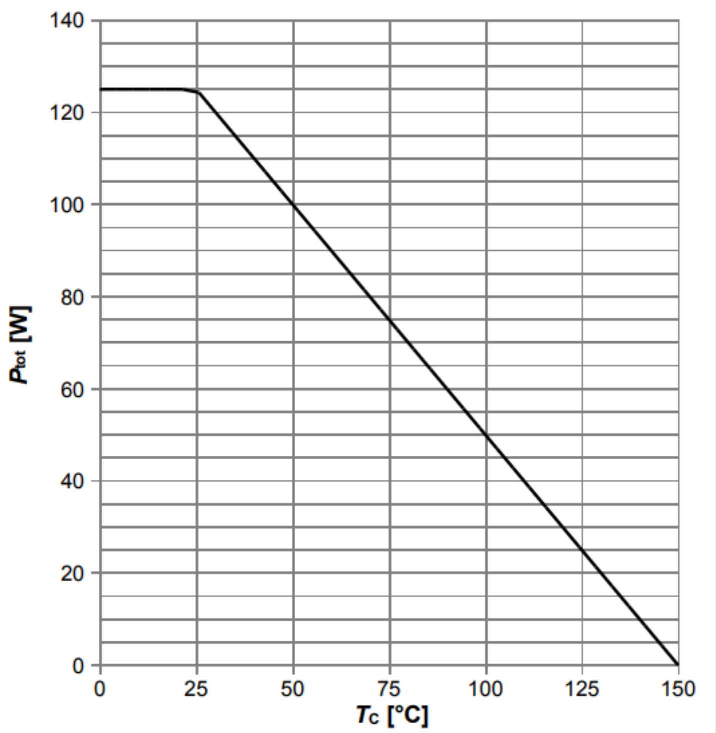
表 7 反向二极管

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	76	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	304	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.83	1.2	V	V_{GS}=0 V, I_F=38 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	24.3	48.6	ns	V_R=75 V, I_F=40 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	15.7	31.4	nC	V_R=75 V, I_F=40 A, di_F/dt=100 A/µs

[1)]由设计标定，不受制于生产测试。

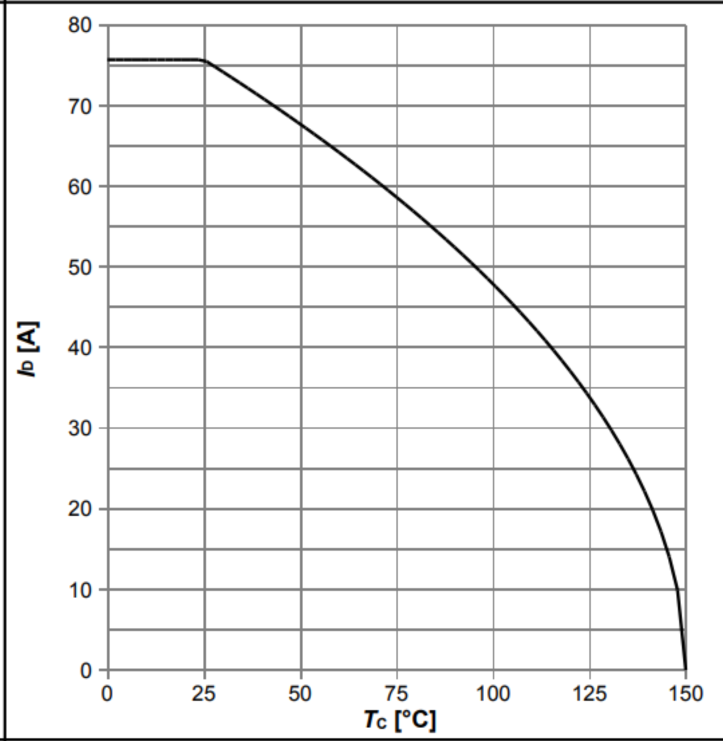
4 电气特性图

Diagram 1: Power dissipation



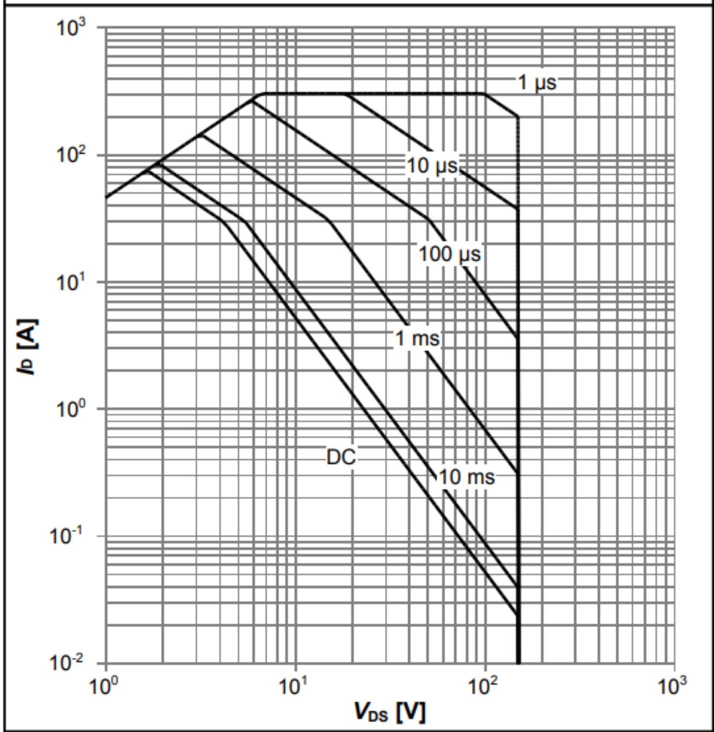
P_{tot}=f(T_C)

Diagram 2: Drain current



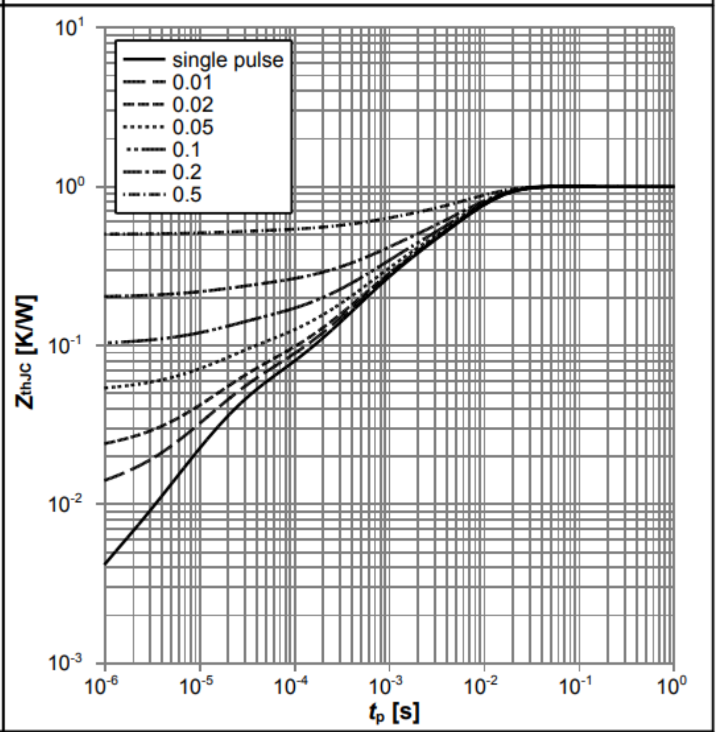
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



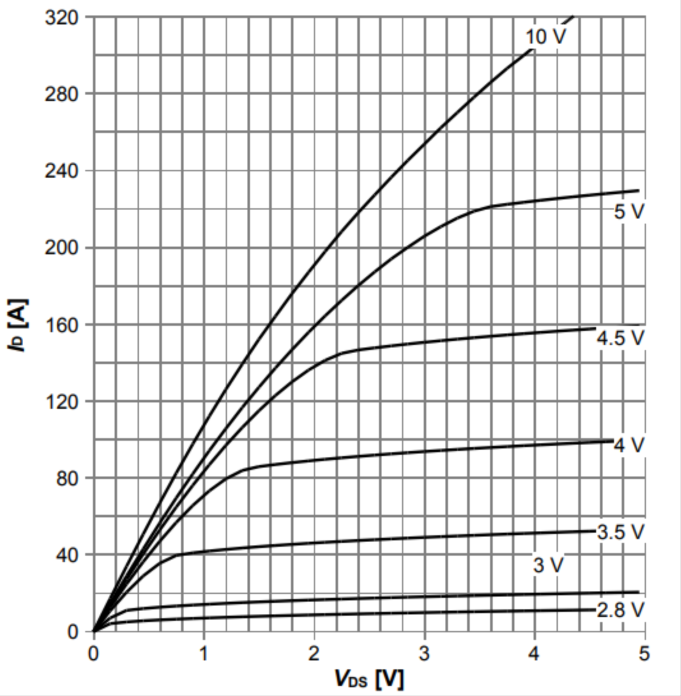
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



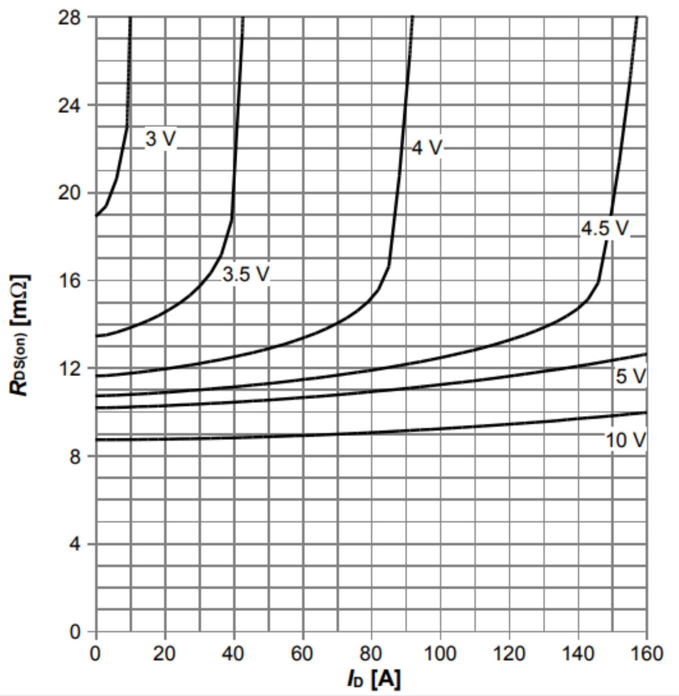
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



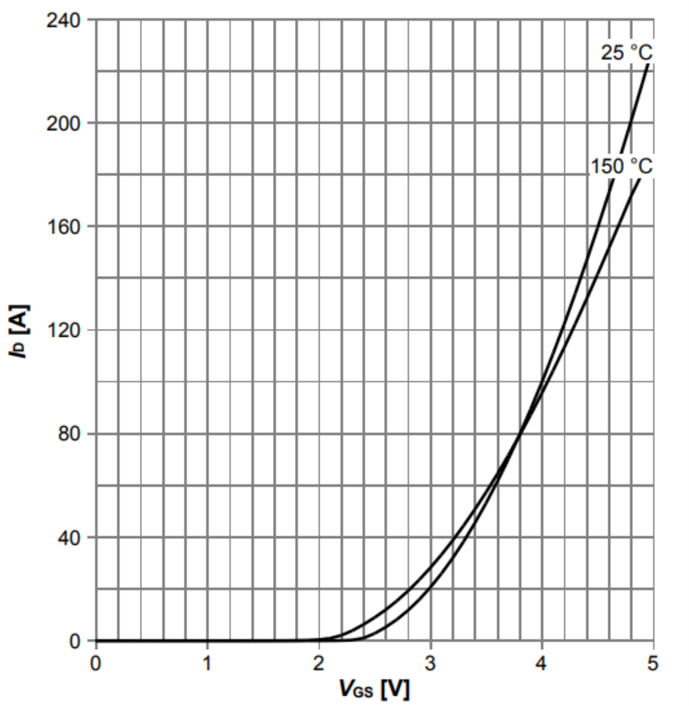
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



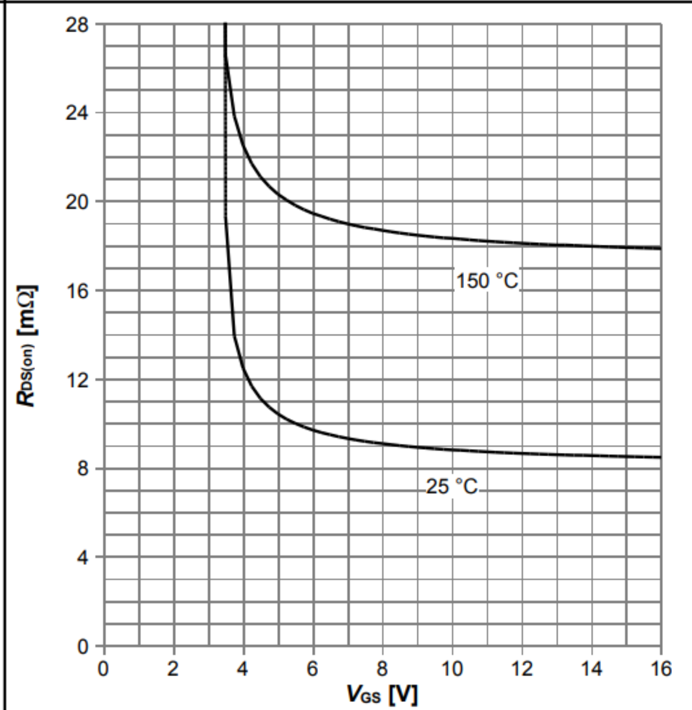
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



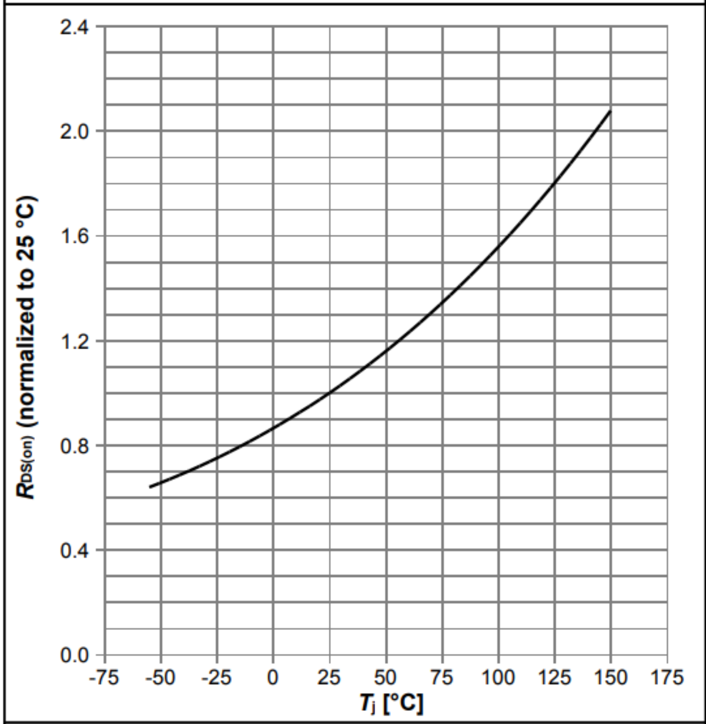
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



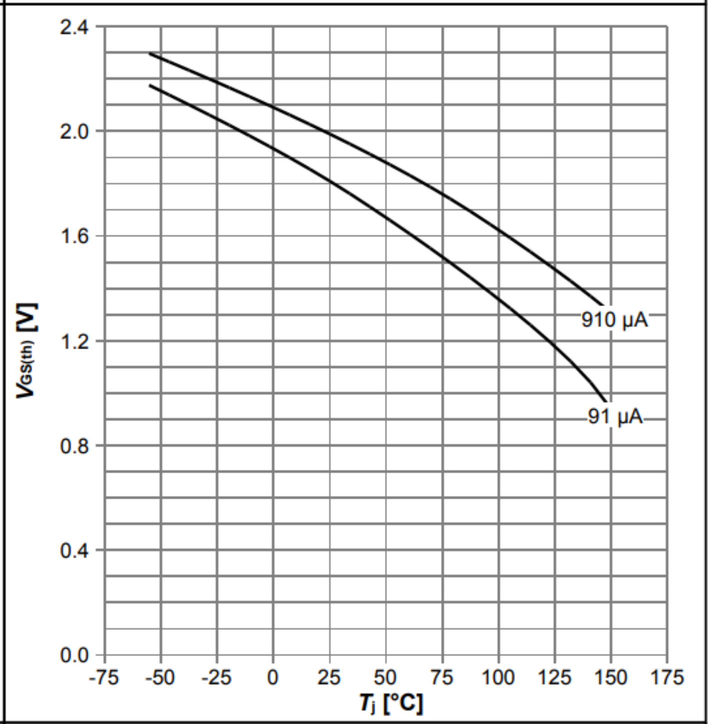
$R_{DS(on)}$=f(V_{GS}), I_D=40 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



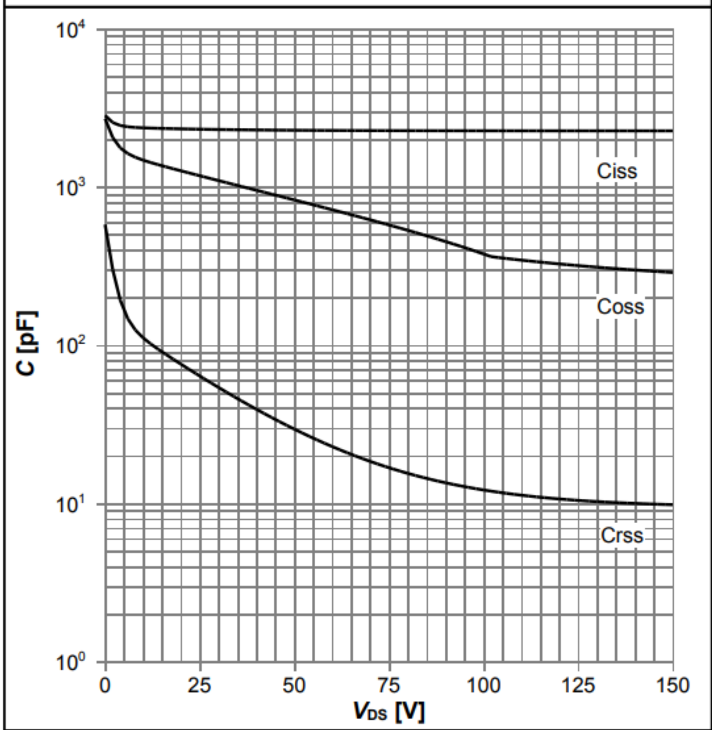
$R_{DS(on)}$=f(T_j), I_D=40 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



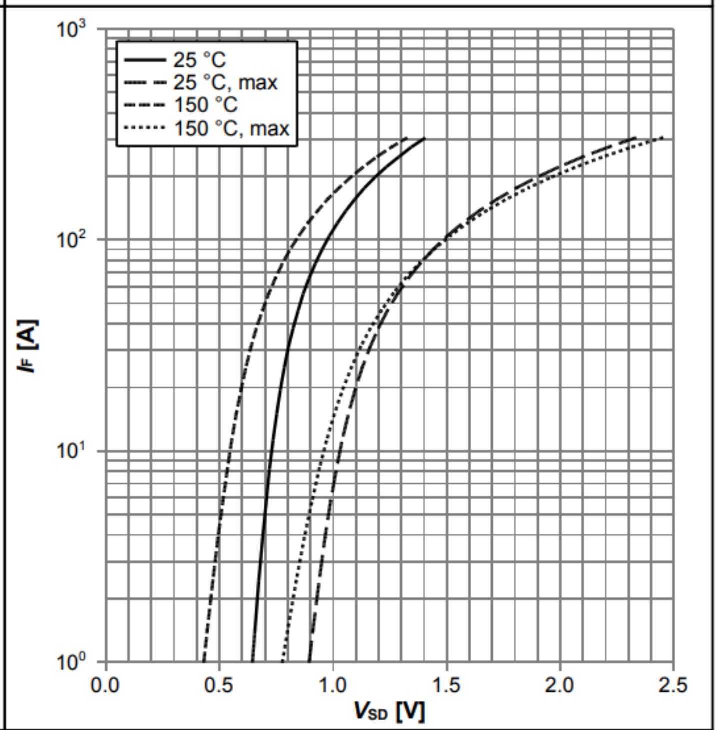
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



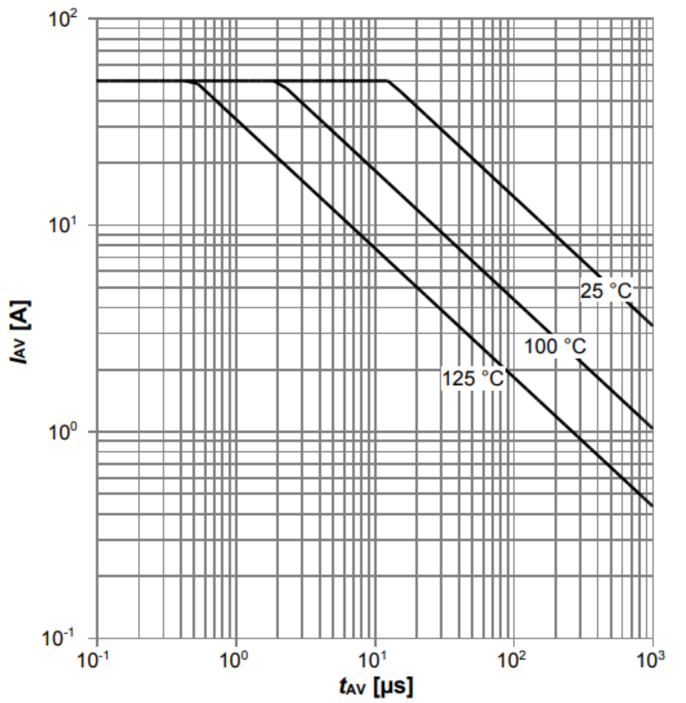
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



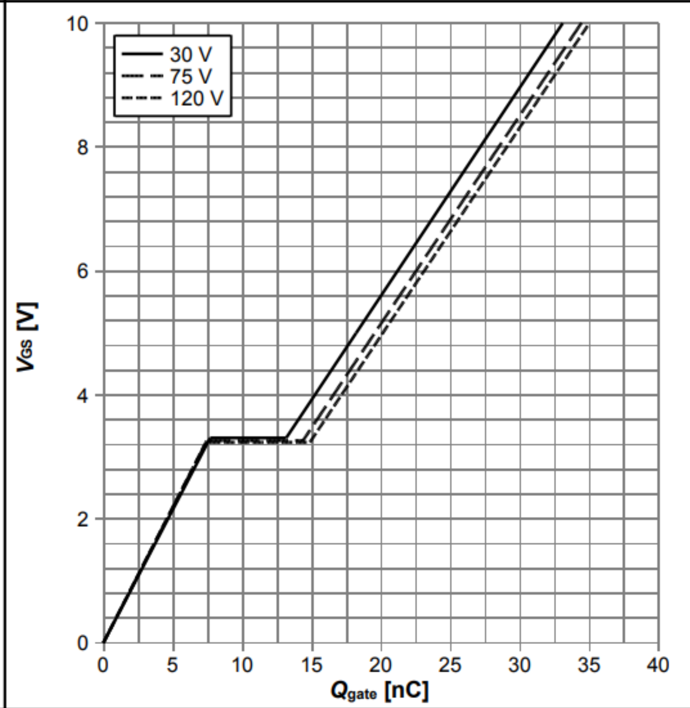
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



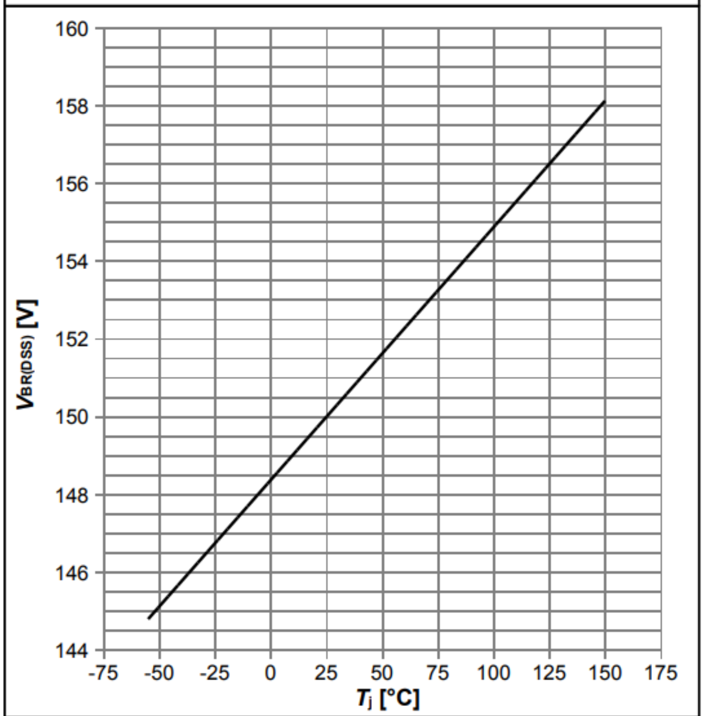
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



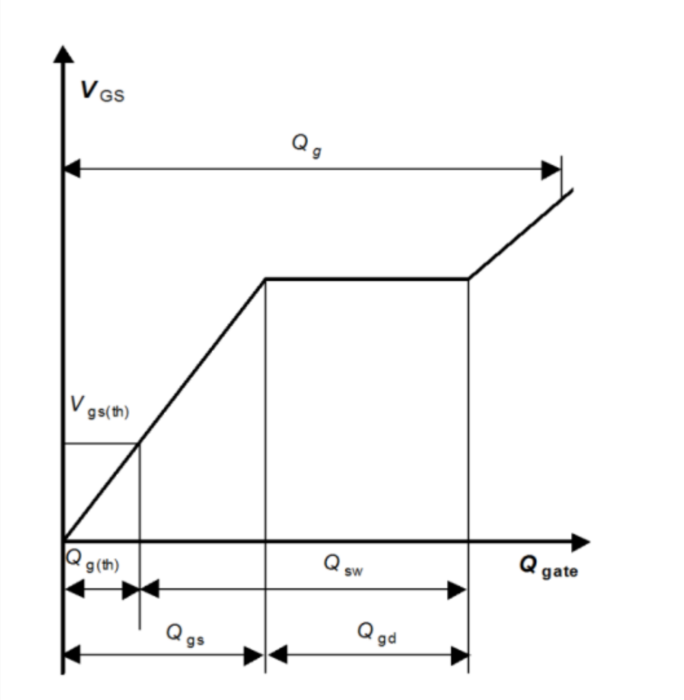
V_{GS}=f(Q_{gate}), I_D=40 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage

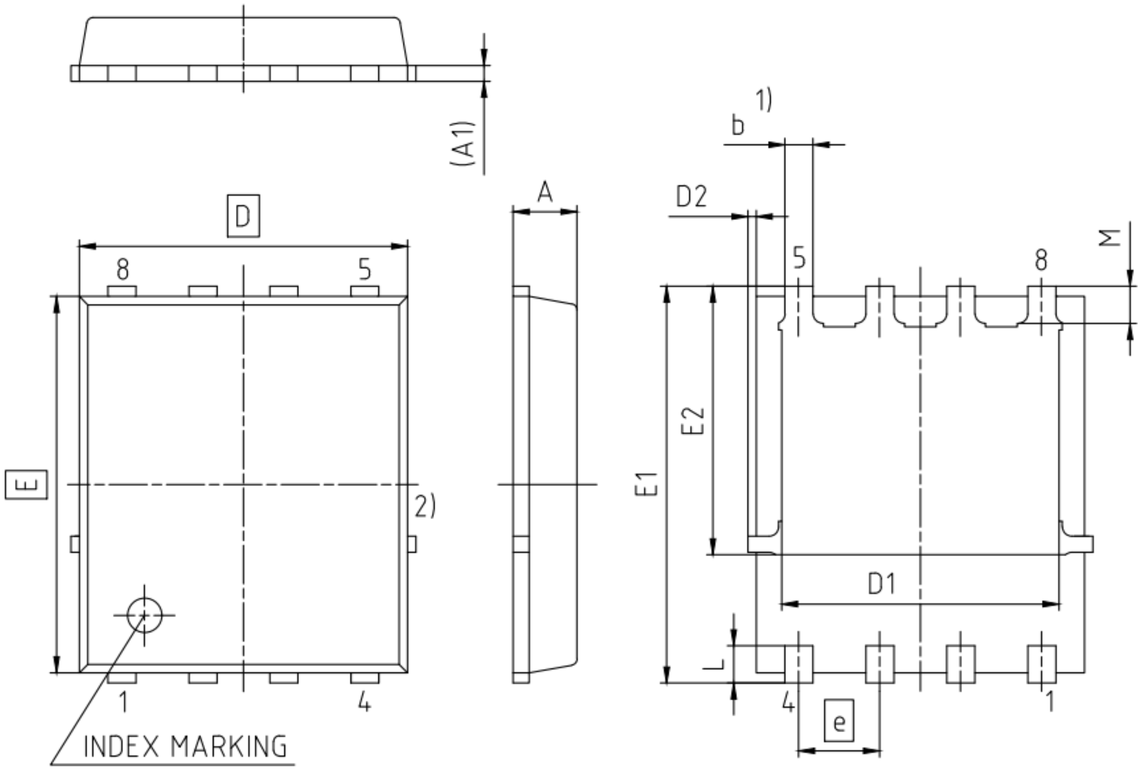


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 封装外形



1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

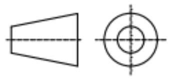
DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.00	0.22
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

DOCUMENT NO.
Z8B00003332

REVISION
08

SCALE 10:1
0 1 2 3mm

EUROPEAN PROJECTION



ISSUE DATE
05.11.2019

图1 **PG-TDSON-8 外形图，尺寸单位为毫米**

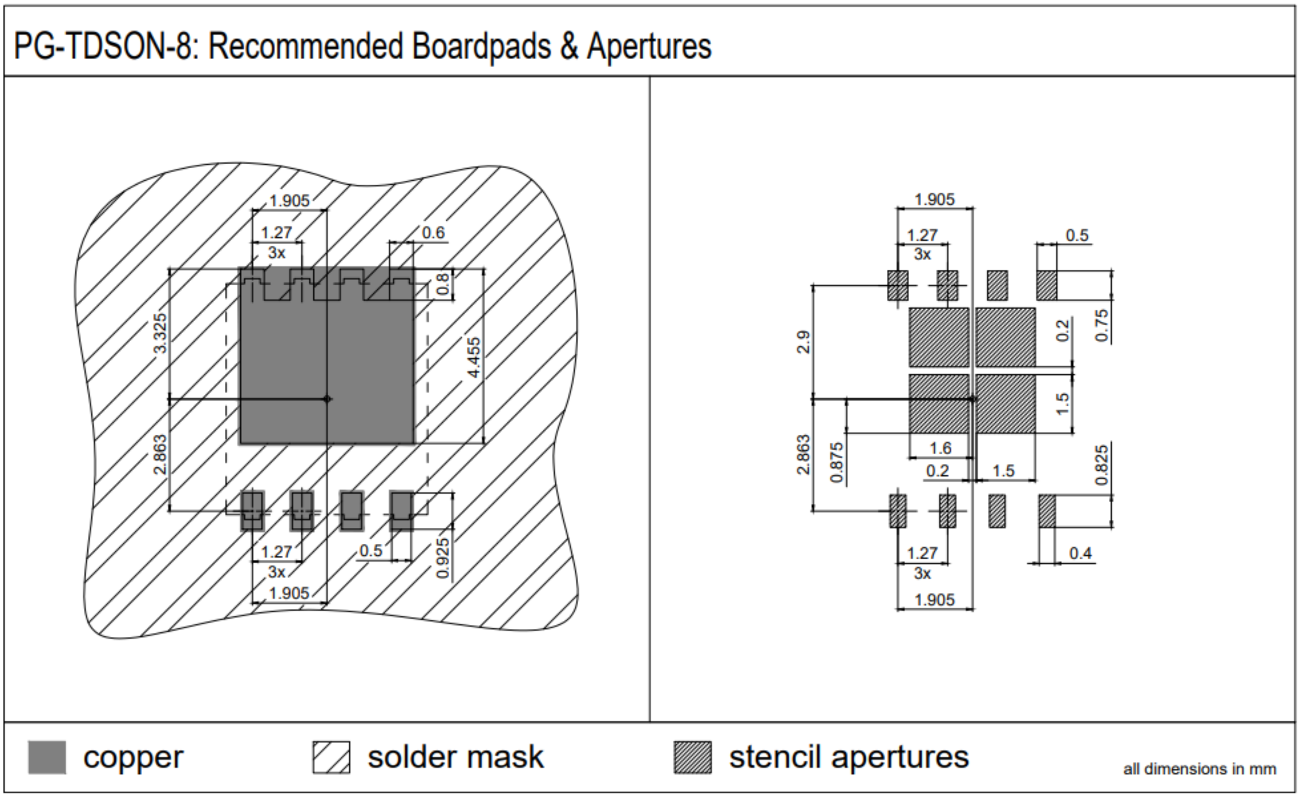


图2 外形板焊盘 (TDSON-8)，尺寸单位为毫米

修订记录

BSC105N15LS5

Revision: 2023-12-13, Rev. 2.0

历史修订版本

Revision	Date	Subjects (major changes since last revision)
2.0	2023-12-13	Release of final version

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