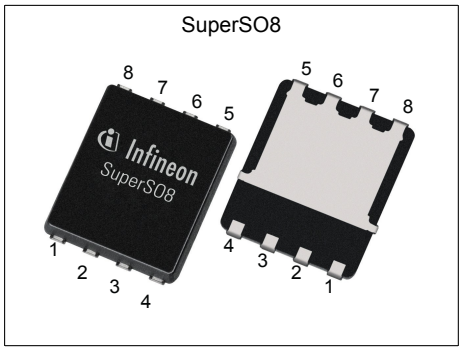
MOSFET

OptiMOS™ 5 Power-Transistor, 100 V



Features

- Optimized for high performance SMPS, e.g. Sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

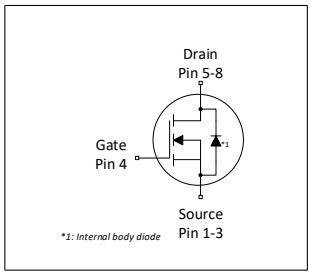


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	8.5	mΩ
I_D	70	A
Q_{oss}	35	nC
Q_G(0V..10V)	26	nC

Type / Ordering Code	Package	Marking	Related Links
BSC085N10NS5	PG-TDSON-8	085N10NS	-

Table of Contents

Description 1
Maximum ratings 3
Thermal characteristics 3
Electrical characteristics 4
Electrical characteristics diagrams 6
Package Outlines 10
Revision History 13
Trademarks 13
Disclaimer 13

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	70 44 13	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{THJA}=50 °C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	280	A	T_A=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	64	mJ	I_D=35 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	78 2.5	W	T_C=25 °C T_A=25 °C, R_{THJA}=50 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	-	1.6	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Device on PCB, 6 cm² cooling area[2]	R_{thJA}	-	-	50	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	V_{DS}=V_{GS}, I_D=38 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1.0 100	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	7.0 8.8	8.5 10.6	mΩ	V_{GS}=10 V, I_D=35 A V_{GS}=6 V, I_D=18 A
Gate resistance	R_G	-	1.2	1.8	Ω	-
Transconductance[1]	g_{fs}	33	66	-	S	|V_{DS}|≥2|I_D|$R_{DS(on)max}$, I_D=35 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	1800	2300	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	300	400	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	14	25	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	7.2	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=35 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	3.2	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=35 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	11	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=35 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	3.8	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=35 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	8.7	-	nC	V_{DD}=50 V, I_D=35 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	5.5	-	nC	V_{DD}=50 V, I_D=35 A, V_{GS}=0 to 10 V
Gate to drain charge[1]	Q_{gd}	-	5.5	9.3	nC	V_{DD}=50 V, I_D=35 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	8.8	-	nC	V_{DD}=50 V, I_D=35 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	26	33	nC	V_{DD}=50 V, I_D=35 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	V_{DD}=50 V, I_D=35 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	23	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1]	Q_{oss}	-	35	47	nC	V_{DS}=50 V, V_{GS}=0 V

[1] Defined by design. Not subject to production test.
[2] See ″Gate charge waveforms″ for parameter definition

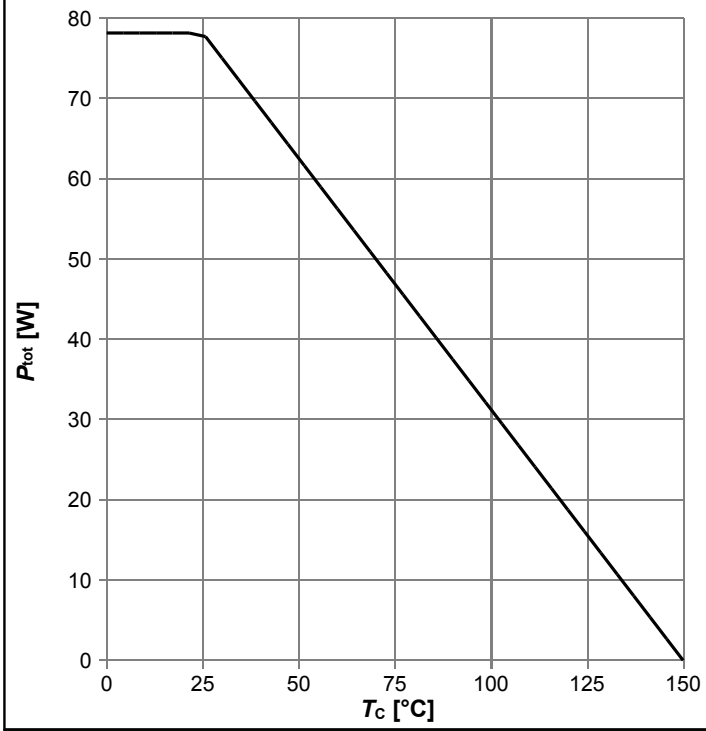
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	65	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	280	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.88	1.1	V	V_{GS}=0 V, I_F=35 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	39	78	ns	V_R=50 V, I_F=35 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	43	86	nC	V_R=50 V, I_F=35 A, di_F/dt=100 A/µs

[1)] Defined by design. Not subject to production test.

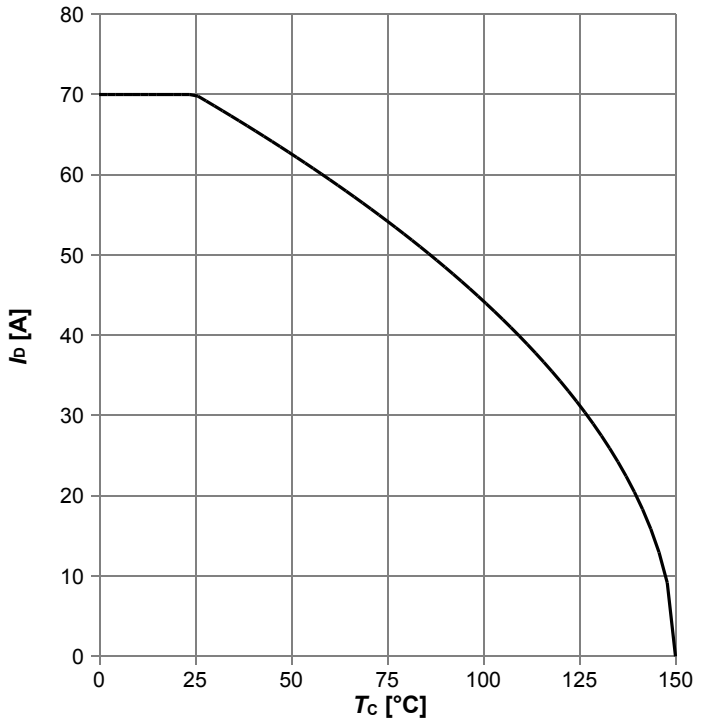
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



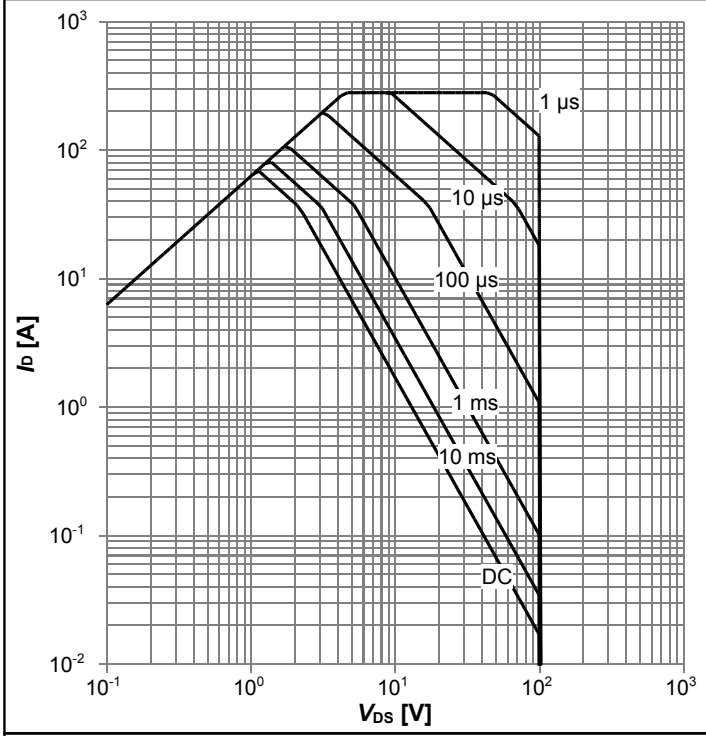
$P_{tot}=f(T_C)$

Diagram 2: Drain current



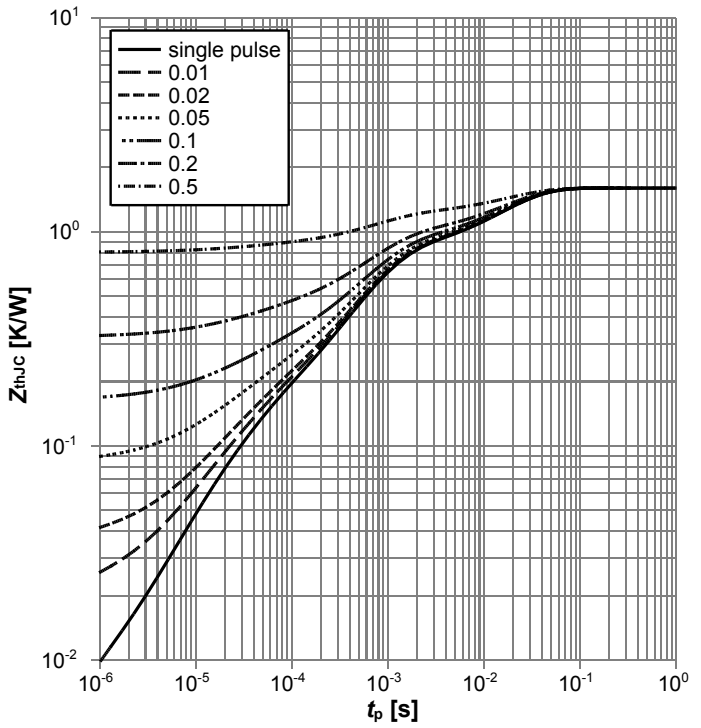
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



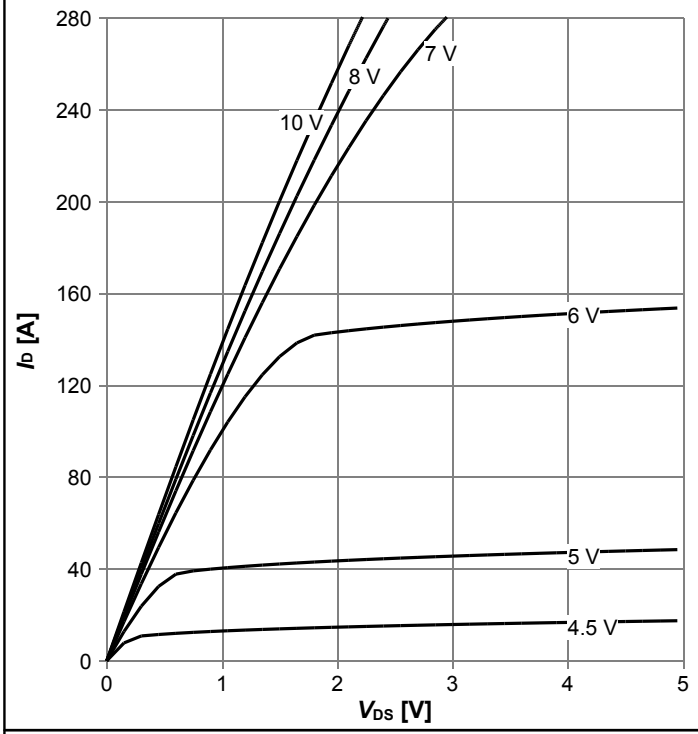
$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



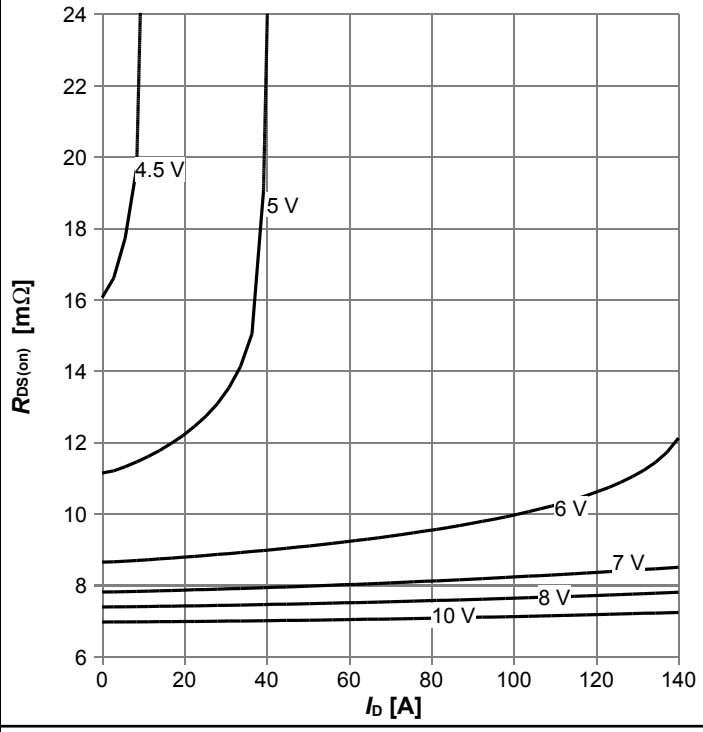
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



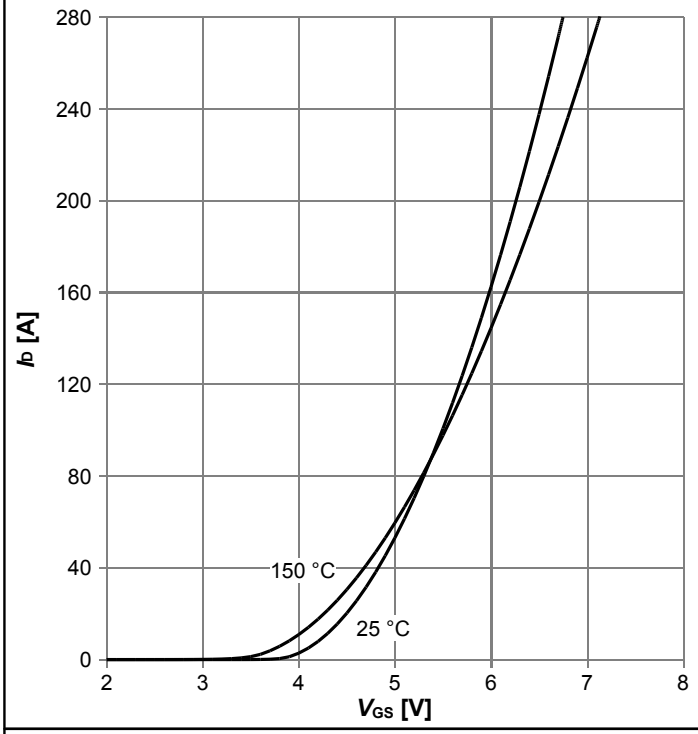
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



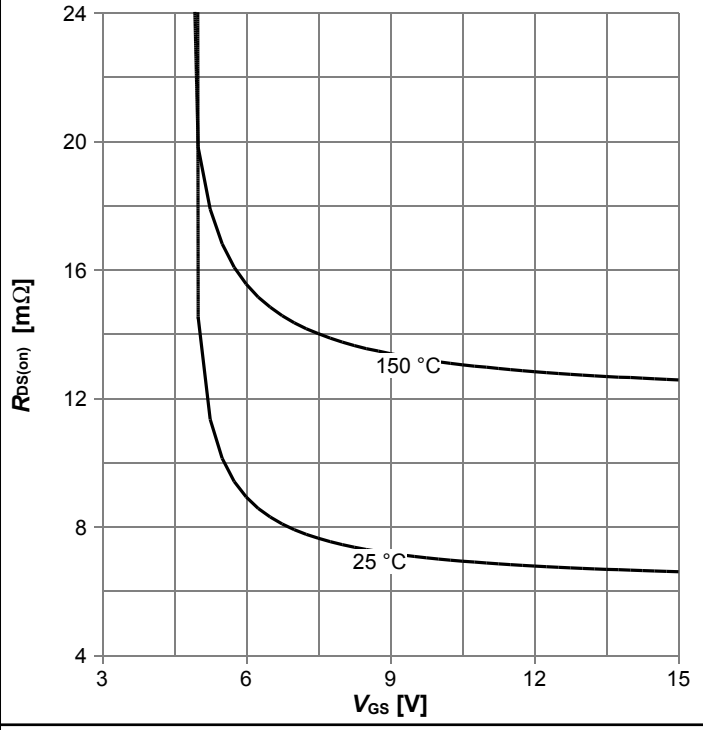
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



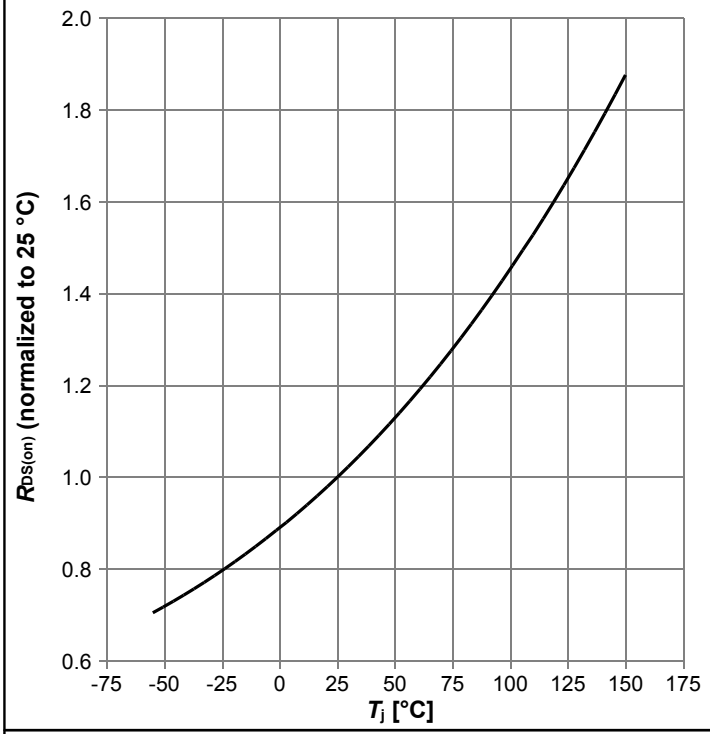
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



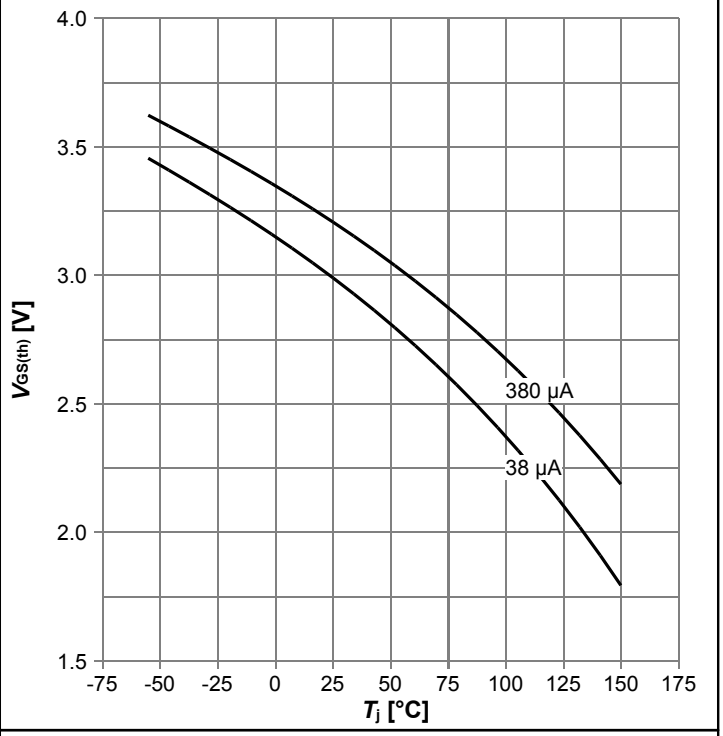
$R_{DS(on)}=f(V_{GS})$, $I_D=35$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



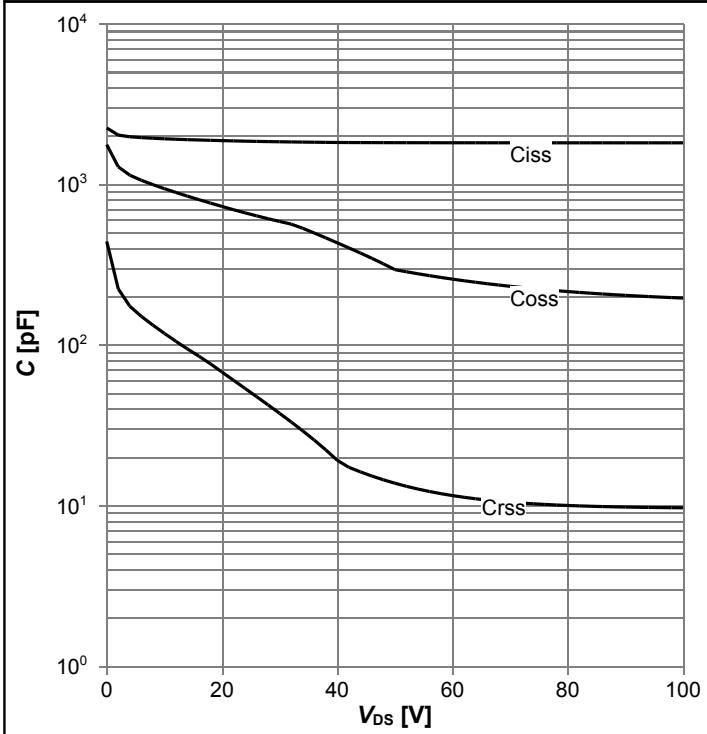
$R_{DS(on)}$=f(T_j), I_D=35 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



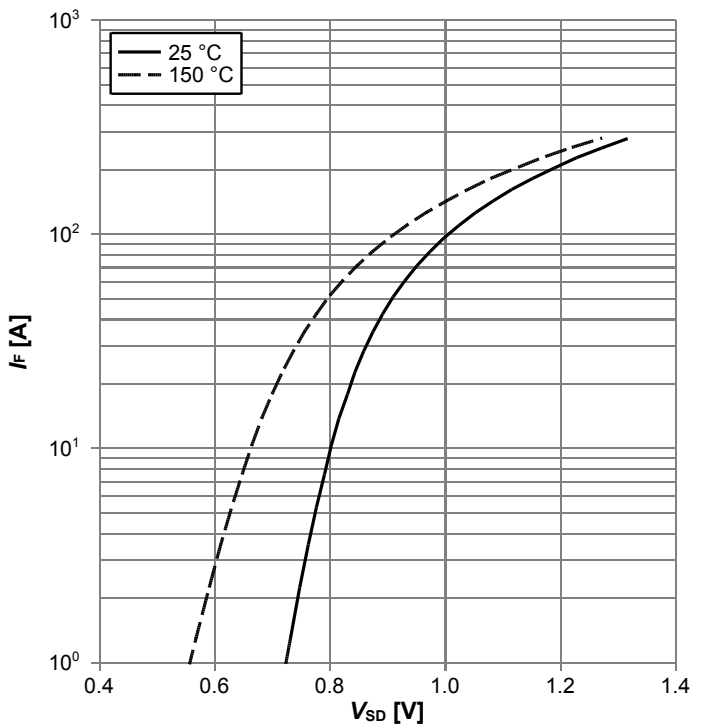
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



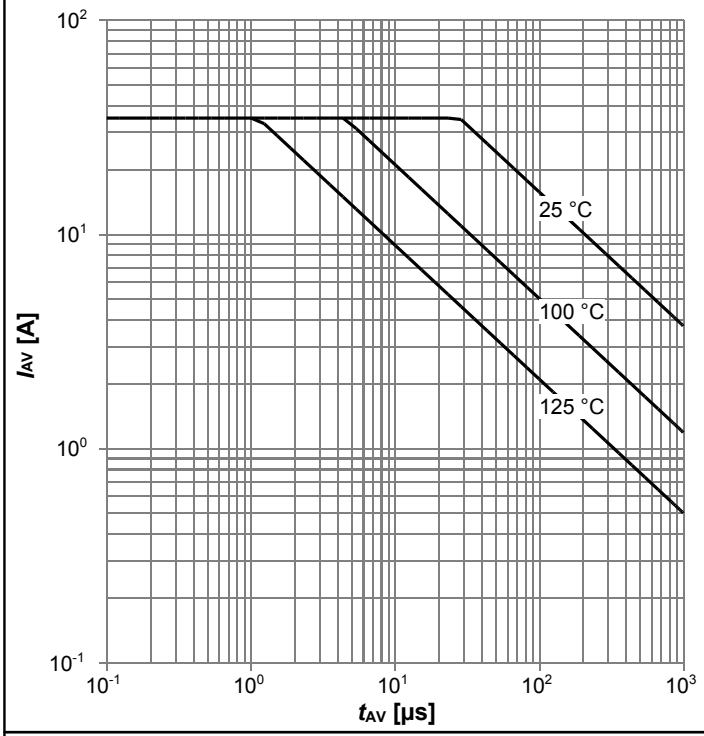
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Typ. forward characteristics of reverse diode



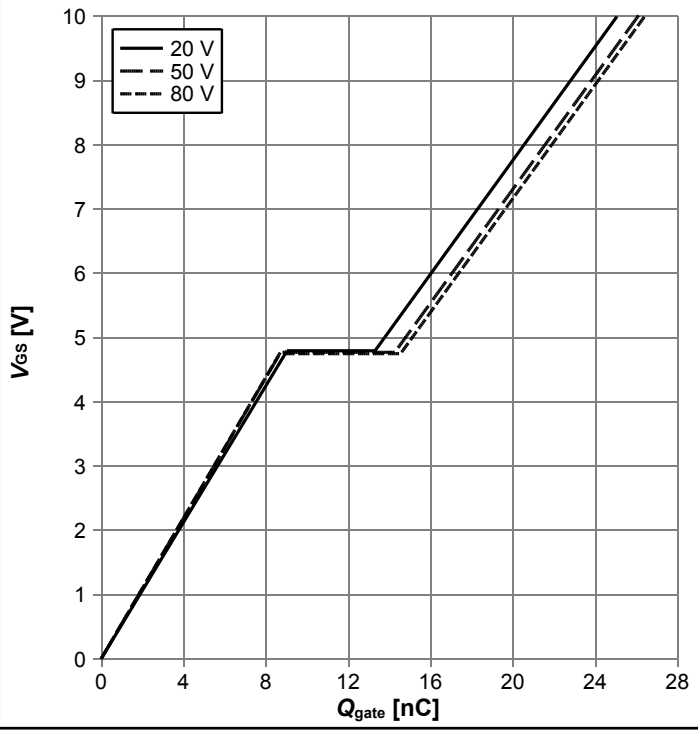
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



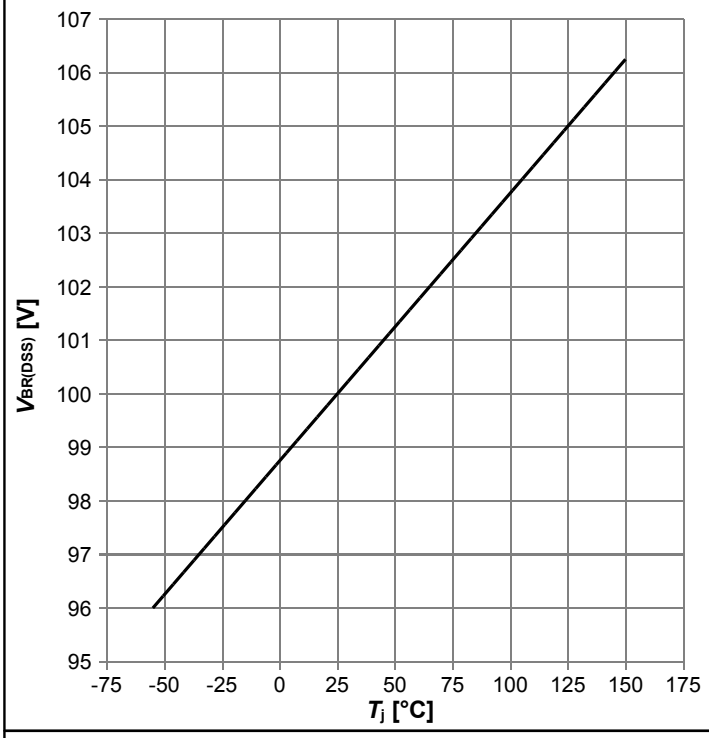
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



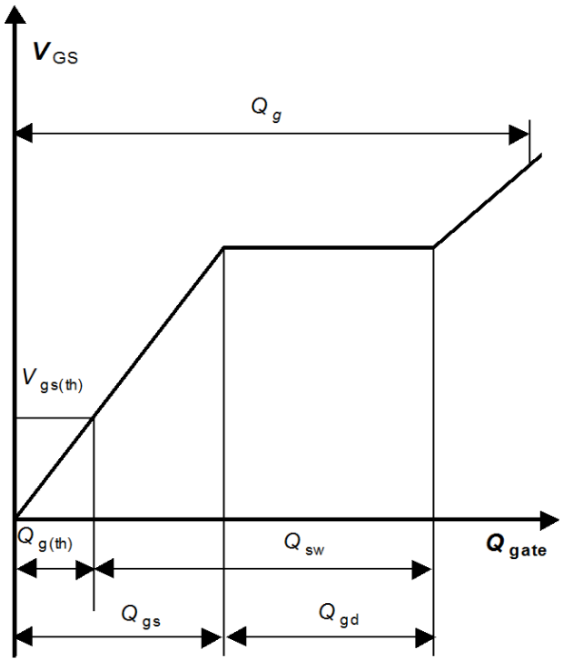
$V_{GS}=f(Q_{gate})$, $I_D=35$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

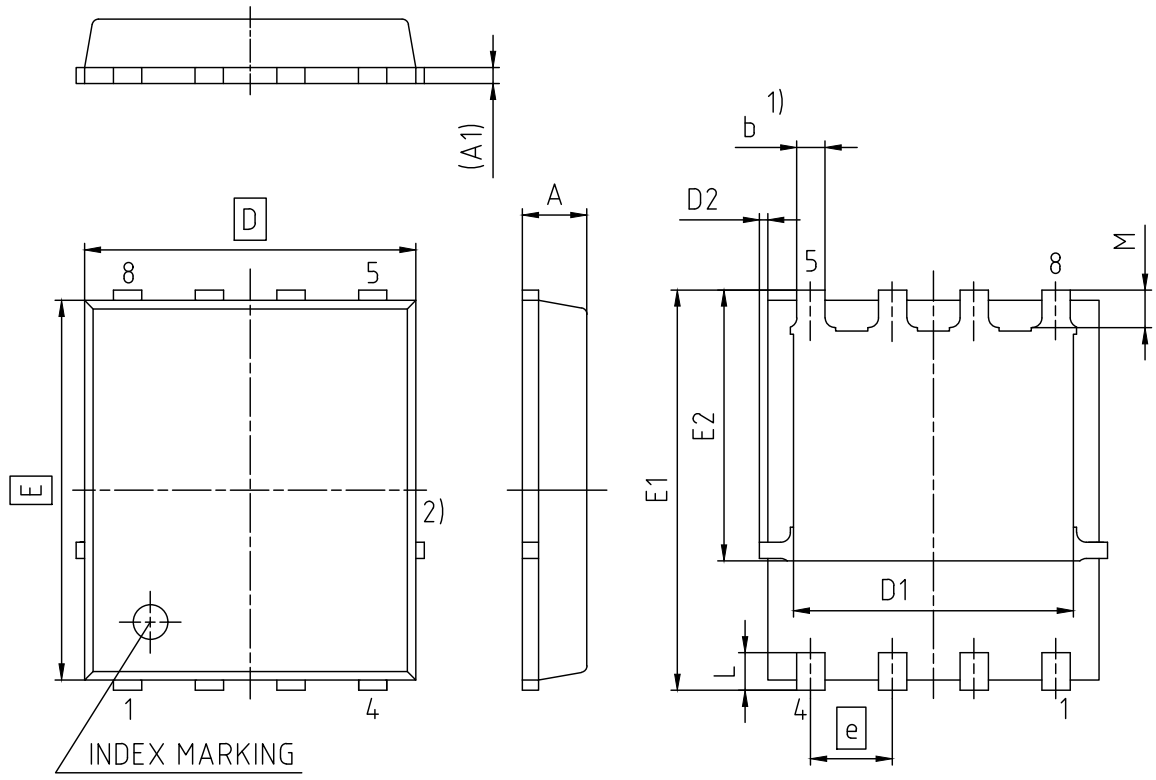


$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines

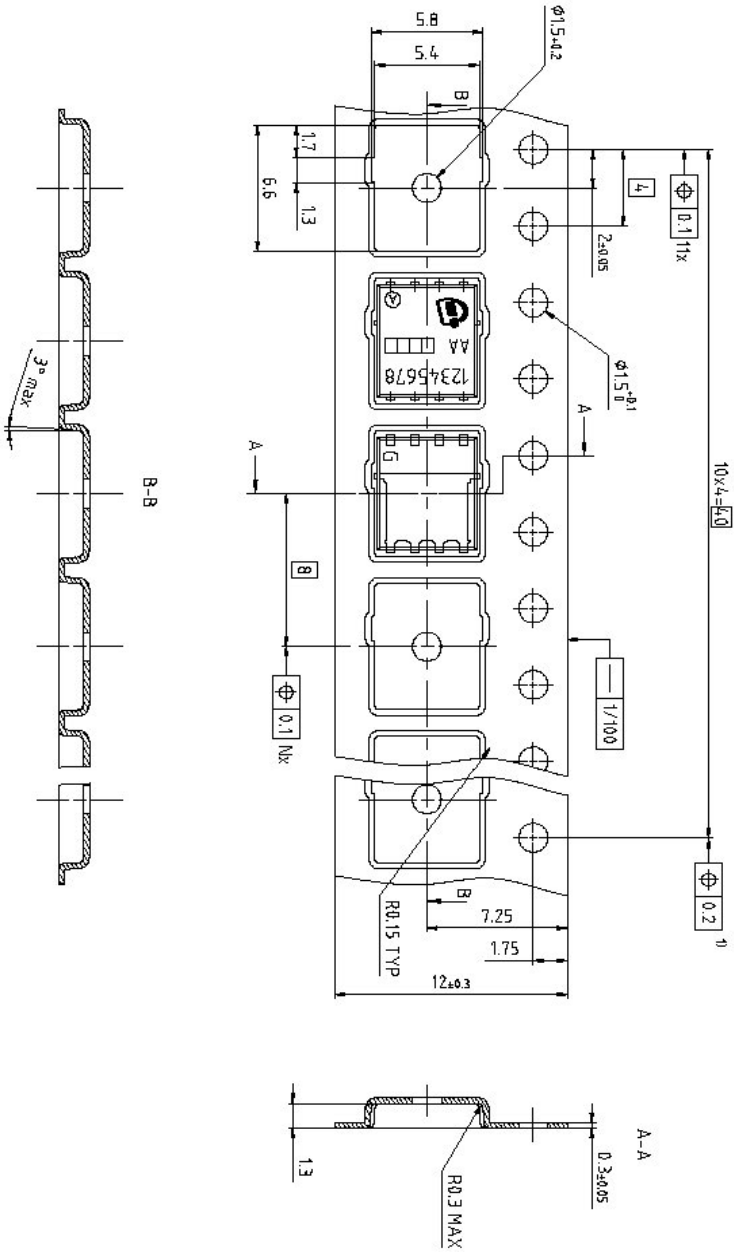


1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.00	0.22
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

DOCUMENT NO. Z8B00003332
REVISION 08
SCALE 10:1 0 1 2 3mm
EUROPEAN PROJECTION
ISSUE DATE 05.11.2019

Figure 1 Outline PG-TDSON-8, dimensions in mm



Dimension in mm

Figure 2 Outline Tape (TDSON-8)

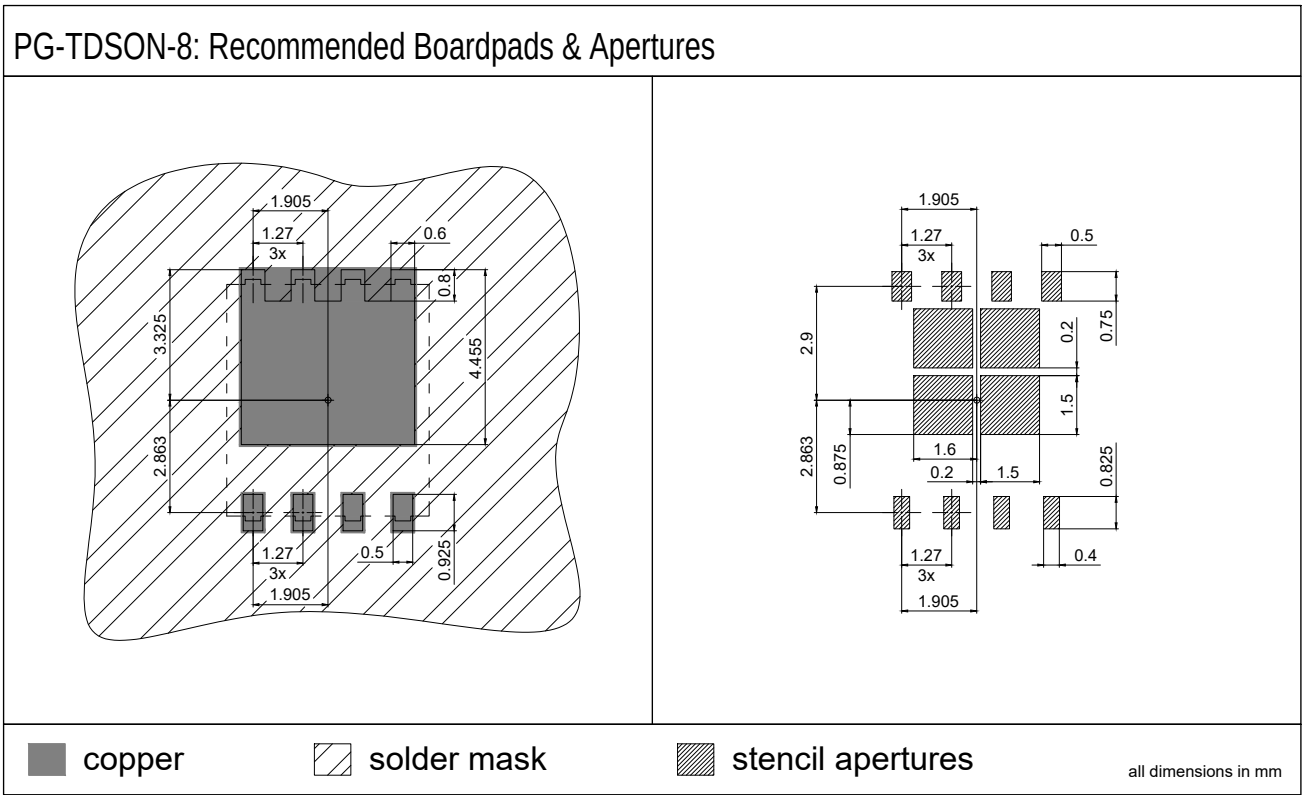


Figure 3 Outline Boardpads (TDSON-8), dimensions in mm

Revision History

BSC085N10NS5

Revision: 2022-06-23, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-06-23	Release of final version

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
erratum@infineon.com

Published by
Infineon Technologies AG
81726 München, Germany
© 2022 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”) .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.
In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.
The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Information
For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.