

英飞凌MOSFET功率晶体管

英飞凌BSC070N10LS5 OptiMOS™ 5 100 V 功率晶体管

特性

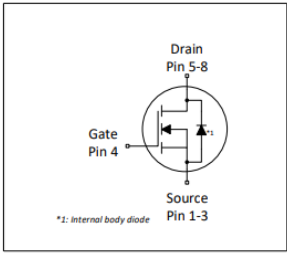
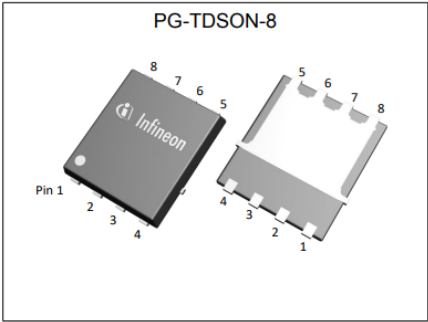
- 针对高性能 SMPS（例如同步整流）进行优化同步整流
- 100% 雪崩测试
- 卓越的耐热性
- N沟道，逻辑电平
- 无铅镀层；符合RoHS标准
- 符合 IEC61249-2-21 标准的无卤素

产品验证

完全符合 JEDEC 工业应用标准

表 1 主要性能参数

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	7	mΩ
I_D	79	A
Q_{oss}	41	nC
$Q_G(0V..4.5V)$	16	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
BSC070N10LS5	PG-TDSON-8	070N10L5	-

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1 最大额定值

除非另有规定, $T_A = 25\text{ °C}$

表 2 最大额定值

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	79 61 14	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}^{1)}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	318	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ³⁾	E_{AS}	-	-	55	mJ	$I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	83 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}^{2)}$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 热特性

表 3 热特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.9	1.5	°C/W	-
Device on PCB, 6 cm ² cooling area ¹⁾	R_{thJA}	-	-	50	°C/W	-

¹⁾ 器件位于 40 mm x 40 mm x 1.5 mm 环氧树脂 PCB FR4 上, 具有 6 cm² (一层, 70 µm 厚) 的铜面积用于漏极连接。PCB 在静止空气中垂直放置。

²⁾ 详细信息请参见图 3

³⁾ 详细信息请参见图 13

3 电气特性

除非另有规定, $T_j = 25\text{ °C}$

表4 静态特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.3	V	$V_{DS}=V_{GS}$, $I_D=49\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	6.0 7.7	7.0 8.5	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=40\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=20\text{ A}$
Gate resistance ¹⁾	R_G	-	1.0	1.5	Ω	-
Transconductance	g_{fs}	36	73	-	S	$ V_{DS} \geq I_D R_{DS(on)max}$, $I_D=40\text{ A}$

表5 动态特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	2100	2700	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	340	440	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	16	28	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	6.5	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=40\text{ A}$, $R_{G,ext}=3\text{ }\Omega$
Rise time	t_r	-	3.6	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=40\text{ A}$, $R_{G,ext}=3\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	20	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=40\text{ A}$, $R_{G,ext}=3\text{ }\Omega$
Fall time	t_f	-	5.3	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=40\text{ A}$, $R_{G,ext}=3\text{ }\Omega$

表6 栅极电荷特性²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	7	-	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	4	-	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	6	8	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	9	-	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	16	20	nC	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	3.2	-	V	$V_{DD}=50\text{ V}$, $I_D=40\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	26	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	41	54	nC	$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾由设计标定, 不受限于生产测试。

²⁾参数定义请参见“栅极电荷波形”

表 7 反向二极管

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	70	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	318	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.9	1.1	V	$V_{GS}=0\text{ V}$, $I_F=40\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	21	42	ns	$V_R=50\text{ V}$, $I_F=40\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	12	24	nC	$V_R=50\text{ V}$, $I_F=40\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾由设计标定，不受制于生产测试。

4 电气特性图

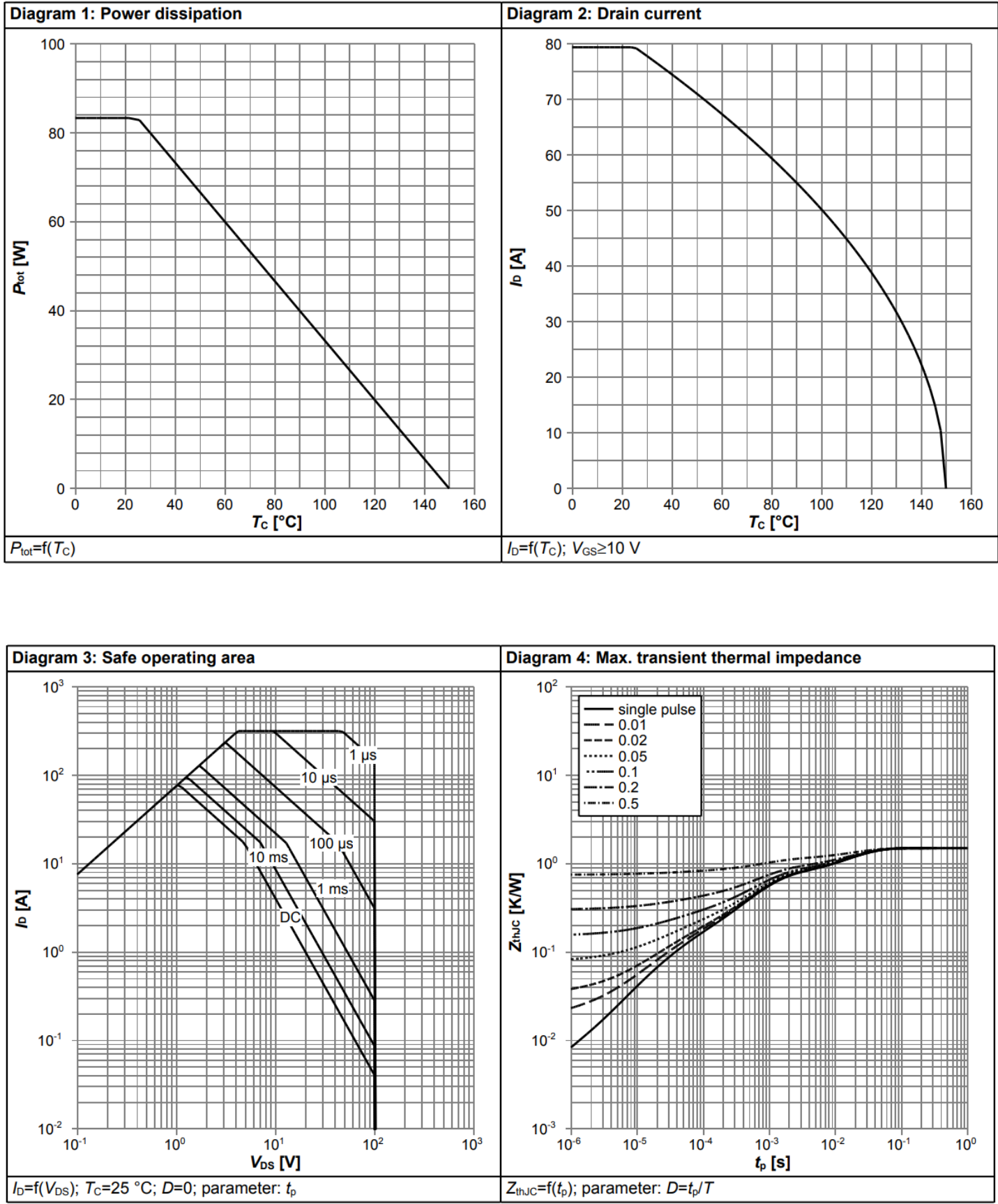
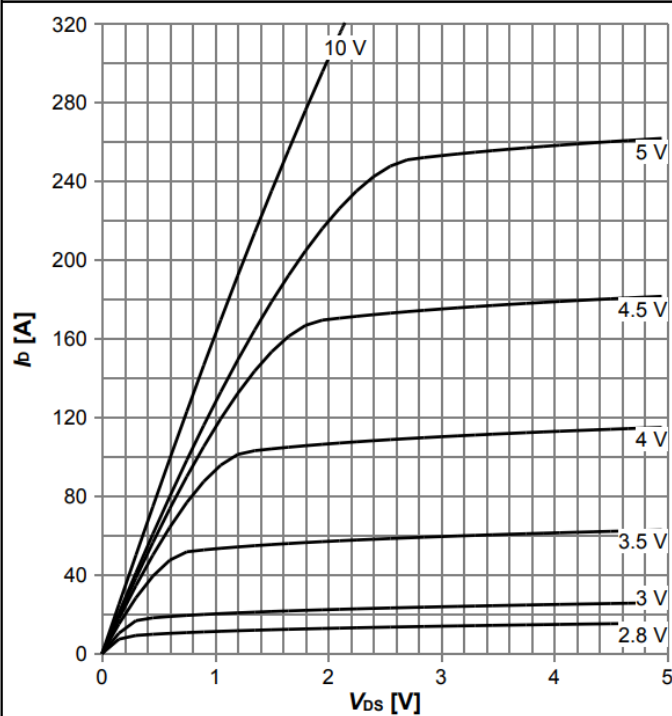
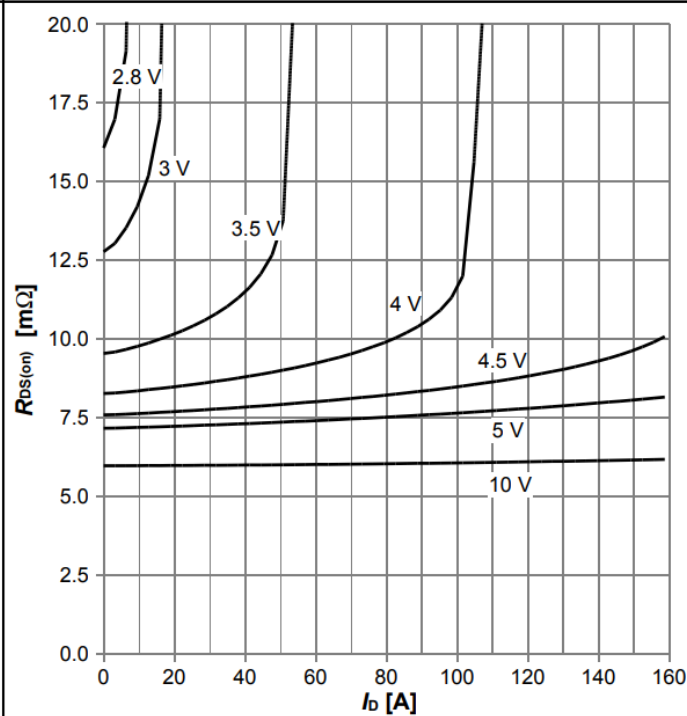


Diagram 5: Typ. output characteristics



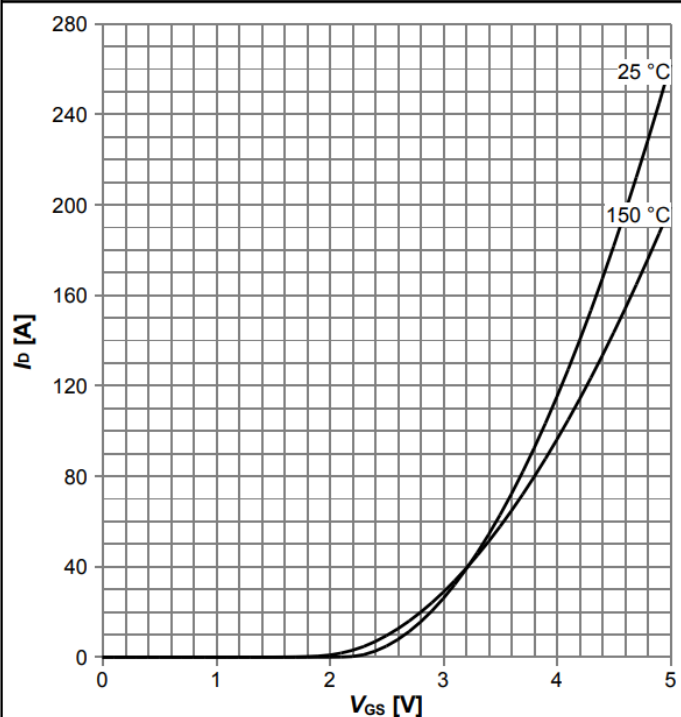
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



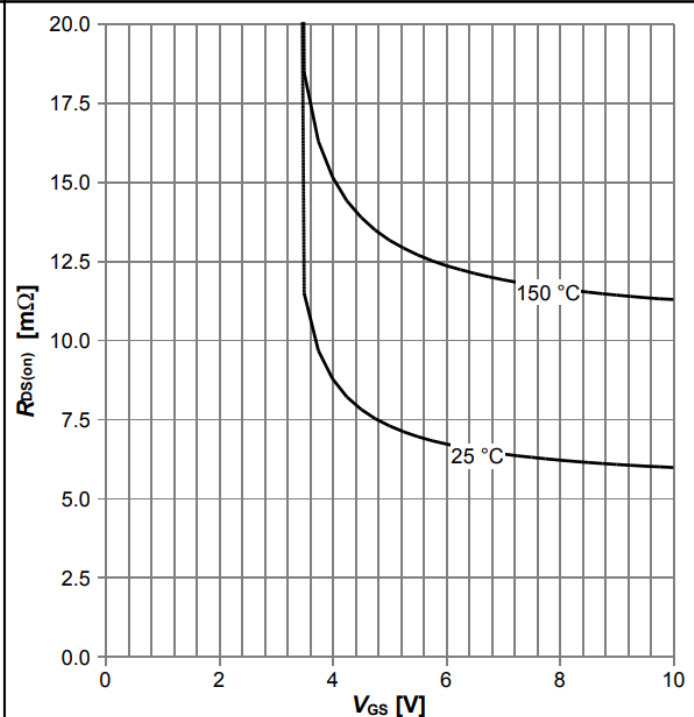
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



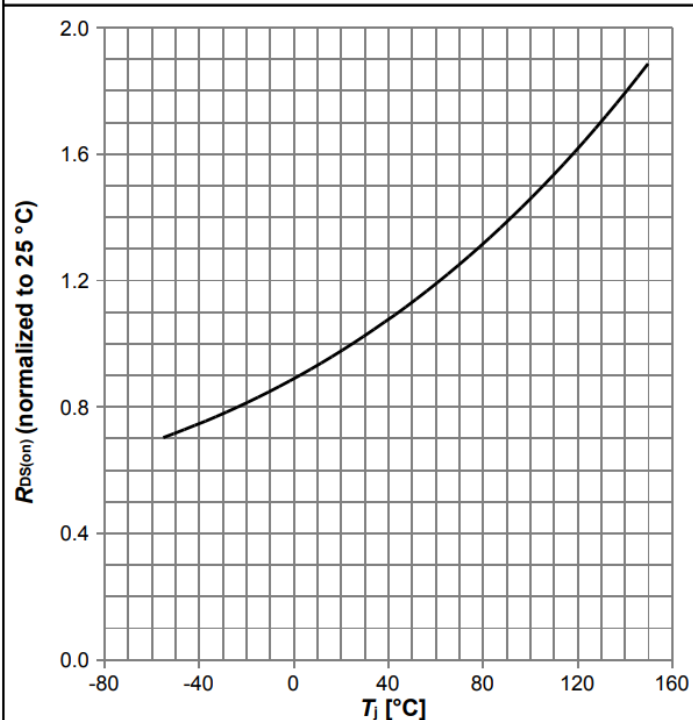
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



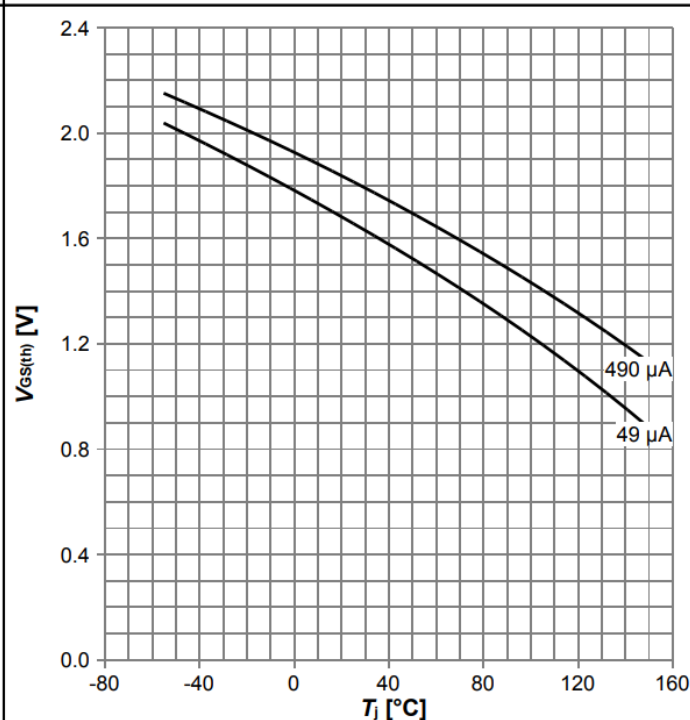
$R_{DS(on)} = f(V_{GS})$, $I_D = 40$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



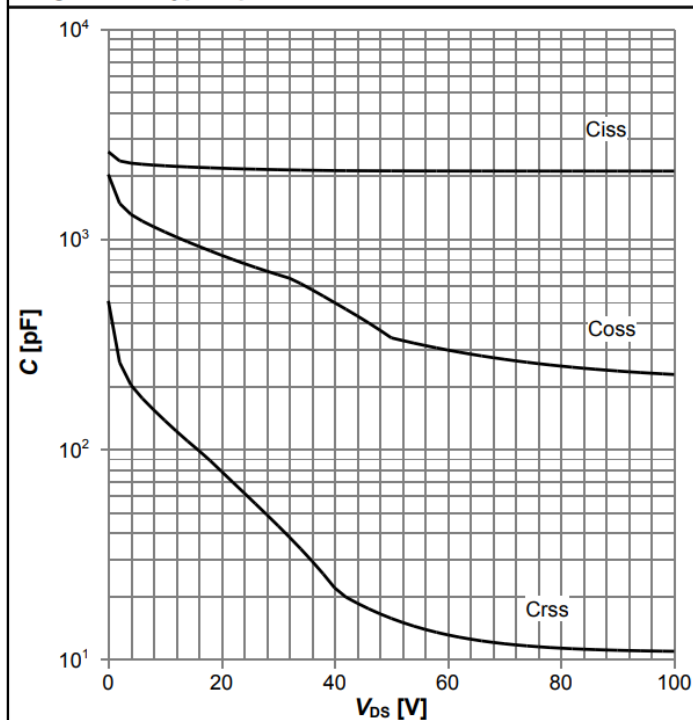
$R_{DS(on)} = f(T_j)$, $I_D = 40$ A, $V_{GS} = 10$ V

Diagram 10: Typ. gate threshold voltage



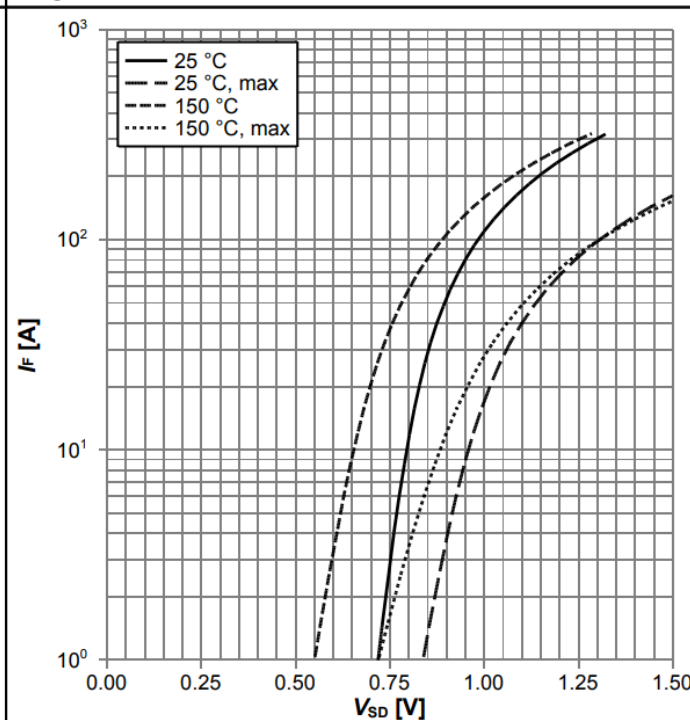
$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode

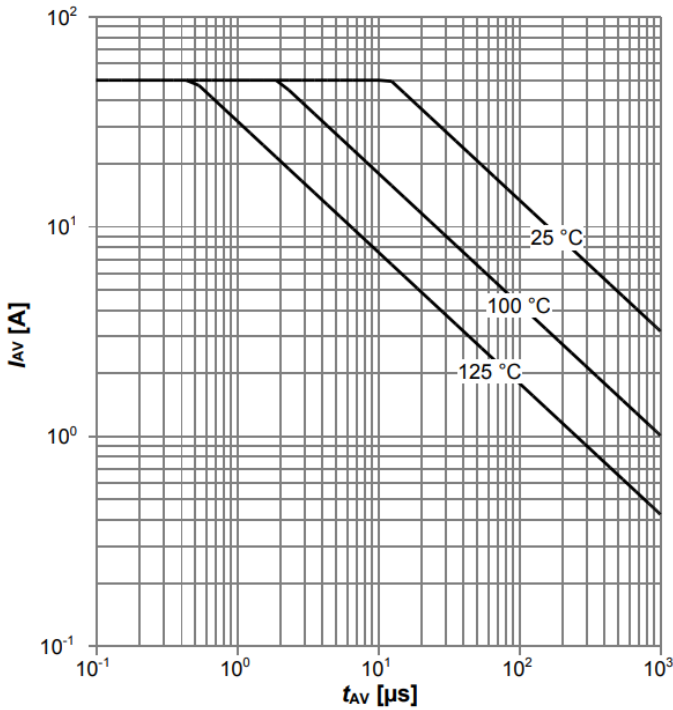


$I_F = f(V_{SD})$; parameter: T_j

OptiMOS™ 5 Power-Transistor, 100 V

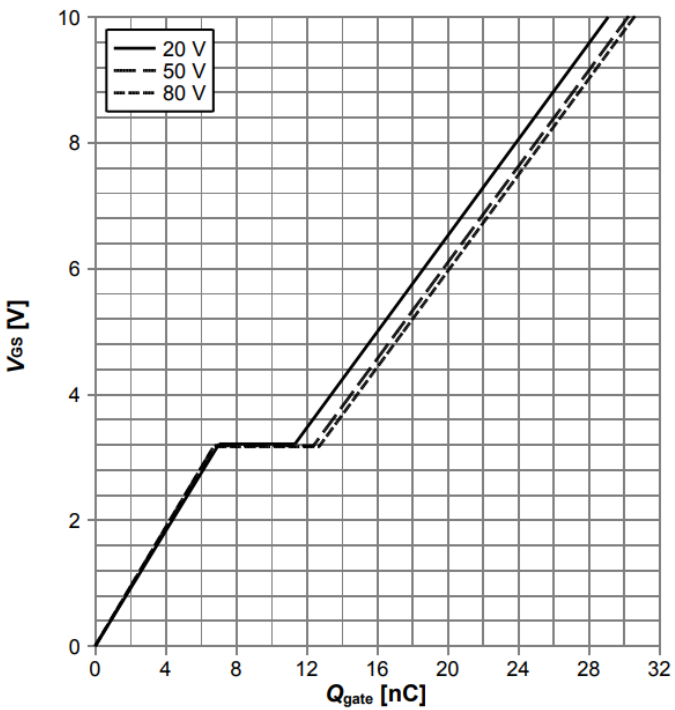
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Diagram 13: Avalanche characteristics



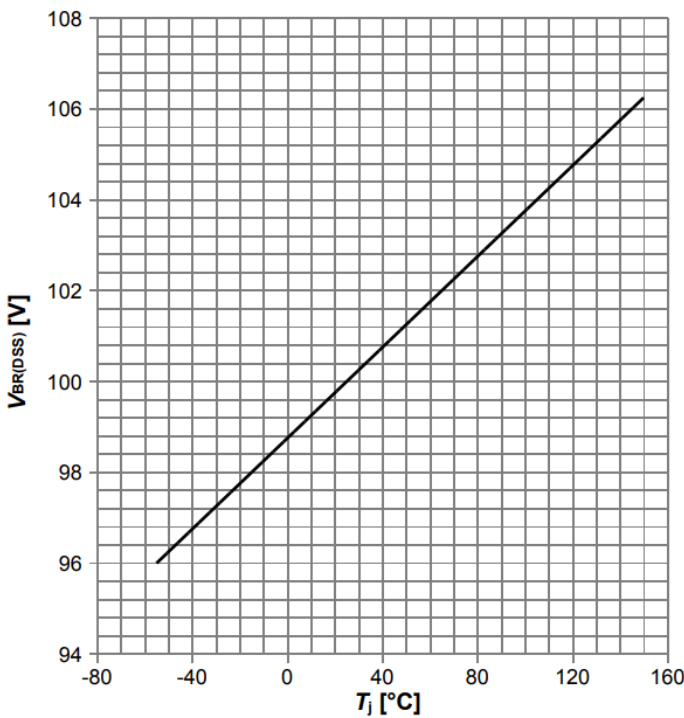
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



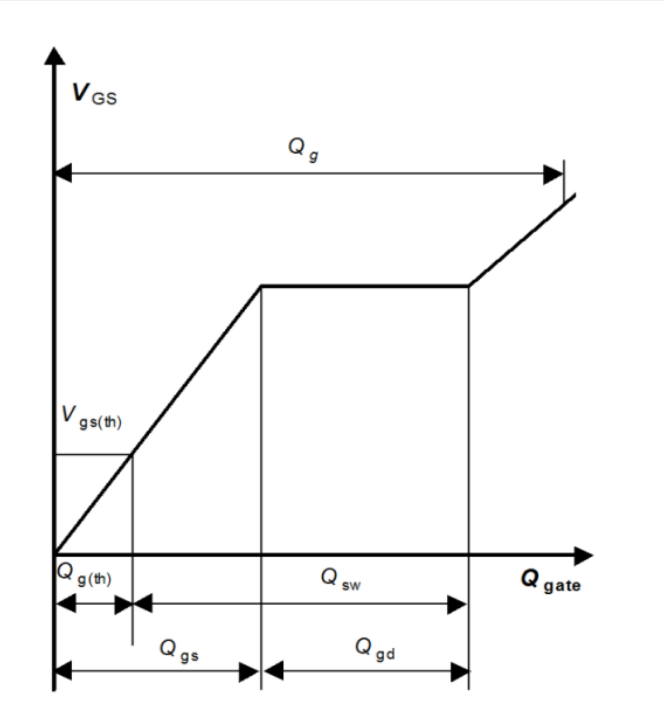
$V_{GS}=f(Q_{gate})$, $I_D=40\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

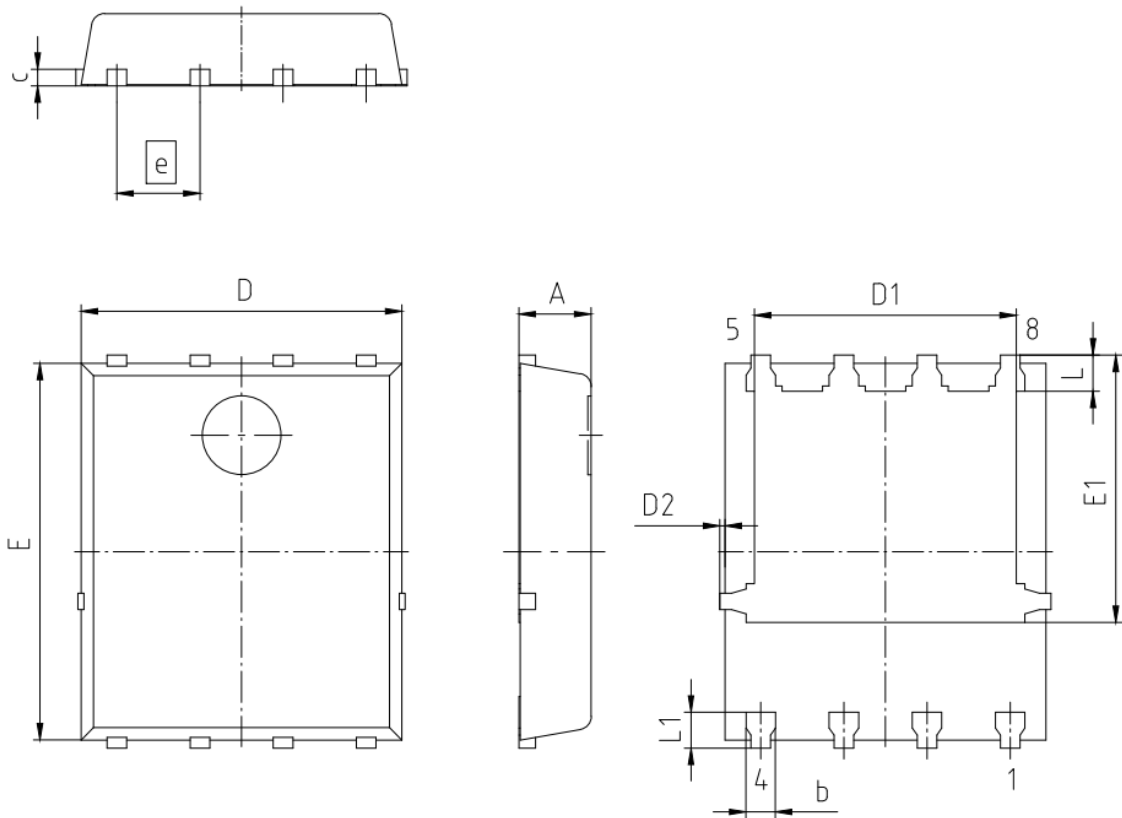


$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Diagram Gate charge waveforms



5 封装外形



PACKAGE - GROUP NUMBER: PG-TDSON-8-U08		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
b	0.34	0.54
c	0.15	0.35
D	4.80	5.35
D1	3.90	4.40
D2	0.00	0.22
E	5.70	6.10
E1	4.05	4.25
e	1.27	
L	0.45	0.65
L1	0.45	0.65

- 1) EXCLUDING MOLD FLASH
- 2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
- 3) ALL METAL SURFACES ARE PLATED,
EXCEPT AREA OF CUT

图 1 PG-TDSON-8 外形图，尺寸单位为毫米

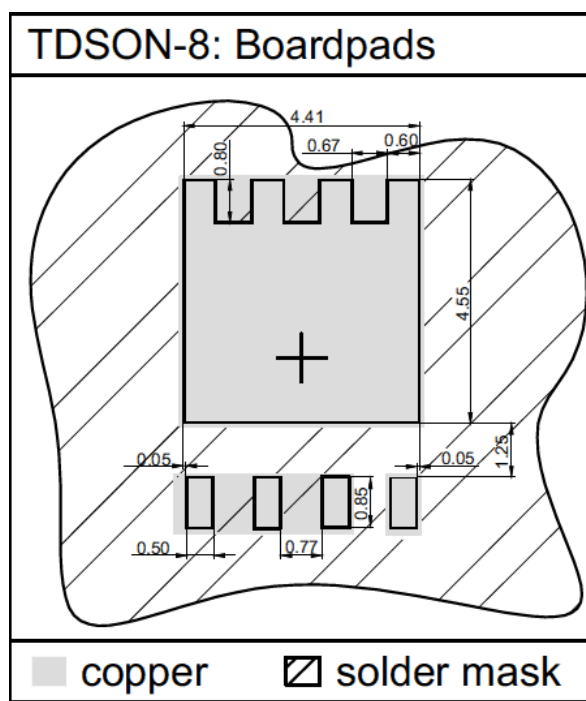


图 2 外形封装 (TDSON-8)

修订记录

BSC070N10LS5

Revision: 2023-03-08, Rev. 2.2

历史修订版本

Revision	Date	Subjects (major changes since last revision)
2.0	2019-04-01	Release of final version
2.1	2021-12-06	Update "Avalanche energy"
2.2	2023-03-08	Update package outline drawing

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