

英飞凌MOSFET功率晶体管

英飞凌BSC035N10NS5 OptiMOS™ 5 100 V功率晶体管

特性

- 针对高性能 SMPS（例如同步整流）进行优化同步整流
- 100% 雪崩测试
- 卓越的耐热性
- N沟道
- 符合 JEDEC ¹⁾目标应用要求
- 无铅镀层；符合RoHS标准
- 符合 IEC61249-2-21 标准的无卤素

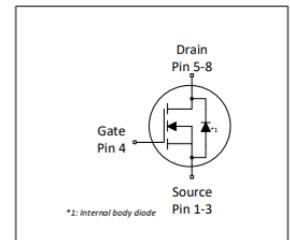
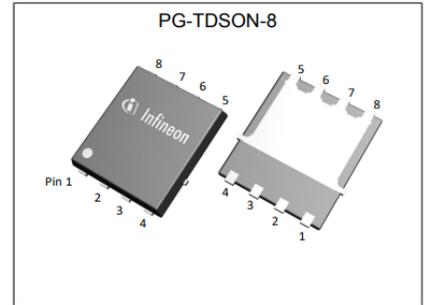


表 1 主要性能参数

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	3.5	mΩ
I_D	155	A
Q_{oss}	91	nC
$Q_G(0V..10V)$	70	nC



Type / Ordering Code	Package	Marking	Related Links
BSC035N10NS5	PG-TDSON-8	035N10NS	-

¹⁾ J-STD20 和 JESD22

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。为确认准确性，请务必访问 infineon.com 参考最新的英文版本（控制文档）。

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1 最大额定值

除非另有规定， $T_A = 25\text{ °C}$

表 2 最大额定值

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	155 98 19	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{K/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	620	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	398	mJ	$I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	156 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ K/W}^3)$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 热特性

表3 热特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.5	0.8	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	50	K/W	-

¹⁾额定值指产品仅具有数据表指定的绝对最大值，保持外壳温度符合规定要求。其他外壳温度请参见图 2。需要根据实际环境条件降低额定值。

²⁾器件位于 40 mm x 40 mm x 1.5 mm 环氧 PCB FR4 上，具有 6 cm²（一层，70 μm 厚）铜面积用于漏极连接。PCB 在静止空气中垂直放置。

³⁾详细信息请参见图 3

⁴⁾详细信息请参见图 13

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3 电气特性

除非另有规定， $T_j = 25\text{ °C}$

表4 静态特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}, I_D=115\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=100\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$ $V_{DS}=100\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.9 3.5	3.5 4.7	$\text{m}\Omega$	$V_{GS}=10\text{ V}, I_D=50\text{ A}$ $V_{GS}=6\text{ V}, I_D=25\text{ A}$
Gate resistance	R_G	-	1.5	2.3	Ω	-
Transconductance	g_{fs}	65	130	-	S	$ V_{DS} > 2 I_D R_{DS(on)max}, I_D=50\text{ A}$

表5 动态特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	5000	6500	pF	$V_{DS}=0\text{ V}, V_{GS}=50\text{ V}, f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	770	1000	pF	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V}, f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{riss}	-	34	60	pF	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V}, f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	22	-	ns	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A},$ $R_{G,ext}=3\text{ }\Omega$
Rise time	t_r	-	13	-	ns	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A},$ $R_{G,ext}=3\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	47	-	ns	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A},$ $R_{G,ext}=3\text{ }\Omega$
Fall time	t_f	-	15	-	ns	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V}, I_D=50\text{ A},$ $R_{G,ext}=3\text{ }\Omega$

表6 栅极电荷特性²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	22	-	nC	$V_{DD}=50\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{G(th)}$	-	14	-	nC	$V_{DD}=50\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	14	21	nC	$V_{DD}=50\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	23	-	nC	$V_{DD}=50\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	70	87	nC	$V_{DD}=50\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	$V_{DD}=50\text{ V}, I_D=50\text{ A}, V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	61	-	nC	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	91	121	nC	$V_{DD}=50\text{ V}, V_{GS}=0\text{ V}$

¹⁾由设计标定，不受制于生产测试。

²⁾参数定义请参见“栅极电荷波形”

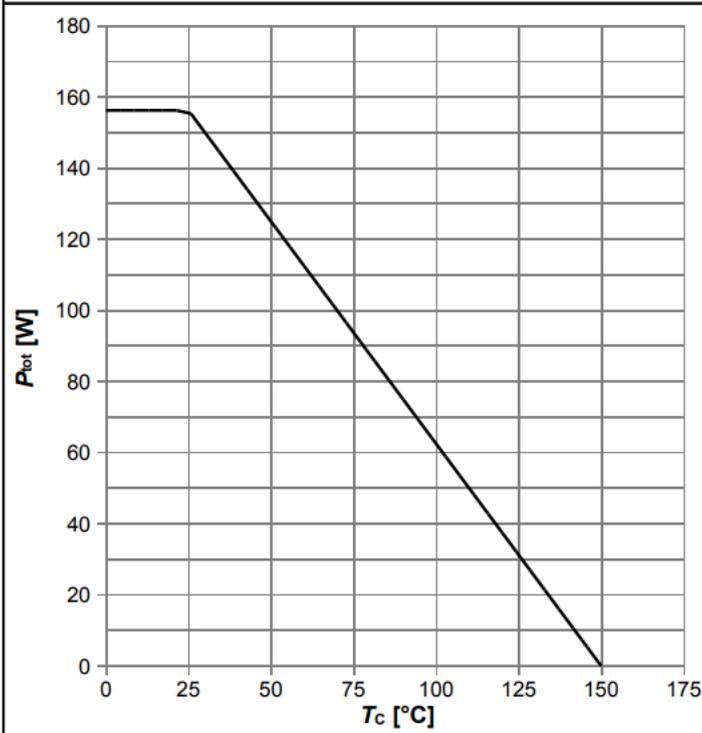
表 7 反向二极管

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	117	A	$T_C=25\text{ }^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$	-	-	620	A	$T_C=25\text{ }^\circ\text{C}$
Diode forward voltage	V_{SD}	-	0.82	1.1	V	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_J=25\text{ }^\circ\text{C}$
Reverse recovery time ¹⁾	t_{rr}	-	62	124	ns	$V_R=50\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	122	244	nC	$V_R=50\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾由设计标定，不受制于生产测试。

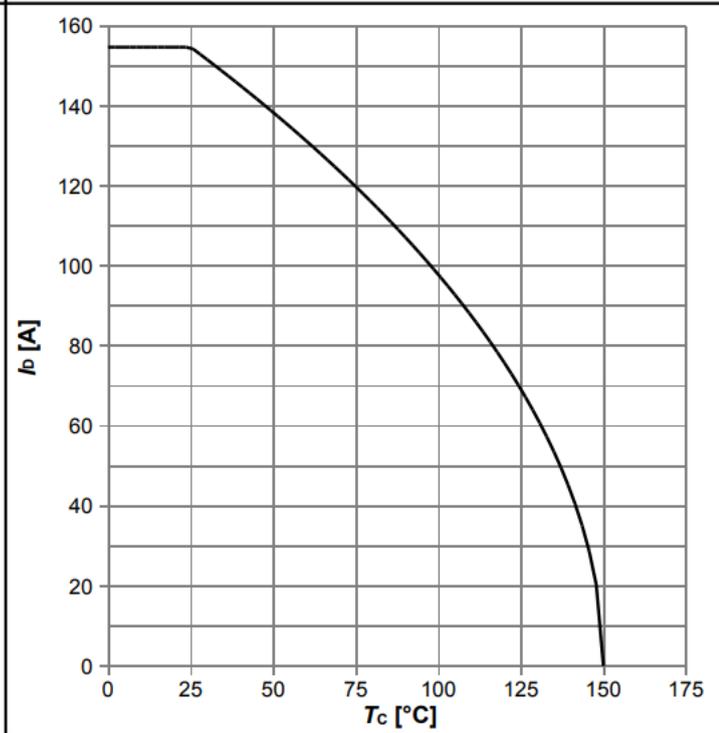
4 电气特性图

Diagram 1: Power dissipation



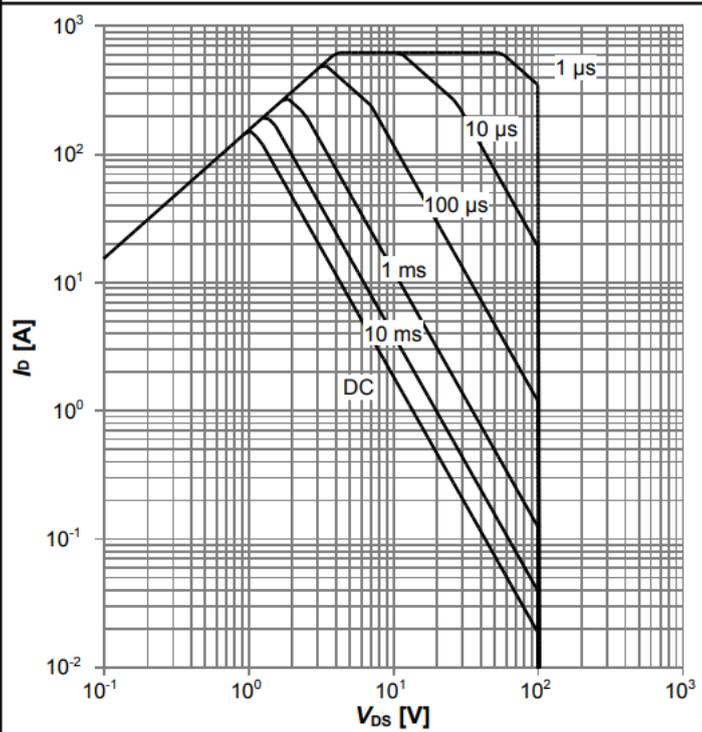
$P_{tot}=f(T_c)$

Diagram 2: Drain current



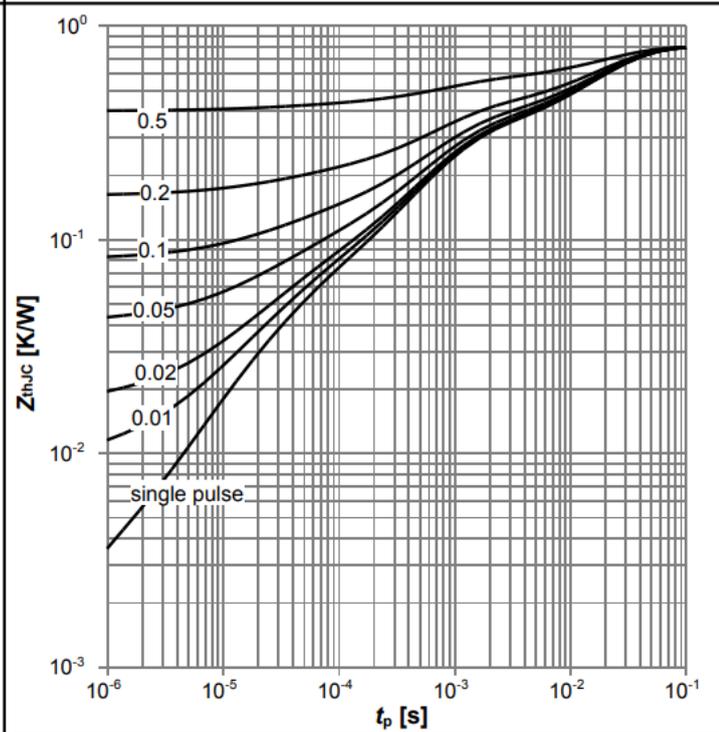
$I_D=f(T_c); V_{GS} \geq 10 \text{ V}$

Diagram 3: Safe operating area



$I_D=f(V_{DS}); T_c=25 \text{ °C}; D=0; \text{ parameter: } t_p$

Diagram 4: Max. transient thermal impedance

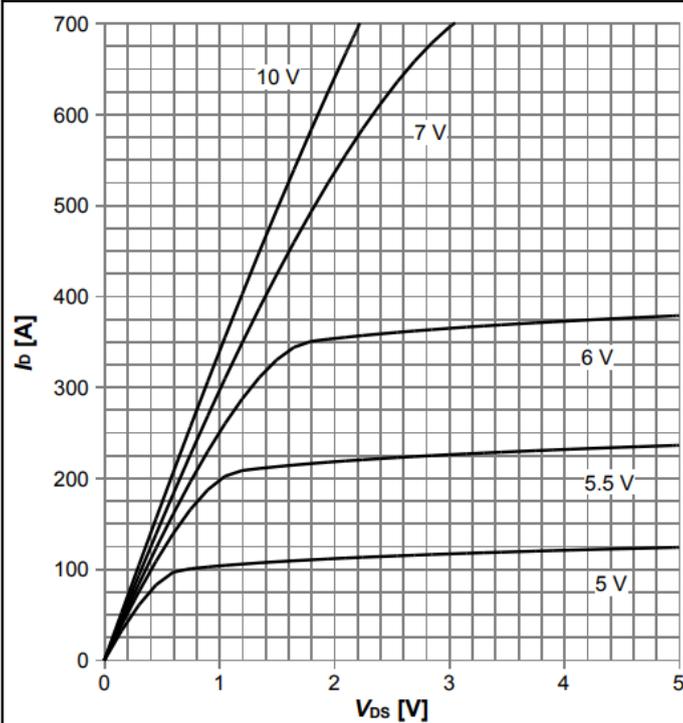


$Z_{thjC}=f(t_p); \text{ parameter: } D=t_p/T$

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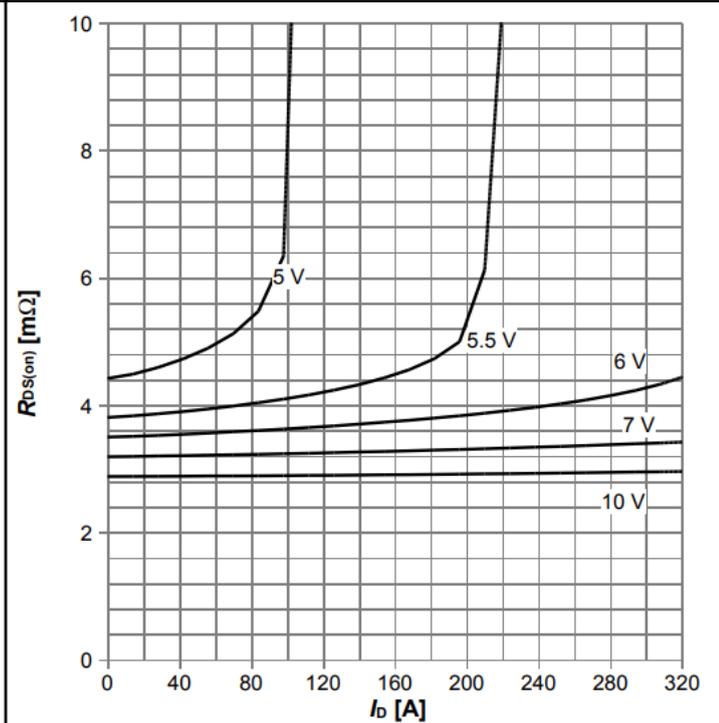
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Diagram 5: Typ. output characteristics



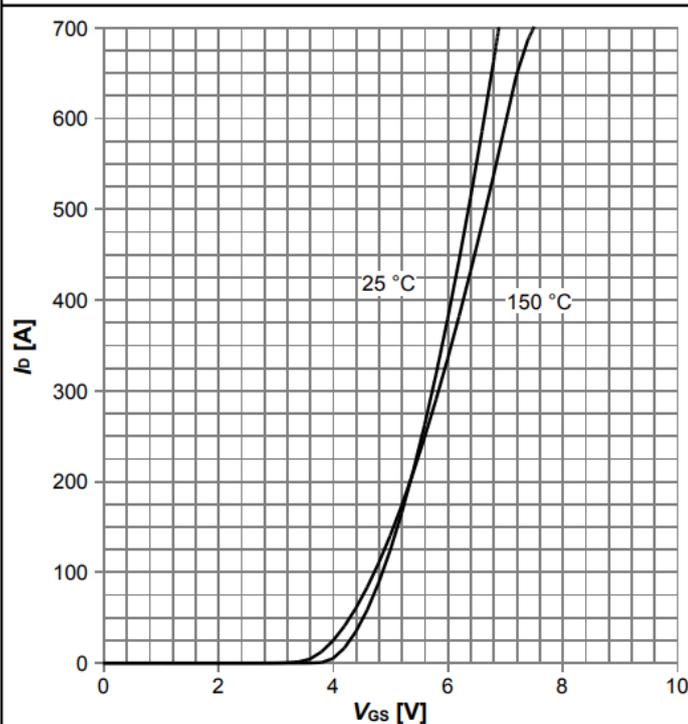
$I_D = f(V_{DS}, T_j = 25\text{ °C}; \text{parameter: } V_{GS})$

Diagram 6: Typ. drain-source on resistance



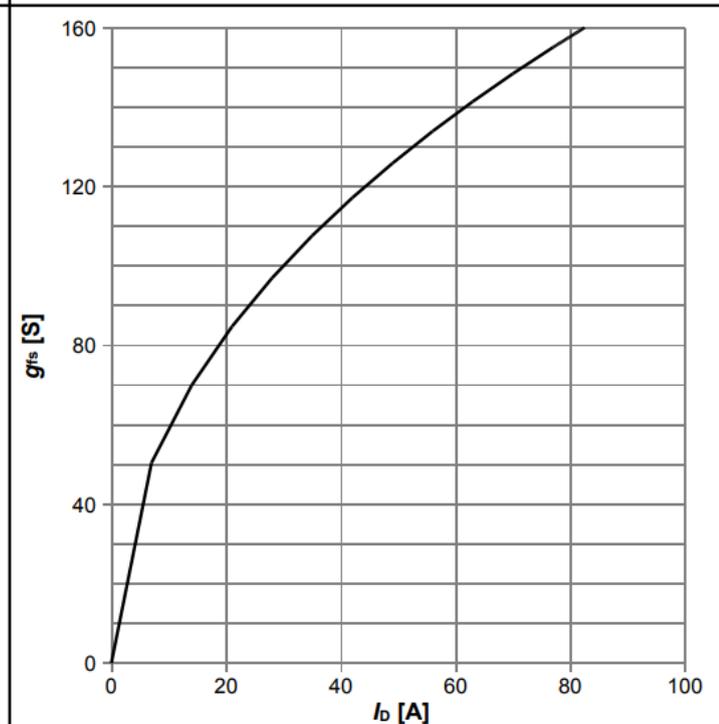
$R_{DS(on)} = f(I_D, T_j = 25\text{ °C}; \text{parameter: } V_{GS})$

Diagram 7: Typ. transfer characteristics



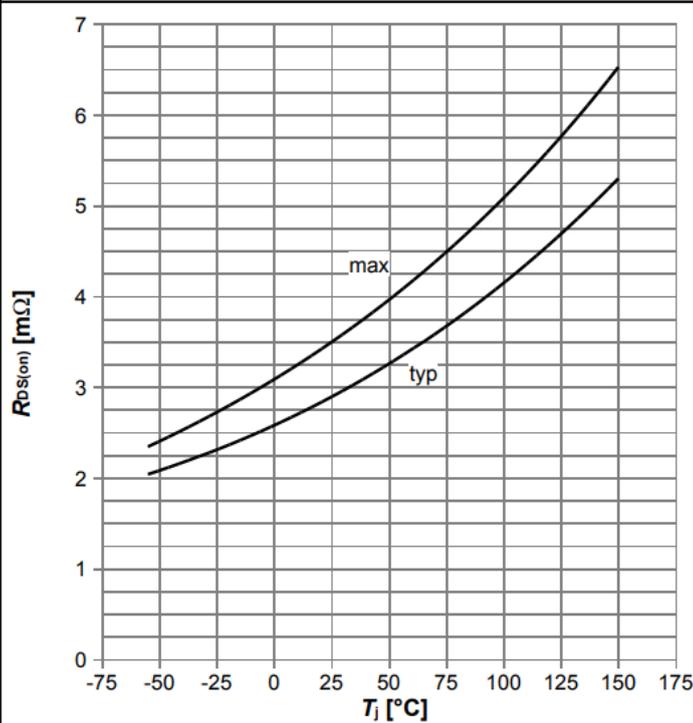
$I_D = f(V_{GS}, |V_{DS}| > 2|I_D|R_{DS(on)max}; \text{parameter: } T_j)$

Diagram 8: Typ. forward transconductance



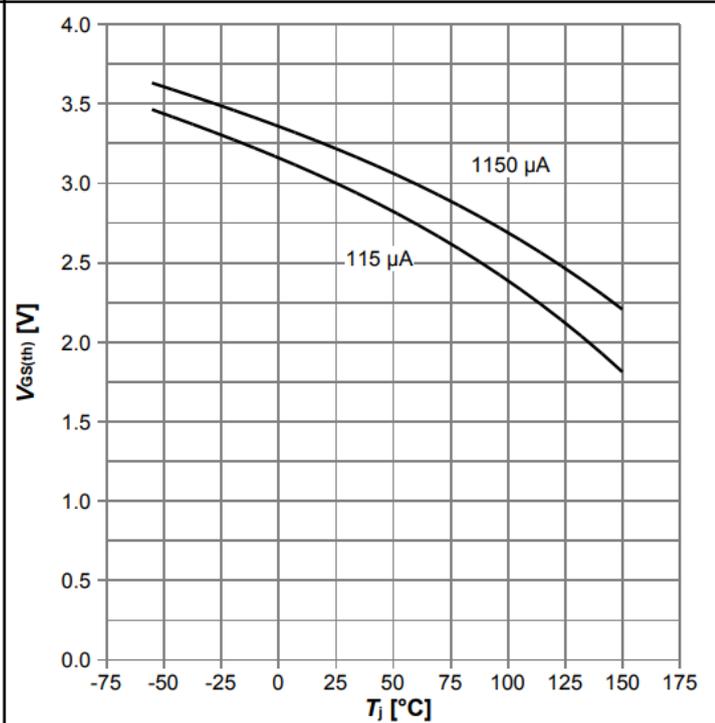
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on resistance



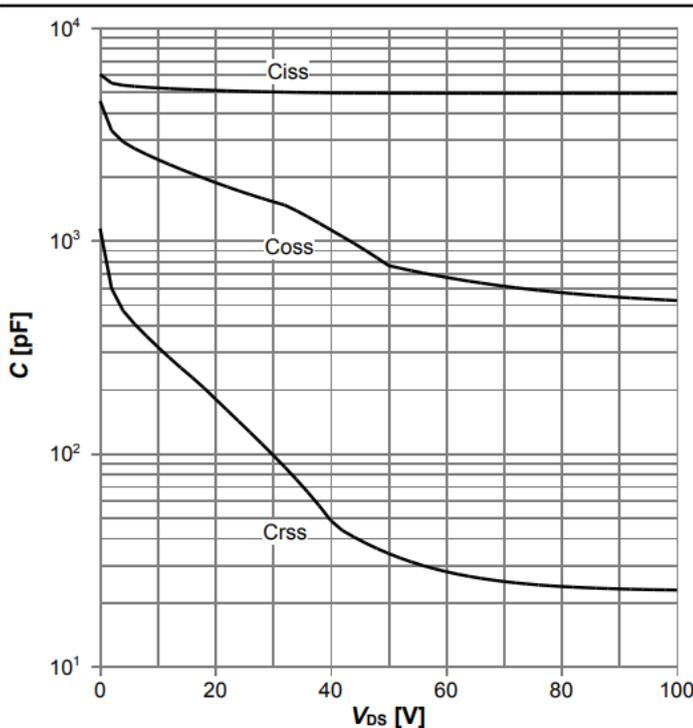
$R_{DS(on)}=f(T_j)$, $I_D=50$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



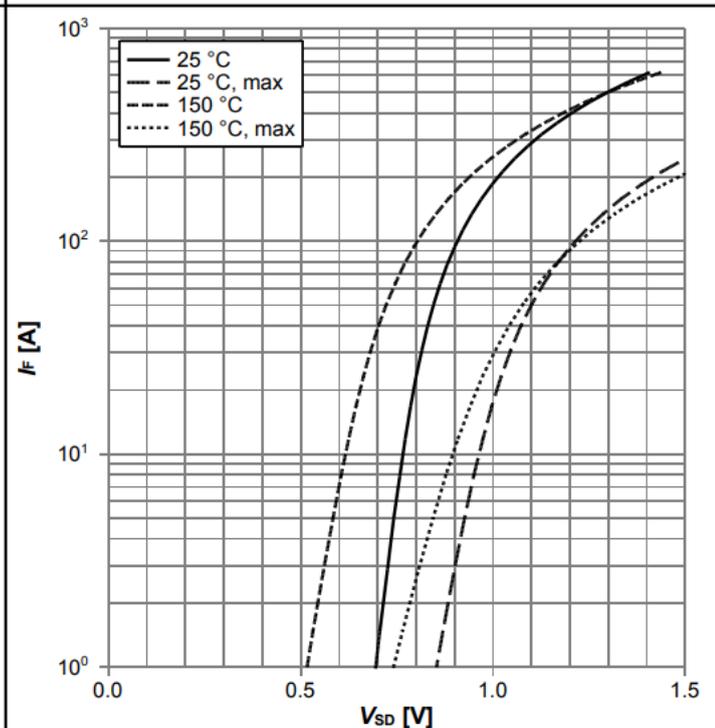
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode

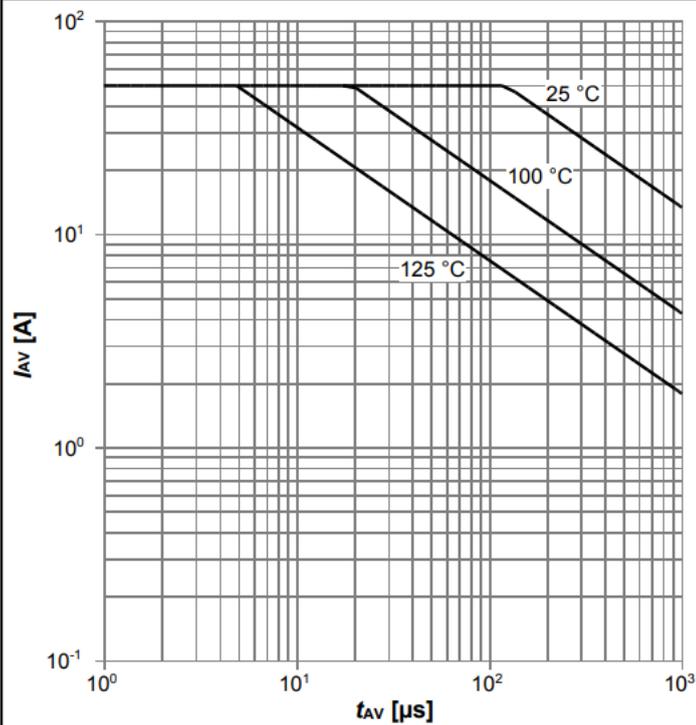


$I_F=f(V_{SD})$; parameter: T_j

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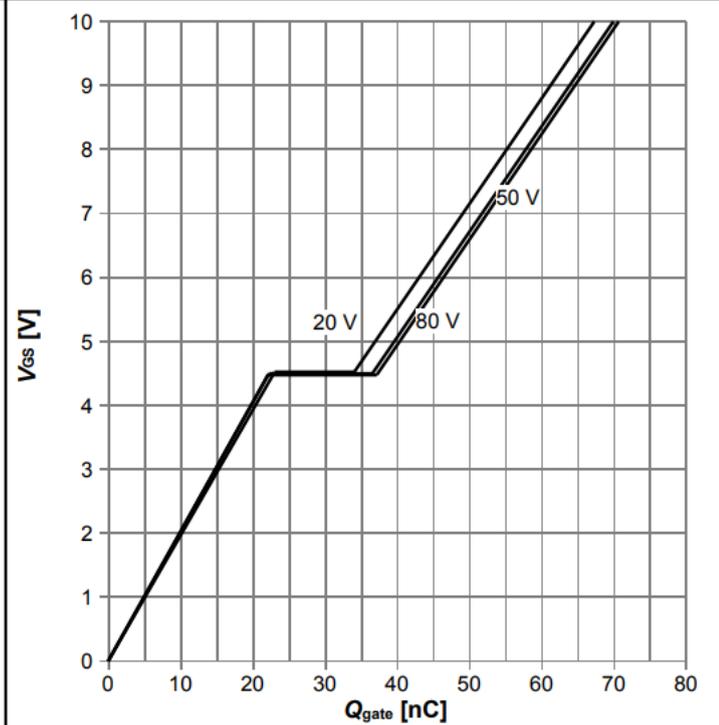
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Diagram 13: Avalanche characteristics



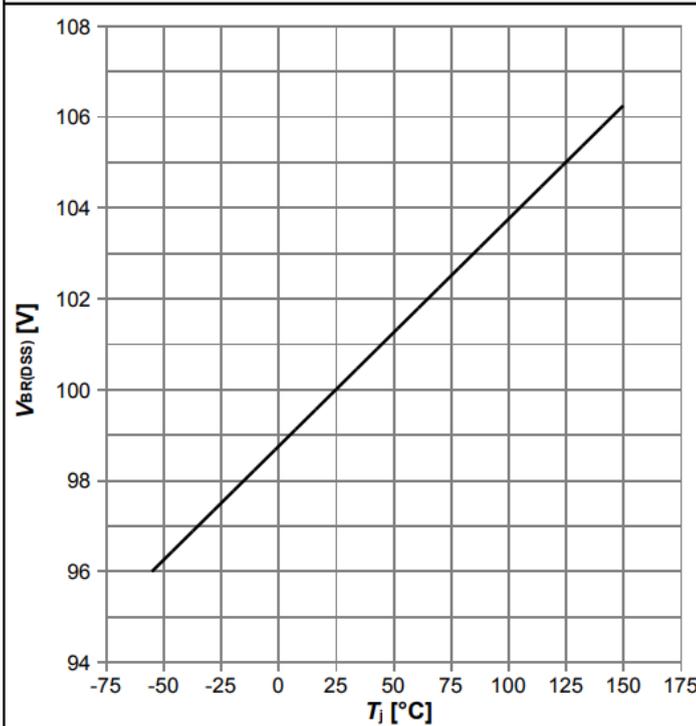
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



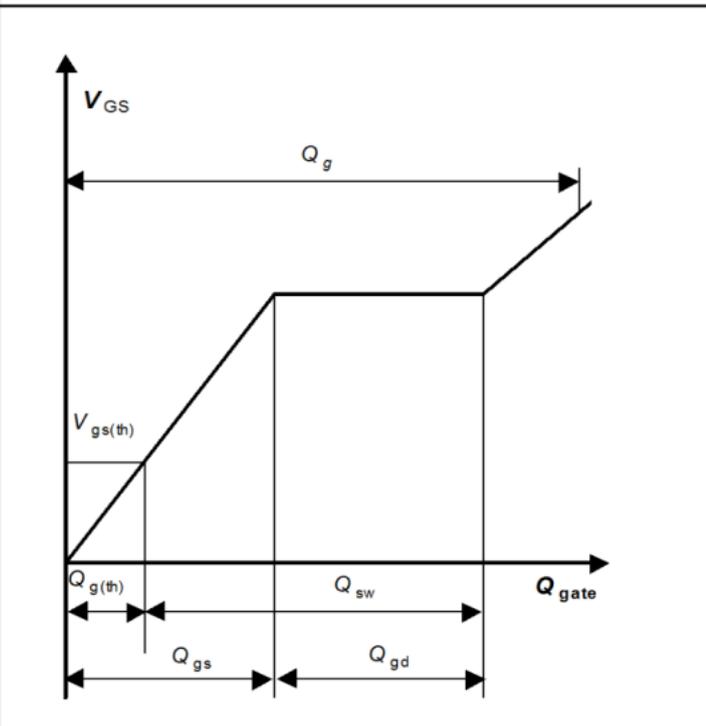
$V_{GS}=f(Q_{gate}); I_D=50 \text{ A pulsed}$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

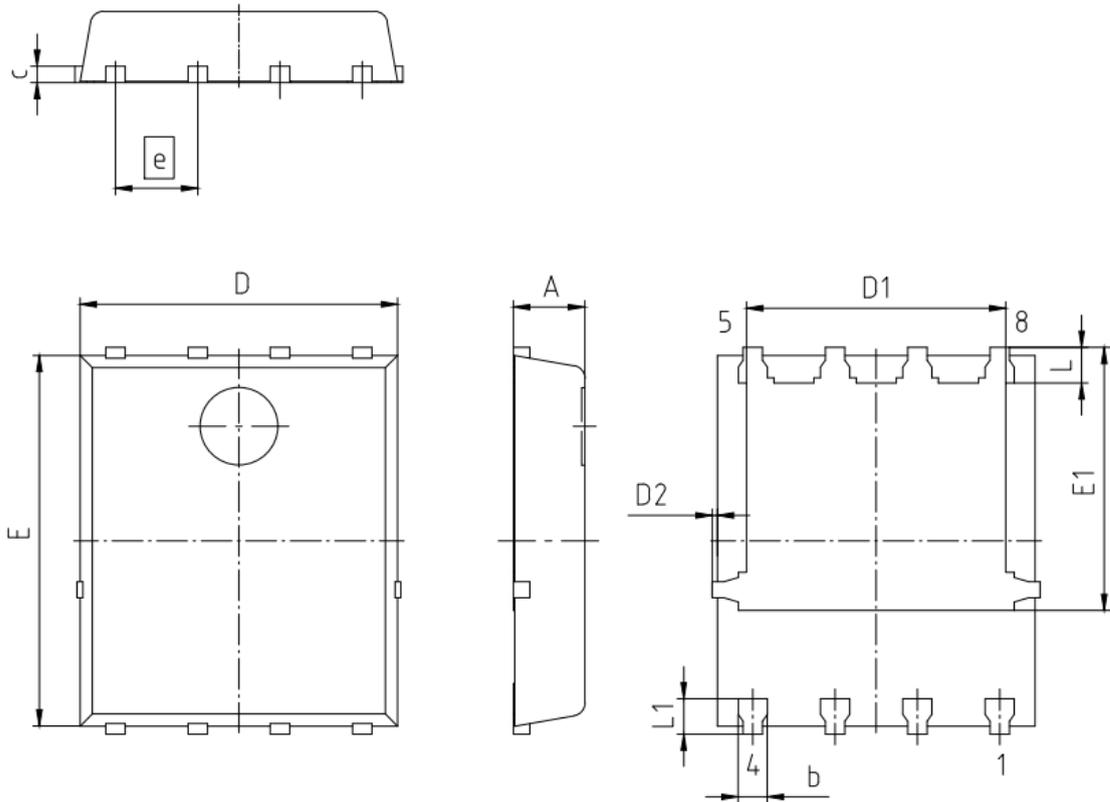
Diagram Gate charge waveforms



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5 封装外形



PACKAGE - GROUP NUMBER: PG-TDSON-8-U08		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
b	0.34	0.54
c	0.15	0.35
D	4.80	5.35
D1	3.90	4.40
D2	0.00	0.22
E	5.70	6.10
E1	4.05	4.25
e	1.27	
L	0.45	0.65
L1	0.45	0.65

- 1) EXCLUDING MOLD FLASH
- 2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
- 3) ALL METAL SURFACES ARE PLATED,
EXCEPT AREA OF CUT

图1 PG-TDSON-8 外形图，尺寸单位为毫米

修订记录

BSC035N10NS5

Revision: 2022-09-05, Rev. 2.5

历史修订版本

Revision	Date	Subjects (major changes since last revision)
2.0	2014-12-17	Release of final version
2.1	2016-09-07	Update Avalanche Energy
2.2	2021-02-09	Update current rating
2.3	2021-05-10	Update package drawings
2.4	2021-05-11	Fix naming mismatch
2.5	2022-09-05	Update outline drawing and footnotes

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