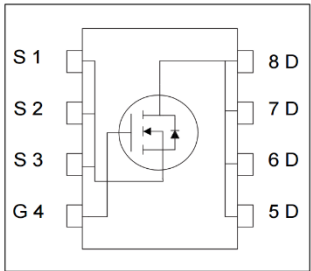
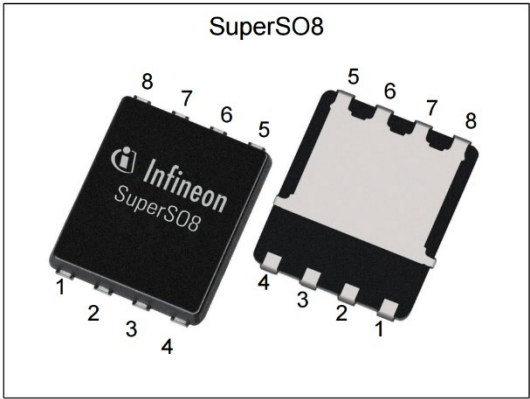


英飞凌MOSFET

OptiMOS™功率晶体管，60V

特性

- 针对高性能 SMPS（例如同步整流）进行优化
- 100% 雪崩测试
- 卓越的热阻
- N沟道
- 符合 JEDEC¹⁾ 目标应用要求
- 无铅引脚镀层；符合 RoHS 标准
- 符合 IEC61249-2-21 标准的无卤设计



RoHS

表 1 主要性能参数

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	3.4	mΩ
I_D	112	A
Q_{oss}	37	nC
$Q_c(0V..10V)$	33	nC

Type / Ordering Code	Package	Marking	Related Links
BSC034N06NS	PG-TDSON-8	034N06NS	-

¹⁾ J-STD20 和 JESD22

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OptiMOS™功率晶体管，60 V

BSC034N06NS

目录

描述1

最大额定值3

热特性3

电气特性4

电气特性图6

封装外形10

修订记录13

商标13

免责声明13

OptiMOS™功率晶体管，60 V

BSC034N06NS

1 最大额定值

除非另有规定， $T_j = 25^\circ\text{C}$

表 2 最大额定值

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	112 71 21	A	$V_{GS}=10\text{ V}$, $T_C=25^\circ\text{C}$ $V_{GS}=10\text{ V}$, $T_C=100^\circ\text{C}$ $V_{GS}=10\text{ V}$, $T_C=25^\circ\text{C}$, $R_{thJA}=50\text{K/W}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	448	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	71	mJ	$I_D=50\text{ A}$, $R_{GS}=25\ \Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	74 2.5	W	$T_C=25^\circ\text{C}$ $T_A=25^\circ\text{C}$, $R_{thJA}=50\text{ K/W}^{2)}$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	$^\circ\text{C}$	IEC climatic category; DIN IEC 68-1: 55/150/56

2 热特性

表 3 热特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.0	1.7	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	50	K/W	-

¹⁾ 额定值指产品仅具有数据表指定的绝对最大值，保持外壳温度为25°C。更高外壳温度请参见图 2。需要根据实际环境条件降低额定值。

²⁾ 器件置于 40 mm x 40 mm x 1.5 mm 环氧树脂印刷电路板 FR4 上，配有 6 cm²（单层，70 μm 厚）铜层面积用于漏极连接。印刷电路板在静止空气中垂直放置。

³⁾ 详细信息请参见图 3

⁴⁾ 详细信息请参见图 13

OptiMOS™功率晶体管，60 V

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3 电气特性

除非另有规定， $T_j = 25^\circ\text{C}$

表 4 静态特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}$, $I_D=41\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25^\circ\text{C}$ $V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.8 4.0	3.4 5.1	m Ω	$V_{GS}=10\text{ V}$, $I_D=50\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=12.5\text{ A}$
Gate resistance ¹⁾	R_G	-	1.3	2.0	Ω	-
Transconductance	g_{fs}	46	93	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=50\text{ A}$

表 5 动态特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	2400	3000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	560	700	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	27	54	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	9	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	5	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	19	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	5	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext,ext}=1.6\text{ }\Omega$

表 6 栅极电荷特性²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	11	-	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	6.7	-	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	6.5	9.2	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	11	-	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	33	41	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.7	-	V	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	29	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	37	47	nC	$V_{DD}=30\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ 由设计指定，未经过生产测试。

²⁾ 参数定义请参见“栅极电荷波形”

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表 7 反向二极管

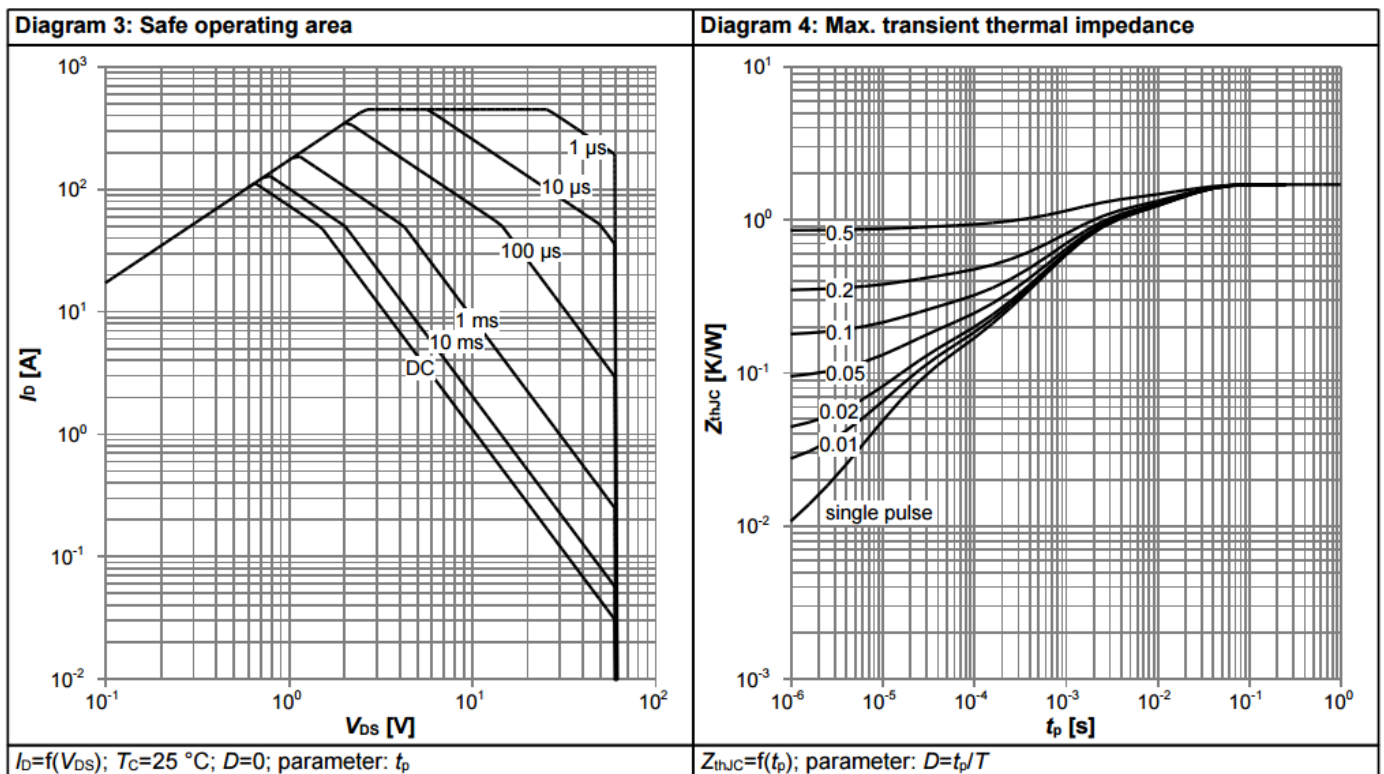
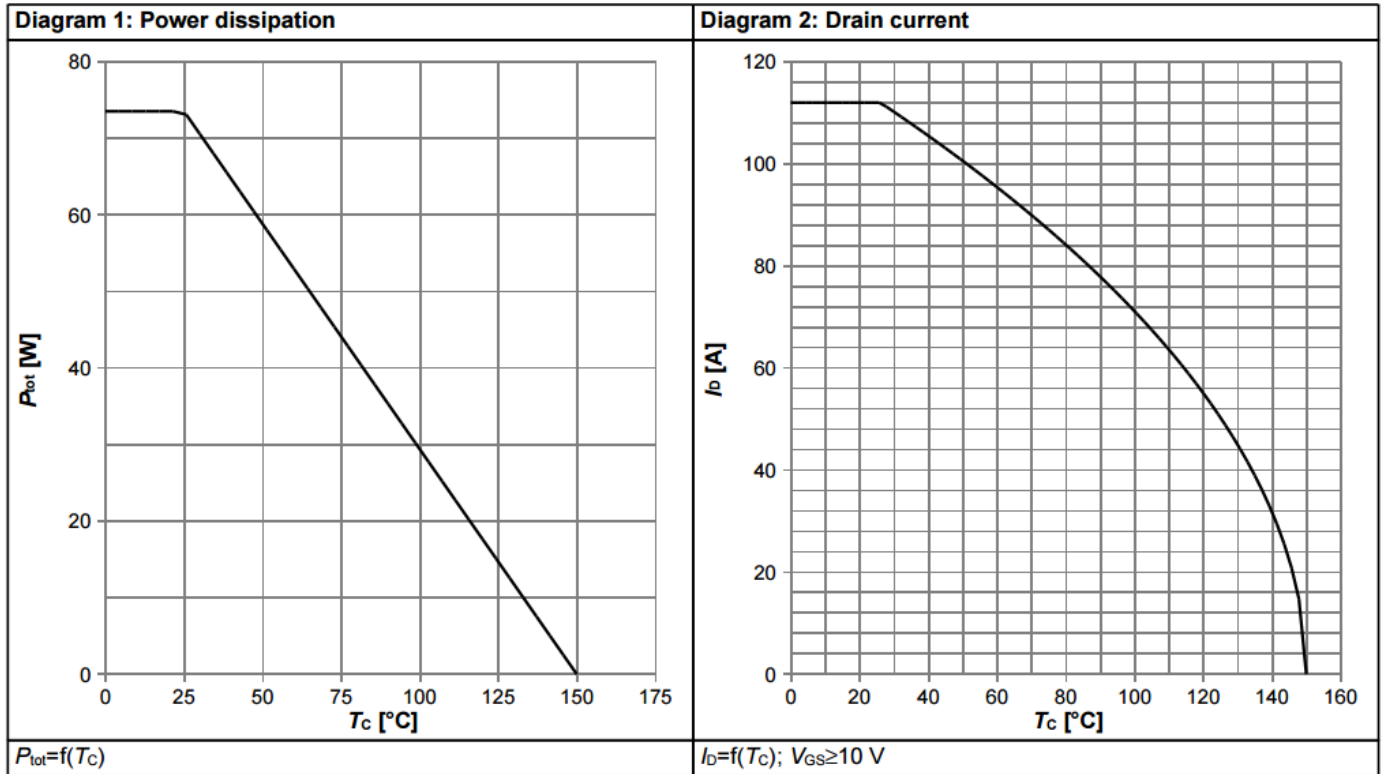
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	67	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	448	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.9	1.2	V	$V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	49	78	ns	$V_R=30\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	65	-	nC	$V_R=30\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ 由设计指定，未经过生产测试

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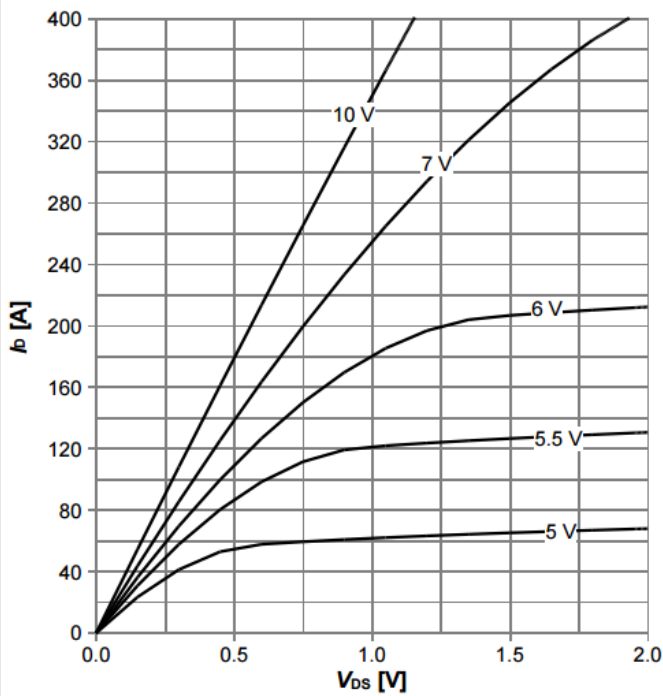
4 电气特性图



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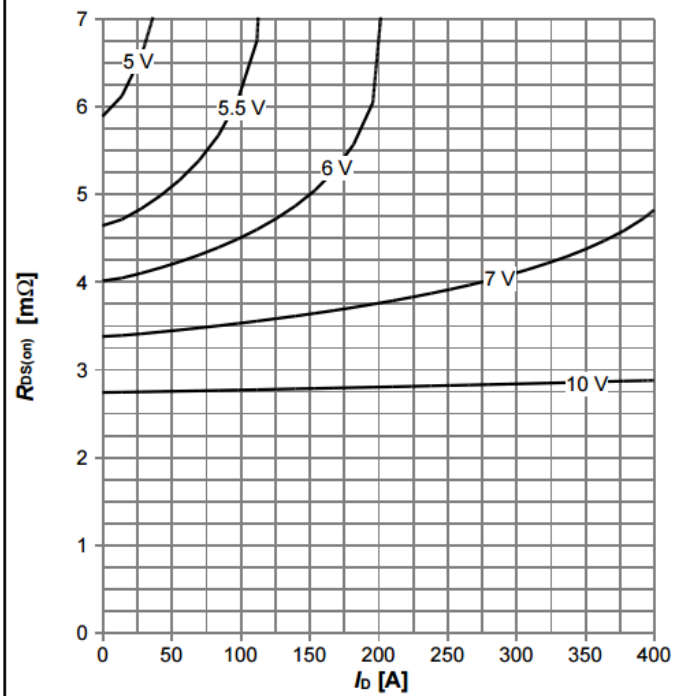
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Diagram 5: Typ. output characteristics



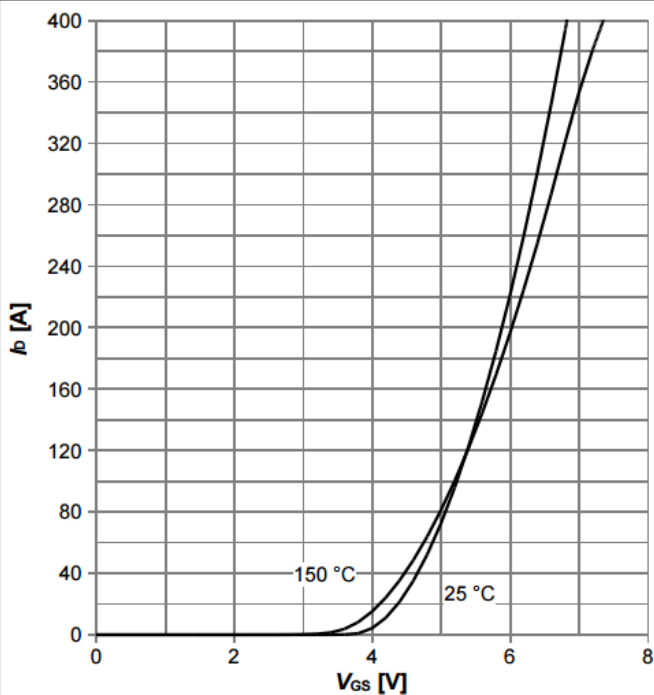
$I_D = f(V_{DS})$; $T_J = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



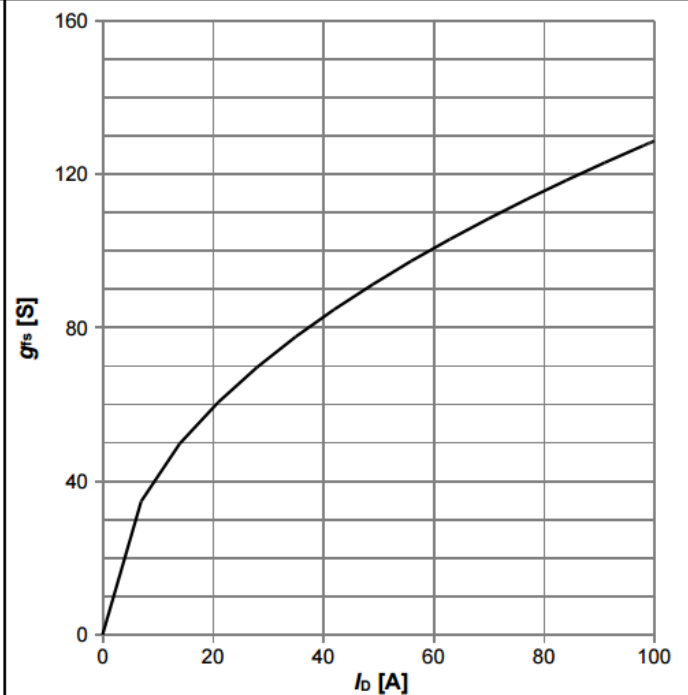
$R_{DS(on)} = f(I_D)$; $T_J = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



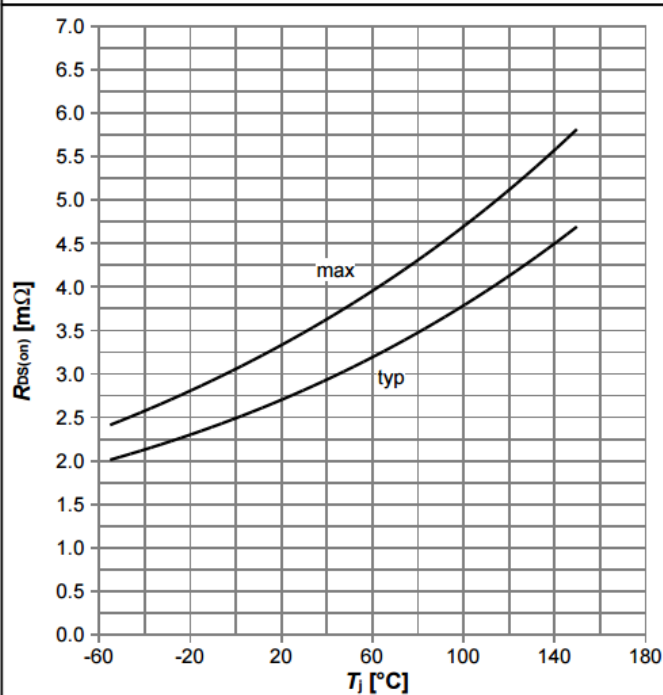
$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_J

Diagram 8: Typ. forward transconductance



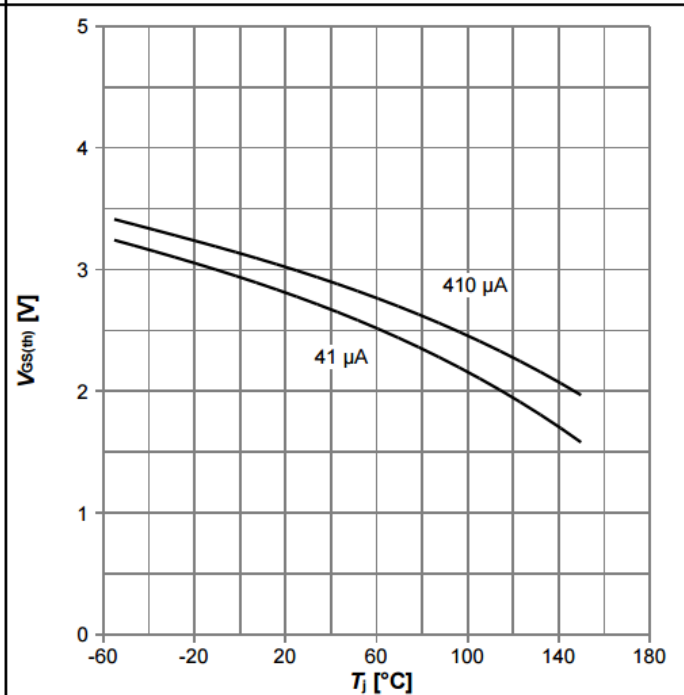
$g_{fs} = f(I_D)$; $T_J = 25^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



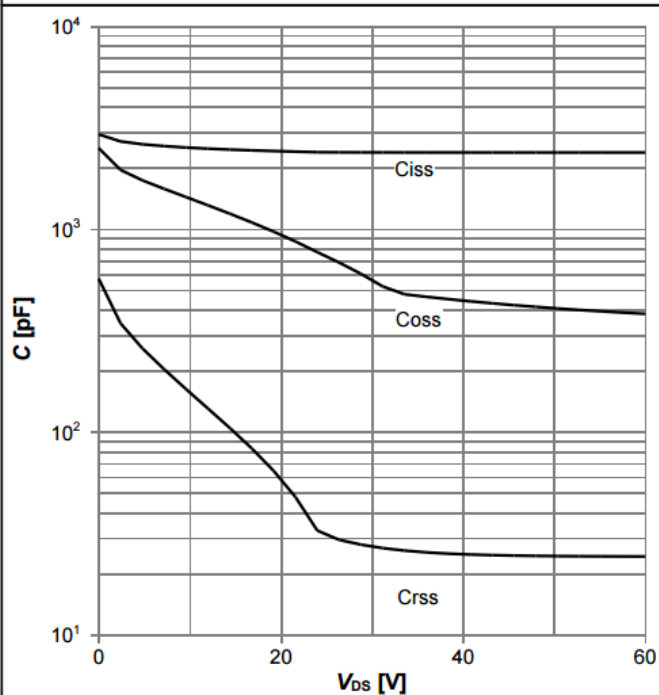
$R_{DS(on)} = f(T_J)$; $I_D = 50$ A; $V_{GS} = 10$ V

Diagram 10: Typ. gate threshold voltage



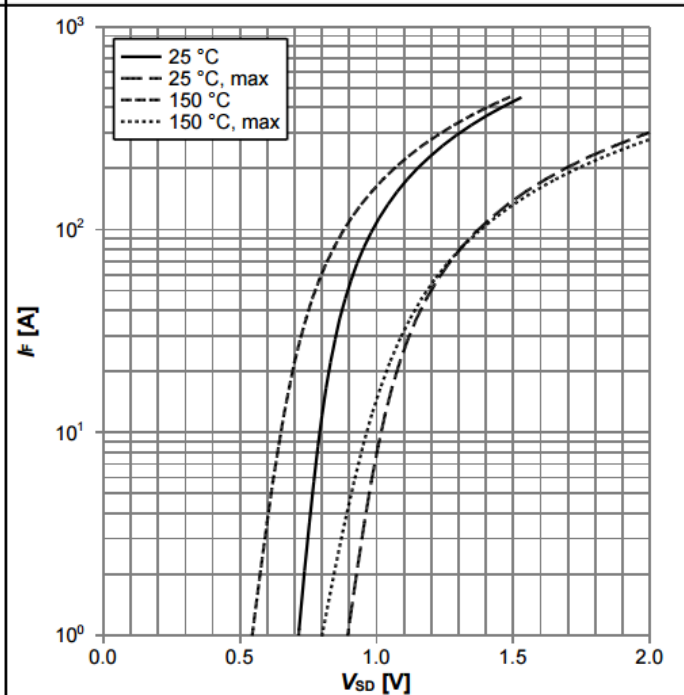
$V_{GS(th)} = f(T_J)$; $V_{GS} = V_{DS}$

Diagram 11: Typ. capacitances



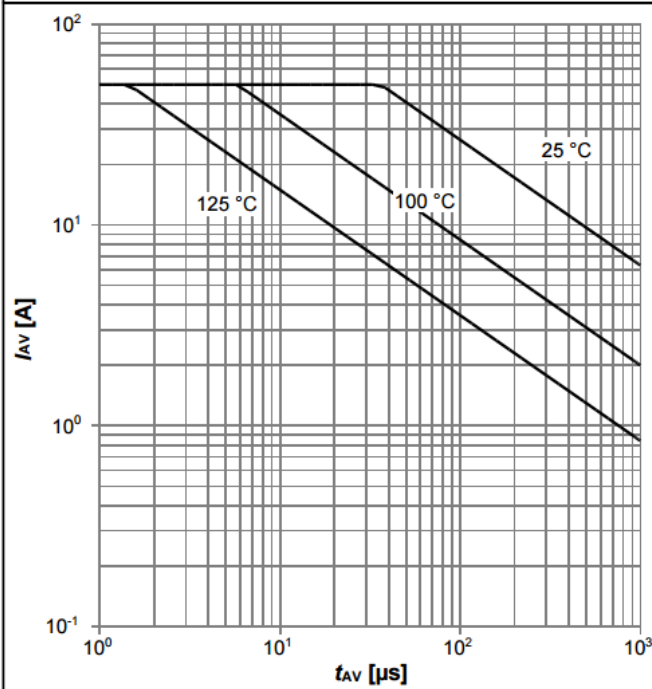
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode



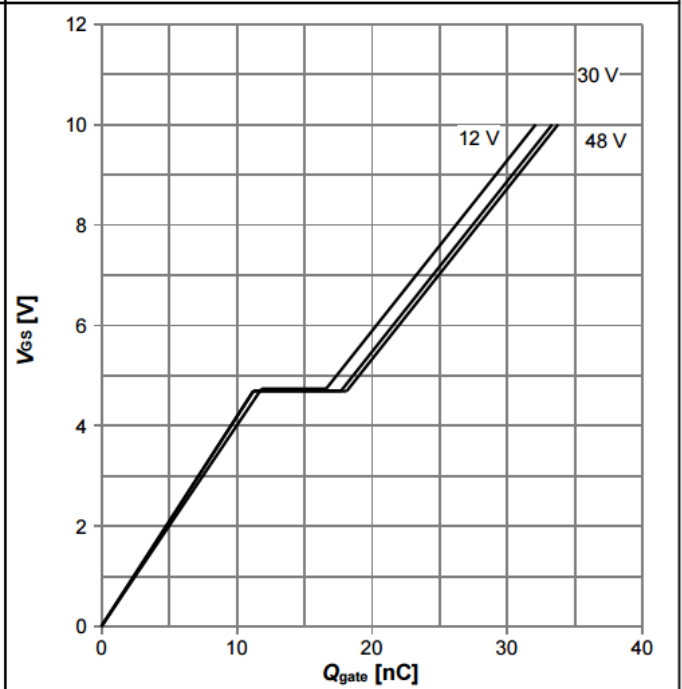
$I_F = f(V_{SD})$; parameter: T_J

Diagram 13: Avalanche characteristics



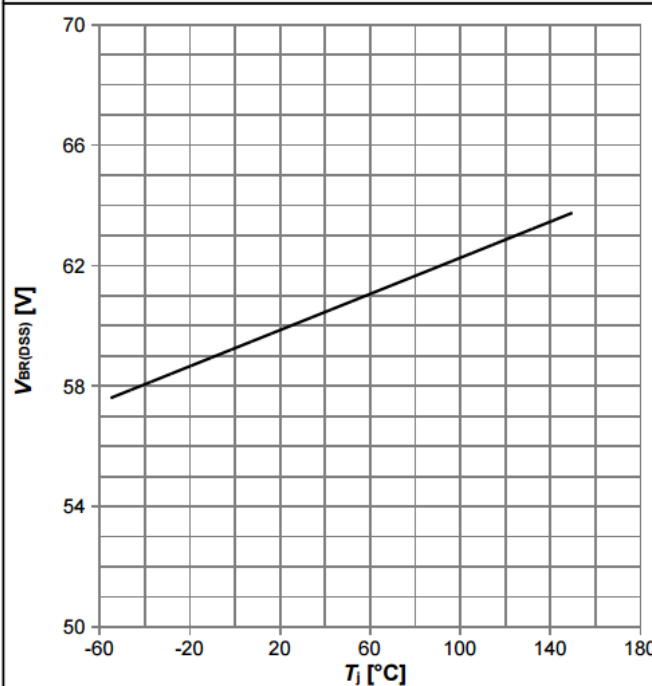
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{J(start)}$

Diagram 14: Typ. gate charge



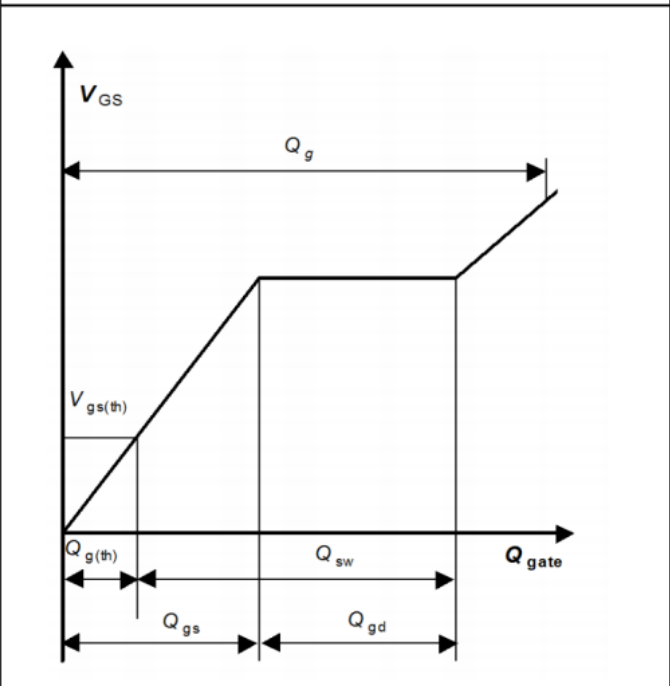
$V_{GS}=f(Q_{gate})$; $I_D=50\text{ A}$ pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

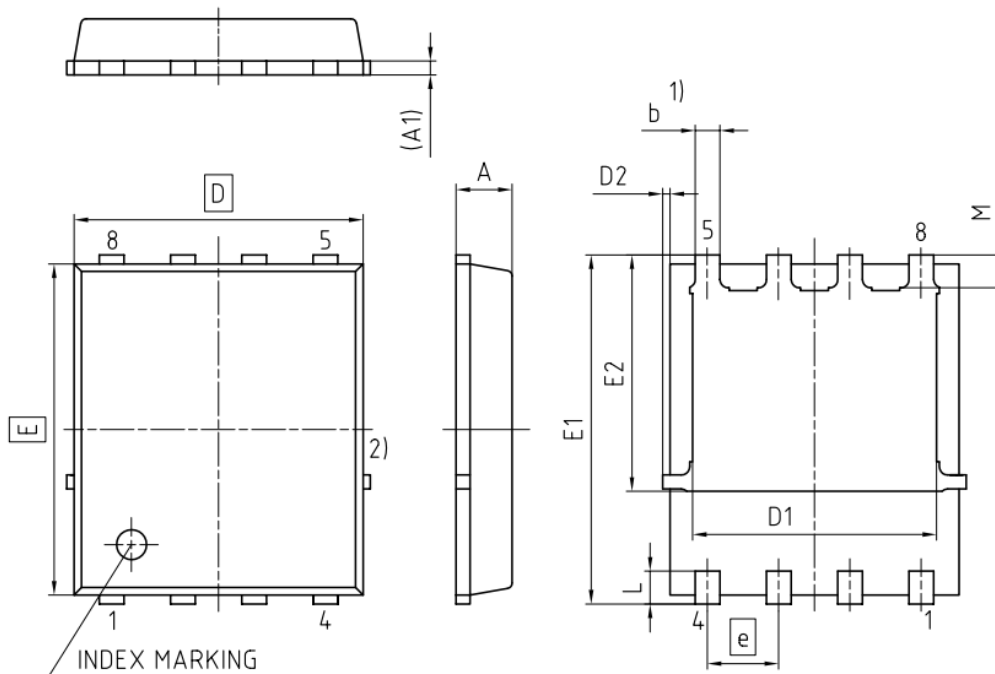


$V_{BR(DSS)}=f(T_J)$; $I_D=1\text{ mA}$

Diagram Gate charge waveforms



5 封装外形



- 1) EXCLUDING MOLD FLASH
 2) REMOVAL ON MOLD GATE
 INTRUSION 0.1 MM
 PROTRUSION 0.1 MM
 LEAD LENGTH UP TO ANTI FLASH LINE
 ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.03	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

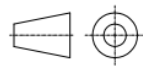
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REVISION 07
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EUROPEAN PROJECTION 
ISSUE DATE 06.06.2019

图 1 PG-TDSON-8 外形图，尺寸单位为毫米

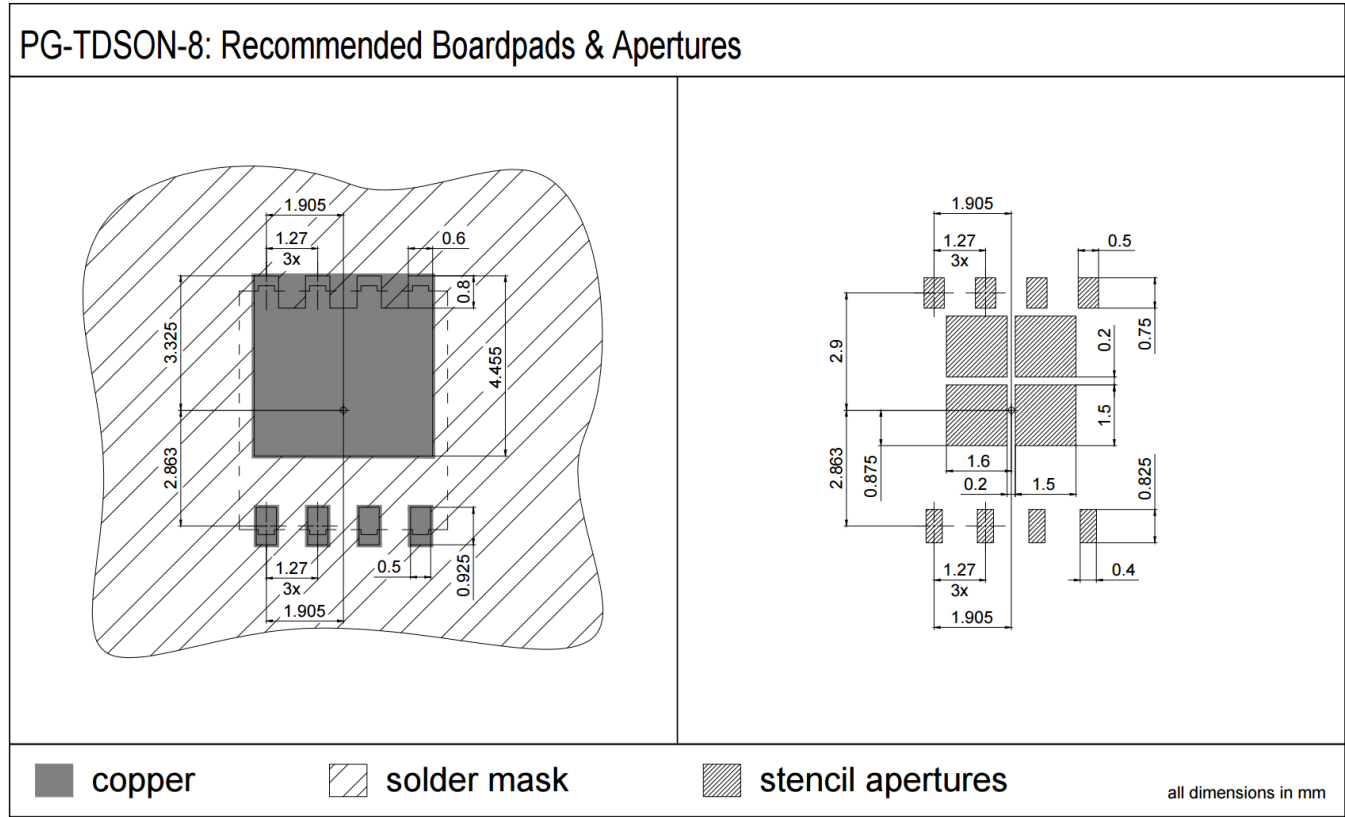
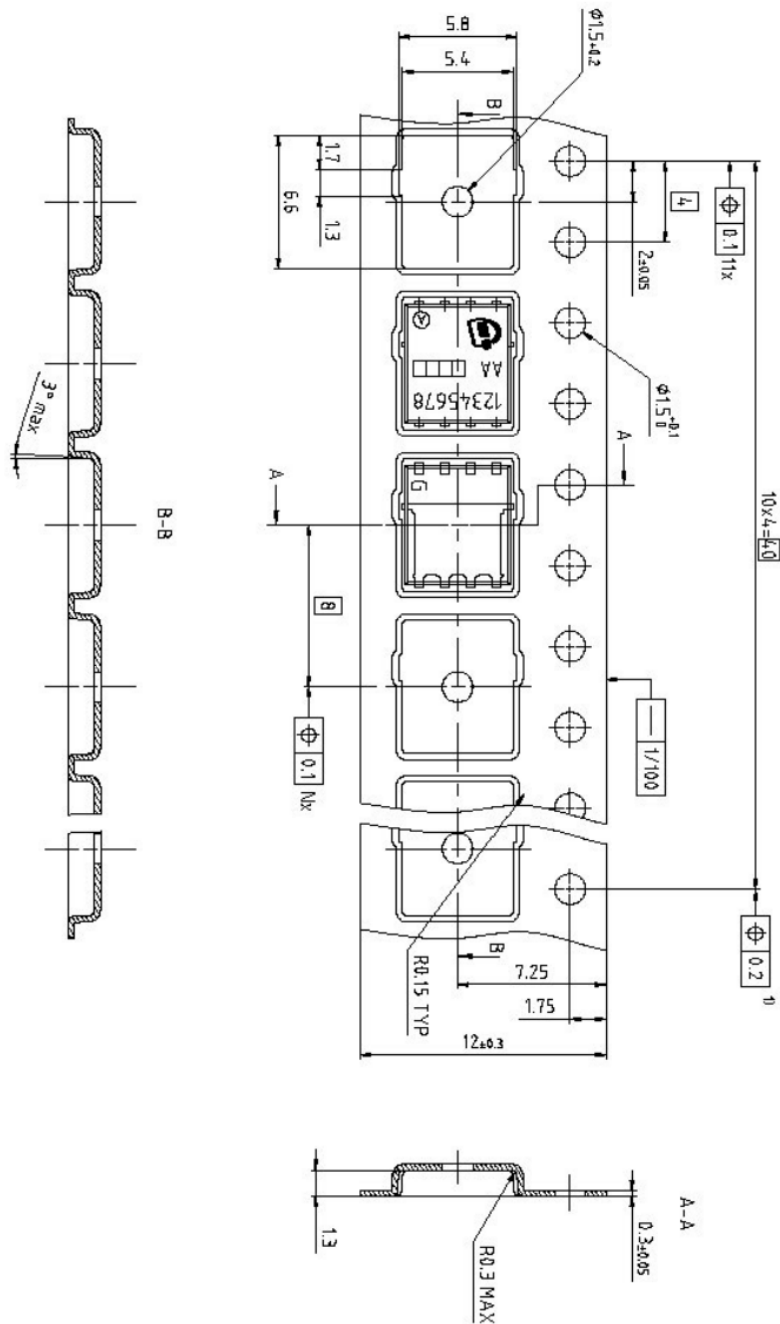


图 2 外形板焊盘 (TDSON-8)，尺寸单位为毫米

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Dimension in mm

图3 封装外形胶带（TDSO-8）

OptiMOS™功率晶体管，60 V

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修订记录

BSC034N06NS

Revision: 2020-05-06, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.2	2019-10-31	Update package drawings. Addition RthJC_typ and Qoss_max.
2.3	2020-05-06	Update current rating

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