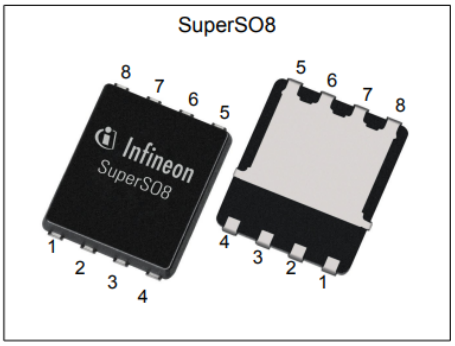
英飞凌功率MOSFET

英飞凌BSC032NE2LS OptiMOS™ 25 V N沟道功率MOSFET



特性

- 针对高性能降压转换器进行了优化
- 极低导通电阻 $R_{DS(on)}$ @ V_{GS} =4.5 V
- 100% 雪崩测试
- 卓越的耐热性
- N沟道
- 符合 JEDEC [1]目标应用要求
- 无铅镀层；符合RoHS标准
- 符合 IEC61249-2-21 标准的无卤素

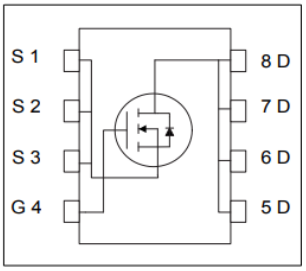


表 1　　主要性能参数

Parameter	Value	Unit
V_{DS}	25	V
$R_{DS(on),max}$	3.2	mΩ
I_D	84	A
Q_{OSS}	9.4	nC
Q_G(0V..10V)	16	nC

Type / Ordering Code	Package	Marking	Related Links
BSC032NE2LS	PG-TDSON-8	032NE2LS	-

[1] J-STD20 和 JESD22

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。 为确认准确性请务必访问 infineon.com 参考最新的英文版本（控制文档）。

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1 最大额定值

除非另有规定， T_j = 25 °C

表 2 最大额定值

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - - - -	- - - - -	84 53 68 43 22	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_C=25 °C V_{GS}=4.5 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 K/W[1)]
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	336	A	T_C=25 °C
Avalanche current, single pulse[3)]	I_{AS}	-	-	45	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	20	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	37 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W[1)]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 热特性

表3 热特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.4	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm² cooling area[1)]	R_{thJA}	-	-	50	K/W	-

[1)]器件位于 40 mm x 40 mm x 1.5 mm 环氧 FR4 PCB 上，其中 6 cm2（单层，70 µm 厚）的铜面积用于漏极连接。PCB 垂直放置在静止空气中。
[2)]详细信息请参见图 3
[3)]详细信息请参见图 13

3 电气特性

除非另有规定， T_j = 25 °C

表4 静态特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	25	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	10 100	µA	V_{DS}=25 V, V_{GS}=0 V, T_j=25 °C V_{DS}=25 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	3.8 2.7	4.8 3.2	mΩ	V_{GS}=4.5 V, I_D=30 A V_{GS}=10 V, I_D=30 A
Gate resistance	R_G	0.5	0.9	1.8	Ω	-
Transconductance	g_{fs}	46	93	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=30 A

表 5 动态特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1200	1596	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Output capacitance	C_{oss}	-	470	625	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	51	-	pF	V_{GS}=0 V, V_{DS}=12 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	3.3	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	2.8	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	15	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	2.2	-	ns	V_{DD}=12 V, V_{GS}=10 V, I_D=30 A, $R_{G,ext}$=1.6 Ω

表6 栅极电荷特性[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	3.1	4.1	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	1.9	-	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate to drain charge	Q_{gd}	-	1.9	2.9	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	3.1	-	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total	Q_g	-	7.7	10	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.7	-	V	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge total	Q_g	-	16	21	nC	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	6.7	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge	Q_{oss}	-	9.4	13	nC	V_{DD}=12 V, V_{GS}=0 V

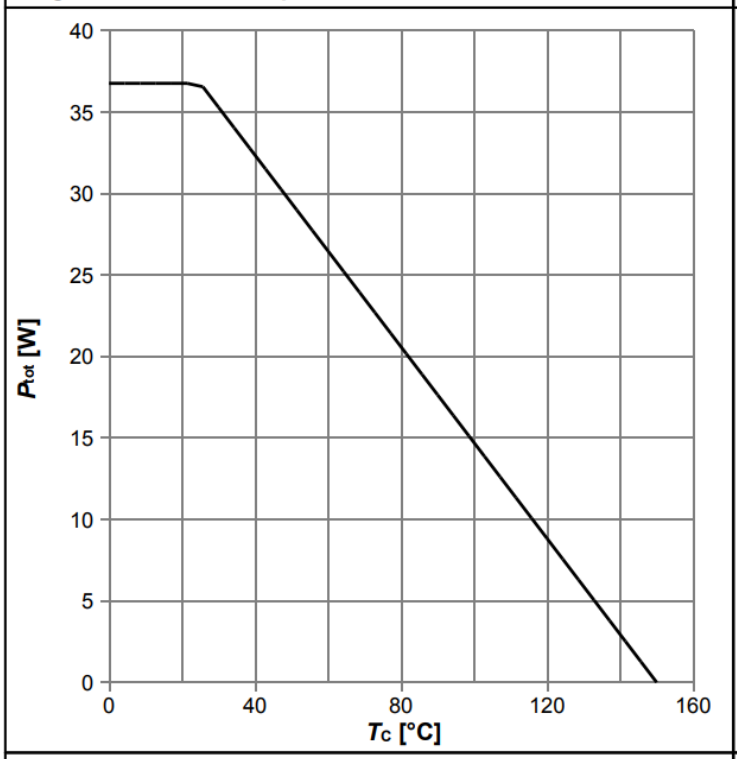
[1)]参数定义请参见"栅极充电波形"

表 7 反向二极管

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	37	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	148	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.87	1	V	V_{GS}=0 V, I_F=30 A, T_j=25 °C
Reverse recovery charge	Q_{rr}	-	10	-	nC	V_R=15 V, I_F=I_S, di_F/dt=400 A/µs

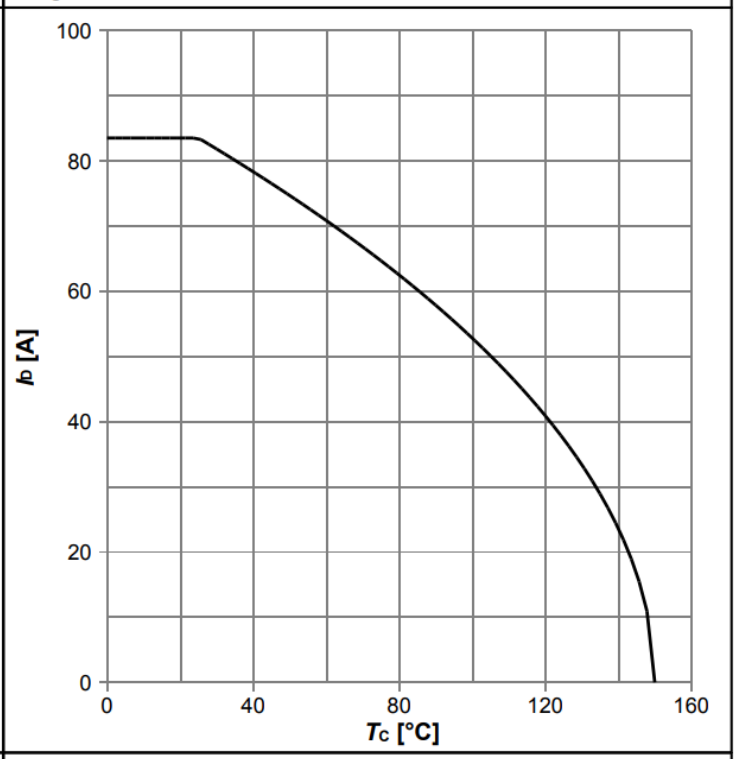
4 电气特性图

Diagram 1: Power dissipation



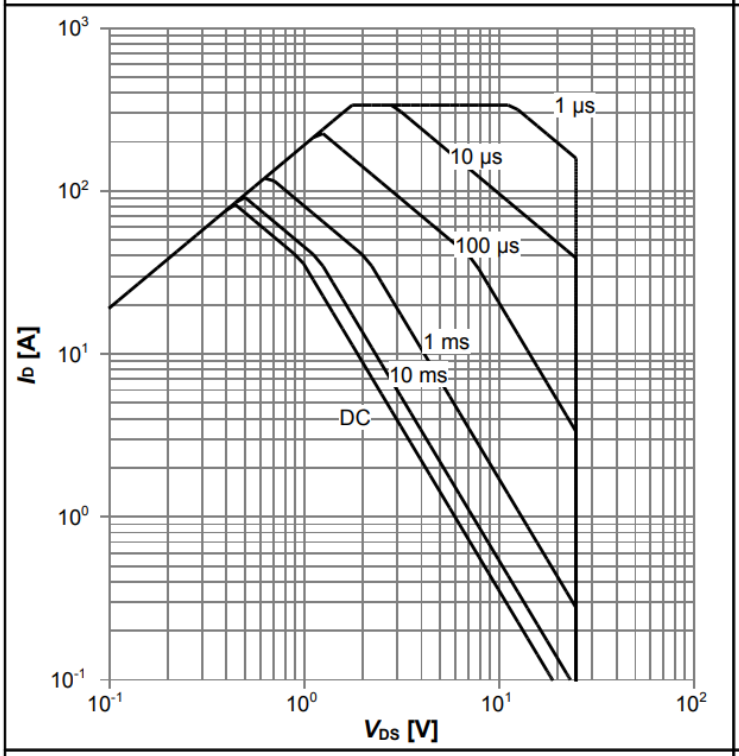
P_{tot}=f(T_C)

Diagram 2: Drain current



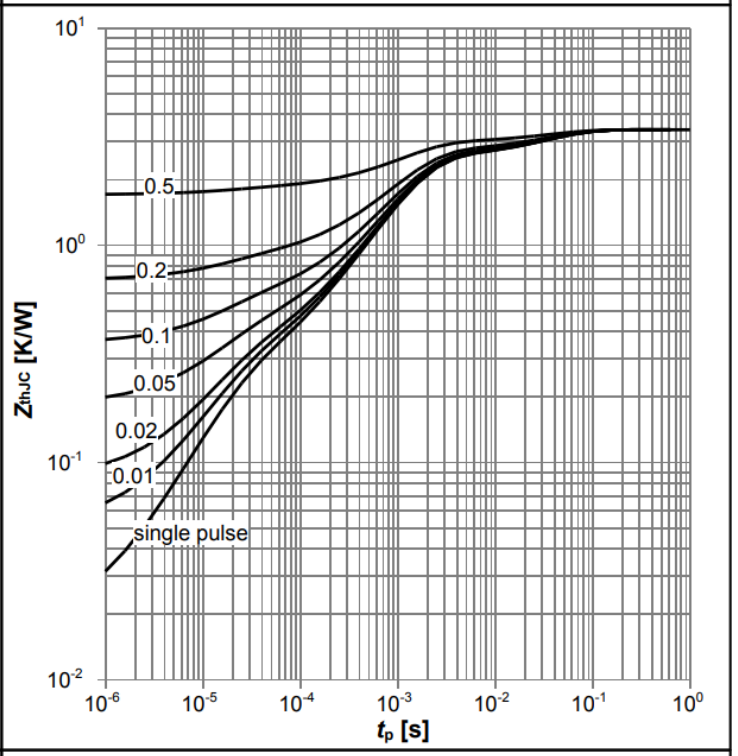
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



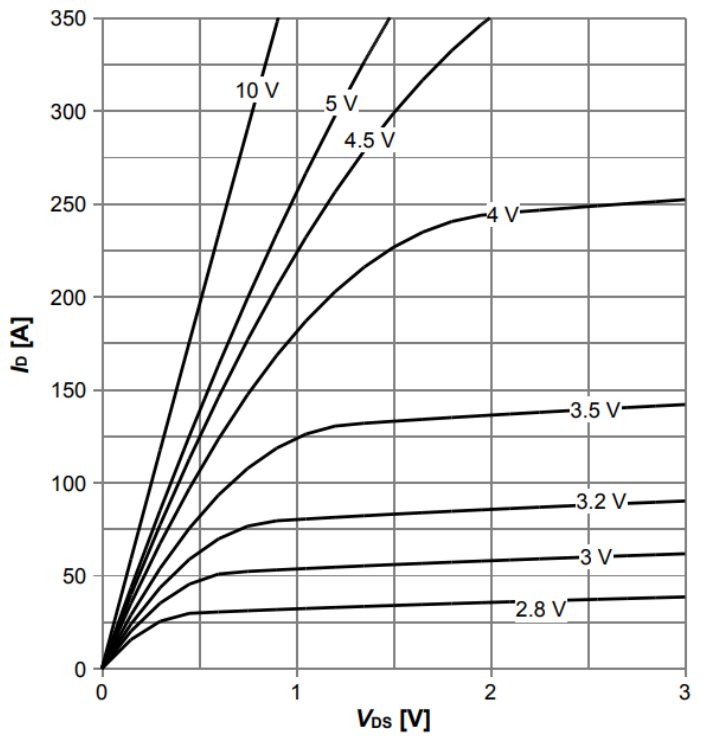
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



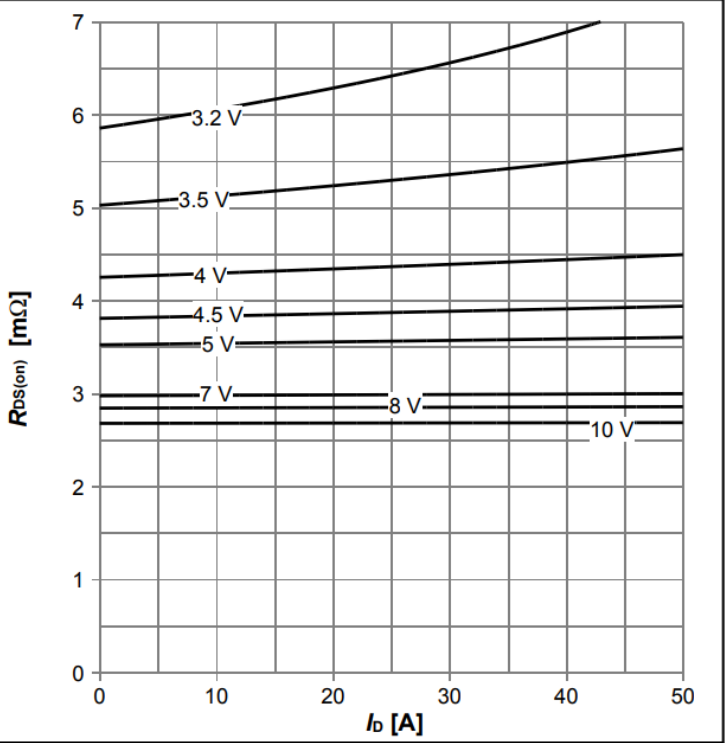
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



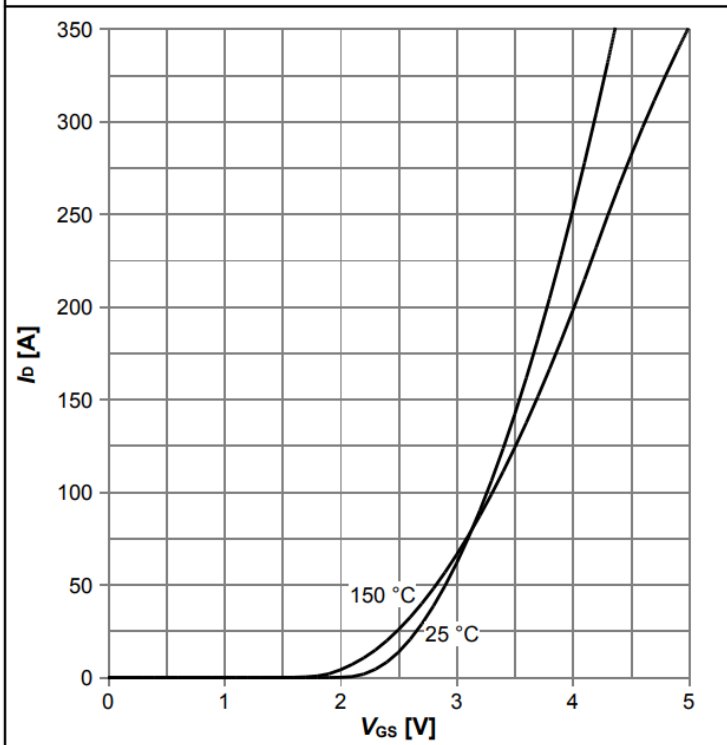
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



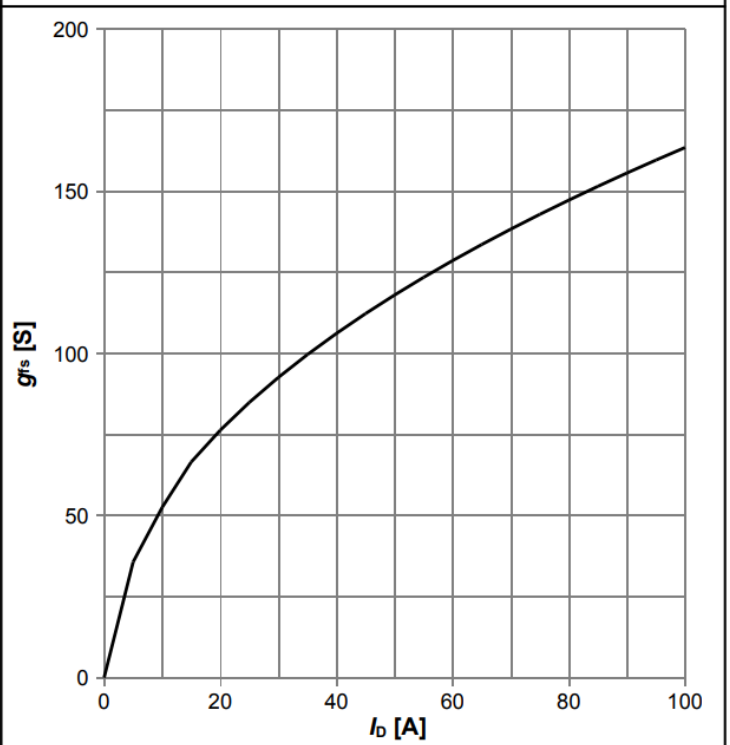
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



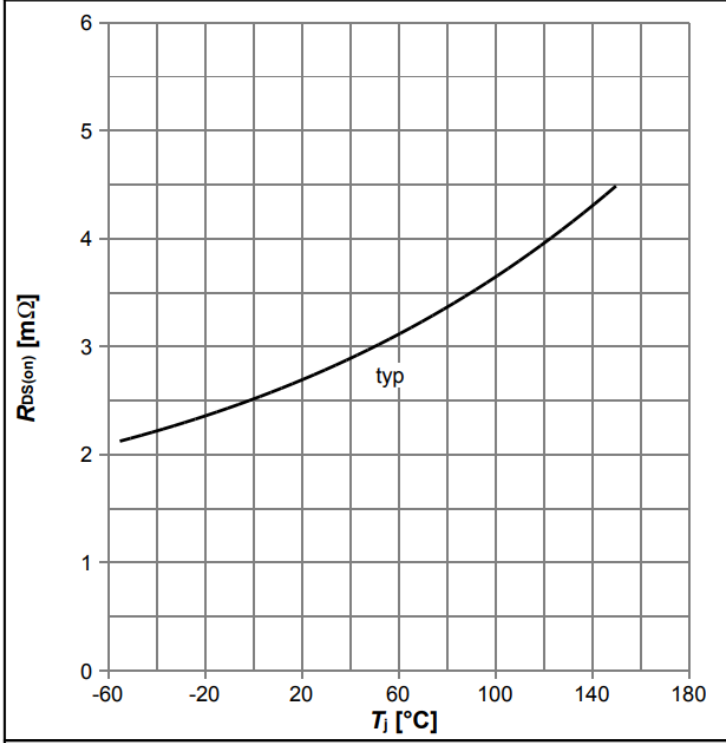
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



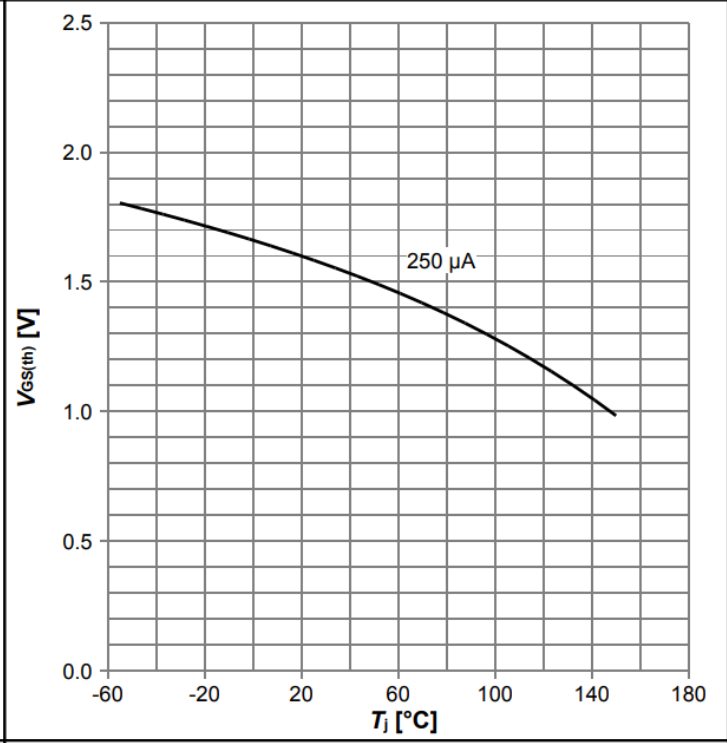
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance



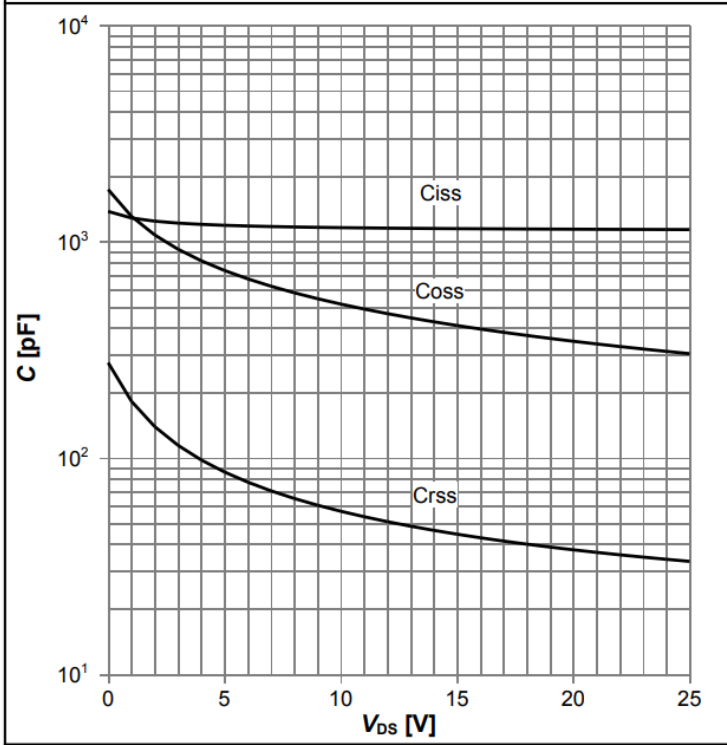
$R_{DS(on)}$=f(T_j); I_D=30 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



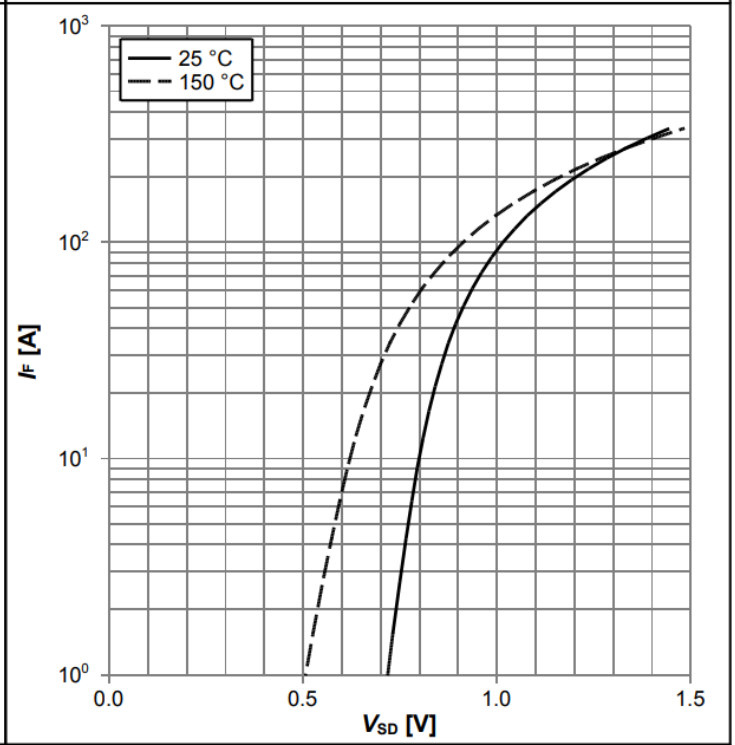
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA

Diagram 11: Typ. capacitances



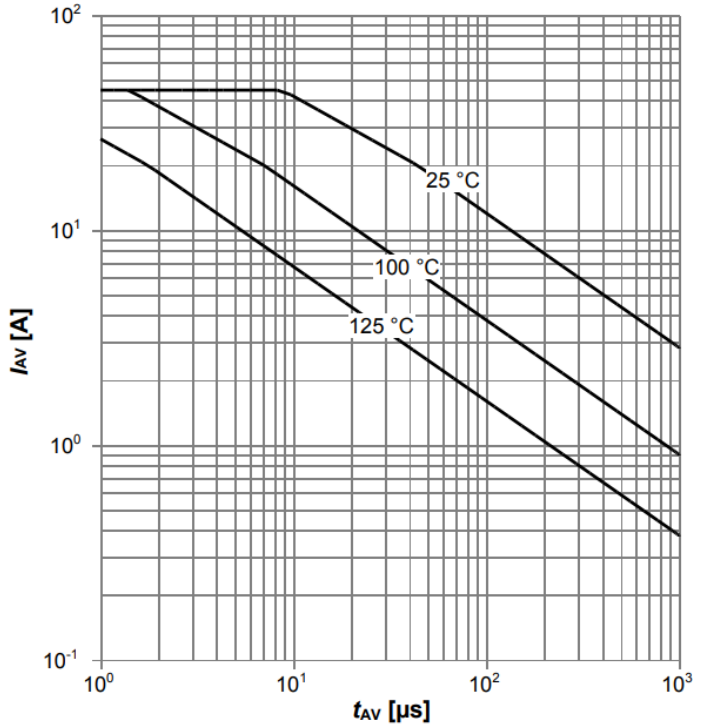
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



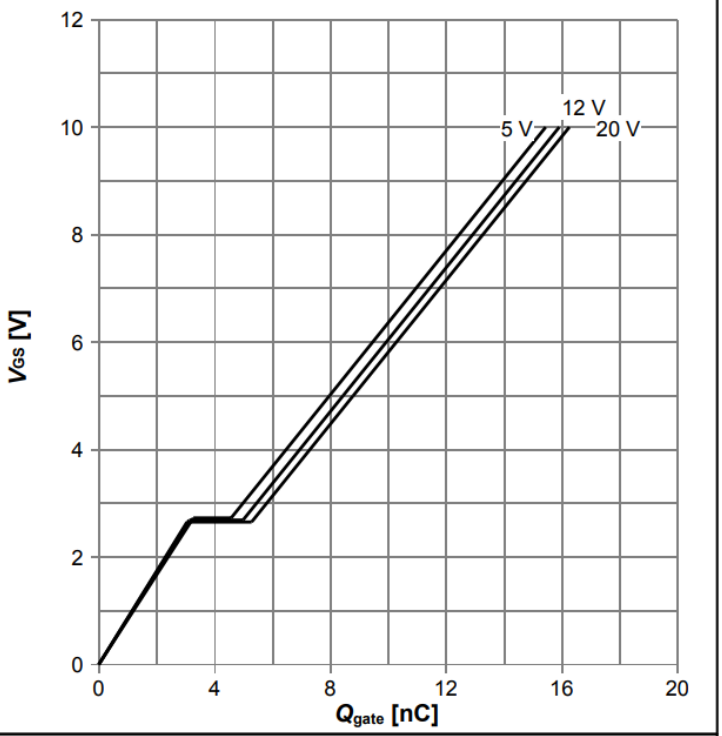
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



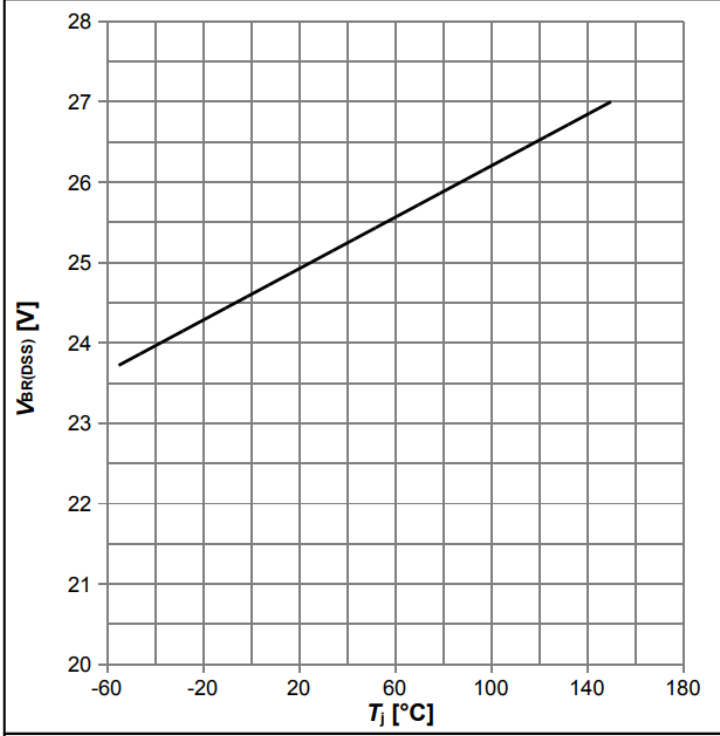
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



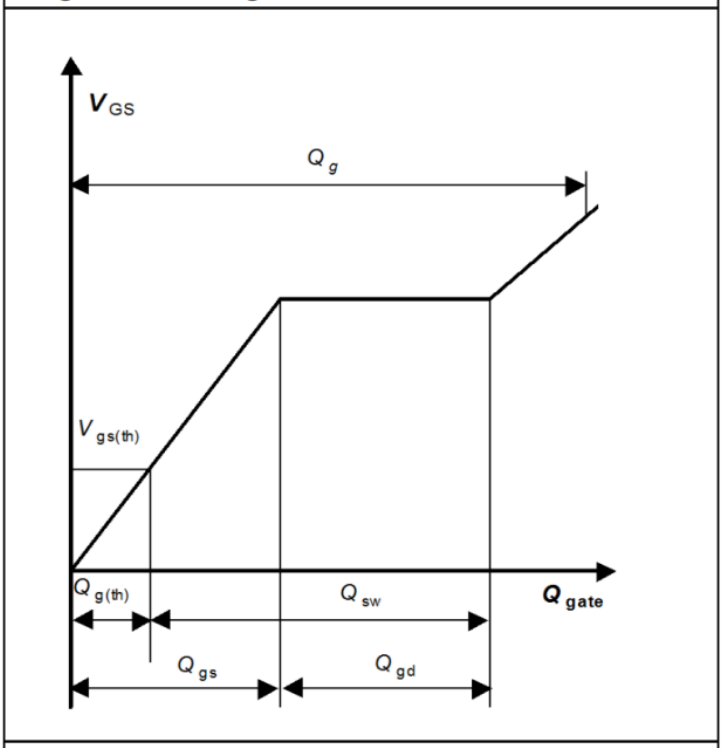
V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

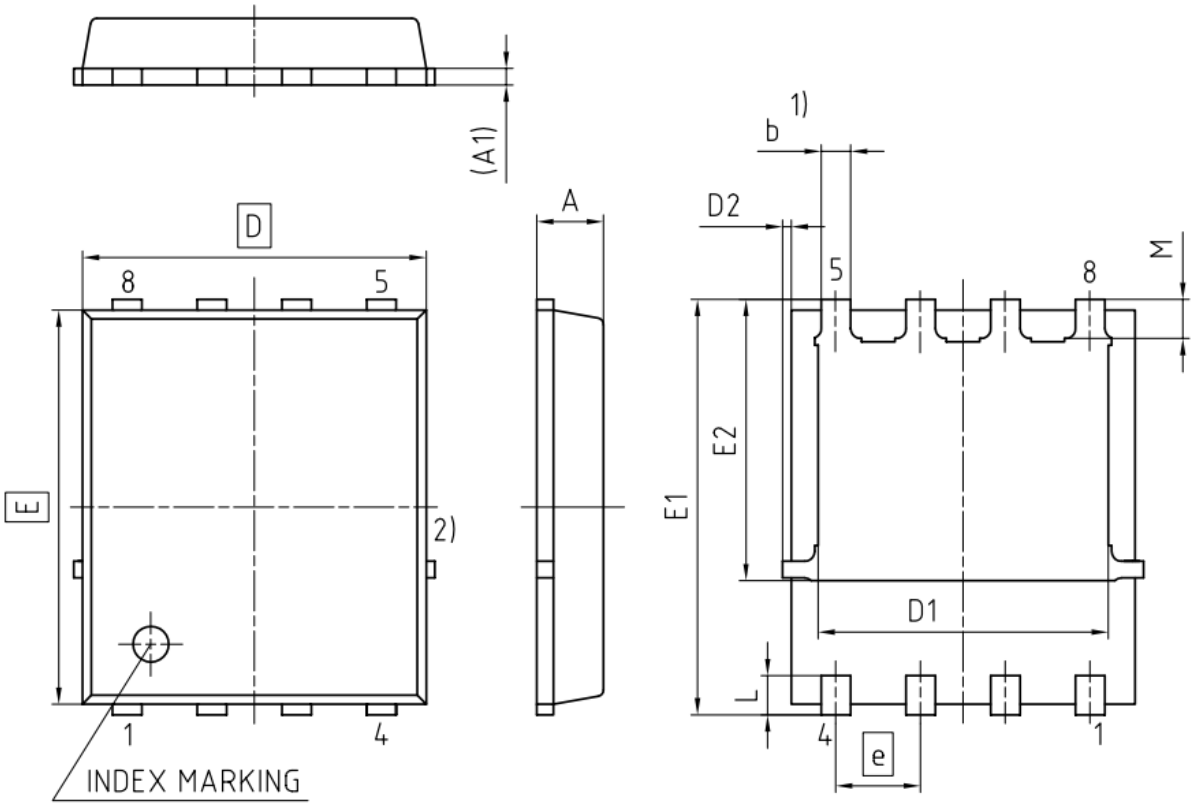


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 封装外形

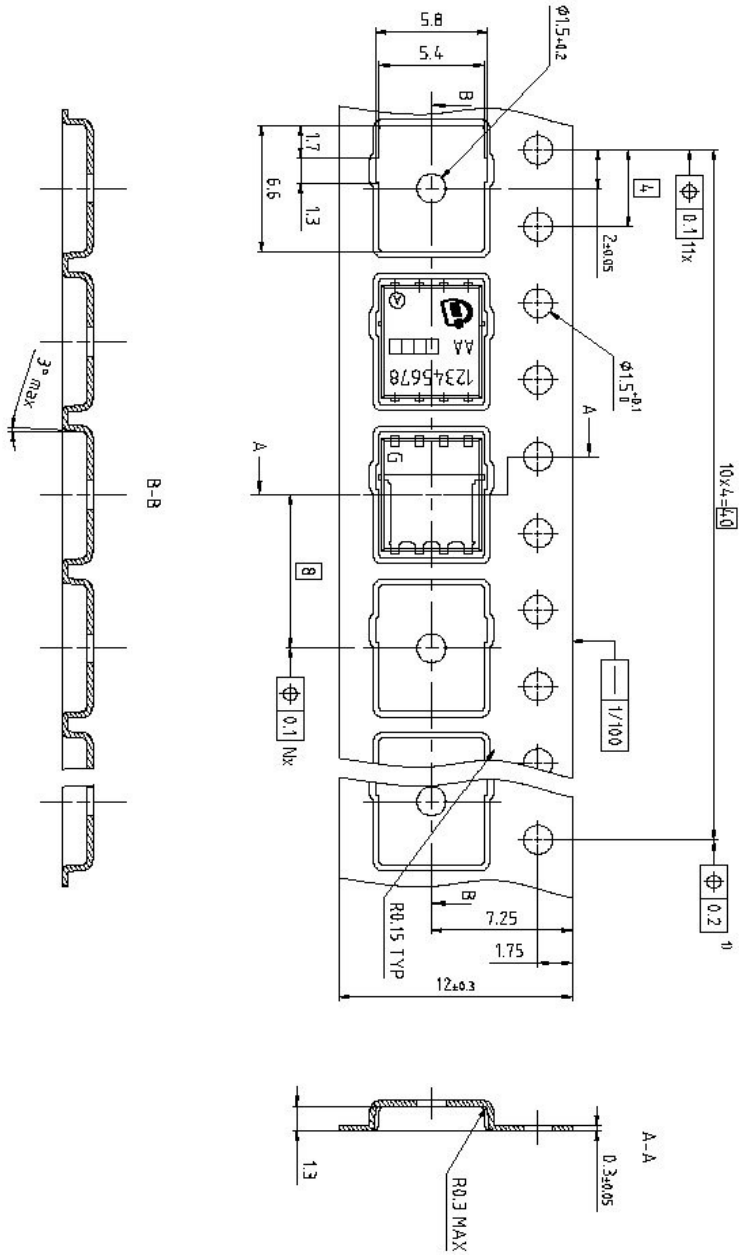


1) EXCLUDING MOLD FLASH
2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
LEAD LENGTH UP TO ANTI FLASH LINE
ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.03	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

DOCUMENT NO.
Z8B00003332
REVISION
07
SCALE 10:1
0 1 2 3mm
EUROPEAN PROJECTION
ISSUE DATE
06.06.2019

图 1 PG-TDSON-8 外形图，尺寸单位为毫米



尺寸（毫米）

图2　　封装外形胶带（TDSON-8）

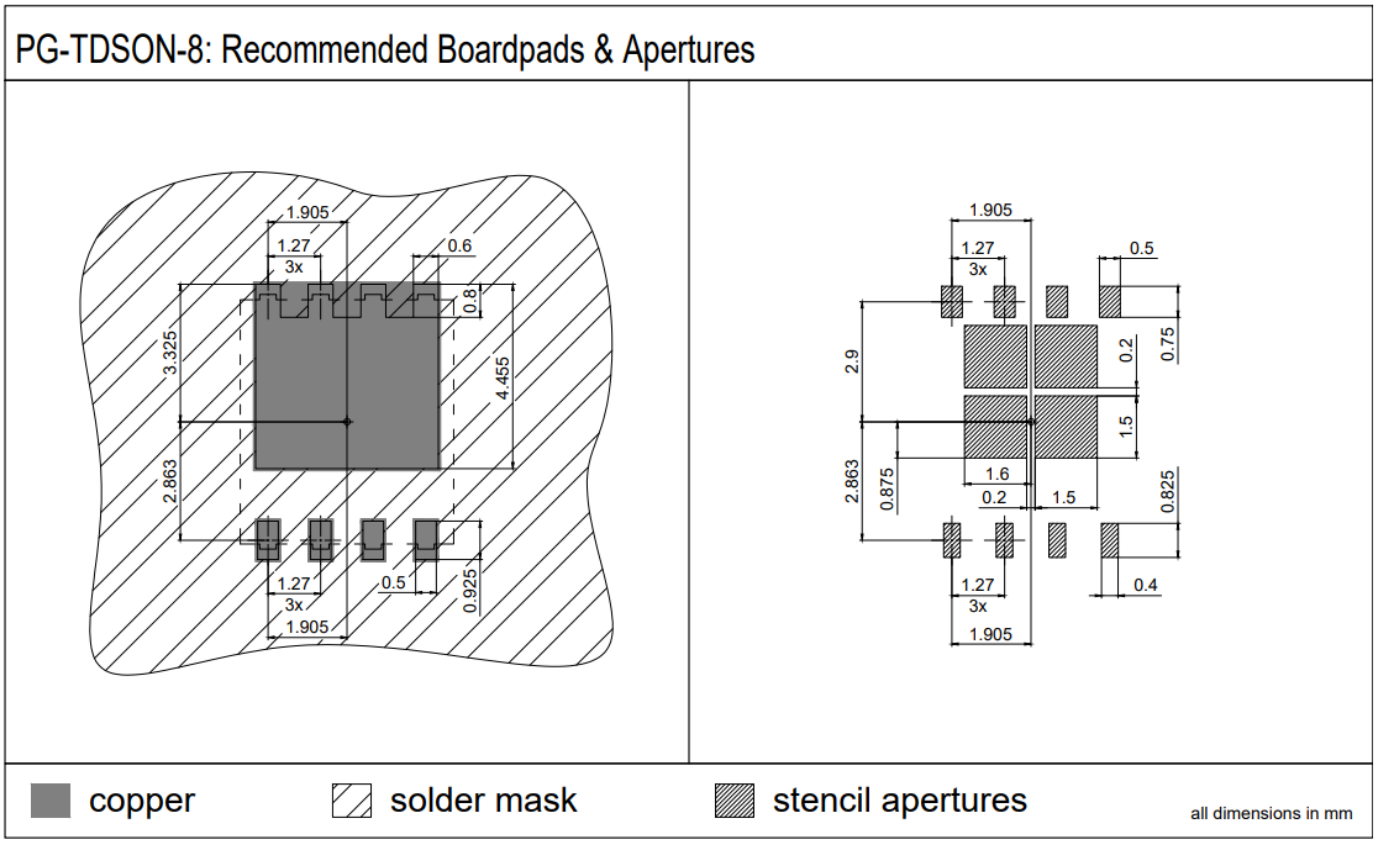


图 3　　外形板焊盘 (TDSON-8)，尺寸单位为毫米

修订记录

BSC032NE2LS

Revision: 2019-11-04, Rev. 2.3

历史修订版本

Revision	Date	Subjects (major changes since last revision)
2.3	2019-11-04	Update package drawings

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München, Germany
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版本 **2025-12-24**

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