

MOSFET

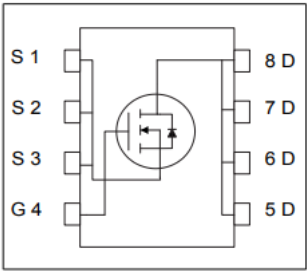
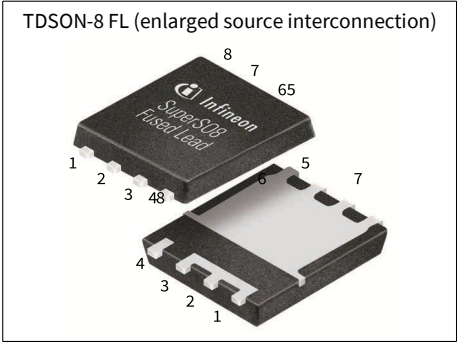
英飞凌高耐热60V OptiMOS™功率 MOSFET

特性

- 针对同步整流进行了优化
- 额定温度为 175°C
- 100% 雪崩测试
- 卓越的耐热性
- N沟道
- 符合 JEDEC ¹⁾ 工业应用标准
- 无铅镀层；符合RoHS标准
- 符合 IEC61249-2-21 标准的无卤素
- 源极互连尺寸增大，焊点可靠性更高

表 1 主要性能参数

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	1.6	mΩ
I_D	234	A
Q_{oss}	81	nC
$Q_g(0V..10V)$	71	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
BSC016N06NST	PG-TDSO-8 FL	016N06NT	-

¹⁾ J-STD20 和 JESD22

本数据手册的原文使用英文撰写。为方便起见，英飞凌提供了译文；由于翻译过程中可能使用了自动化工具，英飞凌不保证译文的准确性。为确认准确性，请务必访问 infineon.com 参考最新的英文版本（控制文档）。

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1 最大额定值

除非另有规定, $T_j = 25\text{ °C}$

表 2 最大额定值

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	234 164 31	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ K/W}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	936	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	380	mJ	$I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	167 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ K/W}$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	-

2 热特性

表3 热特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.5	0.9	K/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	K/W	-
Device on PCB, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	50	K/W	-

¹⁾额定值指产品仅具有数据表指定的绝对最大值, 保持外壳温度符合规定要求。其他外壳温度请参见图 2。需要根据实际环境条件降低额定值。

²⁾器件安装在 40 mm x 40 mm x 1.5 mm 环氧树脂印刷电路板 FR4 上, 漏极连接用铜面积为 6 cm² (一层, 70 μm 厚)。印刷电路板垂直放置在静止空气中。

³⁾详细信息请参见图 3

⁴⁾详细信息请参见图 13

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3 电气特性

除非另有规定, $T_j = 25\text{ }^{\circ}\text{C}$

表4 静态特性

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}$, $I_D=95\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.5 10	1 100	μA	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ }^{\circ}\text{C}$ $V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ }^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.4 1.9	1.6 2.4	m Ω	$V_{GS}=10\text{ V}$, $I_D=50\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=12.5\text{ A}$
Gate resistance ¹⁾	R_G	-	1.9	2.9	Ω	-
Transconductance	g_{fs}	70	140	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=50\text{ A}$

表5 动态特性¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	3900	5200	6500	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	900	1200	1500	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	14	48	96	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	19	38	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	9	18	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	35	70	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	9	18	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=30\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

表6 栅极电荷特性²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	16	22	30	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	10	14	19	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	8.8	13	20	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	14	21	30	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	58	71	95	nC	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	3.7	4.3	4.9	V	$V_{DD}=30\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	49	62	86	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	60	81	102	nC	$V_{DD}=30\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾由设计标定, 不受制于生产测试。

²⁾参数定义请参见“栅极电荷波形”。由设计标定, 不受制于生产测试。

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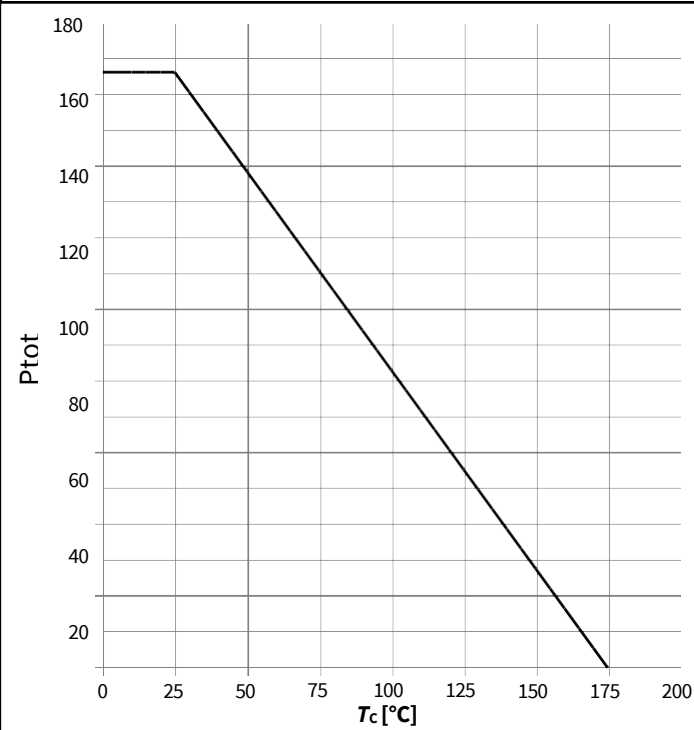
表 7 反向二极管

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	167	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	936	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.9	1.2	V	$V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	24	61	98	ns	$V_R=30\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	39	78	156	nC	$V_R=30\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾由设计标定，不受制于生产测试。

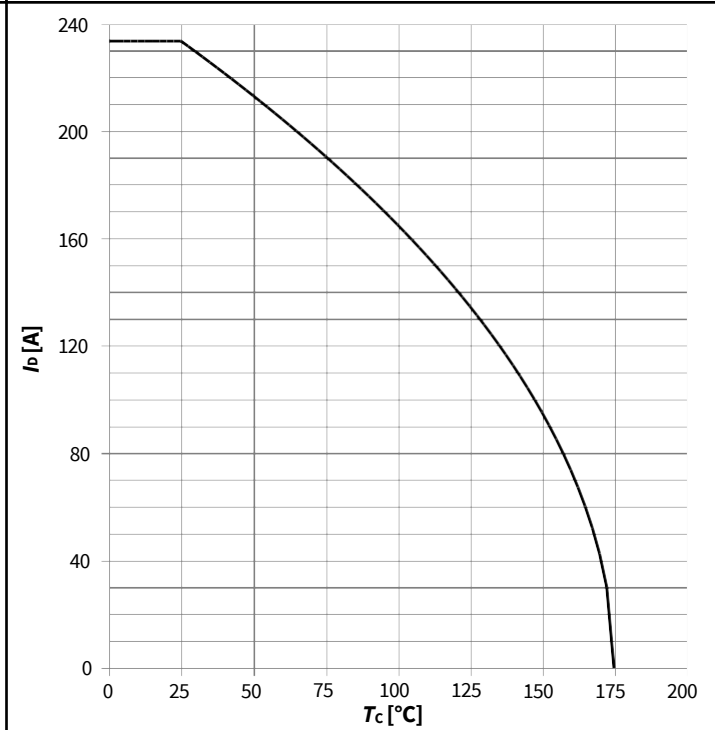
4 电气特性图

图 1: 功率耗散



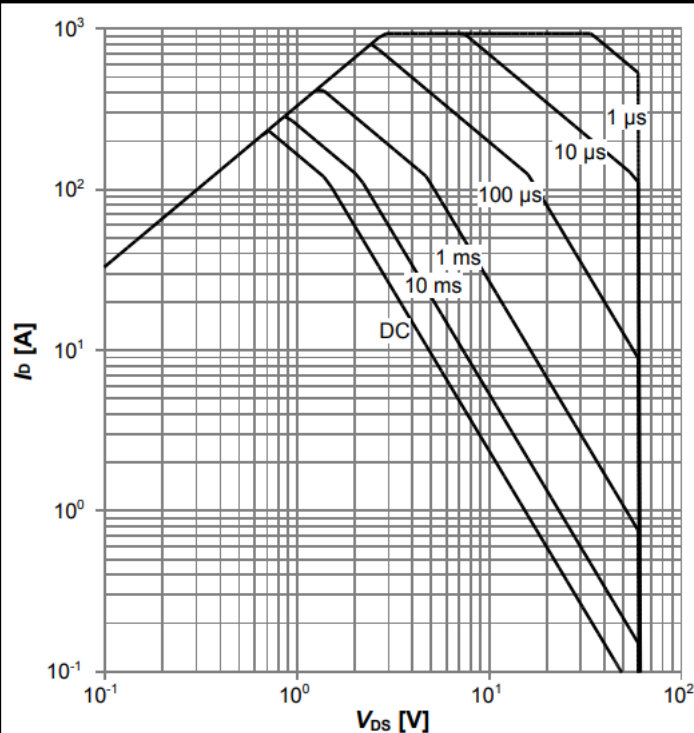
$$P_{tot}=f(T_c)$$

图 2: 漏极电流



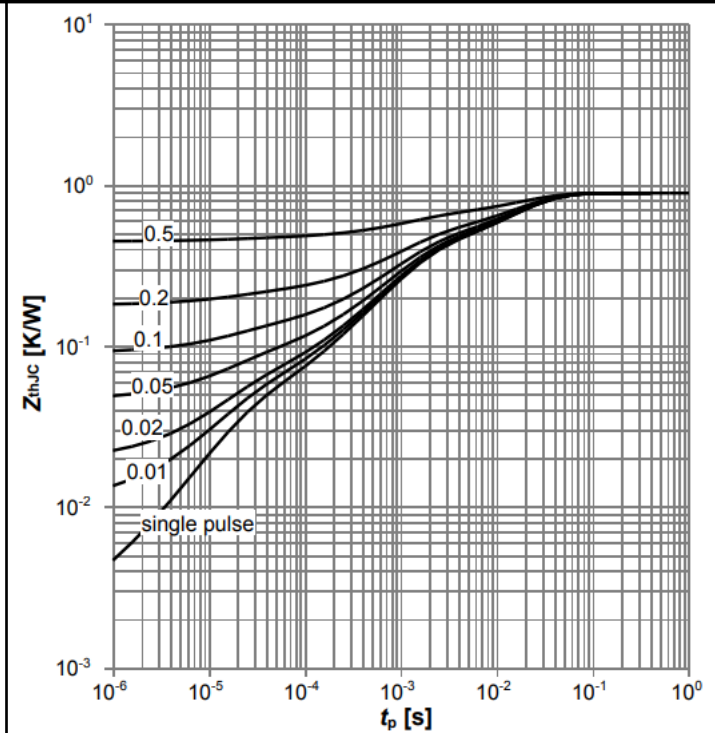
$$I_D=f(T_c); V_{GS}\geq 10\text{ V}$$

图 3: 安全操作区



$$I_D=f(V_{DS}); T_c=25\text{ °C}; D=0; \text{参数: } t_p$$

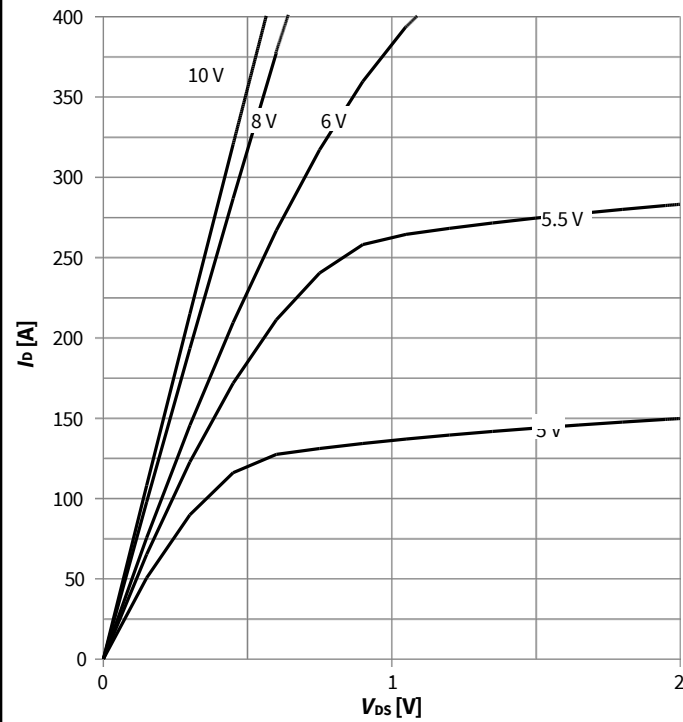
图 4: 最大瞬态热阻抗



$$Z_{thJC}=f(t_p); \text{参数: } D=t_p/T$$

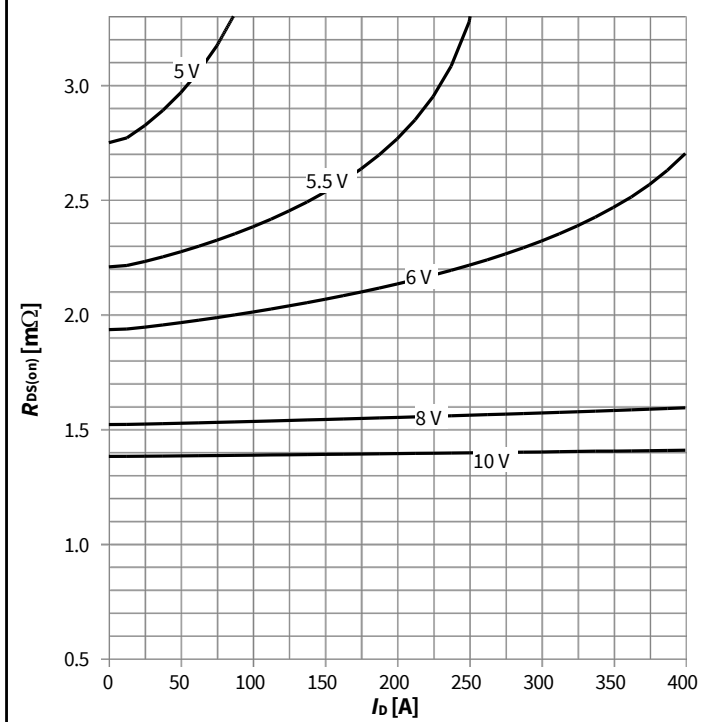
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图 5：典型输出特性



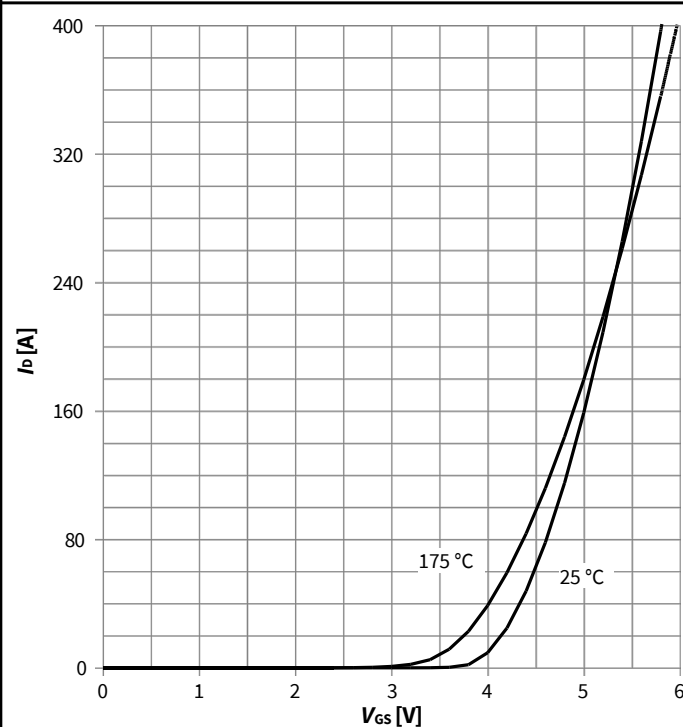
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; 参数: V_{GS}

图 6：典型漏源导通电阻



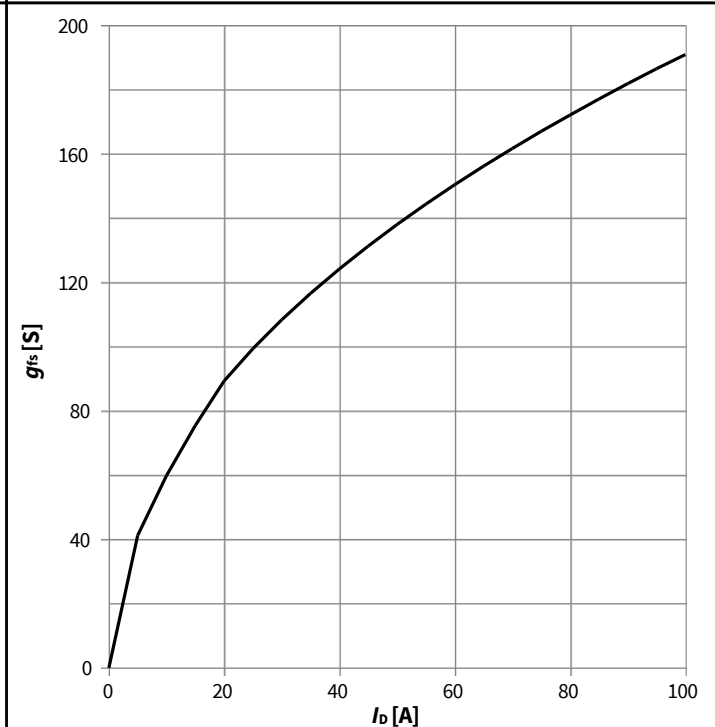
$R_{DS(on)} = f(I_D)$; $T_j = 25^\circ\text{C}$; 参数: V_{GS}

图 7：典型转移特性



$I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D|R_{DS(on)max}$; 参数: T_j

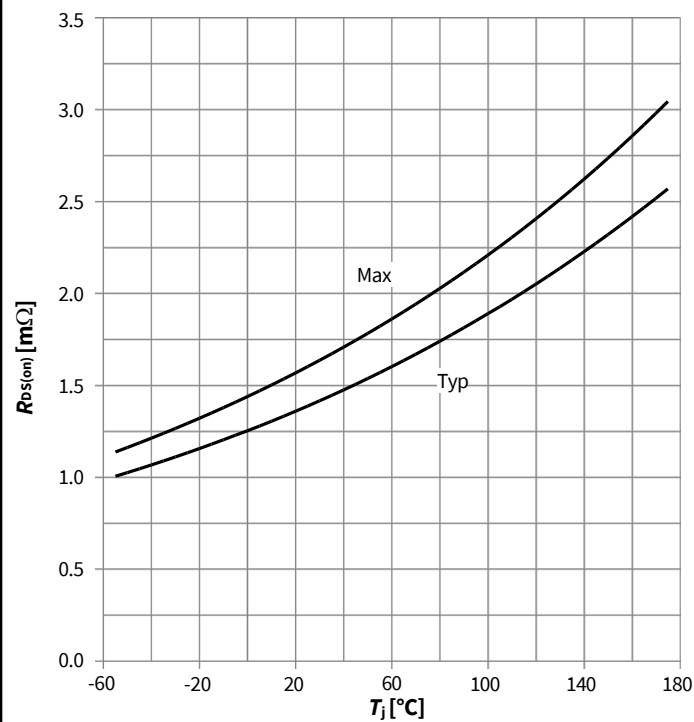
图 8：典型正向跨导



$g_{fs} = f(I_D)$; $T_j = 25^\circ\text{C}$

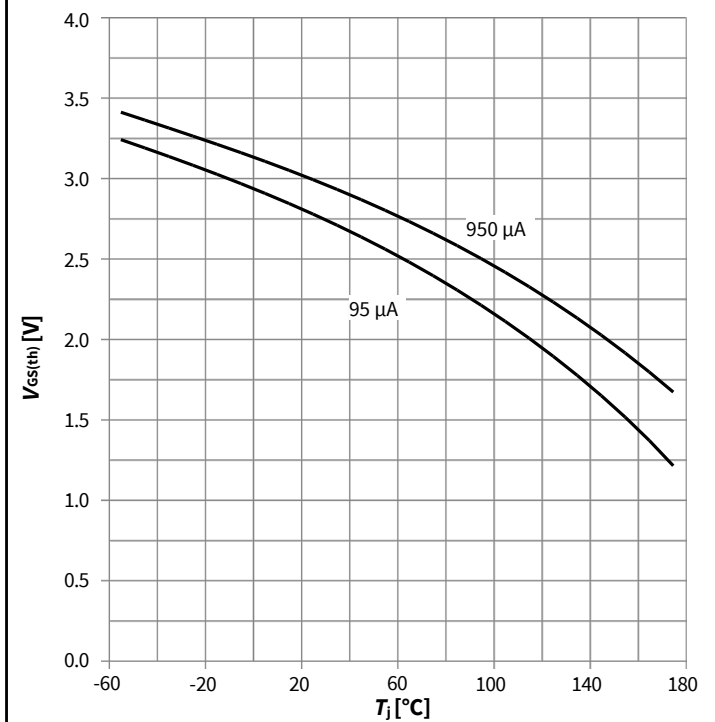
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图 9: 漏源导通电阻



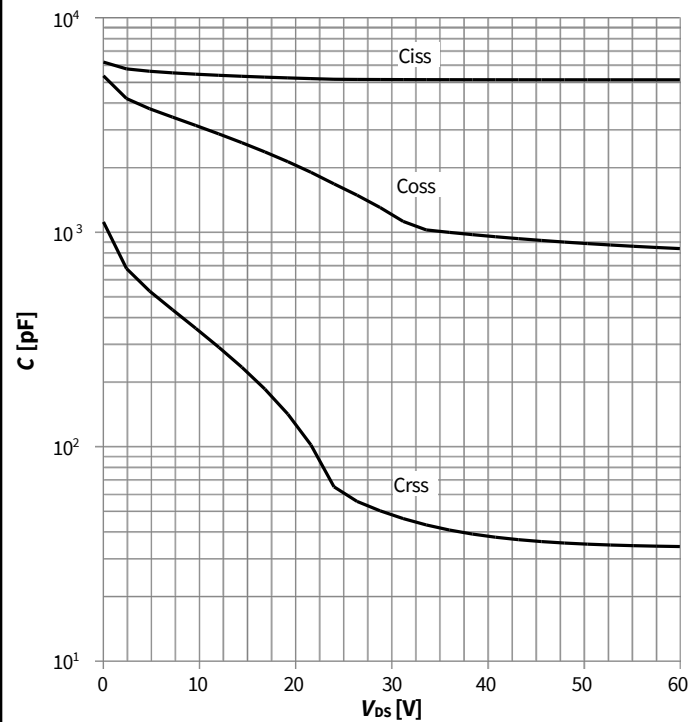
$$R_{DS(on)} = f(T_j); I_D = 50 \text{ A}; V_{GS} = 10 \text{ V}$$

图 10: 典型栅极阈值电压



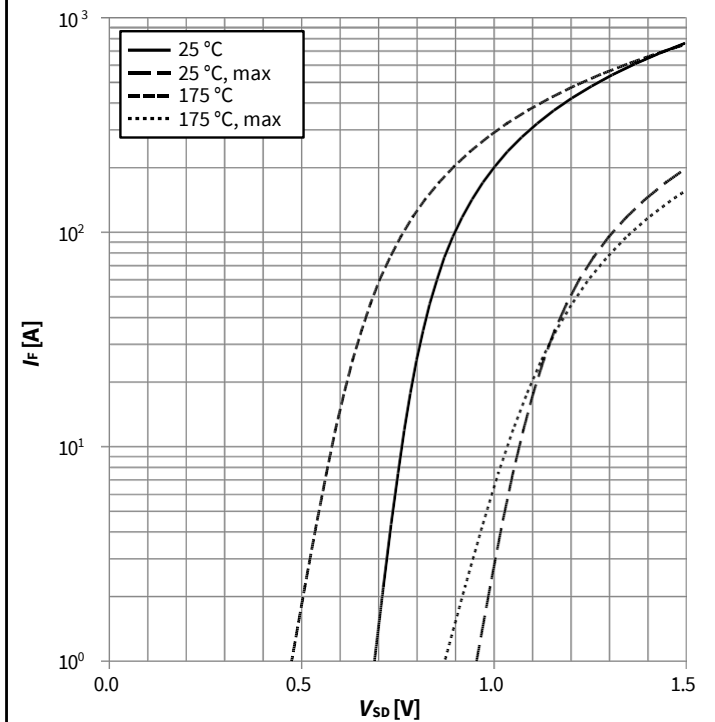
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

图 11: 典型电容值



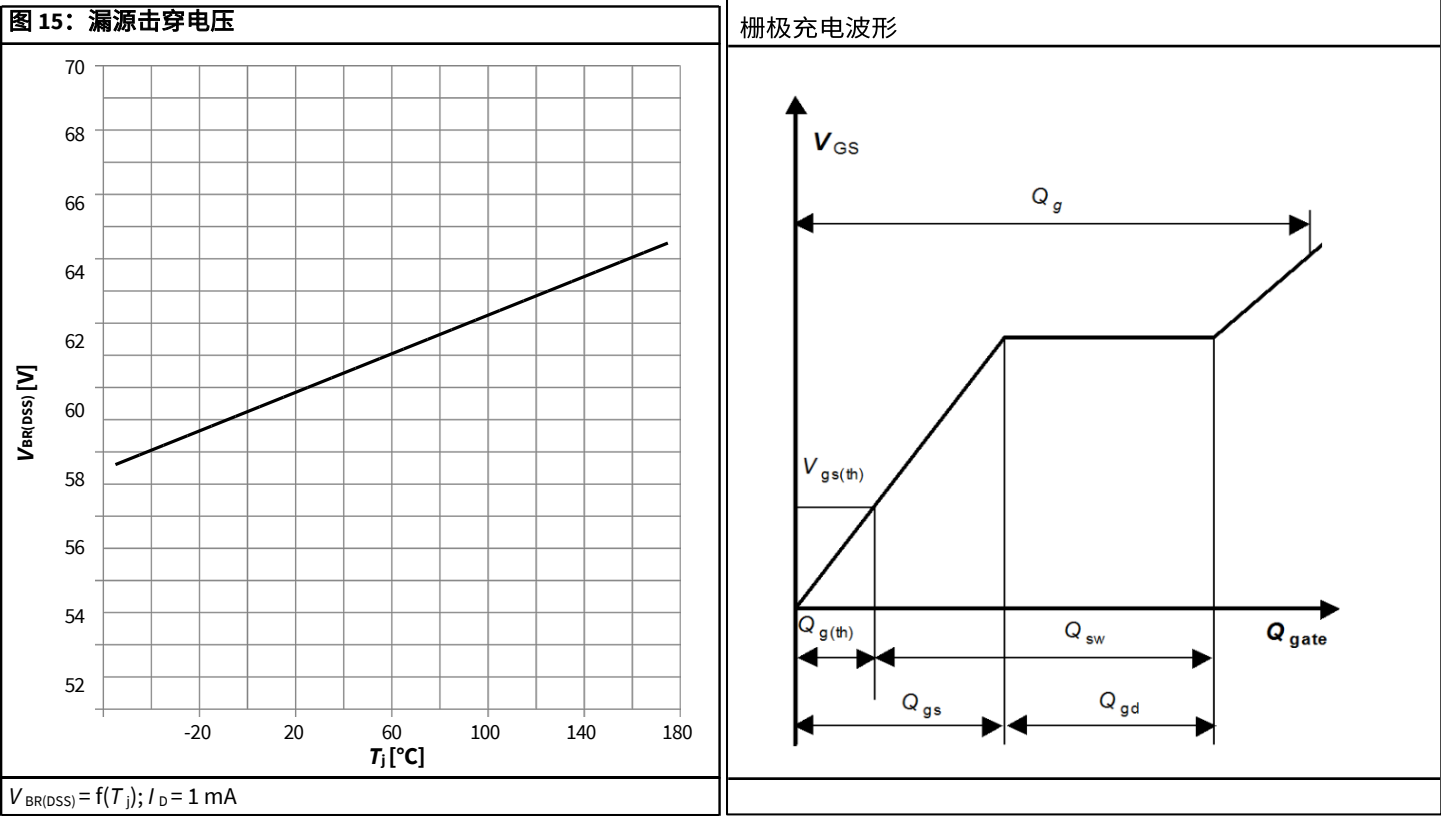
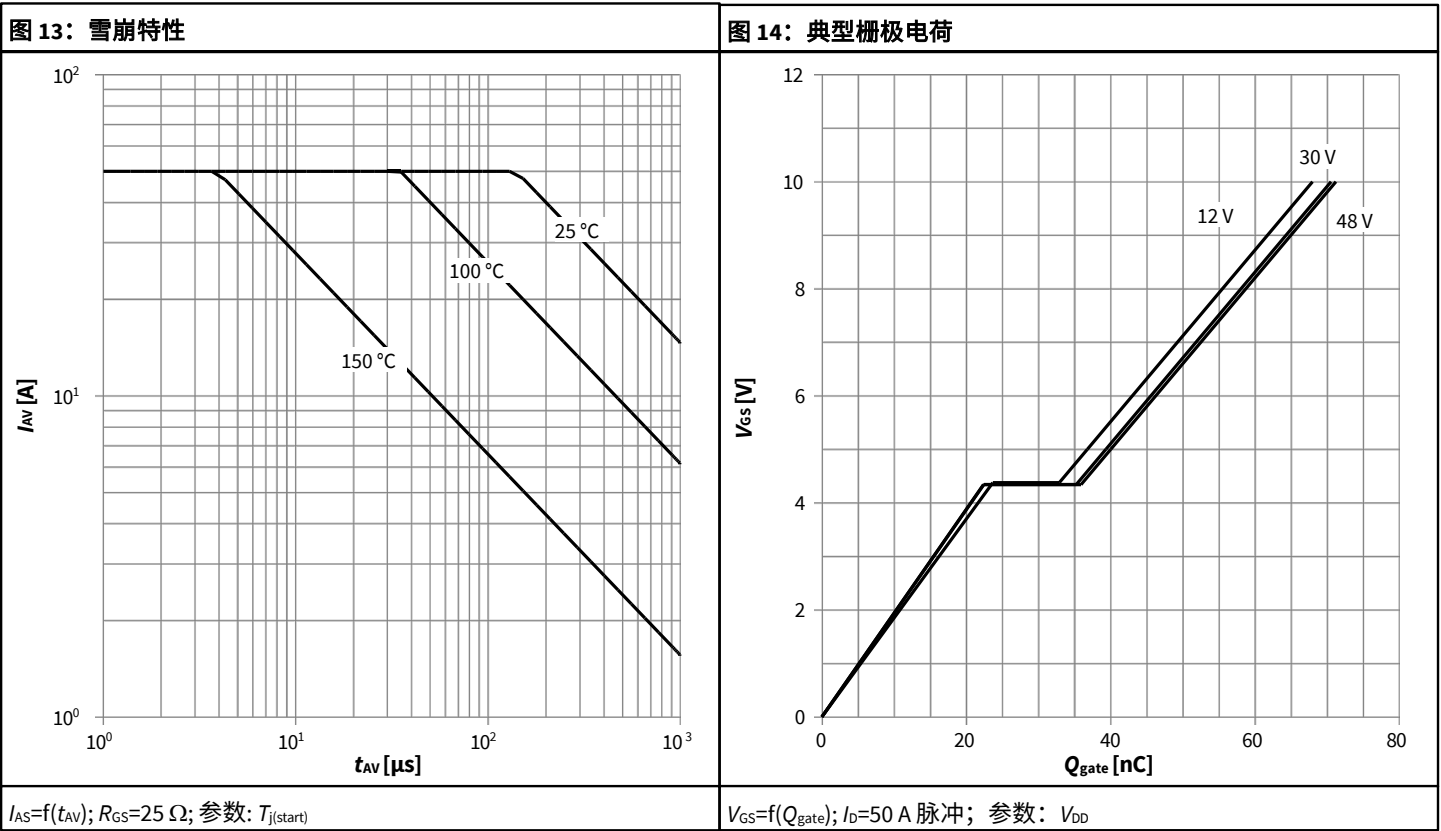
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

图 12: 反向二极管的正向特性

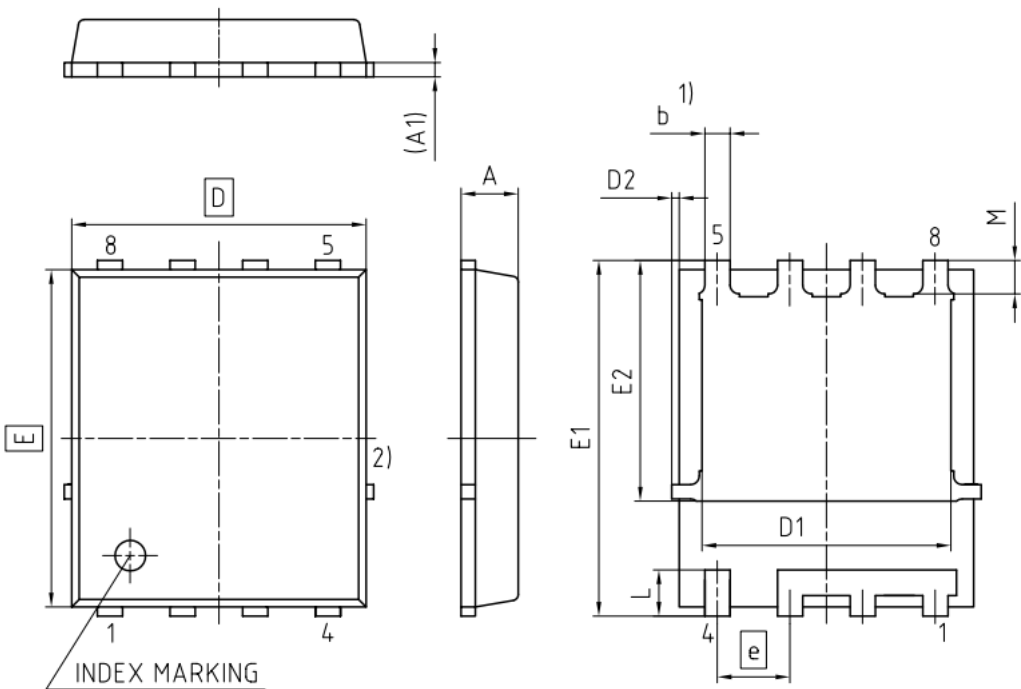


$$I_F = f(V_{SD}); \text{参数: } T_j$$

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5 封装外形



1) EXCLUDING MOLD FLASH
 2) REMOVAL ON MOLD GATE
 INTRUSION 0.1 MM
 PROTRUSION 0.1 MM
 LEAD LENGTH UP TO ANTI FLASH LINE
 ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.26	0.54
D	4.40	5.44
D1	3.70	4.40
D2	0.02	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.42
e	1.27	
L	0.69	0.90
M	0.45	0.69

DOCUMENT NO.
 Z8B000193699

REVISION
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EUROPEAN PROJECTION

ISSUE DATE
 19.06.2019

图 1 PG-TDSON-8 FL 外形图，尺寸单位为毫米

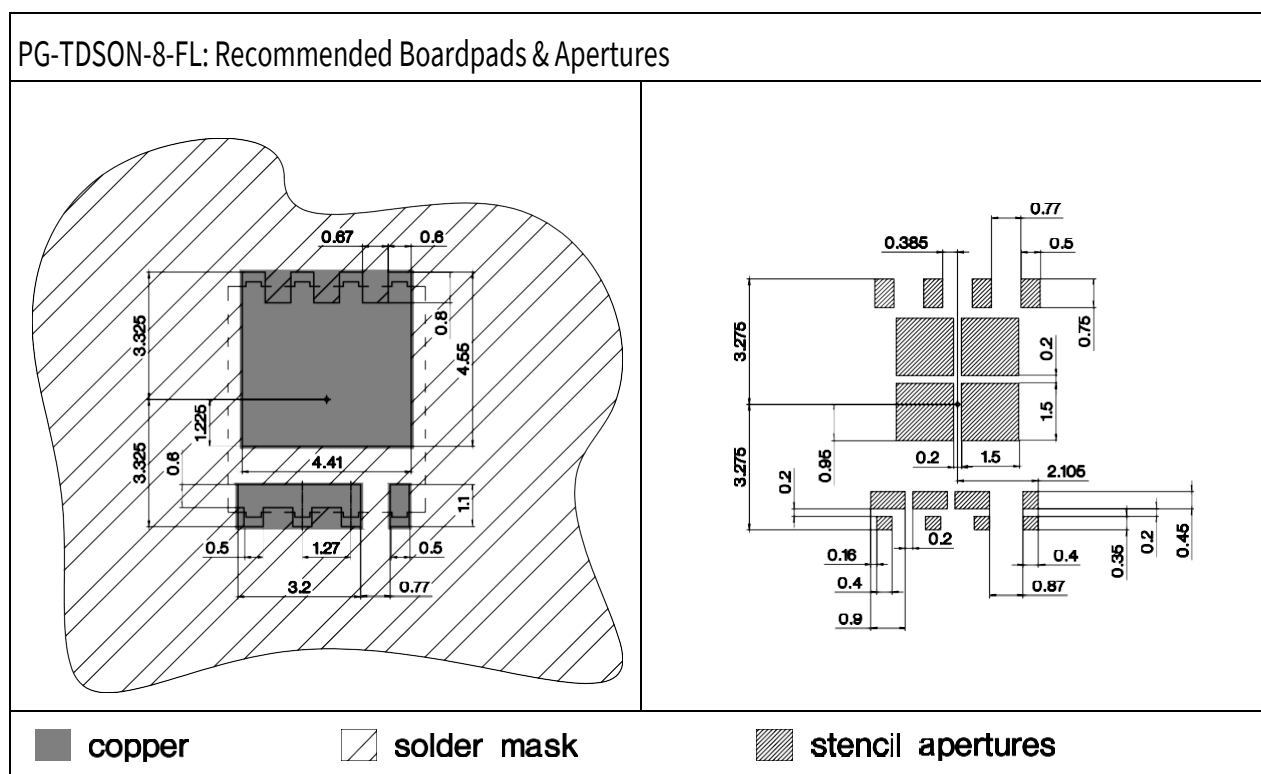


图2 外形板焊盘 (TDSO-8 FL)

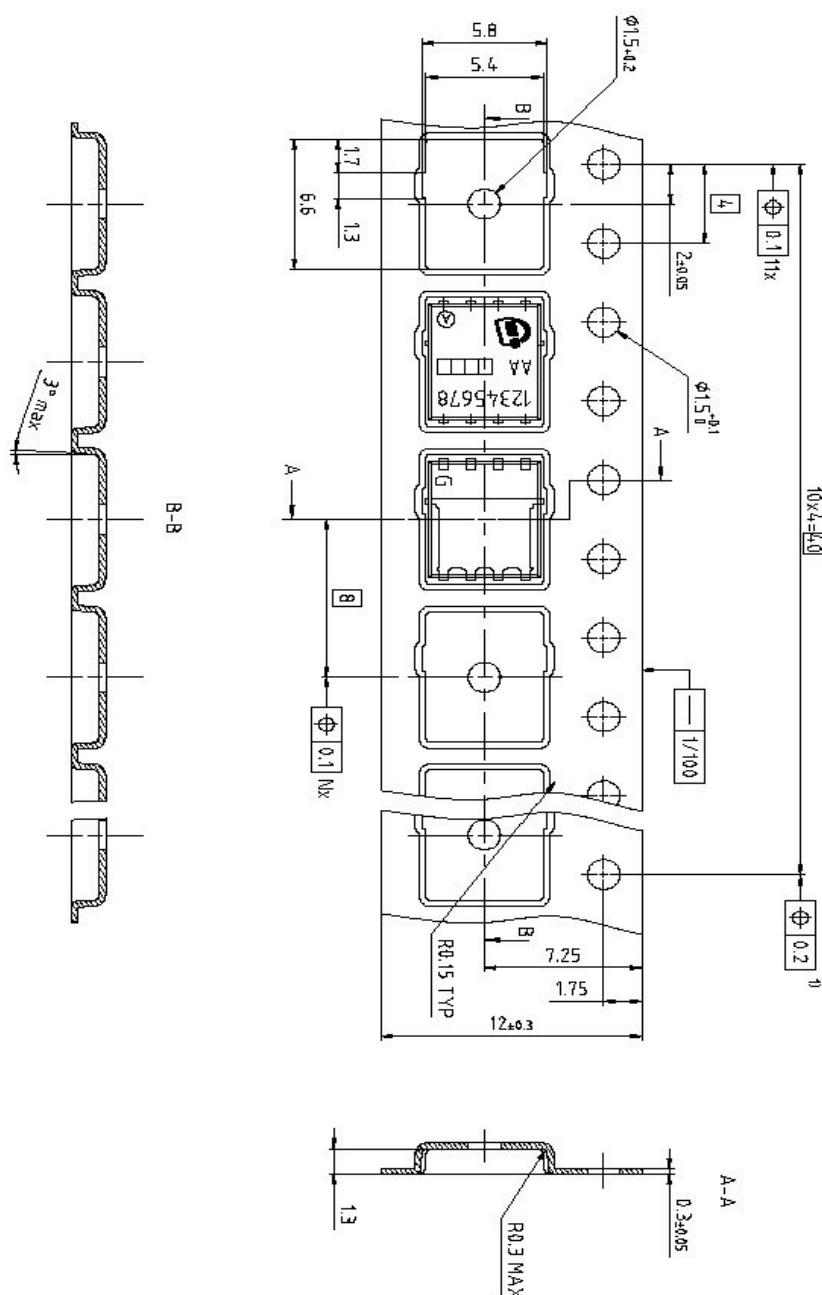


图 3 封装外形胶带 (TDSO-8 FL)

修订记录

BSC016N06NST

Revision: 2020-08-13, Rev. 2.2

历史修订版本

Revision	Date	Subjects (major changes since last revision)
2.0	2017-03-01	Release of final version
2.1	2019-10-22	Update package drawings
2.2	2020-08-13	Update current rating

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Infineon Technologies AG 81726

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Edition 2025-04-21

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