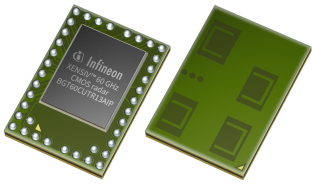
Features

- Integrated state machine for low-power and real time operation
- Flexible frame definition enabled by hardware sequencer
- 60 GHz radar with 7 GHz bandwidth and ramp speed up to 700 MHz/µs
- Embedded SAR ADCs with 20 MSps
- Antenna in Package (AiP) with ±60° FoV



RoHS

Lead-free

Potential Applications

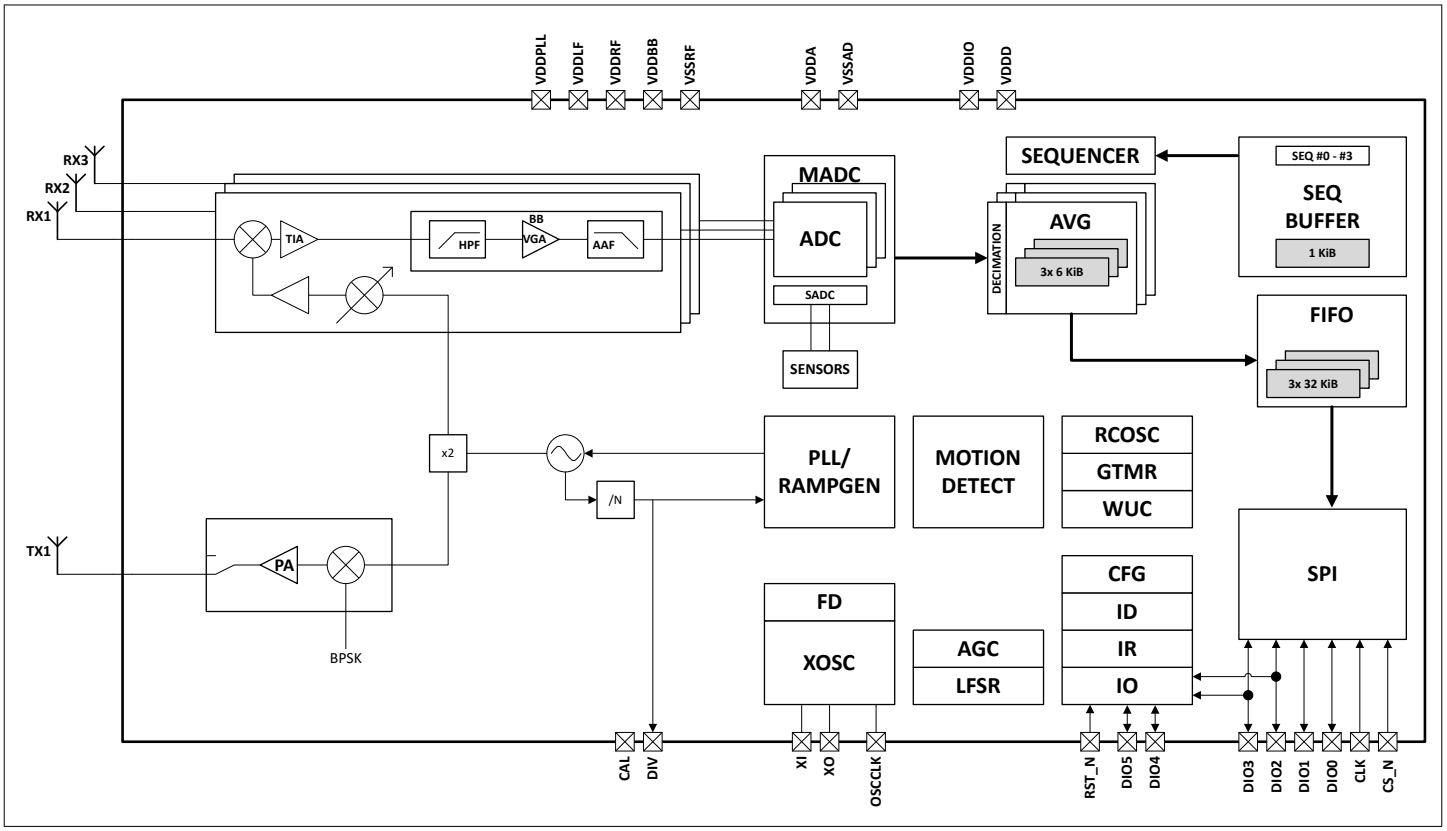
- Presence detection, segmentation and tracking for smart home devices such as TV's, monitors, smart speakers, air conditioners and doorbell applications
- Vital sign tracking for health care devices, such as sleep trackers and baby monitors
- Gesture sensing for smart appliances such as kitchen machines or thermostats

Product Validation

Qualified for applications listed above based on the test conditions in the relevant tests of JEDEC JESD47.

Description

The CMOS radar, a 60 GHz radar sensor with antenna in package, provides ultra-wide bandwidth FMCW operation with a single chip solution inside a small package. Sensor configuration, data acquisition trigger and data transfer are enabled by a digital interface so called Serial Peripheral Interface (SPI). An integrated hardware sequencer together with a finite state machine (FSM) offers full flexibility to the user defining configurable chirps and timings while ensuring cycle accurate data acquisition with lowest power consumption. The embedded motion/presence detection block with low false alarm rate reduces further the system power by waking up external hosts via a dedicated interrupt pin.



BGT60CUTR13AIP simplified block diagram

Table of contents

Table of contents . . . 2
1 Pin Configuration . . . 4
1.1 Pin Assignment . . . 4
1.2 Pin Definitions and Functions . . . 5
2 General Product Characteristics . . . 7
2.1 Absolute Maximum Ratings . . . 7
2.2 Functional Range . . . 8
2.3 Thermal Resistance . . . 9
2.4 Current Consumption . . . 9
2.4.1 Current Consumption Overall 1.2 V Domain . . . 9
2.4.2 Current Consumption Overall 1.8 V Domain . . . 9
2.4.3 Current Consumption IO Domain . . . 10
2.4.4 Current Consumption D Domain . . . 10
2.4.5 Current Consumption A Domain . . . 10
2.4.6 Current Consumption PLL Domain . . . 10
2.4.7 Current Consumption RF Domain . . . 11
2.4.8 Current Consumption BB Domain . . . 11
2.4.9 Current Consumption LF Domain . . . 11
2.5 ESD Integrity . . . 12
2.6 Extended Temperature Range . . . 12
3 IO . . . 13
3.1 DIO . . . 13
3.1.1 Electrical Characteristics DIO . . . 13
3.2 Reset . . . 13
3.2.1 Electrical Characteristics RESET . . . 14
3.3 SPI . . . 14
3.3.1 Standard Timing . . . 14
3.3.2 High Speed Timing . . . 15
3.3.3 Electrical Characteristics . . . 16
3.3.4 SPI Operation Modes . . . 16
4 XOSC . . . 19
4.1 Overview . . . 19
4.2 XOSC Parameters . . . 19
5 RCOSC . . . 21
5.1 RCOSC Parameters . . . 21
6 PLL . . . 22
6.1 PLL Parameters . . . 22
6.1.1 Settling Time . . . 22

6.1.2 Ramp Linearity 23

7 RF Frontend 24
7.1 RF FE Parameters 24
7.2 On-chip Sensor Parameters 25

8 Analog Baseband 26
8.1 Analog Baseband Current Consumption 26
8.2 Analog Baseband HPF Parameters 27
8.3 Analog Baseband Gain Parameters 27
8.4 Analog Baseband AAF Parameters 27

9 ADC 29
9.1 Overview 29
9.2 ADC Parameters 29

10 Package Information 31
10.1 Package 31
10.2 Built-in Antenna Specification 33
10.2.1 Built-in Antenna Parameters 33

11 Terms and Abbreviations 35

12 Revision History 38

Disclaimer 39

1 Pin Configuration

The following Figure 1 shows the transparent top view of laminate package with the pin and antenna number assignment.

1.1 Pin Assignment

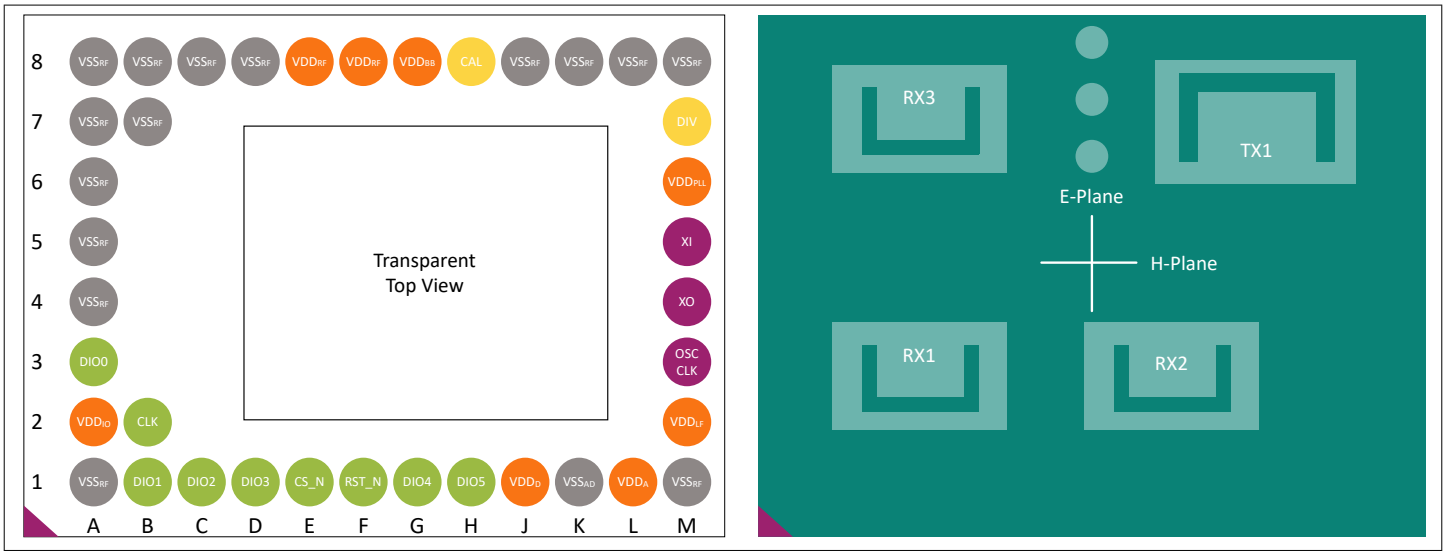


Figure 1 BGT60CUTR13AIP pin out in bottom view (left) and antenna numbers assignment in top view (right)

Ball	Symbol
A1	VSS_{RF}
A2	VDD_{IO}
A3	DIO0
A4	VSS_{RF}
A5	VSS_{RF}
A6	VSS_{RF}
A7	VSS_{RF}
A8	VSS_{RF}
B1	DIO1
B2	CLK
B7	VSS_{RF}
B8	VSS_{RF}
C1	DIO2
C8	VSS_{RF}
D1	DIO3
D8	VSS_{RF}
E1	CS_N
E8	VDD_{RF}

F1	RST_N
F8	VDD_{RF}
G1	DIO4
G8	VDD_{BB}
H1	DIO5
H8	CAL
J1	VDD_{D}
J8	VSS_{RF}
K1	VSS_{AD}
K8	VSS_{RF}
L1	VDD_{A}
L8	VSS_{RF}
M1	VSS_{RF}
M2	VDD_{LF}
M3	OSCCLK
M4	XO
M5	XI
M6	VDD_{PLL}
M7	DIV
M8	VSS_{RF}

1.2 Pin Definitions and Functions

Symbol	Package	Direction	Type	Domain	Description
Supply pins					
VDD_{D}	Yes	Input	Power	Supply	Supply for digital LDO
VDD_{PLL}	Yes	Input	Power	Supply	Supply for PLL
VDD_{LF}	Yes	Input	Power	Supply	Supply for PLL loop filter
VDD_{A}	Yes	Input	Power	Supply	Supply for ADC
VDD_{BB}	Yes	Input	Power	Supply	Supply for BB
VDD_{RF}	Yes	Input	Power	Supply	Supply for RF
VDD_{IO}	Yes	Input	Power	Supply	Supply for IO pads
VSS_{RF}	Yes	Input	Ground	Supply	Ground for PLL and RF
VSS_{AD}	Yes	Input	Ground	Supply	Ground for ADC and digital

Antenna pins					
Test pins					
DIV	Yes	Output	Analog	RF	Divided VCO output
CAL	Yes	Input	Analog	BB	PD calibration
Input output pins					
XI	Yes	Input	Analog	LF	XOSC input (XTAL) or clock input for external oscillator
XO	Yes	Output	Analog	LF	XOSC output (XTAL)
OSCCLK	Yes	Output	Analog	LF	XOSC output clock
RST_N	Yes	Input	Digital	IO	Chip reset (active low)
CS_N	Yes	Input	Digital	IO	SPI chip select (active low)
CLK	Yes	Input	Digital	IO	SPI clock
DIO0	Yes	Input Output	Digital	IO	SPI MOSI or SPI IO0
DIO1	Yes	Input Output	Digital	IO	SPI MISO or SPI IO1
DIO2	Yes	Input Output	Digital	IO	DIO or SPI IO2
DIO3	Yes	Input Output	Digital	IO	DIO or SPI IO3
DIO4	Yes	Input Output	Digital	IO	DIO
DIO5	Yes	Input Output	Digital	IO	DIO

2 General Product Characteristics

2.1 Absolute Maximum Ratings

Table 1 Absolute maximum ratings

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
RF input power level	P_{RF}	-	-	7	dBm	At RX input port
Storage temperature	T_{stg}	-40	-	150	°C	-
Supply						
Supply Digital	VDD_D	-0.3	-	1.32	V	-
Supply PLL	VDD_{PLL}	-0.3	-	1.32	V	-
Supply Loop Filter	VDD_{LF}	-0.3	-	2	V	-
Supply ADC	VDD_A	-0.3	-	2	V	-
Supply Base Band	VDD_{BB}	-0.3	-	2	V	-
Supply RF	VDD_{RF}	-0.3	-	1.32	V	-
Supply IO	VDD_{IO}	-0.3	-	2	V	-
Functional						
Chip Reset	*RST_N*	-0.3	-	2	V	-
SPI Chip Select	*CS_N*	-0.3	-	2	V	-
SPI Clock	*CLK*	-0.3	-	2	V	-
Digital IO	*DIO*	-0.3	-	2	V	-
XTAL input	*XI*	-0.2	-	1.89	V	DC
XTAL output	*XO*	-0.2	-	1.89	V	DC
Oscillator clock out	*OSCCLK*	-0.2	-	1.15	V	AC
Test						
RF Divider	*DIV*	-0.4	-	1.15	V	AC
Calibration	*CAL*	-0.3	-	2	V	-

Attention: ***Stresses above the maximum values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and lifetime. Functionality of the device might not be given under these conditions.***

2.2 Functional Range

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Backside temperature	T_b	-20	-	85	°C	Measured with the on-chip temperature sensor
Frequency range	f_{RF}	57	-	63.36	GHz	MASH3 3rd order (SDMALGO_SEL=2_D) Phase noise and chirp linearity optimized
Frequency range	f_{RF}	57	-	64	GHz	Rhee/DeMuer 3rd order (SDMALGO_SEL=0_D) Bandwidth and best resolution optimized
System clock frequency	f_{SYSCLK}	75	80	85	MHz	
Low power clock frequency	f_{RCOSC}	71	80	84	kHz	
Supply						
Supply Digital	VDD_D	1.14	1.2	1.26	V	± 5 %
Supply PLL	VDD_{PLL}	1.14	1.2	1.26	V	± 5 %
Supply Loop Filter	VDD_{LF}	1.71	1.8	1.89	V	± 5 %
Supply ADC	VDD_A	1.71	1.8	1.89	V	± 5 %
Supply Base Band	VDD_{BB}	1.71	1.8	1.89	V	± 5 %
Supply RF	VDD_{RF}	1.14	1.2	1.26	V	± 5 %
Supply IO 1V2	VDD_{IO}	1.14	1.2	1.26	V	± 5 %
Supply IO 1V8	VDD_{IO}	1.71	1.8	1.89	V	± 5 %
Ground Digital	VSS_D	-	0	-	V	-
Ground ADC	VSS_A	-	0	-	V	-
Ground RF	VSS_{RF}	-	0	-	V	-
Functional						
Chip Reset	*RST_N*	0	1.2	1.26	V	VDDIO = 1.2 V
SPI Chip Select	*CS_N*	0	1.2	1.26	V	VDDIO = 1.2 V
SPI Clock	*CLK*	0	1.2	1.26	V	VDDIO = 1.2 V
Digital IO	*DIO*	0	1.2	1.26	V	VDDIO = 1.2 V
XTAL input	*XI*	0	0.9	0.99	V	-
XTAL output	*XO*	0	0.9	0.99	V	-
Oscillator clock out	*OSCCLK*	0	0.9	0.99	V	-

(table continues...)

Table 2 (continued) Functional range

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Test						
Calibration	*CAL*	0	1.8	1.98	V	-

***Note**: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.*

2.3 Thermal Resistance

Table 3 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Package thermal resistance	R_{th}	-	35	-	K/W	Chip backside to ambient temperature

2.4 Current Consumption

2.4.1 Current Consumption Overall 1.2 V Domain

Table 4 Current consumption overall 1.2 V domain

$VDD_D = VDD_{PLL} = VDD_{RF}$ = 1.26V, *T*b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Idd Deep Sleep	Idd_{DS}	0.02	0.1	1.8	mA	All off
Idd Active	Idd_{ACTIVE}	200	345	500	mA	XOSC active, analog modules powered up and PA active

2.4.2 Current Consumption Overall 1.8 V Domain

Table 5 Current consumption overall 1.8 V domain

$VDD_{IO} = VDD_{LF} = VDD_A = VDD_{BB}$ = 1.89V, *T*b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Idd Deep Sleep	Idd_{DS}	0	0.0001	0.004	mA	All off
Idd Active	Idd_{ACTIVE}	20	100	150	mA	XOSC active, analog modules powered up and PA active

2.4.3 Current Consumption IO Domain

Table 6 Current consumption supply domain VDDIO

$VDD_D = VDD_{PLL} = VDD_{RF}$ = 1.26V, $VDD_{IO} = VDD_{LF} = VDD_A = VDD_{BB}$ = 1.89V, *T*b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Idd Deep Sleep	Idd_{DS}	0	0.5	2.5	µA	-
Idd Active	Idd_{ACTIVE}	0	0.001	0.0025	mA	-

2.4.4 Current Consumption D Domain

Table 7 Current consumption supply domain VDDD

$VDD_D = VDD_{PLL} = VDD_{RF}$ = 1.26V, $VDD_{IO} = VDD_{LF} = VDD_A = VDD_{BB}$ = 1.89V, *T*b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Idd Deep Sleep	Idd_{DS}	0.02	0.1	1.45	mA	All off
Idd Active	Idd_{ACTIVE}	2	4.2	9	mA	XOSC active, sequencer and FSM active

2.4.5 Current Consumption A Domain

Table 8 Current consumption supply domain VDDA

$VDD_D = VDD_{PLL} = VDD_{RF}$ = 1.26V, $VDD_{IO} = VDD_{LF} = VDD_A = VDD_{BB}$ = 1.89V, *T*b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Idd Deep Sleep	Idd_{DS}	0	0.013	1.5	µA	All off
Idd Idle	Idd_{IDLE}	13.3	14.6	15.6	mA	MADC (4 ADC) powered up, no conversion, inactive. Values verified by CV over DoE
Idd Active 4 ADC's	Idd_{ACTIVE}	13.9	15.2	16.2	mA	ADC active and converting (20 MSps)

2.4.6 Current Consumption PLL Domain

Table 9 Current consumption supply domain VDDPLL

$VDD_D = VDD_{PLL} = VDD_{RF}$ = 1.26V, $VDD_{IO} = VDD_{LF} = VDD_A = VDD_{BB}$ = 1.89V, *T*b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Idd Deep Sleep	Idd_{DS}	0.015	0.20	75.50	µA	-
Idd Active	Idd_{Active}	50	86	108	mA	-

2.4.7 Current Consumption RF Domain

Table 10 Current consumption supply domain VDDRF

$VDD_D = VDD_{PLL} = VDD_{RF}$ = 1.26V, $VDD_{IO} = VDD_{LF} = VDD_A = VDD_{BB}$ = 1.89V, *T*b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Idd Deep Sleep	Idd_{DS}	0	0.40	62	µA	-
Idd Idle	Idd_{IDLE}	0.9	1.2	1.5	mA	Powered up, PA inactive. Values verified by CV over DoE
Idd Active 3 RX	Idd_{ACTIVE}	150	255	303	mA	PA active

2.4.8 Current Consumption BB Domain

Table 11 Current consumption supply domain VDDBB

$VDD_D = VDD_{PLL} = VDD_{RF}$ = 1.26V, $VDD_{IO} = VDD_{LF} = VDD_A = VDD_{BB}$ = 1.89V, *T*b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Idd Deep Sleep	Idd_{DS}	0	0.20	22	µA	-
Idd Idle	Idd_{IDLE}	0.5	0.8	1.1	mA	Power up, RF/BB blocks inactive. Values verified by CV over DoE
Idd Active 2 BB's	Idd_{ACTIVE}	36	44	54	mA	BB blocks active. Values verified by CV over DoE
Idd Active 3 BB's	Idd_{ACTIVE}	35	59	77	mA	BB blocks active

2.4.9 Current Consumption LF Domain

Table 12 Current consumption supply domain VDDLF

$VDD_D = VDD_{PLL} = VDD_{RF}$ = 1.26V, $VDD_{IO} = VDD_{LF} = VDD_A = VDD_{BB}$ = 1.89V, *T*b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Idd Deep Sleep	Idd_{DS}	0	0.04	6	µA	
Idd Active	Idd_{ACTIVE}	4.5	9	14.4	mA	OSCCLK pad disabled

2.5 ESD Integrity

Table 13 ESD integrity

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ESD robustness, HBM	$V_{ESD-HBM}$	-2000	-	2000	V	According to JS-001
ESD robustness, CDM	$V_{ESD-CDM}$	-500	-	500	V	According to JS-002

***Note**:* CDM*: Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.*

HBM*: Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C = 100 pF).*

2.6 Extended Temperature Range

The device is stressed during qualification up to 125°C junction temperature. The stress due to higher temperature range does not damage the functionality of the device. It has been characterized up to +105°C backside temperature (which implies a junction temperature of ~125°C, ~20K higher). The effect of the extended temperature range leads to a degradation of several parameters, including transmitter output power, receiver conversion gain, PLL locking range, etc. Thus, a drop of the performance has to be expected. An overview is reported in the table below for the most important parameters (deviation vs typ values at room temperature).

Table 14 Extended temperature range parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Drop of transmit output power	P_{TX}	TBD	2	TBD	dB	T_b = 105°C
Increase of receiver NFssb @1 MHz	$NFSSB_{RX\_1MHz}$	TBD	2	TBD	dB	T_b = 105°C
Increase of PLL phase noise @ 1MHz offset	PN_{PLL_1MHz}	TBD	3	TBD	dB	T_b = 105°C
Reduction of PLL locking range	*PLL_BW*	TBD	+/-0.5	TBD	GHz	T_b = 105°C
Increase of VDDD domain Idd Deep Sleep	$VDDD\_Idd_{DS}$	TBD	TBD	TBD	µA	T_b = 105°C
Drop of conversion gain	CG_{RX}	TBD	1.5	TBD	dB	T_b = 105°C

3 IO

3.1 DIO

For control and communication purposes, the device comes with several digital input output (DIO) pins.
Some of them are fixed to a certain functionality while others could be flexible mapped to the specific functionality required by the application.

3.1.1 Electrical Characteristics DIO

Table 15 Electrical characteristics DIO

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input						
Low level	V_{IL}	0	-	0.3 * VDD_{IO}	V	-
High level	V_{IH}	0.7 * VDD_{IO}	-	VDD_{IO}	V	-
Minimum hysteresis voltage range	V_{HYST}	0.1	-	-	V	V_{HSYST_H} - V_{HYST_L}, Verified by design
Lower hysteresis level	V_{HYST_L}	0.3 * VDD_{IO}	0.5 * VDD_{IO} - V_{HYST}/2	-	V	Verified by design
Upper hysteresis level	V_{HYST_H}	-	0.5 * VDD_{IO} + V_{HYST}/2	0.7 * VDD_{IO}	V	Verified by design
Output						
Maximum load	C_{LOAD}	-	-	15	pF	-
Current						
Pull-up current	I_{PU}	0	-	15	uA	VDD_{IO} = 1.8 V, Verified by design
Pull-down current	I_{PD}	0	-	30	uA	VDD_{IO} = 1.8 V, Verified by design
Leakage	$I_{LEAKAGE}$	0	-	1	uA	No pin activity

3.2 Reset

For a proper operation the device must be set to a defined state. This is done by applying an asynchronous hardware reset to the complete circuitry.

After all supply voltages are settled and stable at the device input, the RST_N pin must be driven to a low level for at least the minimum T_RES time. Figure 2 illustrates the hardware reset sequence.

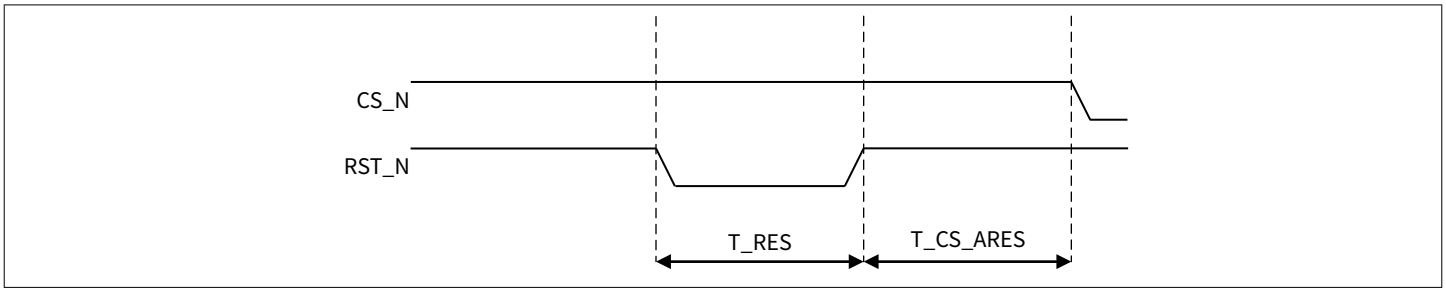


Figure 2 Hardware reset sequence

3.2.1 Electrical Characteristics RESET

Table 16 Electrical characteristics RESET

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Low level	V_{IL}	0	-	0.3 * VDD_{IO}	V	-
High level	V_{IH}	0.7 * VDD_{IO}	-	VDD_{IO}	V	-
Time for active reset	T_{RES}	300	-	-	ns	Verified by design
Time CS after reset	T_{CS_ARES}	5	-	-	µs	Verified by design

3.3 SPI

For communication with the device, a serial peripheral interface (SPI) with mode 0 is provided. It is used to configure the chip in order to operate in the targeted mode and read out the captured sensor data.

The device features up to six DIO pins for SPI communication whereby four of them are fixed in terms of functionality and two of them flexible programmable based on the application needs.

- CS_N to be connected to SS of the SPI master
- CLK to be connected to the CLK of the SPI master
- DIO0 to be connected to the MOSI/IO0 of the SPI master
- DIO1 to be connected to the MISO/IO1 of the SPI master
- DIO2 to be connected to the IO2 of the SPI master (optional, required by Quad SPI)
- DIO3 to be connected to the IO3 of the SPI master (optional, required by Quad SPI)

The device operates in mode 0 with clock polarity (CPOL) and clock phase (CPH) zero.

3.3.1 Standard Timing

The timing diagram for standard SPI timing is presented in the following Figure 3. A SPI transfer is started with a falling edge of chip select signal CS_N generated by the SPI master. At the same time the SPI master shall drive the level of the data input signal DIO0 (MOSI) according to the first bit. Also, with the falling edge of the chip select signal CS_N the SPI slave applies the level of the data on the output signal DIO1 (MISO) according to the first bit which shall

be transferred to the SPI master, the level becomes stable after the period t_{ds}. The SPI master has to wait for the time t_L before the clock signal CLK can be generated. With the rising edge of CLK the SPI slave captures the level of DIO0. The SPI master must keep the DIO0 level stable for t_{sis} before and for t_{sih} after the rising edge of CLK to ensure valid setup and hold time of the SPI slave. With the falling edge of CLK the SPI master shall set the level of DIO0 according to the next bit the master wants to send. The SPI master is supposed to read the level of DIO1 with the rising edge of CLK. The SPI slave keeps the DIO1 level stable for t_{soh} after the falling edge of CLK. With the falling edge of CLK the SPI slave drives the level of DIO1 according to the next bit, DIO1 becomes stable after latest t_{sov}. After the last bit has been transferred and CLK has gone to low level, the SPI master must set CSN to high level to stop the transfer. The master must take care that the period between the last rising edge of CLK and the rising edge of CS_N is not shorter than t_T. Within the period t_{dh} after the rising edge of CS_N the SPI slave drives DIO1 to high impedance state again.

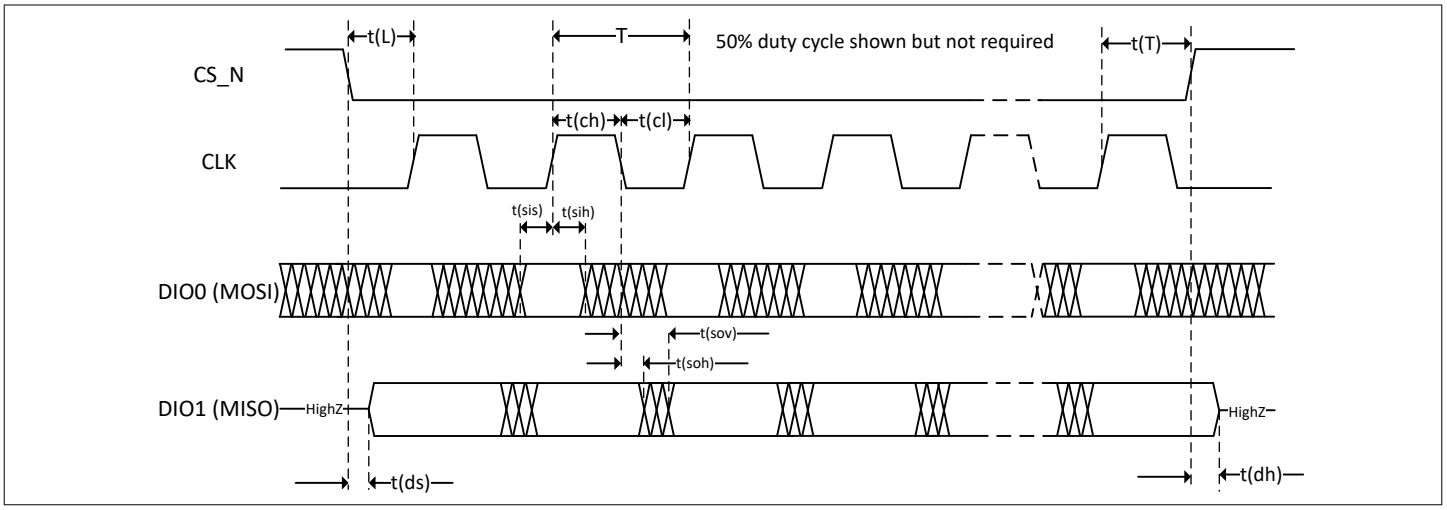


Figure 3 SPI standard timing

3.3.2 High Speed Timing

The device can operate at SPI clock frequencies up to 50 MHz, but the maximum achievable SPI clock frequency is limited by input related setup and hold times of SPI master and SPI slave. In case the SPI master requires a longer setup time than T/2 - t_{sov}, the SPI clock speed in the standard SPI must be reduced. However, this device offers a mode that sends out the data earlier to still allow higher speed. The timing diagram for this SPI mode is presented in the following Figure 4. The SPI master is still supposed to capture the level of DIO1 with the rising edge of CLK. The SPI slave keeps the level of DIO1 stable for t_{soh} after the rising edge of CLK, and then sets the level of DIO1 according to the next bit which is send out. This alternative SPI mode enables frequencies higher than 25 MHz.

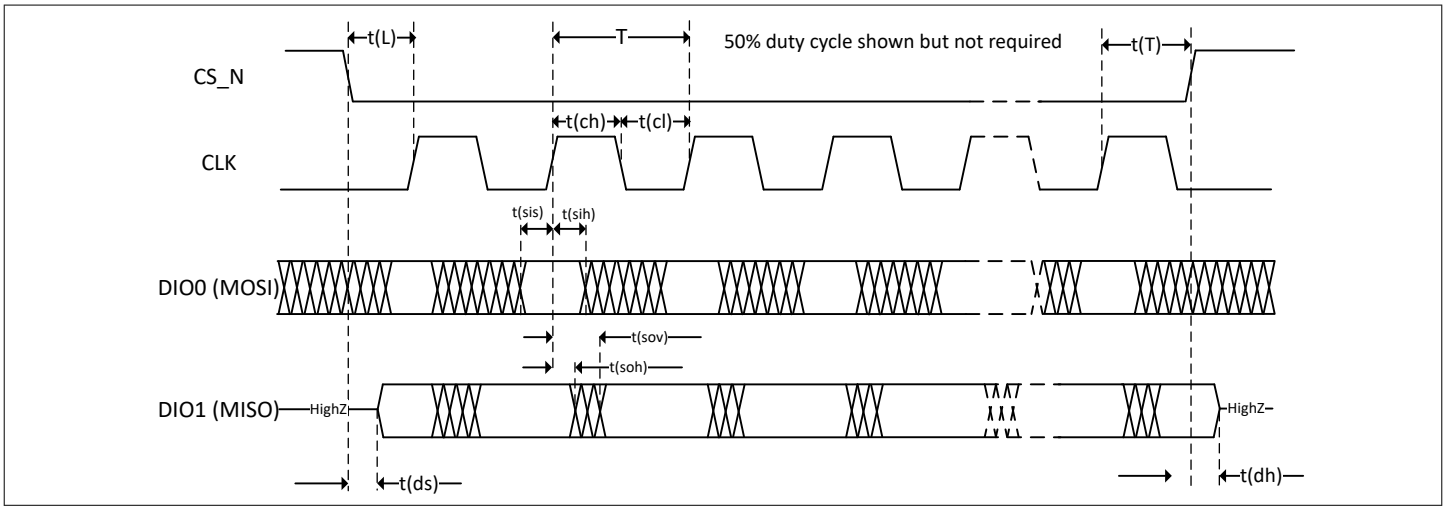


Figure 4 SPI high speed timing

3.3.3 Electrical Characteristics

Table 17 Electrical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Clock frequency	f_{SPI}	-	25	50	MHz	-
Clock period	T_{SPI}	20	40	-	ns	-
Clock duty cycle	DC_{SPI_CLK}	45	50	55	%	-
Clock high phase	t_{ch}	9.0	-	-	ns	At maximum f_{SPI}
Clock low phase	t_{cl}	9.0	-	-	ns	At maximum f_{SPI}
Slave input setup	t_{sis}	5.0	-	-	ns	-
Slave input hold	t_{sih}	5.0	-	-	ns	-
Slave output valid	t_{sov}	-	-	12.0	ns	@ 15 pF load [1)], f_{SPI} > 25 MHz output driving edge is rising edge. Pad driver strength set to strong.
Slave output hold	t_{soh}	1.0	-	-	ns	-
Lead time before the first working clock edge	t_L	9.0	-	-	ns	-
Tailing time after the last working clock edge	t_T	9.0	-	-	ns	-
Data setup time after DO goes to low impedance	t_{ds}	-	-	5.0	ns	-
Data hold time before DO goes to high impedance	t_{dh}	-	-	8.0	ns	-
Synchronization time	t_{sync}	100	-	-	ns	Synchronization time between two SPI transactions if SPI mode is changed
Chip select high phase	$t_{CS\_N\_h}$	15	-	-	ns	Back to back SPI transactions

3.3.4 SPI Operation Modes

Each SPI transaction consists of three phases. The command, the address and data phase.

The command phase starts with one bit **WR** (read:0_B, write: 1_B) to specify the kind of operation, read or write operation. Followed by a seven bit field so called **NUM** to specify the overall number of intended transactions.

Afterwards, there is a two byte wide **ADDRESS** field to define the targeted destination address.

Based on the type of operation, read or write, the device has to switch the direction of its used pins which requires a minimum of five cycles wait time.

Once the configurable wait time is over, the last phase the so-called data phase starts. In this phase the read or write **DATA** is transferred on one, two or four pins based on the selected operation mode.

Note: Only during the data phase, if the transaction type is read and the broad-cast mode is disabled then the output drivers of the respective IO pins are enabled.

By default, the device uses LSB first however, this can be re-configured to MSB first for all modes.

If required, the SPI transaction can be paused at any time of the protocol by stopping the SPI clock (CLK).

This is possible as the device is only sensitive to SPI clock edges.

The device offers three different modes of operation:

- Standard/single SPI (DIO0 + DIO1) (see Figure 5 and Figure 6)
- Dual SPI (DIO0 + DIO1) (see Figure 7)
- Quad SPI (DIO0 + DIO1 + DIO2 + DIO3) (see Figure 8)

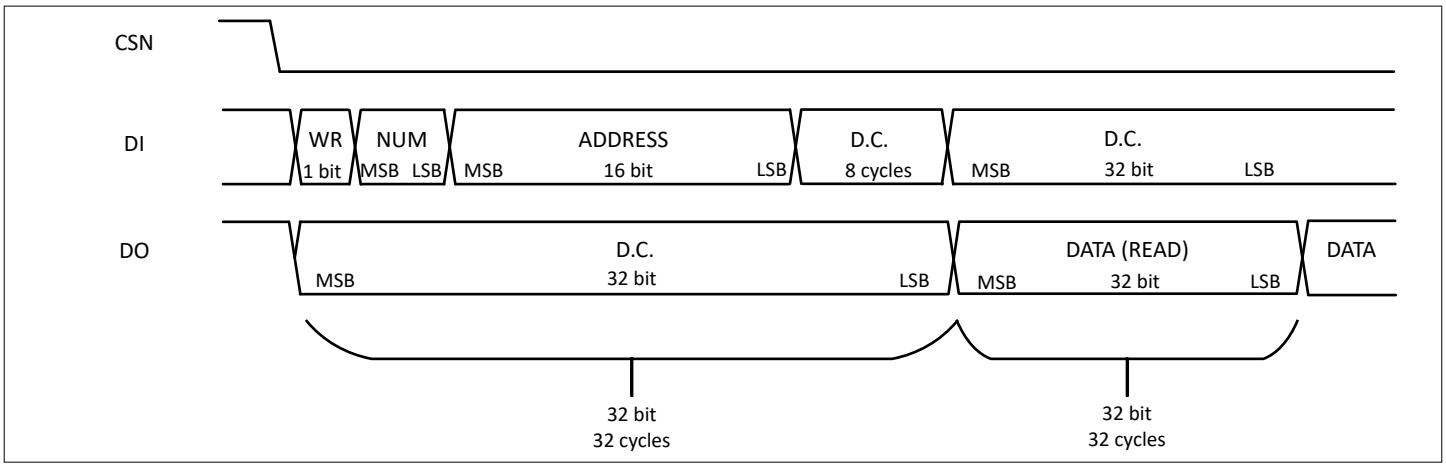


Figure 5 Standard SPI read transaction

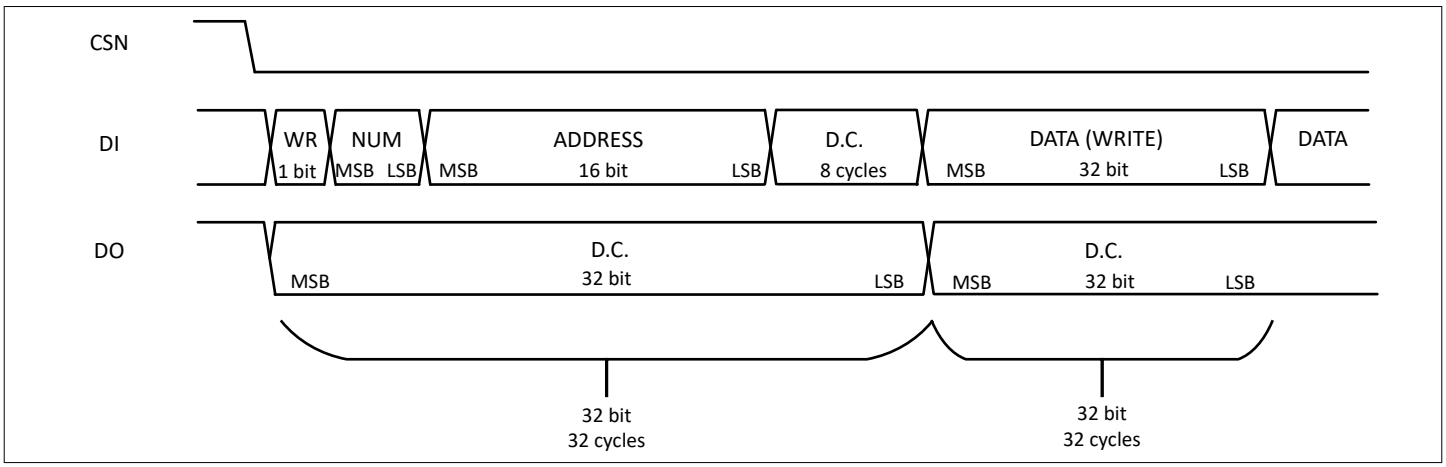


Figure 6 Standard SPI write transaction

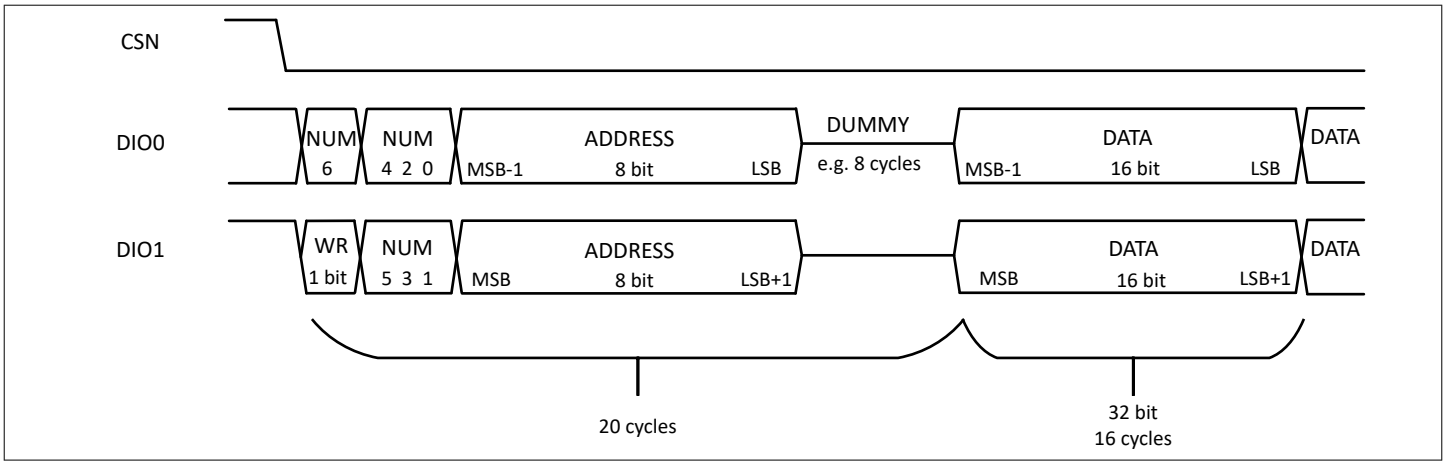


Figure 7 Dual SPI transaction

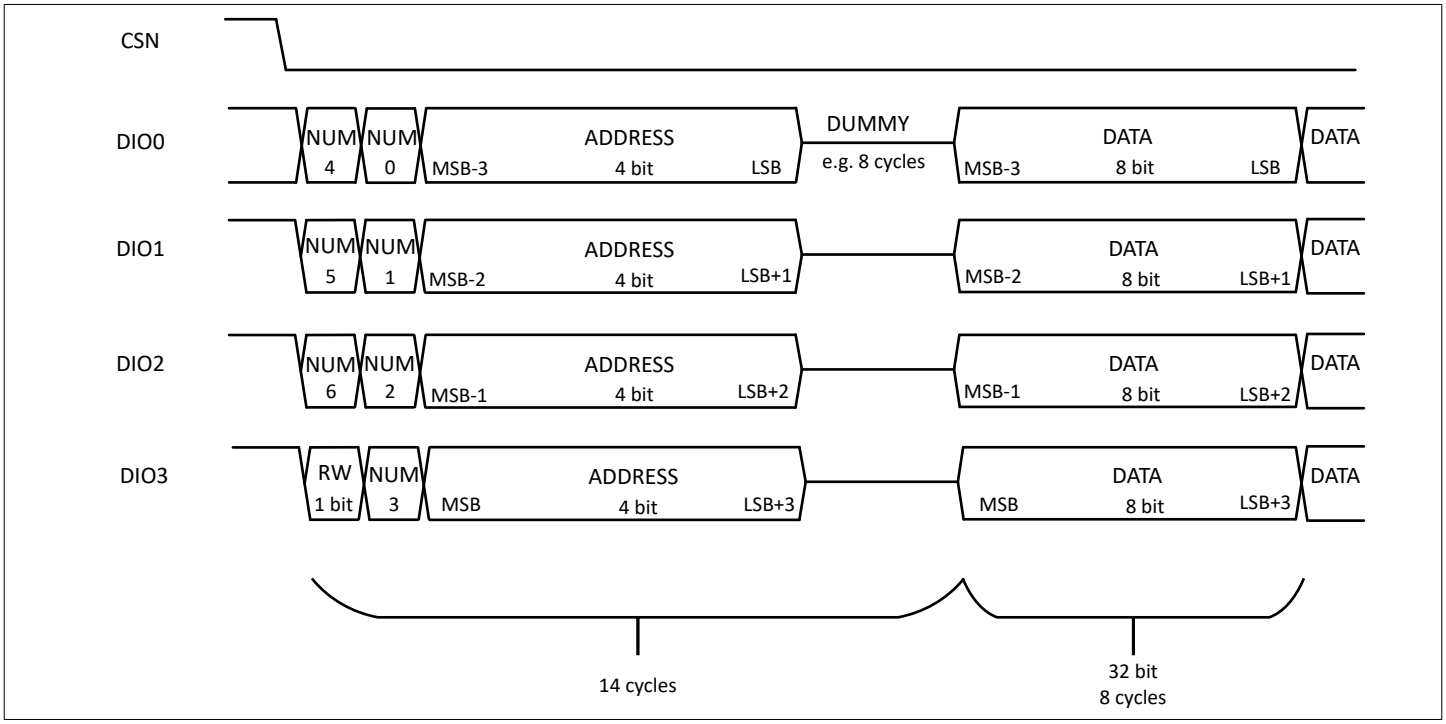


Figure 8 Quad SPI transaction

4 XOSC

4.1 Overview

The device requires a 80 MHz system clock for proper operation. This system clock can be either provided by an external oscillator via the XI pin or generated by the MMIC itself using the embedded crystal oscillator.

For this a crystal resonator and additional capacitors need to be connected to the XI and XO pins of the device, as shown in Figure 9.

To get the required 80 MHz system frequency it is possible to apply the 80 MHz directly or to use the on-chip frequency doubler circuitry by feeding it with a 40 MHz signal.

The embedded crystal oscillator supports both 40 MHz (38.4 MHz) and 80 MHz (76.8 MHz), respectively.

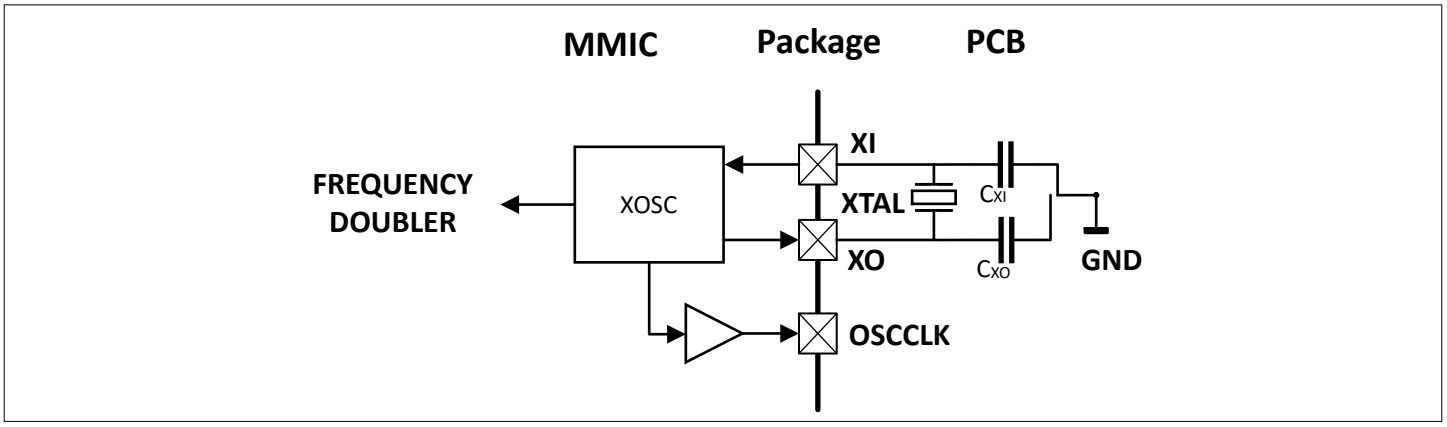


Figure 9 XOSC interface to external XTAL

4.2 XOSC Parameters

Table 18 XOSC parameters

VDD_{PLL} = 1.14 to 1.26 V, VDD_{LF} = 1.71 to 1.89 V, T_b = -20°C to +85°C, values verified by CV over DoE

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
XOSC total load capacitance	C_{XOSC}	6	8	10	pF	$C_{XOSC\_Load} \approx ((C_{XI} * C_{XO}) / (C_{XI} + C_{XO})) + C_{PCB}$
XOSC start up time	$t_{STARTUP}$	-	350	500	µs	-
XTAL						
XTAL equivalent series resistance	ESR_{XTAL}	-	30	60	Ω	Higher resistance leads to increased phase noise and increased start-up time.
XTAL frequency 40 MHz	f_{XTAL_40}	39.9	40	40.1	MHz	Internal frequency doubler must be activated.
XTAL frequency 80 MHz	f_{XTAL_80}	79.9	80	80.1	MHz	-
XTAL voltage	V_{XTAL_IO}	0	0.9	1	V	-

(table continues...)

Table 18 (continued) XOSC parameters

VDD_{PLL} = 1.14 to 1.26 V, VDD_{LF} = 1.71 to 1.89 V, T_b = -20°C to +85°C, values verified by CV over DoE

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
External clock via XI						
External input clock frequency 80 MHz	f_{EXT_OSCCLK}	75	80	85	MHz	Input clock frequency of 76.8 MHz or 80 MHz
External input clock frequency 40 MHz	$f_{EXT\_OSCCLK/2}$	37.5	40	42.5	MHz	Input clock frequency of 38.4 MHz or 40 MHz. Internal frequency doubler must be activated.
External input clock duty cycle 80 MHz	DC_{EXT_OSCCLK}	45	50	55	%	Input clock frequency of 76.8 MHz or 80 MHz
External input clock duty cycle 40 MHz	$DC_{EXT\_OSCCLK/2}$	47.5	50	52.5	%	Input clock frequency of 38.4 MHz or 40 MHz
External input clock voltage	V_{EXT_OSCCLK}	0	0.9	1.2	V	-
External input clock rise time	$t_{EXT\_OSCCLK,R}$	-	-	2	ns	20% to 80%
External input clock fall time	$t_{EXT\_OSCCLK,F}$	-	-	2	ns	20% to 80%
External input clock jitter	$J_{EXT\_OSCCLK,PH}$	-	300	400	fs	-
OSCCLK pad						
OSCCLK load capacitance	C_{OSCCLK}	-	-	5	pF	-
OSCCLK equivalent series resistance	ESR_{OSCCLK}	-	-	1	Ω	-
OSCCLK voltage	V_{OSCCLK}	0	0.9	0.99	V	-
OSCCLK clock duty cycle	DC_{OSCCLK}	40	50	60	%	System clock duty cycle
System clock						
System clock frequency	f_{SYSCLK}	75	80	85	MHz	-
System clock duty cycle	DC_{SYSCLK}	45	50	55	%	-

5 RCOSC

5.1 RCOSC Parameters

Table 19 RCOSC parameters

VDD_D = 1.14 to 1.26 V, T_b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ROSC start up time	$t_{STARTUP}$	10	26	40	µs	Verified by design
RCOSC frequency range	f_{RCOSC}	71.0	76.8 80.0	84.0	kHz	Target frequency of 76.8 kHz based on f_{SYSCLK} = 76.8 MHz Target frequency of 80 kHz based on f_{SYSCLK} = 80 MHz
RCOSC frequency error	f_{RCOSC_error}	-3	0	3	kHz	Trimming applied
RCOSC duty cycle	DC_{RCOSC}	47.5	50	52.5	%	-

6 PLL

The PLL is designed to generate high performance frequency chirps in the range of 57.0 GHz to 64.0 GHz. The modulation is performed inside the PLL bandwidth (in-band-modulation, 1MHz loop bandwidth) with an analog charge pump based fractional-N RF-PLL architecture. It furthermore features a shape generator with high flexibility to allow different ramp shapes and duration times.

6.1 PLL Parameters

Table 20 PLL parameters

VDD_{PLL} = 1.14 to 1.26 V, VDD_{LF} = 1.71 to 1.89 V, T_b = -20°C to +85°C, values verified by CV over DoE

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output frequency range	f_{RF}	57.0	-	64.0	GHz	For PLL SDM Rhee/DeMuer
Continous FM chirp bandwidth	*BW*	0	-	7	GHz	-
Chirp slope	*Slope*	-	-	700	MHz/µs	-
Frequency ramp linearity error	*Error*	-2	-	2	MHz	5 GHz bandwidth
Frequency ramp settling time	t_{PLL_settle}	-	-	6	µs	-
PLL phase noise @1MHz offset	PN_{PLL_1MHz}	-	-	-80	dBc/Hz	Single sideband for specified output frequency range
PLL phase noise @5MHz offset	PN_{PLL_5MHz}	-	-	-85	dBc/Hz	Single sideband for specified output frequency range
PLL phase noise @10MHz offset	PN_{PLL_10MHz}	-	-	-95	dBc/Hz	Single sideband for specified output frequency range

6.1.1 Settling Time

The ramp settling time is required by the PLL to damp undershoot and overshoot in case of saw-tooth shapes as illustrated in Figure 10.

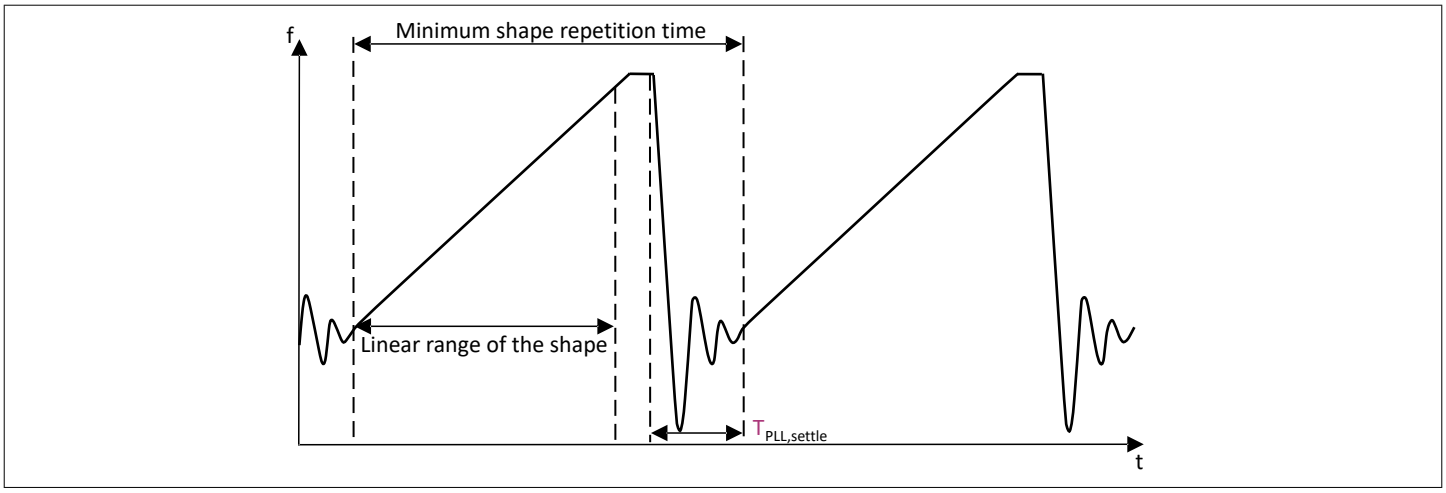


Figure 10 Chirp settling time

6.1.2 Ramp Linearity

Frequency ramp linearity error is defined to be < 1% of the frequency-modulated (FM) chirp bandwidth (2 GHz). The linearity error is calculated as the deviation from an “ideal” frequency ramp. The specification needs to be fulfilled after the frequency ramp settling time. The assumed worst case FM chirp bandwidth for linearity evaluations is 2 GHz. Figure 11 illustrates the frequency linearity definition.

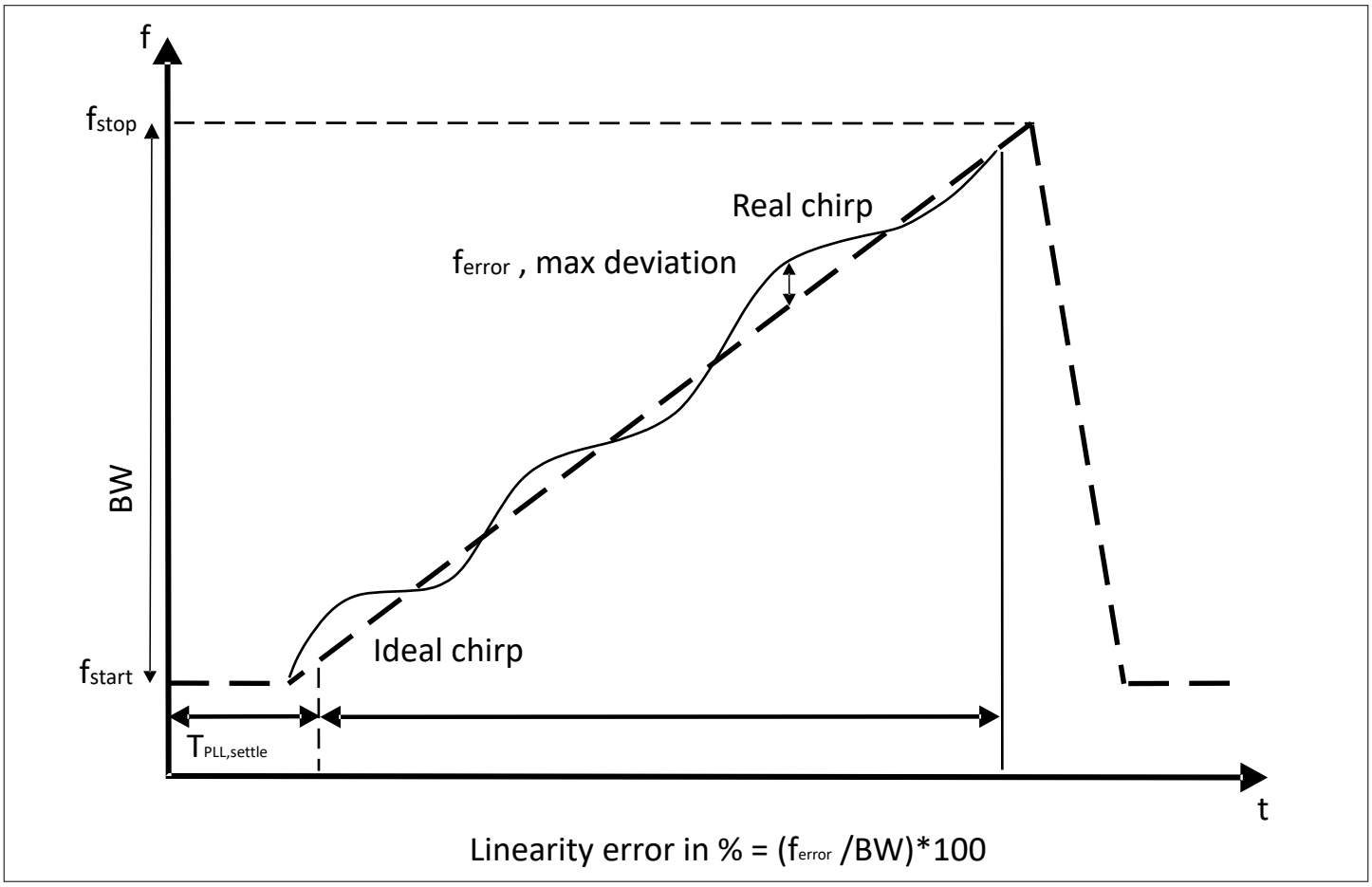


Figure 11 Frequency linearity definition

7 RF Frontend

In the RF frontend, all features to enable the radar functionality are implemented.

7.1 RF FE Parameters

Table 21 RF FE parameters

VDD_{RF} = 1.14 to 1.26 V, VDD_{BB} = 1.71 to 1.89 V, T_b = -20°C to +85°C, values verified by CV over DoE

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Frequency range	f_{RF}	57.0	-	64.0	GHz	-
Transmitter						
Transmit output power	P_{TX}	7	11	13	dBm	Conducted power at pad
Transmit output power variation over temperature	P_{TX_Temp}	0	1.0	2.0	dB	With maximum PA setting
Transmitter power control dynamic range	P_{TX_D}	-	15	-	dB	-
BPSK phase error	ERR_{BPSK}	-	-	6	°	-
Receiver						
Receiver conversion gain	CG_{RX}	9.5	14	16	dB	at 1 MHz IF offset
Conversion gain variation over temperature	CG_{RX_Temp}	-	1	-	dB	-
Noise figure single sideband RX @100 kHz	$NFSSB_{RX\_100kHz}$	11	14.5	22	dB	at RX input (die), Verified by design
Noise figure single sideband RX @500 kHz	$NFSSB_{RX\_500kHz}$	10	13	20	dB	at RX input (die), Verified by design
Noise figure single sideband RX @5 MHz	$NFSSB_{RX\_5MHz}$	8	12.5	19	dB	at RX input (die), Verified by design
Receiver 1dB compression point	$P\text{-}1dB_{RX}$	-7	-5	-1	dBm	-
Phase shifter resolution	RES_{PS}	-	4.5	-	°	

(table continues...)

Table 21 (continued) RF FE parameters

VDD_{RF} = 1.14 to 1.26 V, VDD_{BB} = 1.71 to 1.89 V, T_b = -20°C to +85°C, values verified by CV over DoE

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Phase shifter steps	N_{PHS}	0	-	42	-	-

7.2 On-chip Sensor Parameters

Relation between actual chip backside temperature (Temp) and temperature sensor readout in mV (V_T):

Temp = (V_T - b) / k

Table 22 On-chip sensor parameters

VDD_{PLL} = 1.14 to 1.26 V, VDD_{BB} = 1.71 to 1.89 V, T_b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Temperature						
Temperature sensor slope	*k*	-	-3.542967	-	mV / °C	-
Temperature sensor offset	*b*	-	212.686	-	mV	-
Temperature range	T_{Range}	-20	-	85	°C	± 9°C
Temperature range (high precision)	T_{Range_HP}	30	40	50	°C	± 5°C, Verified by design
Power detector						
Peak detector accuracy	PD_{PA_acc}	-2	-	2	dB	Over f_{RF}, Verified by design
Peak detector dynamic range	PD_{PA_dr}		15		dBm	-

8 Analog Baseband

The analog baseband block consists of a high-pass-filter (HPF), a programmable gain amplifier (PGA), an anti-aliasing-filter (AAF) and a driver for the ADC input, as illustrated in Figure 12.

The HPF is used to remove the direct current (DC) offset at the output of the RX mixer and suppresses the reflected signal from close targets (radome, e.g.).

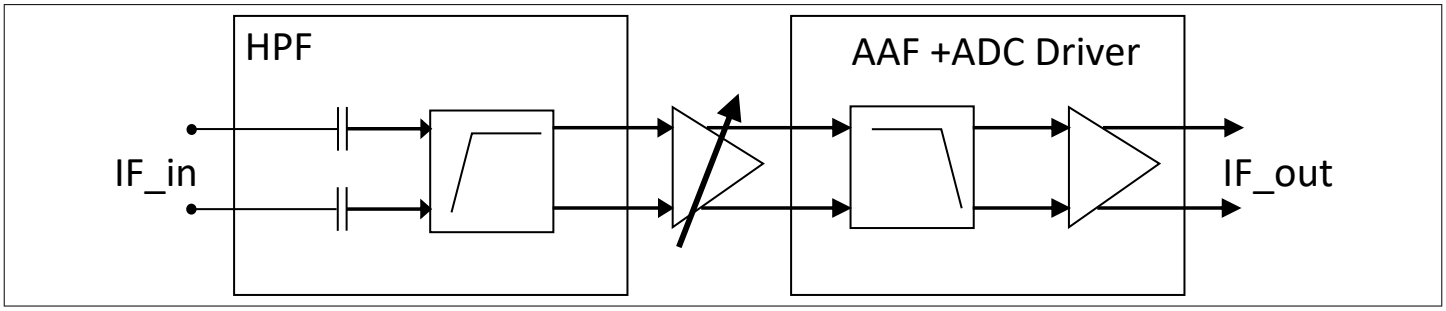


Figure 12 Baseband simplified block diagram, one for each RX channel

The IF signal is filtered by a HPF. It's a two stage HPF. First stage is selectable between 100kHz and 1MHz, second one is set around 40kHz and can be disabled.

The programable gain amplifier (PGA) provides a minimum voltage gain of 24 dB. The gain can be adjusted in steps of 3 dB each up to a maximum gain of 60 dB.

Afterwards, the PGA is followed by an AAF which cut-off frequency can be set to four different frequencies between 1 and 6 MHz. Followed by an ADC driver amplifier with a gain of 1.

Figure 13 illustrates baseband bandpass characteristic.

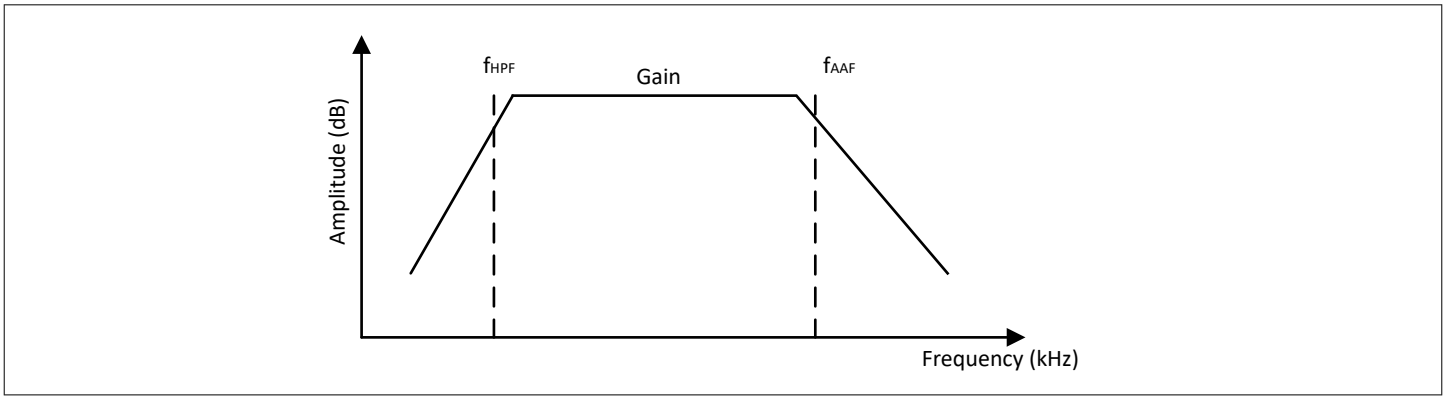


Figure 13 Baseband bandpass characteristic

8.1 Analog Baseband Current Consumption

Table 23 Analog baseband current consumption

VDD_{BB} = 1.71 V to 1.89 V, T_b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ABB current consumption off	I_{ABB_OFF}	-	-	0.5	µA	-

(table continues...)

Table 23 (continued) Analog baseband current consumption

VDD_{BB} = 1.71 V to 1.89 V, T_b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ABB current consumption on	I_{ABB_ON}	-	6	-	mA	-

8.2 Analog Baseband HPF Parameters

Table 24 Analog base band HPF parameters

VDD_{BB} = 1.71 V to 1.89 V, T_b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HPF1_0	f_{HPF1_0}	78	100	122	kHz	HPF 3 dB cutoff frequency
HPF1_1	f_{HPF1_1}	273	350	427	kHz	HPF 3 dB cutoff frequency
HPF1_2	f_{HPF1_2}	507	650	793	kHz	HPF 3 dB cutoff frequency
HPF1_3	f_{HPF1_3}	780	1000	1220	kHz	HPF 3 dB cutoff frequency
HPF2	f_{HPF2}	31	40	49	kHz	HPF 3 dB cutoff frequency 2nd HPF stage bypass disabled

8.3 Analog Baseband Gain Parameters

Table 25 Analog base band gain parameters

VDD_{BB} = 1.71 V to 1.89 V, T_b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ABB gain	G_{ABB}	24	-	60	dB	Verified by design
ABB gain step	G_{ABB_STEP}	2	3	4	dB	Verified by design

8.4 Analog Baseband AAF Parameters

Table 26 Analog base band AAF parameters

VDD_{BB} = 1.71 V to 1.89 V, T_b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
AAF_0	f_{AAF_0}	0.83	1	1.17	MHz	AAF 3 dB cutoff frequency
AAF_1	f_{AAF_1}	1.66	2	2.34	MHz	AAF 3 dB cutoff frequency

(table continues...)

Table 26 (continued) Analog base band AAF parameters

VDD_{BB} = 1.71 V to 1.89 V, T_b = -20°C to +85°C

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
AAF_2	f_{AAF_2}	4.15	5	5.85	MHz	AAF 3 dB cutoff frequency
AAF_3	f_{AAF_3}	4.98	6	7.02	MHz	AAF 3 dB cutoff frequency

9 ADC

9.1 Overview

The multichannel ADC (MADC) block consists of one SAR ADC for sensor measurement plus one per RX channel. The ADC captures the differential IF output signals from the ABB and convert it into a digital representation of the same. Figure 14 illustrates the MADC simplified block diagram.

The following table specifies the ADC parameters. All parameters are only valid with executed calibration.

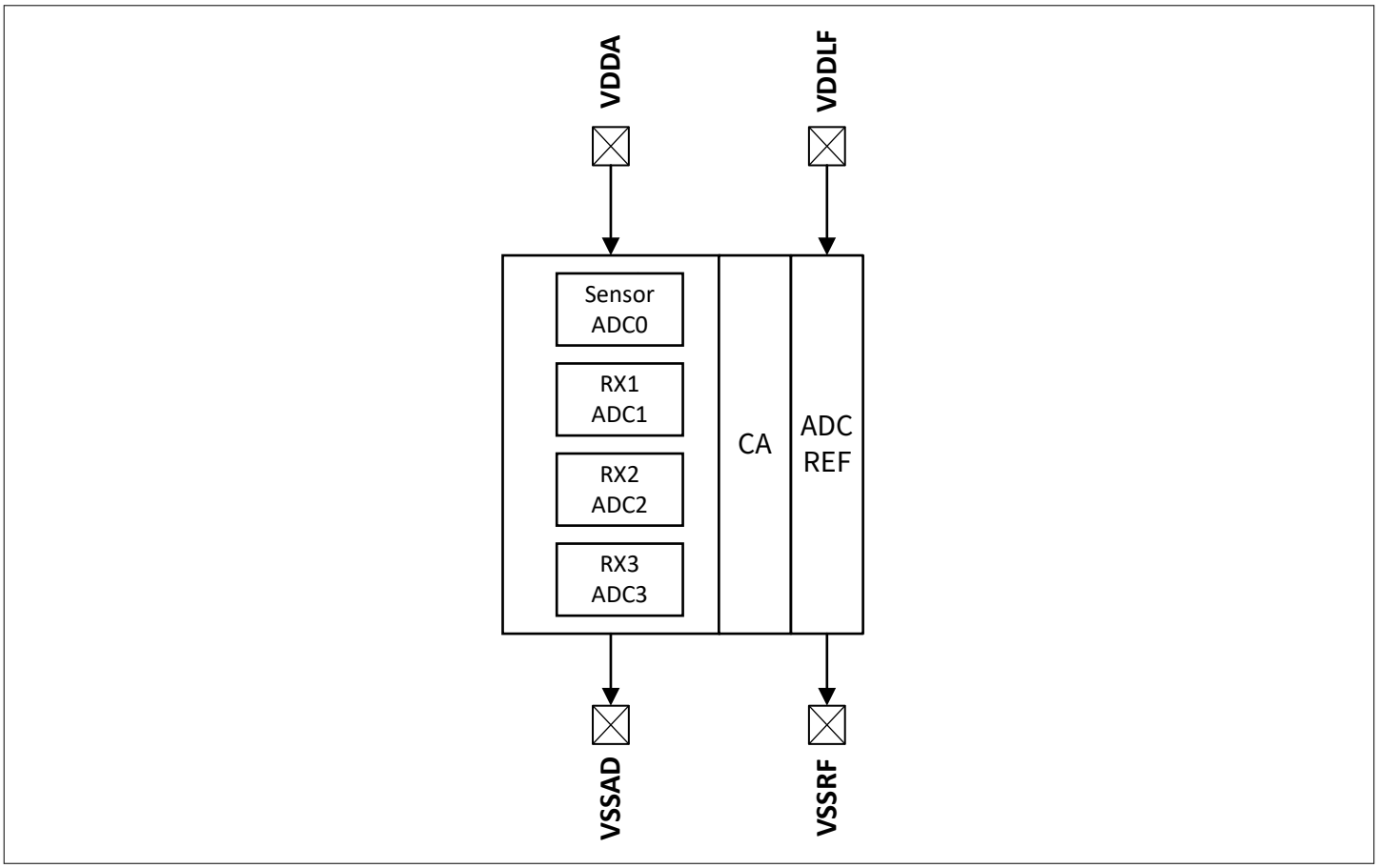


Figure 14 MADC simplified block diagram

9.2 ADC Parameters

Table 27 ADC parameters

VDD_A = VDD_{LF} = 1.71 V to 1.89 V, T_b = -20°C to +85°C, values verified by CV over DoE

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
ADC clock frequency	f_{ADC_CLK}	-	80	-	MHz	-
Resolution	*Resolution*	-	12	-	Bit	Plus 4 fractional bits
Signal to noise ratio	*SNR*	55	63.5	-	dBFS	-

(table continues...)

Table 27 (continued) ADC parameters

VDD_A = VDD_{LF} = 1.71 V to 1.89 V, T_b = -20°C to +85°C, values verified by CV over DoE

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Spurious free dynamic range	*SFDR*	58	69	-	dBFS	-
Inter modulation product	*IM3*	58	69	-	dBFS	-
Offset	*Offset*	-30	-	30	-	Absolute value of ADC output (5 LSB's) with applied offset calibration
Gain	G_{ADC}	0.94	1	1.06	-	@ -6 dBFS input
Bandwidth	*BW*	-	-	5	MHz	-
Sample rate	*SR*	-	-	20	MS/s	@ f_{SYS_CLK} = f_{ADC_CLK} = 80 MHz
Sampling time	T_S	-	12.5	-	ns	@ f_{SYS_CLK} = f_{ADC_CLK} = 80 MHz
Conversion time	T_{Conv}	-	37.5	-	ns	@ f_{SYS_CLK} = f_{ADC_CLK} = 80 MHz
Calibration time	T_{Cal}	-	100	120	us	@ f_{SYS_CLK} = f_{ADC_CLK} = 80 MHz, timing, offset and linearity calibration enabled

10 Package Information

10.1 Package

The chip is housed in a laminate package with solder balls of 300 µm diameter and integrates the antennas. According to IPC/JEDEC's J-STD0, the moisture sensitivity level (MSL) is 3.

The bottom view of the package is presented in Figure 15. The package size is 6.05 x 4.30 x 0.9 mm^3 with ball pitch of 500 µm. Package outline and marking layout are shown in Figure 16 and Figure 17, respectively.

Package name: PG-VF2BGA-38-1

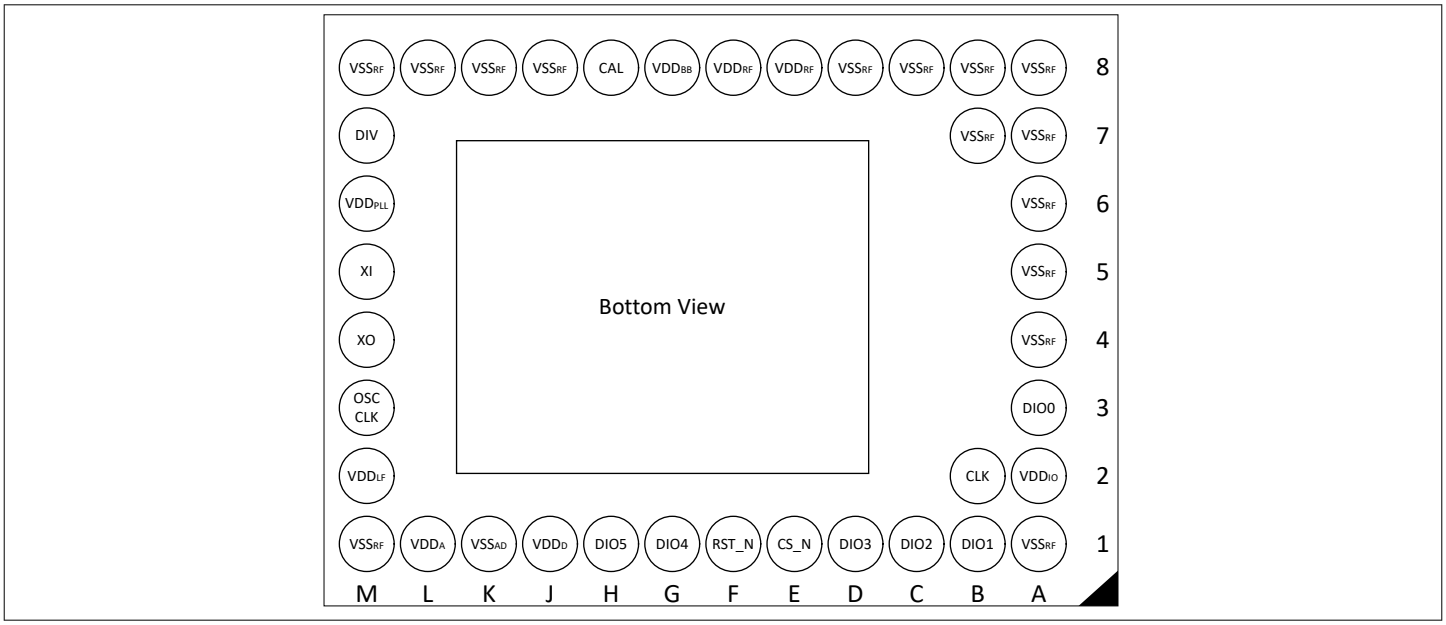


Figure 15 Device bottom view

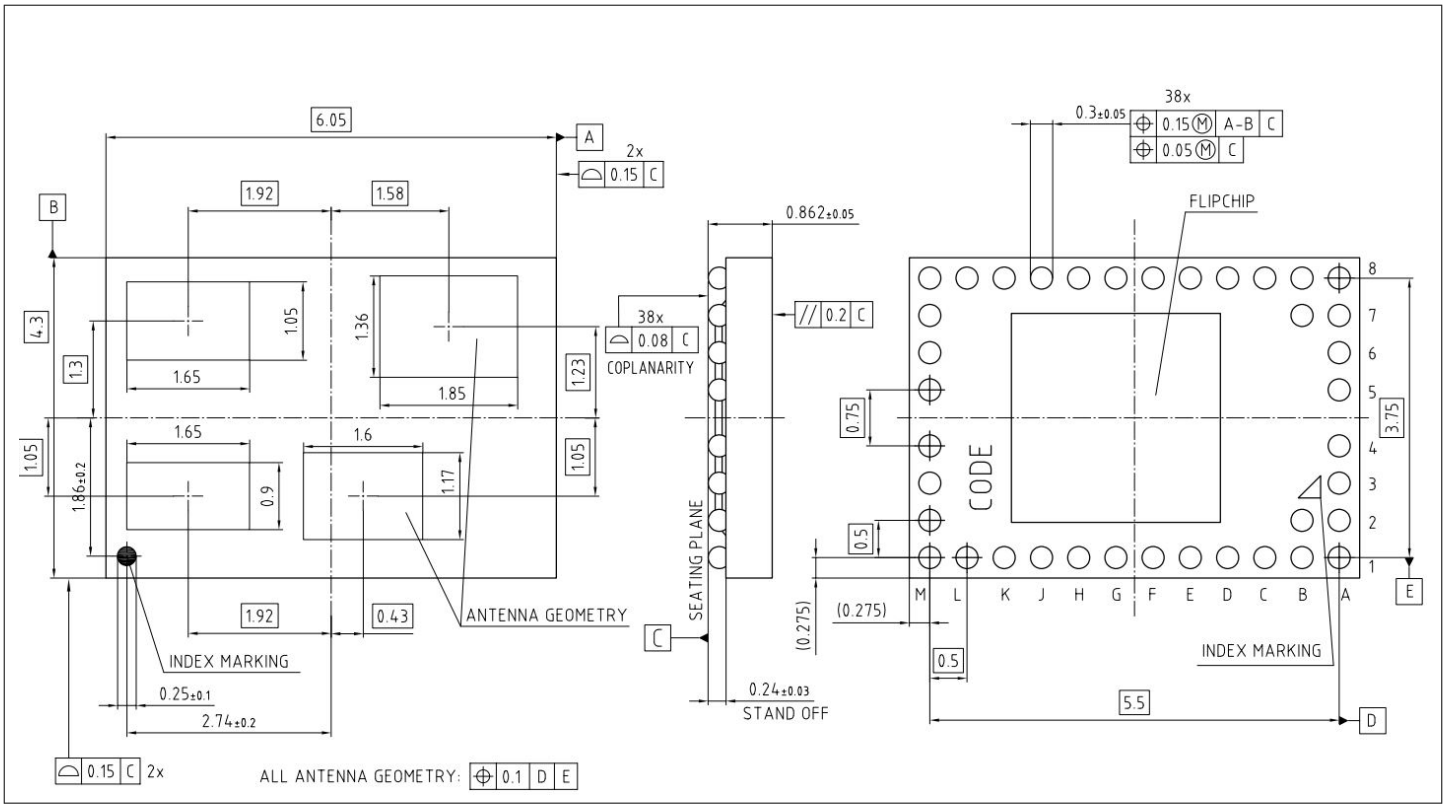


Figure 16 Package outline of PG-VF2BGA-38-1

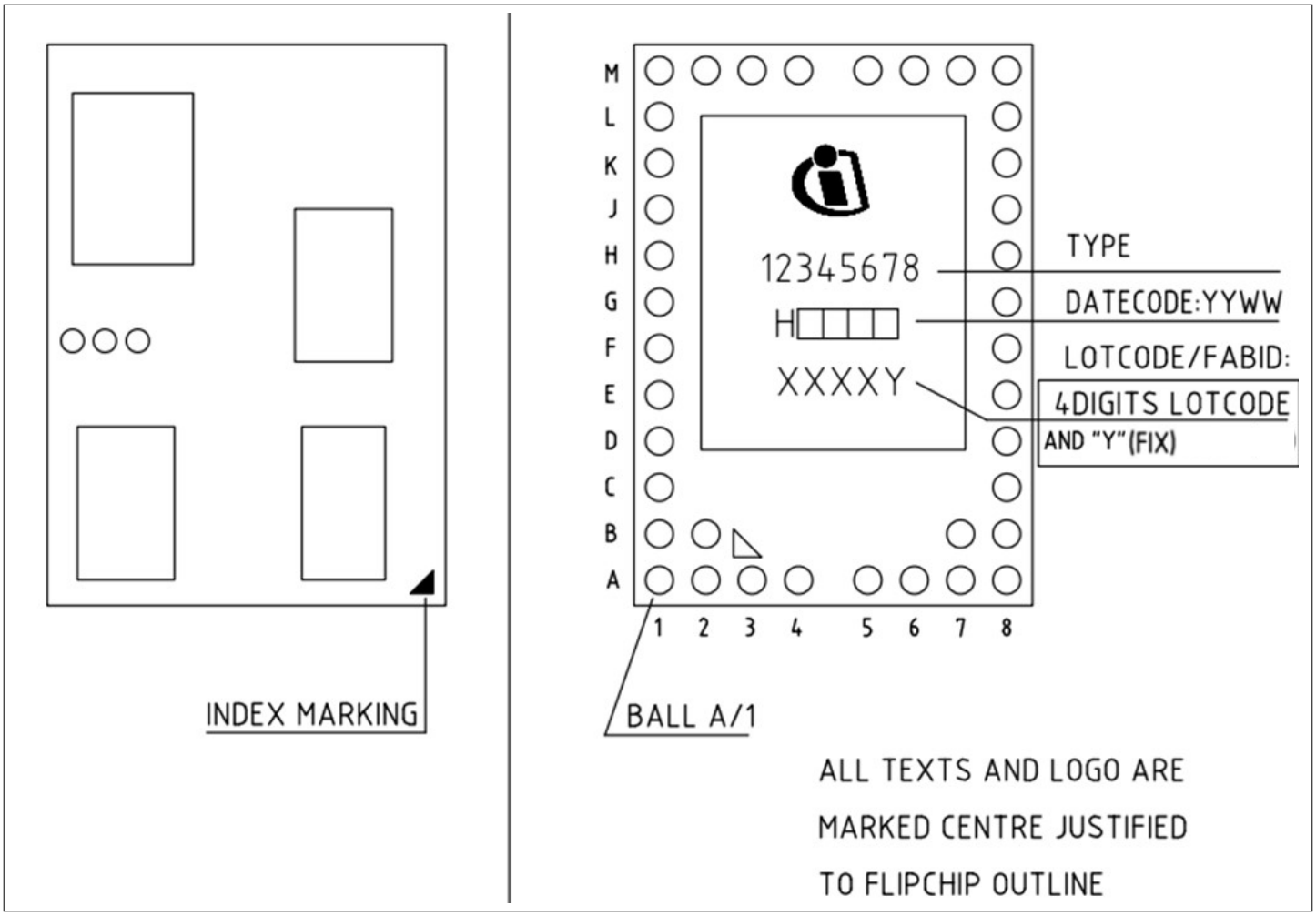


Figure 17 Marking layout of PG-VF2BGA-38-1

10.2 Built-in Antenna Specification

Antenna performance reported in the following table are ensured by design. Typical antenna behavior is measured on Infineon reference board. Typical antenna beam plots are available in a specific application note and upon specific request.

10.2.1 Built-in Antenna Parameters

Table 28 Built-in antenna parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Bandwidth						
Transmitter antenna bandwidth	TX_{BW}	57.0	-	64.0	GHz	Transmitter bandwidth, Verified by design
Receiver antenna bandwidth	RX_{BW}	57.0	-	64.0	GHz	Receiver antenna bandwidth, Verified by design

(table continues...)

Table 28 (continued) Built-in antenna parameters

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Gain						
TX antenna gain	G_{TX}	-	3.0	-	dBi	Antenna gain of a single TX antenna, Verified by design
RX antenna gain	G_{RX}	-	3.0	-	dBi	Antenna gain of a single RX antenna, Verified by design
Field of view						
Field of view E-plane	FOV_E	-	120	-	Deg	Field of view of radar mode in the E-plane, Verified by design
Field of view H-plane	FOV_H	-	90	-	Deg	Field of view of radar mode in the H-plane, Verified by design
Distance and isolation						
RX antenna distance	D_{RX_RX}	-	2.35	-	mm	Center to center distance between RX antennas in X and Y direction
TX - RX isolation	ISO_{TX_RX}	-	25	-	dB	Isolation from TX antenna to RX antenna in package Verified by design

11 Terms and Abbreviations

Abbreviation	Term	Definition
AAF	anti-aliasing filter	A filter used before a signal sampler to restrict the bandwidth of a signal to satisfy the Nyquist–Shannon sampling theorem over the band of interest.
ABB	analog base band	A signal that has a near-zero frequency range, this is, a spectral magnitude that is nonzero only for frequencies in the vicinity of the origin and negligible elsewhere.
AC	alternating current	A form of power supply in which the flow of electric charge periodically reverses direction.
ADC	analog-to-digital converter	A device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.
AP	application processor	A chip that is used to run primary user applications.
CDM	charge device model	A model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge.
CMOS	complementary metal-oxide semiconductor	A technology for constructing integrated circuits that uses a combination of p-channel and n-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) to implement logic gates.
CW	continuous wave	The emission of a sinusoidal radio wave, which may be modulated by signals.
CV	component verification	Is the process of ensuring that a device functions as intended and meets the required specifications. This involves a series of tests and evaluations to validate the component's performance, reliability, and compatibility with other components and systems.
DC	direct current	A form of power supply in which the flow of electric charge is only in one direction.
DoE	design of experiment	Is a statistical technique used to determine the relationship between factors affecting a process and the output of that process. It is a methodology for optimizing device performance, yield, and reliability.
EOL	end of line	The last stage of a production process where functional tests are executed.
ESR	equivalent series resistance	The internal alternating current resistance that appears in series with an ideal capacitance or an ideal inductance of the device.
FIFO	first in first out	A method for organizing the manipulation of a data structure where the first entry is processed first.
FM	frequency-modulated	A angle modulation in which the instantaneous frequency deviation varies in accordance with a given function, generally linear, of the instantaneous value of the modulating signal.
FMCW	frequency-modulated continuous wave	A type of radar system where a known frequency continuous wave radio energy is transmitted and then received from any reflecting object.

FSM	finite state machine	An abstract machine that can be in exactly one of a finite number of states at any given time.
HBM	human body model	A model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge based on a human body.
HPF	high-pass filter	An electronic filter that passes signals with a frequency higher than a certain cutoff frequency and attenuates signals with frequencies lower than the cutoff frequency.
HW	hardware	The collection of physical components that comprise a computer or any other electronic system.
IF	intermediate frequency	The frequency corresponding to the carrier frequency or another characteristic frequency of an input radio-frequency signal in a signal resulting from each frequency translation.
SW	low-dropout voltage regulator	A direct current linear voltage regulator that can regulate the output voltage even if the supply voltage is very close to the output voltage.
LFSR	linear feedback shift register	A shift register whose input bit is a linear function of its previous state.
LO	local oscillator	An electronic oscillator used with a mixer to change the frequency of a signal.
LSB	least significant bit	The binary digit of the least significance within a code word.
MCU	microcontroller unit	A small computer on a single integrated circuit containing a processor core, memory, and programmable input/ output peripherals.
MISO	master in slave out	The input line of a serial peripheral interface master.
MOSI	master out slave in	The output line of a serial peripheral interface master.
MSB	most significant bit	The binary digit of the most significance within a code word.
MSL	moisture sensitivity level	An electronic standard for the time period in which a moisture-sensitive device can be exposed to ambient room conditions.
PA	power amplifier	An electronic circuitry that converts a low-power signal to a high-power signal.
PGA	programmable ga in amplifier	An electronic amplifier that varies its gain depending on a programmable control voltage.
PLL	phase-locked loop	A feedback circuit for synchronizing an oscillator with the phase of an input signal.
RF	radio frequency	A frequency of a periodic radio wave or of the corresponding electric oscillation.
RSVD	reserved	A placeholder for future functionalities or features.
RX	receiver	A device that accepts signals from remote transmitters.

SAR	successive approximation register	A type of analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation using a binary search through all possible quantization levels.
SPI	serial peripheral interface	A synchronous serial communication interface specification used for inter-chip communication, primarily in embedded systems.
SW	software	The collection of non-physical components that comprise a set of instructions executed by a processor.
TX	transmitter	A device that sends out signals.
VCO	voltage controlled oscillator	An oscillator whose frequency is a function of the voltage of an input signal.

12 Revision History

Document version	Date of release	Description of changes
0.50	2025-10-09	• Added condition for idle current consumption values • Added description of the supply domains • Added conditions for IO, XOSC, PLL, RF frontend, Analog baseband and Built-in antenna parameters • Updated phase noise values

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