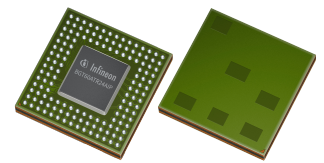


**BGT 60ATR24AIP**  
**60 GHz radar sensor with antennas in package**

**Features**

- Optimized radar frontend for short range sensing operation
- On chip power and temperature sensor
- Integrated crystal oscillator
- Single 50 MHz SPI for chip configuration and data transfer with 1.8 V and 3.3 V IO level support
- 60 GHz radar with 4.7 GHz bandwidth and a chirp slope of up to 400 MHz/μs
- 4 MSps ADC sampling rate
- 4 receiving and 2 transmitting antennas in package (AIP) with ±60° FoV



**Potential applications**

- Unattended/left-behind child detection
- Seat occupancy detection to optimize seat belt reminder
- Driver vital-sign and drowsiness monitoring (heart rate, respiration)
- Gesture sensing for car infotainment
- Intrusion and proximity alerts

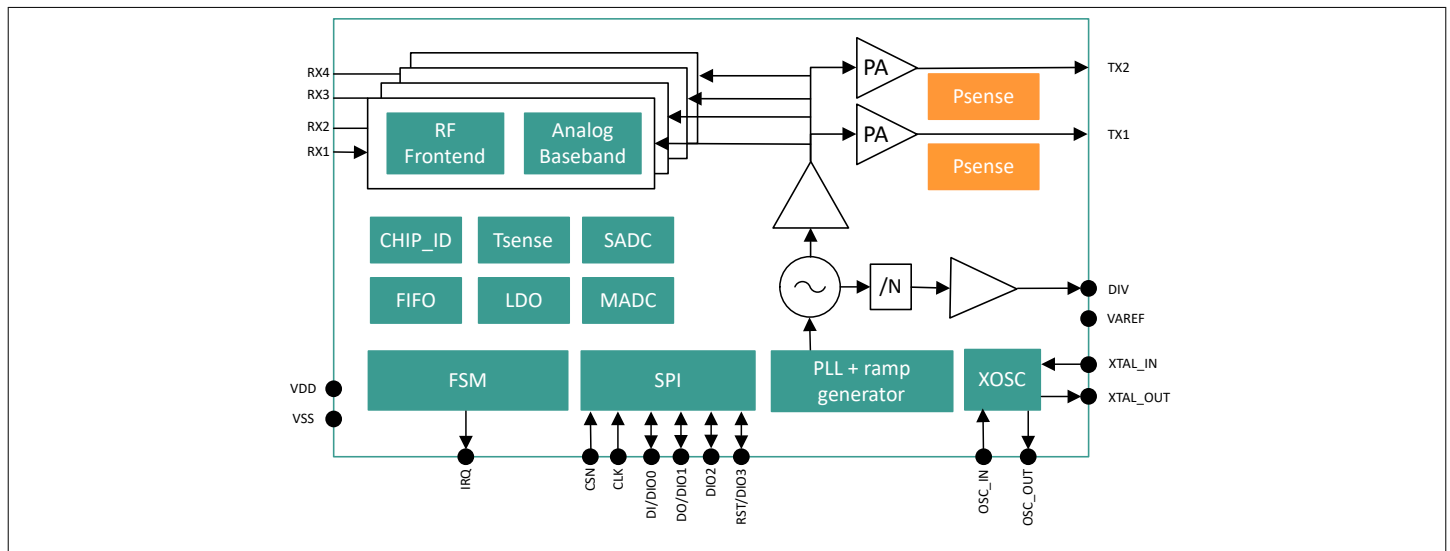
**Product validation**

Qualified for automotive applications.

Product validation according to AEC-Q100, Grade 2.

**Description**

BGT60ATR24AIP, an automotive 60 GHz radar sensor, enables ultra-wide bandwidth FMCW operation in a small package. Sensor configuration and data acquisition are enabled with a digital interface and the integrated state machine enables independent data acquisition with power mode optimization for lowest power consumption.



| Product Name   | Package         | Marking type |
|----------------|-----------------|--------------|
| BGT 60ATR24AIP | PG-VF2BGA-144-1 | 6ATR24E      |

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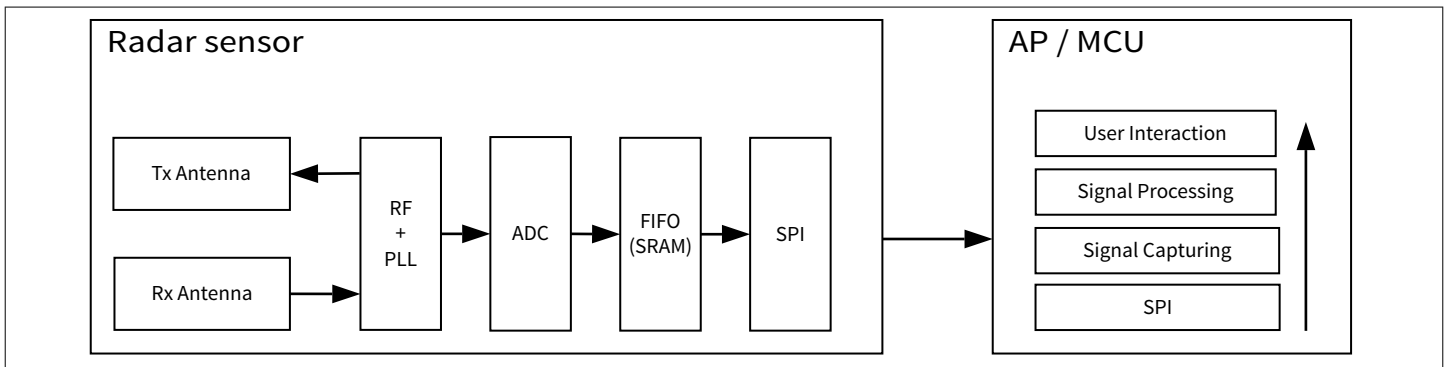
## 1 Introduction

Smart sensors can be based on radar systems, in special case, *frequency-modulated continuous wave (FMCW)* radars. Those systems can comprise several blocks: *radio frequency (RF)* front-end, *analog base band (ABB)*, *analog-to-digital converter (ADC)*, *phase-locked loop (PLL)*, memory (*first in first out (FIFO)*), *serial peripheral interface (SPI)* and antennas. Smart sensors require a high level of integration, thus, the components listed above should be integrated in a single chip solution. BGT60ATR24AIP offers this level of integration in a single chip.

### 1.1 Product overview

The core functionality of BGT60ATR24AIP is to transmit frequency modulated continuous wave signal through the *transmitter (TX)* channel and receive the echo signals from the target object on the 4 *receiver (RX)* channels. Each receiver path includes a baseband filtering, a *variable gain amplifier (VGA)*, as well as an *ADC*. The digitized output is stored in a *FIFO* based memory. The data are transferred to an external host, *microcontroller unit (MCU)* or *application processor (AP)*, to run radar signal processing. A typical implementation of a sensor system consists of two main blocks:

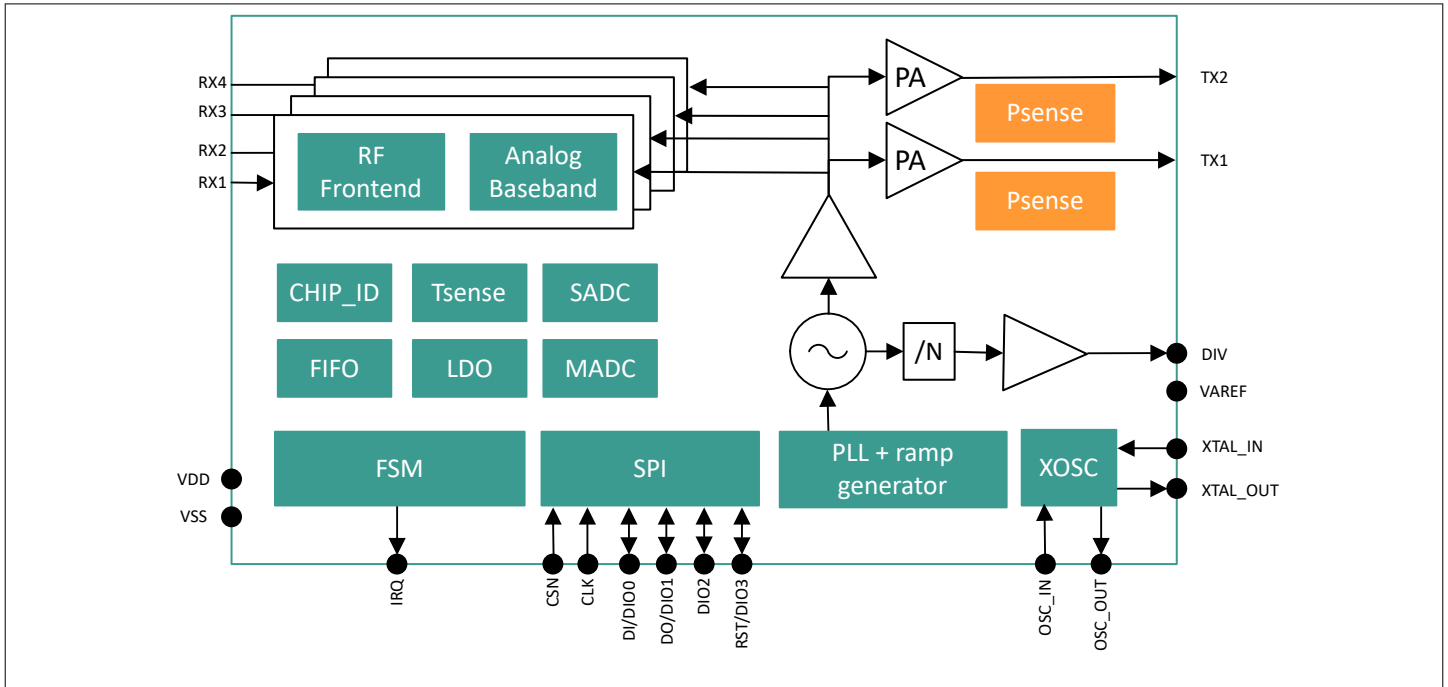
- Radar sensor (BGT60ATR24AIP) handles the *RF* signals and provides the sampled *intermediate frequency (IF)* signals
- AP or microcontroller unit which captures and processes the digital radar signals



**Figure 2** Data flow in the complete radar sensor system

## 1.2 BGT60ATR24AIP block diagram

BGT60ATR24AIP block diagram is presented in the following figure.



**Figure 3 BGT60ATR24AIP block diagram**

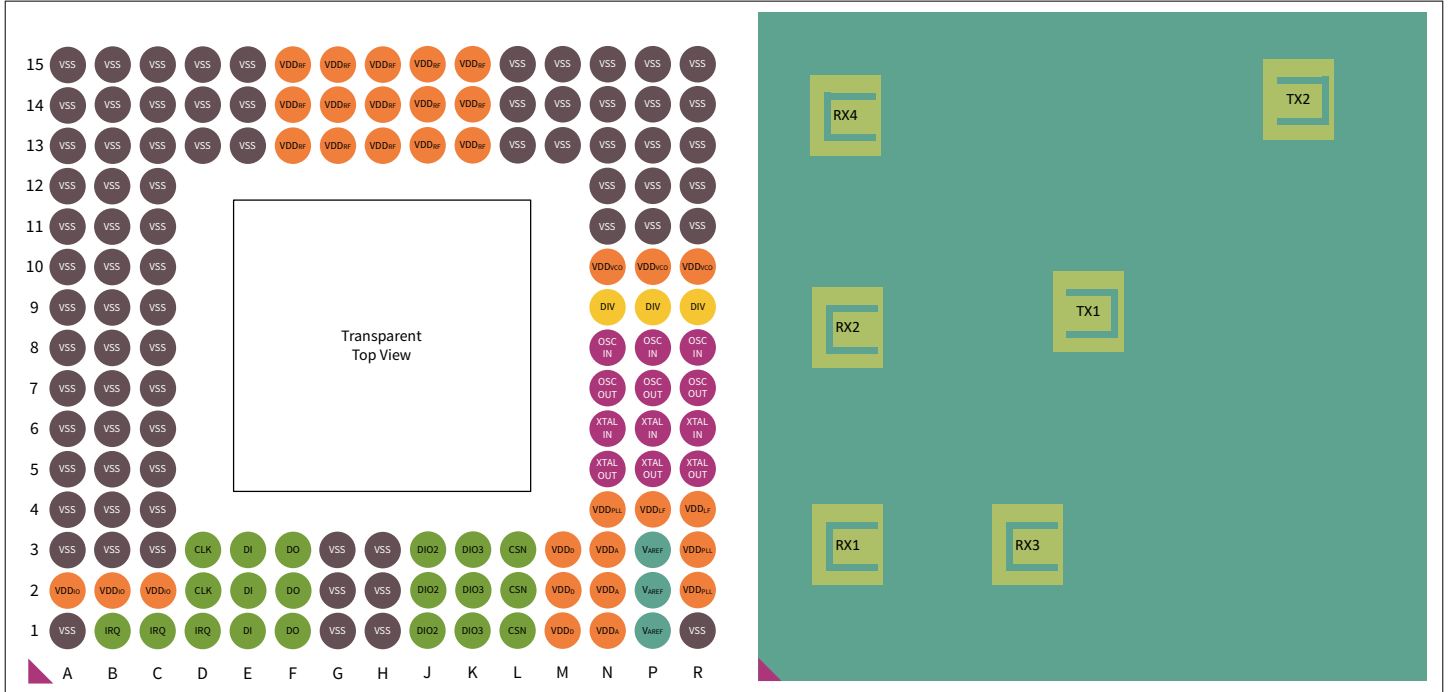
Feature list:

- Single supply voltage level of 1.8 V for both, digital and analog domains
- Integrated *low-dropout voltage regulator (LDO)* to supply the digital domain
- Separated 3.3 V supply for loop filter
- RF-Frontend at 60 GHz covering frequencies from 57.7 to 62.4 GHz with 2 TX and 4 RX channels
- Baseband chain consisting of *high-pass filter (HPF)*, low noise *VGA*, and *anti-aliasing filter (AAF)*
- 4 *ADC* channels with 12 bits resolution and up to 4 MSps sampling rate to sample the RX-IF channels
- Integrated RF *PLL*, timers, counters and a *finite state machine (FSM)* to run sets of frames in standalone mode (no communication with *AP* or microcontroller unit required except first trigger and raw data transfer)
- Full duplex *FIFO* structure as data buffer (196 kbit = 8192 words x 24 bits)
- 8 to 10 bits sensor ADC for power and temperature measurement
- Standard *SPI* mode for configuration and status register read accesses
- Integrated level-shifters for 1.8 V and 3.3 V digital IO support
- Dedicated power modes for power reduction
- An on chip or external 38.4/40/76.8/80 MHz oscillator can be used as a system clock source
- An internal frequency doubler is used in case the input clock is 38.4/40 MHz
- *built-in test equipment (BITE)* for *end of line (EOL)* test in production at Infineon to verify *RF* performance
- *linear feedback shift register (LFSR)* test pattern generator on chip for data transfer check
- Fabricated with BiCMOS Infineon process technology
- Housed in a laminate package
- Antennas integrated in the package
- 48 bits for unique CHIP ID for each device

**1 Introduction**

**1.3 BGT60ATR24AIP pin definition and function**

The following figure shows the transparent top view of the BGT60ATR24AIP laminate package with the pin and antenna number assignment.



**Figure 4 BGT60ATR24AIP pin and antenna number assignment**

The function of each pin is described in the following tables.

**Table 1 Ball definition**

| Ball  | Function |
|---|----------|
| A1, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, D13, D14, D15, E13, E14, E15, G1, G2, G3, H1, H2, H3, L13, L14, L15, M13, M14, M15, N11, N12, N13, N14, N15, P11, P12, P13, P14, P15, R1, R11, R12, R13, R14, R15 | VSS      |
| D2, D3  | CLK      |
| L1, L2, L3  | CSN      |
| E1, E2, E3  | DIO0/DI  |
| F1, F2, F3  | DIO1/DO  |
| J1, J2, J3  | DIO2     |
| K1, K2, K3  | DIO3/RST |
| B1, C1, D1  | IRQ      |
| N9, P9, R9  | DIV      |
| N8, P8, R8  | OSC_IN   |
| N7, P7, R7  | OSC_OUT  |
| N6, P6, R6  | XTAL_IN  |

**(table continues...)**

**Table 1** (continued) **Ball definition**

| Ball  | Function           |
|---|--------------------|
| N5, P5, R5  | XTAL_OUT           |
| A2, B2, C2  | VDD <sub>IO</sub>  |
| F13, F14, F15, G13, G14, G15, H13, H14, H15, J13, J14, J15, K13, K14, K15 | VDD <sub>RF</sub>  |
| N1, N2, N3  | VDD <sub>A</sub>   |
| N10, P10, R10   | VDD <sub>VCO</sub> |
| P1, P2, P3  | V <sub>AREF</sub>  |
| P4, R4  | VDD <sub>LF</sub>  |
| N4, R2, R3  | VDD <sub>PLL</sub> |
| M1, M2, M3  | VDD <sub>D</sub>   |

**Table 2** **Antenna definition**

| Antenna | Function      |
|---------|---------------|
| TX1     | Transmitter 1 |
| TX2     | Transmitter 2 |
| RX1     | Receiver 1    |
| RX2     | Receiver 2    |
| RX3     | Receiver 3    |
| RX4     | Receiver 4    |

### 1.3.1 IO and supply pins

The following table gives an overview on the input/output pins of BGT60ATR24AIP.

#### Abbreviations:

- V<sub>IN</sub>: voltage input pin
- V<sub>OUT</sub>: voltage output pin
- D<sub>IN</sub>: digital input pin
- D<sub>OUT</sub>: digital output pin
- D<sub>INOUT</sub>: digital input output pin
- A<sub>IN</sub>: analog input pin
- A<sub>OUT</sub>: analog output pin
- GND<sub>D</sub>: digital ground connection
- GND<sub>A</sub>: analog ground connection

**Table 3** **BGT60ATR24AIP input/output pins**

| Symbol | Type             | Domain            | Description              | Type   |
|--------|------------------|-------------------|--------------------------|--------|
| DIV    | A <sub>OUT</sub> | VDD <sub>RF</sub> | VCO divided by 16 output | Analog |

(table continues...)

**Table 3 (continued) BGT60ATR24AIP input/output pins**

| Symbol      | Type               | Domain            | Description   | Type    |
|-------------|--------------------|-------------------|---|---------|
| OSC_IN      | A <sub>IN</sub>    | VDD <sub>RF</sub> | Oscillator input  | Analog  |
| OSC_OUT     | A <sub>OUT</sub>   | VDD <sub>RF</sub> | Oscillator output   | Analog  |
| XTAL_IN     | A <sub>IN</sub>    | VDD <sub>RF</sub> | Crystal input   | Analog  |
| XTAL_OUT    | A <sub>OUT</sub>   | VDD <sub>RF</sub> | Crystal output  | Analog  |
| CLK         | D <sub>IN</sub>    | VDD <sub>IO</sub> | SPI clock input   | Digital |
| CSN         | D <sub>IN</sub>    | VDD <sub>IO</sub> | SPI chip select input, active low                                       | Digital |
| DI<br>DIO0  | D <sub>INOUT</sub> | VDD <sub>IO</sub> | SPI signal from the host output (MOSI)<br>SPI data 0 signal to the host | Digital |
| DO<br>DIO1  | D <sub>INOUT</sub> | VDD <sub>IO</sub> | SPI signal to the host input (MISO)<br>SPI data 1 signal to the host    | Digital |
| DIO2        | D <sub>INOUT</sub> | VDD <sub>IO</sub> | SPI data 2 signal to the host   | Digital |
| RST<br>DIO3 | D <sub>INOUT</sub> | VDD <sub>IO</sub> | Hardware reset pin<br>SPI data 3 signal to the host                     | Digital |
| IRQ         | D <sub>OUT</sub>   | VDD <sub>IO</sub> | Interrupt output  | Digital |

The power supply pins are described in the following table.

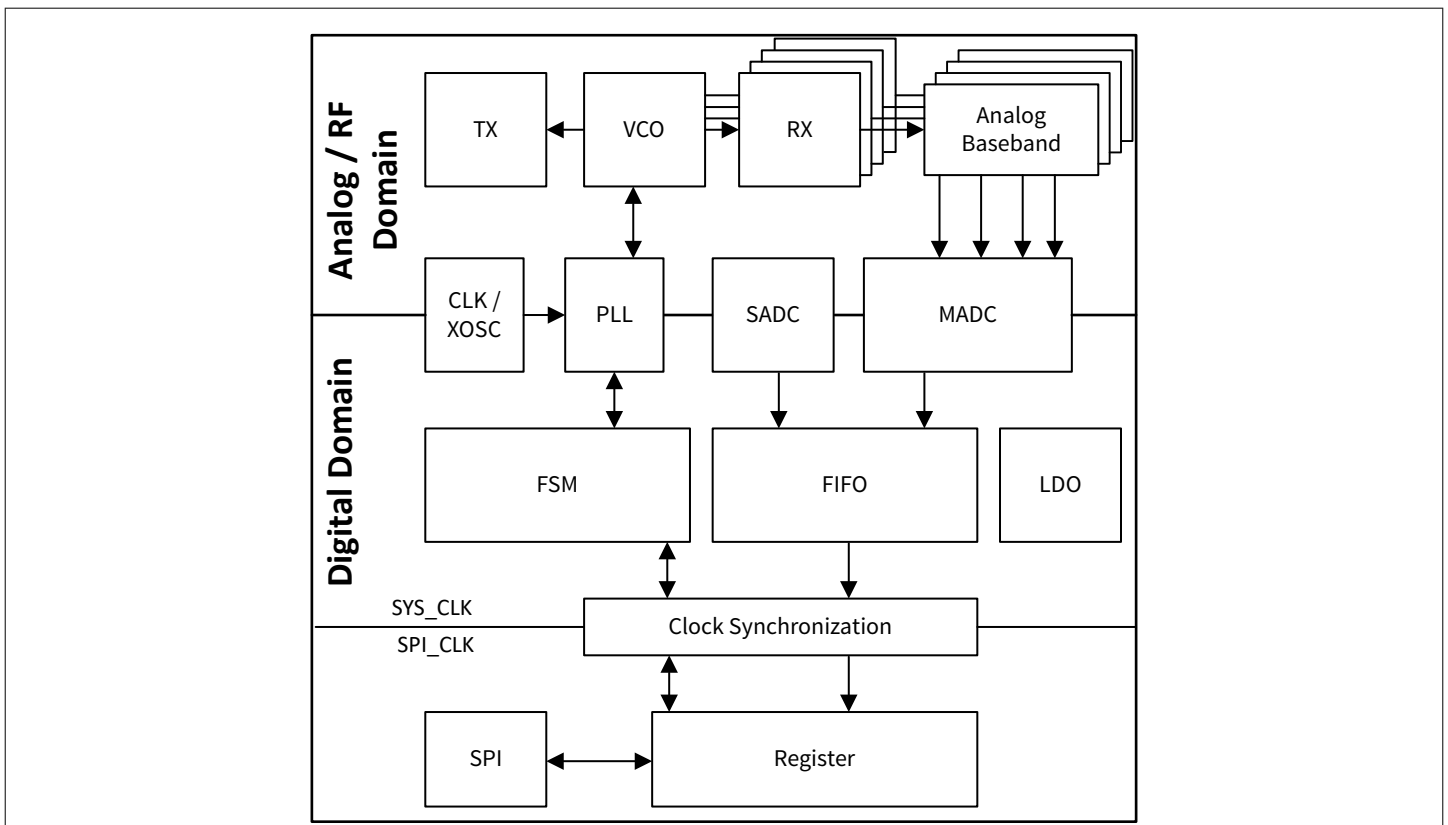
**Table 4 BGT60ATR24AIP supply pins**

| Domain             | Type             | Value          | Description                                       | Domain     |
|--------------------|------------------|----------------|---|------------|
| VDD <sub>D</sub>   | V <sub>IN</sub>  | 1.8 V          | Digital supply voltage                            | Digital    |
| VDD <sub>A</sub>   | V <sub>IN</sub>  | 1.8 V          | Analog supply voltage                             | Analog-ADC |
| VDD <sub>IO</sub>  | V <sub>IN</sub>  | 1.8 V<br>3.3 V | IO pad supply voltage                             | IO         |
| V <sub>AREF</sub>  | V <sub>OUT</sub> | 1.2 V          | Positive reference voltage output; for bypass cap | Analog-ADC |
| VDD <sub>VCO</sub> | V <sub>IN</sub>  | 1.8 V          | Analog supply voltage to the VCO                  | Analog-RF  |
| VDD <sub>RF</sub>  | V <sub>IN</sub>  | 1.8 V          | Analog supply voltage                             | Analog-RF  |
| VDD <sub>LF</sub>  | V <sub>IN</sub>  | 3.3 V          | Analog supply voltage for the PLL loop filter     | Analog-RF  |
| VDD <sub>PLL</sub> | V <sub>IN</sub>  | 1.8 V          | Analog supply voltage to the PLL                  | Analog-RF  |
| VSS <sub>RF</sub>  | GND <sub>A</sub> | 0 V            | Analog ground connection                          | Analog-RF  |
| VSS <sub>A</sub>   | GND <sub>A</sub> | 0 V            | Analog ground connection                          | Analog-ADC |
| VSS <sub>D</sub>   | GND <sub>D</sub> | 0 V            | Digital ground connection                         | Digital    |

## 1.4 BGT60ATR24AIP functional block diagram

BGT60ATR24AIP consists of some main functional blocks:

- *FSM* which manages the complete chip
- Register banks, see [Chapter 4](#)
- *FIFO*, 196 kbit = 8192 words x 24 bits
- *SPI*, up to 50 MHz clock
- Two clock domains
  - system clock domain for example 38.4/40/76.8/80 MHz for *PLL*, *ADC* and *FIFO*
  - *SPI* clock for example 50 MHz
- *PLL*, 3<sup>rd</sup> order sigma-delta based to perform *FMCW* ramp
- *RF* frontend consisting of 4 *RX* channels, 2 *TX* channels, *local oscillator (LO)* generation and divider by 4/5, see [Chapter 7.1](#)
- *ABB* consisting of *HPF*, *VGA* and *AAF*, see [Chapter 7.2](#)
- 4 channel multi ADC, 12 bits differential SAR ADC interfaced to the *ABB* via a driver and to the *FIFO* via a multiplexer, see [Chapter 8](#)
- Sensor ADC, 8 to 10 bits single-ended SAR ADC used to sense the sensor data, see [Chapter 9](#)
- Antenna built in package, see [Chapter 12](#)



**Figure 5** BGT60ATR24AIP functional overview

## 2 General product specification

The reference for all specified data is the Infineon application board, available on request.

### 2.1 Absolute maximum ratings

**Table 5 Absolute maximum ratings**

$T_b = -40\text{ °C}$  to  $105\text{ °C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified). Parameters not subject to production test.

| Parameter            | Symbol      | Value |      |      | Unit | Condition                 |
|----------------------|-------------|-------|------|------|------|---------------------------|
|                      |             | Min.  | Typ. | Max. |      |                           |
| Supply Voltage       | $VDD_D$     | -0.3  | -    | +2.0 | V    | -                         |
| Supply Voltage       | $VDD_A$     | -0.3  | -    | +2.0 | V    | -                         |
| Supply Voltage       | $VDD_{IO}$  | -0.3  | -    | +3.6 | V    | -                         |
| Supply Voltage       | $VDD_{RF}$  | -0.3  | -    | +2.0 | V    | -                         |
| Supply Voltage       | $VDD_{VCO}$ | -0.3  | -    | +2.0 | V    | -                         |
| Supply Voltage       | $VDD_{PLL}$ | -0.3  | -    | +2.0 | V    | -                         |
| Supply Voltage       | $VDD_{LF}$  | -0.3  | -    | +3.7 | V    | -                         |
| RF Input Power Level | $P_{RF}$    | -     | -    | +10  | dBm  | At the RX input pad (die) |
| Junction Temperature | $T_j$       | -40   | -    | +125 | °C   | -                         |
| Storage Temperature  | $T_{stg}$   | -40   | -    | +150 | °C   | -                         |

**Warning:** Stresses above the maximum values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and lifetime. Functionality of the device might not be given under these conditions.

### 2.2 Range of functionality

**Table 6 Range of functionality**

| Parameter      | Symbol      | Value |      |       | Unit | Condition  |
|----------------|-------------|-------|------|-------|------|--|
|                |             | Min.  | Typ. | Max.  |      |  |
| Supply Voltage | $VDD_D$     | 1.71  | 1.8  | 1.89  | V    | Noise on each supply domain should not exceed the level of $20\text{ }\mu\text{Vpp}$ in the frequency range $20\text{ kHz} - 1\text{ MHz}$ <sup>1)</sup> |
| Supply Voltage | $VDD_A$     | 1.71  | 1.8  | 1.89  | V    |  |
| Supply Voltage | $VDD_{IO}$  | 1.71  | 1.8  | 1.89  | V    |  |
|                |             | 3.135 | 3.3  | 3.465 |      |  |
| Supply Voltage | $VDD_{RF}$  | 1.71  | 1.8  | 1.89  | V    |  |
| Supply Voltage | $VDD_{VCO}$ | 1.71  | 1.8  | 1.89  | V    |  |

(table continues...)

**Table 6** (continued) Range of functionality

| Parameter                           | Symbol                         | Value |                   |      | Unit | Condition                                       |
|-------------------------------------|--------------------------------|-------|-------------------|------|------|---|
|                                     |                                | Min.  | Typ.              | Max. |      |   |
| Supply Voltage                      | $VDD_{PLL}$                    | 1.71  | 1.8               | 1.89 | V    |   |
| Supply Voltage                      | $VDD_{LF}$                     | 2.5   | 3.3 <sup>2)</sup> | 3.63 | V    |   |
| Chip Backside Temperature           | $T_b$                          | -40   | -                 | 105  | °C   | Measured with the on-chip temperature sensor    |
| Frequency Range                     | $f_{RF}$                       | 57.7  | -                 | 62.4 | GHz  | -   |
| Oscillator Input Clock Frequency    | $f_{OSC\_IN\#1}$               | 75    | 80                | 85   | MHz  | 78 MHz not allowed (frequency doubler disabled) |
|                                     | $f_{OSC\_IN\#2}$ <sup>3)</sup> | 37.5  | 40                | 42.5 | MHz  | 39 MHz not allowed (frequency doubler enabled)  |
| Duty cycle of $f_{OSC\_IN}$         | $f_{DUTOSC}$                   | 45    | 50                | 55   | %    | -   |
| Rise and Fall Time of $f_{OSC\_IN}$ | $t_{RS,FS,SYS}$                | -     | 2                 | 6    | ns   | -   |
| Phase Jitter of $f_{OSC\_IN}$       | $J_{PHOSC}$                    | -     | 1                 | -    | ps   | BW: 12 kHz to 20 MHz                            |

- 1) This value will ensure no artifact/false target in the Range-Doppler map when it is calculated with a minimum of 8 chirps.
- 2) Specified maximum bandwidth requires at least  $VDD_{LF} = 3.3$  V.
- 3) In case  $f_{OSC\_IN\#2}$  is used as input clock, an internal doubler will be used to multiply the input frequency by two. The doubler duty-cycle can be calibrated. See [PLL interfaces and clock distribution](#), [Reference clock distribution](#).

## 2.3 Current consumption

**Table 7** Overall current consumption

$VDD_X = 1.71$  V to  $1.89$  V,  $VDD_{LF} = 2.5$  V to  $3.3$  V and  $T_b = -40$  °C to  $+105$  °C.

| Parameter                           | Symbol         | Value |      |                   | Unit | Condition |
|-------------------------------------|----------------|-------|------|-------------------|------|-----------|
|                                     |                | Min.  | Typ. | Max.              |      |           |
| Idd Deep Sleep <sup>1)</sup>        | $Idd_{DS}$     | 0.05  | 0.12 | 2.4 <sup>2)</sup> | mA   |           |
| Idd Idle <sup>3)</sup>              | $Idd_{Idle}$   | 2.4   | 3.5  | 7.0               | mA   | -         |
| Idd Init0, 4RX + 2TX                | $Idd_{Init0}$  | 3.4   | 4.8  | 8.5               | mA   | -         |
| Idd Init1, 4RX + 2TX <sup>4)</sup>  | $Idd_{Init1}$  | 142   | 200  | 262               | mA   | -         |
| Idd Active, 4RX + 2TX <sup>5)</sup> | $Idd_{Active}$ | 180   | 240  | 305               | mA   | -         |

- 1) All registers in reset mode,  $f_{SYS\_CLK}$  clock path disabled.
- 2) The value at maximum refers to the maximum temperature,  $+105$  °C, and the maximum supply,  $1.89$  V.
- 3) MADC band gap running.
- 4) Idd for the rest of interchirp similar to Init1.
- 5) Device set in radar mode; DAC TX set to  $31_D$ .

**Table 8** **VDD<sub>D</sub> domain current consumption**

VDD<sub>X</sub> = 1.71 V to 1.89 V, VDD<sub>LF</sub> = 2.5 V to 3.3 V and T<sub>b</sub> = -40 °C to +105 °C.

| Parameter                           | Symbol                  | Value |      |                   | Unit | Condition |
|-------------------------------------|-------------------------|-------|------|-------------------|------|-----------|
|                                     |                         | Min.  | Typ. | Max.              |      |           |
| Idd Deep Sleep <sup>1)</sup>        | Dlidd <sub>DS</sub>     | 0.02  | 0.1  | 1.9 <sup>2)</sup> | mA   |           |
| Idd Idle <sup>3)</sup>              | Dlidd <sub>Idle</sub>   | 2.2   | 3.1  | 6.7               | mA   | -         |
| Idd Init0, 4RX + 2TX                | Dlidd <sub>Init0</sub>  | 2.2   | 3.1  | 6.7               | mA   | -         |
| Idd Init1, 4RX + 2TX <sup>4)</sup>  | Dlidd <sub>Init1</sub>  | 2.8   | 3.8  | 7.5               | mA   | -         |
| Idd Active, 4RX + 2TX <sup>5)</sup> | Dlidd <sub>Active</sub> | 3.0   | 4.2  | 7.9               | mA   | -         |

- 1) All registers in reset mode, f<sub>SYS\_CLK</sub> clock path disabled.
- 2) The value at maximum refers to the maximum temperature, +105 °C, and the maximum supply, 1.89 V.
- 3) MADC band gap running.
- 4) Idd for the rest of interchirp similar to Init1.
- 5) Device set in radar mode, FIFO in low power mode, DAC TX set to 31<sub>D</sub> for a maximum output power

**Table 9** **VDD<sub>A</sub> domain current consumption**

VDD<sub>X</sub> = 1.71 V to 1.89 V, VDD<sub>LF</sub> = 2.5 V to 3.3 V and T<sub>b</sub> = -40 °C to +105 °C.

| Parameter                           | Symbol                  | Value |        |      | Unit | Condition |
|-------------------------------------|-------------------------|-------|--------|------|------|-----------|
|                                     |                         | Min.  | Typ.   | Max. |      |           |
| Idd Deep Sleep <sup>1)</sup>        | Alidd <sub>DS</sub>     | 0     | 0.0001 | 0.01 | mA   | -         |
| Idd Idle <sup>2)</sup>              | Alidd <sub>Idle</sub>   | 0.23  | 0.36   | 0.47 | mA   | -         |
| Idd Init0, 4RX + 2TX                | Alidd <sub>Init0</sub>  | 0.23  | 0.36   | 0.47 | mA   | -         |
| Idd Init1, 4RX + 2TX <sup>3)</sup>  | Alidd <sub>Init1</sub>  | 1.65  | 2.18   | 2.65 | mA   | -         |
| Idd Active, 4RX + 2TX <sup>4)</sup> | Alidd <sub>Active</sub> | 1.75  | 2.18   | 2.65 | mA   | -         |

- 1) All registers in reset mode, f<sub>SYS\_CLK</sub> clock path disabled.
- 2) MADC band-gap running.
- 3) Idd for the rest of interchirp similar to Init1.
- 4) Device set in radar mode, DAC TX set to 31<sub>D</sub>.

**Table 10** **VDD<sub>PLL</sub> domain current consumption**

VDD<sub>X</sub> = 1.71 V to 1.89 V, VDD<sub>LF</sub> = 2.5 V to 3.3 V and T<sub>b</sub> = -40 °C to +105 °C.

| Parameter                           | Symbol                    | Value |       |      | Unit | Condition |
|-------------------------------------|---------------------------|-------|-------|------|------|-----------|
|                                     |                           | Min.  | Typ.  | Max. |      |           |
| Idd Deep Sleep <sup>1)</sup>        | PLLlidd <sub>DS</sub>     | 0     | 0.005 | 0.2  | mA   | -         |
| Idd Idle <sup>2)</sup>              | PLLlidd <sub>Idle</sub>   | 0     | 0.005 | 0.2  | mA   | -         |
| Idd Init0, 4RX + 2TX                | PLLlidd <sub>Init0</sub>  | 0.58  | 0.95  | 1.51 | mA   | -         |
| Idd Init1, 4RX + 2TX <sup>3)</sup>  | PLLlidd <sub>Init1</sub>  | 6.75  | 7.65  | 8.84 | mA   | -         |
| Idd Active, 4RX + 2TX <sup>4)</sup> | PLLlidd <sub>Active</sub> | 6.95  | 7.85  | 8.74 | mA   | -         |

- 1) All registers in reset mode, f<sub>SYS\_CLK</sub> clock path disabled.
- 2) MADC band-gap running.
- 3) Idd for the rest of interchirp similar to Init1.

**2 General product specification**

4) Device set in radar mode, DAC TX set to 31<sub>D</sub>.

**Table 11** **VDD<sub>LF</sub> domain current consumption**

VDD<sub>X</sub> = 1.71 V to 1.89 V, VDD<sub>LF</sub> = 2.5 V to 3.3 V and T<sub>b</sub> = -40 °C to +105 °C.

| Parameter                                       | Symbol                              | Value |       |      | Unit | Condition |
|---|-------------------------------------|-------|-------|------|------|-----------|
|   |                                     | Min.  | Typ.  | Max. |      |           |
| I <sub>dd</sub> Deep Sleep <sup>1)</sup>        | LF <sub>idd</sub> <sub>DS</sub>     | 0     | 0.005 | 0.2  | mA   | -         |
| I <sub>dd</sub> Idle <sup>2)</sup>              | LF <sub>idd</sub> <sub>Idle</sub>   | 0     | 0.005 | 0.2  | mA   | -         |
| I <sub>dd</sub> Init0, 4RX + 2TX                | LF <sub>idd</sub> <sub>Init0</sub>  | 0.3   | 0.39  | 0.67 | mA   | -         |
| I <sub>dd</sub> Init1, 4RX + 2TX <sup>3)</sup>  | LF <sub>idd</sub> <sub>Init1</sub>  | 0.3   | 0.39  | 0.67 | mA   | -         |
| I <sub>dd</sub> Active, 4RX + 2TX <sup>4)</sup> | LF <sub>idd</sub> <sub>Active</sub> | 0.3   | 0.39  | 0.67 | mA   | -         |

1) All registers in reset mode, f<sub>SYS\_CLK</sub> clock path disabled.

2) MADC band-gap running.

3) I<sub>dd</sub> for the rest of interchirp similar to Init1.

4) Device set in radar mode, DAC TX set to 31<sub>D</sub>.

**Table 12** **VDD<sub>RF</sub> + VDD<sub>VCO</sub> domain current consumption**

VDD<sub>X</sub> = 1.71 V to 1.89 V, VDD<sub>LF</sub> = 2.5 V to 3.3 V and T<sub>b</sub> = -40 °C to +105 °C.

| Parameter                                       | Symbol                              | Value |      |       | Unit | Condition |
|---|-------------------------------------|-------|------|-------|------|-----------|
|   |                                     | Min.  | Typ. | Max.  |      |           |
| I <sub>dd</sub> Deep Sleep <sup>1)</sup>        | RF <sub>idd</sub> <sub>DS</sub>     | 0     | 0.02 | 0.135 | mA   | -         |
| I <sub>dd</sub> Idle <sup>2)</sup>              | RF <sub>idd</sub> <sub>Idle</sub>   | 0     | 0.02 | 0.175 | mA   | -         |
| I <sub>dd</sub> Init0, 4RX + 2TX                | RF <sub>idd</sub> <sub>Init0</sub>  | 0.005 | 0.02 | 0.165 | mA   | -         |
| I <sub>dd</sub> Init1, 4RX + 2TX <sup>3)</sup>  | RF <sub>idd</sub> <sub>Init1</sub>  | 132   | 185  | 247   | mA   | -         |
| I <sub>dd</sub> Active, 4RX + 2TX <sup>4)</sup> | RF <sub>idd</sub> <sub>Active</sub> | 165   | 225  | 290   | mA   | -         |

1) All registers in reset mode, f<sub>SYS\_CLK</sub> clock path disabled.

2) MADC band-gap running.

3) I<sub>dd</sub> for the rest of interchirp similar to Init1.

4) Device set in radar mode, DAC TX set to 31<sub>D</sub>.

## 2.4 ESD integrity

**Table 13** **ESD integrity**

VDD<sub>X</sub> = 1.71 V to 1.89 V, VDD<sub>LF</sub> = 2.5 V to 3.3 V and T<sub>b</sub> = -40 °C to +105 °C.

| Parameter   | Symbol               | Value |      |       | Unit | Condition                         |
|---|----------------------|-------|------|-------|------|-----------------------------------|
|   |                      | Min.  | Typ. | Max.  |      |                                   |
| ESD robustness, <i>human body model (HBM)</i>     | V <sub>ESD-HBM</sub> | -2000 | -    | +2000 | V    | According to JS-001.<br>All pins. |
| ESD robustness, <i>charged device model (CDM)</i> | V <sub>ESD-CDM</sub> | -500  | -    | +500  | V    | According to JS-002.              |

charged device model: Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

human body model: Human Body Model ANSI/ESDA/JEDEC JS-001 ( $R = 1.5 \text{ k}\Omega$ ,  $C = 100 \text{ pF}$ ).

## 2.5 Thermal resistance

**Table 14 Thermal resistance**

$VDD_{\chi} = 1.71 \text{ V to } 1.89 \text{ V}$ ,  $VDD_{LF} = 2.5 \text{ V to } 3.3 \text{ V}$  and  $T_b = -40 \text{ }^{\circ}\text{C to } +105 \text{ }^{\circ}\text{C}$ .

| Parameter                  | Symbol   | Value |      |      | Unit | Condition                         |
|----------------------------|----------|-------|------|------|------|-----------------------------------|
|                            |          | Min.  | Typ. | Max. |      |                                   |
| Package thermal resistance | $R_{th}$ | -     | 35   | -    | K/W  | Chip backside to PCB landing pads |

### 3 Shapes, frames and channel set definition

This section is intended to provide the user with an overview on the overall modulation and power modes capabilities of BGT60ATR24AIP. Specifically, the structure of timers, counters, shapes, channel set and frames will be presented. The section also gives a description of how the *FSM* is setting and controlling the *PLL* for the expected modulation shapes and sequences programmed by the host.

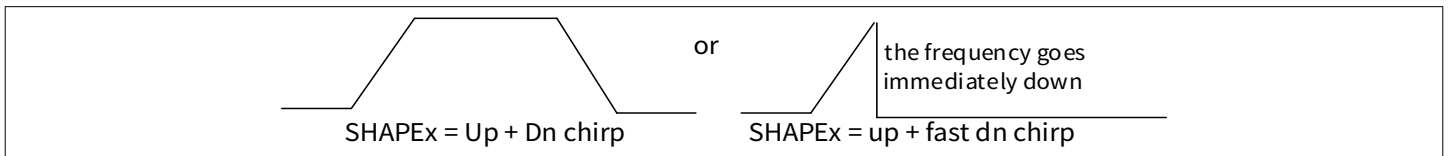
#### 3.1 Shapes and frames

The shape is the modulation chirp that should be performed by the PLL. Two basic shapes are allowed (see [Shape definition](#)):

- Triangular shape: consisting of a frequency upchirp and a frequency downchirp
- Saw-tooth shape: consisting of a frequency upchirp followed by a fast downchirp

The shapes are set and enabled in the PLLx[0..7] registers (see [PLL shape x register 0](#) and [PLL shape x register 7](#)) by the bit PLLx7:SH\_EN. Up to four different shapes can be programmed. If more than one shape is used, the lower shapes must be programmed (e.g. if 3 shapes are needed by the application, then x = 1...3).

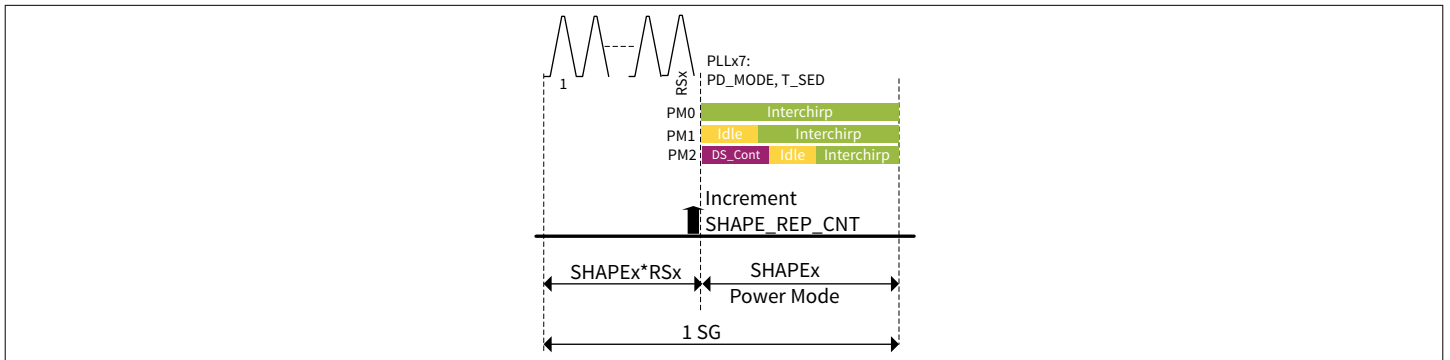
N\_SHAPE\_EN is the number of shapes enabled.



**Figure 6** Shape definition

#### Shape group

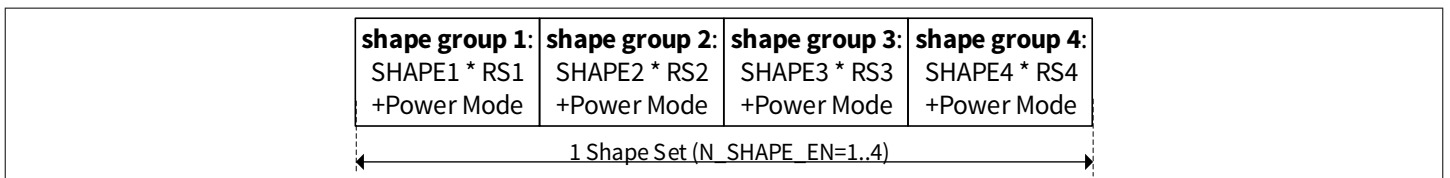
Each shape defined above can be repeated several times (see [Shape group](#)). The same shape repeated several times represents a shape group (SG). The repetition factor for the shape x is called REPSx and described in [PLL shape x register 7](#). Each shape is repeated  $RSx = 2^{REPSx}$  times.



**Figure 7** Shape group

After the last repetitions the FSM will enter, for a period PLLx7:T\_SED (see [PLL shape x register 7](#)), the power mode programmed according to what is specified in PLLx7:PD\_MODE (see [PLL shape x register 7](#)).

After a shape group, the shape groups counter STAT1: SHAPE\_GRP\_CNT is incremented (see [Status register 1](#)). In [Shape set](#) an example of four programmed shape groups is shown. It represents a shape set.



**Figure 8** Shape set

**Frame**

A frame, as shown in [Example of one frame](#), is a sequence of shape sets followed by a specific power mode. Each shape set can be repeated several times. The repetition factor for the shape set x is called REPTx and described in [Chirp control register 0](#). Each shape set is repeated  $RTx = 2^{REPTx}$  times.

The length of a frame is defined through CCR2: FRAME\_LEN (see [Chirp control register 2](#)), which is the number of shape groups to be executed.

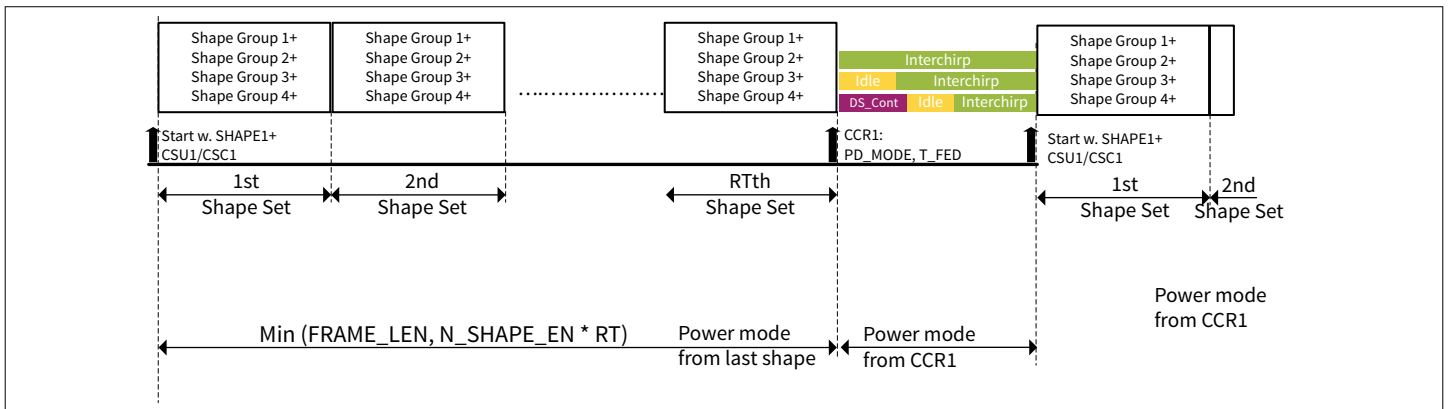
At each start of a frame, the first shape SHAPE1 together with the first channel set, CSU1+CSC1, is loaded.

The number of frame groups the FSM will execute will be:

- $\min(\text{CCR2:FRAME\_LEN}, N\_SHAPE\_EN * RT)$

With  $RT \leq (4096/\text{shape groups})$  and  $\text{CCR2:FRAME\_LEN} < 4096$ .

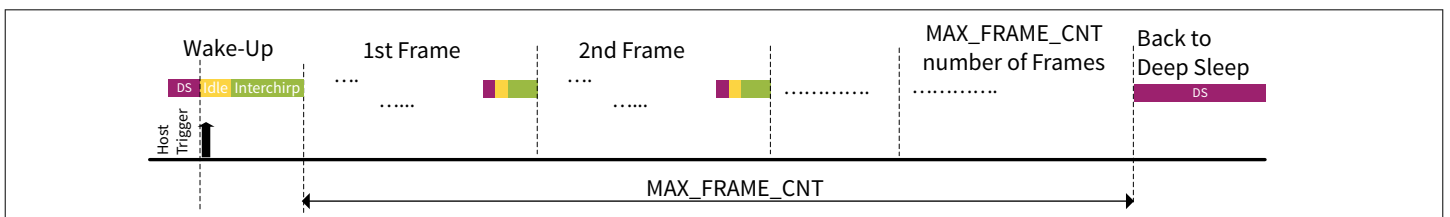
After the last shape group in a frame, the power mode from CCR1:PD\_MODE is used for the period programmed in CCR1:T\_FED instead of PPLx7:MODE for period PLLx7:T\_SED.



**Figure 9 Example of one frame**

**Maximum number of frames**

- The overall frame generation starts after the wake-up period with the first frame
- After the last frame CCR2: MAX\_FRAME\_CNT (see [Chirp control register 2](#)) is reached, the FSM will enter the deep sleep mode instead of the power mode defined at the end of the last but one frame
  - In order to trigger the chip again, a FSM reset is required



**Figure 10 Maximum number of frames**

**3.2 Channel set**

A channel set is a set of registers to control the configurations of the available transmit and receive channels. Each channel set can be repeated several times. The repetition factor for the channel set x is called REPCx and described in [Channel set control x register](#). Each channel set is repeated  $RCx = 2^{REPCx}$  times. There are in total 10 channel sets of 3 different types acting in the specific “modes”. 8 channel sets relate to the shapes (4 shapes x “up” and “down” segment settings) and two to the power modes, idle and deep sleep, respectively:

- Deep sleep power mode is related to channel set CSDS and CSCDS
- Idle mode is related to channel set CSI and CSCSI

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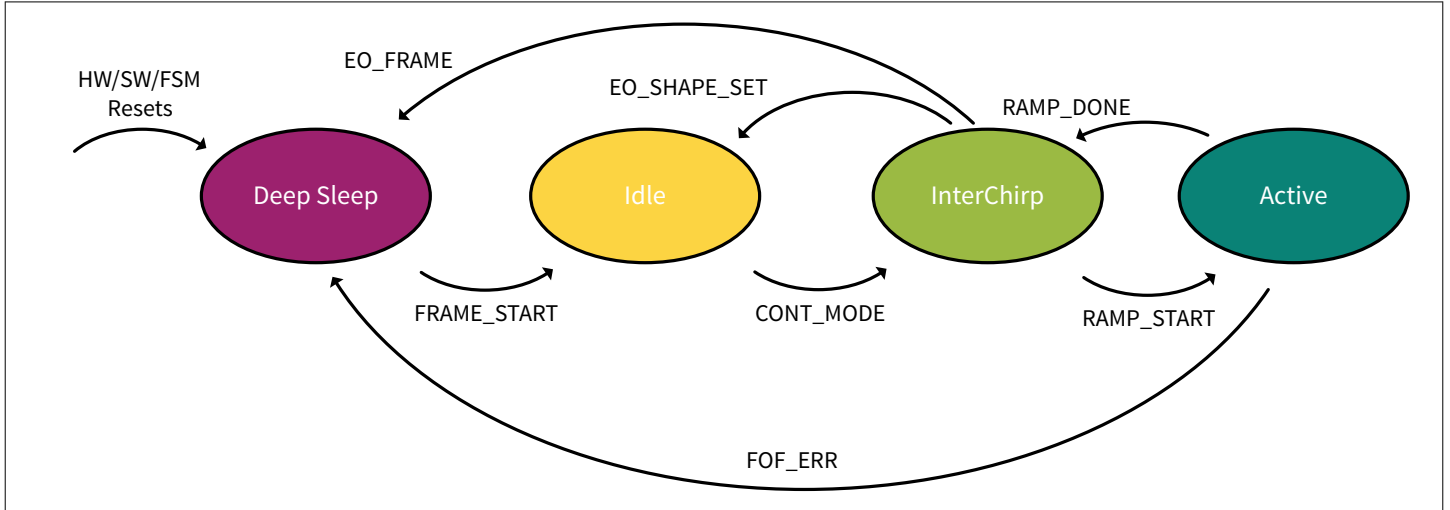
**3 Shapes, frames and channel set definition**

- 8 channel sets are defined for the shapes:
  - CSU1 ... CSU4 registers for up-chirp
  - CSD1 ... CSD4 registers for down-chirp
  - CSC1 ... CSC4 channel set configuration registers for up- and down-chirp
- Each shape from above has up to 2 channel sets CSUx and CSDx
  - In case triangular shape is used, CSUx and CSDx are applied
  - In case sawtooth shape is used, CSDx is skipped
- Channel sets are repeated independent of the shapes
- Channel set repetition factor tells how often a single channel set is repeated until the next channel set is loaded
- On the channel set sequence:
  - The lower channel set number is followed by the next higher channel set number
  - In case the highest channel set number is reached, the next channel set loaded is channel set 1
- On the enabling sequence of channel sets:
  - In case not all channel sets are used, the lower number channel sets have to be used
  - In between the enabled channel sets must not be a disabled channel set
  - E.g.: 2 channel sets expected: use only CS1 and CS2. In case 3 channel sets are expected, use only CS1, CS2, and CS3
- Start and end of channel set sequences:
  - After reset, the first channel set loaded is CS1
  - After a frame starts the first channel set loaded will be CS1

**Note:**        *It would be preferable to have REPS = REPC.*

### 3.3 Power modes

The following figure shows the flow chart on all possible power modes for the FSM.



**Figure 11** FSM flow chart

#### Power Management through the power modes

The power modes enable the host to have full flexibility on power consumption during each state of radar frame generation. A set of isolation registers (see [Channel set control x register](#)) enables/disables the different blocks of the chip. The power modes are managed by the FSM.

#### 3.3.1 Mode descriptions

In active, idle, and deep sleep mode the power mode can be defined in the CSCx register, [Channel set control x register](#), for all channel sets: CSC1..4, CSI, CSCDS (CSUx = Channel Set Upchirp, CSDx = Channel Set Downchirp, CSI = Channel Set Idle, CSDS = Channel Set Deep Sleep).

##### Active mode definition:

- During a shape: PLLx7:PD\_MODE = 0<sub>D</sub>
- Power mode defined through registers CSx (CHS1..CHS4), same mode for up-/downchirp
- Default Setting: all expected settings are enabled by the host

##### Interchirp mode definition:

- During a shape: PLLx7:PD\_MODE = 0<sub>D</sub>
- Power mode basically the same as active mode, exception: TX1 off (PAOFF)

##### Idle mode definition:

- After a shape: PLLx7:PD\_MODE = 1<sub>D</sub>
- After a frame: CCR1:PD\_MODE = 1<sub>D</sub>
- Idle mode is defined through CSCI
- Wake-up from deep sleep for TR\_WKUP

The idle mode can be used as a low-power mode in between interchirp modes or after deep sleep mode to further reduce the overall power consumption while not entering the deep sleep mode. The wake-up times after Idle mode are faster compared to the ones after deep sleep mode.

**Entering deep sleep mode:**

- After a frame: CCR1:PD\_MODE = 2<sub>D</sub> and CCR0:CONT\_MODE = 0<sub>B</sub>
- Deep sleep mode is defined through CSCDS register (see [Channel set control x register](#))
- All blocks can be turned off
- Internal system clock is also turned off - to achieve extra power saving - when CONT\_MODE = 0<sub>B</sub> otherwise (CONT\_MODE = 1<sub>B</sub>) the clock is kept up to count the internal timer T\_FED/T\_SED during the deep sleep
- In order to wake up the FSM from the deep sleep, the host has to program:
  - PACR1:OSCCLKEN = 1<sub>B</sub> to enable the clock gating
  - Then the first trigger can be applied via FRAME\_START

**Note:** *No re-configuration need to be performed as the register content is retained in deep sleep mode.*

**Entering deep sleep continuous mode:**

- After a shape: PLLx7: PD\_MODE = 2<sub>D</sub> and PLLx7:CONT\_MODE = 1<sub>B</sub>
- After a frame: CCR1:PD\_MODE = 2<sub>D</sub> and CCR0:CONT\_MODE = 1<sub>B</sub>

In case CCR0:CONT\_MODE = 1<sub>B</sub> is enabled, the wake-up from deep sleep is done automatically. The internal system clock is kept running.

**In case of errors:**

If a FIFO overflow condition occurs, the FSM will bring the radar sensor into the deep sleep power mode even if the internal counters are holding the previous value, i.e., the FSM is not reset and a reset is required. In order to reset the FIFO, the host should send at least a MAIN:FIFO\_RESET command (see [Main register](#)).

If the FIFO overflow occurs, the event is reported in FSTAT:FOF\_ERR (see [FIFO status register](#)) or in GSR0:FOF\_ERR (see [Chapter 4.49](#)).

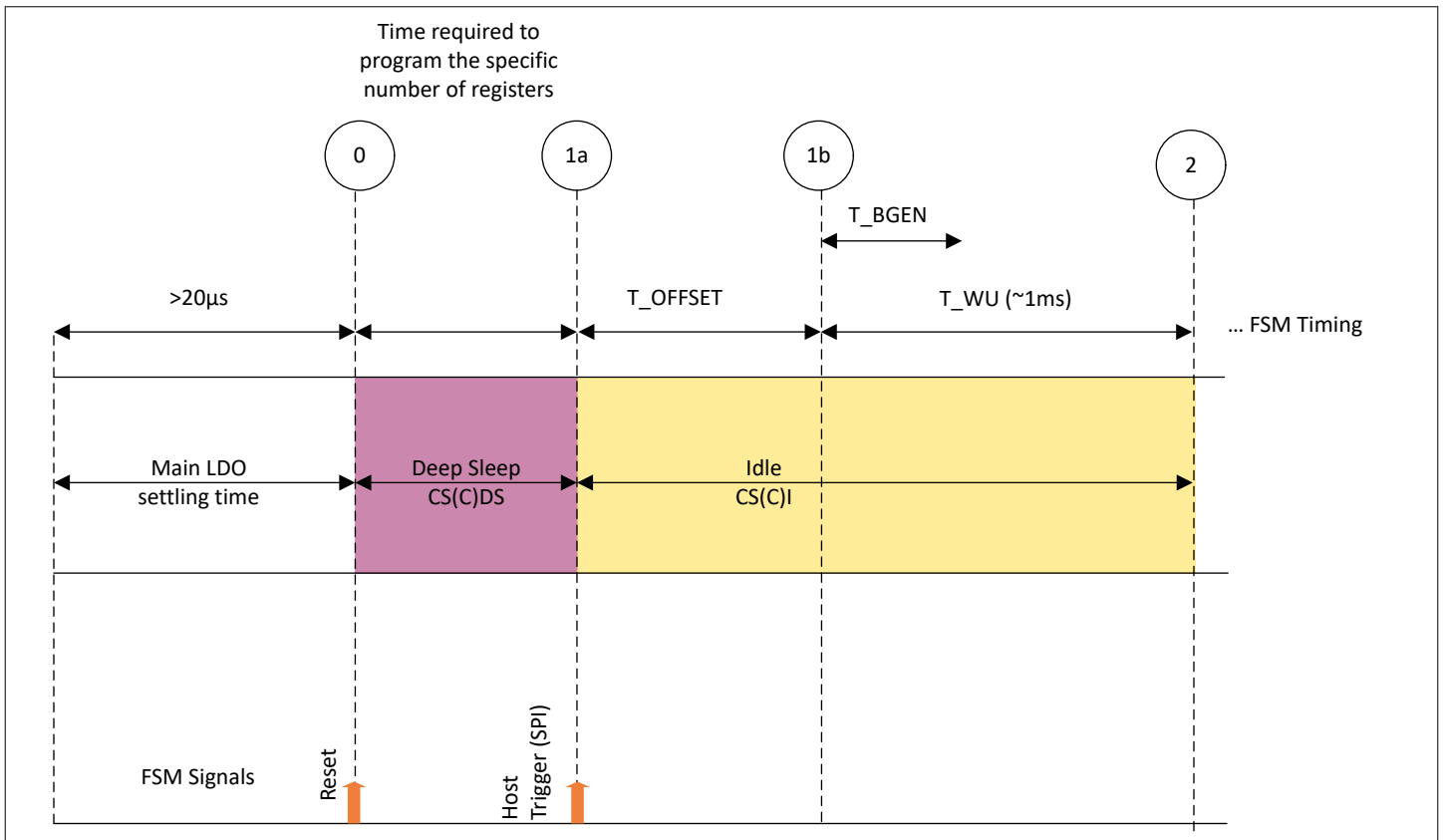
In this case, the data inside a FIFO can be read from the host as long as no reset occurs.

The flags FSTAT:FOF\_ERR and GSR0:FOF\_ERR are cleared after a reset.

**Note:** *Each time the SPI will access the chip, the system clock will be enabled internally for synchronization reasons.*

### 3.3.2 Wake-up phase from “deep sleep” to “idle”

For powering up the device, start with  $VDD_D$  first followed by all other supply domains. There is no strict timing sequence to be followed. 20  $\mu$ s after  $VDD_D$  has been applied, the main LDO will have settled to generate the internally generated core voltage  $VDD_C$ . Subsequently, the host has to perform a hardware reset according to [Hardware reset sequence](#) to set the chip to the reset state (deep sleep). The following figure describes the timing for waking up the chip.



**Figure 12** Deep sleep to idle transition

**Table 15** Transitions from deep sleep into idle

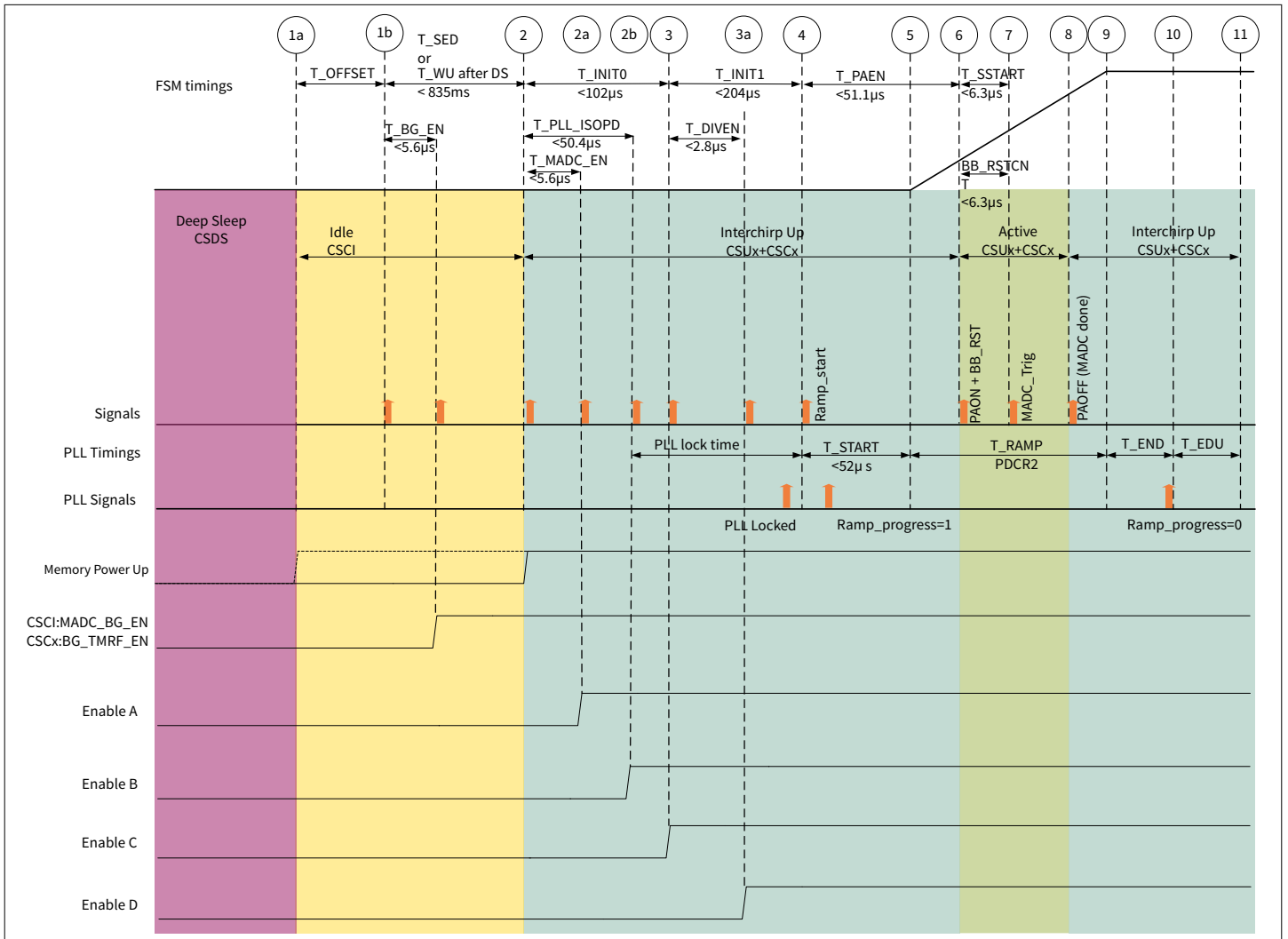
| From # | To # | Description  | Signals | Related time |
|--------|------|--|---------|--------------|
| #0     |      | Chip is reset by host (see <a href="#">Hardware reset sequence</a> )   |         |              |
| #0     | #1a  | Host programs all registers needed for expected functionality  |         |              |
| #1a    |      | Host enables the oscillator: PACR1:OSCCLKEN= 1 <sub>B</sub> to enable the clock gating   |         |              |
| #1a    |      | Host starts the first trigger; it can be applied through MAIN:FRAME_START  |         |              |
| #1a    | #1b  | Time to apply a specific offset time to a device in case multiple devices are used and triggered together (by <i>SPI</i> broadcast for example.) |         | T_OFFSET     |
| #1b    |      | Activate bandgap for MADC  |         |              |
| #1b    | #2   | Time required to settle the ADC BG (charge of external cap)  |         | T_WU         |
| #2     |      | Enable PLL, MADC, and SADC   |         |              |

(table continues...)

**Table 15** (continued) Transitions from deep sleep into idle

| From # | To # | Description                    | Signals  | Related time |
|--------|------|--------------------------------|----------|--------------|
| #2     |      | MADC sends ready signal to FSM | madc_rdy |              |

### 3.3.3 Idle to interchirp then active



**Figure 13** Transition from idle to interchirp to active to interchirp again

**Table 16** Transition from idle to interchirp to active to interchirp

| From # | To # | Description  | Signals | Related time |
|--------|------|--|---------|--------------|
| #1b    |      | Idle mode is activated   |         |              |
| #1b    |      | The user has to enable the bandgap (CSCI:BG_EN= 1 <sub>B</sub> in <a href="#">Channel set control x register</a> ) |         |              |

(table continues...)

**Table 16 (continued) Transition from idle to interchirp to active to interchirp**

| From # | To # | Description   | Signals    | Related time  |
|--------|------|---|------------|---------------|
| #1b    |      | In the case the memory is powered up after DS (SFCTL:FIFO_PD_MODE = 1 <sub>D</sub> ) the bandgap should be enabled delayed. This can be done by the user by programming CSCI:TR_BGEN  |            | T_BG_EN       |
| #1b    | #2   | If Idle mode comes after a deep sleep (see transition from deep sleep to idle). Wake up time can be used as offset for chirps   |            | T_WU          |
| #1     | #2   | If Idle mode comes after an interchirp mode, the bandgap is already running   |            | T_SED         |
| #2     |      | Interchirp Up mode is activated by selecting CSUx + CSCx register depending on the actual channel set (see <a href="#">Channel set up x register 0</a> )                              |            |               |
| #2     |      | Host already enabled the blocks required by the PLL:<br>CSx:VCO_EN = 1 <sub>B</sub><br>CSx:FDIV_EN = 1 <sub>B</sub>   |            |               |
| #2     |      | FSM sets power mode from CSUx + CSCx  |            |               |
| #2     |      | FSM sets PACR1.RFILTSEL = 0 <sub>B</sub>  |            |               |
| #2     | #2a  | In the case the memory is powered up after Idle (SFCTL:FIFO_PD_MODE = 2 <sub>D</sub> ) the MADC should be enabled delayed. This can be done by the user by programming CSCI:TR_MADCEN |            | T_MADC_EN     |
| #2a    |      | After T_MADC_EN is over, enable A gets active which gates CSxx_1:MADC_BBCHx_EN  |            |               |
| #2     | #2b  | To save power there is the option to keep the PLL in reset state and enable the PLL delayed   |            | T_PLL_ISOPD   |
| #2b    |      | After T_PLL_ISOPD is over, enable B gets active which gates CSCx:PLL_ISOPD  |            |               |
| #2     | #3   | The PLL needs some time to initialize the filter settings (see <a href="#">Chirp control register 3</a> )   |            | T_INIT0       |
| #3     |      | Enable C gets active which gates following signals: PACR1.RFILTSEL, CSxx_0:VCO_EN, CSxx_0:FDIV_EN, CSCx:ABB_ISOPD, CSCx:RF_ISOPD  |            |               |
| #3     | #3a  | To save power there is the option to close the feedback loop within the PLL delayed   |            | T_DIVEN       |
| #3a    |      | After T_DIVEN is over, enable D gets active which gates PACR2:TR_DIVEN  |            |               |
| #3     | #4   | The PLL needs again some time to settle the mode (see <a href="#">Chirp control register 0</a> )  |            | T_INIT1       |
| #4     |      | PLL sets lock bit   | PLL_lock   |               |
| #4     |      | FSM triggers ramp start of PLL  | RAMP_START |               |
| #4     | #5   | PLL needs some settling time before chirp can start. The PLL timer is running in parallel to the FSM timer. T_START will be evaluated during system testing                           |            | T_START (PLL) |

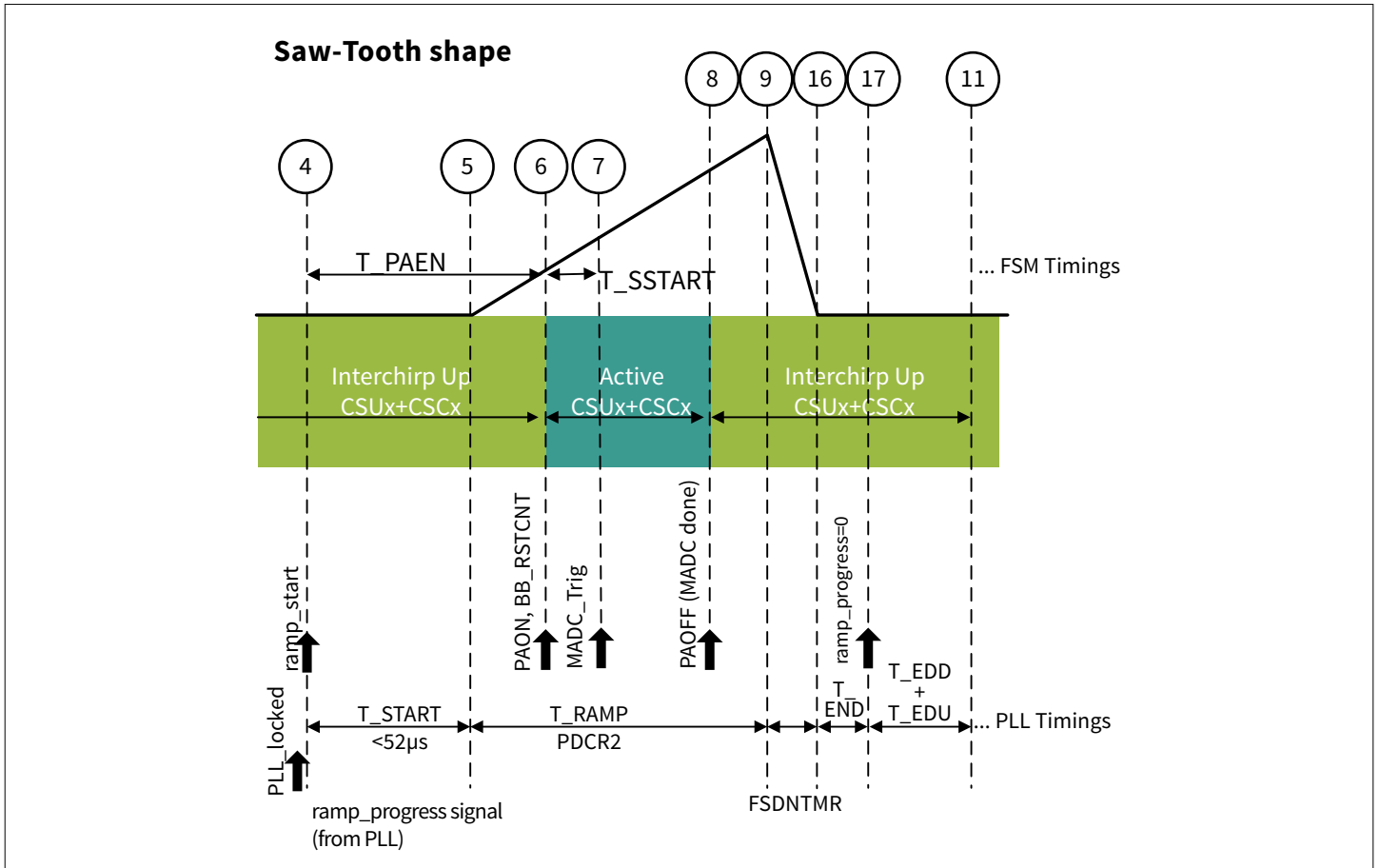
(table continues...)

**Table 16** (continued) Transition from idle to interchirp to active to interchirp

| From # | To # | Description   | Signals   | Related time |
|--------|------|---|-----------|--------------|
| #5     | #9   | PLL will run the frequency chirp  |           | T_RAMP (PLL) |
| #4     | #6   | Delay PA enable   |           | T_PAEN       |
| #6     |      | Active mode starts here   |           |              |
| #6     |      | PA is enabled (PAON).<br>Host makes sure that PA is not ON before the chirp starts (>#5)  | PAON      |              |
| #6     |      | Baseband reset timer is enabled here based on the CSx:BB_RSTCNT value   |           |              |
| #6     | #7   | During this phase, the baseband can settle  |           | T_SSTART     |
| #7     |      | MADC is triggered for the active segment (Up)   | MADC_TRIG |              |
| #7     |      | SADC is triggered once here   |           |              |
| #7     | #8   | MADC starts acquiring the given number of samples (PLLx:APU in <a href="#">PLL shape x register 3</a> ).  |           | T_ACQUx      |
| #8     |      | MADC has completed the acquisition of the expected number of samples  | MADC_DONE |              |
| #8     |      | PA is disabled (PAOFF)<br>This condition must be reached before #9<br>The condition is:<br>$T\_PAEN + T\_SSTART + T\_ACQUx > T\_START + T\_RAMPx$ | PAOFF     |              |
| #8     |      | Interchirp up mode is activated again here (CSUx + CSCx)  |           |              |
| #9     |      | PLL has completed the up-chirp  |           |              |
| #9     | #10  | Programmable delay time (e.g. 3 μs)   |           | T_END        |
| #10    |      | Ramp completed  | RAMP_DONE |              |
| #10    | #11  | Programmable delay time (e.g. 1 μs)   |           | T_EDU        |
| #11    |      | Interchirp up mode ends here  |           |              |
| #11    |      | Interchirp down mode is programmed here   |           |              |

### 3.3.4 Saw-tooth shape timing

In the saw-tooth mode, after a normal upchirp segment there will be a fast ramp down segment. The saw-tooth shape should be enabled in the bitfield PACR2:FSTDNEN (see [PLL analog control register 2](#)). For the sawtooth only CSU (Upchirp) is used (see [Channel set up x register 0](#)). The time T\_EDU (see [PLL shape x register 2](#), PLLx2#) is applied after the segment is completed. See following figure.



**Figure 14** Saw-tooth shape timing

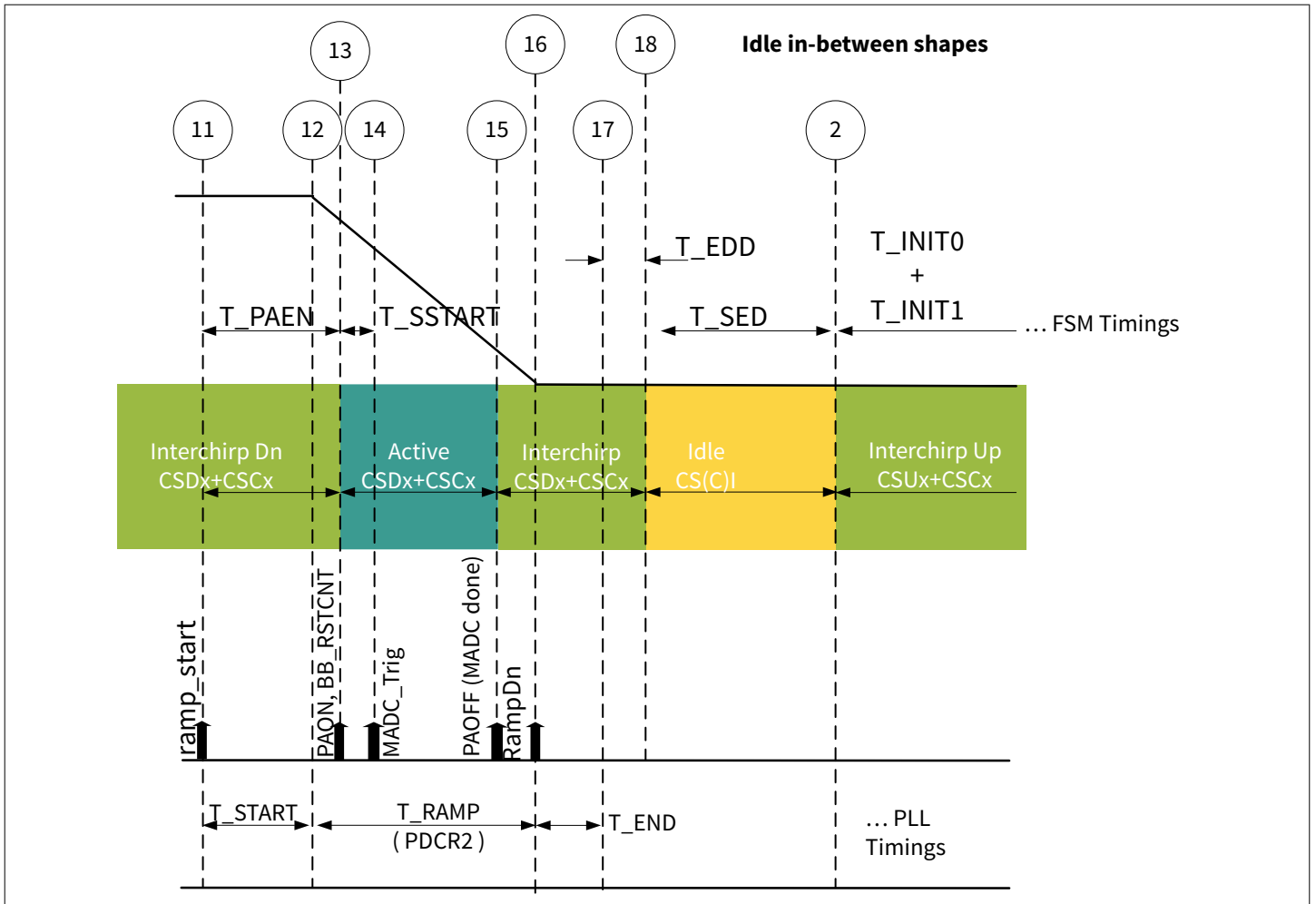
### 3.3.5 Different power modes after shapes and shape groups

After the downchirp shape, the chip can enter different power modes based on the settings (PLLx, CSx, CSCx):

- Interchirp mode in-between shapes – for fast chirp repetitions
- Idle mode after shape groups – in case of longer delay between shape groups and max power saving is required
- Deep sleep + idle mode after shape groups in case if very long delays are expected

#### 3.3.5.1 Idle after shape or shape groups

The idle mode after a shape or shape groups can be set when a long time in low power mode between shapes is required. The following figure represents a time behavior continuation of what is presented in [Figure 13](#).



**Figure 15** Idle mode after shape groups

**Table 17** End of shape and interchirp in-between shapes

| From #       | To # | Description  | Signals    | Related time |
|--------------|------|--|------------|--------------|
| #11          |      | Interchirp Dn mode is programmed here (CSDx + CSCx)                                      |            |              |
| #11          |      | FSM generates ramp_start signal  | Ramp_start |              |
| PLL related: |      |  |            |              |
| #11          | #12  | Preparation for downchirp  |            | T_START      |
| #12          | #16  | downchirp time   |            | T_RAMP       |
| #16          | #17  | Some delay after downchirp is completed  |            | T_END        |
| FSM related: |      |  |            |              |
| #11          | #13  | Some delay (see above T_PAEN)  |            | T_PAEN       |
| #13          |      | Active mode is entered with settings from previous interchirp Dn mode (CSDx+CSCx)        |            |              |
| #13          |      | PA is enabled (PAON)<br>Host makes sure that PA is not on before the chirp starts (>#12) | PAON       |              |

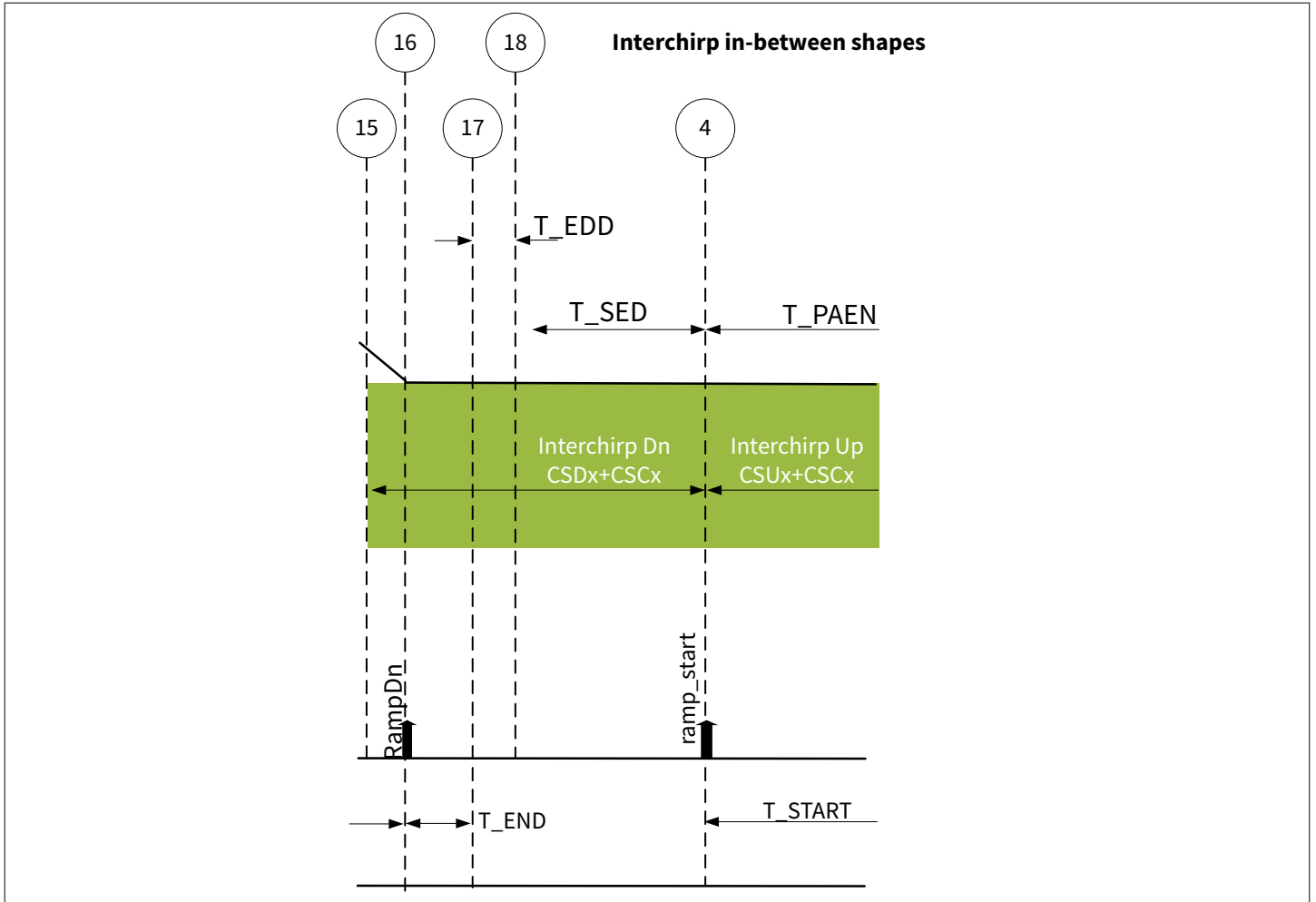
(table continues...)

**Table 17** (continued) End of shape and interchirp in-between shapes

| From # | To # | Description   | Signals   | Related time |
|--------|------|---|-----------|--------------|
| #13    |      | Baseband reset timer is enabled here based on the CSx:BB_RSTCNT value   |           |              |
| #13    | #14  | During this phase, the baseband can settle  |           | T_SSTART     |
| #14    | #15  | MADC starts acquiring the given number of samples (PLLx:APD in <a href="#">PLL shape x register 3</a> ).  | MADC_TRIG | T_ACQDx      |
| #15    |      | MADC has completed the acquisition of the expected number of samples  | MADC_DONE |              |
| #15    |      | PA is disabled (PAOFF)<br>This condition must be reached before #16<br>The condition is:<br>$T_{PAEN} + T_{SSTART} + T_{ACQDx} > T_{START} + T_{RAMPx}$ . | PAOFF     |              |
| #15    |      | Interchirp Dn mode is activated again here (CSDx + CSCx)  |           |              |
| #14    | #16  | FSM waits for PLL if ramp down to calculate #17 (TMREND)  |           |              |
| #16    |      | PLL signals the end of the downchirp (ramp progress)  | RampDN    |              |
| #17    | #18  | Time delay programmed by the host   |           | T_EDD        |
| #18    | #2   | Time programmed by the host to stay in Idle mode  |           | T_SED        |
| #2     |      | Same state #2 as in <a href="#">Figure 13</a> starts here   |           |              |

### 3.3.5.2 Interchirp in-between shapes

Interchirp between shapes can be set when the required gap between two shapes is relatively small (< 25 µs).



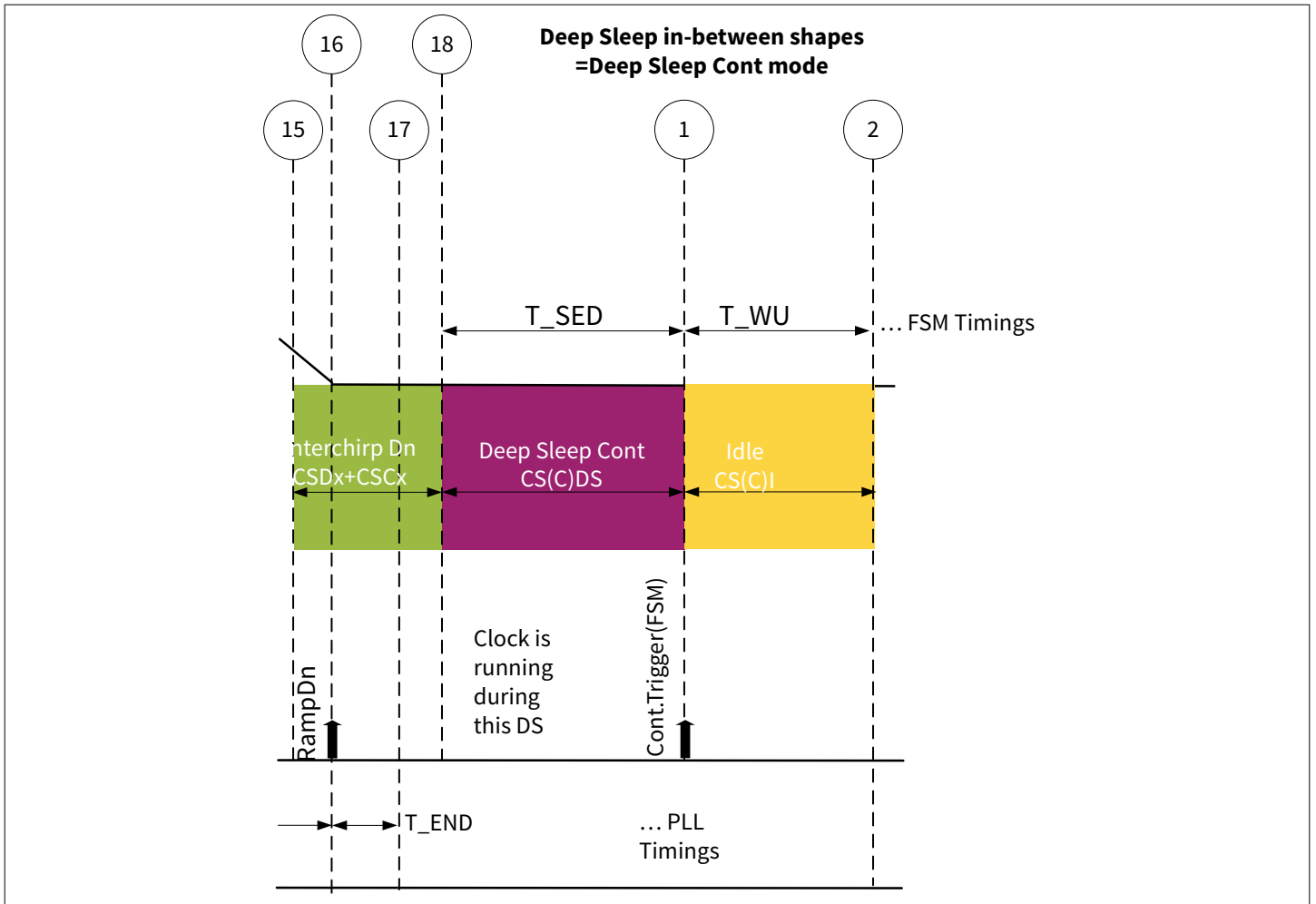
**Figure 16** Interchirp in-between shapes

**Table 18** Interchirp in-between shapes

| From # | To # | Description   | Signals | Related time |
|--------|------|---|---------|--------------|
| #15    |      | Interchirp Dn (CSDx + CSCx) is activated after active mode                                      |         |              |
| #16    |      | PLL signals the end of the downchirp (ramp progress)  | RampDN  |              |
| #16    | #17  | Some delay after downchirp is completed   |         | T_END        |
| #17    |      | PLL has completed its action  |         |              |
| #17    | #18  | Time delay programmed by the host   |         | T_EDD        |
| #18    | #4   | The chip will remain in the same interchirp power state for the provided amount of time (T_EDD) |         | T_SED        |
| #4     |      | Same state #4 as in <a href="#">Figure 13</a> starts here                                       |         |              |
| #4     |      | Interchirp up mode programmed by FSM here (CSUx + CSCx)   |         |              |

### 3.3.5.3 Deep sleep continuous + idle wake-up after shape groups

In deep sleep cont(inuous) mode after the shape group is completed, the FSM wakes up automatically after the programmed time T\_SED. The internal clock is kept running during this time. Deep sleep cont is the only deep sleep power mode possible between shape groups.



**Figure 17** Deep sleep + idle wake-up after shape groups

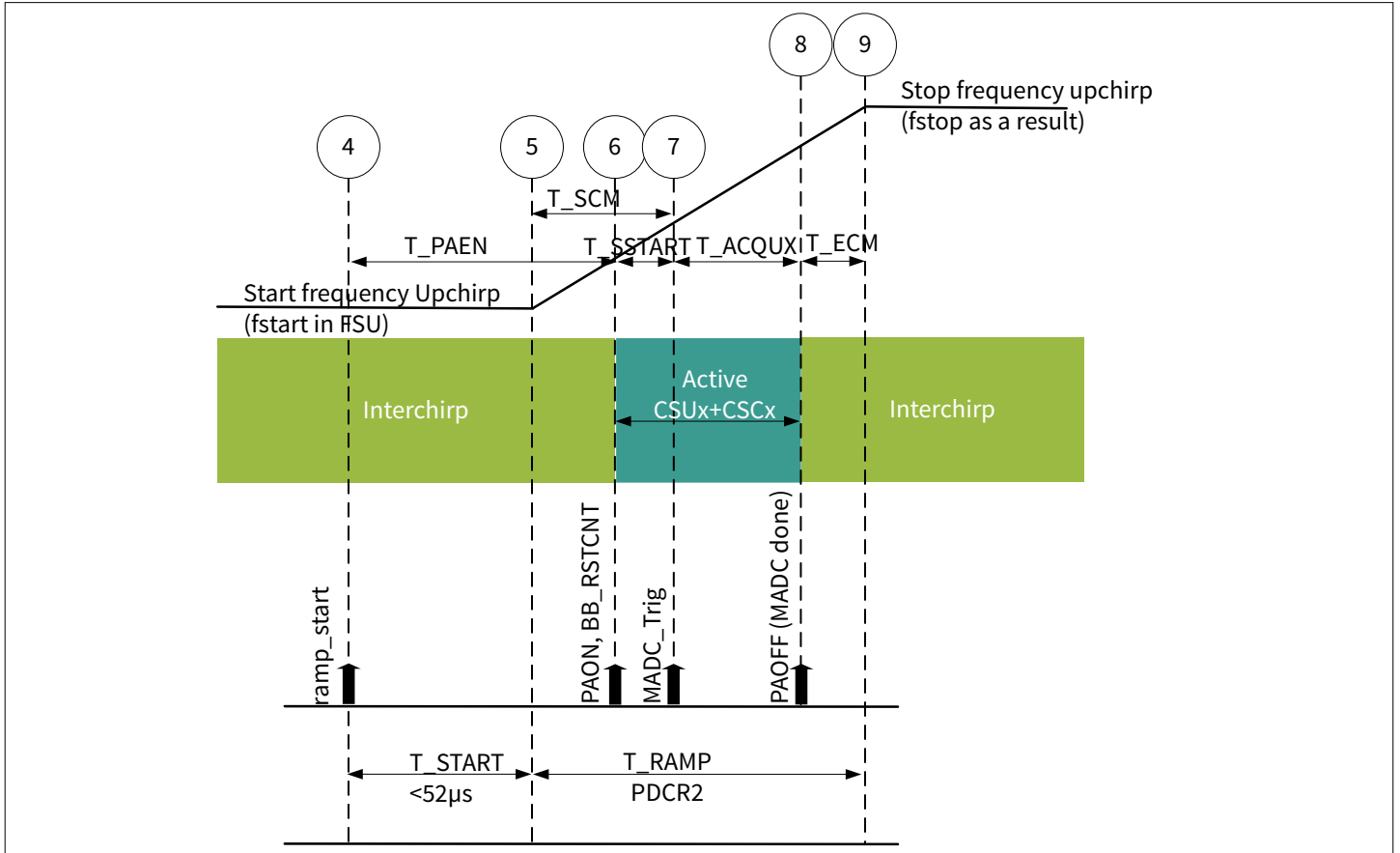
**Table 19** Deep sleep cont + idle wake-up after shape groups

| From # | To # | Description   | Signals | Related time |
|--------|------|---|---------|--------------|
| #16    | #17  | Some delay after downchirp is completed   |         | T_END        |
| #17    |      | PLL is completed its action   |         |              |
| #17    |      | Deep sleep cont mode is enabled. The difference to the normal deep sleep mode is, the $f_{SYS\_CLK}$ is kept running to count the internal timers |         |              |
| #17    |      | The internal system clock $f_{SYS\_CLK}$ is kept running  |         |              |
| #17    | #18  | Time delay programmed by the host   |         | T_EDD        |
| #18    | #1   | The chip will be in deep sleep cont mode  |         | T_SED        |
| #1b    |      | Continuous trigger coming from the FSM  |         |              |
| #1b    |      | Same start-up procedure as <a href="#">Figure 13</a> starts here  |         |              |

### 3.4 System constraints

#### 3.4.1 MADC sampling timing conditions and calculations

The number of MADC samples during a frequency chirp (up or down segment of the shape) should fulfill some specific requirements.



**Figure 18** T\_RAMP timing conditions

**Table 20** T\_RAMP timing conditions

| From # | To # | Description   | Signals | Related time    |
|--------|------|---|---------|-----------------|
| #4     |      | PLL starts counting   |         |                 |
| #4     | #5   | PLL starts  |         | T_START         |
| #5     | #9   | PLL performs the frequency upchirp, chirp from $f_{start}$ (PLLx[1]:FSU) to $f_{stop}$            |         | T_RAMP          |
| #6     | #8   | Active phase  |         |                 |
| #4     | #7   | Time to start the MADC  |         | T_PAEN+T_SSTART |
| #7     | #8   | MADC sampling time for upchirp raw data   |         | T_ACQUX         |
| #8     | #9   | End chirp margin T_ECM is needed to avoid transmission out of band. Empirically derived in system |         | T_ECM           |

(table continues...)

**Table 20 (continued) T\_RAMP timing conditions**

| From # | To # | Description   | Signals | Related time |
|--------|------|---|---------|--------------|
| #5     | #7   | Start chirp margin T_SCM is needed to avoid transmission out of band. Empirically derived in system |         | T_SCM        |

**Summary:**

ADC sampling rate  $f_{ADC\_SAMP}$  (see [Chapter 8.5.5](#)):

- $f_{ADC\_SAMP} = f_{ADC\_CLK}/ADC\_DIV$

ADC acquisition time for Upchirp T\_ACQUx:

- $T\_ACQUx = APUx/f_{ADC\_SAMP}$

Where APU is the number of samples.

End chirp margin T\_ECM is tested in system but assumed to be more than 0  $\mu$ s:

- $T\_ECM > 0 \mu s, T\_SCM > 0 \mu s$

Condition on the data acquisition start time:

- $T\_PAEN + T\_SSTART > T\_START$

Considering the start chirp margin TCM at the beginning:

- $T\_PAEN + T\_SSTART - T\_SCM = T\_START$

Overall timing equation:

- $T\_PAEN + T\_SSTART + T\_ACQUx + T\_ECM = T\_START + T\_RAMP$

**Example with fixed number of samples:**

In case the user expects a fixed number of samples, the APU is set and T\_RAMP is calculated.

The time for a frequency ramp T\_RAMP is:

- $T\_RAMP (PLLx2\#:RTU \text{ in } \text{PLL shape x register 2}) = T\_PAEN + T\_SSTART + T\_ACQUx + T\_ECM - T\_START$

**Example with fixed chirp-time (T\_RAMP):**

- $T\_ACQUx = T\_RAMP - (T\_SCM + T\_ECM)$

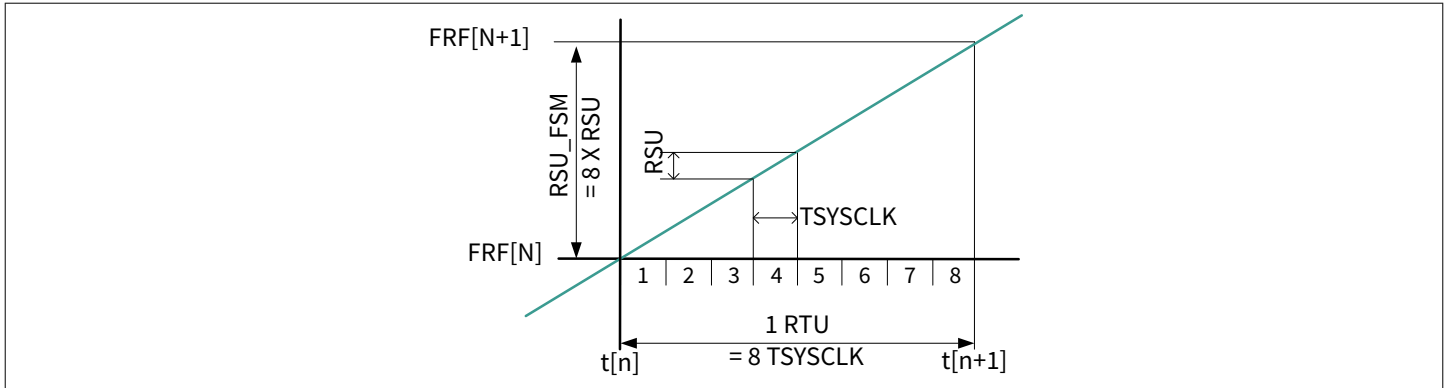
- $APU = (T\_ACQUx * f_{ADC\_SAMP}),$

- $APU (PLLx3\#:APU \text{ in } \text{PLL shape x register 3}) = (T\_RAMP - (T\_SCM + T\_ECM)) * (f_{SYS\_CLK}/ADC\_DIV)$

**3.4.2 PLL frequency ramp setup**

The RF frequency ramps generated by the PLL are controlled through the PLLx registers (see [PLL shape x register 0](#)), where the bit fields FSU, RSU and RTU control the Upchirp of a shape and the registers FSD, RSD and RTD control the down chirp of a shape. The following description refers only to up chirp ramp setup. The given formulas can be adopted to down chirp ramps by replacing FSU by FSD, RSU by RSD and RTU by RTD.

Each RF frequency ramp is defined by the start frequency programmed to FSU, the ramp slope programmed to RSU and the ramp time programmed to RTU. It must be noted that the slope in RSU is specified as frequency increment per clock cycle while the ramp time in RTU is specified as number of steps where a single step means 8 clock cycles. The relation between RSU and RTU is shown in the following figure.



**Figure 19 Relationship between RTU and RSU**

The value  $N_{FSU}$  that is programmed to FSU bit field to control the ramp start frequency is a signed 2's complement number in the range of  $-2^{23} \dots (2^{23} - 1)$ . The relation between the RF frequency  $f_{RF}$  and  $N_{FSU}$  is given by:

$$f_{RF} = 8f_{SYS\_CLK} \left[ 4(N_{DIVSET} + 2) + 8 + \frac{N_{FSU}}{2^{20}} \right] \quad (1)$$

where  $f_{SYS\_CLK}$  is the frequency of the reference clock oscillator and  $N_{DIVSET}$  is the value programmed to the bit field DIVSET in register PACR2 (default 20, see [PLL analog control register 2](#)). Accordingly the value  $N_{FSU}$  can be calculated by this formula:

$$N_{FSU} = 2^{20} \left[ \frac{f_{RF}}{8f_{SYS\_CLK}} - 4(N_{DIVSET} + 2) - 8 \right] \quad (2)$$

The value  $N_{RSU}$  that is programmed to RSU bit field to control the frequency increment per clock cycle is also a signed 2's complement number in the range of  $-2^{23} \dots (2^{23} - 1)$ . The relation between the RF frequency increment  $\Delta f_{RF}$  and  $N_{RSU}$  is given by:

$$\Delta f_{RF} = 8f_{SYS\_CLK} \frac{N_{RSU}}{2^{20}} \quad (3)$$

or

$$N_{RSU} = 2^{20} \frac{\Delta f_{RF}}{8f_{SYS\_CLK}} \quad (4)$$

**Note:** Both slope bit fields RSU and RSD can hold positive and negative values, so an up chirp can also be programmed with a falling ramp and a down chirp can be programmed with a rising ramp. The naming convention “up chirp” and “down chirp” are based on the assumption that a triangle shape always starts with the rising ramp. Therefore regardless of the actual ramp slope the up chirp registers always refer to the first chirp of a shape and the down chirp registers always refer to the 2nd chirp of a shape in triangle mode.

### PLL setup example 1 ( $f_{SYS\_CLK} = 80$ MHz)

With a reference clock frequency of 40 MHz and activated frequency doubler the recommended value for  $N_{DIVSET}$  is 20, the default values. With these parameters the conversion formulas simplify to:

$$N_{\text{FSU}} = 2^{20} \left[ \frac{f_{\text{RF}}}{640 \text{ MHz}} - 96 \right] \quad (5)$$

and

$$N_{\text{RSU}} = 2^{20} \frac{\Delta f_{\text{RF}}}{640 \text{ MHz}} \quad (6)$$

With the PLL's 24 bit 2's complement frequency registers the total programmable RF frequency range is  $56.32 \text{ GHz} \leq f_{\text{RF}} \leq 66.559 \text{ GHz}$ . This may be a wider range than the effectively achievable frequency range.

To achieve a frequency ramp for example from 58 GHz to 62 GHz in 36  $\mu\text{s}$ , the FSU register is programmed to:

$$N_{\text{FSU}} = 2^{20} \left[ \frac{58 \text{ GHz}}{640 \text{ MHz}} - 96 \right] = -5636096 \hat{=} AA0000_{\text{hex}} \quad (7)$$

The ramp time bit field RTU is programmed to:

$$N_{\text{RTU}} = \frac{t_{\text{ramp}}}{8 * T_{\text{SYS\_CLK}}} = 36 \mu\text{s} \frac{80 \text{ MHz}}{8} = 360 \quad (8)$$

The frequency increment per clock cycle result to:

$$\Delta f_{\text{RF}} = \frac{f_{\text{RF, end}} - f_{\text{RF, start}}}{8 * N_{\text{RTU}}} = \frac{62 \text{ GHz} - 58 \text{ GHz}}{8 * 360} = \frac{4 \text{ GHz}}{2880} = 1.3\bar{8} \text{ MHz} \quad (9)$$

Accordingly the bit field RSU is programmed to:

$$N_{\text{RSU}} = 2^{20} \frac{1.3\bar{8} \text{ MHz}}{640 \text{ MHz}} = 2275.\bar{5} \cong 2276 \hat{=} 0008E4_{\text{hex}} \quad (10)$$

Due to rounding errors from the above calculation, the ramp will end at a slightly different end frequency:

$$f_{\text{RF, end}} = f_{\text{RF, start}} + 8 * N_{\text{RTU}} * \frac{640 \text{ MHz}}{2^{20}} N_{\text{RSU}} = 62.000781 \text{ GHz} \quad (11)$$

### PLL setup example 2 ( $f_{\text{SYS\_CLK}} = 76.8 \text{ MHz}$ )

With a reference clock frequency of 38.4 MHz and activated frequency doubler the recommended value for  $N_{\text{DIVSET}}$  is 21. With these parameters the conversion formulas simplify to:

$$N_{\text{FSU}} = 2^{20} \left[ \frac{f_{\text{RF}}}{614.4 \text{ MHz}} - 100 \right] \quad (12)$$

and

$$N_{\text{RSU}} = 2^{20} \frac{\Delta f_{\text{RF}}}{614.4 \text{ MHz}} \quad (13)$$

**3 Shapes, frames and channel set definition**

With the PLL's 24 bit 2's complement frequency registers the total programmable RF frequency range is  $56.5248 \text{ GHz} \leq f_{\text{RF}} \leq 66.3552 \text{ GHz}$ . This may be a wider range than the effectively achievable frequency range.

To achieve a frequency ramp from 58 GHz to 62 GHz in 36  $\mu\text{s}$ , the FSU register is programmed to:

$$N_{\text{FSU}} = 2^{20} \left[ \frac{58 \text{ GHz}}{614.4 \text{ MHz}} - 100 \right] = -5870933.\bar{3} \cong -5870933 \hat{=} A66AAB_{\text{hex}} \quad (14)$$

The ramp time bit field RTU is programmed to:

$$N_{\text{RTU}} = \frac{t_{\text{ramp}}}{8 * T_{\text{SYSCLK}}} = 36 \mu\text{s} \frac{76.8 \text{ MHz}}{8} = 345.6 \cong 346 \quad (15)$$

The frequency increment per clock cycle results to:

$$\Delta f_{\text{RF}} = \frac{f_{\text{RF,end}} - f_{\text{RF,start}}}{8 * N_{\text{RTU}}} = \frac{62 \text{ GHz} - 58 \text{ GHz}}{8 * 346} = \frac{4 \text{ GHz}}{2768} = 1.44509 \text{ MHz} \quad (16)$$

Accordingly, the bit field RSU is programmed to:

$$N_{\text{RSU}} = 2^{20} \frac{1.44509 \text{ MHz}}{614.4 \text{ MHz}} = 2466.28 \cong 2466 \hat{=} 0009A2_{\text{hex}} \quad (17)$$

Due to rounding errors from the above calculation, the ramp will end at a slightly different end frequency:

$$f_{\text{RF,start}} = 614.4 \text{ MHz} \left[ 100 + \frac{N_{\text{FSU}}}{2^{20}} \right] = 58.0000002 \text{ GHz} \quad (18)$$

$$f_{\text{RF,end}} = f_{\text{RF,start}} + 8 * N_{\text{RTU}} * \frac{614.4 \text{ MHz}}{2^{20}} N_{\text{RSU}} = 61.99954 \text{ GHz} \quad (19)$$

## 4 BGT60ATR24AIP registers

An array of registers accessible via the SPI is used to control and program the states of the different blocks inside the chip.

The registers are arranged in blocks of 24 bits each. Each block is identified by its unique address. The registers are accessed from the SPI module. The bit fields from each register are arranged in MSB first order.

The following table gives an overview on the BGT60ATR24AIP registers.

### 4.1 Abbreviations

Access modes on the registers:

- r: readable register or bit field
- w: writeable register or bit field
- h: hardware writeable register or bit field

**Note:** The *reserved (RSVD)* bits in the registers should not be modified. They should be kept in the reset state unless otherwise specified. This is also valid for the RSVD states of multi bit fields.

### 4.2 Register overview - BGT60ATR24AIP (ascending offset address)

**Table 21** Register overview - BGT60ATR24AIP (ascending offset address)

| Short name   | Long name                               | Offset address            | Page number |
|--------------|---|---------------------------|-------------|
| MAIN         | Main register                           | 000 <sub>H</sub>          | 37          |
| ADC0         | Multi ADC control register              | 001 <sub>H</sub>          | 40          |
| CHIP_Version | Digital and RF version register         | 002 <sub>H</sub>          | 41          |
| STAT1        | Status register 1                       | 003 <sub>H</sub>          | 42          |
| PACR1        | PLL analog control register 1           | 004 <sub>H</sub>          | 42          |
| PACR2        | PLL analog control register 2           | 005 <sub>H</sub>          | 44          |
| SFCTL        | SPI and FIFO control register           | 006 <sub>H</sub>          | 46          |
| SADC_CTRL    | Sensor ADC control register             | 007 <sub>H</sub>          | 47          |
| CSI_0        | Channel set idle register 0             | 008 <sub>H</sub>          | 49          |
| CSI_1        | Channel set idle register 1             | 009 <sub>H</sub>          | 51          |
| CSI_2        | Channel set idle register 2             | 00A <sub>H</sub>          | 52          |
| CSCI         | Channel set control idle register       | 00B <sub>H</sub>          | 55          |
| CSDS_0       | Channel set deep sleep register 0       | 00C <sub>H</sub>          | 56          |
| CSDS_1       | Channel set deep sleep register 1       | 00D <sub>H</sub>          | 58          |
| CSDS_2       | Channel set deep sleep register 2       | 00E <sub>H</sub>          | 59          |
| CSCDS        | Channel set control deep sleep register | 00F <sub>H</sub>          | 62          |
| CSUx_0       | Channel set up x register 0             | 010 <sub>H</sub> +(x-1)*7 | 63          |
| CSUx_1       | Channel set up x register 1             | 011 <sub>H</sub> +(x-1)*7 | 65          |
| CSUx_2       | Channel set up x register 2             | 012 <sub>H</sub> +(x-1)*7 | 66          |
| CSDx_0       | Channel set down x register 0           | 013 <sub>H</sub> +(x-1)*7 | 69          |

(table continues...)

**Table 21** (continued) Register overview - BGT60ATR24AIP (ascending offset address)

| Short name  | Long name                      | Offset address            | Page number |
|-------------|--------------------------------|---------------------------|-------------|
| CSDx_1      | Channel set down x register 1  | 014 <sub>H</sub> +(x-1)*7 | 71          |
| CSDx_2      | Channel set down x register 2  | 015 <sub>H</sub> +(x-1)*7 | 72          |
| CSCx        | Channel set control x register | 016 <sub>H</sub> +(x-1)*7 | 75          |
| CCR0        | Chirp control register 0       | 02C <sub>H</sub>          | 76          |
| CCR1        | Chirp control register 1       | 02D <sub>H</sub>          | 77          |
| CCR2        | Chirp control register 2       | 02E <sub>H</sub>          | 78          |
| CCR3        | Chirp control register 3       | 02F <sub>H</sub>          | 78          |
| PLLx_0      | PLL shape x register 0         | 030 <sub>H</sub> +(x-1)*8 | 79          |
| PLLx_1      | PLL shape x register 1         | 031 <sub>H</sub> +(x-1)*8 | 80          |
| PLLx_2      | PLL shape x register 2         | 032 <sub>H</sub> +(x-1)*8 | 80          |
| PLLx_3      | PLL shape x register 3         | 033 <sub>H</sub> +(x-1)*8 | 81          |
| PLLx_4      | PLL shape x register 4         | 034 <sub>H</sub> +(x-1)*8 | 81          |
| PLLx_5      | PLL shape x register 5         | 035 <sub>H</sub> +(x-1)*8 | 82          |
| PLLx_6      | PLL shape x register 6         | 036 <sub>H</sub> +(x-1)*8 | 82          |
| PLLx_7      | PLL shape x register 7         | 037 <sub>H</sub> +(x-1)*8 | 83          |
| RFT0        | RF test register 0             | 055 <sub>H</sub>          | 84          |
| EFUSE0      | EFUSE register 0               | 057 <sub>H</sub>          | 85          |
| EFUSE1      | EFUSE register 1               | 058 <sub>H</sub>          | 86          |
| PDFT0       | PLL test register 0            | 059 <sub>H</sub>          | 87          |
| CHIP_ID0    | Chip ID register 0             | 05D <sub>H</sub>          | 87          |
| CHIP_ID1    | Chip ID register 1             | 05E <sub>H</sub>          | 88          |
| CLK_IN      | Clock input register           | 05F <sub>H</sub>          | 88          |
| WU          | Wake up register               | 060 <sub>H</sub>          | 90          |
| STAT0       | Status register 0              | 061 <sub>H</sub>          | 91          |
| SADC_RESULT | Sensor ADC result register     | 062 <sub>H</sub>          | 93          |
| FSTAT       | FIFO status register           | 063 <sub>H</sub>          | 93          |

### 4.3 Main register

This register controls the top level behavior of the chip.

|               |                 |                      |
|---------------|-----------------|----------------------|
| <b>MAIN</b>   | Offset address: | 000 <sub>H</sub>     |
| Main register | Reset value:    | 1C 0F00 <sub>H</sub> |

4 BGT60ATR24AIP registers

|             |    |    |    |                  |                  |                  |                  |                  |                  |                  |                           |                   |                  |                 |                    |                      |    |                         |    |                         |    |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|-------------|----|----|----|------------------|------------------|------------------|------------------|------------------|------------------|------------------|---------------------------|-------------------|------------------|-----------------|--------------------|----------------------|----|-------------------------|----|-------------------------|----|-----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
|             |    |    |    |                  |                  |                  |                  |                  |                  |                  |                           |                   |                  |                 | 23                 | 22                   | 21 | 20                      | 19 | 18                      | 17 | 16              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|             |    |    |    |                  |                  |                  |                  |                  |                  |                  |                           |                   |                  |                 | <b>LDO_MOD_E</b>   | <b>LOAD_STRENGTH</b> |    | <b>MADC_BG_C LK_DIV</b> |    | <b>SADC_BG_C LK_DIV</b> |    | <b>CW_MOD_E</b> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|             |    |    |    |                  |                  |                  |                  |                  |                  |                  |                           |                   |                  |                 | rw                 | rw                   |    | rw                      |    | rw                      |    | rw              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 15          | 14 | 13 | 12 | 11               | 10               | 9                | 8                | 7                | 6                | 5                | 4                         | 3                 | 2                | 1               | 0                  |                      |    |                         |    |                         |    |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| <b>RSVD</b> |    |    |    | <b>PU_EN_D03</b> | <b>PU_EN_D02</b> | <b>PU_EN_D01</b> | <b>PU_EN_D00</b> | <b>PU_EN_CLK</b> | <b>PU_EN_CSN</b> | <b>PU_EN_IRQ</b> | <b>SPI_BROADCAST_MODE</b> | <b>FIFO_RESET</b> | <b>FSM_RESET</b> | <b>SW_RESET</b> | <b>FRAME_START</b> |                      |    |                         |    |                         |    |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| r           |    |    |    | rw               | rw               | rw               | rw               | rw               | rw               | rw               | rw                        | w                 | w                | w               | w                  |                      |    |                         |    |                         |    |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

| Field              | Bits | Type | Description  |
|--------------------|------|------|--|
| FRAME_START        | 0    | w    | <b>Start a frame generation:</b><br>0 <sub>B</sub> ... No effect<br>1 <sub>B</sub> ... Executes a frame start and clears this bit<br>Note: Can be stopped by executing a HW_RESET, SW_RESET or FSM_RESET.  |
| SW_RESET           | 1    | w    | <b>Reset the complete chip:</b><br>0 <sub>B</sub> ... No effect<br>1 <sub>B</sub> ... Executes a software reset and clears this bit  |
| FSM_RESET          | 2    | w    | <b>Reset the Finite State Machine:</b><br>0 <sub>B</sub> ... No effect<br>1 <sub>B</sub> ... Executes a FSM reset and clears this bit  |
| FIFO_RESET         | 3    | w    | <b>Reset the FIFO:</b><br>0 <sub>B</sub> ... No effect<br>1 <sub>B</sub> ... Executes a FIFO reset and clears this bit   |
| SPI_BROADCAST_MODE | 4    | rw   | <b>SPI broadcast mode:</b><br>0 <sub>B</sub> ... SPI broadcast mode disabled<br>1 <sub>B</sub> ... SPI broadcast mode enabled<br>When enabled the output drivers of SPI pins are disabled to avoid conflicts on shared MISO lines. Can be used to program multiple devices at the same time (e.g. initial configuration or trigger FRAME_START). It is not allowed to set this bit together with SW_RESET. SPI_BROADCAST_MODE and SW_RESET are mutually exclusive. |
| PU_EN_IRQ          | 5    | rw   | <b>Pull-up of IRQ pad:</b><br>0 <sub>B</sub> ... disabled<br>1 <sub>B</sub> ... enabled  |
| PU_EN_CSN          | 6    | rw   | <b>Pull-up of CSN pad:</b><br>0 <sub>B</sub> ... disabled<br>1 <sub>B</sub> ... enabled  |
| PU_EN_CLK          | 7    | rw   | <b>Pull-up of CLK pad:</b><br>0 <sub>B</sub> ... disabled<br>1 <sub>B</sub> ... enabled  |

(table continues...)

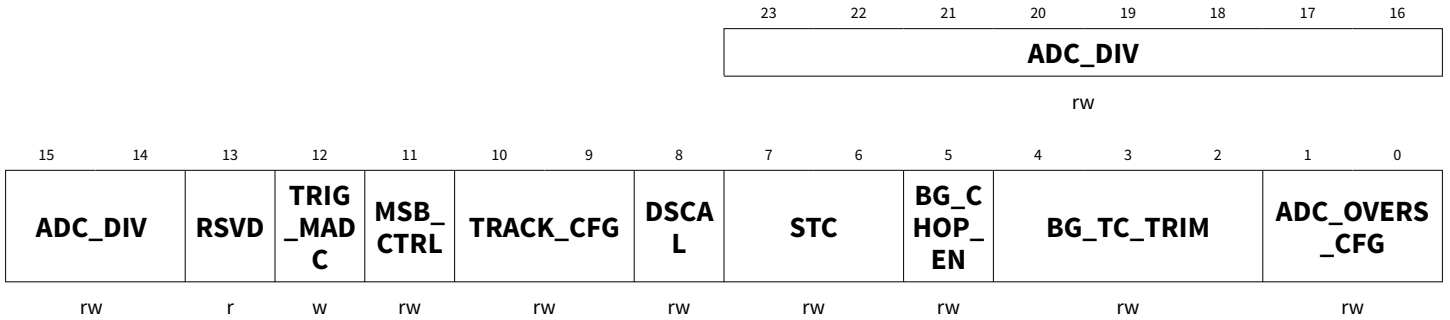
(continued)

| Field           | Bits  | Type | Description   |
|-----------------|-------|------|---|
| PU_EN_DIO0      | 8     | rw   | <b>Pull-up of DIO0 pad:</b><br>0 <sub>B</sub> ... disabled<br>1 <sub>B</sub> ... enabled  |
| PU_EN_DIO1      | 9     | rw   | <b>Pull-up of DIO1 pad:</b><br>0 <sub>B</sub> ... disabled<br>1 <sub>B</sub> ... enabled  |
| PU_EN_DIO2      | 10    | rw   | <b>Pull-up of DIO2 pad:</b><br>0 <sub>B</sub> ... disabled<br>1 <sub>B</sub> ... enabled  |
| PU_EN_DIO3      | 11    | rw   | <b>Pull-up of DIO3 pad:</b><br>0 <sub>B</sub> ... disabled<br>1 <sub>B</sub> ... enabled  |
| RSVD            | 15:12 | r    | <b>Reserved</b>   |
| CW_MODE         | 16    | rw   | <b>Continuous wave mode:</b><br>0 <sub>B</sub> ... Normal mode<br>1 <sub>B</sub> ... Continuous wave mode<br>Note: When active no shapes are executed but PLL, RF, ADC run with values programmed in PDFT0, PDFT1 and channel set 1 registers.  |
| SADC_BG_CLK_DIV | 18:17 | rw   | <b>SADC bandgap clock frequency divider value:</b><br>0 <sub>D</sub> ... Bandgap clock off<br>1 <sub>D</sub> ... Divider value is 1<br>2 <sub>D</sub> ... Divider value is 2<br>3 <sub>D</sub> ... Divider value is 4<br>Note: not clock tree balanced  |
| MADC_BG_CLK_DIV | 20:19 | rw   | <b>MADC bandgap clock frequency divider value:</b><br>0 <sub>D</sub> ... Bandgap clock off<br>1 <sub>D</sub> ... Divider value is 1<br>2 <sub>D</sub> ... Divider value is 2<br>3 <sub>D</sub> ... Divider value is 4<br>Note: not clock tree balanced  |
| LOAD_STRENGTH   | 22:21 | rw   | <b>LDO dummy load to smooth current peaks (over and under shoots of VDD<sub>C</sub> caused by toggling of digital logic):</b><br>0 <sub>D</sub> ... Disabled<br>1 <sub>D</sub> ... 100 μA (current in the dummy load)<br>2 <sub>D</sub> ... 200 μA (current in the dummy load)<br>3 <sub>D</sub> ... 400 μA (current in the dummy load) |
| LDO_MODE        | 23    | rw   | <b>The LDO settling time is defined by:</b><br>0 <sub>B</sub> ... Low power (50 μA), slow settling time<br>1 <sub>B</sub> ... High power (100 μA), fast settling time   |

## 4.4 Multi ADC control register

The bits in this register are used to set properly the ADCs in the Rx chain.

**ADC0** Offset address: 001<sub>H</sub>  
Multi ADC control register Reset value: 0A 0200<sub>H</sub>



| Field         | Bits | Type | Description   |
|---------------|------|------|---|
| ADC_OVERS_CFG | 1:0  | rw   | <b>ADC oversampling configuration:</b><br>0 <sub>D</sub> ... No oversampling (standard 11 bits conversion)<br>1 <sub>D</sub> ... Reserved<br>2 <sub>D</sub> ... Reserved<br>3 <sub>D</sub> ... Reserved   |
| BG_TC_TRIM    | 4:2  | rw   | <b>Temperature coefficient trimming (static):</b><br>0 <sub>D</sub> ... Minimum value<br>7 <sub>D</sub> ... Maximum value   |
| BG_CHOP_EN    | 5    | rw   | <b>Enables chopping within the bandgap:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| STC           | 7:6  | rw   | <b>Sample time control:</b><br>0 <sub>D</sub> ... 50 ns<br>1 <sub>D</sub> ... 100 ns<br>2 <sub>D</sub> ... 200 ns<br>3 <sub>D</sub> ... 400 ns  |
| DSCAL         | 8    | rw   | <b>Disables startup calibration:</b><br>0 <sub>B</sub> ... Enabled<br>1 <sub>B</sub> ... Disabled   |
| TRACK_CFG     | 10:9 | rw   | <b>Tracking conversion configuration bits:</b><br>0 <sub>D</sub> ... No sub conversion<br>1 <sub>D</sub> ... 1 sub conversion<br>2 <sub>D</sub> ... 3 sub conversions<br>3 <sub>D</sub> ... 7 sub conversions<br>Note: Sub conversions are executed and averaged. |
| MSB_CTRL      | 11   | rw   | <b>MSB decision time selection during calibration and conversion:</b><br>0 <sub>B</sub> ... Single MSB decision time<br>1 <sub>B</sub> ... Double MSB decision time   |

(table continues...)

(continued)

| Field     | Bits  | Type | Description  |
|-----------|-------|------|--|
| TRIG_MADC | 12    | w    | <b>Trigger for manual ADC conversion:</b><br>0 <sub>B</sub> ... No effect<br>1 <sub>B</sub> ... Executes a single ADC conversion and clears this bit   |
| RSVD      | 13    | r    | <b>Reserved</b>  |
| ADC_DIV   | 23:14 | rw   | <b>ADC sampling frequency divider value. The actual sampling frequency will be <math>f_{ADC\_SAMP} = f_{ADC\_CLK} / ADC\_DIV</math>:</b><br>0 <sub>D</sub> ..19 <sub>D</sub> ... Reserved<br>20 <sub>D</sub> ... Minimum divider value<br>1023 <sub>D</sub> ... Maximum divider value<br>Note: A typical value is 33 <sub>D</sub> resulting in $f_{ADC\_SAMP} = 2.42$ MS/s (@ $f_{SYS\_CLK} = 80$ MHz) |

## 4.5 Digital and RF version register

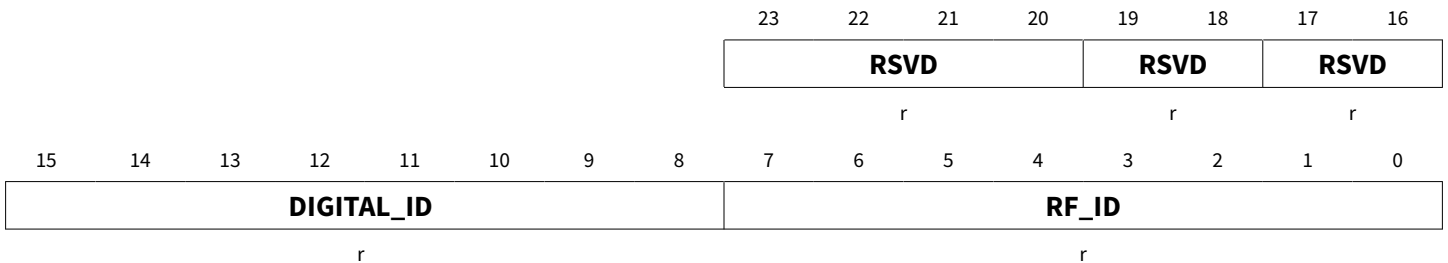
The register CHIP\_Version provides information regarding the digital code version, the RF block version, and the antenna configuration (number of channels, position of the antennas e.g.). It is used by the driver to configure the device properly according to the information below.

### CHIP\_Version

Digital and RF version register

Offset address: 002<sub>H</sub>

Reset values see: [Table 22](#)



| Field      | Bits   | Type | Description   |
|------------|--------|------|---|
| RF_ID      | 7:0    | r    | <b>Revision of analog logic:</b><br>15 <sub>D</sub> ... BGT60ATR24AIP         |
| DIGITAL_ID | 15:8   | r    | <b>Revision of digital control logic:</b><br>9 <sub>D</sub> ... BGT60ATR24AIP |
| RSVD       | 23:16, | r    | <b>Reserved</b>   |

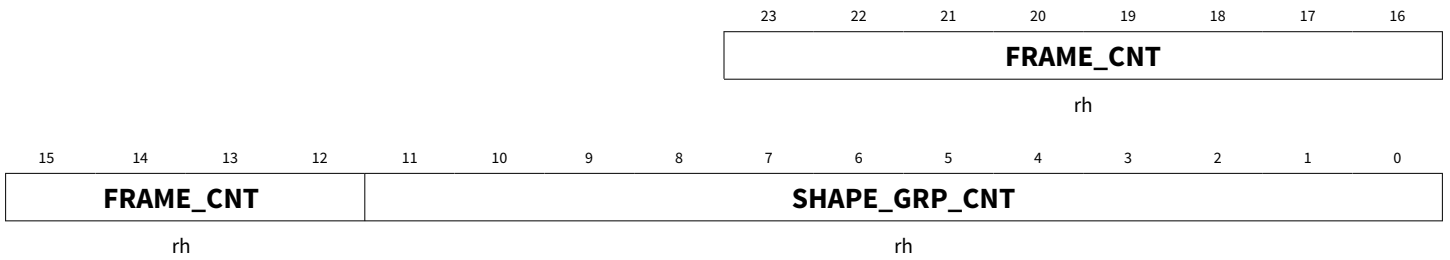
**Table 22** Reset values of **CHIP\_Version**

| Reset type | Reset value                                   | Note |
|------------|---|------|
| Reset      | X000 0000 0000 1001 0000<br>1111 <sub>B</sub> |      |

## 4.6 Status register 1

The status register provides internal counter values for the actual number of frames and shapes. They are also provided to the data header. However, it should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after e.g. 100  $\mu$ s.

**STAT1** Offset address: 003<sub>H</sub>  
Status register 1 Reset value: 00 0000<sub>H</sub>

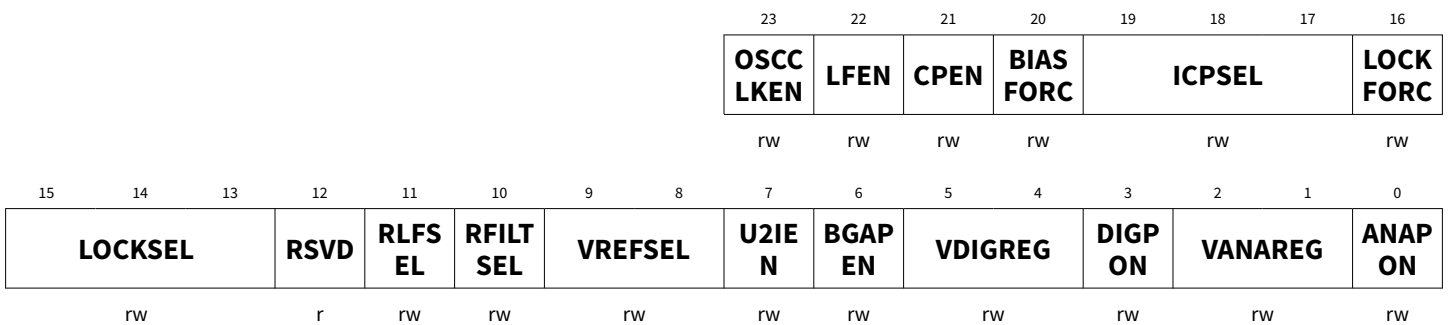


| Field         | Bits  | Type | Description   |
|---------------|-------|------|---|
| SHAPE_GRP_CNT | 11:0  | rh   | <b>Shape group counter:</b><br>0 <sub>D</sub> ... Reset value / rollover value after maximum value reached<br>4095 <sub>D</sub> ... Maximum value   |
| FRAME_CNT     | 23:12 | rh   | <b>Frame counter:</b><br>0 <sub>D</sub> ... Reset value / rollover value after maximum value reached<br>4095 <sub>D</sub> ... Maximum value<br>Note: This field is for debug only. FRAME_CNT info should not be used when endless mode enabled (please check CCR2:MAX_FRAME_CNT). |

## 4.7 PLL analog control register 1

The bits in this register are used to properly set the PLL.

**PACR1** Offset address: 004<sub>H</sub>  
PLL analog control register 1 Reset value: 19 6524<sub>H</sub>



| Field    | Bits | Type | Description  |
|----------|------|------|--|
| ANAPON   | 0    | rw   | <b>Enables the power of the analog regulator:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| VANAREG  | 2:1  | rw   | <b>Selects the output voltage of analog regulator:</b><br>0 <sub>D</sub> ... 1.44 V<br>1 <sub>D</sub> ... 1.50 V<br>2 <sub>D</sub> ... 1.55 V<br>3 <sub>D</sub> ... 1.60 V (@V <sub>bg</sub> = 1.2 V)  |
| DIGPON   | 3    | rw   | <b>Enables the power of the digital regulator:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| VDIGREG  | 5:4  | rw   | <b>Selects the output voltage of digital regulator:</b><br>0 <sub>D</sub> ... 1.44 V<br>1 <sub>D</sub> ... 1.50 V<br>2 <sub>D</sub> ... 1.55 V<br>3 <sub>D</sub> ... 1.60 V (@V <sub>bg</sub> = 1.2 V)   |
| BGAPEN   | 6    | rw   | <b>Enables bandgap reference:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| U2IEN    | 7    | rw   | <b>Enables voltage-to-current converter:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| VREFSEL  | 9:8  | rw   | <b>Selects the reference voltage/common mode level of loop filter:</b><br>0 <sub>D</sub> ... 433 mV<br>1 <sub>D</sub> ... 506 mV<br>2 <sub>D</sub> ... 578 mV<br>3 <sub>D</sub> ... 650 mV   |
| RFILTSEL | 10   | rw   | <b>Selects the resistance R<sub>filt</sub> of the reference filter:</b><br>0 <sub>B</sub> ... R <sub>filt</sub> = 100 kΩ<br>1 <sub>B</sub> ... R <sub>filt</sub> = 1 MΩ<br>Note: Switch together with CPEN from 0 <sub>B</sub> to 1 <sub>B</sub> to improve start-up time! |
| RLFSEL   | 11   | rw   | <b>Selects the resistance R<sub>f</sub> inside the loop filter:</b><br>0 <sub>B</sub> ... R <sub>f</sub> = 5 kΩ<br>1 <sub>B</sub> ... R <sub>f</sub> = 7 kΩ  |
| RSVD     | 12   | r    | <b>Reserved</b>  |

(table continues...)

(continued)

| Field    | Bits  | Type | Description   |
|----------|-------|------|---|
| LOCKSEL  | 15:13 | rw   | <b>Selects the lock detection window:</b><br>0 <sub>D</sub> ... 0.265 ns<br>1 <sub>D</sub> ... 0.5 ns<br>2 <sub>D</sub> ... 1.0 ns<br>3 <sub>D</sub> ... 1.5 ns<br>4 <sub>D</sub> ... 2.0 ns<br>5 <sub>D</sub> ... 2.8 ns<br>6 <sub>D</sub> ... 3.8 ns<br>7 <sub>D</sub> ... 4.6 ns       |
| LOCKFORC | 16    | rw   | <b>Forces the lock signal:</b><br>0 <sub>B</sub> ... Lock not forced<br>1 <sub>B</sub> ... Lock forced (to high)  |
| ICPSEL   | 19:17 | rw   | <b>Selects the charge pump current:</b><br>0 <sub>B</sub> ... 40 μA<br>1 <sub>B</sub> ... 80 μA<br>2 <sub>B</sub> ... 120 μA<br>3 <sub>B</sub> ... 160 μA<br>4 <sub>B</sub> ... 200 μA<br>5 <sub>B</sub> ... 240 μA<br>6 <sub>B</sub> ... 280 μA<br>7 <sub>B</sub> ... 280 μA             |
| BIASFORC | 20    | rw   | <b>Enables fixed biasing inside charge pump:</b><br>0 <sub>B</sub> ... Disabled (Bias regulation loop active)<br>1 <sub>B</sub> ... Enabled (Bias regulation loop deactivated)  |
| CPEN     | 21    | rw   | <b>Enables charge pump:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| LFEN     | 22    | rw   | <b>Enables loop filter:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| OSCCLKEN | 23    | rw   | <b>Enables system clock (SYS_CLK):</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: This bit is controlled by FSM during operation. After deep sleep this bit should be enabled by the host. Before the MAIN:FRAME_START is raised the OSCCLKEN must be enabled! |

## 4.8 PLL analog control register 2

The bits in this register are used to properly set the PLL.

### PACR2

PLL analog control register 2

Offset address: 005<sub>H</sub>

Reset value: 04 0014<sub>H</sub>



(continued)

| Field    | Bits  | Type | Description   |
|----------|-------|------|---|
| TR_DIVEN | 23:21 | rw   | <b>Time for T_DIVEN. Defines the delay after PACR2:DIVEN is handed over to PLL and pll_rst_n is released. Running in parallel to T_INIT1.</b><br>$T\_DIVEN = (TR\_DIVEN * 32 + 1) * T_{SYS\_CLK}$<br>0 <sub>D</sub> ... Minimum value<br>7 <sub>D</sub> ... Maximum value |

## 4.9 SPI and FIFO control register

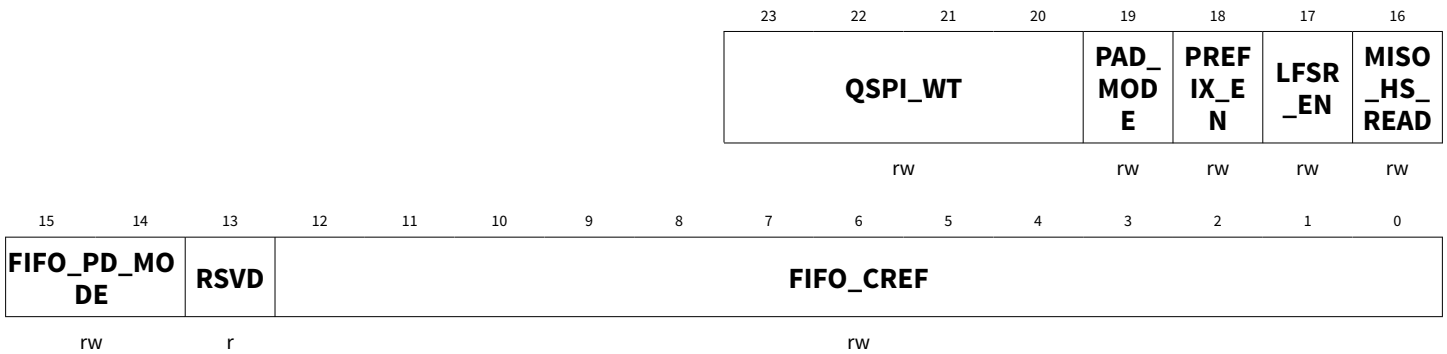
This register is used to configure the SPI and FIFO.

### SFCTL

SPI and FIFO control register

Offset address: 006<sub>H</sub>

Reset value: 79 6000<sub>H</sub>



| Field        | Bits  | Type | Description   |
|--------------|-------|------|---|
| FIFO_CREF    | 12:0  | rw   | <b>FIFO compare reference defines the compare filling status for interrupt and CREF reporting. When filling status is &gt; FIFO_CREF an interrupt is issued:</b><br>0 <sub>D</sub> ... Minimum value is 0, interrupt generated in case first sample is written into FIFO<br>8191 <sub>D</sub> ... Maximum value in case FIFO is full with 8192 memory locations |
| RSVD         | 13    | r    | <b>Reserved</b>   |
| FIFO_PD_MODE | 15:14 | rw   | <b>RAM power mode for power saving (power switch):</b><br>0 <sub>D</sub> ... FIFO RAM always powered up<br>1 <sub>D</sub> ... FIFO RAM powered down during Deepsleep<br>2 <sub>D</sub> ... FIFO RAM powered down during Deepsleep + Pre-Idle + Idle<br>3 <sub>D</sub> ... Reserved<br>Note: RAM is only powered down when FIFO is empty.                        |

(table continues...)

(continued)

| Field        | Bits  | Type | Description  |
|--------------|-------|------|--|
| MISO_HS_READ | 16    | rw   | <b>Change working edge of SPI DO (MISO) to enable higher SPI frequencies (&gt;= 25 MHz):</b><br>0 <sub>B</sub> ... MISO data is sent with falling edge of SPI_CLK<br>1 <sub>B</sub> ... MISO data is sent with rising edge of SPI_CLK<br>Note: HS_RD = 0 <sub>B</sub> can only be used for a f <sub>SPI_CLK</sub> less than 25 MHz. For high speed transfer please check the timing of the SPI master and adjust settings accordingly. The setting becomes active when the last bit of FSCTL is clocked out and it affects MISO immediately. |
| LFSR_EN      | 17    | rw   | <b>Enable LFSR data generation:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: LFSR should be enabled after a FIFO reset to ensure an empty FIFO.   |
| PREFIX_EN    | 18    | rw   | <b>Enables the prefix data header written into the FIFO prior to the sampling data of each chirp:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| PAD_MODE     | 19    | rw   | <b>SPI pad driver mode to control the slew rate:</b><br>0 <sub>B</sub> ... Normal mode<br>1 <sub>B</sub> ... Strong mode (enables up to 15% shorter fall times)  |
| QSPI_WT      | 23:20 | rw   | <b>Number of QSPI wait cycles:</b><br>0 <sub>D</sub> ... Reserved<br>1 <sub>D</sub> ...15 <sub>D</sub> ... QSPI_WT + 1 SYS_CLK cycle delay   |

### 4.10 Sensor ADC control register

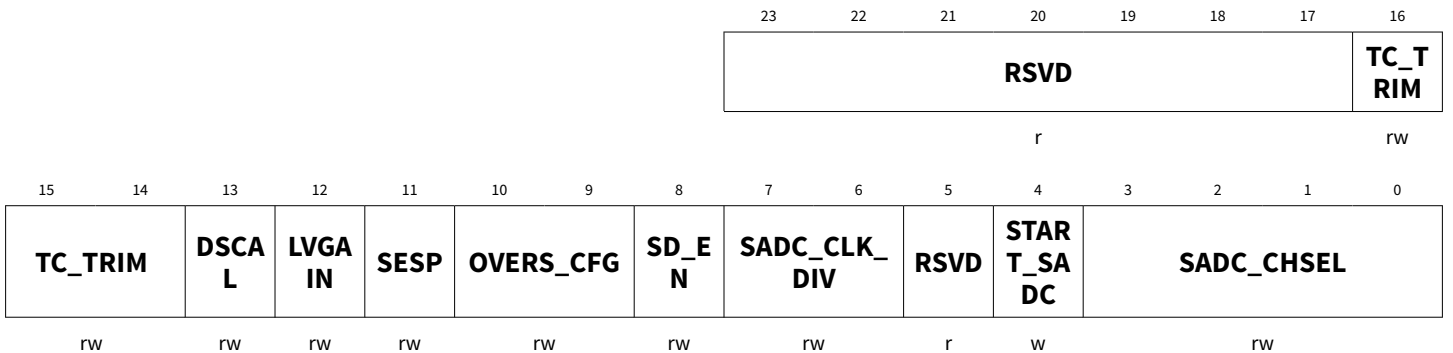
The bits in this register are used to configure the sensor ADC. The SADC is used to monitor the on chip sensor outputs, temperature and power, as well as some internal voltage nodes.

#### SADC\_CTRL

Sensor ADC control register

Offset address: 007<sub>H</sub>

Reset value: 00 00C0<sub>H</sub>



| Field        | Bits        | Type | Description  |
|--------------|-------------|------|--|
| SADC_CHSEL   | 3:0         | rw   | <b>Analog multiplexer input for channel selection to the SADC:</b><br>0 <sub>D</sub> ... Tsense (Temperature sensor)<br>1 <sub>D</sub> ... Reserved<br>2 <sub>D</sub> ... Tref (Temperature sensor reference)<br>3 <sub>D</sub> ... pd1_outx<br>4 <sub>D</sub> ... pd1_out<br>5 <sub>D</sub> ... ifx_mix4<br>6 <sub>D</sub> ... if_mix4<br>7 <sub>D</sub> ... ifx_mix3<br>8 <sub>D</sub> ... if_mix3<br>9 <sub>D</sub> ... ifx_mix2<br>10 <sub>D</sub> ... if_mix2<br>11 <sub>D</sub> ... ifx_mix1<br>12 <sub>D</sub> ... if_mix1<br>13 <sub>D</sub> ... pd2_outx<br>14 <sub>D</sub> ... pd2_out<br>15 <sub>D</sub> ... xosc_v |
| START_SADC   | 4           | w    | <b>Trigger for manual sensor ADC conversion:</b><br>0 <sub>B</sub> ... No effect<br>1 <sub>B</sub> ... Executes a single sensor ADC conversion and clears this bit   |
| RSVD         | 5,<br>23:17 | r    | <b>Reserved</b>  |
| SADC_CLK_DIV | 7:6         | rw   | <b>SADC clock divider provides the system clock for the sensor ADC. SADC clock frequency divider value. <math>f_{SADC\_CLK} = f_{SYS\_CLK} / SADC\_CLK\_DIV</math>:</b><br>0 <sub>D</sub> ... Divider value is 1<br>1 <sub>D</sub> ... Divider value is 2<br>2 <sub>D</sub> ... Divider value is 3<br>3 <sub>D</sub> ... Divider value is 4  |
| SD_EN        | 8           | rw   | <b>Enables sigma delta loop:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| OVERS_CFG    | 10:9        | rw   | <b>Oversampling configuration:</b><br>0 <sub>D</sub> ... No oversampling (8 bits resolution)<br>1 <sub>D</sub> ... Oversampling x2<br>2 <sub>D</sub> ... Oversampling x4 (9 bits resolution)<br>3 <sub>D</sub> ... Oversampling x32 (10 bits resolution)   |
| SESP         | 11          | rw   | <b>Spread early sampling point enable:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| LVGAIN       | 12          | rw   | <b>Sample configuration for LV channels:</b><br>0 <sub>B</sub> ... Gain = 1.0<br>1 <sub>B</sub> ... Gain = 0.75  |

(table continues...)

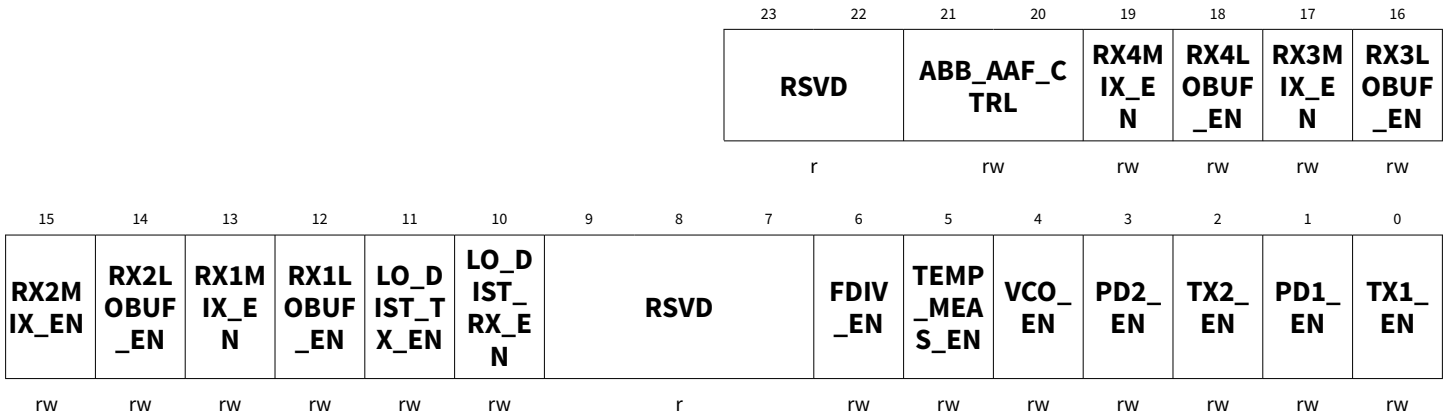
(continued)

| Field   | Bits  | Type | Description  |
|---------|-------|------|--|
| DSCAL   | 13    | rw   | <b>Disables startup calibration:</b><br>0 <sub>B</sub> ... Enabled<br>1 <sub>B</sub> ... Disabled                        |
| TC_TRIM | 16:14 | rw   | <b>Bandgap trimming value:</b><br>0 <sub>D</sub> ... Minimum trimming value<br>7 <sub>D</sub> ... Maximum trimming value |

## 4.11 Channel set idle register 0

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

**CSI\_0** Offset address: 008<sub>H</sub>  
 Channel set idle register 0 Reset value: 00 0000<sub>H</sub>



| Field  | Bits | Type | Description   |
|--------|------|------|---|
| TX1_EN | 0    | rw   | <b>Enables the DAC and power amplifier of TX1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| PD1_EN | 1    | rw   | <b>Enables the power detector of TX1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled          |
| TX2_EN | 2    | rw   | <b>Enables the DAC and power amplifier of TX2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| PD2_EN | 3    | rw   | <b>Enables the power detector of TX2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled          |
| VCO_EN | 4    | rw   | <b>Enables the VCO:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                            |

(table continues...)

(continued)

| Field         | Bits          | Type | Description  |
|---------------|---------------|------|--|
| TEMP_MEAS_EN  | 5             | rw   | <b>Enables the temperature sensor:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| FDIV_EN       | 6             | rw   | <b>Enables the VCO frequency divider:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: DIV output           |
| RSVD          | 9:7,<br>23:22 | r    | <b>Reserved</b>  |
| LO_DIST_RX_EN | 10            | rw   | <b>Enables the local oscillator distribution buffer to RX channels:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| LO_DIST_TX_EN | 11            | rw   | <b>Enables the local oscillator distribution buffer to TX channels:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| RX1LOBUF_EN   | 12            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX1MIX_EN     | 13            | rw   | <b>Enables the mixer on channel 1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| RX2LOBUF_EN   | 14            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX2MIX_EN     | 15            | rw   | <b>Enables the mixer on channel 2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| RX3LOBUF_EN   | 16            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 3:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX3MIX_EN     | 17            | rw   | <b>Enables the mixer on channel 3:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| RX4LOBUF_EN   | 18            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 4:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX4MIX_EN     | 19            | rw   | <b>Enables the mixer on channel 4:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |

(table continues...)

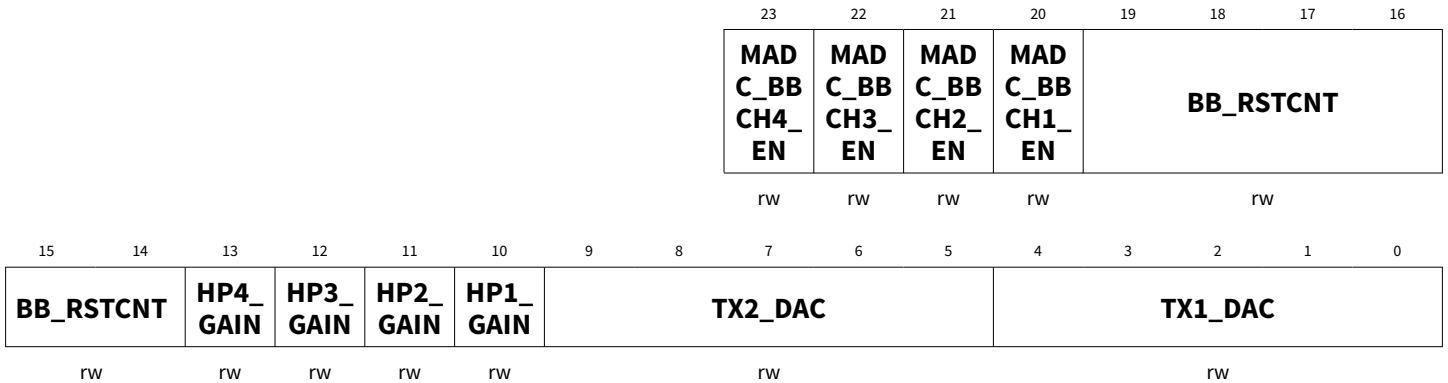
(continued)

| Field        | Bits  | Type | Description  |
|--------------|-------|------|--|
| ABB_AAF_CTRL | 21:20 | rw   | <b>Selection of analog base band anti-aliasing filter frequency of RX channels:</b><br>0 <sub>D</sub> ... 500 kHz<br>1 <sub>D</sub> ... 1000 kHz<br>2 <sub>D</sub> ... 1500 kHz<br>3 <sub>D</sub> ... 1800 kHz |

## 4.12 Channel set idle register 1

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

**CSI\_1** Offset address: 009<sub>H</sub>  
 Channel set idle register 1 Reset value: 00 0000<sub>H</sub>



| Field    | Bits | Type | Description  |
|----------|------|------|--|
| TX1_DAC  | 4:0  | rw   | <b>TX1 output power setting:</b><br>0 <sub>D</sub> ... Minimum output power<br>31 <sub>D</sub> ... Maximum output power              |
| TX2_DAC  | 9:5  | rw   | <b>TX2 output power setting:</b><br>0 <sub>D</sub> ... Minimum output power<br>31 <sub>D</sub> ... Maximum output power              |
| HP1_GAIN | 10   | rw   | <b>Gain setting of the first stage of the high pass filter of channel 1:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB |
| HP2_GAIN | 11   | rw   | <b>Gain setting of the first stage of the high pass filter of channel 2:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB |
| HP3_GAIN | 12   | rw   | <b>Gain setting of the first stage of the high pass filter of channel 3:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB |

(table continues...)

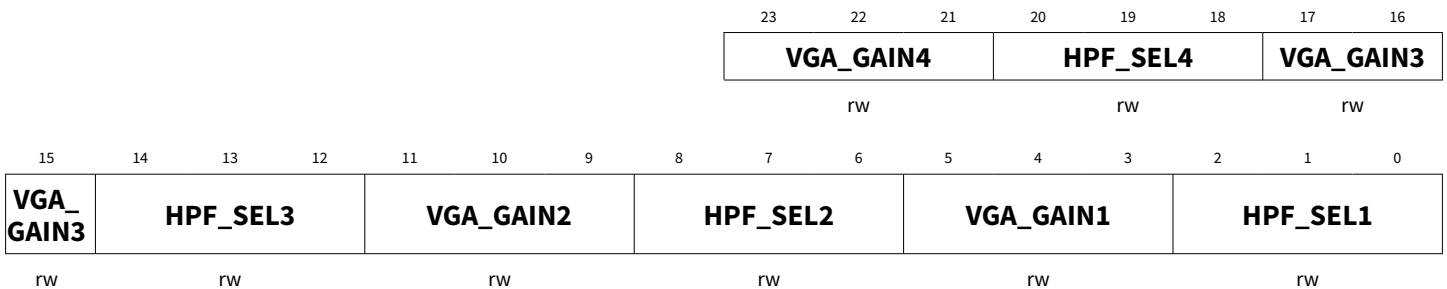
(continued)

| Field         | Bits  | Type | Description  |
|---------------|-------|------|--|
| HP4_GAIN      | 13    | rw   | <b>Gain setting of the first stage of the high pass filter of channel 4:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB   |
| BB_RSTCNT     | 19:14 | rw   | <b>Baseband reset timer counter value for the analog baseband amplifiers. The reset counter will start together with the PAON signal after the T_PAEN timer. <math>T_{BBRST} = BB\_RSTCNT * 8 * T_{SYS\_CLK}</math>:</b><br>0 <sub>D</sub> ... No analog baseband reset<br>1 <sub>D</sub> ... Minimum value<br>63 <sub>D</sub> ... Maximum value |
| MADC_BBCH1_EN | 20    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_BBCH2_EN | 21    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_BBCH3_EN | 22    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 3:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_BBCH4_EN | 23    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 4:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |

### 4.13 Channel set idle register 2

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

**CSI\_2** Offset address: 00A<sub>H</sub>  
Channel set idle register 2 Reset value: 00 0000<sub>H</sub>



| Field     | Bits | Type | Description  |
|-----------|------|------|--|
| HPF_SEL1  | 2:0  | rw   | <b>High pass filter cutoff frequency setting of channel 1:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |
| VGA_GAIN1 | 5:3  | rw   | <b>VGA gain setting of channel 1:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |
| HPF_SEL2  | 8:6  | rw   | <b>High pass filter cutoff frequency setting of channel 2:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |
| VGA_GAIN2 | 11:9 | rw   | <b>VGA gain setting of channel 2:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |

(table continues...)

(continued)

| Field     | Bits  | Type | Description  |
|-----------|-------|------|--|
| HPF_SEL3  | 14:12 | rw   | <b>High pass filter cutoff frequency setting of channel 3:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |
| VGA_GAIN3 | 17:15 | rw   | <b>VGA gain setting of channel 3:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |
| HPF_SEL4  | 20:18 | rw   | <b>High pass filter cutoff frequency setting of channel 4:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |
| VGA_GAIN4 | 23:21 | rw   | <b>VGA gain setting of channel 4:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |

## 4.14 Channel set control idle register

The channel set control register CSCI is related to the channel set register CSI.

All bits are used to define a specific power mode.

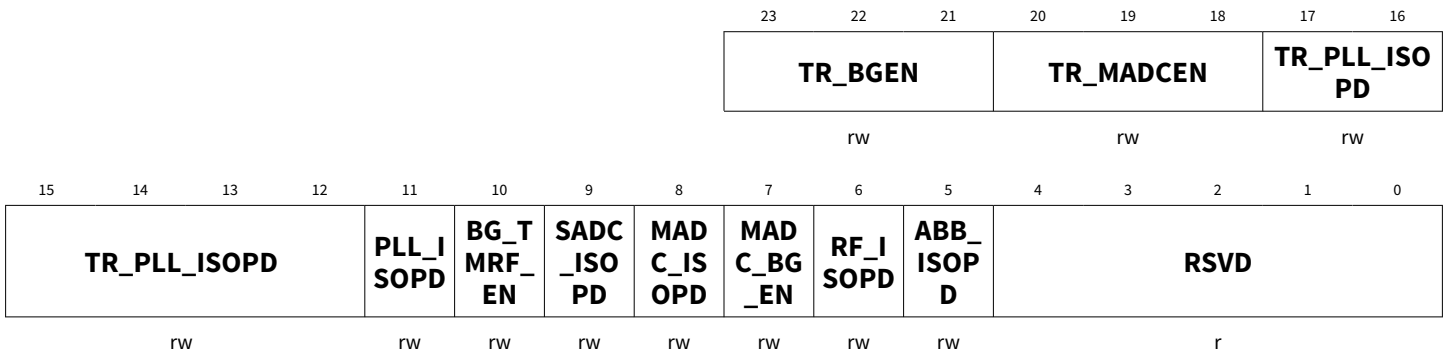
ISOPD represent a logical isolation layer and is used to disable complete modules (e.g. MADC) while preserving its configuration (no change in the ADC0 register configuration).

### CSCI

Channel set control idle register

Offset address: 00B<sub>H</sub>

Reset value: 24 0B60<sub>H</sub>



| Field      | Bits | Type | Description   |
|------------|------|------|---|
| RSVD       | 4:0  | r    | <b>Reserved</b>   |
| ABB_ISOPD  | 5    | rw   | <b>Enables the isolation of all control signals to the ABB:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: In case the isolation is enabled all control signals are connected to 0 <sub>B</sub> .  |
| RF_ISOPD   | 6    | rw   | <b>Enables the isolation of all control signals to the RF:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: In case the isolation is enabled all control signals are connected to 0 <sub>B</sub> .   |
| MADC_BG_EN | 7    | rw   | <b>Enables the bandgap of the MADC:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_ISOPD | 8    | rw   | <b>Enables the isolation of all control signals to the MADC:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: In case the isolation is enabled all control signals are connected to 0 <sub>B</sub> . |
| SADC_ISOPD | 9    | rw   | <b>Enables the isolation of all control signals to the SADC:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: In case the isolation is enabled all control signals are connected to 0 <sub>B</sub> . |
| BG_TMRF_EN | 10   | rw   | <b>Enables the temperature sensor:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |

**(table continues...)**



(continued)

| Field         | Bits          | Type | Description  |
|---------------|---------------|------|--|
| PD1_EN        | 1             | rw   | <b>Enables the power detector of TX1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                               |
| TX2_EN        | 2             | rw   | <b>Enables the DAC and power amplifier of TX2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                      |
| PD2_EN        | 3             | rw   | <b>Enables the power detector of TX2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                               |
| VCO_EN        | 4             | rw   | <b>Enables the VCO:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| TEMP_MEAS_EN  | 5             | rw   | <b>Enables the temperature sensor:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| FDIV_EN       | 6             | rw   | <b>Enables the VCO frequency divider:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: DIV output           |
| RSVD          | 9:7,<br>23:22 | r    | <b>Reserved</b>  |
| LO_DIST_RX_EN | 10            | rw   | <b>Enables the local oscillator distribution buffer to RX channels:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| LO_DIST_TX_EN | 11            | rw   | <b>Enables the local oscillator distribution buffer to TX channels:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| RX1LOBUF_EN   | 12            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX1MIX_EN     | 13            | rw   | <b>Enables the mixer on channel 1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| RX2LOBUF_EN   | 14            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX2MIX_EN     | 15            | rw   | <b>Enables the mixer on channel 2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |

(table continues...)

(continued)

| Field        | Bits  | Type | Description  |
|--------------|-------|------|--|
| RX3LOBUF_EN  | 16    | rw   | <b>Enables the local oscillator buffer to the mixer on channel 3:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX3MIX_EN    | 17    | rw   | <b>Enables the mixer on channel 3:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| RX4LOBUF_EN  | 18    | rw   | <b>Enables the local oscillator buffer to the mixer on channel 4:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX4MIX_EN    | 19    | rw   | <b>Enables the mixer on channel 4:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| ABB_AAF_CTRL | 21:20 | rw   | <b>Selection of analog base band anti-aliasing filter frequency of RX channels:</b><br>0 <sub>D</sub> ... 500 kHz<br>1 <sub>D</sub> ... 1000 kHz<br>2 <sub>D</sub> ... 1500 kHz<br>3 <sub>D</sub> ... 1800 kHz |

## 4.16 Channel set deep sleep register 1

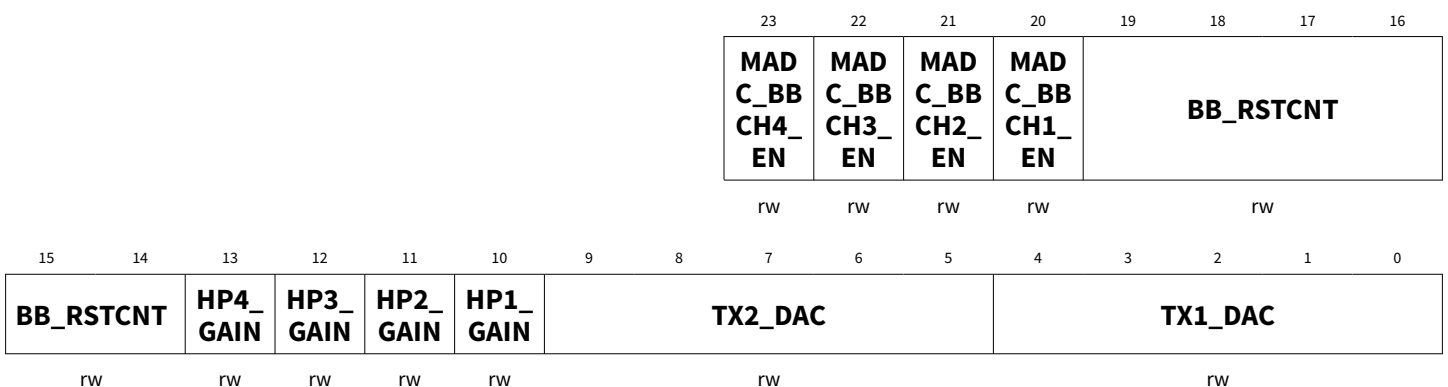
The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

### CSDS\_1

Offset address: 00D<sub>H</sub>

Channel set deep sleep register 1

Reset value: 00 0000<sub>H</sub>



| Field   | Bits | Type | Description   |
|---------|------|------|---|
| TX1_DAC | 4:0  | rw   | <b>TX1 output power setting:</b><br>0 <sub>D</sub> ... Minimum output power<br>31 <sub>D</sub> ... Maximum output power |

(table continues...)

(continued)

| Field         | Bits  | Type | Description  |
|---------------|-------|------|--|
| TX2_DAC       | 9:5   | rw   | <b>TX2 output power setting:</b><br>0 <sub>D</sub> ... Minimum output power<br>31 <sub>D</sub> ... Maximum output power  |
| HP1_GAIN      | 10    | rw   | <b>Gain setting of the first stage of the high pass filter of channel 1:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB   |
| HP2_GAIN      | 11    | rw   | <b>Gain setting of the first stage of the high pass filter of channel 2:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB   |
| HP3_GAIN      | 12    | rw   | <b>Gain setting of the first stage of the high pass filter of channel 3:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB   |
| HP4_GAIN      | 13    | rw   | <b>Gain setting of the first stage of the high pass filter of channel 4:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB   |
| BB_RSTCNT     | 19:14 | rw   | <b>Baseband reset timer counter value for the analog baseband amplifiers. The reset counter will start together with the PAON signal after the T_PAEN timer. <math>T_{BBRST} = BB\_RSTCNT * 8 * T_{SYS\_CLK}</math>:</b><br>0 <sub>D</sub> ... No analog baseband reset<br>1 <sub>D</sub> ... Minimum value<br>63 <sub>D</sub> ... Maximum value |
| MADC_BBCH1_EN | 20    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_BBCH2_EN | 21    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_BBCH3_EN | 22    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 3:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_BBCH4_EN | 23    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 4:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |

## 4.17 Channel set deep sleep register 2

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

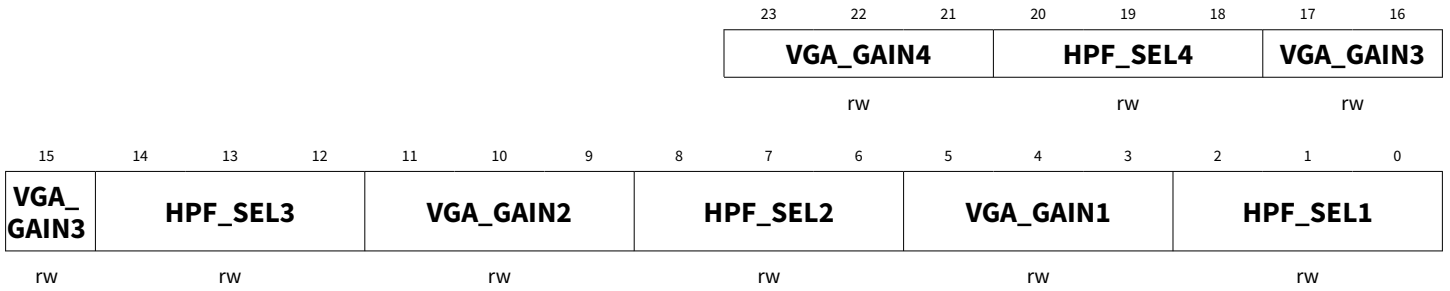
### CSDS\_2

Channel set deep sleep register 2

Offset address: 00E<sub>H</sub>

Reset value: 00 0000<sub>H</sub>

4 BGT60ATR24AIP registers



| Field     | Bits | Type | Description  |
|-----------|------|------|--|
| HPF_SEL1  | 2:0  | rw   | <b>High pass filter cutoff frequency setting of channel 1:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |
| VGA_GAIN1 | 5:3  | rw   | <b>VGA gain setting of channel 1:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |
| HPF_SEL2  | 8:6  | rw   | <b>High pass filter cutoff frequency setting of channel 2:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |

(table continues...)

(continued)

| Field     | Bits  | Type | Description  |
|-----------|-------|------|--|
| VGA_GAIN2 | 11:9  | rw   | <b>VGA gain setting of channel 2:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |
| HPF_SEL3  | 14:12 | rw   | <b>High pass filter cutoff frequency setting of channel 3:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |
| VGA_GAIN3 | 17:15 | rw   | <b>VGA gain setting of channel 3:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |
| HPF_SEL4  | 20:18 | rw   | <b>High pass filter cutoff frequency setting of channel 4:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |

(table continues...)

(continued)

| Field     | Bits  | Type | Description  |
|-----------|-------|------|--|
| VGA_GAIN4 | 23:21 | rw   | <b>VGA gain setting of channel 4:</b><br>$0_D$ ... 0 dB<br>$1_D$ ... 5 dB<br>$2_D$ ... 10 dB<br>$3_D$ ... 15 dB<br>$4_D$ ... 20 dB<br>$5_D$ ... 25 dB<br>$6_D$ ... 30 dB<br>$7_D$ ... Reserved |

### 4.18 Channel set control deep sleep register

The channel set control register CSCDS is related to the channel set register CSDS.

All bits are used to define a specific power mode.

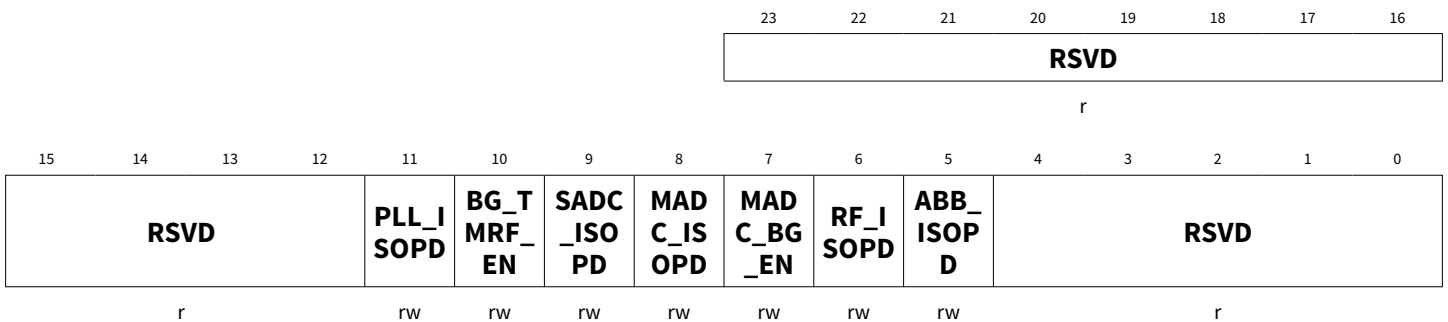
ISOPD represent a logical isolation layer and is used to disable complete modules (e.g. MADC) while preserving its configuration (no change in the ADC0 register configuration).

#### CSCDS

Offset address: 00F<sub>H</sub>

Channel set control deep sleep register

Reset value: 00 0B60<sub>H</sub>



| Field      | Bits          | Type | Description   |
|------------|---------------|------|---|
| RSVD       | 4:0,<br>23:12 | r    | <b>Reserved</b>   |
| ABB_ISOPD  | 5             | rw   | <b>Enables the isolation of all control signals to the ABB:</b><br>$0_B$ ... Disabled<br>$1_B$ ... Enabled<br>Note: In case the isolation is enabled all control signals are connected to $0_B$ . |
| RF_ISOPD   | 6             | rw   | <b>Enables the isolation of all control signals to the RF:</b><br>$0_B$ ... Disabled<br>$1_B$ ... Enabled<br>Note: In case the isolation is enabled all control signals are connected to $0_B$ .  |
| MADC_BG_EN | 7             | rw   | <b>Enables the bandgap of the MADC:</b><br>$0_B$ ... Disabled<br>$1_B$ ... Enabled  |

(table continues...)

(continued)

| Field      | Bits | Type | Description   |
|------------|------|------|---|
| MADC_ISOPD | 8    | rw   | <b>Enables the isolation of all control signals to the MADC:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: In case the isolation is enabled all control signals are connected to 0 <sub>B</sub> . |
| SADC_ISOPD | 9    | rw   | <b>Enables the isolation of all control signals to the SADC:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: In case the isolation is enabled all control signals are connected to 0 <sub>B</sub> . |
| BG_TMRF_EN | 10   | rw   | <b>Enables the temperature sensor:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| PLL_ISOPD  | 11   | rw   | <b>Enables the isolation of all control signals to the PLL:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: In case the isolation is enabled all control signals are connected to 0 <sub>B</sub> .  |

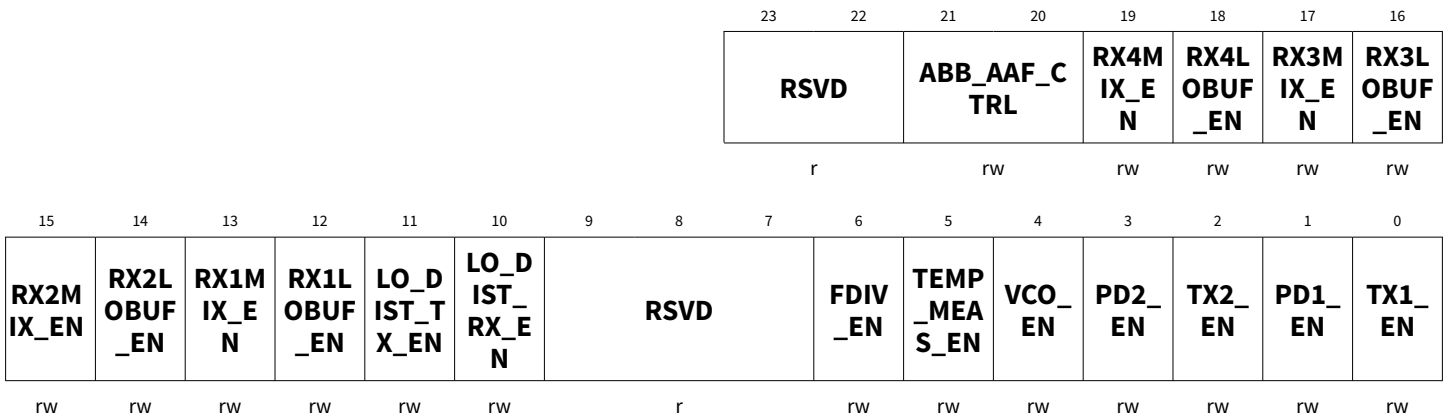
#### 4.19 Channel set up x register 0

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

**CSU\_0 (x=1-4)**

Offset address: 010<sub>H</sub>+(x-1)\*7

Reset value: 00 0000<sub>H</sub>



| Field  | Bits | Type | Description   |
|--------|------|------|---|
| TX1_EN | 0    | rw   | <b>Enables the DAC and power amplifier of TX1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| PD1_EN | 1    | rw   | <b>Enables the power detector of TX1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled          |

(table continues...)

(continued)

| Field         | Bits          | Type | Description  |
|---------------|---------------|------|--|
| TX2_EN        | 2             | rw   | <b>Enables the DAC and power amplifier of TX2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                      |
| PD2_EN        | 3             | rw   | <b>Enables the power detector of TX2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                               |
| VCO_EN        | 4             | rw   | <b>Enables the VCO:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| TEMP_MEAS_EN  | 5             | rw   | <b>Enables the temperature sensor:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| FDIV_EN       | 6             | rw   | <b>Enables the VCO frequency divider:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: DIV output           |
| RSVD          | 9:7,<br>23:22 | r    | <b>Reserved</b>  |
| LO_DIST_RX_EN | 10            | rw   | <b>Enables the local oscillator distribution buffer to RX channels:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| LO_DIST_TX_EN | 11            | rw   | <b>Enables the local oscillator distribution buffer to TX channels:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| RX1LOBUF_EN   | 12            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX1MIX_EN     | 13            | rw   | <b>Enables the mixer on channel 1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| RX2LOBUF_EN   | 14            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX2MIX_EN     | 15            | rw   | <b>Enables the mixer on channel 2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| RX3LOBUF_EN   | 16            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 3:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |

(table continues...)

(continued)

| Field        | Bits  | Type | Description  |
|--------------|-------|------|--|
| RX3MIX_EN    | 17    | rw   | <b>Enables the mixer on channel 3:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| RX4LOBUF_EN  | 18    | rw   | <b>Enables the local oscillator buffer to the mixer on channel 4:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX4MIX_EN    | 19    | rw   | <b>Enables the mixer on channel 4:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| ABB_AAF_CTRL | 21:20 | rw   | <b>Selection of analog base band anti-aliasing filter frequency of RX channels:</b><br>0 <sub>D</sub> ... 500 kHz<br>1 <sub>D</sub> ... 1000 kHz<br>2 <sub>D</sub> ... 1500 kHz<br>3 <sub>D</sub> ... 1800 kHz |

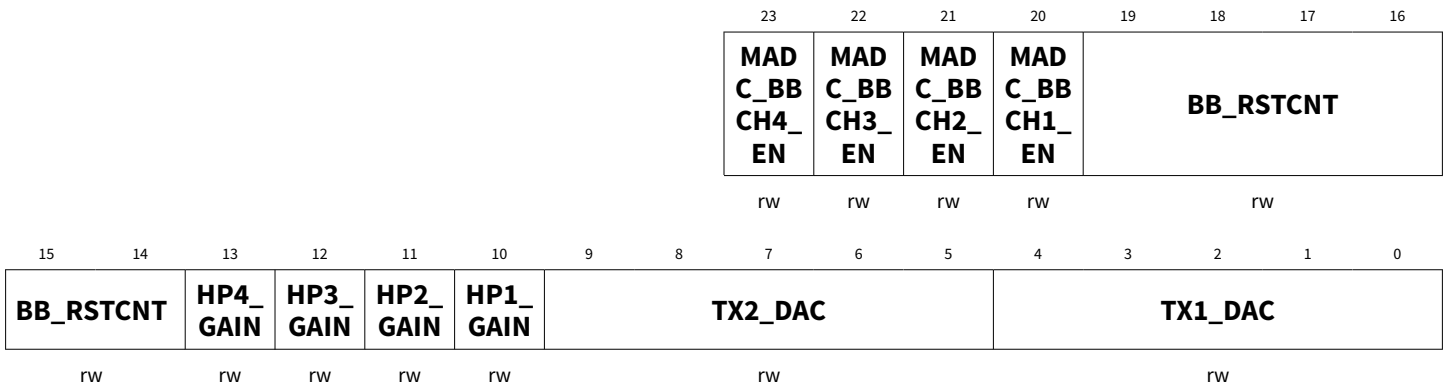
## 4.20 Channel set up x register 1

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

**CSU\_1 (x=1-4)**

Offset address: 011<sub>H</sub>+(x-1)\*7

Reset value: 00 0000<sub>H</sub>



| Field   | Bits | Type | Description   |
|---------|------|------|---|
| TX1_DAC | 4:0  | rw   | <b>TX1 output power setting:</b><br>0 <sub>D</sub> ... Minimum output power<br>31 <sub>D</sub> ... Maximum output power |
| TX2_DAC | 9:5  | rw   | <b>TX2 output power setting:</b><br>0 <sub>D</sub> ... Minimum output power<br>31 <sub>D</sub> ... Maximum output power |

(table continues...)

(continued)

| Field         | Bits  | Type | Description  |
|---------------|-------|------|--|
| HP1_GAIN      | 10    | rw   | <b>Gain setting of the first stage of the high pass filter of channel 1:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB   |
| HP2_GAIN      | 11    | rw   | <b>Gain setting of the first stage of the high pass filter of channel 2:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB   |
| HP3_GAIN      | 12    | rw   | <b>Gain setting of the first stage of the high pass filter of channel 3:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB   |
| HP4_GAIN      | 13    | rw   | <b>Gain setting of the first stage of the high pass filter of channel 4:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB   |
| BB_RSTCNT     | 19:14 | rw   | <b>Baseband reset timer counter value for the analog baseband amplifiers. The reset counter will start together with the PAON signal after the T_PAEN timer. <math>T_{BBRST} = BB\_RSTCNT * 8 * T_{SYS\_CLK}</math>:</b><br>0 <sub>D</sub> ... No analog baseband reset<br>1 <sub>D</sub> ... Minimum value<br>63 <sub>D</sub> ... Maximum value |
| MADC_BBCH1_EN | 20    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_BBCH2_EN | 21    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_BBCH3_EN | 22    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 3:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_BBCH4_EN | 23    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 4:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |

## 4.21 Channel set up x register 2

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

**CSU\_2 (x=1-4)**

Offset address: 012<sub>H</sub>+(x-1)\*7

Reset value: 00 0000<sub>H</sub>



(continued)

| Field     | Bits  | Type | Description  |
|-----------|-------|------|--|
| VGA_GAIN2 | 11:9  | rw   | <b>VGA gain setting of channel 2:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |
| HPF_SEL3  | 14:12 | rw   | <b>High pass filter cutoff frequency setting of channel 3:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |
| VGA_GAIN3 | 17:15 | rw   | <b>VGA gain setting of channel 3:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |
| HPF_SEL4  | 20:18 | rw   | <b>High pass filter cutoff frequency setting of channel 4:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |

(table continues...)

(continued)

| Field     | Bits  | Type | Description  |
|-----------|-------|------|--|
| VGA_GAIN4 | 23:21 | rw   | <b>VGA gain setting of channel 4:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved |

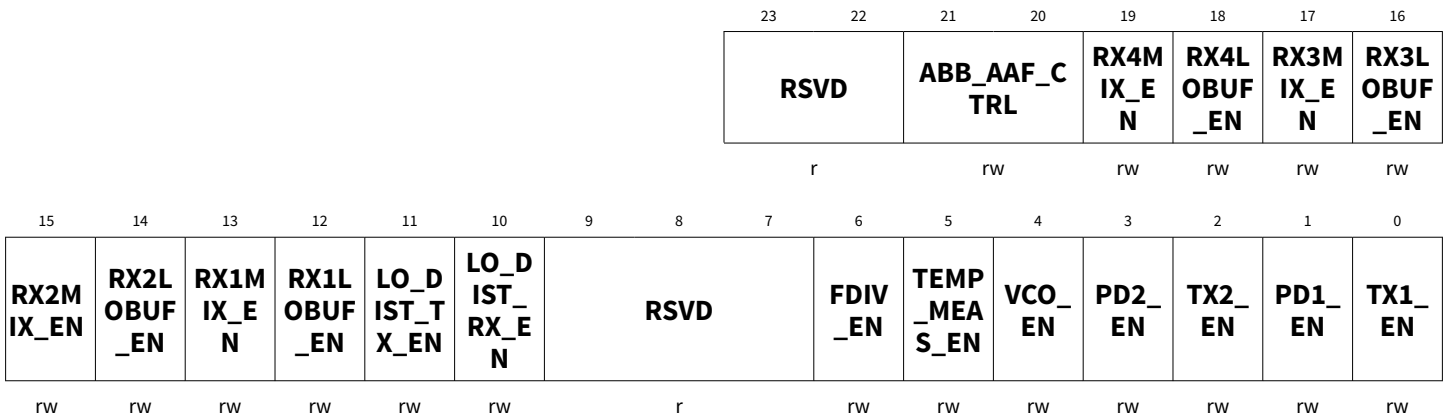
## 4.22 Channel set down x register 0

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

**CSD\_0 (x=1-4)**

Offset address: 013<sub>H</sub>+(x-1)\*7

Reset value: 00 0000<sub>H</sub>



| Field  | Bits | Type | Description   |
|--------|------|------|---|
| TX1_EN | 0    | rw   | <b>Enables the DAC and power amplifier of TX1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| PD1_EN | 1    | rw   | <b>Enables the power detector of TX1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled          |
| TX2_EN | 2    | rw   | <b>Enables the DAC and power amplifier of TX2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| PD2_EN | 3    | rw   | <b>Enables the power detector of TX2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled          |

(table continues...)

(continued)

| Field         | Bits          | Type | Description  |
|---------------|---------------|------|--|
| VCO_EN        | 4             | rw   | <b>Enables the VCO:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| TEMP_MEAS_EN  | 5             | rw   | <b>Enables the temperature sensor:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| FDIV_EN       | 6             | rw   | <b>Enables the VCO frequency divider:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: DIV output           |
| RSVD          | 9:7,<br>23:22 | r    | <b>Reserved</b>  |
| LO_DIST_RX_EN | 10            | rw   | <b>Enables the local oscillator distribution buffer to RX channels:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| LO_DIST_TX_EN | 11            | rw   | <b>Enables the local oscillator distribution buffer to TX channels:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled |
| RX1LOBUF_EN   | 12            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX1MIX_EN     | 13            | rw   | <b>Enables the mixer on channel 1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| RX2LOBUF_EN   | 14            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX2MIX_EN     | 15            | rw   | <b>Enables the mixer on channel 2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| RX3LOBUF_EN   | 16            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 3:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| RX3MIX_EN     | 17            | rw   | <b>Enables the mixer on channel 3:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                                  |
| RX4LOBUF_EN   | 18            | rw   | <b>Enables the local oscillator buffer to the mixer on channel 4:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |

(table continues...)

(continued)

| Field        | Bits  | Type | Description  |
|--------------|-------|------|--|
| RX4MIX_EN    | 19    | rw   | <b>Enables the mixer on channel 4:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| ABB_AAF_CTRL | 21:20 | rw   | <b>Selection of analog base band anti-aliasing filter frequency of RX channels:</b><br>0 <sub>D</sub> ... 500 kHz<br>1 <sub>D</sub> ... 1000 kHz<br>2 <sub>D</sub> ... 1500 kHz<br>3 <sub>D</sub> ... 1800 kHz |

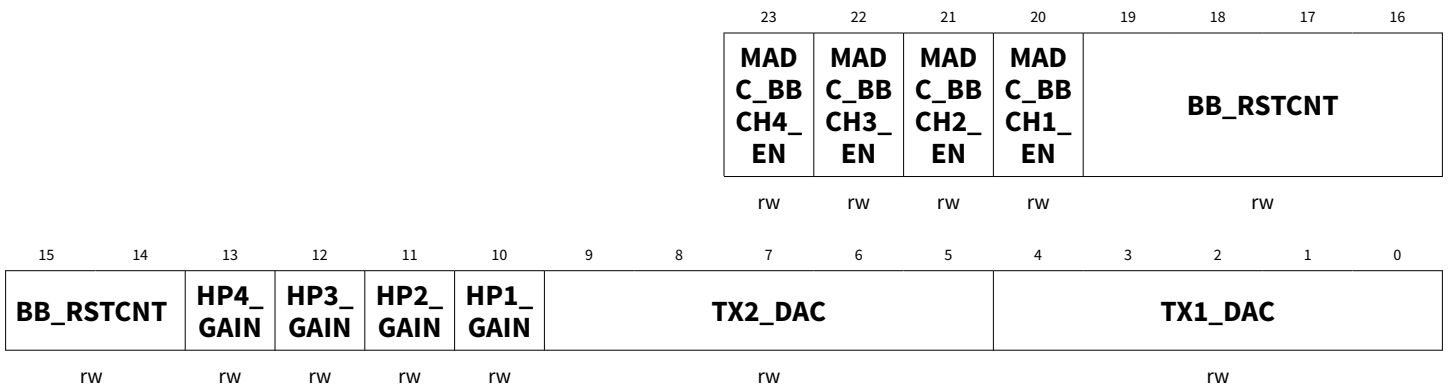
### 4.23 Channel set down x register 1

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

**CSD\_1 (x=1-4)**

Offset address: 014<sub>H</sub>+(x-1)\*7

Reset value: 00 0000<sub>H</sub>



| Field    | Bits | Type | Description  |
|----------|------|------|--|
| TX1_DAC  | 4:0  | rw   | <b>TX1 output power setting:</b><br>0 <sub>D</sub> ... Minimum output power<br>31 <sub>D</sub> ... Maximum output power              |
| TX2_DAC  | 9:5  | rw   | <b>TX2 output power setting:</b><br>0 <sub>D</sub> ... Minimum output power<br>31 <sub>D</sub> ... Maximum output power              |
| HP1_GAIN | 10   | rw   | <b>Gain setting of the first stage of the high pass filter of channel 1:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB |
| HP2_GAIN | 11   | rw   | <b>Gain setting of the first stage of the high pass filter of channel 2:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB |

(table continues...)

(continued)

| Field         | Bits  | Type | Description  |
|---------------|-------|------|--|
| HP3_GAIN      | 12    | rw   | <b>Gain setting of the first stage of the high pass filter of channel 3:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB   |
| HP4_GAIN      | 13    | rw   | <b>Gain setting of the first stage of the high pass filter of channel 4:</b><br>0 <sub>B</sub> ... 30 dB<br>1 <sub>B</sub> ... 18 dB   |
| BB_RSTCNT     | 19:14 | rw   | <b>Baseband reset timer counter value for the analog baseband amplifiers. The reset counter will start together with the PAON signal after the T_PAEN timer. <math>T_{BBRST} = BB\_RSTCNT * 8 * T_{SYS\_CLK}</math>:</b><br>0 <sub>D</sub> ... No analog baseband reset<br>1 <sub>D</sub> ... Minimum value<br>63 <sub>D</sub> ... Maximum value |
| MADC_BBCH1_EN | 20    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 1:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_BBCH2_EN | 21    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 2:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_BBCH3_EN | 22    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 3:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| MADC_BBCH4_EN | 23    | rw   | <b>Enables the baseband filters, baseband amplifiers and ADC on channel 4:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |

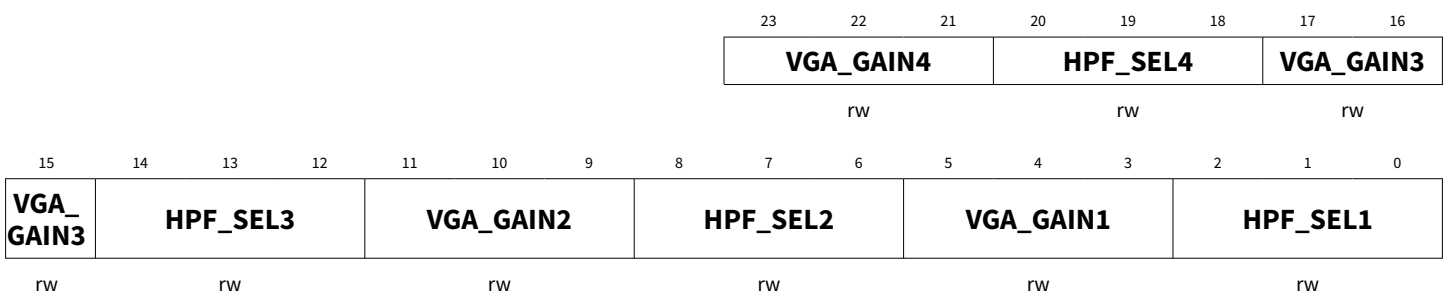
## 4.24 Channel set down x register 2

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes.

**CSD\_2 (x=1-4)**

Offset address: 015<sub>H</sub>+(x-1)\*7

Reset value: 00 0000<sub>H</sub>



| Field     | Bits | Type | Description  |
|-----------|------|------|--|
| HPF_SEL1  | 2:0  | rw   | <b>High pass filter cutoff frequency setting of channel 1:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |
| VGA_GAIN1 | 5:3  | rw   | <b>VGA gain setting of channel 1:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |
| HPF_SEL2  | 8:6  | rw   | <b>High pass filter cutoff frequency setting of channel 2:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |
| VGA_GAIN2 | 11:9 | rw   | <b>VGA gain setting of channel 2:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |

(table continues...)

(continued)

| Field     | Bits  | Type | Description  |
|-----------|-------|------|--|
| HPF_SEL3  | 14:12 | rw   | <b>High pass filter cutoff frequency setting of channel 3:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |
| VGA_GAIN3 | 17:15 | rw   | <b>VGA gain setting of channel 3:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |
| HPF_SEL4  | 20:18 | rw   | <b>High pass filter cutoff frequency setting of channel 4:</b><br>0 <sub>D</sub> ... 20 kHz<br>1 <sub>D</sub> ... 40 kHz<br>2 <sub>D</sub> ... 100 kHz<br>3 <sub>D</sub> ... 160 kHz<br>4 <sub>D</sub> ... 200 kHz<br>5 <sub>D</sub> ... 800 kHz<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |
| VGA_GAIN4 | 23:21 | rw   | <b>VGA gain setting of channel 4:</b><br>0 <sub>D</sub> ... 0 dB<br>1 <sub>D</sub> ... 5 dB<br>2 <sub>D</sub> ... 10 dB<br>3 <sub>D</sub> ... 15 dB<br>4 <sub>D</sub> ... 20 dB<br>5 <sub>D</sub> ... 25 dB<br>6 <sub>D</sub> ... 30 dB<br>7 <sub>D</sub> ... Reserved   |

## 4.25 Channel set control x register

The channel set control register CSCx is related to the channel set register CSUx.

Besides REPC, all other bits are used to define a specific power mode.

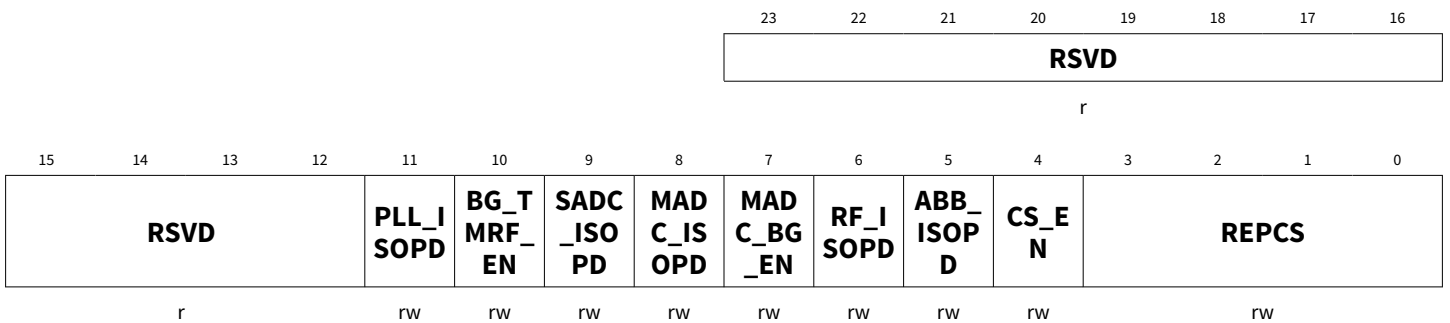
ISOPD represent a logical isolation layer and is used to disable complete modules (e.g. MADC) while preserving its configuration (no change in the ADC0 register configuration).

REPC is one parameter used to define the modulation sequence.

### CSC (x=1-4)

Offset address:  $016_H + (x-1) * 7$

Reset value:  $00\ 0B60_H$



| Field      | Bits | Type | Description  |
|------------|------|------|--|
| REPCS      | 3:0  | rw   | <b>Repetition factor of channel set:</b><br>$0_D..15_D \dots RC = 2^{REPC}$  |
| CS_EN      | 4    | rw   | <b>Enables channel set (CS):</b><br>$0_B \dots$ Disabled<br>$1_B \dots$ Enabled<br>Note: At least the first channel set should be used (CSC1:CS_EN = $1_B$ ).  |
| ABB_ISOPD  | 5    | rw   | <b>Enables the isolation of all control signals to the ABB:</b><br>$0_B \dots$ Disabled<br>$1_B \dots$ Enabled<br>Note: In case the isolation is enabled all control signals are connected to $0_B$ .  |
| RF_ISOPD   | 6    | rw   | <b>Enables the isolation of all control signals to the RF:</b><br>$0_B \dots$ Disabled<br>$1_B \dots$ Enabled<br>Note: In case the isolation is enabled all control signals are connected to $0_B$ .   |
| MADC_BG_EN | 7    | rw   | <b>Enables the bandgap of the MADC:</b><br>$0_B \dots$ Disabled<br>$1_B \dots$ Enabled   |
| MADC_ISOPD | 8    | rw   | <b>Enables the isolation of all control signals to the MADC:</b><br>$0_B \dots$ Disabled<br>$1_B \dots$ Enabled<br>Note: In case the isolation is enabled all control signals are connected to $0_B$ . |

(table continues...)

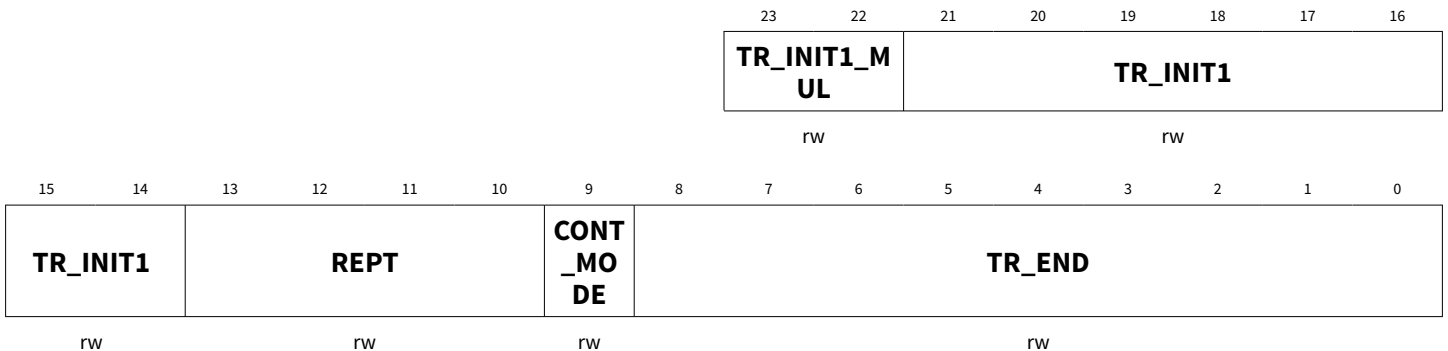
(continued)

| Field      | Bits  | Type | Description   |
|------------|-------|------|---|
| SADC_ISOPD | 9     | rw   | <b>Enables the isolation of all control signals to the SADC:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: In case the isolation is enabled all control signals are connected to 0 <sub>B</sub> . |
| BG_TMRF_EN | 10    | rw   | <b>Enables the temperature sensor:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| PLL_ISOPD  | 11    | rw   | <b>Enables the isolation of all control signals to the PLL:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: In case the isolation is enabled all control signals are connected to 0 <sub>B</sub> .  |
| RSVD       | 23:12 | r    | <b>Reserved</b>   |

## 4.26 Chirp control register 0

Register CCR0 is used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counters to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

**CCR0** Offset address: 02C<sub>H</sub>  
Chirp control register 0 Reset value: 00 0000<sub>H</sub>



| Field     | Bits | Type | Description   |
|-----------|------|------|---|
| TR_END    | 8:0  | rw   | <b>Timer for T_END. Waiting time after the generation of a ramp:</b><br>0 <sub>D</sub> ... T_END = 5 * T <sub>sys_clk</sub><br>1 <sub>D</sub> ..511 <sub>D</sub> ... T_END = (TR_END * 8 + 5) * T <sub>sys_clk</sub>  |
| CONT_MODE | 9    | rw   | <b>Continuous mode. After last channel set repetition RT, the specified power mode (CCR1:PD_MODE) is applied and</b><br>0 <sub>B</sub> ... the FSM stops immediately<br>1 <sub>B</sub> ... after T_FED the next channel set is applied<br>Note: In case DS power mode (CCR1:PD_MODE = 2 <sub>D</sub> ) is selected and the continuous mode is not active the system clock is disabled internally. |

(table continues...)

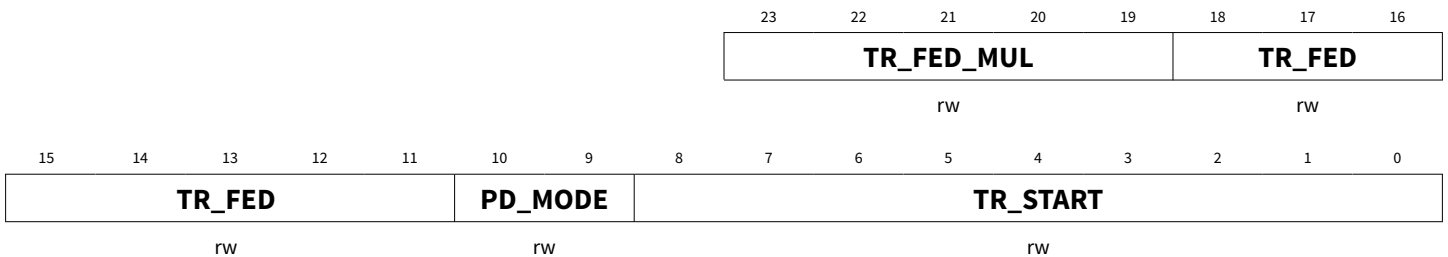
(continued)

| Field        | Bits  | Type | Description   |
|--------------|-------|------|---|
| REPT         | 13:10 | rw   | <b>Repetition factor for a channel set in a frame:</b><br>$0_D..15_D \dots RT = 2^{REPT}$<br><b>Note:</b> The host should program the maximum value $15_D$ as default.  |
| TR_INIT1     | 21:14 | rw   | <b>Timer for T_INIT1:</b><br>$0_D \dots T_{SYS\_CLK}$<br>$1_D..255_D \dots T\_INIT1 = (TR\_INIT1 * 2^{TR\_INIT\_MUL} * 8 + TR\_INIT\_MUL + 3) * T_{SYS\_CLK}$<br>Note: These values are used for every up and every down-ramp.<br>Note: After the wake-up period the timer for T_INIT1 should be at least 15 $\mu$ s according to the typical ADC calibration time. |
| TR_INIT1_MUL | 23:22 | rw   | <b>Timer multiplier factor for T_INIT1:</b><br>$0_D..3_D \dots 2^{TR\_INIT1\_MUL}$  |

## 4.27 Chirp control register 1

Register CCR1 is used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counters to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

**CCR1** Offset address: 02D<sub>H</sub>  
Chirp control register 1 Reset value: 00 0000<sub>H</sub>

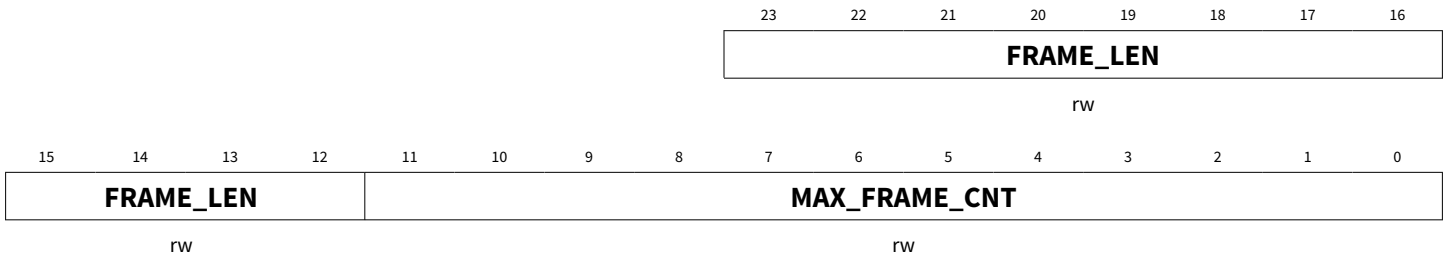


| Field      | Bits  | Type | Description   |
|------------|-------|------|---|
| TR_START   | 8:0   | rw   | <b>Timer for T_START. Ramp start delay defines the delay before generating the ramp:</b><br>$0_D..511_D \dots T\_START = (TR\_START * 8 + 10) * T_{SYS\_CLK}$   |
| PD_MODE    | 10:9  | rw   | <b>Power down mode. After the last repetition RT, the chip enters the defined power mode (during T_FED):</b><br>$0_D \dots$ Keep the same power mode (CSx + CSCx)<br>$1_D \dots$ Change to IDLE power mode (CSI + CSCi)<br>$2_D \dots$ Change to DS power mode (CSDS + CSCDS)<br>$3_D \dots$ Reserved |
| TR_FED     | 18:11 | rw   | <b>Timer for T_FED:</b><br>$0_D \dots T_{SYS\_CLK}$<br>$1_D..255_D \dots T\_FED = (TR\_FED * 2^{TR\_FED\_MUL} * 8 + TR\_FED\_MUL + 3) * T_{SYS\_CLK}$   |
| TR_FED_MUL | 23:19 | rw   | <b>Timer multiplier factor for T_FED:</b><br>$0_D..31_D \dots 2^{TR\_FED\_MUL}$   |

## 4.28 Chirp control register 2

Register CCR2 is used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counters to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

**CCR2** Offset address: 02E<sub>H</sub>  
 Chirp control register 2 Reset value: 00 0000<sub>H</sub>

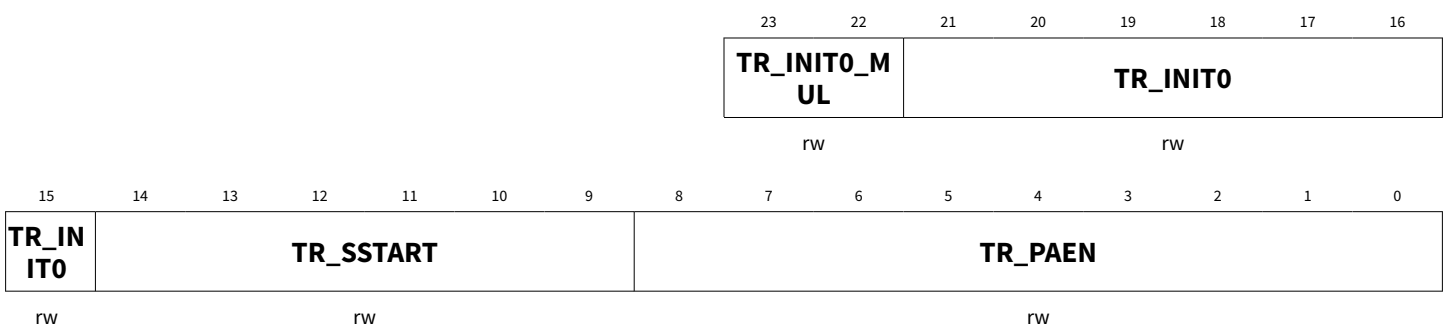


| Field         | Bits  | Type | Description   |
|---------------|-------|------|---|
| MAX_FRAME_CNT | 11:0  | rw   | <p><b>Maximum number of frames to be executed. When MAX_FRAME_CNT is reached, the shape generation is stopped, and the chip is set to deep sleep power mode. The next frame can be triggered only after a reset (eg. FSM_RESET). The frame generation can be stopped at any time by resetting the FSM (see MAIN:FSM_RESET).</b></p> <p>0<sub>D</sub> ... Endless frame generation<br/>                     1<sub>D</sub> ... 1 frame is generated<br/>                     4095<sub>D</sub> ... 4095 frames are generated</p> |
| FRAME_LEN     | 23:12 | rw   | <p><b>Frame Length specifies the number of shape groups in a frame. When specified frame length is reached the frame counter is incremented and the shape group counter is reset:</b></p> <p>0<sub>D</sub> ... Minimum value (1 shape group)<br/>                     4095<sub>D</sub> ... Maximum value (4096 shape groups)</p>  |

## 4.29 Chirp control register 3

Register CCR3 is used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counters to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

**CCR3** Offset address: 02F<sub>H</sub>  
 Chirp control register 3 Reset value: 00 0000<sub>H</sub>



| Field        | Bits  | Type | Description  |
|--------------|-------|------|--|
| TR_PAEN      | 8:0   | rw   | <b>Timer for T_PAEN. Delay time after PLL start and power amplifier enable:</b><br>$0_D \dots$ Reserved<br>$1_D..511_D \dots T\_PAEN = TR\_PAEN * 8 * T_{SYS\_CLK}$  |
| TR_SSTART    | 14:9  | rw   | <b>Timer for T_SSTART. Delay time after power amplifier enable and first trigger to ADC:</b><br>$0_D..63_D \dots T\_SSTART = (TR\_SSTART * 8 + 1) * T_{SYS\_CLK}$  |
| TR_INIT0     | 21:15 | rw   | <b>Timer for T_INIT0:</b><br>$0_D \dots T_{SYS\_CLK}$<br>$1_D..128_D \dots T\_INIT0 = (TR\_INIT0 * 2^{TR\_INIT0\_MUL} * 8 + TR\_INIT0\_MUL + 3) * T_{SYS\_CLK}$<br>Note: After the wake-up period the timer for T_INIT0 should be at least 70 $\mu$ s according to the typical ADC calibration time. |
| TR_INIT0_MUL | 23:22 | rw   | <b>Timer multiplier for T_INIT0:</b><br>$0_D..3_D \dots 2^{TR\_INIT0\_MUL}$  |

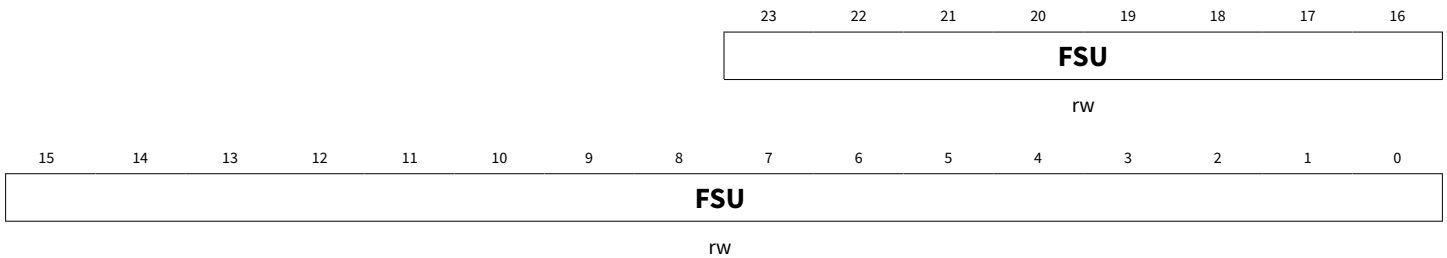
### 4.30 PLL shape x register 0

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

**PLL\_0 (x=1-4)**

Offset address:  $030_H + (x-1) * 8$

Reset value:  $00\ 0000_H$



| Field | Bits | Type | Description   |
|-------|------|------|---|
| FSU   | 23:0 | rw   | <b>Chirp start frequency for up chirp. Sigma delta start frequency for the ramp generator:</b><br>$0_D \dots$ Sawtooth shape<br>Note: In case FSD = $0_D$ , RSD = $0_D$ , and RTD = $0_D$ , the fast sawtooth shape is enabled. In all other cases the triangular shape is enabled. |

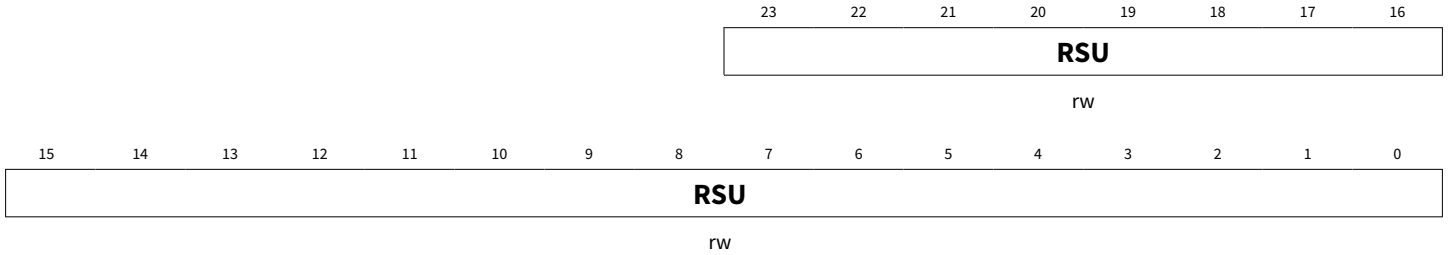
### 4.31 PLL shape x register 1

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

**PLL\_1 (x=1-4)**

Offset address:  $031_H + (x-1) * 8$

Reset value:  $00\ 0000_H$



| Field | Bits | Type | Description  |
|-------|------|------|--|
| RSU   | 23:0 | rw   | <p><b>Ramp step up chirp. A ramp step is the RF frequency difference added to the actual frequency during single clock cycle time of <math>T_{SYS\_CLK}</math>. In case the value is zero the RF frequency will be almost constant during the RTU time.</b></p> <p>Bit(23) represents the sign for the ramp:<br/> <math>0_D</math> ... Up chirp<br/> <math>1_D</math> ... Down chirp</p> |

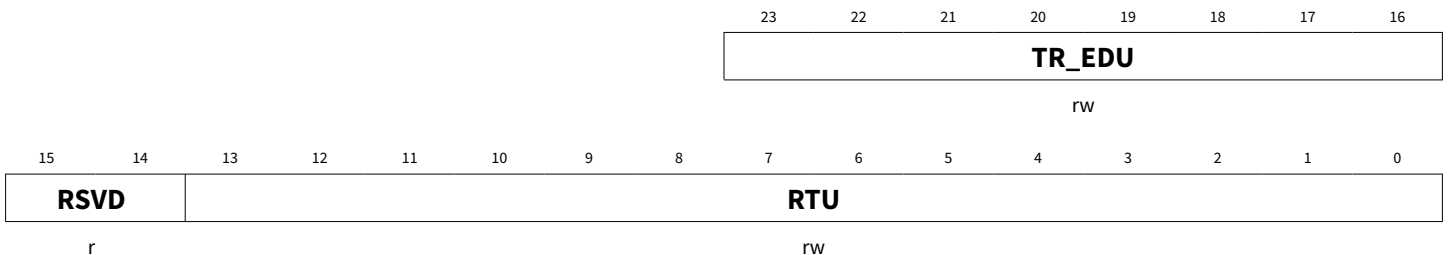
### 4.32 PLL shape x register 2

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

**PLL\_2 (x=1-4)**

Offset address:  $032_H + (x-1) * 8$

Reset value:  $00\ 0000_H$



| Field | Bits | Type | Description  |
|-------|------|------|--|
| RTU   | 13:0 | rw   | <p><b>Ramp time for up chirp. RTU defines the number of clock cycles for the up chirp. The actual ramp time is:</b></p> <p><math>0_D</math> ... Timer disabled (needed for fast down chirp)<br/> <math>1_D..16383_D</math> ... <math>T\_RAMP = RTU * 8 * T_{SYS\_CLK}</math></p> |

(table continues...)

(continued)

| Field  | Bits  | Type | Description   |
|--------|-------|------|---|
| RSVD   | 15:14 | r    | <b>Reserved</b>   |
| TR_EDU | 23:16 | rw   | <b>Timer for T_EDU. End of chirp delay applied after every up chirp:</b><br>$0_D \dots T\_EDU = 2 * T_{SYS\_CLK}$<br>$1_D..255_D \dots T\_EDU = (TR\_EDU * 8 + 5) * T_{SYS\_CLK}$ |

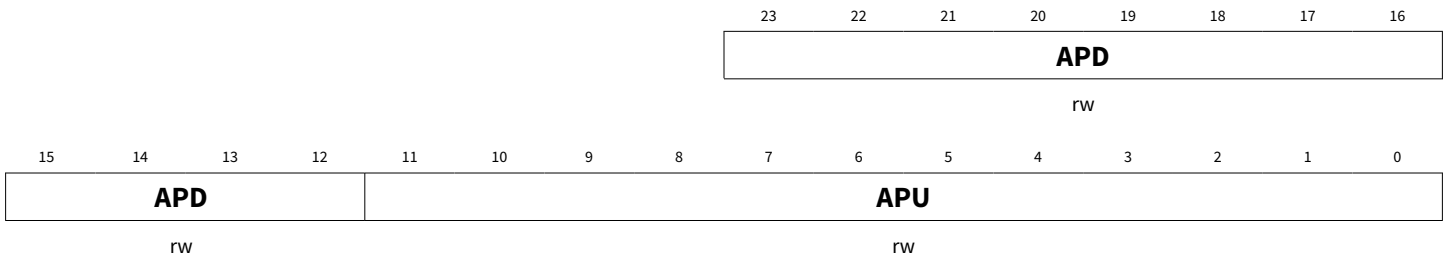
### 4.33 PLL shape x register 3

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

**PLL\_3 (x=1-4)**

Offset address:  $033_H + (x-1) * 8$

Reset value:  $00\ 0000_H$



| Field | Bits  | Type | Description   |
|-------|-------|------|---|
| APU   | 11:0  | rw   | <b>Number of samples for an up chirp of a single ADC:</b><br>$0_D..4095_D \dots$ Number of samples  |
| APD   | 23:12 | rw   | <b>Number of samples for a down chirp of a single ADC:</b><br>$0_D..4095_D \dots$ Number of samples |

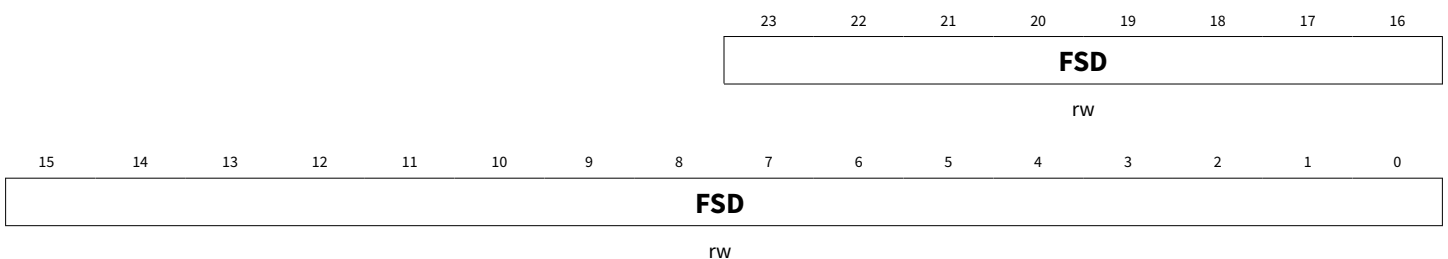
### 4.34 PLL shape x register 4

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

**PLL\_4 (x=1-4)**

Offset address:  $034_H + (x-1) * 8$

Reset value:  $00\ 0000_H$



| Field | Bits | Type | Description   |
|-------|------|------|---|
| FSD   | 23:0 | rw   | <b>Chirp start frequency for down chirp. Sigma delta start frequency for the ramp generator:</b><br>$0_D$ ... Sawtooth shape<br>Note: In case $FSD = 0_D$ , $RSD = 0_D$ , and $RTD = 0_D$ , the fast sawtooth shape is enabled. In all other cases the triangular shape is enabled. |

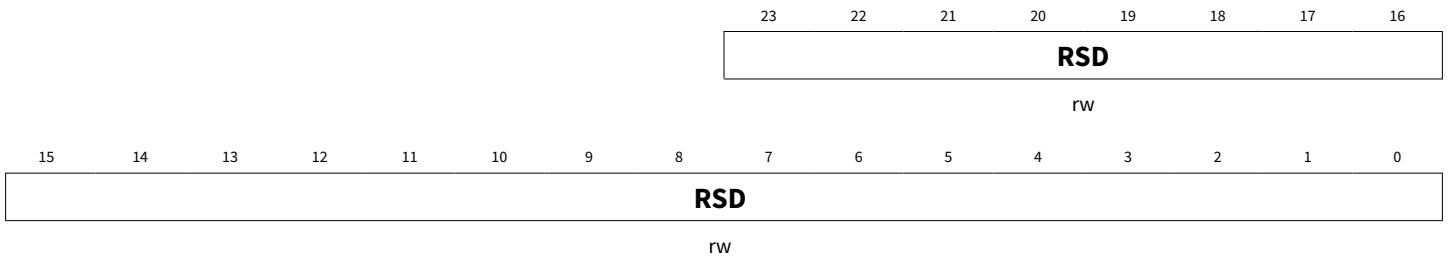
### 4.35 PLL shape x register 5

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

**PLL\_5 (x=1-4)**

Offset address:  $035_H + (x-1) * 8$

Reset value:  $00\ 0000_H$



| Field | Bits | Type | Description   |
|-------|------|------|---|
| RSD   | 23:0 | rw   | <b>Ramp step down chirp. A ramp step is the RF frequency difference added to the actual frequency during single clock cycle time of <math>T_{SYS\_CLK}</math>. In case the value is zero the RF frequency will be almost constant during the RTD time.</b><br>Bit(23) represents the sign for the ramp:<br>$0_D$ ... Up chirp<br>$1_D$ ... Down chirp |

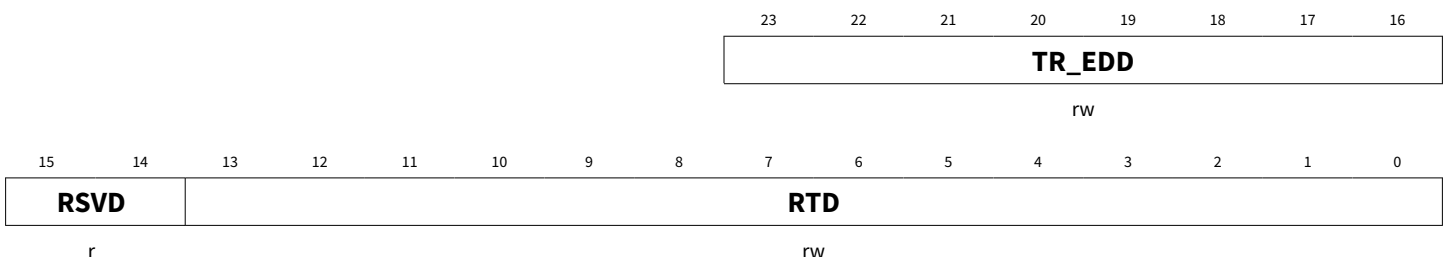
### 4.36 PLL shape x register 6

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

**PLL\_6 (x=1-4)**

Offset address:  $036_H + (x-1) * 8$

Reset value:  $00\ 0000_H$



| Field  | Bits  | Type | Description  |
|--------|-------|------|--|
| RTD    | 13:0  | rw   | <b>Ramp time for down chirp. RTD defines the number of clock cycles for the down chirp. The actual ramp time is:</b><br>$0_D \dots$ Timer disabled (needed for fast down chirp)<br>$1_D..16383_D \dots T\_RAMP = RTD * 8 * T_{SYS\_CLK}$ |
| RSVD   | 15:14 | r    | <b>Reserved</b>  |
| TR_EDD | 23:16 | rw   | <b>Timer for T_EDD. End of chirp delay applied after every down chirp:</b><br>$0_D \dots T\_EDD = 2 * T_{SYS\_CLK}$<br>$1_D..255_D \dots T\_EDD = (TR\_EDD * 8 + 5) * T_{SYS\_CLK}$  |

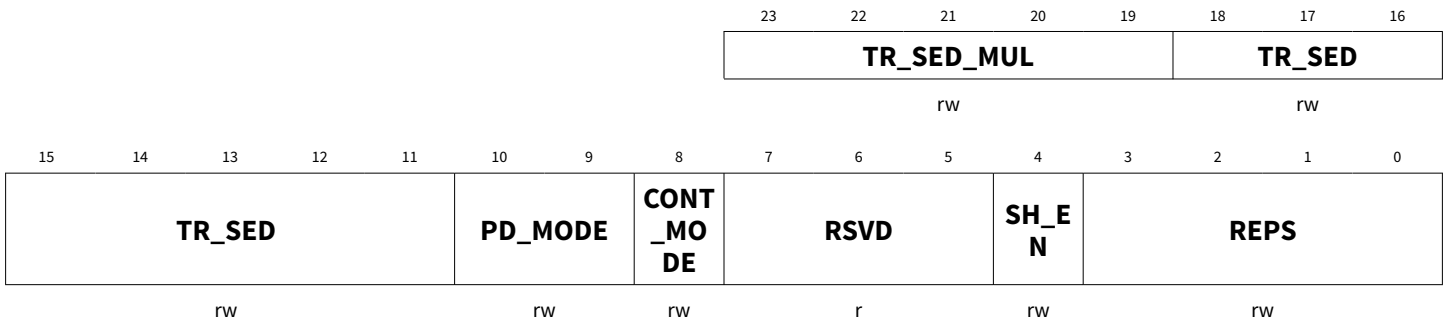
### 4.37 PLL shape x register 7

Registers PLLx, they are used to program the parameters for the modulation sequence inside the local PLL FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

#### PLL\_7 (x=1-4)

Offset address:  $037_H + (x-1) * 8$

Reset value:  $00\ 0000_H$



| Field     | Bits | Type | Description   |
|-----------|------|------|---|
| REPS      | 3:0  | rw   | <b>Repetition factor for a single shape:</b><br>$0_D..15_D \dots RS = 2^{REPS}$   |
| SH_EN     | 4    | rw   | <b>Enable shape:</b><br>$0_B \dots$ Disabled<br>$1_B \dots$ Enabled<br>Note: Values for disabled shapes are ignored. At least the first shape needs to be enabled (PLL1_7:SH_EN = 1 <sub>B</sub> ). Fields for unused shapes must be programmed to its default reset value. |
| RSVD      | 7:5  | r    | <b>Reserved</b>   |
| CONT_MODE | 8    | rw   | <b>Continuous mode. After last shape repetition RS, the specified power mode (PLL<sub>y</sub>_7:PD_MODE) is applied and</b><br>$0_B \dots$ the FSM stops immediately<br>$1_B \dots$ after T_SED the next shape set is applied   |

(table continues...)

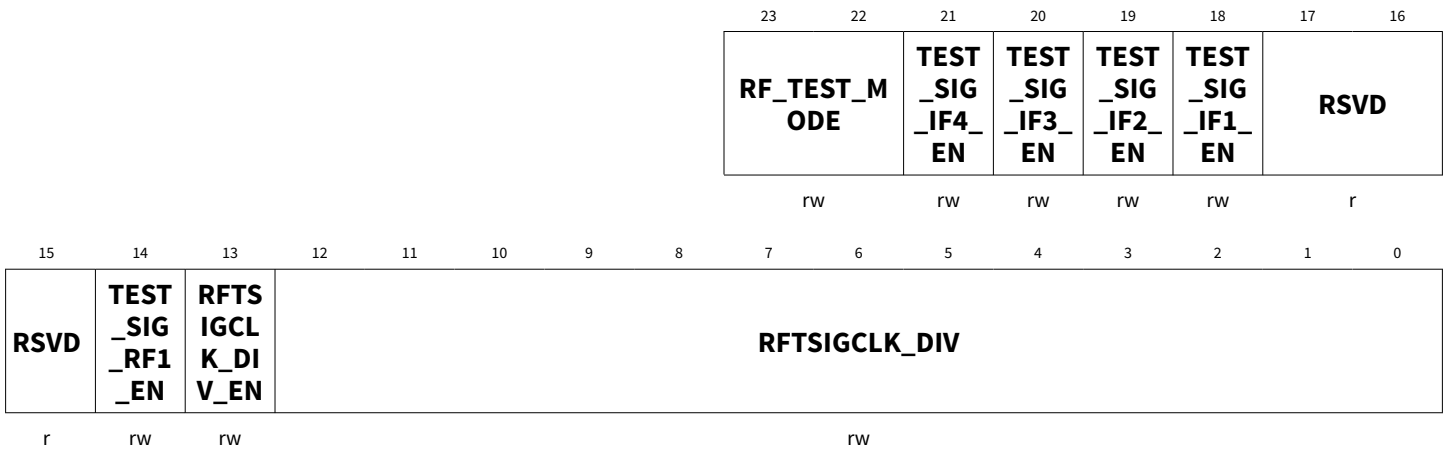
(continued)

| Field      | Bits  | Type | Description  |
|------------|-------|------|--|
| PD_MODE    | 10:9  | rw   | <b>Power down mode. After the last repetition RS the chip enters the defined power mode (during T_SED):</b><br>0 <sub>D</sub> ... Keep the same power mode (CSx + CSCx)<br>1 <sub>D</sub> ... Change to IDLE power mode (CSI + CSCi)<br>2 <sub>D</sub> ... Change to DS power mode (CSDS + CSCDS)<br>3 <sub>D</sub> ... Reserved |
| TR_SED     | 18:11 | rw   | <b>Timer for T_SED:</b><br>0 <sub>D</sub> ... T <sub>SYS_CLK</sub><br>1 <sub>D</sub> ..255 <sub>D</sub> ... T_SED = (TR_SED * 2 <sup>TR_SED_MUL</sup> * 8 + TR_SED_MUL + 3) * T <sub>SYS_CLK</sub>   |
| TR_SED_MUL | 23:19 | rw   | <b>Timer multiplier for T_SED:</b><br>0 <sub>D</sub> ..31 <sub>D</sub> ... 2 <sup>TR_SED_MUL</sup>   |

### 4.38 RF test register 0

Register contains several bits used to enable dedicated paths for self-test.

**RFT0** Offset address: 055<sub>H</sub>  
 RF test register 0 Reset value: 00 1F40<sub>H</sub>



| Field            | Bits | Type | Description   |
|------------------|------|------|---|
| RFTSIGCLK_DIV    | 12:0 | rw   | <b>RF test tone signal divider value. <math>f_{RFTST} = f_{SYS\_CLK} / RFTSIGCLK\_DIV</math>:</b><br>0 <sub>D</sub> ... Reserved<br>1 <sub>D</sub> ... Reserved<br>2 <sub>D</sub> ... Minimum value<br>8191 <sub>D</sub> ... Maximum value<br>Note: RFTSIGCLK_DIV should only be changed when RFTSIGCLK_DIV_EN=0 <sub>B</sub> |
| RFTSIGCLK_DIV_EN | 13   | rw   | <b>Enable the RF test tone signal output to the baseband:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |

(table continues...)



| Field       | Bits                    | Type | Description  |
|-------------|-------------------------|------|--|
| RSVD        | 3:0,<br>13:5,<br>23:15, | r    | <b>Reserved</b>  |
| EFUSE_EN    | 4                       | rw   | <b>Enable EFUSE:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| EFUSE_SENSE | 14                      | w    | <b>Start EFUSE read sequence:</b><br>0 <sub>B</sub> ... No effect<br>1 <sub>B</sub> ... Executes EFUSE reading and clears this bit |

**Table 23** Reset values of **EFUSE0**

| Reset type | Reset value                                   | Note |
|------------|---|------|
| Reset      | X000 0000 0000 0010 0000<br>0000 <sub>B</sub> |      |

## 4.40 EFUSE register 1

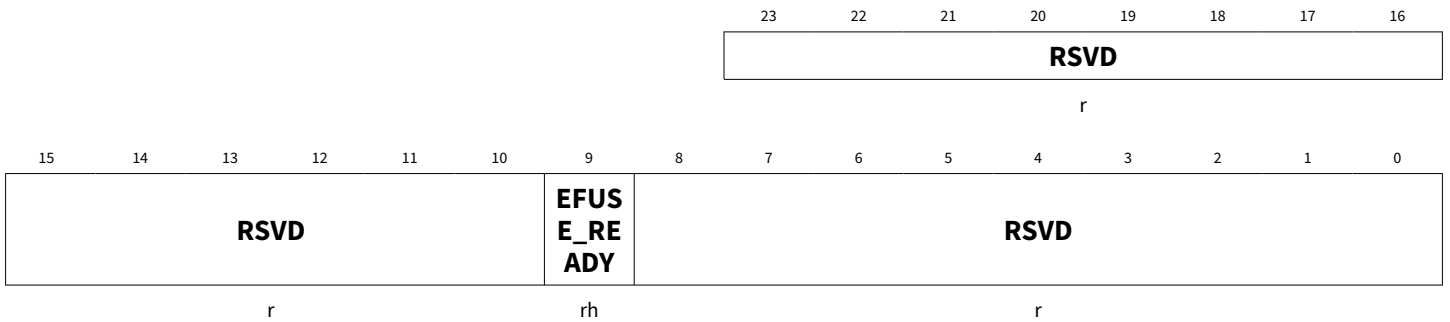
Register contains several bits used to read out eFuses.

### EFUSE1

EFUSE register 1

Offset address: 058<sub>H</sub>

Reset value: 00 0300<sub>H</sub>



| Field       | Bits          | Type | Description   |
|-------------|---------------|------|---|
| RSVD        | 8:0,<br>23:10 | r    | <b>Reserved</b>   |
| EFUSE_READY | 9             | rh   | <b>EFUSE ready:</b><br>0 <sub>B</sub> ... Not ready<br>1 <sub>B</sub> ... Ready<br>Note: Only valid after EFUSE_SENSE was executed! Result stored in CHIP_ID0 and CHIP_ID1. |

### 4.41 PLL test register 0

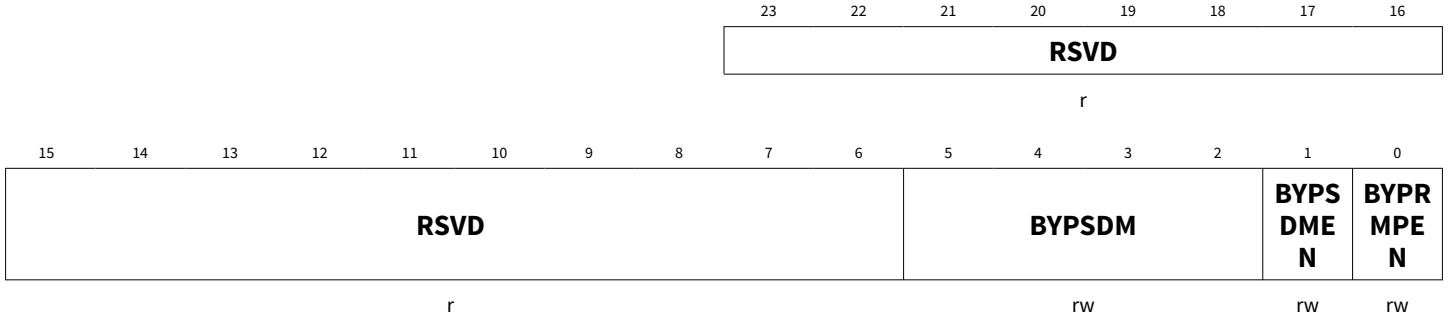
The setting in this register should be used when the CW mode is enabled. Sigma delta modulator (SDM) is bypassed in CW mode.

**PDFT0**

Offset address: 059<sub>H</sub>

PLL test register 0

Reset value: 00 0000<sub>H</sub>



| Field    | Bits | Type | Description  |
|----------|------|------|--|
| BYPRMPEN | 0    | rw   | <b>Enable bypass ramp generator:</b><br>0 <sub>B</sub> ... Ramp generator enabled<br>1 <sub>B</sub> ... Ramp generator disabled (bypassed) |
| BYPSDMEN | 1    | rw   | <b>Enable bypass for sigma delta modulator:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled                               |
| BYPSDM   | 5:2  | rw   | <b>Value used for bypassed sigma delta modulator:</b><br>0 <sub>D</sub> ... Minimum value<br>15 <sub>D</sub> ... Maximum value             |
| RSVD     | 23:6 | r    | <b>Reserved</b>  |

### 4.42 Chip ID register 0

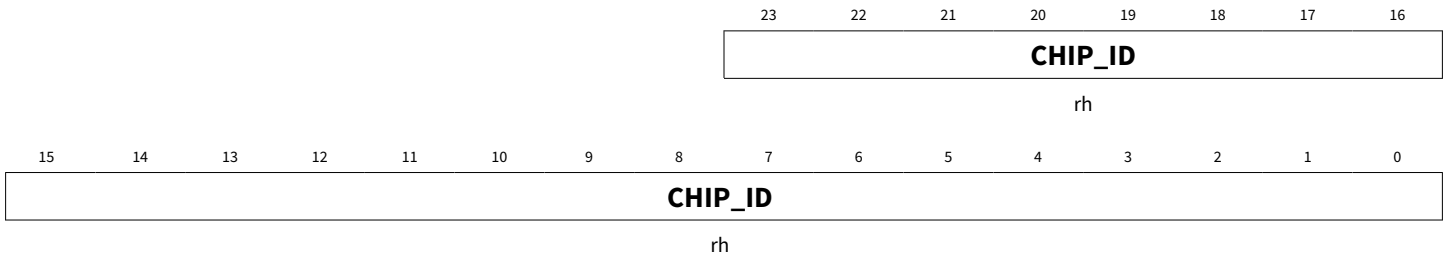
The unique chip ID consists of 48 bits. Register CHIP\_ID0 provides the first 24bits of the ID.

**CHIP\_ID0**

Offset address: 05D<sub>H</sub>

Chip ID register 0

Reset value: FF FFFF<sub>H</sub>



| Field   | Bits | Type | Description  |
|---------|------|------|--|
| CHIP_ID | 23:0 | rh   | <b>Chip ID[23:0].</b><br>Note: Valid after EFUSE_SENSE was executed. |

### 4.43 Chip ID register 1

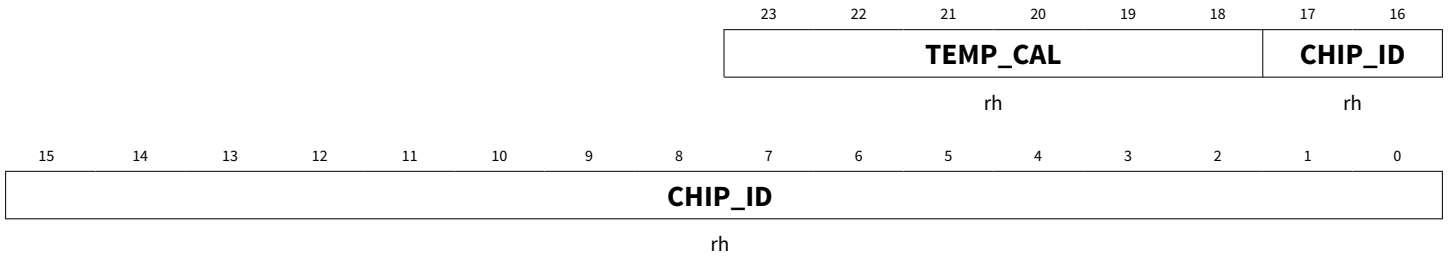
The unique chip ID consists of 48 bits. Register CHIP\_ID1 provides the second 18 bits of the Chip ID and the 6 bits of the temperature sensor calibration value.

**CHIP\_ID1**

Chip ID register 1

Offset address: 05E<sub>H</sub>

Reset value: FF FFFF<sub>H</sub>



| Field    | Bits  | Type | Description   |
|----------|-------|------|---|
| CHIP_ID  | 17:0  | rh   | <b>Chip ID[41:24].</b><br>Note: Valid after EFUSE_SENSE was executed.                                       |
| TEMP_CAL | 23:18 | rh   | <b>Temperature sensor calibration value in two's complement (range -32<sub>D</sub> to +31<sub>D</sub>).</b> |

### 4.44 Clock input register

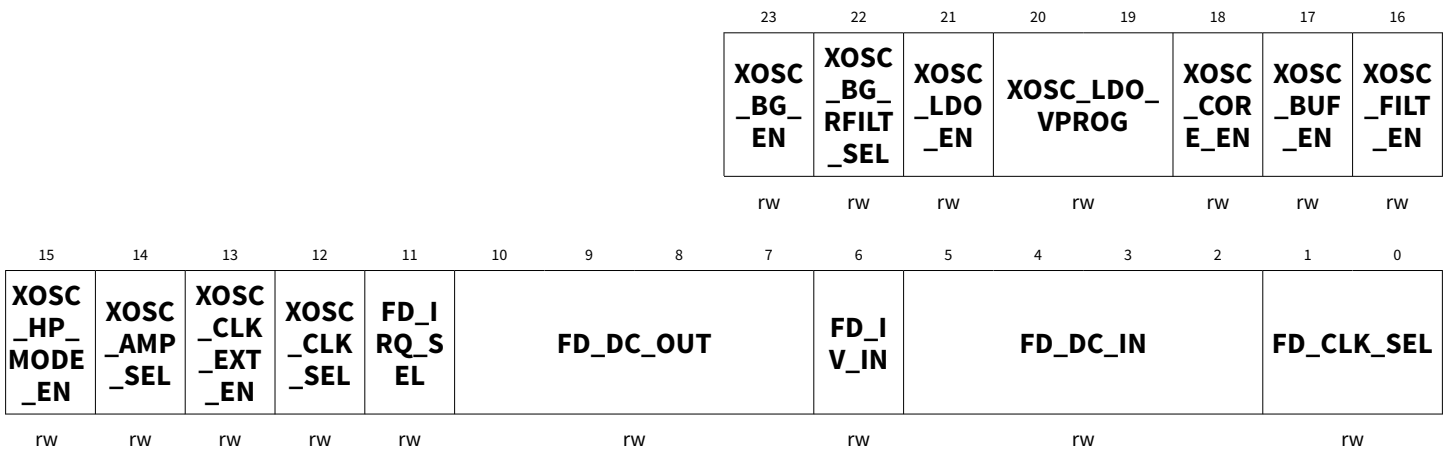
CLK\_IN register bit fields are used to program the input clock path.

**CLK\_IN**

Clock input register

Offset address: 05F<sub>H</sub>

Reset value: 10 4400<sub>H</sub>



| Field           | Bits | Type | Description  |
|-----------------|------|------|--|
| FD_CLK_SEL      | 1:0  | rw   | <p><b>Selection of input clock frequency and clock path:</b></p> <p>0<sub>D</sub> ... Frequency doubler bypassed<br/>           1<sub>D</sub> ... Frequency doubler without DC_IN<br/>           2<sub>D</sub> ... Frequency doubler with DC_IN<br/>           3<sub>D</sub> ... Frequency doubler with DC calibration for system clock and without DC calibration for PLL clock</p> <p><b>Note:</b> It is important to program FD register first and enable the system clock afterwards by programming PACR1(23) register.</p>  |
| FD_DC_IN        | 5:2  | rw   | <p><b>Duty cycle of input clock can be adjusted before entering the internal clock doublers. This adjustment can be used for equalizing the input clock to a DC of 50 % by applying a clock delay to the input clock. Delay times are in steps of 125 ps.:</b></p> <p>0<sub>D</sub> ... +0.23 ns (minimal adjustment)<br/>           ...<br/>           15<sub>D</sub> ... +2.1 ns (maximal adjustment)</p>  |
| FD_IV_IN        | 6    | rw   | <p><b>Inverts input clock of duty cycle adjustment. Only active if FD_CLK_SEL = 2<sub>D</sub> or 3<sub>D</sub>.</b></p> <p>0<sub>B</sub> ... Clock not inverted<br/>           1<sub>B</sub> ... Clock inverted</p>  |
| FD_DC_OUT       | 10:7 | rw   | <p><b>Duty cycle adjustment of clock doubler for system clock. The system clock pulse width can be adjusted by 15 delay cells, starting from 4.3 ns up to 4.3 ns + 15 * 0.45 ns. The duty cycle then is <math>DC_{SYS\_CLK} = (4.3\text{ ns} + FD\_DC\_OUT * 0.4\text{ ns}) / T_{SYS\_CLK}</math>.</b></p> <p>0<sub>D</sub> ... 4.3 ns<br/>           1<sub>D</sub> ... 4.7 ns<br/>           ...<br/>           4<sub>D</sub> ... 6.10 ns (preferred value for e.g. 80 MHz)<br/>           5<sub>D</sub> ... 6.55 ns (preferred value for e.g. 76.8 MHz)<br/>           ...<br/>           15<sub>D</sub> ... 11.05 ns</p> <p>Note: The duty cycle of the system clock can be adjusted via CLK_IN:FD_DC_OUT and can be monitored via IRQ pin.</p> |
| FD_IRQ_SEL      | 11   | rw   | <p><b>Select frequency doubler output at IRQ pin:</b></p> <p>0<sub>B</sub> ... Normal irq functionality at IRQ pin<br/>           1<sub>B</sub> ... Frequency doubler output at IRQ pin</p> <p>Note: Frequency doubler has higher priority as interrupt.</p>   |
| XOSC_CLK_SEL    | 12   | rw   | <p><b>Clock source selection:</b></p> <p>0<sub>B</sub> ... On-chip crystal oscillator<br/>           1<sub>B</sub> ... External clock</p>  |
| XOSC_CLK_EXT_EN | 13   | rw   | <p><b>Forward oscillator clock to OSC_OUT:</b></p> <p>0<sub>B</sub> ... Disabled<br/>           1<sub>B</sub> ... Enabled</p>  |

(table continues...)

(continued)

| Field                 | Bits  | Type | Description   |
|-----------------------|-------|------|---|
| XOSC_AMP_SE<br>L      | 14    | rw   | <b>XOSC amplitude selection:</b><br>0 <sub>B</sub> ... Low amplitude (normal)<br>1 <sub>B</sub> ... Reserved  |
| XOSC_HP_MOD<br>E_EN   | 15    | rw   | <b>Enables high performance mode of XOSC output clock buffer:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: Switch from 0 <sub>B</sub> to 1 <sub>B</sub> after start-up to reduce start-up time.                          |
| XOSC_FILT_EN          | 16    | rw   | <b>Enables XOSC noise filter:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: Switch from 0 <sub>B</sub> to 1 <sub>B</sub> after start-up to reduce start-up time.  |
| XOSC_BUF_EN           | 17    | rw   | <b>Enables XOSC output clock buffer:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled<br>Note: Switch from 0 <sub>B</sub> to 1 <sub>B</sub> after start-up to reduce start-up time.   |
| XOSC_CORE_E<br>N      | 18    | rw   | <b>Enables XOSC core:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled  |
| XOSC_LDO_VP<br>ROG    | 20:19 | rw   | <b>LDO output voltage of XOSC LDO:</b><br>0 <sub>D</sub> ... Reserved<br>1 <sub>D</sub> ... 1.50 V (normal)<br>2 <sub>D</sub> ... Reserved<br>3 <sub>D</sub> ... Reserved   |
| XOSC_LDO_EN           | 21    | rw   | <b>Enables XOSC LDO:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |
| XOSC_BG_RFIL<br>T_SEL | 22    | rw   | <b>Selection of resistor value of bandgap filter:</b><br>0 <sub>B</sub> ... R <sub>FILT</sub> = 7.5 kΩ<br>1 <sub>B</sub> ... R <sub>FILT</sub> = 1.0 MΩ<br>Note: Switch from 0 <sub>B</sub> to 1 <sub>B</sub> after start-up to reduce start-up time. |
| XOSC_BG_EN            | 23    | rw   | <b>Enables XOSC bandgap reference:</b><br>0 <sub>B</sub> ... Disabled<br>1 <sub>B</sub> ... Enabled   |

## 4.45 Wake up register

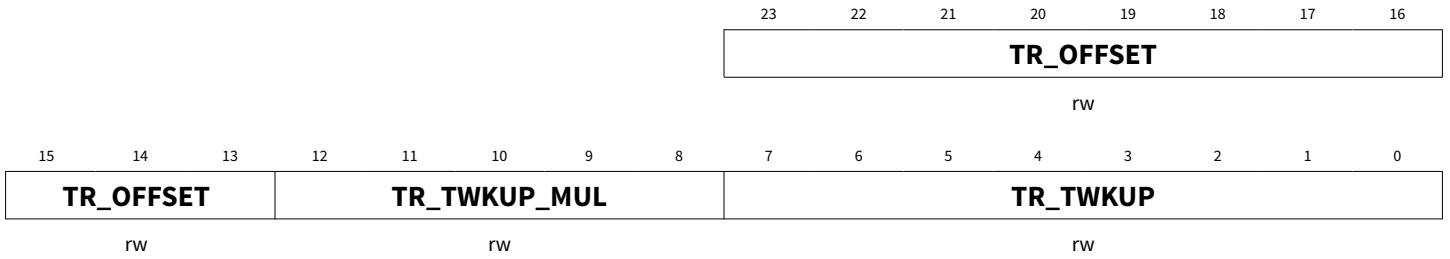
**WU**

Wake up register

Offset address: 060<sub>H</sub>

DefaultName value: 00 0000<sub>H</sub>

4 BGT60ATR24AIP registers



| Field            | Bits  | Type | Description   |
|------------------|-------|------|---|
| TR_TWKUP         | 7:0   | rw   | <b>Timer for T_WU:</b><br>$0_D \dots T_{SYS\_CLK}$<br>$1_D..255_D \dots T_{WU} = (TR\_WKUP * 2^{TR\_WKUP\_MUL} * 8 + TR\_WKUP\_MUL + 3) * T_{SYS\_CLK}$<br>Note: $T_{WU\_TYP} = 1 \text{ ms}$   |
| TR_TWKUP_MU<br>L | 12:8  | rw   | <b>Timer multiplier factor for T_WU:</b><br>$0_D..31_D \dots 2^{TR\_WKUP\_MUL}$   |
| TR_OFFSET        | 23:13 | rw   | <b>Timer for chip offset before wake-up time and after deep-sleep state (after reset). <math>T\_OFFSET = (TR\_OFFSET + 3) * T_{SYS\_CLK}</math></b><br>$0_D \dots T\_OFFSET$ is $0 T_{SYS\_CLK}$ (off)<br>$1_D \dots T\_OFFSET$ is $4 T_{SYS\_CLK}$<br>$2_D \dots T\_OFFSET$ is $5 T_{SYS\_CLK}$<br>... |

**4.46 Status register 0**

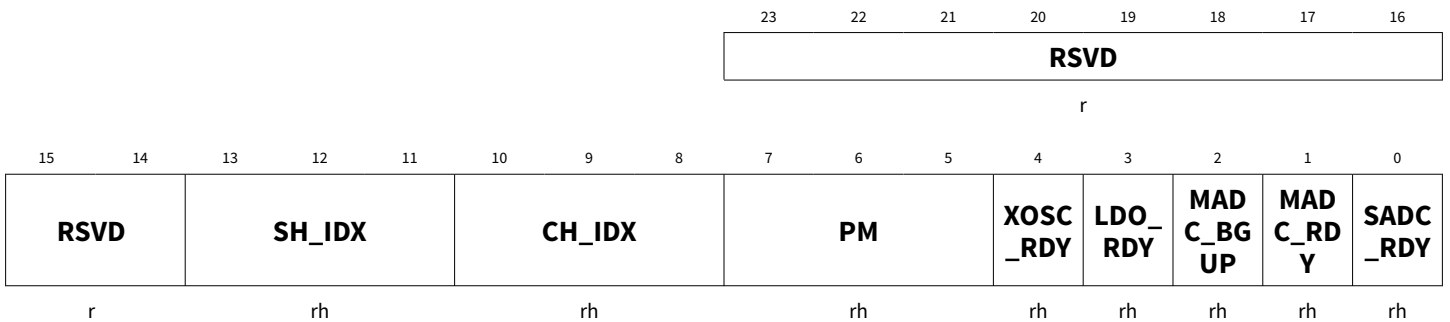
The status register STAT0 provides the actual value of some specific internal states. However it should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after e.g. 100 µs.

**STAT0**

Status register 0

Offset address: 061<sub>H</sub>

Reset value: 00 00A8<sub>H</sub>



| Field     | Bits  | Type | Description  |
|-----------|-------|------|--|
| SADC_RDY  | 0     | rh   | <b>SADC status:</b><br>0 <sub>B</sub> ... Not ready<br>1 <sub>B</sub> ... Ready  |
| MADC_RDY  | 1     | rh   | <b>MADC status:</b><br>0 <sub>B</sub> ... Not ready<br>1 <sub>B</sub> ... Ready  |
| MADC_BGUP | 2     | rh   | <b>MADC bandgap reference power up status:</b><br>0 <sub>B</sub> ... Not ready<br>1 <sub>B</sub> ... Ready   |
| LDO_RDY   | 3     | rh   | <b>LDO status (V<sub>DDC</sub> above the threshold):</b><br>0 <sub>B</sub> ... Not ready<br>1 <sub>B</sub> ... Ready   |
| XOSC_RDY  | 4     | rh   | <b>XOSC power-up status:</b><br>0 <sub>B</sub> ... XOSC not ready (not stable)<br>1 <sub>B</sub> ... XOSC ready (running)  |
| PM        | 7:5   | rh   | <b>Power mode of the FSM:</b><br>0 <sub>D</sub> ... Deep sleep mode (after reset)<br>1 <sub>D</sub> ... Active mode<br>2 <sub>D</sub> ... Interchirp mode<br>3 <sub>D</sub> ... Idle mode<br>4 <sub>D</sub> ... Reserved<br>5 <sub>D</sub> ... Deep sleep mode<br>6 <sub>D</sub> ... Reserved<br>7 <sub>D</sub> ... Reserved |
| CH_IDX    | 10:8  | rh   | <b>Channel set index enabled by the FSM:</b><br>0 <sub>D</sub> ... CSU1<br>1 <sub>D</sub> ... CSD1<br>2 <sub>D</sub> ... CSU2<br>3 <sub>D</sub> ... CSD2<br>4 <sub>D</sub> ... CSU3<br>5 <sub>D</sub> ... CSD3<br>6 <sub>D</sub> ... CSU4<br>7 <sub>D</sub> ... CSD4   |
| SH_IDX    | 13:11 | rh   | <b>Shape index enabled by the FSM:</b><br>0 <sub>D</sub> ... PLLU1<br>1 <sub>D</sub> ... PLLD1<br>2 <sub>D</sub> ... PLLU2<br>3 <sub>D</sub> ... PLLD2<br>4 <sub>D</sub> ... PLLU3<br>5 <sub>D</sub> ... PLLD3<br>6 <sub>D</sub> ... PLLU4<br>7 <sub>D</sub> ... PLLD4   |

(table continues...)

(continued)

| Field | Bits  | Type | Description |
|-------|-------|------|-------------|
| RSVD  | 23:14 | r    | Reserved    |

#### 4.47 Sensor ADC result register

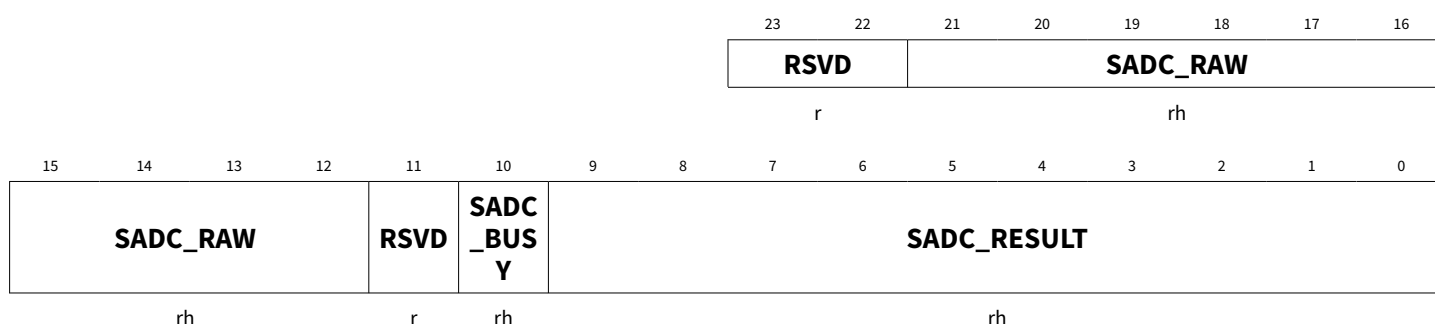
The sensor ADC register SADC\_RESULT is used to monitor the SADC as well as to read out the output from the conversion.

##### SADC\_RESULT

Offset address: 062<sub>H</sub>

Sensor ADC result register

Reset value: 00 0000<sub>H</sub>



| Field       | Bits         | Type | Description   |
|-------------|--------------|------|---|
| SADC_RESULT | 9:0          | rh   | <b>SADC measurement result (10bit).</b><br>Note: In case 8 bit are converted, the 8 bit value is left-shifted by two (multiplied by 4). In case 9 bit are converted, the 9 bit result is left-shifted by one (multiplied by 2). |
| SADC_BUSY   | 10           | rh   | <b>Shows the SADC busy status:</b><br>0 <sub>B</sub> ... Not busy<br>1 <sub>B</sub> ... Busy  |
| RSVD        | 11,<br>23:22 | r    | Reserved  |
| SADC_RAW    | 21:12        | rh   | <b>SADC raw data.</b><br>Note: Should only be used for test.  |

#### 4.48 FIFO status register

The FIFO status register FSTAT is used to monitor the FIFO. It should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after e.g. 100 µs.

##### FSTAT

Offset address: 063<sub>H</sub>

FIFO status register

Reset value: 10 4000<sub>H</sub>



(continued)

| Field   | Bits | Type | Description  |
|---------|------|------|--|
| CREF    | 21   | rh   | <b>FIFO fill status exceeds compare reference:</b><br>0 <sub>B</sub> ... Fill status below reference<br>1 <sub>B</sub> ... Fill status above reference   |
| FULL    | 22   | rh   | <b>FIFO full status:</b><br>0 <sub>B</sub> ... FIFO not full<br>1 <sub>B</sub> ... FIFO full   |
| FOF_ERR | 23   | rh   | <b>FIFO overflow error bit shows if more sample data are transferred to the FIFO than FIFO memory locations are available to store the data. The flag is also shown in GSR0 as a part of FIFO over or underflow error bit FOU_ERR:</b><br>0 <sub>B</sub> ... No FIFO overflow<br>1 <sub>B</sub> ... FIFO overflow<br>Note: Bit will be reset after HW, SW or FIFO reset. |

#### 4.49 Global status register

The global status register GSR0 is related to SPI read/write monitoring.

**GSR0** 0<sub>H</sub>  
Global status register Reset value: x11110100<sub>B</sub>

|  |      |   |   |           |                  |                     |                      |    |
|--|------|---|---|-----------|------------------|---------------------|----------------------|----|
|  | 7    | 6 | 5 | 4         | 3                | 2                   | 1                    | 0  |
|  | RSVD |   |   | FOU_ERROR | MISO_HS_R<br>EAD | SPI_BURST_<br>ERROR | CLK_NUMBE<br>R_ERROR |    |
|  | r    |   |   | rh        | rh               | rh                  | rh                   | rh |

| Field                | Bits | Type | Description  |
|----------------------|------|------|--|
| CLK_NUMBER_<br>ERROR | 0    | rh   | <b>Defined within the SPI chapter:</b><br>0 <sub>B</sub> ... No clock number error<br>1 <sub>B</sub> ... Error condition occurred  |
| SPI_BURST_ER<br>ROR  | 1    | rh   | <b>SPI burst error defined within the SPI chapter:</b><br>0 <sub>B</sub> ... No burst read/write error<br>1 <sub>B</sub> ... Burst error   |
| MISO_HS_REA<br>D     | 2    | rh   | <b>SPI MISO high speed mode:</b><br>0 <sub>B</sub> ... Not active<br>1 <sub>B</sub> ... Active   |
| FOU_ERROR            | 3    | rh   | <b>Shows if FIFO overflow or underflow condition occurred. The error will be cleared after the following resets: FIFO reset or SW reset or HW reset:</b><br>0 <sub>B</sub> ... No error<br>1 <sub>B</sub> ... Error condition occurred |
| RSVD                 | 7:4  | r    | <b>Reserved</b>  |

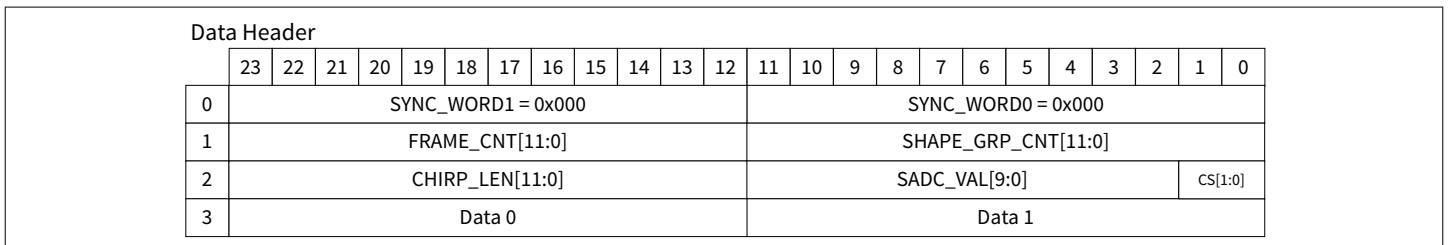
## 5 Data organization and SPI interface

### 5.1 Data header

The main FSM is capable of generating a data header to be attached to the actual radar raw data. The structure of the header is shown in the following figure and table. The data header can be disabled by controlling the bit SFCTL:PREFIX\_EN (see [Chapter 4.9](#)).

A sync-word is sent at the beginning of each acquisition to make the radar raw-data from each shape unique. This can be useful in case of broken communication with the application processor or in case of errors. Supposing the FIFO will generate a “FIFO overflow flag” the sync-word 0x000000 can be evaluated by the host controller and used to resync with the BGT60ATR24AIP and discard the data received before this sync word (if header or sync-word not used then the controller should reset the FIFO, discarding the actual FIFO data). On “FIFO underflow flag”, the received data bits from the host are 111111111111<sub>B</sub>.

Following, the header includes also the frame counter and shape group counter, as well as the actual APU/APD value (see [PLL shape x register 3](#)) and temperature value.



**Figure 20** Data header

**Table 24** Data header description

| Symbol        | Word | Bits  | Description  | RST            |
|---------------|------|-------|--|----------------|
| SYNC_WORD1    | #0   | 23:12 | The sync-word can be used to identify the start of a new chirp. In case the MADC will output also a sequence of 0x000000, to make the sync-word unique, the data from the MADC will be automatically changed to 0x001 before transferring it to the FIFO.  | 0 <sub>D</sub> |
| SYNC_WORD0    | #0   | 11:0  | See SYNC_WORD1.  | 0 <sub>D</sub> |
| FRAME_CNT     | #1   | 23:12 | Same as STAT1:FRAME_CNT (see <a href="#">Status register 1</a> )<br><br><b>Note:</b> <i>FRAME_CNT info should not be used by the host when endless mode is enabled (please check CCR2:MAX_FRAME_CNT). In case it is needed the software has to ensure that any value 0 of the FRAME_CNT after 4095 is treated as value 4095. Afterwards FRAME_CNT starts with the value 1.</i> | 0 <sub>D</sub> |
| SHAPE_GRP_CNT | #1   | 11:0  | Same as STAT1:SHAPE_GRP_CNT (see <a href="#">Status register 1</a> ).  | 0 <sub>D</sub> |
| CHIRP_LEN     | #2   | 23:12 | Number of MADC samples inside the chirp (APU/APD value of related chirp).  | 0 <sub>D</sub> |
| SADC_VAL      | #2   | 11:2  | 10 bits of sensor ADC output data (e.g. temperature).  | 0 <sub>D</sub> |
| CS            | #2   | 1:0   | Indicates the channel shape number to which the following sampling data belongs to.  |                |

(table continues...)

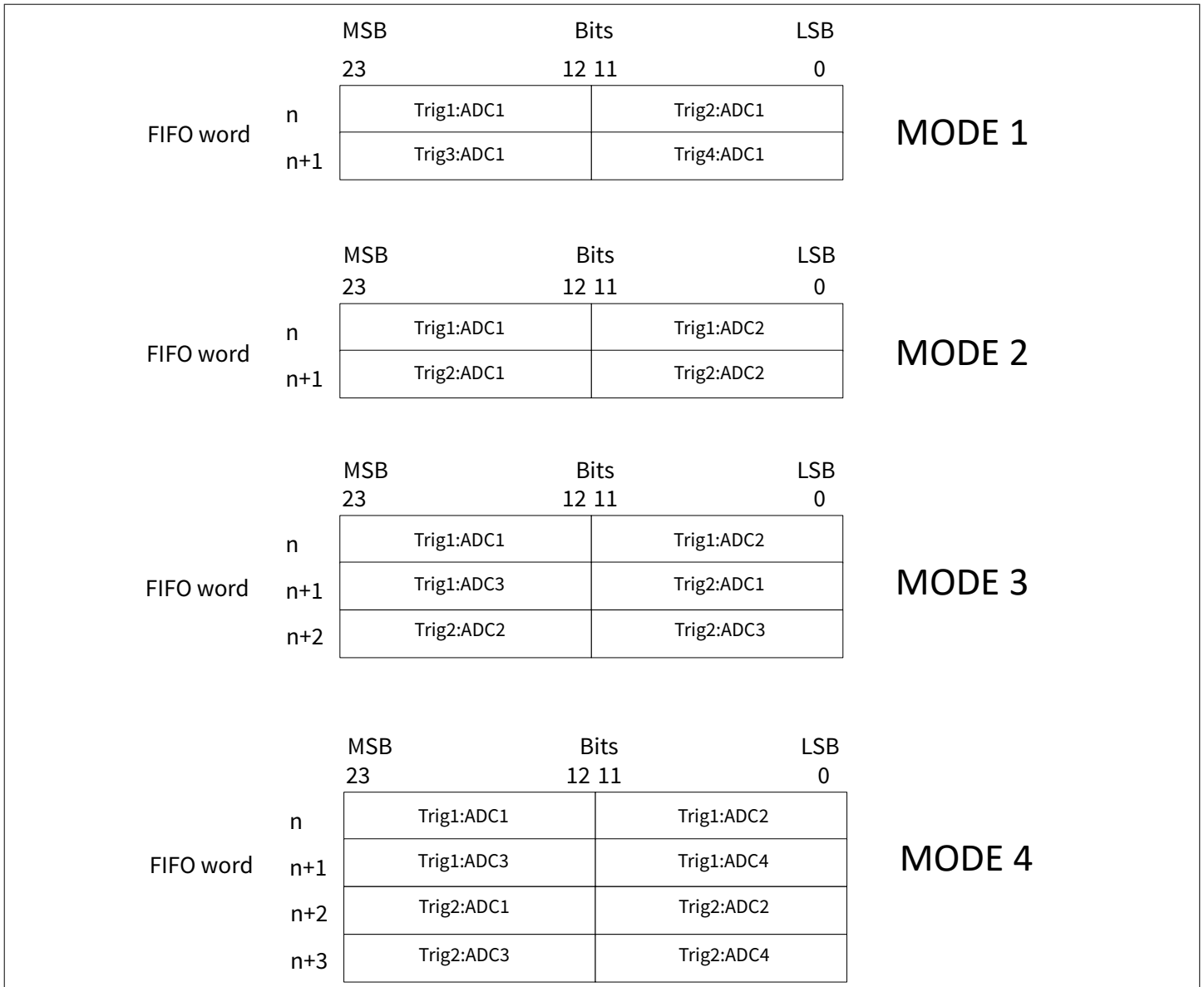
**Table 24** (continued) **Data header description**

| Symbol | Word | Bits  | Description                                  | RST |
|--------|------|-------|--|-----|
| DATA0  | #3   | 23:12 | MSB data (see <a href="#">Chapter 5.2</a> ). |     |
| DATA1  | #3   | 11:0  | LSB data (see <a href="#">Chapter 5.2</a> ). |     |

## 5.2 FIFO and data flow

The memory in the BGT60ATR24AIP is based on a *FIFO*. The FIFO consists of a circular shift register organized in 8192 words of 24 bits each. Following data flow modes from multi *ADC* to the FIFO are supported by the *FSM* (see following figure):

- Mode 1: One ADC active
  - Data from 1<sup>st</sup> sample, 12 bits, are temporarily stored in a buffer
  - When the 2<sup>nd</sup> sample, 12 bits, are available, both, 1<sup>st</sup> and 2<sup>nd</sup> (24 bits), are stored into one data word
- Mode 2: Two ADC active
  - Data from active ADC are occupying one data word in the FIFO
- Mode 3: Three ADC active
  - Data from first two channels are stored into a data word while data from third channel is buffered. On the consecutive trigger the buffered data and the one from first channel are stored in a data word while the data of the second channel is buffered. On the next trigger the buffered data plus the data from the third channel are stored in a third data word, etc.
- Mode 4: Four ADC active
  - Data from active ADC are occupying two data word in the FIFO



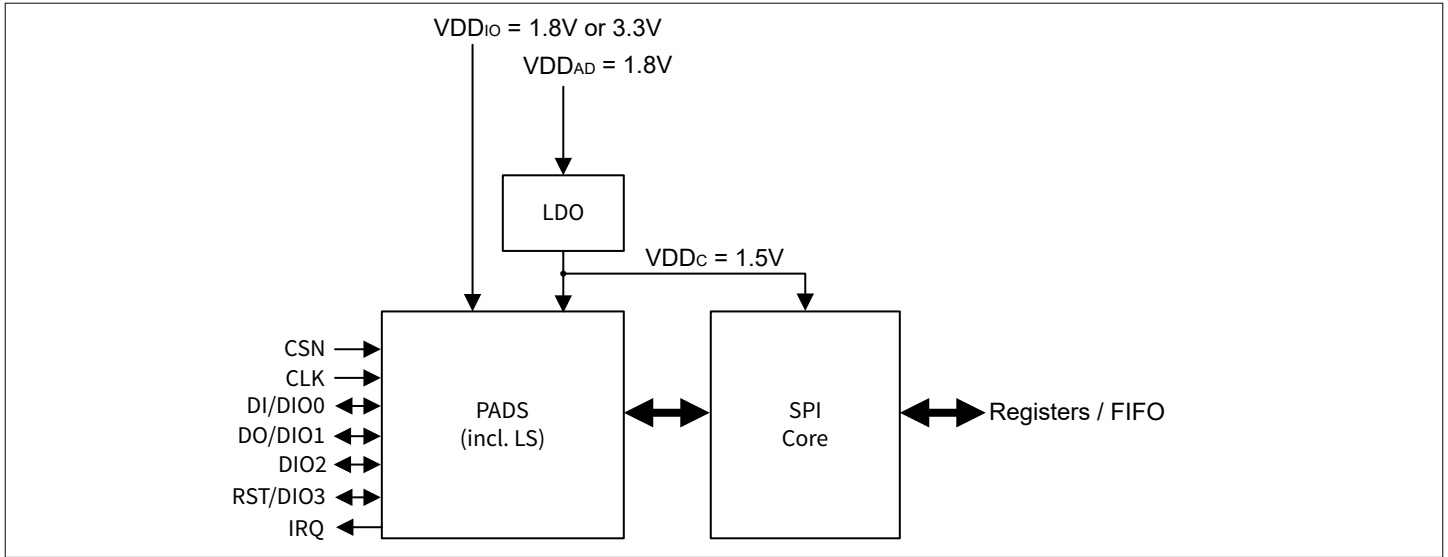
**Figure 21** FIFO organization

Readout from the FIFO should be executed from the host controller using memory address with correct data length. Data length can be derived from the data header or based on the “sync-word”.

**Note:** An illegal write to memory address space will lead to lost FIFO data!

### 5.3 SPI – Serial Peripheral Interface module

The *SPI* is the communication interface between the host and the BGT60ATR24AIP. It enables the host to read from, or write to (program) the registers as well as reading from the FIFO.



**Figure 22 SPI module**

BGT60ATR24AIP device features four I/O pins for SPI communication and one for chip reset. DIO pins are pulled up to logic high inside the pad.

- CSN to be connected to SS of the SPI master
- CLK to be connected to CLK of the SPI master
- DI/DIO0 to be connected to MOSI of the SPI master
- DO/DIO1 to be connected to MISO of the SPI master
- DIO2 to be connected to data 2 of the SPI master
- DIO3 to be connected to data 3 of the SPI master

**Table 25 SPI pins**

| Pin name    | Standard / Quad SPI mode function | Remarks            |
|-------------|-----------------------------------|--------------------|
| CSN         | CSN                               | Chip select not    |
| CLK         | CLK                               | SPI clock          |
| DI<br>DIO0  | MOSI<br>DIO0                      | HiZ, bidirectional |
| DO<br>DIO1  | MISO<br>DIO1                      | HiZ, bidirectional |
| DIO2        | DIO2                              | HiZ, bidirectional |
| RST<br>DIO3 | RESET<br>DIO3                     | HiZ, bidirectional |

The SPI interface can be clocked up to 50 MHz. To meet the timing requirements for higher SPI clock frequencies (e.g., >25 MHz) the BGT60ATR24AIP device offers an additional high speed mode (SFCTL:MISO\_HS\_RD) which increase the timing budget on SPI master side by sending out data via DO with the rising edge instead of the falling edge of the CLK.

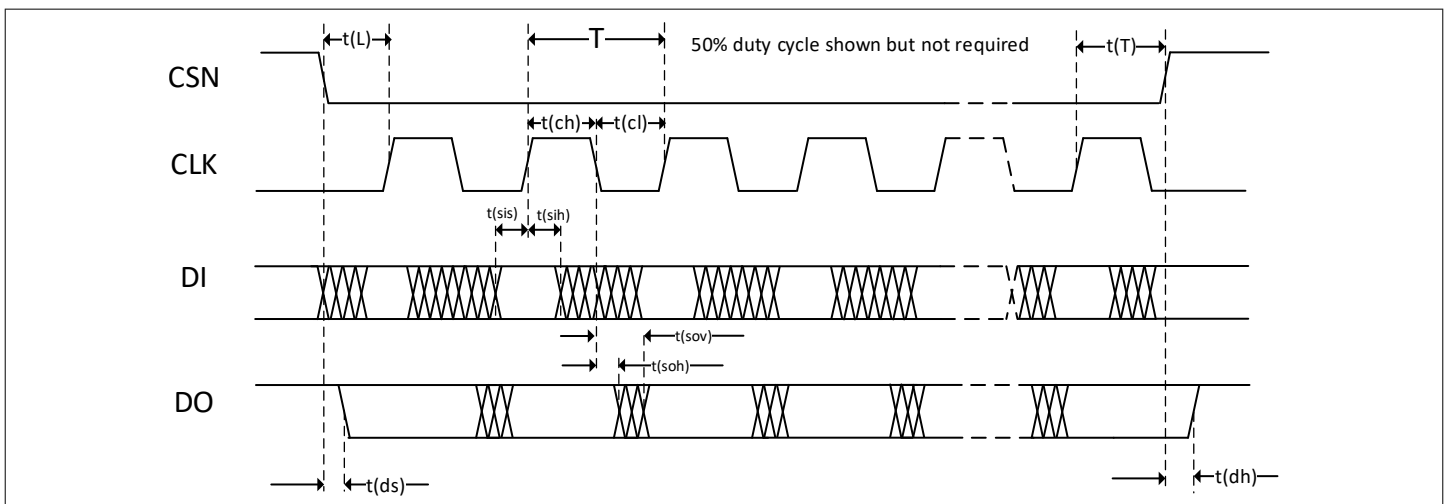
### 5.3.1 Standard SPI timing

The timing diagram for normal SPI mode (SFCTL:MISO\_HS\_RD = 0<sub>B</sub>) is presented in the following figure. A SPI transfer is started with a falling edge of chip select signal CSN generated by the SPI master. At the same time, the SPI master shall drive the level of the data input signal DI (*master out, slave in (MOSI)*) according to the first bit. Also, with the falling edge of the chip select signal CSN the SPI slave applies the level of the data on the output signal DO (*master in, slave out (MISO)*) according to the first bit which shall be transferred to the SPI master, the level becomes stable after the period  $t(ds)$ . The SPI master has to wait for the time  $t(L)$  before the clock signal CLK can be generated.

With the rising edge of CLK the SPI slave captures the level of DI. The SPI master must keep the DI level stable for  $t(sis)$  before and for  $t(sih)$  after the rising edge of CLK to ensure valid setup and hold time of the SPI slave. With the falling edge of CLK the SPI master shall set the level of DI according to the next bit the master wants to send.

The SPI master is supposed to read the level of DO with the rising edge of CLK. The SPI slave keeps the DO level stable for  $t(soh)$  after the falling edge of CLK. With the falling edge of CLK the SPI slave drives the level of DO according to the next bit, DO becomes stable after latest  $t(sov)$ .

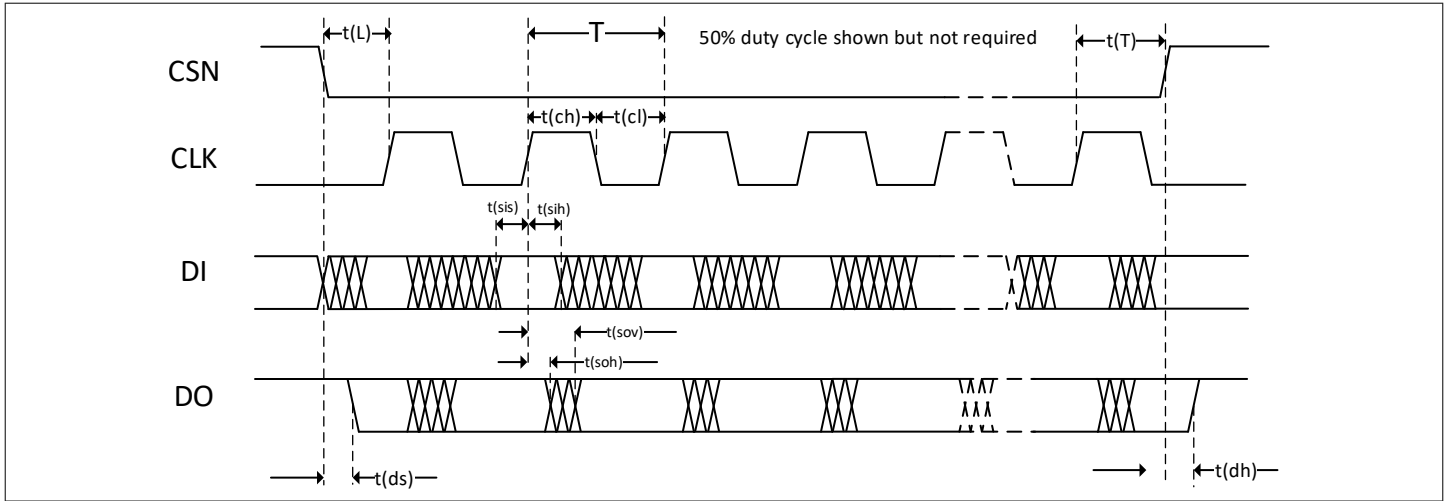
After the last bit has been transferred and CLK has gone to low level, the SPI master must set CSN to high level to stop the transfer. The master must take care that the period between the last rising edge of CLK and the rising edge of CSN is not shorter than  $t(T)$ . Within the period  $t(dh)$  after the rising edge of CSN the SPI slave drives DO to high impedance state again.



**Figure 23** SPI interface timing diagram for SFCTL:MISO\_HS\_RD = 0<sub>B</sub>

BGT60ATR24AIP can operate at SPI clock frequencies up to 50 MHz, but the maximum achievable SPI clock frequency is limited by DI related setup and hold times of SPI master and SPI slave. If for example the SPI master requires a longer setup time than  $T/2 - t(sov)$ , the SPI clock speed in normal SPI mode must be reduced. Alternatively, BGT60ATR24AIP can be switched to SPI high-speed mode by setting SFCTL:MISO\_HS\_RD = 1<sub>B</sub>.

The timing diagram for high speed SPI mode is presented in Figure 24. In this mode the SPI master is still supposed to capture the level of DO with the rising edge of CLK. The SPI slave keeps the level of DO stable for  $t(soh)$  after the rising edge of CLK, and then sets the level of DO according to the next bit which is send out.



**Figure 24** SPI interface timing diagram for SFCTL:MISO\_HS\_RD = 1<sub>B</sub>

**Table 26** SPI Timing Requirements

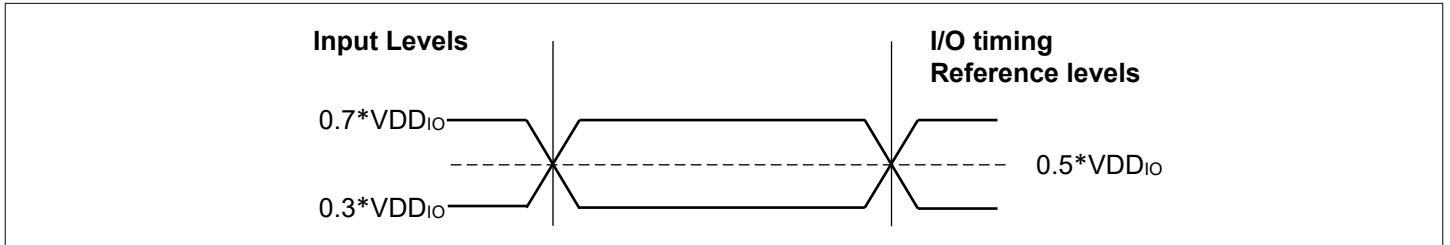
$VDD_{IO} = 1.71\text{ V to }3.465\text{ V}$ ,  $T_b = -40\text{ °C to }+105\text{ °C}$ .

| Parameter  | Symbol          | Values |      |      | Unit | Condition         |
|--|-----------------|--------|------|------|------|-------------------|
|  |                 | Min.   | Typ. | Max. |      |                   |
| SPI clock period: 50 MHz, with 1% clock jitter           | $T$             | 20     | -    | -    | ns   | -                 |
| Clock high   | $t(\text{ch})$  | 9.0    | -    | -    | ns   | -                 |
| Clock low  | $t(\text{cl})$  | 9.0    | -    | -    | ns   | -                 |
| Slave input setup  | $t(\text{sis})$ | 5.0    | -    | -    | ns   | -                 |
| Slave input hold   | $t(\text{sih})$ | 5.0    | -    | -    | ns   | -                 |
| Slave output valid                                       | $t(\text{sov})$ | -      | -    | 12.0 | ns   | see note          |
| Slave output hold  | $t(\text{soh})$ | 1.0    | -    | -    | ns   | -                 |
| Lead time before the first working clock edge occurs     | $t(\text{L})$   | 9.0    | -    | -    | ns   | -                 |
| Tailing time after the last working clock edge           | $t(\text{T})$   | 1      | -    | -    | ns   | -                 |
| Data setup time after the DO goes in low impedance state | $t(\text{ds})$  | -      | -    | 5    | ns   | Ensured by design |
| Data hold time before DO goes in hi impedance state      | $t(\text{dh})$  | -      | -    | 5    | ns   | Ensured by design |

- Note:**
- If SFCTL:MISO\_HS\_RD is not set properly then data read on MISO may not be correct
  - The timing is ensured for worst case condition:  $VDD_{IO} = 1.71\text{ V}$ ,  $T_b = +105\text{ °C}$ , output load of  $C_{load} = 50\text{ pF}$
  - Better conditions results in a much shorter  $t(\text{sov})$  time

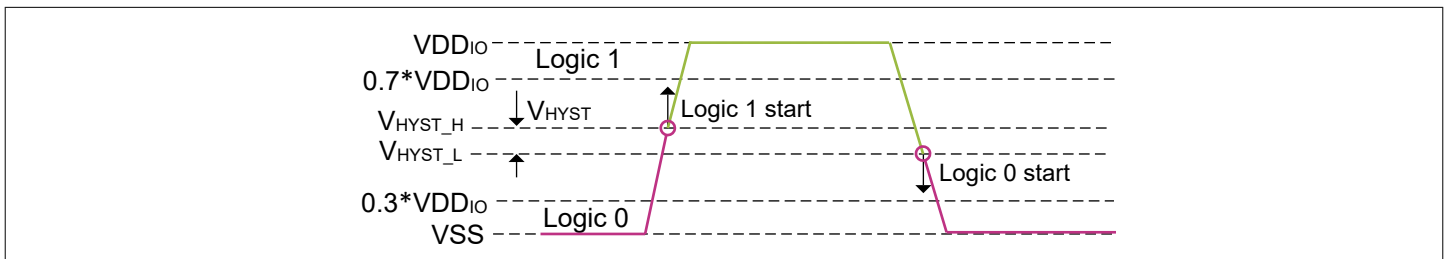
### 5.3.2 Logic levels

The digital inputs and outputs are fully *complementary metal-oxide semiconductor (CMOS)* compatible. All IO input/output timings are based on 50% voltage reference levels (see following figure). I/O interfaces are shown in [Figure 28](#) and [Figure 29](#), which include internal pull-ups.



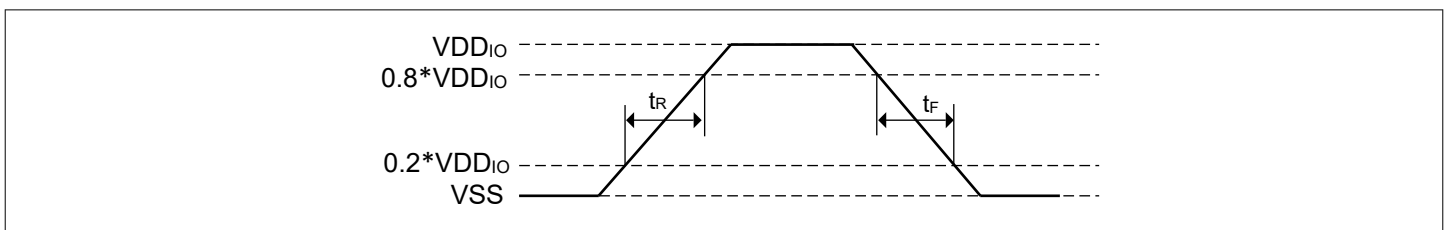
**Figure 25 AC timing input/output reference levels**

The input logic hysteresis prevents input buffers from oscillation. The minimum hysteresis range  $V_{HYST}$  is in between the lower ( $0.3 * VDD_{IO}$ ) and upper logic level ( $0.7 * VDD_{IO}$ ) boundaries (see [Figure 26](#)). Above  $0.7 * VDD_{IO}$  the input signal is a logical '1' while below  $0.3 * VDD_{IO}$  it is a logical '0' regardless of hysteresis. Due to temperature drifts and device variation the hysteresis range  $V_{HYST}$  can be up to  $0.7 * VDD_{IO}$  or down to  $0.3 * VDD_{IO}$  but typically around  $0.5 * VDD_{IO}$ . Parameters are reported in [Table 28](#).



**Figure 26 Logic input levels and hysteresis**

The digital output pads have a programmable output pad strength that gives a specific slew-rate for rising signals,  $dV_{TR}$ , and falling signals,  $dV_{TF}$  (see following figure). Minimum slew rates were simulated considering a total capacitive load of 15 pF. Results reported in [Table 29](#).



**Figure 27 Rise/fall time, slew rate specified between  $0.2 * VDD_{IO}$  and  $0.8 * VDD_{IO}$**

**Table 27 Logical Levels for Input Pins**

$VDD_{IO} = 1.71$  to  $3.465$  V,  $T_b = -40$  to  $+105$  °C, ambient temperature not below  $-40$  °C; all voltages with respect to  $VSS_{IO}$  digital ground, positive current flowing into pin (unless otherwise specified)

| Parameter | Symbol      | Values |      |                  | Unit | Condition |
|-----------|-------------|--------|------|------------------|------|-----------|
|           |             | Min.   | Typ. | Max.             |      |           |
| LOW level | $V_{IN(L)}$ | 0      | -    | $0.3 * VDD_{IO}$ | V    | -         |

(table continues...)

**Table 27 (continued) Logical Levels for Input Pins**

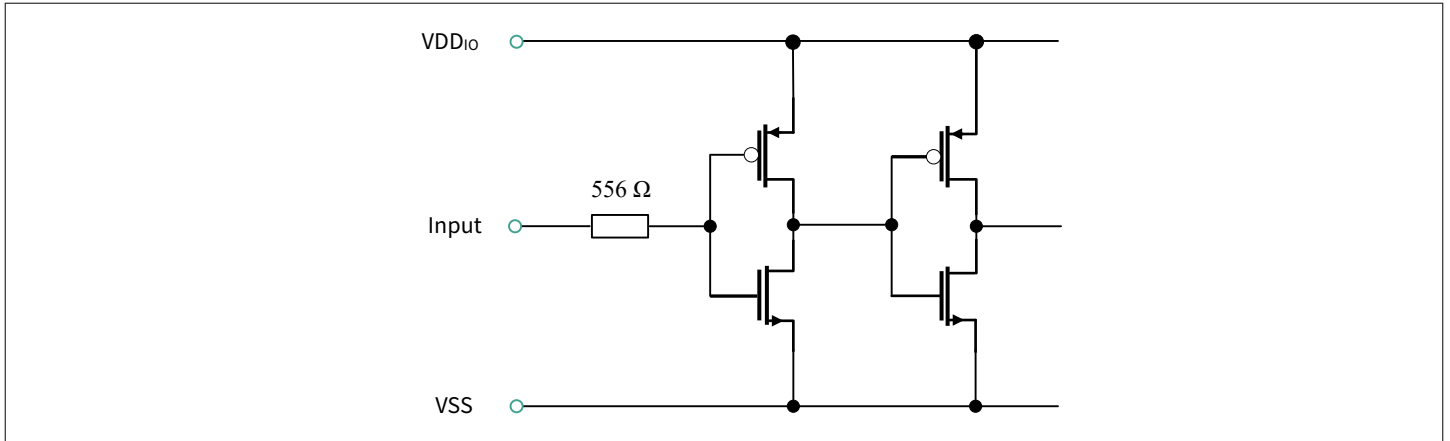
$V_{DDIO} = 1.71$  to  $3.465$  V,  $T_b = -40$  to  $+105$  °C, ambient temperature not below  $-40$  °C; all voltages with respect to  $V_{SSIO}$  digital ground, positive current flowing into pin (unless otherwise specified)

| Parameter  | Symbol        | Values           |                                 |                  | Unit | Condition                   |
|--|---------------|------------------|---------------------------------|------------------|------|-----------------------------|
|  |               | Min.             | Typ.                            | Max.             |      |                             |
| HIGH level   | $V_{IN(H)}$   | $0.7 * V_{DDIO}$ | -                               | $V_{DDIO}$       | V    | -                           |
| Input current ( $0 V < V_{IN} < V_{DDIO}$ )                                    | $I_{IN}$      | -150             | -                               | 150              | μA   | -                           |
| Input capacitance CLK/CSN  | $C_{IN}$      |                  | 2.0                             |                  | pF   |                             |
| Input capacitance DI/RST   | $C_{IN}$      |                  | 3.15                            |                  | pF   |                             |
| Minimum hysteresis voltage range between $0.3 * V_{DDIO}$ and $0.7 * V_{DDIO}$ | $V_{HYST}$    | 175              | -                               | -                | mV   | $V_{HYST\_H} - V_{HYST\_L}$ |
| Upper hysteresis signal level  | $V_{HYST\_H}$ | -                | $0.5 * V_{DDIO} + V_{HYST} / 2$ | $0.7 * V_{DDIO}$ | V    | -                           |
| Lower hysteresis signal level  | $V_{HYST\_L}$ | $0.3 * V_{DDIO}$ | $0.5 * V_{DDIO} - V_{HYST} / 2$ | -                | V    | -                           |

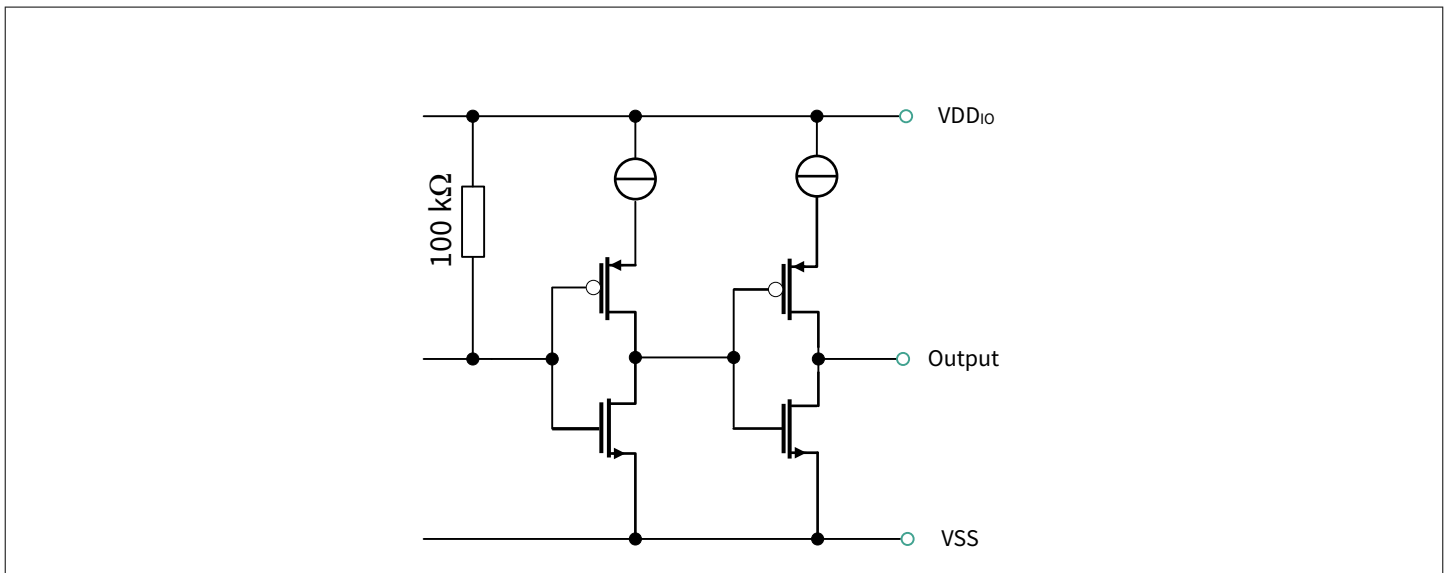
**Table 28 Logic Levels for Output Pins**

$V_{DDIO} = 1.71$  to  $3.465$  V,  $T_b = -40$  to  $+105$  °C, ambient temperature not below  $-40$  °C; all voltages with respect to  $V_{SSIO}$  digital ground, positive current flowing into pin (unless otherwise specified).

| Parameter  | Symbol       | Values           |      |                  | Unit | Condition                            |
|--|--------------|------------------|------|------------------|------|--------------------------------------|
|  |              | Min.             | Typ. | Max.             |      |                                      |
| LOW level  | $V_{OUT(L)}$ | 0                | -    | $0.3 * V_{DDIO}$ | V    | -                                    |
| HIGH level   | $V_{OUT(H)}$ | $0.7 * V_{DDIO}$ | -    | $V_{DDIO}$       | V    | -                                    |
| Output current (LOW)   | $I_{OUT(L)}$ | -                | -    | -5               | mA   | -                                    |
| Output current (HIGH)  | $I_{OUT(H)}$ | -                | -    | 5                | mA   | -                                    |
| Allowed load capacitance to provide maximum signal frequency on DO | $C_{LOAD}$   | -                | -    | 15               | pF   | -                                    |
| Output pad slew rate for rising wave form                          | $dV_{TR}$    | 0.32             | -    | -                | V/ns | $0.2 * V_{DDIO}$ to $0.8 * V_{DDIO}$ |
| Output pad slew rate for falling wave form                         | $dV_{TF}$    | 0.33             | -    | -                | V/ns | $0.2 * V_{DDIO}$ to $0.8 * V_{DDIO}$ |



**Figure 28** Interface for input pins



**Figure 29** Interface for output pins

### 5.3.3 Overshoot and undershoot waveform definition

During operation, the applied signals and supply levels should not exceed absolute maximum *direct current (DC)* levels specified in datasheet. Digital signals can have positive or negative overshoots due to inductive and/or capacitive loads. [Table 29](#) reports the allowed overshoot signal levels for all logic signals.

**Table 29** Overshoot and undershoot signal levels

| Parameter                                 | Symbol   | Values |      |                           | Unit | Condition |
|---|----------|--------|------|---------------------------|------|-----------|
|   |          | Min.   | Typ. | Max.                      |      |           |
| Maximum absolute overshoot voltage level  | $V_{os}$ | -      | -    | $VDD_{IO} + 0.5\text{ V}$ | V    | see note  |
| Maximum absolute undershoot voltage level | $V_{us}$ | -      | -    | $VSS_{IO} - 0.5\text{ V}$ | V    | see note  |

**Note:** Maximum pad current not exceeding  $\pm 5\text{ mA}$  (see also [Chapter 5.3.2](#)). No slew rate limitation existing on digital signals for overshoots/undershoots.

### 5.3.4 IBIS model

A BGT60ATR24AIP *Input/output Buffer Information Specification (IBIS)* model is available under *non-disclosure agreement (NDA)* upon request. It is based on timing simulations. In order to better reflect the real timing behavior, different pad models for input/output signals are used and summarized in the following table. The driver strength and the pull-up can be modified via registers.

**Table 30 IBIS Pad types and models (see IBIS model)**

| Pin  | Ibis PAD Model                      |
|------|-------------------------------------|
| CSN  | IN: Selection_1                     |
| CLK  | IN: Selection_1                     |
| DI   | IN: Selection_2                     |
| DIO0 | OUT: Selection_2                    |
| DO   | IN: Selection_2                     |
| DIO1 | OUT: Selection_2                    |
| DIO2 | IN: Selection_2<br>OUT: Selection_2 |
| RST  | IN: Selection_2                     |
| DIO3 | OUT: Selection_2                    |
| IRQ  | OUT: Selection_0                    |

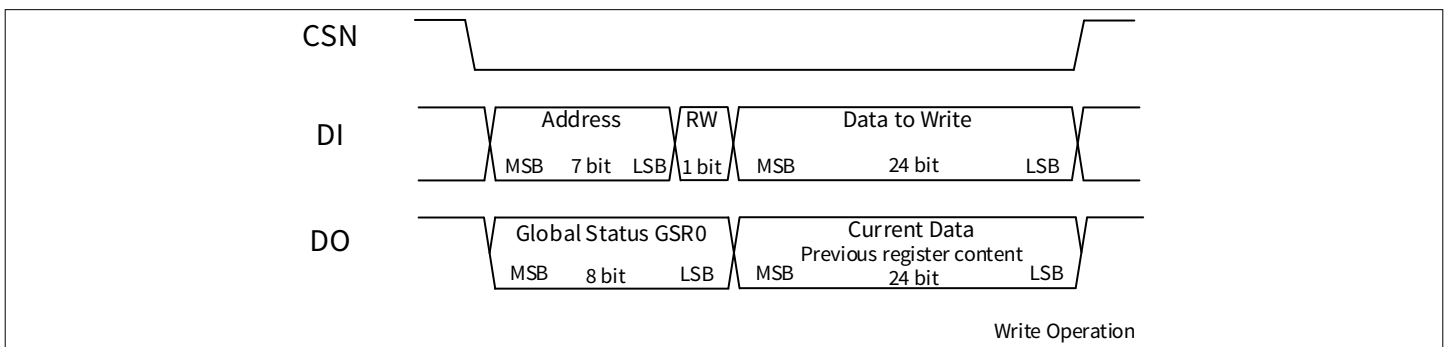
### 5.3.5 SPI functionality

Each word transferred over the *SPI* bus has a length of 1 command byte + 3 data Bytes. The communication is done bitwise. First the address is transferred with *most significant bit (MSB)* first. The address is followed by the R/W-bit and then followed by the data which is sent MSB first, too. At the same time, while command byte is received, a freely from system level configurative global status register (8 bits, GSR0) is serial shifted out on DO (MSB first). On the following 24 clock cycles the selected register content is shifted out on DO, MSB first.

Depending on sent R/W-bit there are two different operation modes available, the write mode and the read mode. Every write mode is a read mode too.

#### Write mode

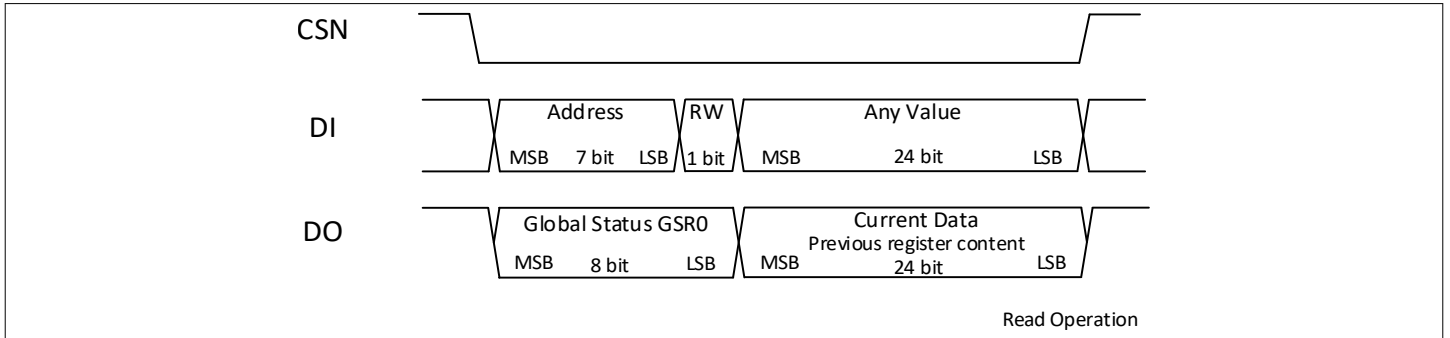
After the start condition the desired address is sent. The address is 7 bits long followed by a bit that is a data direction bit (read/write). A one indicates a write operation (see following figure).



**Figure 30 SPI timing write mode**

**Read mode**

After the start condition, the desired address is sent like in the write operation. A zero of the R/W-bit indicates a read access. The data on DI after the command byte may contain any value. The DO behavior is the same as in write mode.



**Figure 31 SPI timing read mode**

**5.3.6 SPI burst mode**

The burst mode can be used to read or write out several registers or some data from the *SPI* instead of reading just single registers or data. The burst mode command is sent by the host. The burst mode command consists of several bit fields and is shown in the following table.

|                |    |    |    |    |    |    |             |              |    |    |    |    |    |    |            |
|----------------|----|----|----|----|----|----|-------------|--------------|----|----|----|----|----|----|------------|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24          | 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| <b>ADDR</b>    |    |    |    |    |    |    | <b>RW</b>   | <b>SADDR</b> |    |    |    |    |    |    | <b>RWB</b> |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8           | 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| <b>NBURSTS</b> |    |    |    |    |    |    | <b>RSVD</b> |              |    |    |    |    |    |    |            |

| Field   | Bits  | Description  |
|---------|-------|--|
| RSVD    | 8:0   | <b>Reserved</b>  |
| NBURSTS | 15:9  | Number of processed data blocks:<br>$0_H \dots$ "unbounded" burst accesses<br>$1_H \dots 7E_H \dots$ number of words to transfer   |
| RWB     | 16    | Burst read or write:<br>$0_B \dots$ Perform a read burst<br>$1_B \dots$ Perform a write burst, (writes to <i>FIFO</i> not supported)   |
| SADDR   | 23:17 | Starting address where the burst starts processing:<br>$< 64_H$ Register access<br>$= 64_H$ FIFO access<br>$> 64_H$ Reserved<br>Address is incremented automatically inside a burst. |
| RW      | 24    | Read/Write register access:<br>$1_B \dots$ write to address $7F_H$   |

**(table continues...)**

(continued)

| Field | Bits  | Description   |
|-------|-------|---|
| ADDR  | 31:25 | To enter the burst mode the following address is used:<br>7F <sub>H</sub> ... request the burst read/write. |

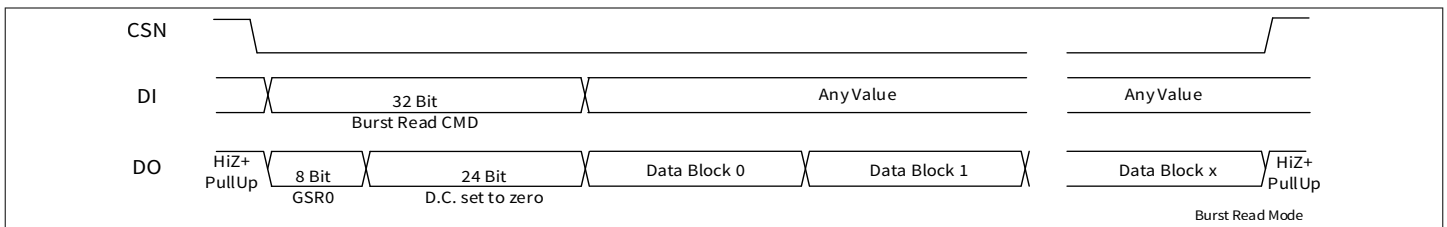
**Note:** A single data block is 24 bits width for both, the sampling memory and the registers.

**Burst mode operation**

After the start condition the 32 bits burst mode command is sent from the SPI master on DI. At the same time, the status register GSR0 (four 1<sub>B</sub> bits + four status bits) followed by 24 padding bits set to 0<sub>B</sub> is shifted out on DO. After the command sequence is done, the register/FIFO data is shifted out to the SPI master on DO. In burst write mode, the register data to be written is shifted in from the SPI master (application processor e.g.).

**Burst mode read sequence**

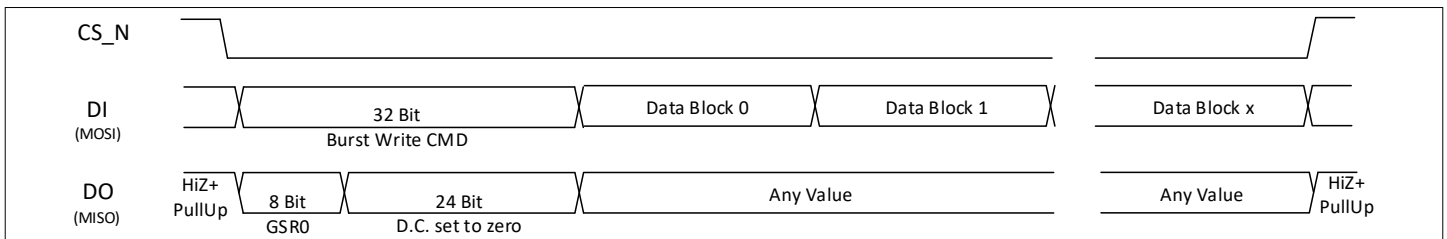
In the read sequence, the SPI master reads from the device.



**Figure 32** Burst mode read sequence

**Burst mode write sequence**

In the burst write mode, the SPI master writes to the device.

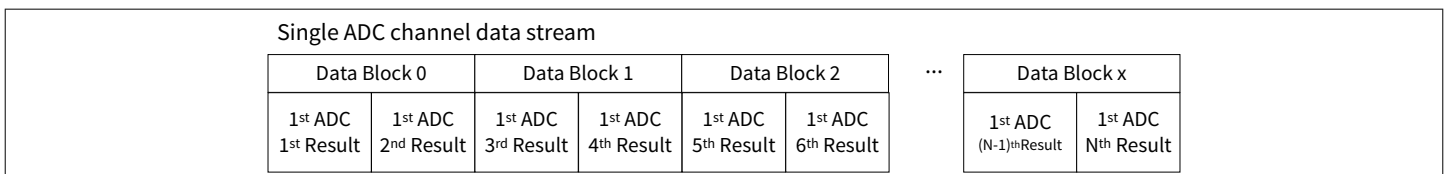


**Figure 33** Burst mode write sequence

**Sampling data arrangements in data blocks**

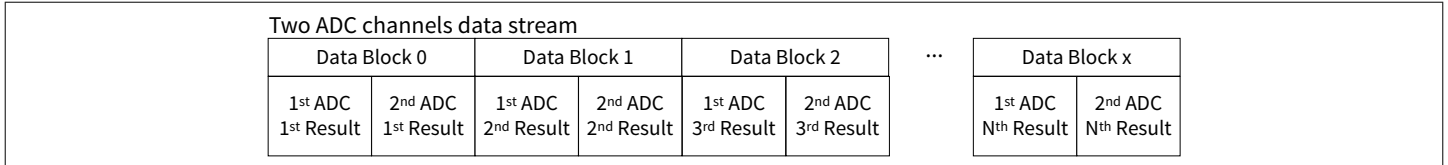
The data from the FIFO are streamed out during the burst read request, starting from the FIFO address zero. The 1<sup>st</sup> ADC is the ADC channel with the lowest channel number. As far as the sampling memory is organized in 24 bits and up to 4 ADC channels are selectable through the ADC channel selection bits (CSx:MADC\_BBCH\_SEL, see [Channel set up x register 1](#)) the data blocks are arranged as follows.

In case a single ADC is selected the data blocks are shown in the following figure.



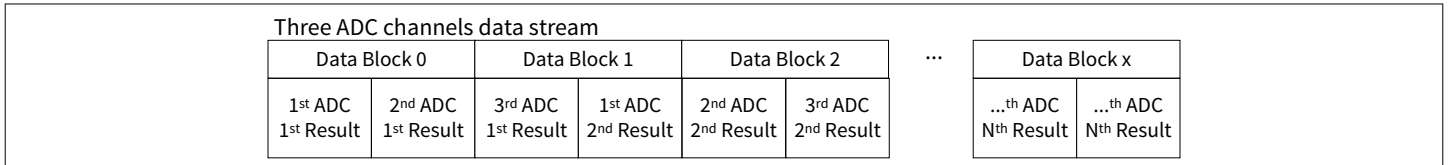
**Figure 34** Single ADC channel selected

In case two ADC are selected the data blocks are arranged as shown in the following figure.



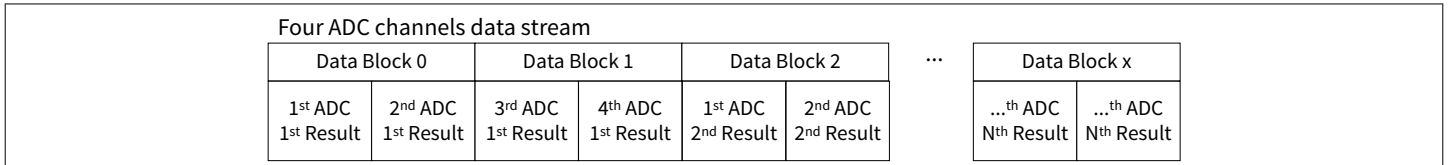
**Figure 35 Two ADC channels selected**

In case three ADC are selected the data blocks are arranged as shown in the following figure.



**Figure 36 Three ADC channels selected**

In case four ADC are selected the data blocks are arranged as shown in the following figure.



**Figure 37 Four ADC channels selected**

**Example: Burst mode read sampling memory sequence**

The following burst mode command is sent from the host to initialize the burst mode to read from the FIFO an undefined number of sampling data:

- BMCMD\_RS = (ADDR = 7F<sub>H</sub>, RW = 1, SADDR = 64<sub>H</sub>, RWB = 0, NBURSTS = 0<sub>H</sub>)

Remark: For each burst read request to the sampling memory, the sampling-memory address pointer is reset to the initial value. So that memory can be read out from the beginning until the application processor stops burst reading.

**Example: Burst mode read registers sequence**

The following burst mode command is sent from the host to initialize the burst mode to read out 10 registers starting from register address 3:

- BMCMD\_RR10 = (ADDR = 7F<sub>H</sub>, RW = 1, SADDR = 3<sub>H</sub>, RWB = 0, NBURSTS = A<sub>H</sub>)

**5.3.7 Quad SPI Mode**

The serial peripheral interface is also capable to run in quad serial peripheral interface mode. For this the four pins DI, DO, DIO2, RST are used for DIO0, DIO1, DIO2, DIO3.

To access the quad serial peripheral interface mode the DIO3 pin must be pulled down together with the CSN pin.

Only one command (undefined length BURST READ) is supported which requires only the start address. Either a register or the first in first out address can be used as start address. During this BURST READ with undefined length the provided address is incremented internally.

Following is supported:

- burst read of registers
- burst read of memory
- burst read of both (mixed mode)

**Table 31** QSPI Protocol (Slave)

| Pin  | Command |       | Wait (min. 2 cycles) |  | Data   |        |        |        |        |
|------|---------|-------|----------------------|--|--------|--------|--------|--------|--------|
|      | input   | input |                      |  | output | output | output | output | output |
| DIO0 | C4      | C0    |                      |  | D4     | D0     | D4     | D0     | ...    |
| DIO1 | C5      | C1    |                      |  | D5     | D1     | D5     | D1     |        |
| DIO2 | C6      | C2    |                      |  | D6     | D2     | D6     | D2     |        |
| DIO3 | C7      | C3    |                      |  | D7     | D3     | D7     | D3     |        |

**Note:** The command (instruction) phase of quad SPI is used for the start address decoding (1 byte). Any further command bytes or alternative command phases of the SPI master need to be skipped with wait cycles. The wait cycles itself require a SPI clock and its number can be programmed via a register (minimum 2 clock cycles to change the pin direction from input to output). The MSB C7 must be always 0<sub>B</sub> as any address above the first in first out address is reserved.

### 5.3.8 SPI error detection

SPI\_BURST\_ERROR and CLK\_NUM\_ERROR (see [FIFO status register](#)) will be cleared after these resets:

- *software (SW)* reset
- *hardware (HW)* reset

SPI\_BURST\_ERROR, CLK\_NUMBER\_ERROR and FOU\_ERROR are reported in the global status bits (GSR0) of the **next SPI** transaction and latched as sticky bits in the FSTAT register.

In order to understand if the captured sample data are corrupted, the host can evaluate the bit field CLK\_NUM\_ERR and SPI BURST\_ERR as reported in the following table.

**Table 32** SPI BURST\_ERR and CLK\_NUM\_ERR Definitions

| Length Range | Transaction                              | SPI BURST_ERR  | CLK_NUM_ERR    | Behavior on read/write             |
|--------------|--|----------------|----------------|------------------------------------|
| 0            | Null command                             | 0 <sub>B</sub> | 0 <sub>B</sub> | Ignored                            |
| 1-31         | Short length error in single             | 0 <sub>B</sub> | 1 <sub>B</sub> | Command ignored                    |
| >32          | Long length error in single              | 0 <sub>B</sub> | 1 <sub>B</sub> | Extra bits ignored                 |
| 1-31         | Short length error in SPI burst header   | 0 <sub>B</sub> | 1 <sub>B</sub> | Command ignored                    |
| <24xN        | Missing whole data word in bounded burst | 1 <sub>B</sub> | 0 <sub>B</sub> | Available data words used          |
| >24xN        | Extra whole data word in bounded burst   | 1 <sub>B</sub> | 0              | Extra data word(s) ignored         |
| %24>0        | Misaligned bit-count for bounded burst   | 1 <sub>B</sub> | 1 <sub>B</sub> | Extra bits ignored                 |
| %24>0        | Misaligned bit-count for infinite burst  | 0 <sub>B</sub> | 1 <sub>B</sub> | Partial data word may be discarded |

- Note:**
- Ignored write transaction means that no register (or memory) content is affected by the partial write command, or incomplete data word.
  - Ignored read transaction means that the returned data is invalid, and for the **FIFO** no words are removed by the partial read command, or incomplete data word.
  - Discarded read transaction means that the data is already read from the FIFO but only partially transferred; subsequent read pops next word from FIFO.
  - Data from the FIFO may be discarded after a length error in the infinite burst ( $NBURST=0$ ) occurs. The FIFO read has to happen, since at that stage the data is required to be shifted out, but if not all bits are shifted out the FIFO is already read and the partial data word may be discarded.

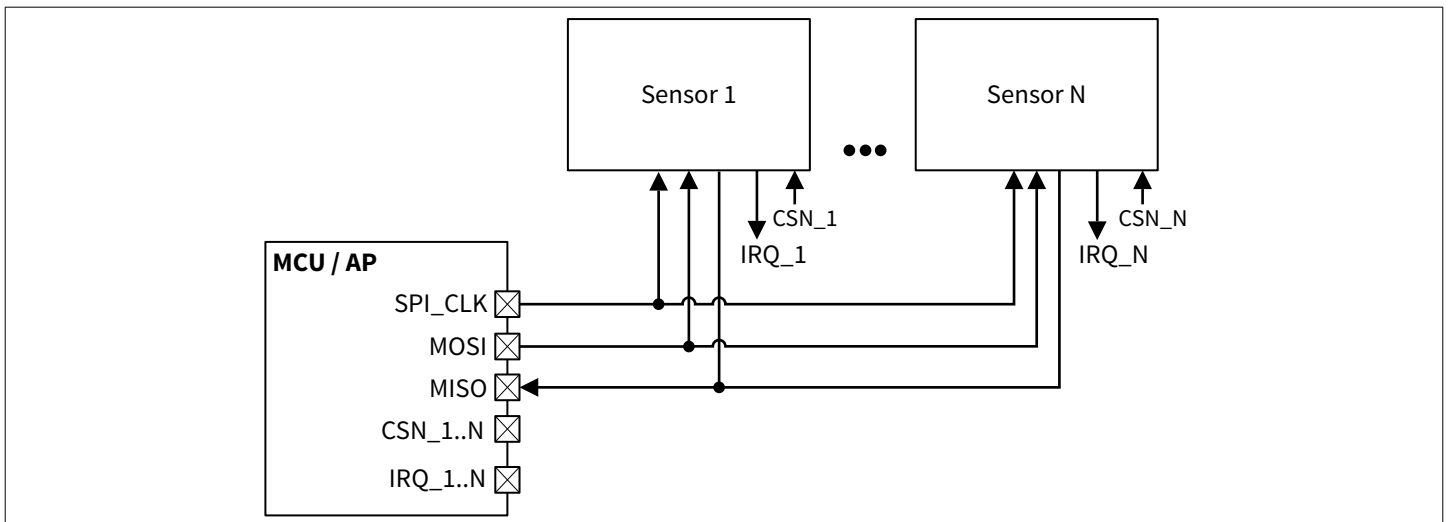
### 5.3.9 SPI broadcast mode

BGT60ATR24AIP comes with a special **SPI** feature called broadcast mode. This mode gives the user the capability to program multiple radar sensors which shares the same SPI bus.

To avoid driver conflicts of contradictory logic levels on the shared **MISO** line the SPI broadcast mode deactivates the output driver of the DO pin. This change becomes active with the rising edge of CS after `MAIN:SPI_BC_MODE` is programmed to  $1_B$ . The deactivation of this mode is done in a similar way by programming `MAIN:SPI_BC_MODE` to  $0_B$  which activates the output driver of the DO pin again with the rising edge of CS.

There are two main use cases to benefit from this SPI broadcast mode:

- To speed up initial radar sensors configuration by programming all devices at the same time
- To synchronize multiple radar sensors by triggering a frame at the same time (single SPI write command with `MAIN:FRAME_START = 1_B`)



**Figure 38** SPI broadcast block diagram

A SPI broadcast system with multiple sensors (e.g. sensor 1, sensor 2 ...) shares the same SPI bus including SPI clock (`SPI_CLK`), data input and output (`MOSI`, `MISO`) and maybe also the same oscillator clock (`OSC_IN`). However, each sensor requires an own chip select (`CSN`) pin on the SPI master (e.g. `MCU, AP`) side to enable individual control over each sensor. Also a dedicated interrupt input pin is needed on SPI master side for each sensor interrupt output (`IRQ`).

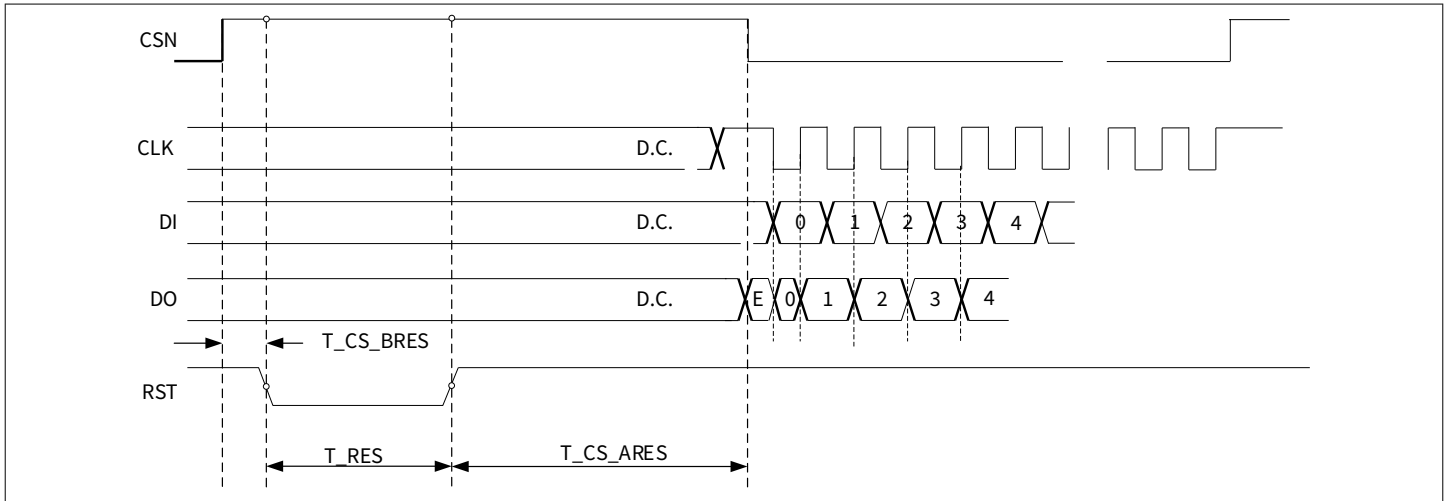
### 5.4 Hardware reset sequence

In order to perform a proper device reset, a special reset sequence is required. For example, after a device power-up according to [Wake-up phase from “deep sleep” to “idle”](#).

While `CSN` is =  $1_B$  RST must perform a  $1_B 0_B 1_B$  transition

The behavior is presented in the following figure with:

- $T_{CS\_BRES} = 100 \text{ ns}$
- $T_{RES} = 100 \text{ ns}$
- $T_{CS\_ARES} = 100 \text{ ns}$



**Figure 39** Hardware reset sequence

## 5.5 Software triggered resets

Besides the hard reset, three reset sequences are supported and can be triggered in the MAIN register (see also [Main register](#)). They are defined according to the following hierarchy:

- *SW* reset -> *FIFO* reset -> *FSM* reset

### Software reset

- Resets all registers to default state
- Resets all internal counters (shape, frame e.g. )
- Perform FIFO reset
- Performs FSM reset
- A delay of 100 ns after the SW reset is needed before the next *SPI* command is sent

### FIFO reset

- Reset the read and write pointers of the FIFO
- Array content will not be reset, but cannot be read out
- FIFO empty is signaled, filling status = 0<sub>D</sub>
- Resets register FSTAT FIFO status register
- Performs an implicit FSM reset

### FSM reset

- Resets FSM to DS power mode
- Resets FSM internal counters for channel/shape set and timers
- Resets Status register 0 and Status register 1 register
- Reset *PLL* ramp start signal
- Reset PA\_ON
- Terminates frame (shape and frame counters incremented although maybe not complete)

## 6 PLL domain functional specification

The *PLL* is designed to generate high performance frequency chirps in the range of 57.7 GHz to 62.4 GHz. The modulation is performed inside the PLL bandwidth (in-band-modulation) with an analog charge pump based fractional-N RF-PLL architecture. It furthermore features a shape generator with high flexibility to allow different ramp shapes and duration times. The loop requires a low noise reference clock with a nominal frequency of SYS\_CLK.

### 6.1 PLL interfaces and clock distribution

Figure 40 shows the interfaces to the *PLL* and the distribution of the internal system clock.

Supported are two different external oscillator input clock frequency ranges  $f_{OSC\_IN\#1}$  and  $f_{OSC\_IN\#2}$ , which requires different settings of the PLL and the correct configuration of the clock input stages DC\_IN (see Clock input register). Each clock-input stage consists of multiplexers for path selection and a selectable frequency doubler. In addition to this, the clock input-stage for the system includes different correction and adjustment options used for the frequency doubling DC\_OUT (see Clock input register).

In case of  $f_{OSC\_IN\#1}$  the register bits CLK\_IN:CLK\_SEL should be set to  $0_D$ , for  $f_{OSC\_IN\#2}$  the register bits CLK\_SEL should be set to  $1_D$  in order to use only the clock frequency doubler (see Clock input register).

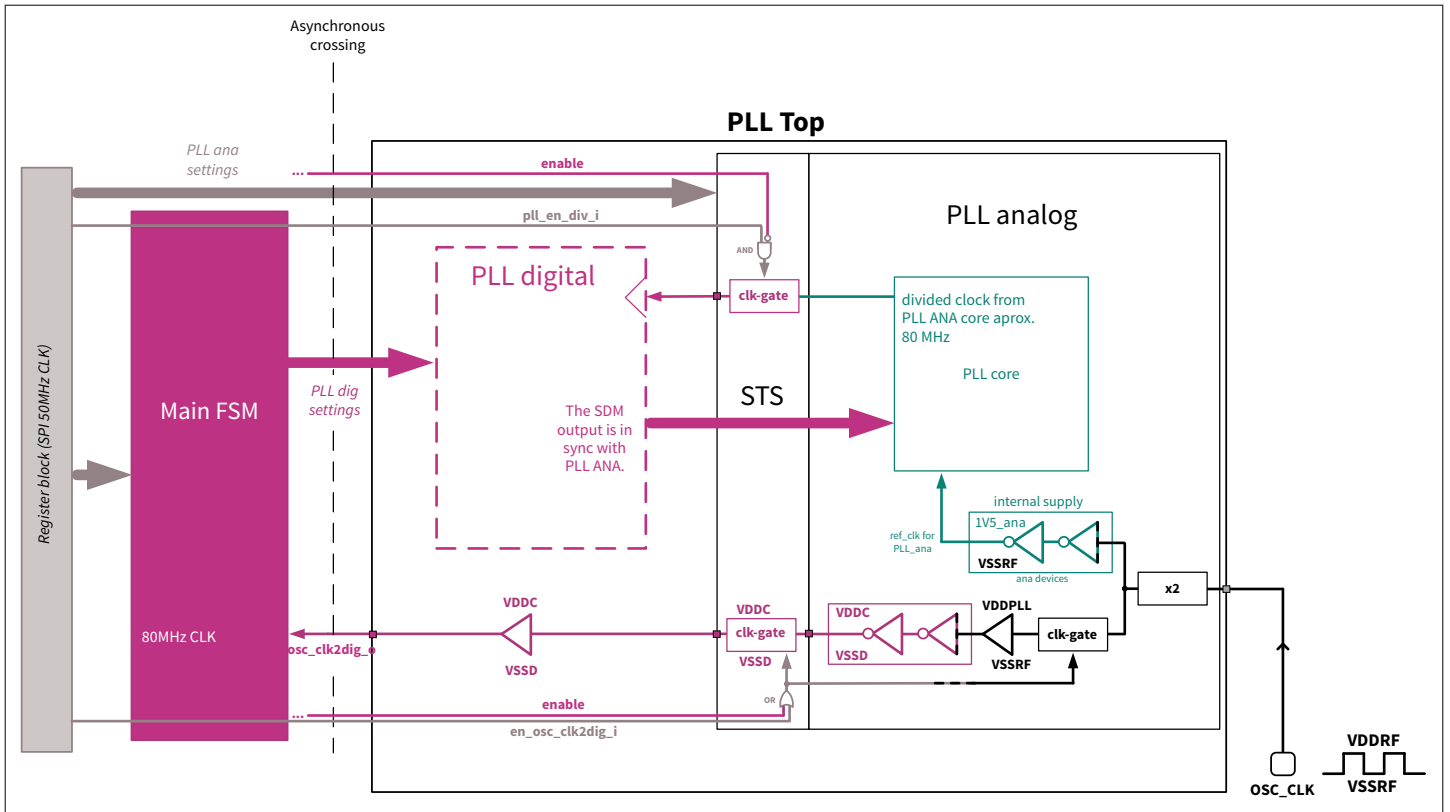
The frequency doubler correction and adjustment options are the following:

- CLK\_IN:CLK\_SEL =  $1_D$ : enables both frequency doublers without an input duty cycle adjustment
- CLK\_IN:CLK\_SEL =  $2_D$ : enables frequency doubling with an input duty cycle adjustment via the bits CLK\_IN:DC\_IN\_ADJ. This adjustment is applied to the input clock. The corrected clock is then the input to both duty cycle dependent frequency doublers (PLL and system clock)
- CLK\_IN:CLK\_SEL =  $3_D$  enables the frequency doubling but only uses the input duty cycle correction for the frequency doubler that generates the system clock

For the case the frequency doubler is used (CLK\_IN:CLK\_SEL  $\geq 1_D$ ) the duty cycle of the generated doubled clock can be modified with the bits CLK\_IN:DC\_OUT\_ADJ to a value close to 50%. This adjustment only applies to the system clock as the PLL only requires a minimum duty cycle for the reference clock, which is ensured by design.

#### 6.1.1 Reference clock distribution

The external reference clock signal is provided via a short, low jitter path directly to the clock input port of the *PLL* analog part (PLL analog). Inside the PLL analog part the clock path is split and goes to two different clock input-stages. One stage is dedicated to the PLL and is under the internally regulated low noise supply of the PLL. The second input stage is used to provide the system clock through the *simplified timing shell (STS)* to the output of the PLL macro (osc\_clk2dig). The STS is a defined timing interface between the PLL analog and the digital part. Since osc\_clk2dig serves as the clock for the main *FSM* it must have an independent path to ensure availability even when the PLL is put into power down. Therefore, the usage of supplies generated inside the PLL is avoided for this path. The main FSM clock can be gated via a dedicated register bit called PACR1:OSCCLKEN (see PLL analog control register 1) which gates the clock path already at its beginning.



**Figure 40** PLL and SYS\_CLK interface to the main FSM

### 6.1.2 Interfaces to the PLL

Most static settings and control signals dedicated to the analog part of the *PLL* are treated as asynchronous signals and are passed from the register bank to the *STS* of the *PLL*. This applies to digital signals that are not timing critical. Ramp generation parameters provided from the main *FSM* to the digital part of the *PLL* are registered inside the *PLL* digital. The start signal of the ramp also acts as a synchronization signal of the ramp parameters. This is required since the *PLL* digital runs on the divided clock of the *PLL* which ensures a known and synchronous timing relation between the sigma-delta bit stream and the analog part of the *PLL* that realizes the ramping behavior. The divided clock is only available if the *PLL* macro and the *voltage controlled oscillator (VCO)* are activated. Other control signals from *PLL* digital to the analog part are kept asynchronous. In order to close the *PLL* loop the analog part of the *PLL* core has interfaces to the *RF* macro where the *VCO* and a part of the divider chain are located.

## 6.2 PLL parameters and specification

The following table summarizes the target parameters of the *PLL* based frequency generator.

**Table 33** PLL specifications

$VDD_{PLL} = 1.71$  to  $1.89$  V,  $VDD_{LF} = 2.5$  to  $3.63$  V,  $T_b = -40$  °C to  $+105$  °C.

| Parameter                   | Symbol   | Values |      |      | Unit | Condition                             |
|-----------------------------|----------|--------|------|------|------|---------------------------------------|
|                             |          | Min.   | Typ. | Max. |      |                                       |
| <b>PLL Chirp Parameters</b> |          |        |      |      |      |                                       |
| Output Frequency Range      | $f_{RF}$ | 57.7   | -    | 62.4 | GHz  | Range depends on the $VDD_{LF}$ value |

(table continues...)

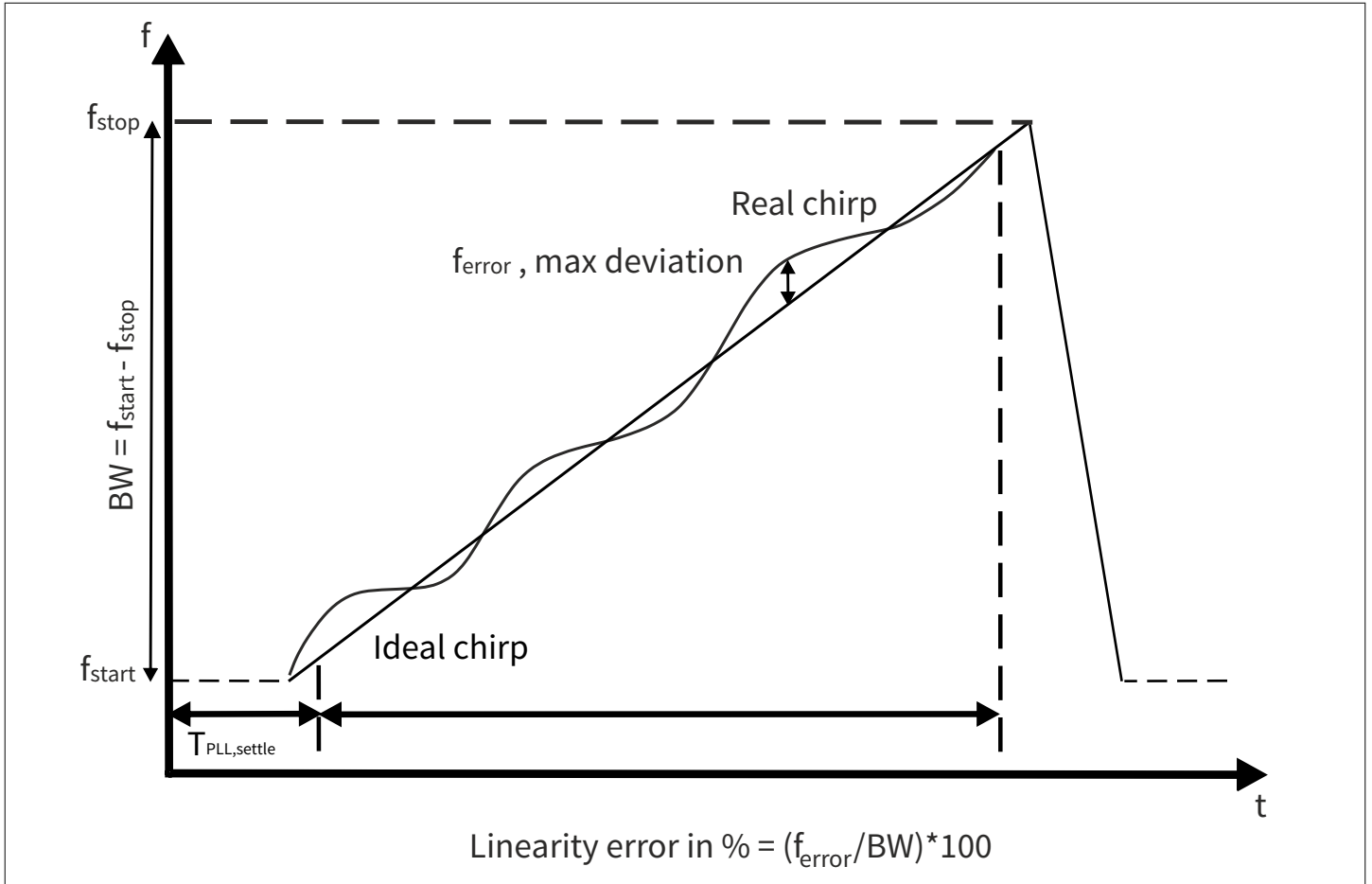
**Table 33 (continued) PLL specifications**

$VDD_{PLL} = 1.71$  to  $1.89$  V,  $VDD_{LF} = 2.5$  to  $3.63$  V,  $T_b = -40$  °C to  $+105$  °C.

| Parameter   | Symbol              | Values |      |      | Unit         | Condition  |
|---|---------------------|--------|------|------|--------------|--|
|   |                     | Min.   | Typ. | Max. |              |  |
| Continuous FM-Chirp Bandwidth                               | $BW$                | 0      | -    | 4.7  | GHz          | PLL tuning range   |
| $VDD_{LF}$ Range  | $VDD_{LF}$          | 2.5    | -    | 3.63 | V            | Complete specified $BW$ requires at least $VDD_{LF} = 3.3$ V |
| Chirp slope   | Slope               | -      | -    | 400  | MHz/ $\mu$ s | -  |
| Frequency Ramp Linearity Error                              | Error               | -      | -    | 1    | %            | For 2 GHz $BW$ minimum<br>See <a href="#">Figure 41</a>      |
| Frequency Ramp Settling Time<br>(fast chirp feature active) | $t_{PLL, settle}$   | -      | 5    | -    | $\mu$ s      | See <a href="#">Figure 42</a>                                |
| PLL Phase Noise Single Sideband                             | $PN_{PLL}, 100$ kHz | -      | -80  | -70  | dBc/Hz       | at 100 kHz offset  |

### 6.2.1 Frequency ramp linearity definition:

Frequency ramp linearity error is defined to be < 1% of the *frequency-modulated (FM)* chirp bandwidth. The linearity error is calculated as the deviation from an “ideal” frequency ramp. The specification needs to be fulfilled after the frequency ramp settling time (see also [Chapter 3.3](#)). The assumed worst-case FM chirp bandwidth for linearity evaluations is 2 GHz.

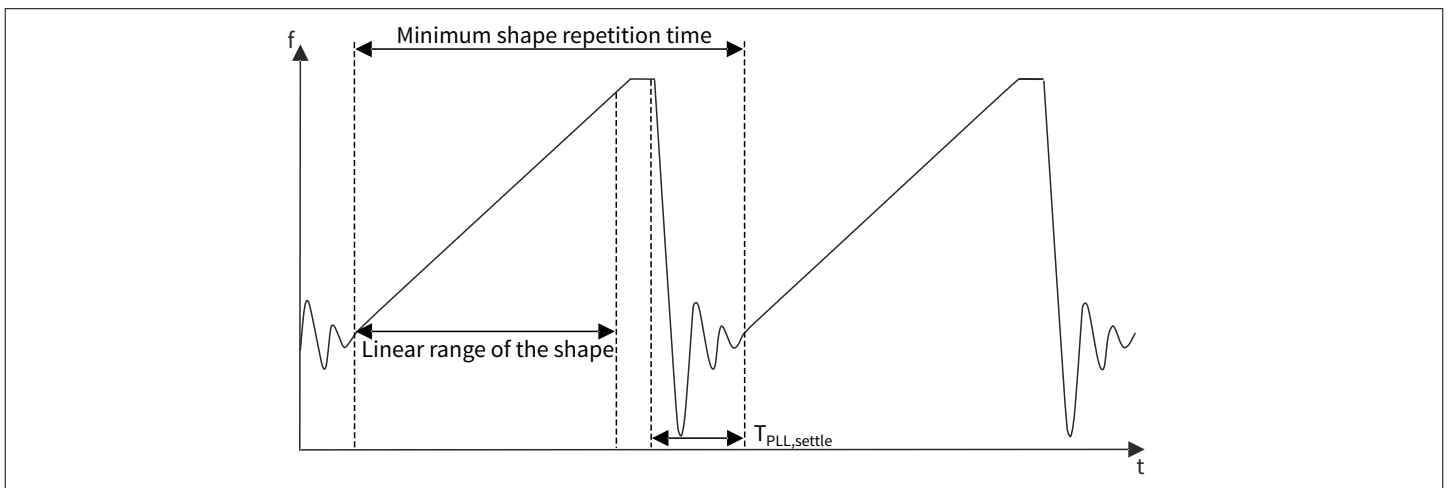


**Figure 41** Frequency linearity definition

The max frequency error expected, assuming 2 GHz minimum *BW* and a max deviation of 1%, will be 20 MHz.

### 6.2.2 Frequency ramp settling time

It is the time required by the *PLL* to damp undershoot and overshoot in case of saw-tooth shapes. A qualitative view is shown in the following figure. See [Chapter 3.3](#) for a more detailed definition of the timings.

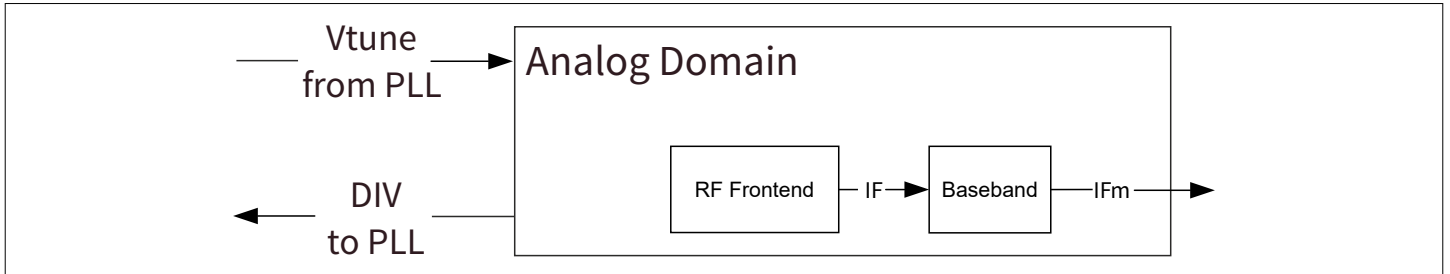


**Figure 42** Chirp settling time

## 7 Analog-RF domain functional specification

In the analog functional specification all analog components like *RF* frontend (RF FE), baseband amplifiers, and filters are described in more details.

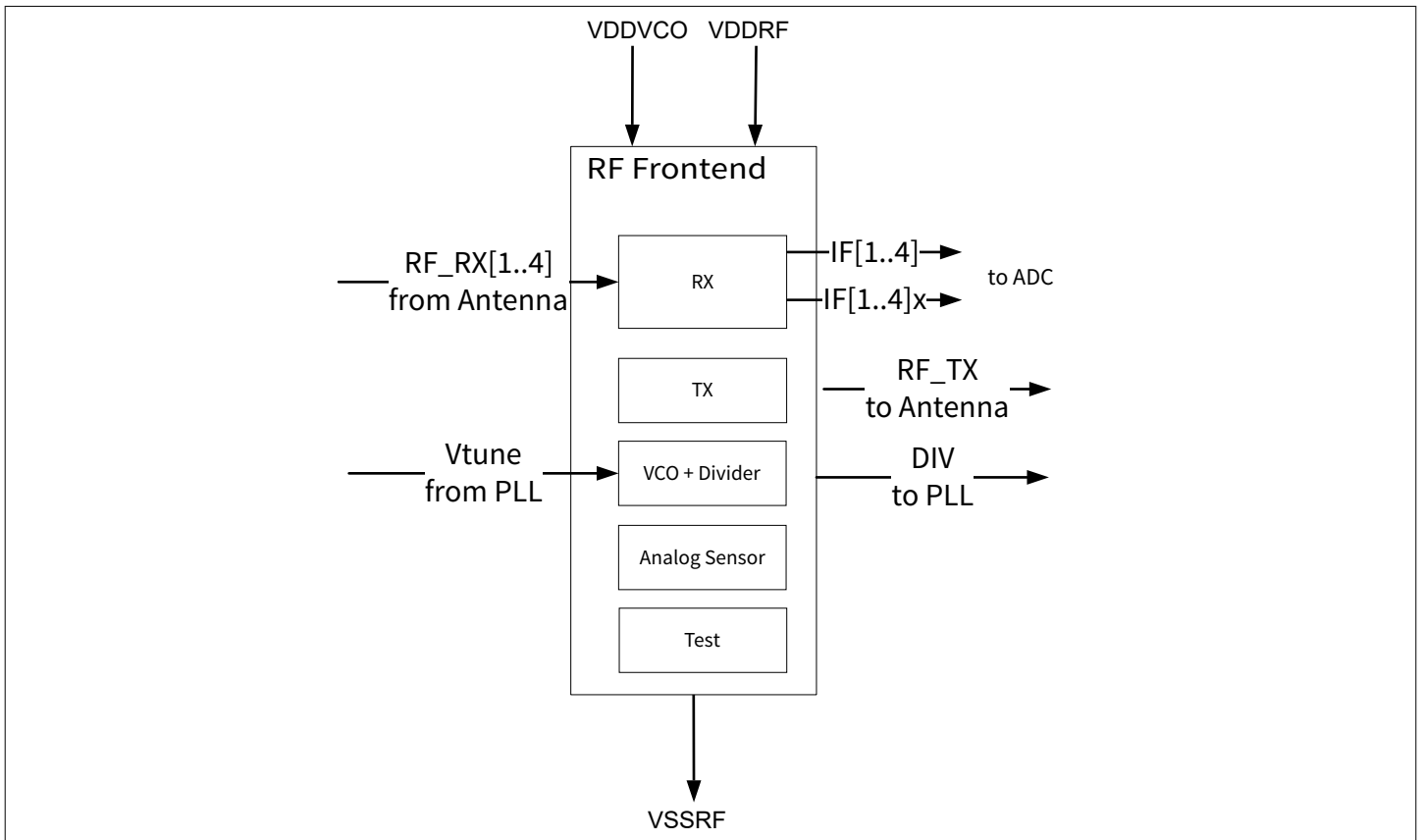
The register definitions for the components are in [Channel set up x register 0](#).



**Figure 43** Analog domain simplified block diagram

### 7.1 RF frontend (RF FE)

In the *RF* frontend, all features to enable the radar functionality are implemented.



**Figure 44** Simplified block diagram of transceiver frontend

#### 7.1.1 On-chip analog sensor output

The analog sensor outputs are connected to the SADC. See [Sensor ADC control register](#) for the SADC input configuration. See [Channel set up x register 0](#) for enable pins definition.

## 7.1.2 RF FE specifications

In the table below the target specifications for the *RF* frontend measured at die PAD interface.

**Table 34 RF FE specifications**

Min and max values cover the specified frequency range,  $f_{RF} = 57.7$  GHz to 62.4 GHz. Temperature range,  $T_b = -40$  °C to +105 °C, and voltage supply range,  $VDD_{RF} = 1.71$  V to 1.89 V (unless otherwise specified).

| Parameter       | Symbol   | Values |      |      | Unit | Condition |
|-----------------|----------|--------|------|------|------|-----------|
|                 |          | Min.   | Typ. | Max. |      |           |
| Frequency Range | $f_{RF}$ | 57.7   | -    | 62.4 | GHz  | -         |

### Transmitter

|  |                |      |     |     |      |                                   |
|--|----------------|------|-----|-----|------|-----------------------------------|
| Transmit Output Power <sup>1)</sup>      | $P_{TX}$       | -    | 4.0 | -   | dBm  | Conducted power                   |
| Output Power Variation over Temperature  | $P_{TX\_Temp}$ | -2.0 | -   | 2.0 | dB   | For TX DAC set to 31 <sub>D</sub> |
| Transmitter Power Control Dynamic Range  | $P_{TXD}$      | -    | 15  | -   | dB   | -                                 |
| DAC Resolution Transmitter Power Control | $P_{TXC}$      | -    | 5   | -   | Bits | -                                 |

### Receiver (for all RX channels)

|   |                  |     |     |    |     |                                       |
|---|------------------|-----|-----|----|-----|---------------------------------------|
| Receiver Conversion Gain <sup>2)</sup>        | $CG_{RX}$        | 12  | 14  | 16 | dB  | -                                     |
| Conversion Gain Variation Over Temperature    | $CG_{RX\_Temp}$  | -3  | -   | 3  | dB  | Including the complete baseband chain |
| Receiver Single Sideband Noise Figure         | $NF_{ssb_{RX}}$  | -   | 12  | 14 | dB  | at 100 kHz offset                     |
| Receiver 1-dB Compression Point               | $P_{-1dB_{RX}}$  | -10 | -5  | -  | dBm | -                                     |
| Channel-to-Channel RX Isolation <sup>3)</sup> | $ISO_{RX}$       | -   | 40  | -  | dB  | -                                     |
| LO feedthrough at the RX port                 | $LO_{feed_{RX}}$ | -   | -30 | -  | dBm | -                                     |
| TX-to-RX Isolation                            | $ISO_{TXRX}$     | -   | 50  | -  | dB  | -                                     |

### Sensors

|  |       |     |   |     |    |   |
|--|-------|-----|---|-----|----|---|
| Temperature Sensor Range <sup>4)</sup> | $T_b$ | -40 | - | 105 | °C | - |
|--|-------|-----|---|-----|----|---|

(table continues...)

**Table 34 (continued) RF FE specifications**

Min and max values cover the specified frequency range,  $f_{RF} = 57.7 \text{ GHz}$  to  $62.4 \text{ GHz}$ . Temperature range,  $T_b = -40 \text{ °C}$  to  $+105 \text{ °C}$ , and voltage supply range,  $VDD_{RF} = 1.71 \text{ V}$  to  $1.89 \text{ V}$  (unless otherwise specified).

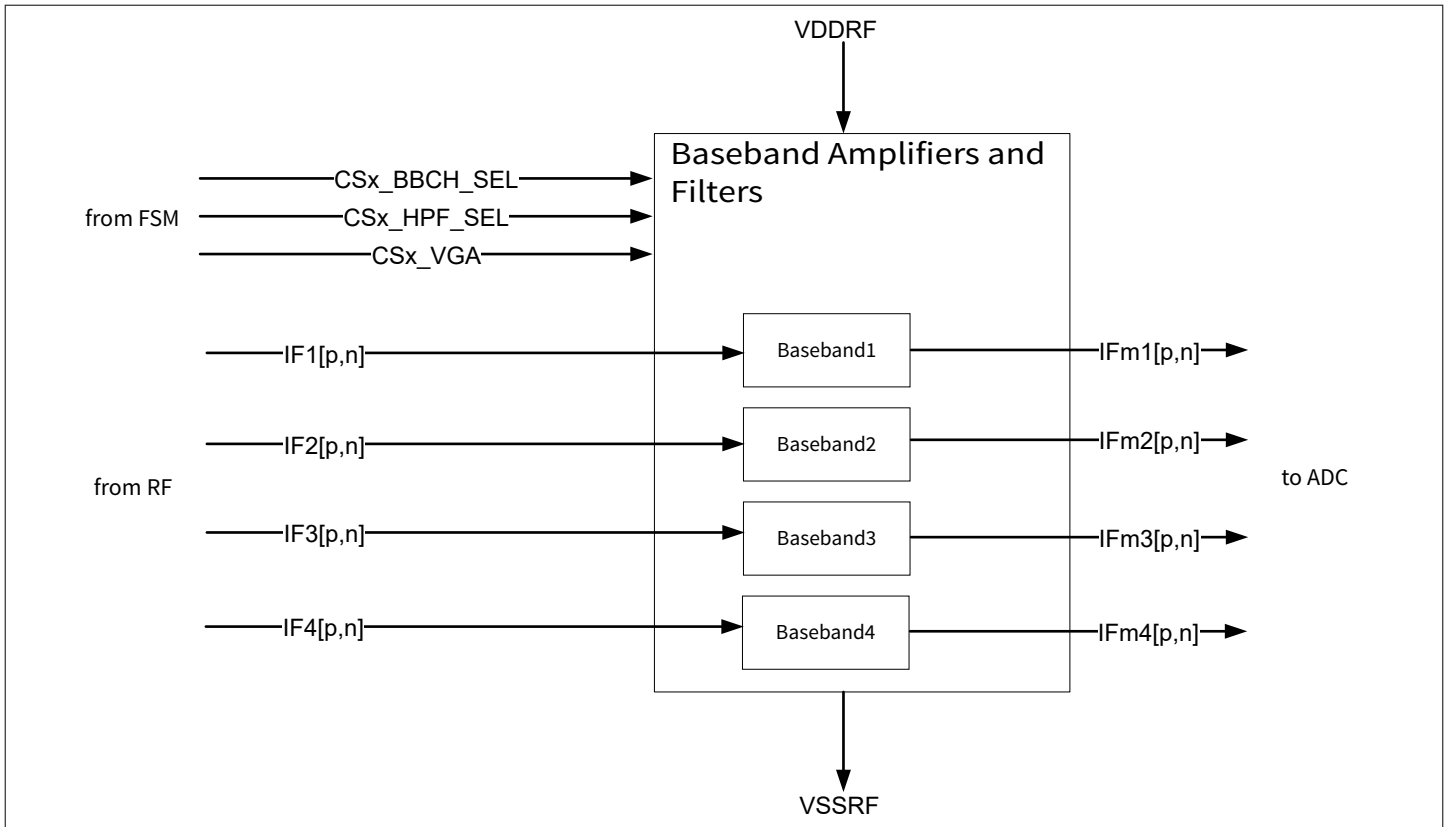
| Parameter   | Symbol                         | Values  |       |       | Unit     | Condition  |
|---|--------------------------------|---|-------|-------|----------|--|
|   |                                | Min.  | Typ.  | Max.  |          |  |
| Chip Backside Temperature ( $Temp$ )                          | $Temp^{5)}$                    | $Temp = a - b \times (T_{ref} - T_{sense}) - 0.23 \times TEMP\_CAL$   |       |       | °C       | Temperature sensor calibration value TEMP_CAL (range $-32_D$ to $+31_D$ ) according to <a href="#">Chip ID register 1</a> .<br>Chip ID readout to follow readout sequence in <a href="#">CHIP ID readout</a> |
| Temperature Sensor Offset (a)                                 | $a$                            | 133.4   | 139.4 | 145.4 | °C       | -  |
| Temperature Sensor Slope (b)                                  | $b$                            | -   | 340   | -     | °C/V     | -  |
| Output Power at Chip Pad Vs TX Peak Detector Readout Relation | $P_{out}$<br>$PPD\_PA^{5) 6)}$ | $P_{out} = t_1 * \ln\left(\frac{PPD\_PA + y_0}{A_1}\right)$<br>$y_0 = 0.04455 \text{ V}$<br>$A_1 = 0.18855 \text{ V}$<br>$t_1 = 11.35808 \text{ dBm}$ |       |       | dBm<br>V | $PPD\_PA$ selected   |
| TX Peak Detector Accuracy                                     | $PPD\_PA_{acc}$                | -2  | -     | 2     | dB       | Over $f_{RF}$  |
| TX Peak Detector Dynamic Range                                | $PPD\_PA_{DR}$                 | -10   | -     | 10    | dBm      | Min. 8 bits  |

- 1) At die pad.
- 2) Power to voltage gain.
- 3) Not including the package.
- 4) If storage temperature exceeds  $105 \text{ °C}$  an additional drift of the temperature sensor readout up to  $\pm 20 \text{ K}$  might occur.
- 5) SADC\_CTRL register settings: TC\_TRIM=0<sub>D</sub>, DSCAL=0<sub>B</sub>, LVGAIN=0<sub>B</sub>, SESP=0<sub>B</sub>, OVERS\_CFG=3<sub>D</sub>, SD\_EN=0<sub>B</sub>, SADC\_CLK\_DIV=3<sub>D</sub>.
- 6) Output power can be evaluated by sampling the level of the peak detector level at the output of the TX power amplifier. This signal has to be compared to a reference to de-embed thermal drift of the sensor. Therefore, both signals on channel SADC:CH3 ( $pd\_outx$ ) and SADC:CH4 ( $pd\_out$ ) are sampled by the SADC in two consecutive steps.  $PPD\_PA = pd\_out - pd\_outx$ .

**Note:** The spurs of the system clock signal could affect the sensor readout. In order to have a more stable read out for the sensors an average over 16 samples for each sensor measurement is recommended.

## 7.2 Analog baseband: amplifiers and filters

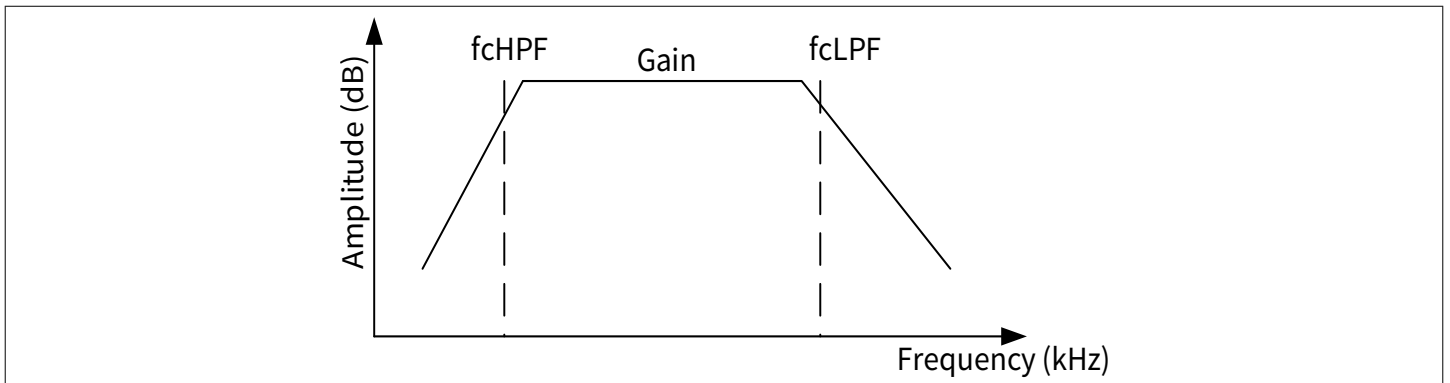
The baseband amplifiers and filters adjusts the *IF* signals to fulfill the system requirements. They set the signal levels to drive full scale the *ADC* inputs without clipping.



**Figure 45** Baseband amplifiers and filters block diagram

### 7.2.1 Baseband characteristics

The baseband block consists of 4 channels. Each channel consists of a *HPF*, a *VGA*, and *AAF* plus a driver for the *ADC* (see [Figure 47](#)).



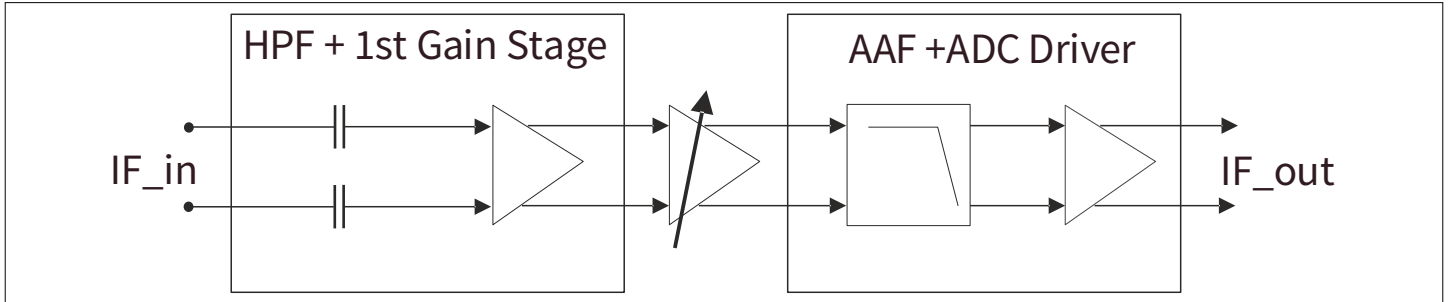
**Figure 46** Baseband characteristics

The *HPF* is used in order to remove the *DC* offset at the output of the *RX* mixer and also suppress the reflected signal from close in unwanted targets (e.g., radome).

### 7.2.2 Baseband requirements

The *HPF* can be tuned to accommodate different *fcHPF* according to different modulation parameters. As presented in the following table, four different settings are possible.

Given the expected power levels the radar system will deal with, the HPF should not degrade the linearity of the system.



**Figure 47** Baseband simplified block diagram, one for each channel

After the *alternating current (AC)* coupling, the *IF* signals are amplified by the first amplifier stage. The first stage shows a selectable voltage gain of 18 or 30 dB. The gain can be adjusted in the *VGA* in 6 steps of 5 dB each up to a maximum gain of 30 dB. The *VGA* is followed by a two-stages, four-poles *AAF*.

The *AAF* cutoff can be set to either 500 kHz, 1 MHz, 1.5 MHz or 2 MHz. The signal is then applied to an *ADC* driver amplifier, which has a gain of 1. The *ADC* driver shows a cut-off behavior above 1 MHz.

Overall, the baseband chain can be set to a maximum gain of 60 dB.

The specific parameters of the baseband chain are summarized in the following tables.

**Table 35** High pass filter selection

$VDD_{RF} = 1.71\text{ V to }1.89\text{ V}$ ,  $T_b = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$

| Parameter | Value |      |      | Unit | Description               |
|-----------|-------|------|------|------|---------------------------|
|           | Min.  | Typ. | Max. |      |                           |
| Fc_HPF_0  | -     | 20   | -    | kHz  | HPF 3 dB cutoff frequency |
| Fc_HPF_1  | -     | 40   | -    | kHz  | HPF 3 dB cutoff frequency |
| Fc_HPF_2  | -     | 100  | -    | kHz  | HPF 3 dB cutoff frequency |
| Fc_HPF_3  | -     | 160  | -    | kHz  | HPF 3 dB cutoff frequency |
| Fc_HPF_4  | -     | 200  | -    | kHz  | HPF 3 dB cutoff frequency |
| Fc_HPF_5  | -     | 800  | -    | kHz  | HPF 3 dB cutoff frequency |

**Table 36** Baseband gain stages

$VDD_{RF} = 1.71\text{ V to }1.89\text{ V}$ ,  $T_b = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$ .

| Parameter                  | Value |       |      | Unit | Description           |
|----------------------------|-------|-------|------|------|-----------------------|
|                            | Min.  | Typ.  | Max. |      |                       |
| 1 <sup>st</sup> Gain Stage | -     | 18/30 | -    | dB   | Selectable, by design |
| VGA                        | -     | 30    | -    | dB   | 6 steps               |
| VGA Step Size              | 4     | 5     | 6    | dB   | -                     |

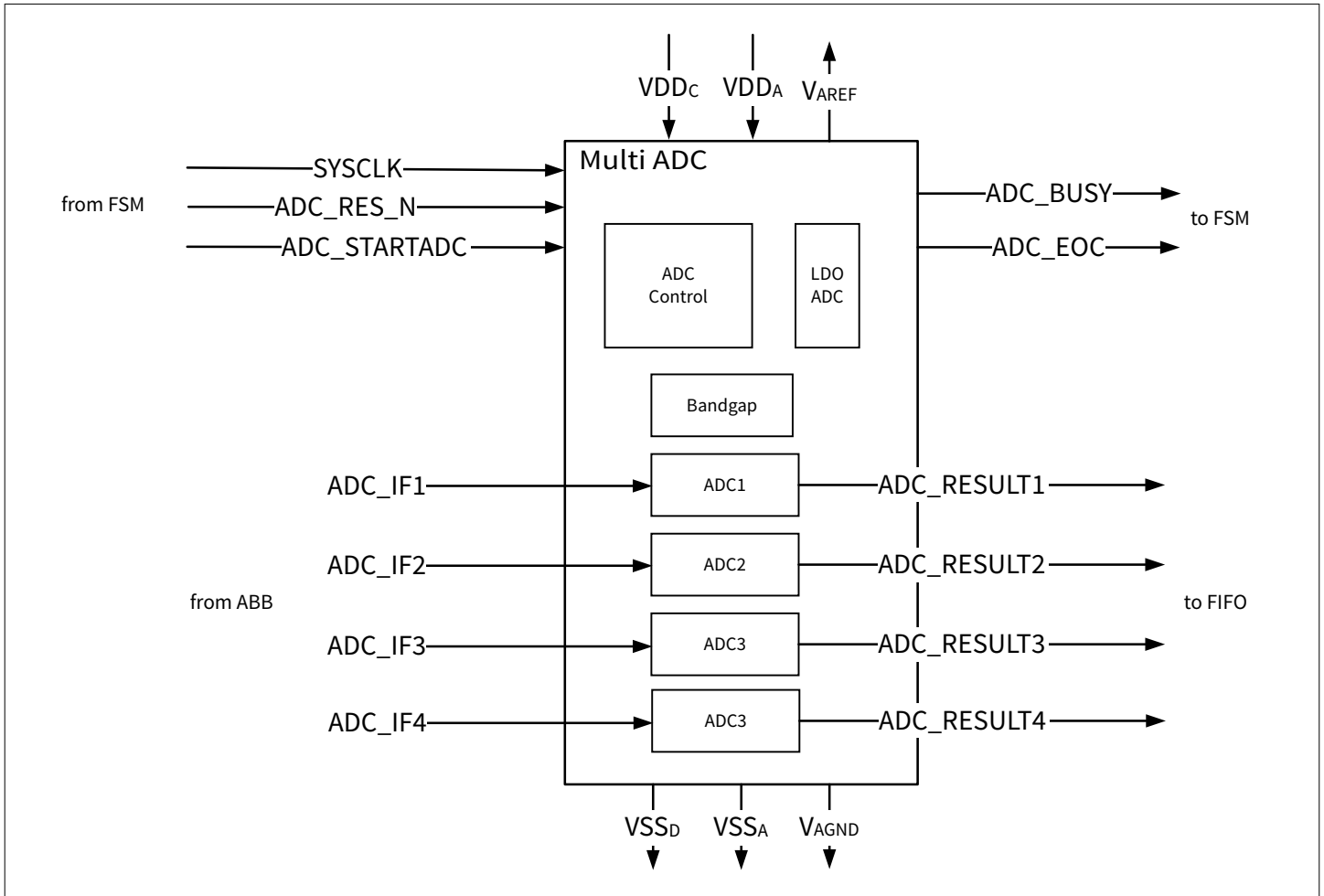
**Table 37**            **Anti-aliasing filter specification**

$VDD_{RF} = 1.71\text{ V to }1.89\text{ V}$ ,  $T_b = -40\text{ °C to }+105\text{ °C}$ .

| Parameter    | Value |                 |      | Unit | Description                         |
|--------------|-------|-----------------|------|------|-------------------------------------|
|              | Min.  | Typ.            | Max. |      |                                     |
| fcLPF1       | 450   | 500             | 650  | kHz  | 3 dB cutoff frequency               |
| fcLPF2       | -     | 1000            | -    | kHz  | 3 dB cutoff frequency               |
| fcLPF3       | -     | 1500            | -    | kHz  | 3 dB cutoff frequency               |
| fcLPF4       | -     | 1800            | -    | kHz  | 3 dB cutoff frequency               |
| LPF_Order    | -     | 4 <sup>th</sup> | -    | -    | Four poles, by design               |
| LPF_Flatness | -     | 1               | -    | dB   | In band flatness, ensured by design |

## 8 MADC domain functional specification

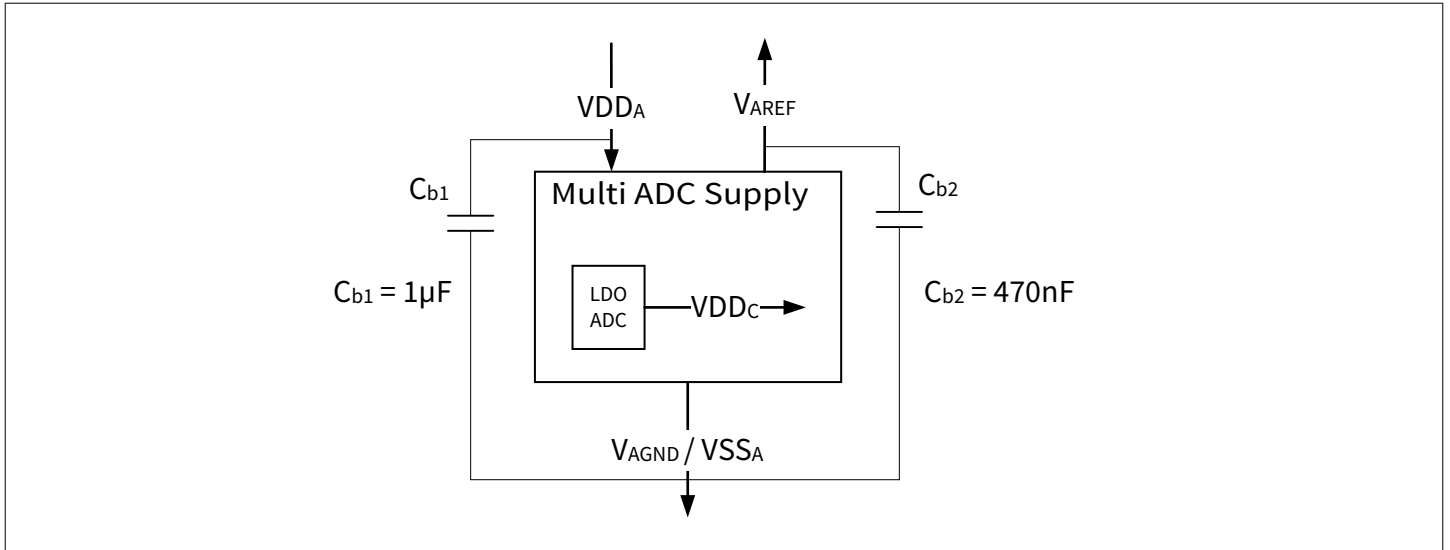
The multichannel *ADC* (MADC) block consists of 4 differential *successive approximation register (SAR)* ADC. The ADC captures the differential *IF* output signals from the *ABB* and convert it into a digital representation of the same. The 1.5 V supply ( $V_{DDC}$ ) is internally generated by a dedicated *LDO* (see Figure 5). For the ADC the parameters are set in *Multi ADC control register*. Each channel of the MADC can be enable/disable together with the respective baseband channel by the bits `MADC_BBCH_EN` in *Channel set up x register 1*. To simplify the dataflow to the channel can be selected via the `BBCH_SEL` in *Channel set up x register 1*. See also *APU* and *APD* in *PLL shape x register 3* and Chapter 5.2.



**Figure 48** MADC block diagram

### 8.1 MADC supply voltage requirements

The voltage supply to the *ADC* domain is provided on pin  $V_{DDA}$  and the output of the internal ADC reference voltage is provided on pin  $V_{AREF}$ . In order to filter out the voltage ripples due to switching effects a low *equivalent series resistance (ESR)* bypass capacitor of  $C_{b2} = 470$  nF should be used on the *printed circuit board (PCB)*.



**Figure 49** MADC input pin requirements

$V_{AGND}$  shares the same analog ground connection pin  $VSS_A$  on PCB. The bypass capacitors should be mounted as close as possible to those pins.

**Table 38** MADC voltage reference

$VDD_A = 1.71\text{ V to }1.89\text{ V}$ ,  $T_b = -40\text{ °C to }+105\text{ °C}$ .

| Parameter  | Symbol     | Values |      |      | Unit | Condition                           |
|--|------------|--------|------|------|------|-------------------------------------|
|  |            | Min.   | Typ. | Max. |      |                                     |
| Positive reference voltage with respect to $V_{AGND}$ , generated internally | $V_{AREF}$ | 1.10   | 1.21 | 1.29 | V    | -                                   |
| Negative analog reference voltage  | $VSS_A$    | -0.1   | 0    | -    | V    | Refers to board design ground plane |

## 8.2 MADC specifications

The following table specifies the *ADC* parameters. The numbers include one over-conversion. All parameters are only valid with executed start-up calibration. No parameter is targeted for production test.

**Note:**  $f_{ADC\_CLK} = f_{SYS\_CLK}$

REMARK:

If the ADC starts sampling before the bandgap is powered up (BG\_EN in [Channel set control x register](#)), the results will show some gain errors. To avoid this, follow the bandgap power up timing presented in section [Chapter 8.4](#).

**Table 39 MADC specifications**

$V_{DDA} = 1.71 \text{ V to } 1.89 \text{ V}$ ,  $T_b = -40 \text{ }^\circ\text{C to } +105 \text{ }^\circ\text{C}$ .

| Parameter                                      | Symbol         | Value |      |       | Unit          | Condition   |
|--|----------------|-------|------|-------|---------------|---|
|  |                | Min.  | Typ. | Max.  |               |   |
| Resolution                                     | Resolution     | -     | 12   | -     | Bits          | With default settings and tracking conversion <a href="#">Table 42</a>  |
| Analog input voltage                           | $V_A$          | 0.145 | -    | 1.455 | V             | -   |
| ADC Clock Frequency                            | $f_{ADC\_CLK}$ | 75    | 80   | 85    | MHz           | $f_{ADC\_CLK} = f_{SYS\_CLK}$<br>See <a href="#">Chapter 2.2</a><br>78 MHz not allowed                        |
| Signal to noise ratio                          | $SNR$          | 38    | -    | 62    | dB            | @ -6 dB FS  |
| Spurious free dynamic range                    | $SFDR$         | 58    | 69   | -     | dB            | @ -6 dB FS<br>@ 600 kHz   |
| Inter modulation product                       | $IM3$          | -62   | -69  | -     | dB FS         | @ -12 dB FS each input tone<br>@ 600 kHz max $f$<br>@ 50 kHz $\Delta f$                                       |
| Bandwidth input buffer                         | $BW$           | 600   | -    | -     | kHz           | 1 <sup>st</sup> order Filter in input Buffer  |
| Conversion time – excluding sample time        | $N_{conv}$     | -     | 24   | -     | Counts of clk | Including one tracking conversion, sampling time not included   |
| Sampling time                                  | $T_s$          | 4     | -    | -     | Counts of clk | @ 76.8/80 MHz   |
| Wake up time – bandgap and BG reference Buffer | $T_{WUBGB}$    | 300   | 600  | 1000  | $\mu\text{s}$ | -   |
| Wake up time – ADC <sup>1)</sup>               | $T_{WUADC}$    | -     | 660  | -     | Counts of clk | without start-up calibration  |
| Startup calibration time <sup>2)</sup>         | $T_{SUCAL}$    | 3361  | 6049 | 16801 | Counts of clk | ADC0:DSCAL= 0 <sub>B</sub><br>Typical conditions:<br>ADC0:STC=1 <sub>B</sub><br>ADC0:MSB_CTRL= 1 <sub>B</sub> |
| Setup time common mode input voltage           | $T_{VCM}$      | -     | -    | 1     | $\mu\text{s}$ | -   |
| Power supply Rejection Ratio on $V_{DD_S}$     | $PSRR$         | 20    | -    | -     | dB            | -   |

1) Overall wake up time when calibration time is enabled =  $T_{WUADC} + T_{SUCAL}$ .

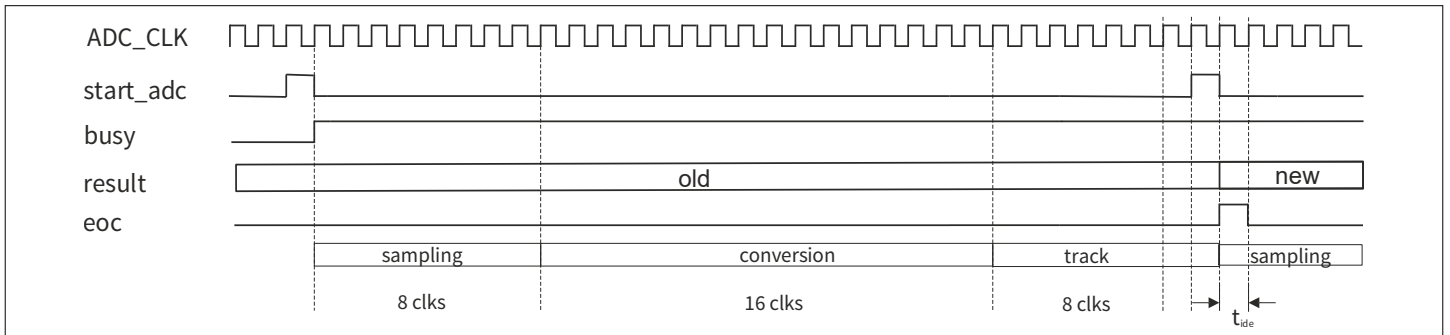
2)  $T_{SUCAL} = (1792 * 2^{ADC0:STC} + 896 * ADC0:MSB\_CTRL + 1569) * T_{SYS\_CLK}$ .

Parameters ensured by design

### 8.3 MADC timing diagrams

The interface is fully synchronized to the main clock. The following figure shows the 12 bits conversion timing in case of one tracking and no oversampling. Thus, the maximum speed of the *ADC* is set to 2.5 MSps at 80 MHz clock input. Figure 50 shows the *SAR* ADC timing.

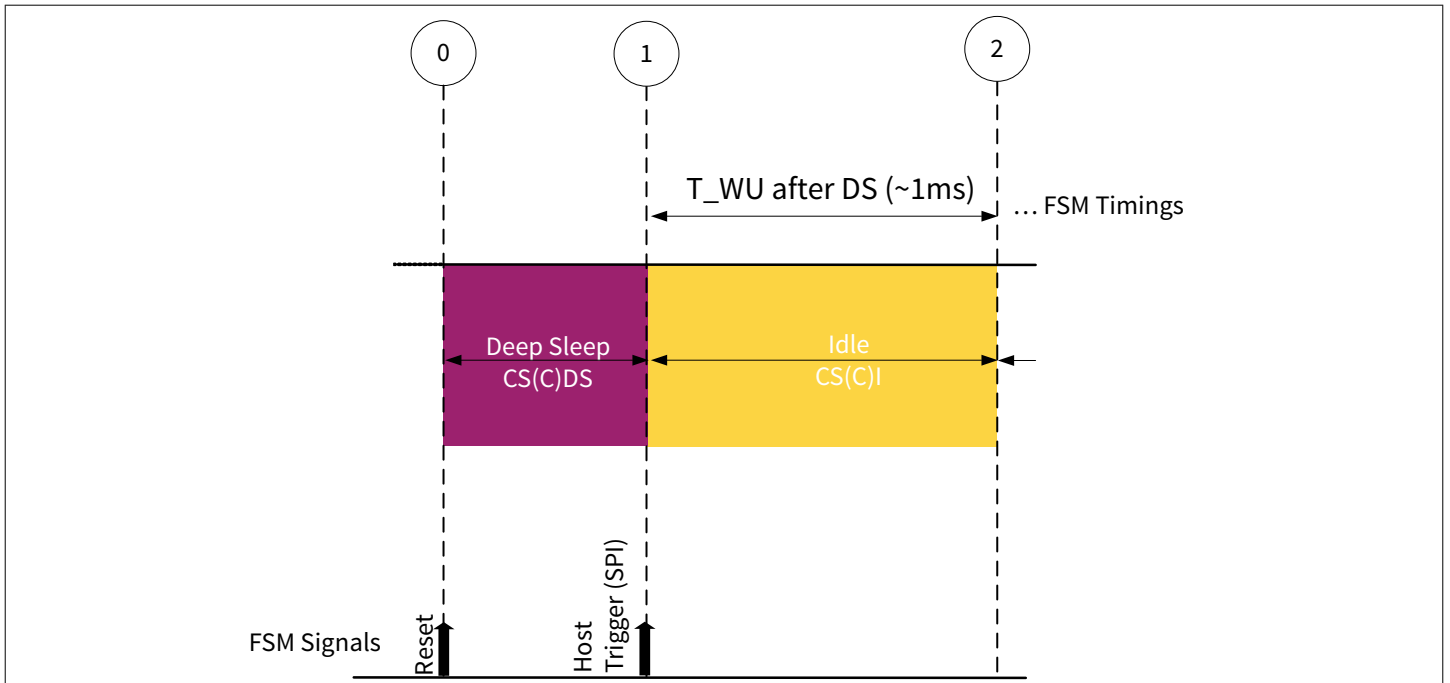
**Important:** All configuration signals must be stable during a running conversion (between start\_adc and one cycle before eoc).



**Figure 50 SAR ADC conversion timing diagram**

### 8.4 MADC start-up sequence

The following figure shows the start-up sequence for the complete *ADC*.



**Figure 51 MADC start-up timing constraints**

After a reset and trigger from the host, the *FSM* will move from the DS power mode into the Idle power mode. Here  $T_{WKUP}$  represents the overall time required by the bandgap to settle and it is the longest time required in the settling of the *ADC*.

**Table 40 MADC start-up timing constraints**

$V_{DDA} = 1.71\text{ V to }1.89\text{ V}$ ,  $T_b = -40\text{ °C to }+105\text{ °C}$ .

| Parameter   | Symbol      | Values |      |      | Unit          | Condition               |
|---|-------------|--------|------|------|---------------|-------------------------|
|   |             | Min.   | Typ. | Max. |               |                         |
| Wake up time  | $T_{WUADC}$ | 8.25   |      |      | $\mu\text{s}$ | @ $f_{\text{SYS\_CLK}}$ |
| Setup time common mode input voltage                  | $T_{VCM}$   |        |      | 1    | $\mu\text{s}$ |                         |
| Wake-up time for bandgap and bandgap reference buffer | $T_{WU}$    | 300    |      | 1000 | $\mu\text{s}$ |                         |

## 8.5 MADC conversion rate

The **ADC** clock input is  $f_{\text{ADC\_CLK}} = f_{\text{SYS\_CLK}} = 76.8/80\text{ MHz}$  and is derived from the system clock.

A conversion can include three different phases:

- Sampling
- Conversion
- Tracking

### 8.5.1 Sampling

During the first phase, the analog input voltage is sampled onto the input capacitor. The duration is controlled using the ADC0:STC bits (see Multi ADC control register). The following table shows the link between the register value ADC0:STC the clock periods STC\_NUM and the sampling time.

**Table 41 ADC0:STC value table**

| ADC0:STC | Sampling clock periods STC_NUM | Sampling time $t_{\text{sample}}$ in ns<br>( $f_{\text{ADC\_CLK}} = 80\text{ MHz}$ ) |
|----------|--------------------------------|--|
| $0_D$    | 4                              | 50   |
| $1_D$    | 8                              | 100  |
| $2_D$    | 16                             | 200  |
| $3_D$    | 32                             | 400  |

The sampling time is calculated as:  $N_{\text{sample}} = \text{STC\_NUM}$ .

### 8.5.2 Conversion

The charge from the sampling capacitor is redistributed to 13 + 2 capacitors. To identify the *least significant bit (LSB)* bits of the result, 13 clock cycles are needed.

To identify the *MSB* bit of the result, one or two clock cycles are used, depending on register setting ADC0:MSB\_CTRL (see [Multi ADC control register](#)):

- In case of MSB\_CTRL is set to  $0_B$ , just a single clock cycle is used (+1)
- In case of MSB\_CTRL is set to  $1_B$ , two clock cycles are used (+2)

The redistribution time is calculated as:  $N_{\text{conv}} = (13 + 2 + \text{ADC0:MSB\_CTRL})$  and results in either 16 clock cycles or 17 clock cycles.

### 8.5.3 Tracking

In this mode, the *ADC* performs a single sample conversion followed by several tracking conversions, depending on the setting of bits *ADC0:TRACK\_CFG* (see Multi ADC control register).

**Table 42** *ADC0:TRACK\_CFG* value

| <i>ADC0:TRACK_CFG</i> | Additional conversions<br><i>TRACK_CFG_NUM</i> | Remarks |
|-----------------------|--|---------|
| 0 <sub>D</sub>        | 0  |         |
| 1 <sub>D</sub>        | 1  | Default |
| 2 <sub>D</sub>        | 3  |         |
| 3 <sub>D</sub>        | 7  |         |

The duration of one tracking conversion is:  $N_{\text{track}} = 8$ .

The duration of all tracking conversions for a single result is:  $N_{\text{track\_all}} = 8 * \text{TRACK\_CFG\_NUM}$ .

### 8.5.4 ADC conversion rate

Based on what is defined in [Chapter 8.5.1](#), [Chapter 8.5.2](#), and [Chapter 8.5.3](#), the following cycles are defined for a single conversion:

$$N_{\text{ADC\_CONV}} = N_{\text{samp}} + N_{\text{conv}} + N_{\text{track\_all}} \quad (20)$$

with  $N_{\text{samp}}$  the number of sampling,  $N_{\text{conv}}$  conversion and  $N_{\text{track}}$  tracking cycles, respectively.

*ADC* are synchronized to  $f_{\text{SYS\_CLK}}$ .

### 8.5.5 ADC sampling rate

The *ADC* sampling rate is controlled by the *ADC0:ADC\_DIV* value (see [Multi ADC control register](#)). The sampling rate of the *ADC* is given then by  $f_{\text{ADC\_SAMP}} = f_{\text{ADC\_CLK}} / \text{ADC\_DIV}$ . The *ADC0:ADC\_DIV* value needs to be greater than the number of clock cycles needed by a single *ADC* conversion as described in [Chapter 8.5.4](#).

The sampling rate of the *ADC* is:

$$f_{\text{ADC\_SAMP}} = f_{\text{ADC\_CLK}} / \text{ADC\_DIV} \quad (21)$$

with  $\text{ADC\_DIV} \geq N_{\text{ADC\_CONV}}$ .

**Table 43** *ADC Sampling Rate*

$V_{\text{DDA}} = 1.71 \text{ V to } 1.89 \text{ V}$ ,  $T_{\text{b}} = -40 \text{ }^\circ\text{C to } +105 \text{ }^\circ\text{C}$ .

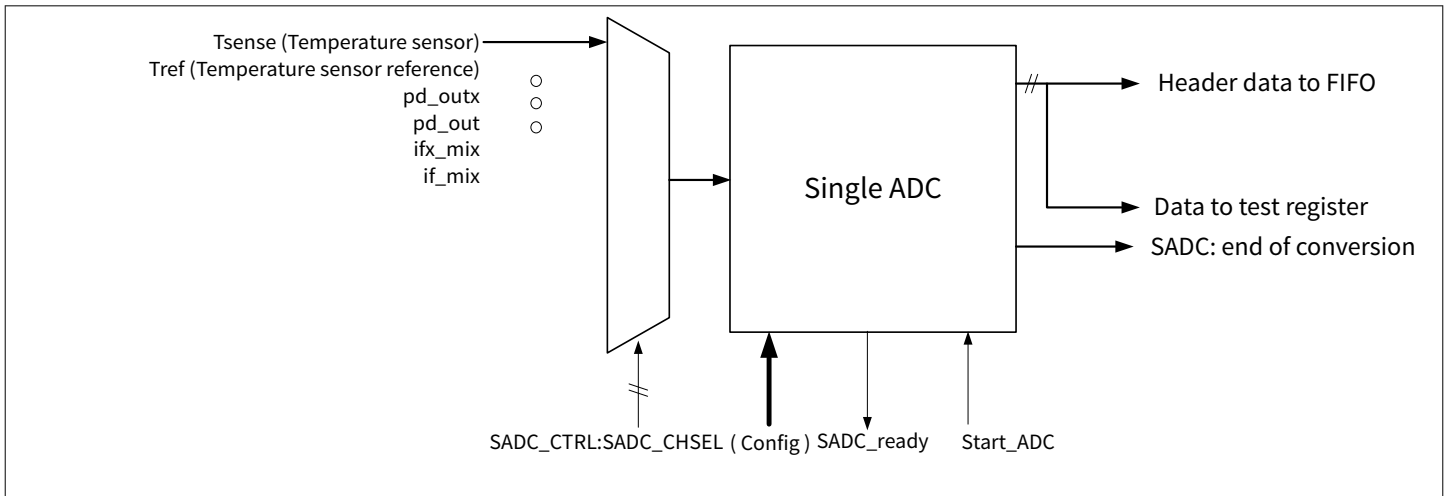
| Parameter                           | Symbol                 | Values |      |      | Unit | Condition |
|-------------------------------------|------------------------|--------|------|------|------|-----------|
|                                     |                        | Min.   | Typ. | Max. |      |           |
| ADC sampling rate                   | $f_{\text{ADC\_SAMP}}$ | -      | 2    | 4    | MHz  | -         |
| Effective number of bits resolution | <i>ENOB</i>            | -      | 10.5 | -    | Bits | -         |

## 9 SADC domain functional specification

The sensor *ADC* (SADC) is a single channel single ended 8 bit *SAR* ADC.

The sensor ADC can be used to monitor the temperature output as well as the power detector outputs from the transmitter channels. Conversion data can be read out through the SADC register (see [Sensor ADC result register](#)). The data can be added also to the header of the data frame in the *FIFO* (see [Figure 20](#)). By default, the SADC is set to read out the temperature sensor out (SADC\_CTRL:SADC\_CHSEL= 0<sub>D</sub>). For additional settings, please check [Sensor ADC control register](#). See also the following figure. The SADC can achieve a better resolution of 10 bits by means of oversampling (see [Chapter 9.2](#)).

Due to the required conversion time, ADC data are not available during a shape, but they would be available during next shape (there is a delay of one shape for these data).



**Figure 52 SADC integration**

### 9.1 SADC functionality

Four main tasks are performed by the *FSM* to control the sensor *ADC*:

#### Enabling

The SADC module is enabled through the CSCx register in any phase of the FSM state (see [Channel set control x register](#))

#### Initialization

The host selects the channel in the channel register from SADC\_CTRL control register (see also [Sensor ADC control register](#))

#### Triggering

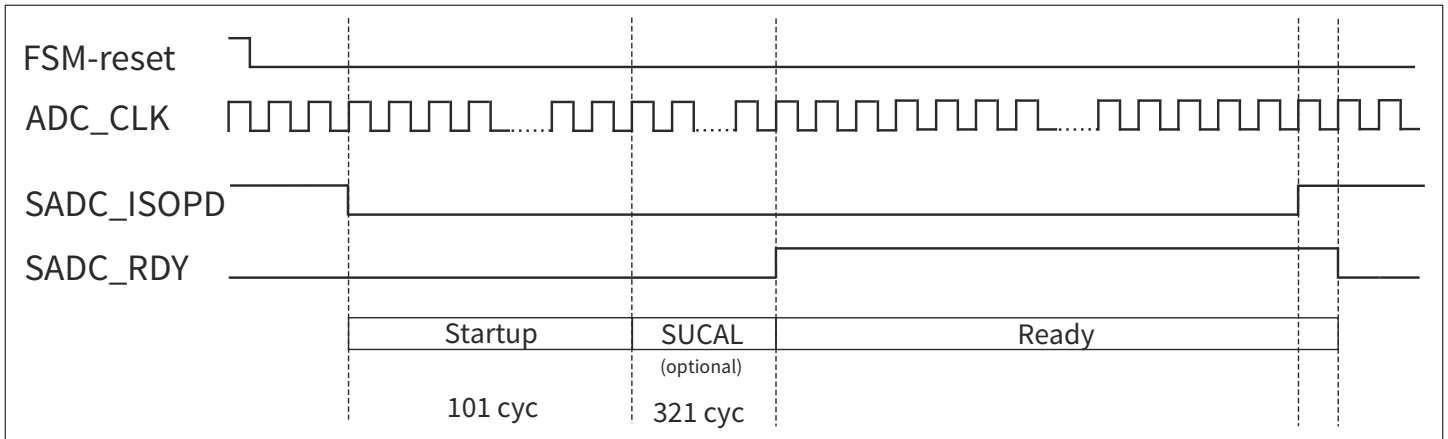
Each chirp-start during the active phase of shapes will trigger the SADC sampling/conversion or by sending a SADC\_START to SADC\_CTRL register (see [Sensor ADC control register](#))

#### Results

The conversion results are stored in the result register SADC\_RESULTS register (see [Sensor ADC result register](#)) after the sampling and conversion is completed

### 9.2 SADC conversion formula

The sensor *ADC* clock signal is running at 20 MHz and is derived from  $f_{SADC\_CLK} = f_{SYS\_CLK} = 80$  MHz. The SADC start-up time is 101 clock cycles without start-up-calibration and 422 clock cycles with start-up-calibration. If temperature or power supply conditions did not change dramatically, the start-up-calibration can be avoided during frames.



**Figure 53 SADC start-up timing**

The conversion time  $N_{CONV\_LEN}$  for a single analog to digital conversion into the result register SADC\_RESULT is defined by the following relation:

$$N_{CONV\_LEN} = (N_{conv} + N_{sample\_dflt} + SESP * N_{spread\_early\_sample}) * OVS \quad (22)$$

Where:

- $N_{conv} = 13$  clock cycles
- $N_{sample\_dflt} = 16$  clock cycles
- $N_{spread\_early\_sample} = 16$  clock cycles
- OVS ... see SADC\_CTRL:OVERS\_CFG (see [Sensor ADC control register](#))
- SESP ... see SADC\_CTRL:SESP (see [Sensor ADC control register](#))

The SADC conversion formula for 8 bits resolution is:

$$Dout8b = ((2^8 * VA_{in}) / V_{AREF}) * GA_{in} \text{ with an error of } \pm 0.1\% \quad (23)$$

Where:

- $VA_{in}$  is the analog input to the SADC
- $GA_{in}$  is the gain of the ADC module and can be set either to 1 or 0.75
- $V_{AREF} = 1.21$  V

In order to achieve a 10 bits resolution the oversampling should be set to 32.

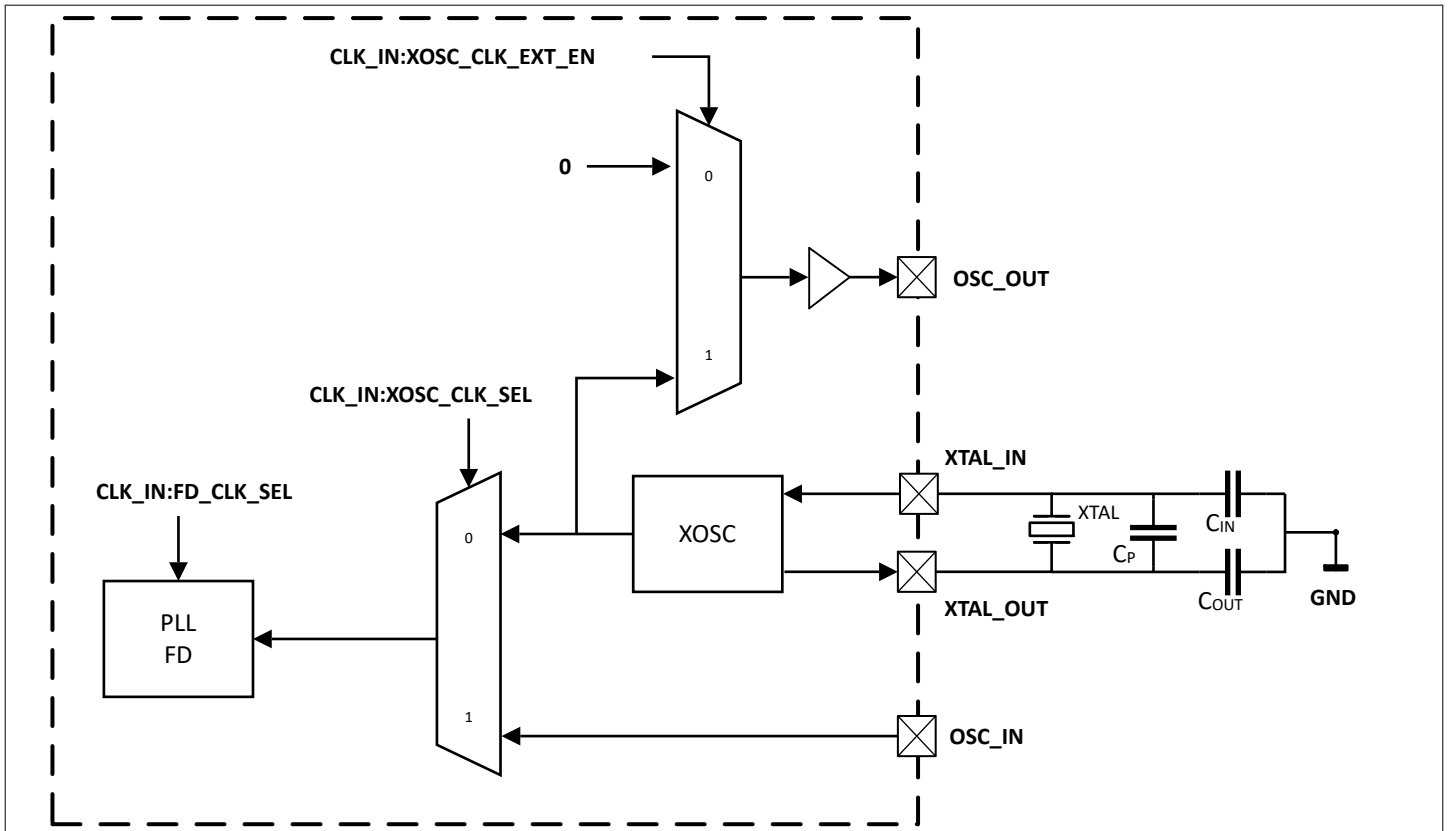
In order to measure correctly the power sensor output, see [Chapter 7.1.2](#) and [Sensor ADC control register](#).

**Note:** To disable the SADC, simply set in register CSCx SADC\_ISOPD = 1<sub>B</sub> ( $f_{SYS\_CLK}$  has to be still provided for at least one additional cycle for the command to take effect).

## 10 XOSC - XTAL Oscillator

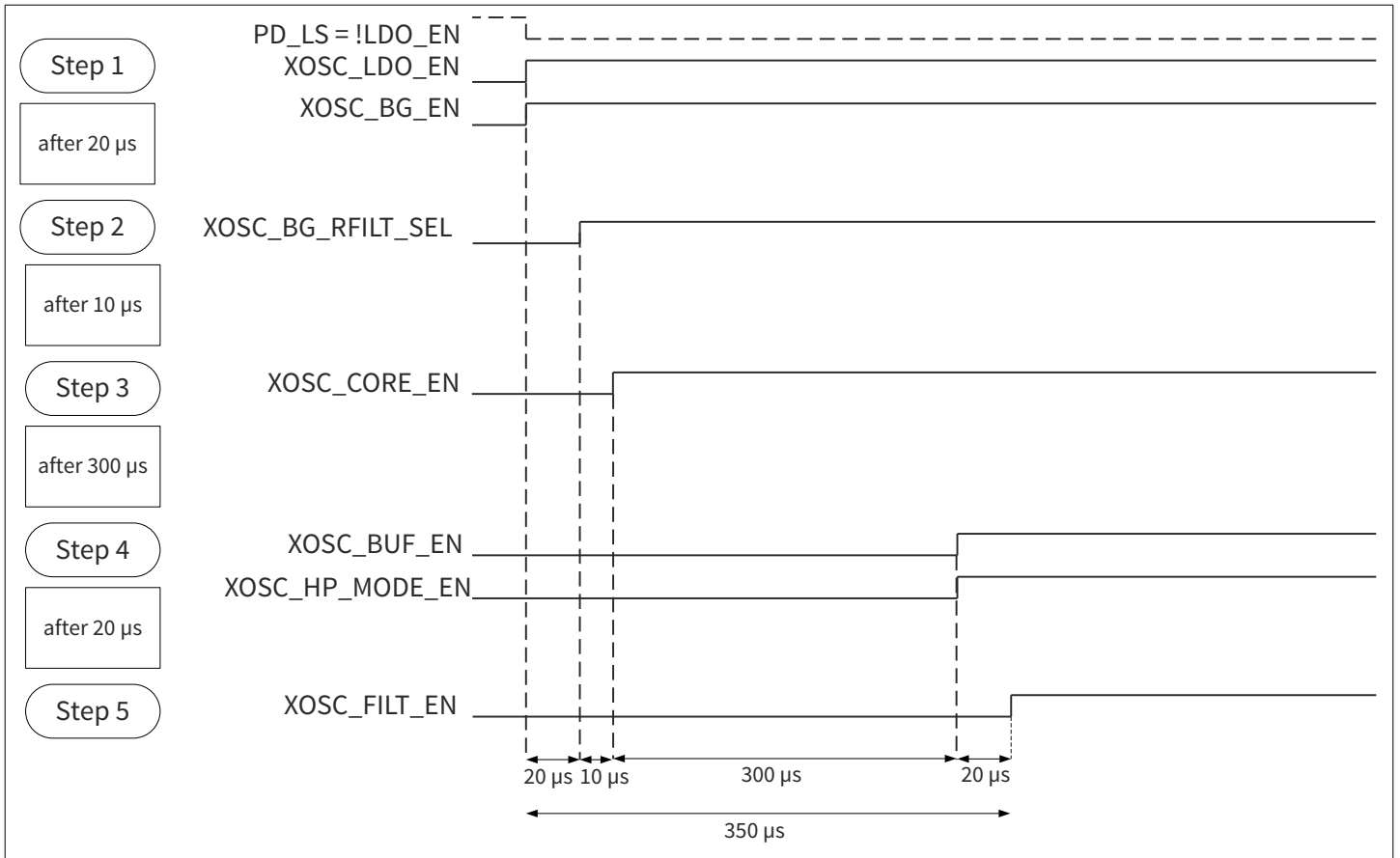
The BGT60ATR24AIP comes with an built-in crystal oscillator to generate the operation clock for the overall system. For use-cases with external available oscillator clock the integrated XOSC can be fully disabled and bypassed to operate the chip via an external clock (OSC\_IN). There is also the option to forward the internal generated clock to external devices via the buffered OSC\_OUT pad.

In all cases the clock is forwarded to the frequency doubler inside the PLL to provide the option to double the clock frequency. Furthermore, there is also the option to apply some duty cycle correction via programmable delay cells.



**Figure 54** Block diagram of clock generation

The XOSC requires a certain start-up routine by enabling dedicated signals at a certain point in time. This can be done by programming the correlating `CLK_IN` registers via *SPI* with single *SPI* commands. The required five configuration steps are described in the figure below.



**Figure 55** XOSC start-up sequence

**Table 44** XOSC specifications

Temperature range,  $T_b = -40\text{ }^\circ\text{C}$  to  $+105\text{ }^\circ\text{C}$ , and voltage supply range,  $VDD_{PLL} = 1.71\text{ V}$  to  $1.89\text{ V}$ ,  $VDD_D = 1.71\text{ V}$  to  $1.89\text{ V}$  (unless otherwise specified).

| Parameter                            | Symbol                   | Values |      |      | Unit | Condition    |
|--------------------------------------|--------------------------|--------|------|------|------|--------------|
|                                      |                          | Min.   | Typ. | Max. |      |              |
| Current consumption (buffer enabled) | $I_{DD_{XOSC\_BUF\_EN}}$ |        |      | 2    | mA   | Without load |

| XTAL   |                  |  |      |                  |          |  |
|--|------------------|--|------|------------------|----------|--|
| Equivalent series resistance XTAL  | $ESR_{XTAL}$     |  | 20   | 50               | $\Omega$ |  |
| Load capacitance XTAL<br>$C_{LOAD\_XTAL} = C_{IN} \times C_{OUT} / (C_{IN} + C_{OUT}) + C_P$ | $C_{LOAD\_XTAL}$ |  | 6    | 12 <sup>1)</sup> | pF       |  |
| Frequency XTAL   | $f_{XTAL\_38}$   |  | 38.4 |                  | MHz      |  |
|  | $f_{XTAL\_40}$   |  | 40   |                  | MHz      |  |

| External oscillator |                   |      |      |      |     |  |
|---------------------|-------------------|------|------|------|-----|--|
| Voltage OSC_IN low  | $V_{OSC\_IN\_L}$  | 0    | -    | 0.2  | V   |  |
| Voltage OSC_IN high | $V_{OSC\_IN\_H}$  | 1.45 | -    | 1.89 | V   |  |
| Frequency OSC_IN    | $f_{OSC\_IN\_38}$ |      | 38.4 |      | MHz |  |
|                     | $f_{OSC\_IN\_40}$ |      | 40   |      | MHz |  |

(table continues...)

**Table 44 (continued) XOSC specifications**

Temperature range,  $T_b = -40\text{ °C}$  to  $+105\text{ °C}$ , and voltage supply range,  $VDD_{PLL} = 1.71\text{ V}$  to  $1.89\text{ V}$ ,  $VDD_D = 1.71\text{ V}$  to  $1.89\text{ V}$  (unless otherwise specified).

| Parameter | Symbol            | Values |      |      | Unit | Condition |
|-----------|-------------------|--------|------|------|------|-----------|
|           |                   | Min.   | Typ. | Max. |      |           |
|           | $f_{OSC\_IN\_76}$ |        | 76.8 |      | MHz  |           |
|           | $f_{OSC\_IN\_80}$ |        | 80   |      | MHz  |           |

**Clock output**

|                          |                      |      |  |      |    |   |
|--------------------------|----------------------|------|--|------|----|---|
| Voltage OSC_OUT low      | $V_{OSC\_OUT\_L}$    | 0    |  | 0.15 | V  | $C_L = 5\text{ pF}$<br>$R_L > 100\text{ k}\Omega$ |
| Voltage OSC_OUT high     | $V_{OSC\_OUT\_H}$    | 1.35 |  | 1.5  | V  | $C_L = 5\text{ pF}$<br>$R_L > 100\text{ k}\Omega$ |
| Load capacitance OSC_OUT | $C_{LOAD\_OSC\_OUT}$ |      |  | 5    | pF |   |

1) Maximum values will lead to higher current consumption and longer start-up time up to 500 us.

## 11 Enhanced functions

### 11.1 CHIP ID readout

Readout sequence:

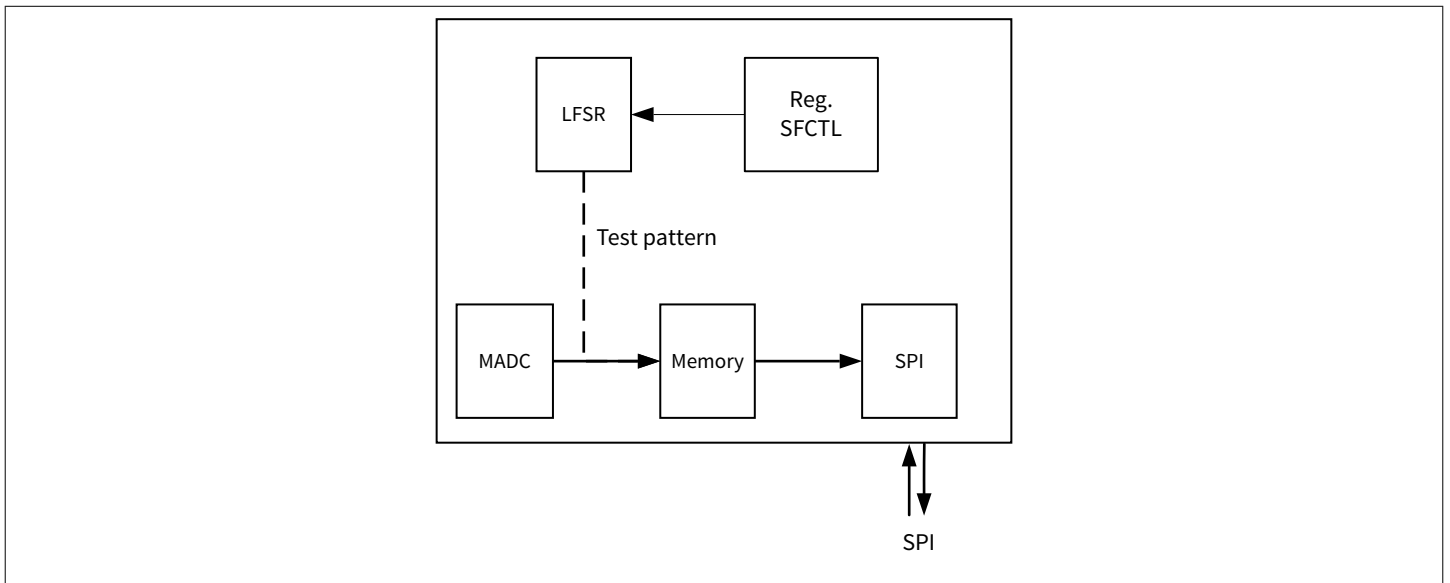
1. Enable the EFUSE block by setting EFUSE0:EFUSE\_EN = 1<sub>B</sub> with a single dedicated *SPI* write (see [EFUSE register 0](#))
2. Initiate the sense operation by setting EFUSE0:EFUSE\_SENSE = 1<sub>B</sub> with a single dedicated *SPI* write
3. Wait for 2 μs or poll the register field EFUSE1:EFUSE\_READY = 1<sub>B</sub> (see [EFUSE register 1](#))
4. Read out the device ID from CHIP\_ID0 and CHIP\_ID1 (see [Chip ID register 0](#) and [Chip ID register 1](#))
5. Disable the EFUSE block EFUSE0:EFUSE\_EN = 0<sub>B</sub>

**Note:** The host has to ensure that the system clock is available for the EFUSE sense operation. Otherwise, reading the CHIP ID which is encoded in the EFUSE is not possible!

### 11.2 Data test mode

A *LFSR* is built-in on chip. It will generate a pseudo random bit M-sequence that can be used to fill up the *FIFO*. This module can be used to develop and test the complete pipeline from the *FIFO* on the BGT60ATR24AIP up to the *AP* memory, including firmware and drivers, with a defined bit sequence. For that the 12-bit ADC1 output data are replaced by the 12-bit generated by the *LFSR*.

The implemented *LFSR* is described by the following polynomial:  $x^{12}+x^{11}+x^{10}+x^4+1$  and starts with the seed 1<sub>D</sub>.



**Figure 56** Digital pipeline simplified block diagram

The first *ADC* channel output data stream is bypassed by the data sequence coming from the *LFSR* generator. Therefore, only ADC1 output data are replaced by *LFSR* data.

- Initialization of the *LFSR* with the start seed via MAIN:FSM\_RESET = 1<sub>B</sub> (see [Main register](#))
- Enable bit SFCTL:LFSR\_EN = 1<sub>B</sub> (see [SPI and FIFO control register](#)) to activate *LFSR* and generate the known test data

### 11.3 CW mode

In the *continuous wave (CW)* mode the device will be set to provide a constant output frequency. During CW mode no shapes are executed.

During the execution of this mode:

- Freq/timing parameters defined in shape registers are ignored
- *PLL / RF / ADC* runs with values programmed in PLL DFT0 (see [PLL test register 0](#)) and CSU1 (see [Channel set up x register 1](#)).
- All other CSx / shape settings are not handed over to functional blocks
- The values for REPS/REPC/REPT and frame relevant timings are used to shape a “virtual frame”
- Data from the *FIFO* can be read out following the structure of that “virtual frame”

**Note:** For test purposes the “virtual frame” definition should be kept simple: 1 shape, 1 CS, e.g.

### 11.3.1 Enabling the CW mode

The *CW* mode should be preceded by at least a *HW* reset after power up. In case the chip is already up and running a *SW* reset may be used instead.

After this in order to enable the CW mode, the steps below should be followed:

- Enable the MAIN: CW\_MODE = 1<sub>B</sub> (see [Main register](#))
- Initialize the chip registers according to defined “virtual frame” (settings in [Channel set up x register 0](#) and [PLL shape x register 0](#))
- Enable the clock: PACR1: OSCCLKEN (see [PLL analog control register 1](#))
- Set frequency via PLLx: FSU setting from shape 1
- Set channel set for CSDS/CSI/CSU1 (see [Channel set deep sleep register 0](#))
- set PLL DFT0: byprmpen = 1<sub>B</sub> (see [PLL test register 0](#))

By using the FRAME\_START as trigger, the chip can be set in the different states of a shape as shown in the following figure.

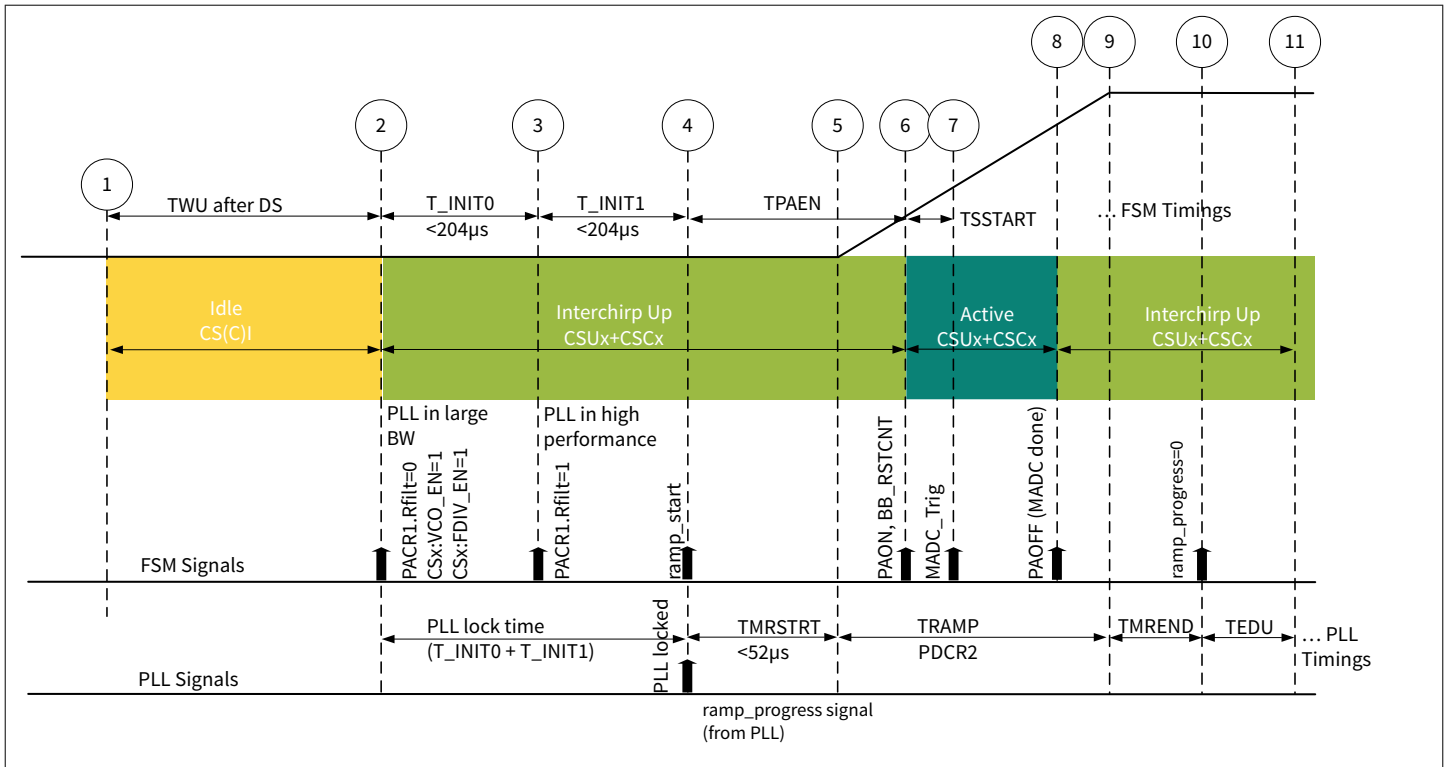
- TRIG#1: jump to 1 (DS -> Idle)
- TRIG#2: jump to 2 (Idle -> Init0)
- TRIG#3: jump to 3 (Init0 -> Init1)
- TRIG#4: jump to 4
- TRIG#5: jump to 6

Frequency update: at this stage the output frequency can be updated/programed (FSU) to any value and the current frequency will be updated immediately after PLL transition of PDFT0: byprmpen = 0<sub>B</sub> -> 1<sub>B</sub>.

- TRIG#6: jump to 7

At this stage, the APU number of samples is generated by the *ADC* according to the ADC0 settings. In case if APU = 0<sub>D</sub> no triggers are generated, manual triggering of MADC can be done via ADC0: TRIG\_MADC. Once the APU number of samples is generated another automatic generation of samples can be done after *FSM* reset.

- TRIG7: jump to 8
- TRIG8: jump to 10
- TRIG9: jump to 11
- TRIGx



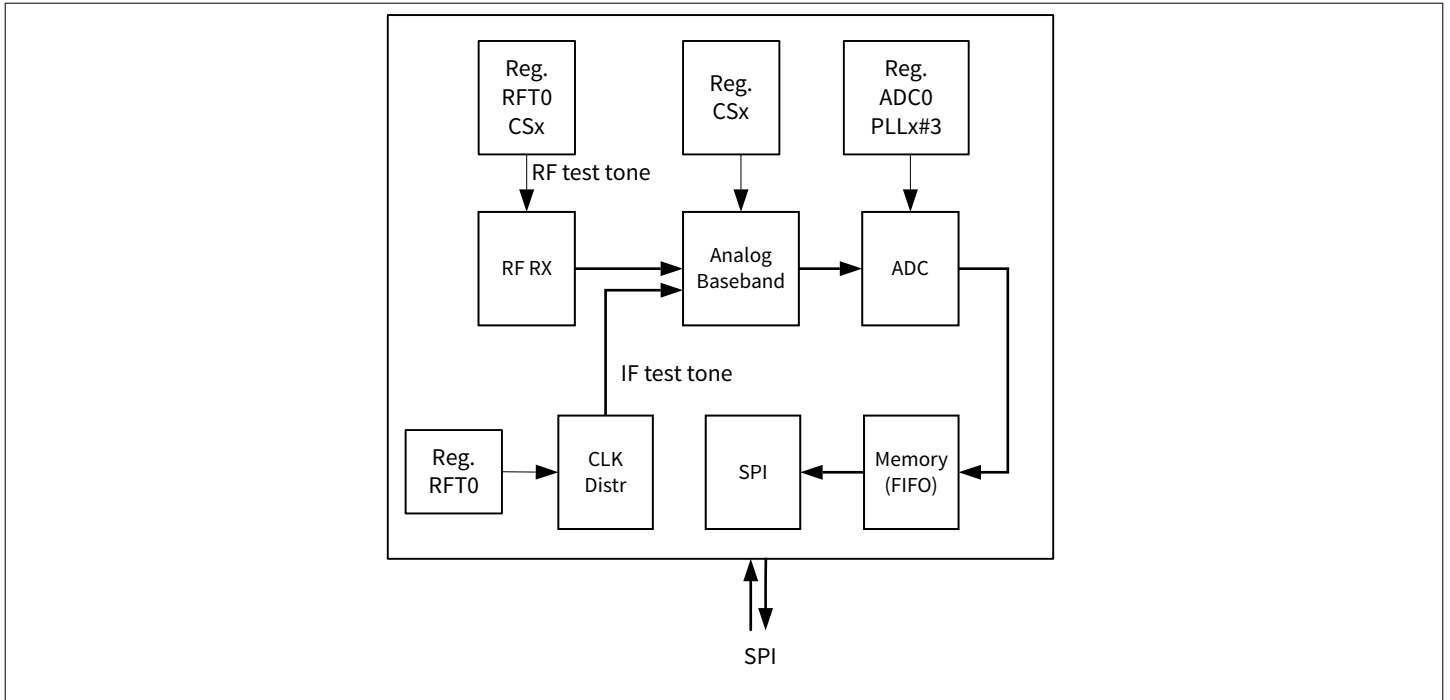
**Figure 57** Steps that can be followed during a “virtual frame”

The FSM-reset will set back the FSM to initial state to start again with TRIG1.

This specific mode is intended also to test the power consumption of the chip during a specific sequence. It will offer the opportunity to break the expected shape that should be run during the radar (active) mode in static steps where the current consumption can be measured.

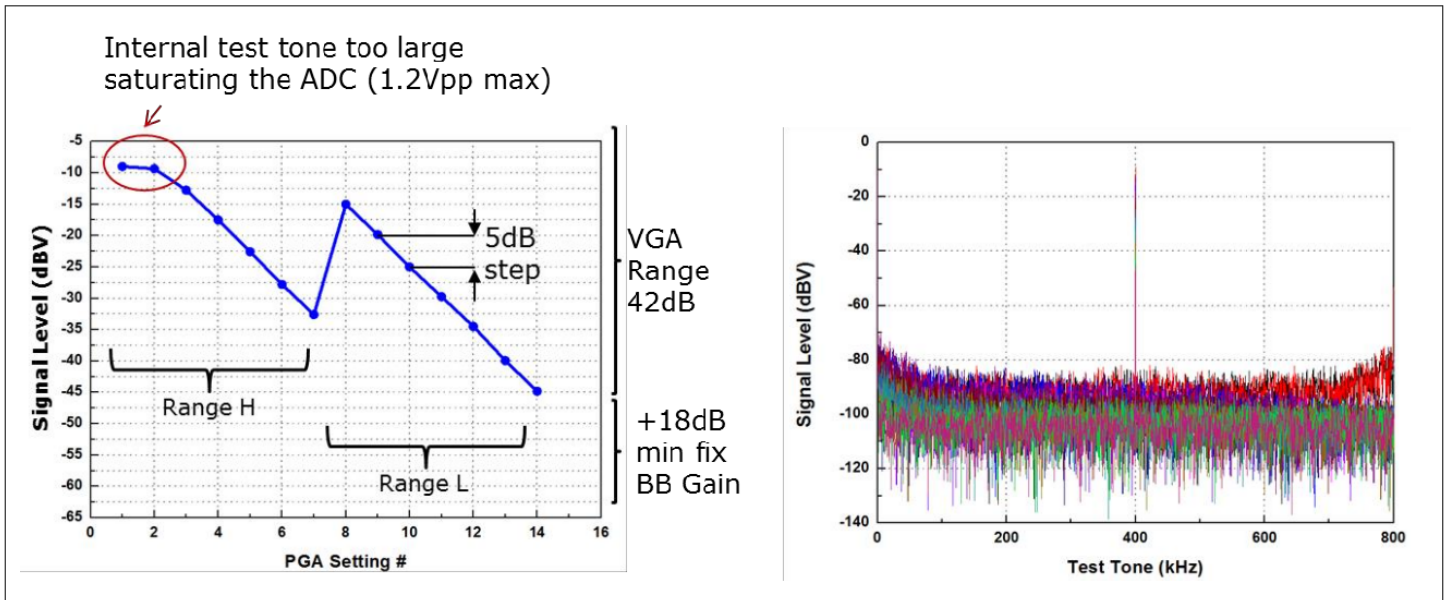
### 11.3.2 Baseband and ADC test mode

A test-tone generator can be used together with the [CW](#) mode. A test signal source derived from the system clock can be activated in the analog receiver chain; the same in each Rx chain. This test signal can be programmed in the register RFT0 (see [RF test register 0](#)). The test tone can propagate through to each baseband chain by enabling a dedicated path. The MADC is triggered by the TRIG7 and will sample the number of samples specified in the APU1 (see [PLL shape x register 3](#)). To run a new measurement, an FSM-reset is required.



**Figure 58 Baseband/ADC test block diagram**

This feature represents a very convenient way to test and debug a complete system. The customer can program a dedicated frequency, set the baseband gain and cutoff filter of the *HPF* (Channel set up x register 2), set the *ADC*, and readout via *SPI* the sampled data into the *AP* or *MCU* to verify if the complete baseband chain is working as expected. The following figure shows one example of *ADC* readout when the baseband is fed with a test tone at 400 kHz internally derived from the *OSC\_IN* input. Different readouts from different *VGA* settings are reported.



**Figure 59 Example: ADC readout after FFT**

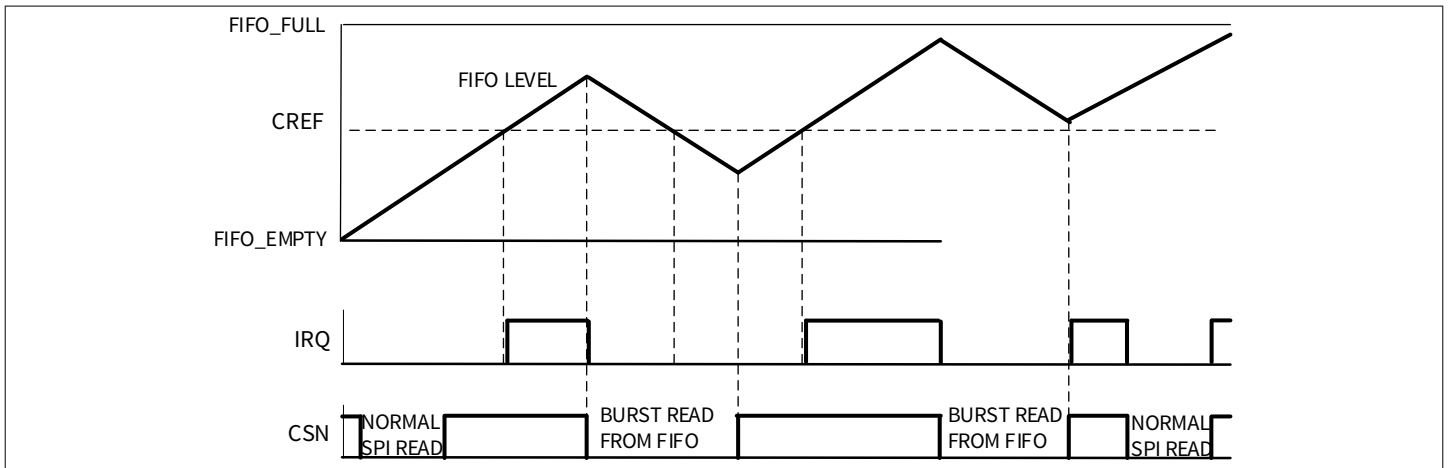
## 11.4 IRQ output

BGT60ATR24AIP provides one interrupt pin output *IRQ*. In default mode, the *IRQ* pin is used to monitor the filling level of the *FIFO* as described below.

**IRQ status definition:**

- IRQ is high after:
  - CSN goes high and  $FSTAT:FILL\_STATUS \geq SFCTL:FIFO\_CREF$  (see [SPI and FIFO control register](#) and [FIFO status register](#))
- IRQ is low (as a consequence of):
  - CSN goes high and  $FSTAT:FILL\_STATUS < SFCTL:FIFO\_CREF$  (see also [Chapter 4.9](#) and [Chapter 4.48](#))
  - CSN is active low

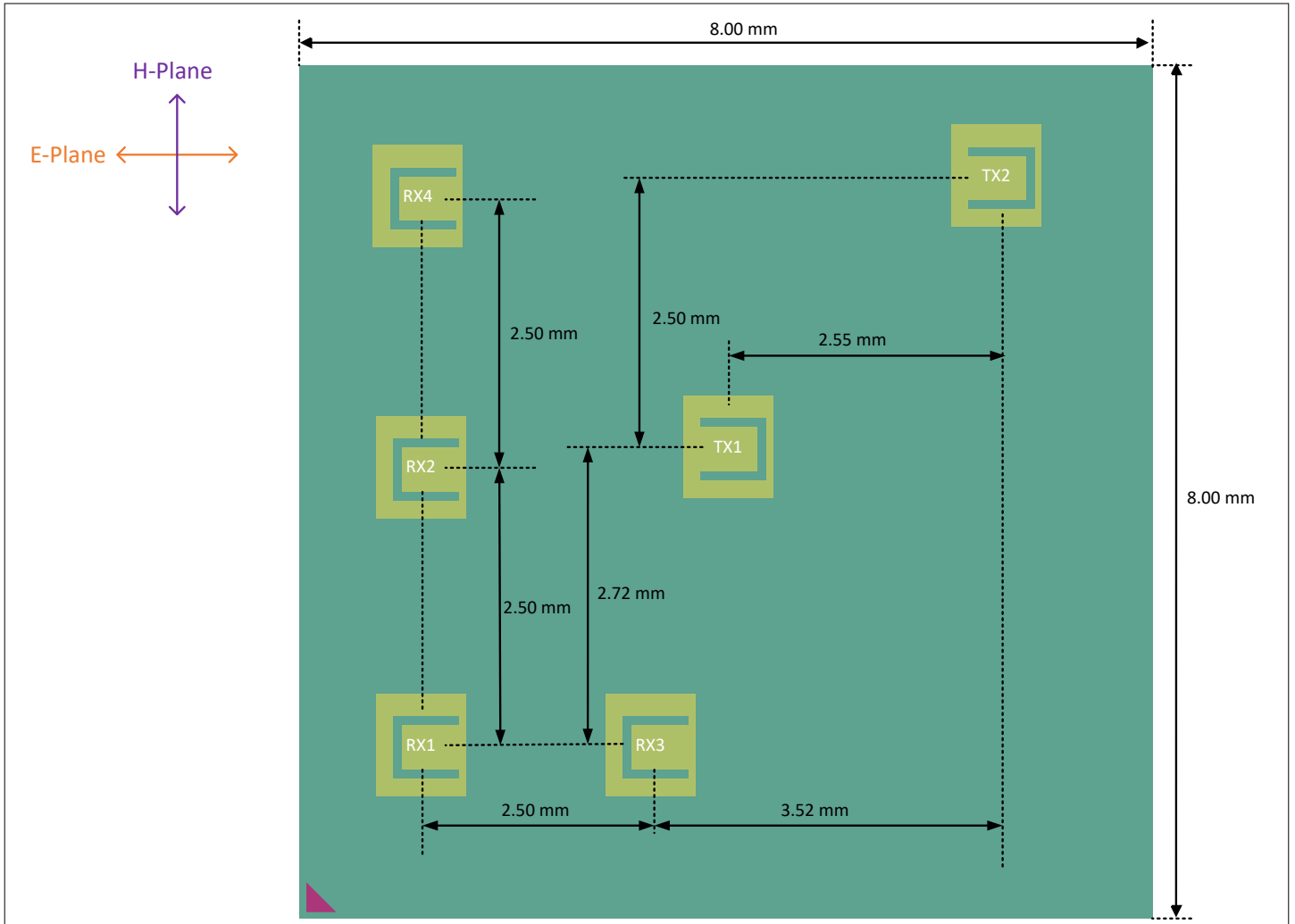
The following figure shows the IRQ signal in case of FIFO burst reads.



**Figure 60** IRQ status behavior during radar mode with FSM capturing data

## 12 Package

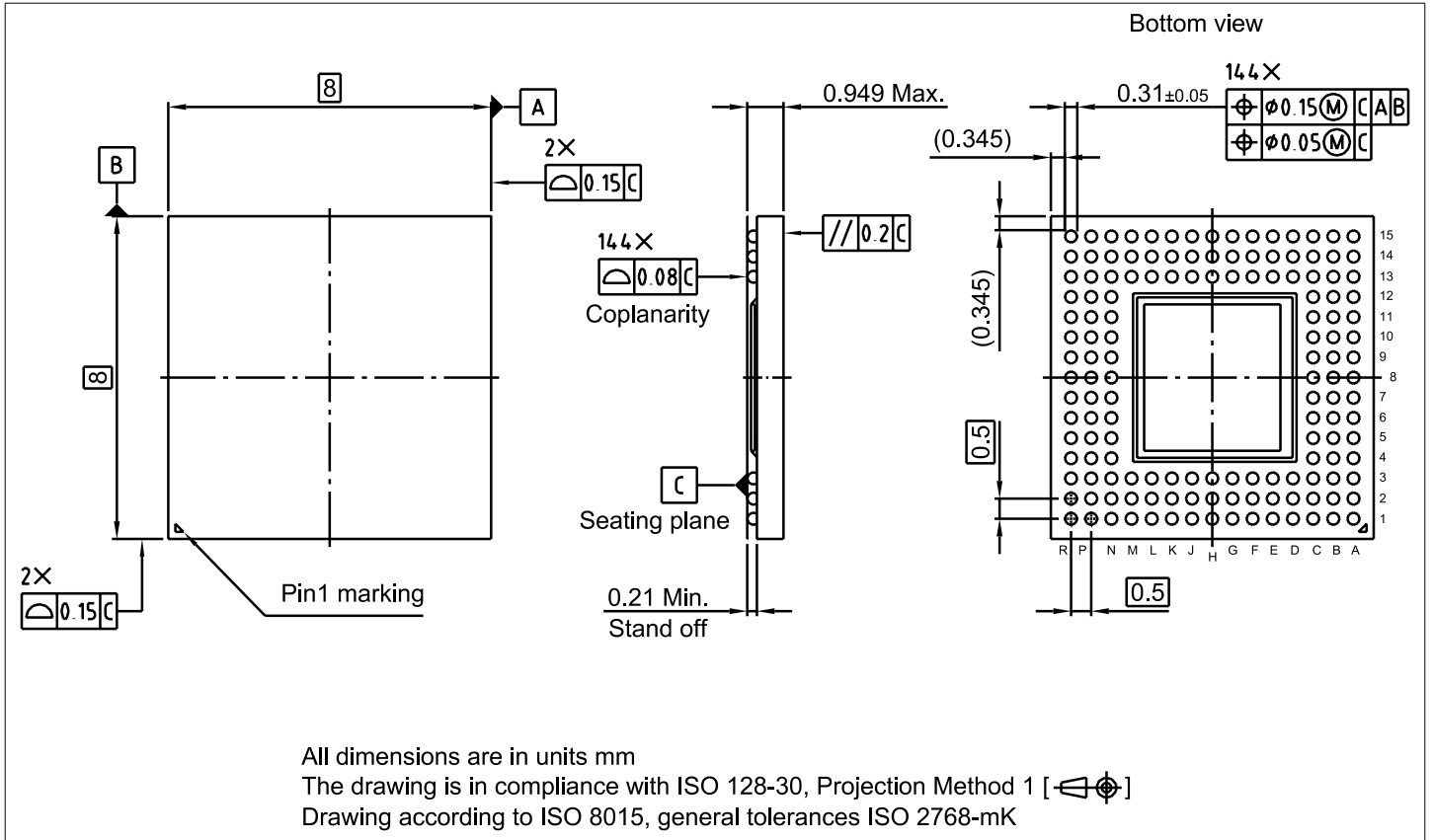
The BGT60ATR24AIP chip is housed in a laminate package with solder balls of 300 µm diameter and integrates the antennas. According to IPC/JEDEC's J-STD0, the *moisture sensitivity level (MSL)* is 3. Figure 61 shows the top view of BGT60ATR24AIP package and the distances of antenna patch midpoints. The bottom view is presented in Figure 62. The package size is 8.0 x 8.0 x 0.862 mm<sup>3</sup> with ball pitch of 500 µm. Package outline is reported on Figure 63. Package name: PG-VF2BGA-144-1.



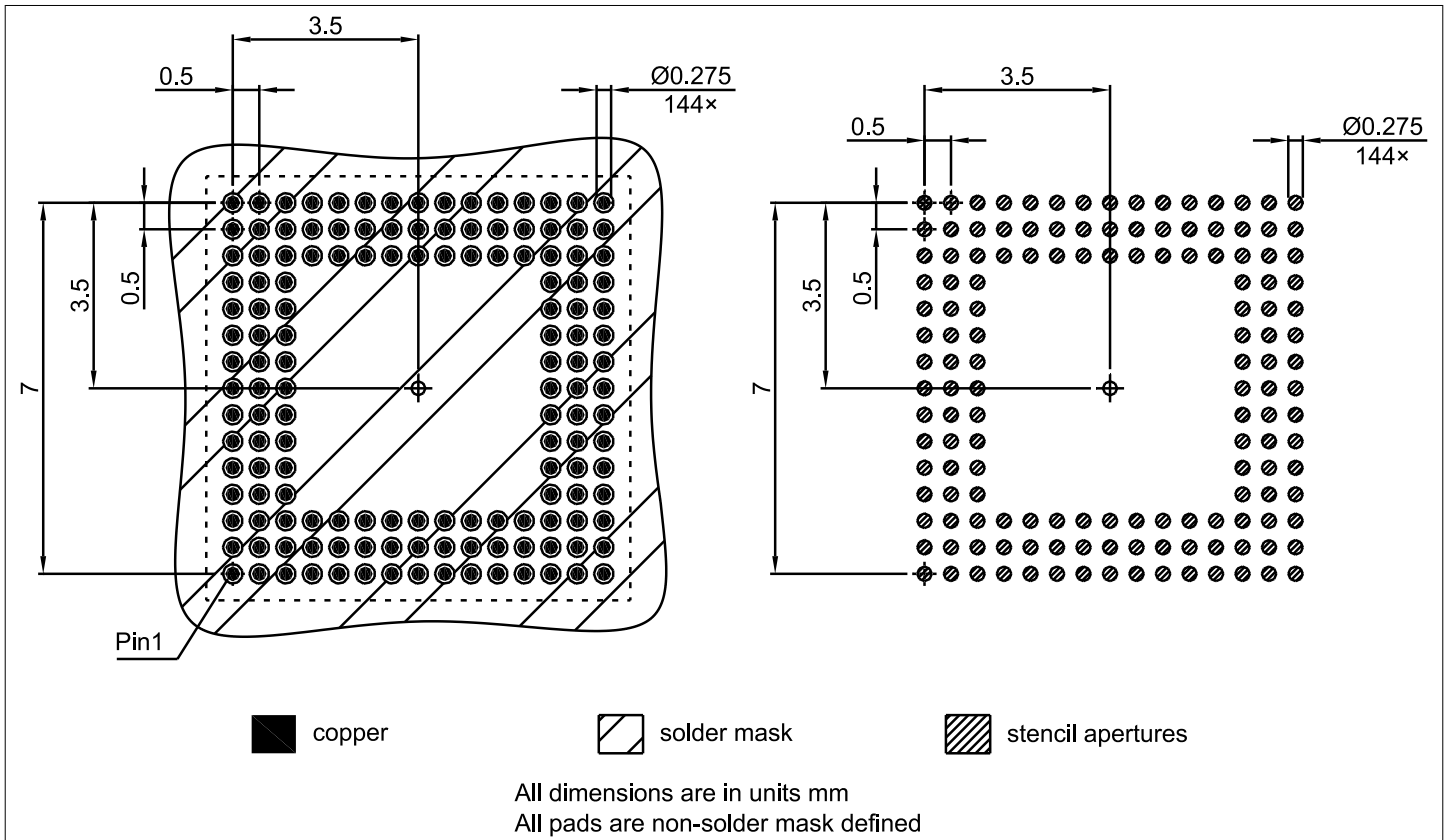
**Figure 61** Top view of BGT60ATR24AIP



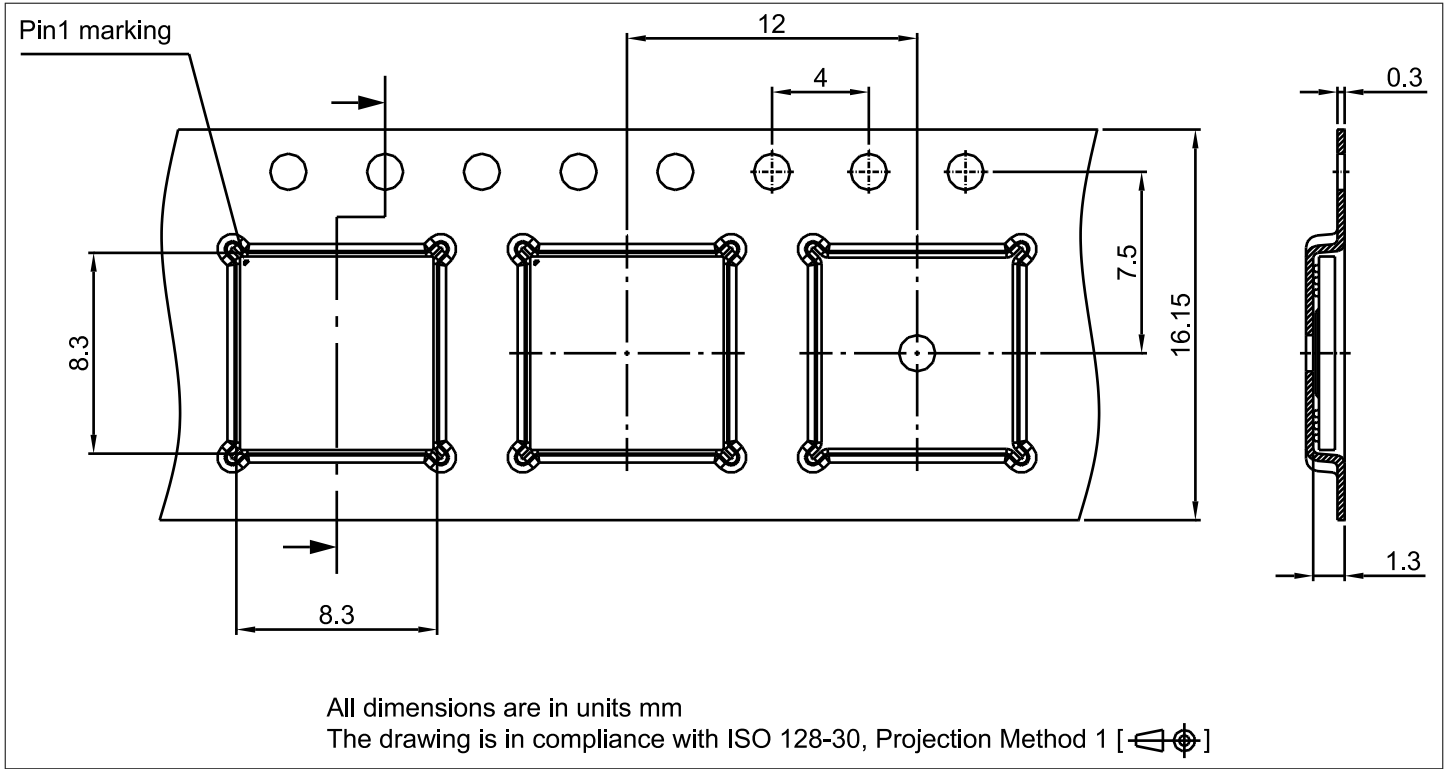
**Figure 62** Bottom view of BGT60ATR24AIP



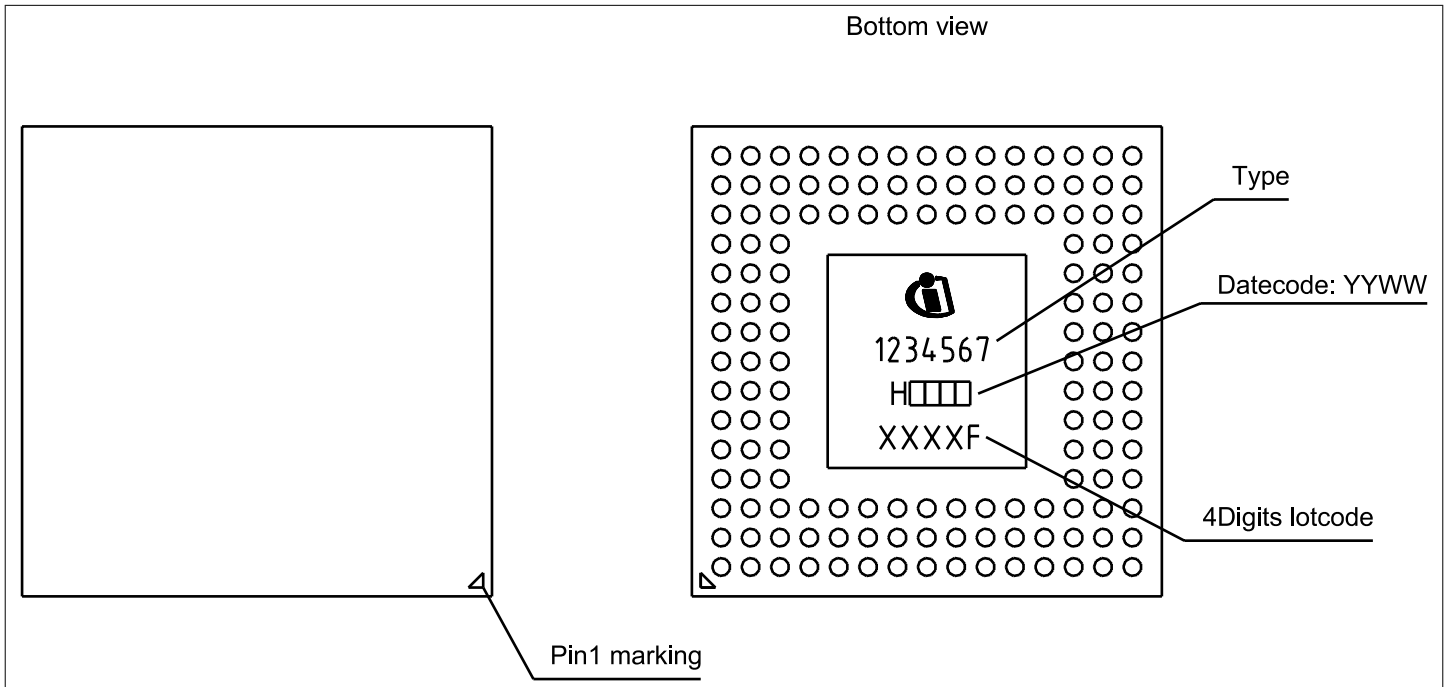
**Figure 63** Package outline PG-VF2BGA-144-1



**Figure 64** Footprint of PG-VF2BGA-144-1



**Figure 65** Tape of PG-VF2BGA-144-1



**Figure 66** Marking pattern details BGT60ATR24AIP

## 12.1 Built-in antenna specifications

Antenna performance reported in the following table are ensured by design. Typical antenna behavior is measured on Infineon reference board (Hatvan+). Typical antenna beam plots are available in a specific application note and upon specific request.

**Table 45** Antennas in package specifications

| Parameter      | Value |      |      | Unit | Condition   |
|----------------|-------|------|------|------|---|
|                | Min.  | Typ. | Max. |      |   |
| $RX_{BW}$      | 57.7  | -    | 62.4 | GHz  | Receiver antenna bandwidth  |
| $TX_{BW}$      | 57.7  | -    | 62.4 | GHz  | Transmitter antenna bandwidth   |
| $G_{TX}$       | -     | 3.5  | -    | dBi  | Antenna gain of a single TX antenna<br>Verified by design                 |
| $G_{RX}$       | -     | 3.5  | -    | dBi  | Antenna gain of a single RX antenna<br>Verified by design                 |
| $FOV_E$        | -     | 108  | -    | Deg  | Field of view of radar mode in the E-plane<br>Verified by design          |
| $FOV_H$        | -     | 115  | -    | Deg  | Field of view of radar mode in the H-plane<br>Verified by design          |
| $ISO_{TX\_RX}$ | -     | 25   | -    | dB   | Isolation from TX antenna to RX antenna in package.<br>Verified by design |

**Attention:** *As of today, it is not possible to test in production the antenna parameters relating to the gain and phase of millimeter-wave antennas integrated into a laminate package. Therefore, deviations of the antenna parameters are not detectable in Infineon's production tests. In addition, the housing of the user's system comprising the Infineon product may impact the antenna parameters. It is the responsibility of the user of the Infineon product to perform an end of line test of user's system which is suitable to detect deviations from the antenna parameters ("End of Line Test"). Infineon assumes no responsibility for failures of Infineon products in case the user has not conducted the End of Line Test for the Infineon products.*

## Glossary

### **AAF**

*anti-aliasing filter (AAF)*

A filter used before a signal sampler to restrict the bandwidth of a signal to satisfy the Nyquist–Shannon sampling theorem over the band of interest.

### **ABB**

*analog base band (ABB)*

A signal that has a near-zero frequency range, this is, a spectral magnitude that is nonzero only for frequencies in the vicinity of the origin and negligible elsewhere.

### **AC**

*alternating current (AC)*

A form of power supply in which the flow of electric charge periodically reverses direction.

### **ADC**

*analog-to-digital converter (ADC)*

A device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

### **AP**

*application processor (AP)*

A chip that is used to run primary user applications.

### **BITE**

*built-in test equipment (BITE)*

Passive diagnosis equipment built into a system to support test processes during production.

### **CDM**

*charged device model (CDM)*

A model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge (ESD).

### **CMOS**

*complementary metal-oxide semiconductor (CMOS)*

A technology for constructing integrated circuits that uses a combination of p-channel and n-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) to implement logic gates.

### **CW**

*continuous wave (CW)*

The emission of a sinusoidal radio wave, which may be modulated by signals.

### **DC**

*direct current (DC)*

A form of power supply in which the flow of electric charge is only in one direction.

### **EOL**

*end of line (EOL)*

The last stage of a production process, where the functional tests are executed.

**ESR**

*equivalent series resistance (ESR)*

The internal alternating current resistance that appears in series with an ideal capacitance or an ideal inductance of the device.

**FIFO**

*first in first out (FIFO)*

A method for organizing the manipulation of a data structure where the first entry is processed first.

**FMCW**

*frequency-modulated continuous wave (FMCW)*

A type of radar system where a known frequency continuous wave radio energy is transmitted and then received from any reflecting object.

**FM**

*frequency-modulated (FM)*

A angle modulation in which the instantaneous frequency deviation varies in accordance with a given function, generally linear, of the instantaneous value of the modulating signal.

**FSM**

*finite state machine (FSM)*

An abstract machine that can be in exactly one of a finite number of states at any given time.

**HBM**

*human body model (HBM)*

A model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge (ESD) based on a human body.

**HPF**

*high-pass filter (HPF)*

An electronic filter that passes signals with a frequency higher than a certain cutoff frequency and attenuates signals with frequencies lower than the cutoff frequency.

**HW**

*hardware (HW)*

The collection of physical components that comprise a computer or any other electronic system.

**IBIS**

*Input/output Buffer Information Specification (IBIS)*

A specification of a method for integrated circuit (IC) vendors to provide information about the input/output buffers of their product to their prospective customers without revealing the intellectual property of their implementation.

**IF**

*intermediate frequency (IF)*

The frequency corresponding to the carrier frequency or another characteristic frequency of an input radio-frequency signal in a signal resulting from each frequency translation.

**LDO**

*low-dropout voltage regulator (LDO)*

A direct current linear voltage regulator that can regulate the output voltage even if the supply voltage is very close to the output voltage.

**LFSR**

*linear feedback shift register (LFSR)*

A shift register whose input bit is a linear function of its previous state.

**LO**

*local oscillator (LO)*

An electronic oscillator used with a mixer to change the frequency of a signal.

**LSB**

*least significant bit (LSB)*

The binary digit of the least significance within a code word.

**MCU**

*microcontroller unit (MCU)*

A small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals.

**MISO**

*master in, slave out (MISO)*

The input line of a serial peripheral interface master.

**MOSI**

*master out, slave in (MOSI)*

The output line of a serial peripheral interface master.

**MSB**

*most significant bit (MSB)*

The binary digit of the most significance within a code word.

**MSL**

*moisture sensitivity level (MSL)*

An electronic standard for the time period in which a moisture-sensitive device can be exposed to ambient room conditions.

**NDA**

*non-disclosure agreement (NDA)*

A legal contract or part of a contract between at least two parties that outlines confidential material, knowledge, or information that the parties wish to share with one another for certain purposes, but wish to restrict access to.

**PCB**

*printed circuit board (PCB)*

A board that mechanically supports and electrically connects electronic components using conductive tracks, pads, and other features etched from copper sheets laminated onto a non-conductive substrate.

**PLL**

*phase-locked loop (PLL)*

A feedback circuit for synchronizing an oscillator with the phase of an input signal.

**RF**

*radio frequency (RF)*

A frequency of a periodic radio wave or of the corresponding electric oscillation.

**RSVD**

*reserved (RSVD)*

A placeholder for future functionalities or features.

**RX**

*receiver (RX)*

A device that accepts signals from remote transmitters.

**SAR**

*successive approximation register (SAR)*

A type of analog-to-digital converter that converts a continuous analog waveform into a discrete digital representation using a binary search through all possible quantization levels.

**SPI**

*serial peripheral interface (SPI)*

A synchronous serial communication interface specification used for inter-chip communication, primarily in embedded systems.

**STS**

*simplified timing shell (STS)*

A wrapper around a module that includes timing information to enable static timing checks for this module.

**SW**

*software (SW)*

The collection of non-physical components that comprise a set of instructions executed by a processor.

**TX**

*transmitter (TX)*

A device that sends out signals.

**VCO**

*voltage controlled oscillator (VCO)*

An oscillator whose frequency is a function of the voltage of an input signal.

**VGA**

*variable gain amplifier (VGA)*

An electronic amplifier that varies its gain depending on a control voltage.

## Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|------------------------|
| 1.0              | 2026-03-12      | Initial release        |

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