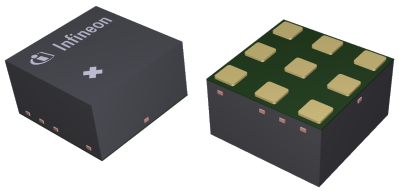
BGS14WMA9

Wideband SP4T Diversity Switch with High Switching Speed

Features

- High switching speed
- High linearity up to 26 dBm input power
- Low insertion loss and high port to port isolation up to 6 GHz
- Low current consumption
- MIPI RFFE 2.1 compliant control interface
- Software programmable MIPI RFFE USID
- RoHS and WEEE compliant package



1.1 x 1.1 mm^2

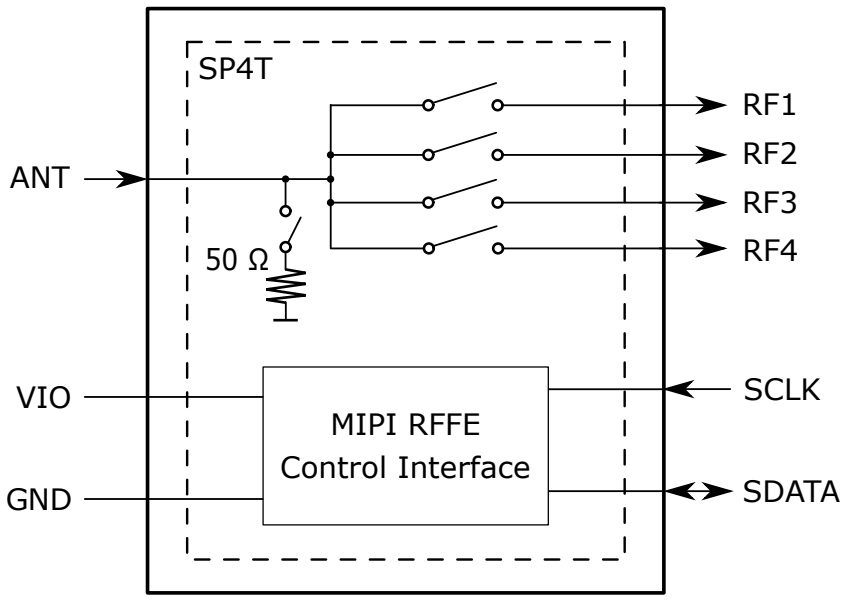
Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Potential Applications

The BGS14WMA9 RF switch is specifically designed for WLAN and Bluetooth applications. Any of the 4 ports can be used as termination of the diversity antenna, handling up to 26 dBm.

Block Diagram



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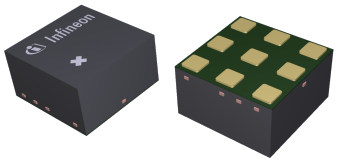
1 Features



- RF CMOS SP4T antenna diversity switch with power handling capability of up to 26 dBm
- High switching speed
- Suitable for WLAN and Bluetooth applications
- 0.05 to 6.0 GHz coverage for FM Radio, LTE, LAA and 5G application
- Low insertion loss and harmonics generation, high port to port isolation up to 6 GHz
- Low current consumption
- On chip control logic including ESD protection
- Fully compatible with MIPI RFFE 2.1 standard operating in 1.65 to 1.95 V voltage range
- Software programmable MIPI RFFE USID
- USID swap feature
- Small form factor of 1.1 x 1.1 mm^2
- No blocking capacitors required if no DC applied on RF lines
- No power supply decoupling required
- 50 Ω termination enabling at isolation mode
- High EMI robustness
- RoHS and WEEE compliant package

RoHS Halogen-Free Lead-Free Green

Description

BGS14WMA9 is a Single Pole Four Throw (SP4T) diversity switch which is specifically designed for WLAN and Bluetooth applications in a very compact 9 pin package with very small size of only 1.1 x 1.1 mm^2 and thickness of 0.55 mm.
Any of the 4 ports can be used as termination of the diversity antenna handling up to 26 dBm.
Unlike GaAs technology, external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally.
BGS14WMA9 RF switch is manufactured in Infineon's patented MOS technology, offering the performance of GaAs with the economy and integration of conventional CMOS including the inherently higher ESD robustness.

Product Name	Marking	Package
BGS14WMA9	M1	PG-ATSLP-9-50

2 Maximum Ratings

Table 1: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range [1]	f	0.05	–	6.0	GHz	
RFFE supply voltage [2]	V_{IO}	-0.5	–	2.2	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF input power	P_{RF}	–	–	28	dBm	At all RF ports, CW / VSWR 1:1 / 50 Ω
ESD capability, CDM [3]	$V_{ESD,CDM}$	-1	–	+1	kV	
ESD capability, HBM [4]	$V_{ESD,HBM}$	-1	–	+1	kV	
ESD capability RF ports, SLT[5]	$V_{ESD,RF}$	-8	–	+8	kV	Each RF port versus GND, with 27 nH shunt inductor
		-6	–	+6	kV	Each RF port versus GND, with 56 nH shunt inductor
Junction temperature	T_j	–	–	125	°C	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0 V.
[2] Note: Consider potential ripple voltages on top of V_{IO}. Including RF ripple, V_{IO} must not exceed the maximum ratings: $V_{IO} = V_{DC} + V_{Ripple}$.
[3] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C = 100 pF).
[5] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Table 2: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction - soldering point	R_{thJS}	–	–	95	K/W	–
Maximum DC-voltage on RF ports and RF ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF ports

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

3 Operation Ranges

Table 3: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[1]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
Supply current	I_{IO}	–	60	150	µA	Operating State
Supply current, stand-by	$I_{IO,sb}$	–	2	5	µA	Idle State, power down mode
Ambient temperature	T_A	-40	25	85	°C	–

[1]SCLK and SDATA

Table 4: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF input power	P_{RF}	–	–	26	dBm	CW / VSWR 1:1 / 50 Ω

4 RF Characteristics

Table 5: RF Characteristics at T_A = 25 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.8 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[1]						
All RF Ports	*IL*	–	0.21	0.26	dB	50–698 MHz
		–	0.22	0.28	dB	699–960 MHz
		–	0.27	0.37	dB	1200–2170 MHz
		–	0.35	0.45	dB	2171–2690 MHz
		–	0.62	0.85	dB	3300–4200 MHz
		–	0.88	1.15	dB	4400–5000 MHz
		–	1.15	1.45	dB	5150–5925 MHz

[1] Measured on application board, without any matching components.

Table 6: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss[1]						
All RF Ports	*IL*	–	0.21	0.35	dB	50–698 MHz
		–	0.22	0.38	dB	699–960 MHz
		–	0.27	0.51	dB	1200–2170 MHz
		–	0.35	0.59	dB	2171–2690 MHz
		–	0.62	0.97	dB	3300–4200 MHz
		–	0.88	1.29	dB	4400–5000 MHz
		–	1.15	1.74	dB	5150–5925 MHz
Return Loss[1]						
All RF Ports	*RL*	24	32	–	dB	50–698 MHz
		21	28	–	dB	699–960 MHz
		15	21	–	dB	1200–2170 MHz
		13	17	–	dB	2171–2690 MHz
		9	12	–	dB	3300–4200 MHz
		8	10	–	dB	4400–5000 MHz
		7	8	–	dB	5150–5925 MHz

[1] Measured on application board, without any matching components.

Table 7: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Isolation[1]						
ANT_RF1 vs RFx	*ISO*	44	53	–	dB	50–698 MHz
		41	46	–	dB	699–960 MHz
		33	39	–	dB	1200–2170 MHz
		30	35	–	dB	2171–2690 MHz
		24	30	–	dB	3300–4200 MHz
		22	27	–	dB	4400–5000 MHz
		20	25	–	dB	5150–5925 MHz
Isolation[1]						
ANT_RF2 vs RFx	*ISO*	44	54	–	dB	50–698 MHz
		41	46	–	dB	699–960 MHz
		33	39	–	dB	1200–2170 MHz
		30	35	–	dB	2171–2690 MHz
		25	30	–	dB	3300–4200 MHz
		22	27	–	dB	4400–5000 MHz
		20	25	–	dB	5150–5925 MHz
Isolation[1]						
ANT_RF3 vs RFx	*ISO*	41	55	–	dB	50–698 MHz
		39	47	–	dB	699–960 MHz
		31	39	–	dB	1200–2170 MHz
		28	34	–	dB	2171–2690 MHz
		23	28	–	dB	3300–4200 MHz
		21	25	–	dB	4400–5000 MHz
		19	23	–	dB	5150–5925 MHz
Isolation[1]						
ANT_RF4 vs RFx	*ISO*	41	55	–	dB	50–698 MHz
		38	47	–	dB	699–960 MHz
		31	39	–	dB	1200–2170 MHz
		28	34	–	dB	2171–2690 MHz
		24	29	–	dB	3300–4200 MHz
		21	26	–	dB	4400–5000 MHz
		19	23	–	dB	5150–5925 MHz
Isolation[1]						
RF-on to RF-off	*ISO*	40	59	–	dB	50–698 MHz
		37	51	–	dB	699–960 MHz
		29	42	–	dB	1200–2170 MHz
		27	37	–	dB	2171–2690 MHz
		21	32	–	dB	3300–4200 MHz
		18	28	–	dB	4400–5000 MHz
		17	26	–	dB	5150–5925 MHz

[1] Measured on application board, without any matching components.

Table 8: RF Characteristics at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Harmonic Generation[1] at P_{RF} = 26 dBm, CW, VSWR 1:1 / 50 Ω						
2nd Harmonic	P_{H2}	–	-82	-69	dBm	600–915 MHz
		–	-80	-67	dBm	1447–1980 MHz
		–	-76	-55	dBm	2300–2690 MHz
3nd Harmonic	P_{H3}	–	-64	-60	dBm	600–915 MHz
		–	-61	-56	dBm	1447–1980 MHz
		–	-58	-52	dBm	2300–2690 MHz
Intermodulation Distortion [1]						
2nd order intermodulation	*IMD*2	–	-109	-90	dBm	*IMD*2 testcases, see Tab. 9
3rd order intermodulation	*IMD*3	–	-106	-90	dBm	*IMD*3 testcases, see Tab. 10
Intercept point[1]						
2nd order intercept point	*IIP*2	97	114	–	dBm	*IMD*2 testcases, see Tab. 9
3rd order intercept point	*IIP*3	58	65	–	dBm	*IMD*3 testcases, see Tab. 10

[1] Measured on application board, without any matching components.

Table 9: IMD2 Testcases

Band	Symbol	In-Band Frequency (MHz)	Blocker Frequency 1 (MHz)	Blocker Power 1 (dBm)	Blocker Frequency 2 (MHz)	Blocker Power 2 (dBm)
Band 1	$B1_{IMD2,high}$	2140	1950	20	4090	-15
	$B1_{IMD2,low}$	2140	1950	20	190	-15
Band 4	$B4_{IMD2,high}$	2132	1732	20	3864	-15
	$B4_{IMD2,low}$	2132	1732	20	400	-15
Band 5	$B5_{IMD2,high}$	881.5	836.5	20	1718	-15
	$B5_{IMD2,low}$	881.5	836.5	20	45	-15
Band 7	$B7_{IMD2,high}$	2655	2535	20	5190	-15
	$B7_{IMD2,low}$	2655	2535	20	120	-15

Table 10: IMD3 Testcases

Band	Symbol	In-Band Frequency (MHz)	Blocker Frequency 1 (MHz)	Blocker Power 1 (dBm)	Blocker Frequency 2 (MHz)	Blocker Power 2 (dBm)
Band 1	$B1_{IMD3,high}$	2140	1950	20	6040	-15
	$B1_{IMD3,mid}$	2140	1950	20	1760	-15
Band 4	$B4_{IMD3,high}$	2132	1732	20	5596	-15
	$B4_{IMD3,mid}$	2132	1732	20	1332	-15
Band 5	$B5_{IMD3,high}$	881.5	836.5	20	2554.5	-15
	$B5_{IMD3,mid}$	881.5	836.5	20	791.5	-15
Band 7	$B7_{IMD3,high}$	2655	2535	20	7725	-15
	$B7_{IMD3,mid}$	2655	2535	20	2415	-15

Table 11: Switching Time at T_A = −40 °C...85 °C, P_{IN} = 0 dBm, Supply Voltage V_{IO} = 1.65...1.95 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Time						
Power Up Settling Time	t_{PUP}	–	10	20	µs	Time from Power Up plus Switch command, 50 % last SCLK falling edge to 90 % RF signal
Switching Time	t_{ST}	–	120	150	ns	Time to switch between RF states, 50 % last SCLK falling edge to 90 % RF signal
RF Rise Time	t_{RT}	–	60	75	ns	Time between 10 % to 90 % RF signal

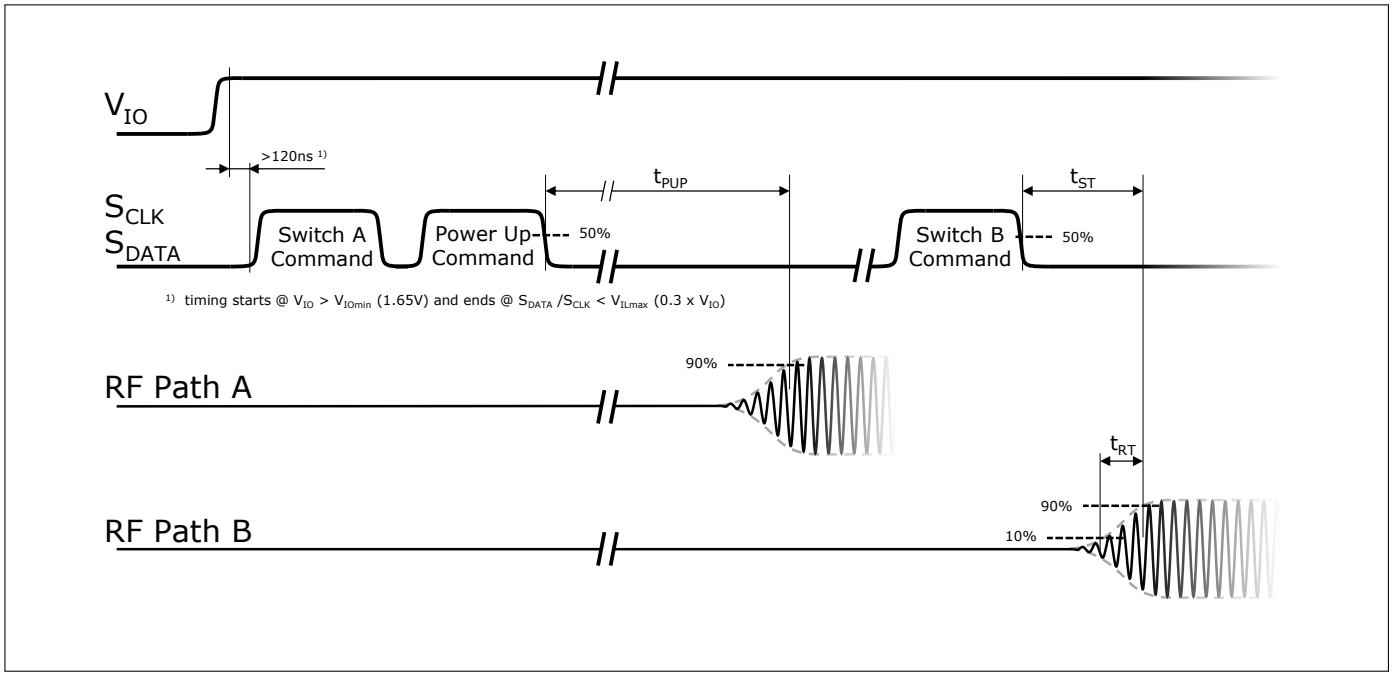


Figure 1: MIPI Timing Diagram

5 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance DRAFT Specification for RF Front-End Control Interface' document version 2.1 Release 10 - 18. December 2017.

Table 12: MIPI Features

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	Backward compatible to MIPI 2.0 standard
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz for read and write
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz for write
Half speed read	Yes	
Full speed read	Yes	
Full speed write	Yes	
Longer Reach RFFE Bus Length Feature	Yes	
Programmable driver strength	Yes	Up to 80 pF
Programmable Group SID	Yes	
Programmable USID	Yes	Support for three registers write and extended write sequences
Trigger functionality	Yes	
Extended Triggers and Trigger Masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID_Sel pin	No	External pin for changing USID is not implemented
USID selection via SDATA / SCLK swap feature	Yes	1: Default → 0x0A 2: SCLK/SDATA swap → 0x0B (SCLK connected to SDATA pin and SDATA connected to SCLK pin)

Table 13: Startup Behavior

Feature	State	Comment
Power status	Low power	Lower power mode after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 14: Register Mapping, Table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	REGISTER_0	7:0	MODE_CTRL	RF Switch Control	00000000	No	Yes Trigger 0-10	R/W MW
0x1C	PM_TRIG	7	PWR_MODE(1) Operation Mode	0: Normal operation (ACTIVE)	1	Yes	No	R/W MW
				1: Low Power Mode (LOW POWER)				
		6	PWR_MODE(0) State Bit Vector	0: No action (ACTIVE)	0			
				1: Powered Reset (STARTUP to ACTIVE to LOW POWER)				
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG)	0	No		
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_2	0: No action (data held in shadow REG)	0	Yes		
				1: Data transferred to active REG				
		1	TRIGGER_1	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_0	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	00011110	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:4	MANUFACTURER_ID [11:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	0001			
		3:0	USID[3:0]	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device.	See Tab. 12	No	No	R/W

Table 15: Register Mapping, Table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID		00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION		0101	No	No	R/W
		3:0	SUB_REVISION		0000			
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	No	R/W
		3:0	RESERVED	Reserved for secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	No	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x2B	BUS_LD	7:3	RESERVED	Reserved for future use	0x0	No	No	R/W
		2:0	BUS_LD[2:0]	Programs the drive strength of the SDATA driver in readback modes. 0x0: Reserved for future use 0x1: Reserved for future use 0x2: Reserved for future use 0x3: Reserved for future use 0x4: 50pF 0x5: 60pF 0x6: 80pF 0x7: 80pF	0x4			
0x2D	EXT_TRIG_MASK	7	TRIGGER_MASK_10	0: Data masked (held in shadow REG)	0	No	No	R/W MW
				1: Data not masked (ready for transfer to active REG)				
		6	TRIGGER_MASK_9	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		5	TRIGGER_MASK_8	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		4	TRIGGER_MASK_7	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		3	TRIGGER_MASK_6	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		2	TRIGGER_MASK_5	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		1	TRIGGER_MASK_4	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				
		0	TRIGGER_MASK_3	0: Data masked (held in shadow REG)	0			
				1: Data not masked (ready for transfer to active REG)				

Table 16: Register Mapping, Table III

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x2E	EXT_TRIG	7	TRIGGER_10	0: No action (data held in shadow REG)	0	Yes	No	R/W MW
				1: Data transferred to active REG				
		6	TRIGGER_9	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		5	TRIGGER_8	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		4	TRIGGER_7	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		3	TRIGGER_6	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		2	TRIGGER_5	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		1	TRIGGER_4	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				
		0	TRIGGER_3	0: No action (data held in shadow REG)	0			
				1: Data transferred to active REG				

Table 17: Modes of Operation (Truth Table, Register_0)

			REGISTER Bits							
State	Value (Hex.)	Mode	D7[1)]	D6	D5	D4	D3	D2	D1	D0
1	0x00	ALL OFF (Isolation)	0	0	0	0	0	0	0	0
2	0x01	RF1 ON	0	0	0	0	0	0	0	1
3	0x02	RF2 ON	0	0	0	0	0	0	1	0
4	0x04	RF3 ON	0	0	0	0	0	1	0	0
5	0x08	RF4 ON	0	0	0	0	1	0	0	0
6	0x10	ALL OFF (Isolation) with 50 Ω termination	0	0	0	1	0	0	0	0

[1)] Reserved

6 Package Information

The switch has a package size of 1100 µm in X-dimension and 1100 µm in Y-dimension with a maximum deviation of ±50 µm in each dimension. Fig. 2 shows the footprint from top view. The definition of each pin can be found in Tab. 19.

Table 18: Mechanical Data

Parameter	Symbol	Value	Unit
Package X-dimension	*X*	1100 ± 50	µm
Package Y-dimension	*Y*	1100 ± 50	µm
Package height	*H*	550 ± 50	µm

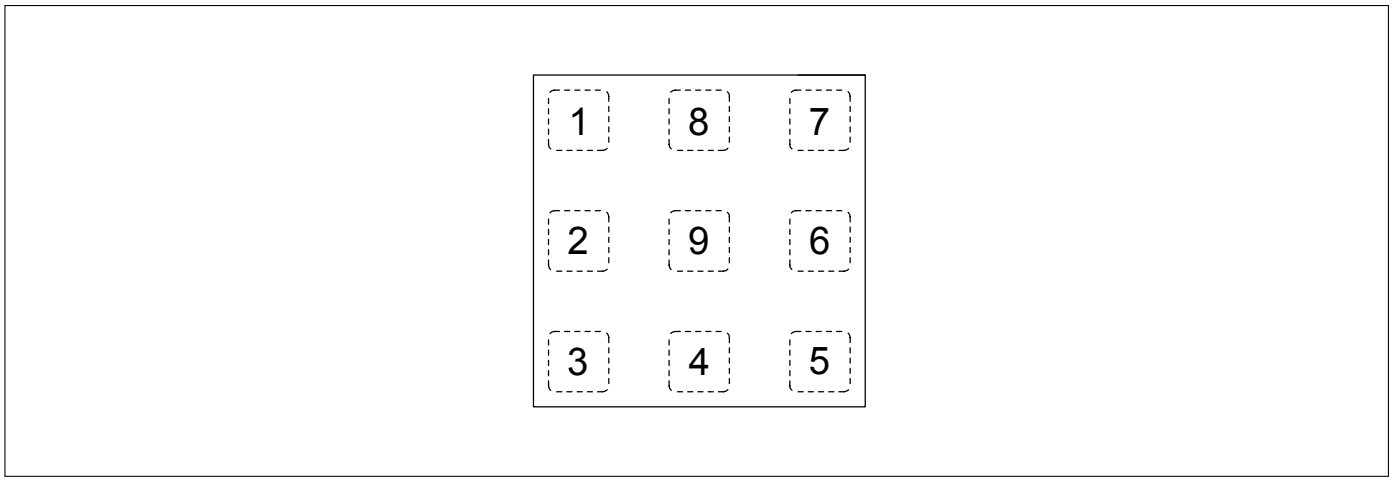


Figure 2: Footprint (top view)

Table 19: Pin Definition

No.	Name	Pin Type	Function
1	VIO	Power	Power Supply
2	RF4	RF	Rx port
3	RF2	RF	Rx port
4	ANT	RF	RF Input
5	RF1	RF	Rx port
6	RF3	RF	Rx port
7	SDATA	I/O	MIPI RFFE
8	SCLK	I/O	MIPI RFFE Clock (Input)
9	GND	Ground	Ground

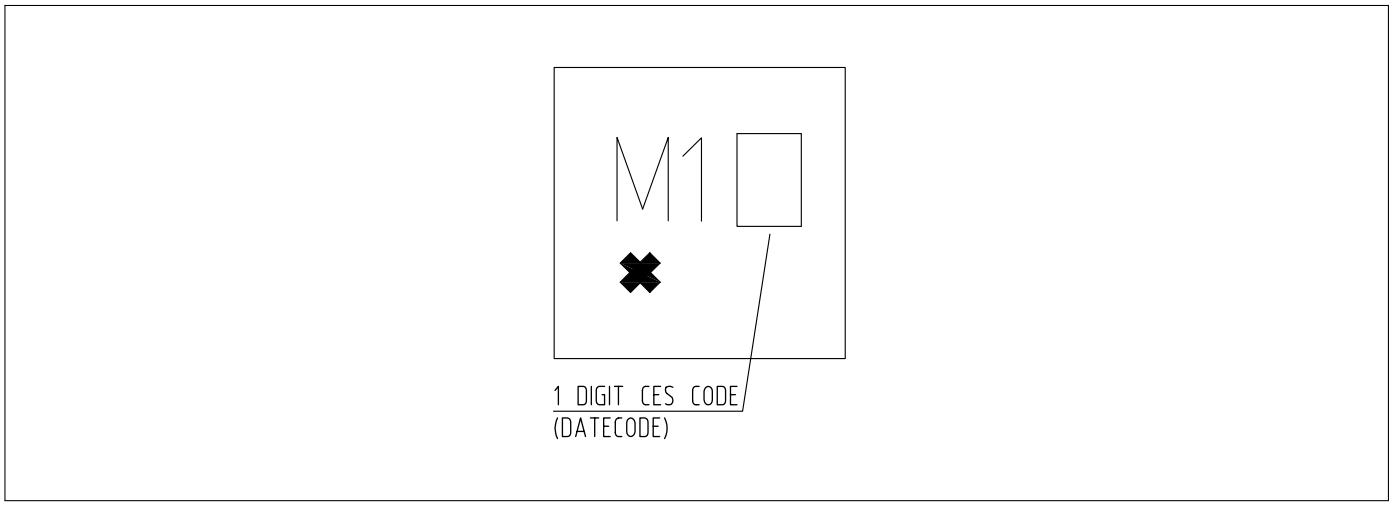


Figure 3: Marking Specification (top view)

Table 20: Monthly Date Code Marking

Month	2019	2020	2021	2022	2023	2024	2025	2026
1	a	p	A	P	a	p	A	P
2	b	q	B	Q	b	q	B	Q
3	c	r	C	R	c	r	C	R
4	d	s	D	S	d	s	D	S
5	e	t	E	T	e	t	E	T
6	f	u	F	U	f	u	F	U
7	g	v	G	V	g	v	G	V
8	h	x	H	X	h	x	H	X
9	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5

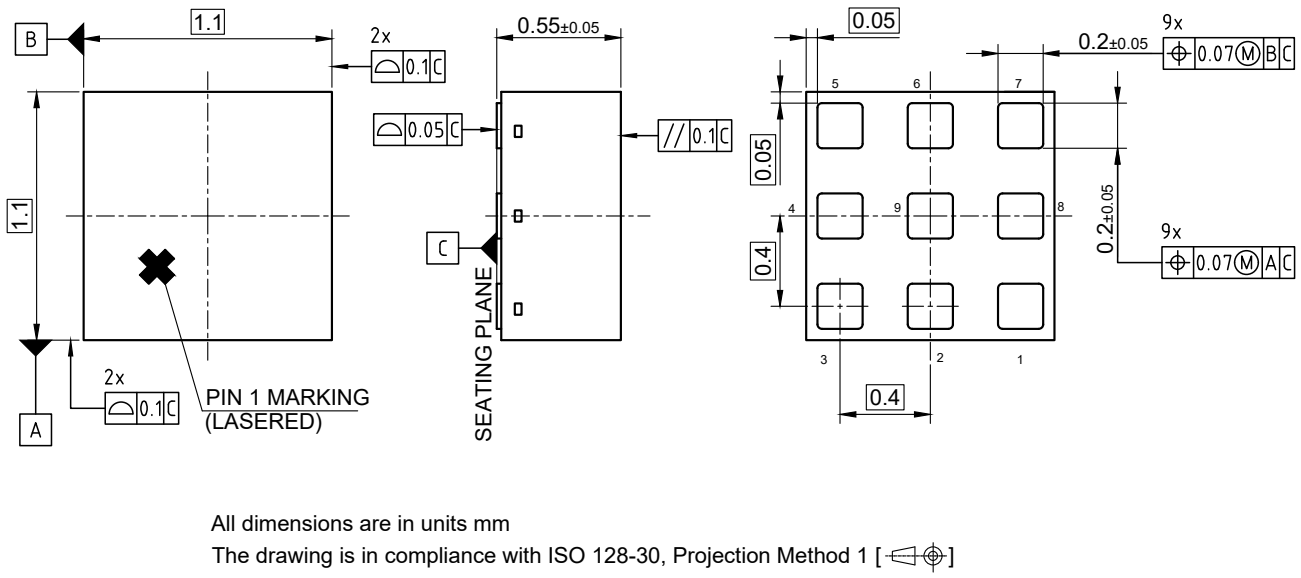


Figure 4: Package Outline (top, side and bottom views)

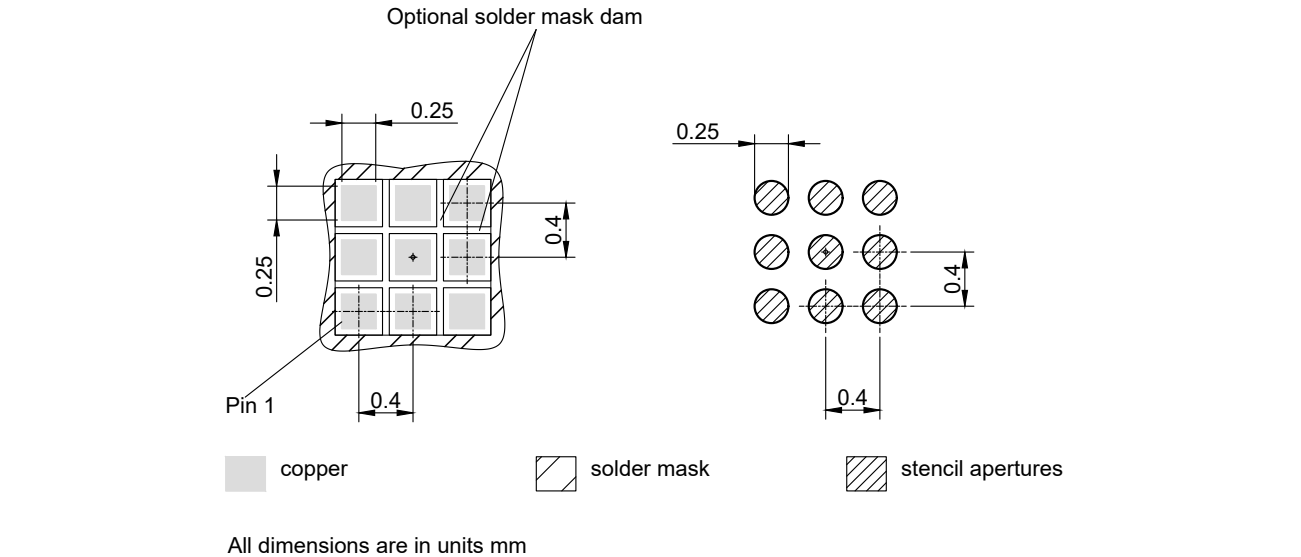


Figure 5: Footprint Recommendation

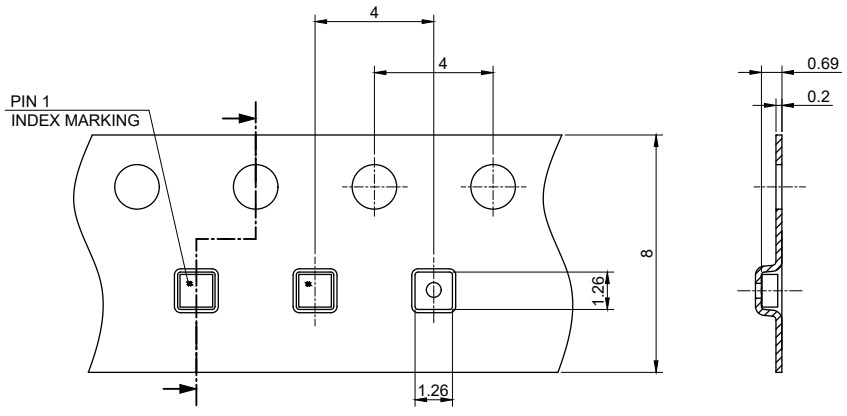


Figure 6: Carrier Tape (top and side views)

Revision History	
Preliminary, Revision 2.1 - 2020-05-27	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.2, 2020-06-18	
15	Package Outline drawing updated in Figure 4
15	Footprint Recommendation drawing updated in Figure 5

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