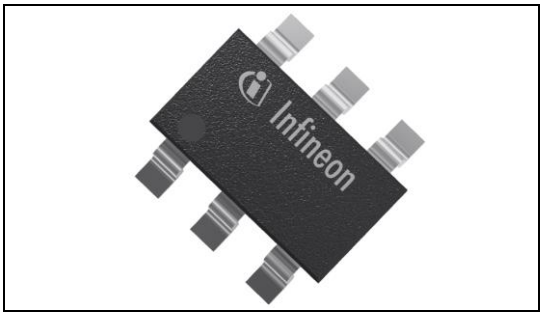
Single-channel low-side radiation tolerant gate driver IC

BDP1CG15NB-01



Features

- 8 A sink driving capability
- 20 ns propagation delay
- 8 V / 7 V UVLO On/Off
- Single Event Effect (SEE) tolerant
  up to Linear Energy Transfer (LET) = 45 MeVcm^2/mg
- Total Ionisation Dose (TID) tolerant
  up to 30 kRad(Si)

Product validation

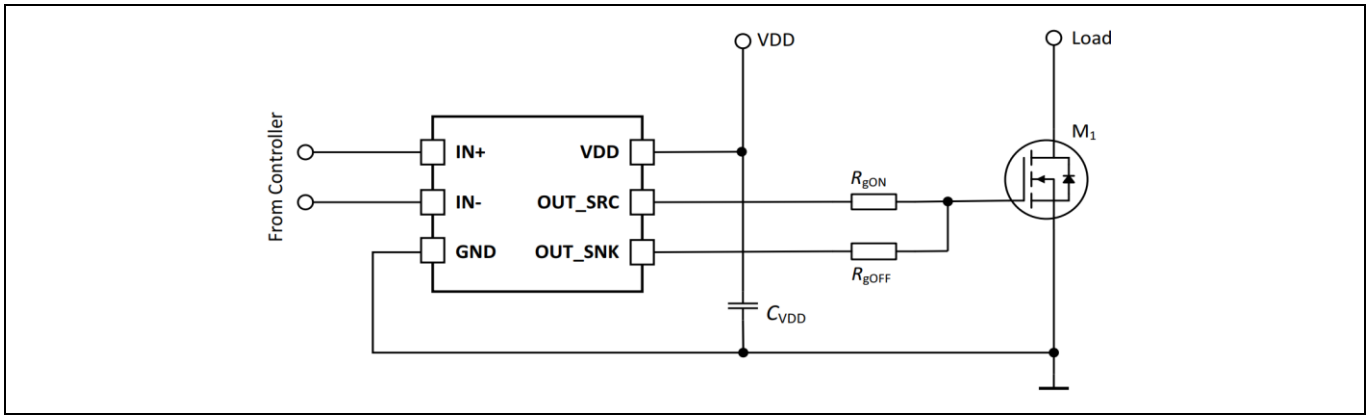
Qualified for space applications according to the relevant tests of JEDEC[1]

TID irradiation according to ESCC 22900 standard[2]

Description

Table 1 Product information

Type	UVLO On / Off	Output Configuration	Output Current	Package
BDP1CG15NB-01	8 V / 7 V	Separated source and sink	-8 A / +4 A	PG-SOT23-6



[1] J-STD20 and JESD22

[2] TID irradiation testing for this device conforms to the ESCC 22900 standard. Parameters specified in this datasheet reflect post irradiation performance only. Rad report can be provided by request. Please contact sales to request a report.

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1 Pin configuration

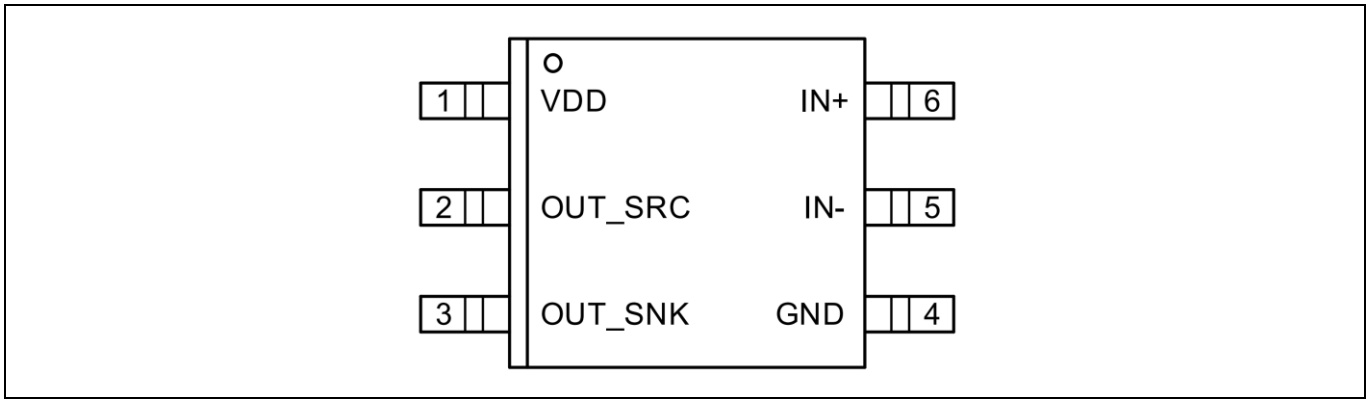
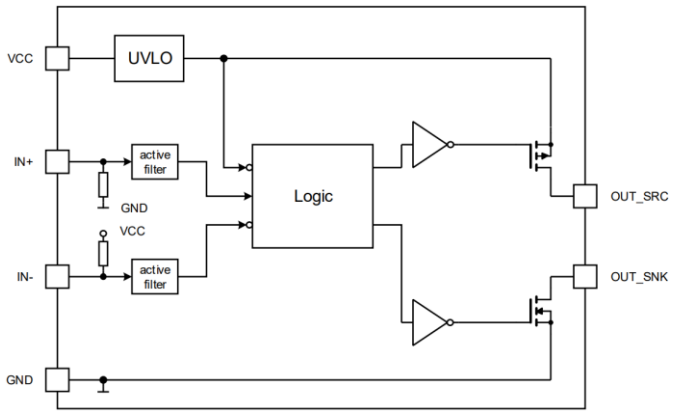


Table 2 Pin Configuration

Pin No.	Symbol	Description
1	VDD	Positive supply voltage. Operating range 8.6 V to 20 V
2	OUT_SRC	Driver output source. Low-impedance output with source capability
3	OUT_SNK	Driver output sink Low-impedance output with sink capability
4	GND	Ground
5	IN-	Inverting input Logic Input; if IN- is high or left open, causes OUT low
6	IN+	Non-inverting input Logic Input; if IN+ is low or left open causes OUT low

2 Block diagram and functional description



The BDP1CG15NB-01 is a fast single-channel radiation tolerant driver for low-side switches. Rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure highest flexibility and cover a high variety of applications. The gate driver IC aims particularly at fast-switching applications, therefore signal delays and rise/fall times have been minimized to support low switching losses in the MOSFET.

The maximum **supply voltage** is 20 V. This high voltage can be valuable in order to exploit the full current capability of the driver when handling very large MOSFETs. The minimum operating supply voltage is set by the undervoltage lockout function to a typical default value of 8 V. This undervoltage lockout function protects power MOSFETs from running into linear mode with subsequent high-power dissipation.

The non-inverting **input** is internally pulled down to a logic low voltage. The inverting input is internally pulled up to a logic high voltage. This prevents a switch-on event during power-up and a not-driven input condition. All inputs are compatible with LV-TTL levels and provide a hysteresis of typically 1.1 V. This hysteresis is independent of the supply voltage.

The rail-to-rail **output** stage realized with complementary MOS transistors is able to provide typical 4 A sourcing and 8 A sinking current. This asymmetrical push-pull stage enables a perfect “brake before make” (turn-off is faster than turn-on) condition, which is needed in half-bridge power MOSFET stages. This driver output stage has a shoot-through protection and current limiting behavior. The output impedance is very low with a typical value below 0.85 Ω for the sourcing p-channel MOS and 0.35 Ω for the sinking n-channel MOS transistor. The use of a p-channel sourcing transistor is crucial for achieving true rail-to-rail behavior and avoiding a source follower’s voltage drop. The gate drive output is actively held low in case of floating inputs, during startup, or power down triggered by the UVLO protection. In any situation (startup, UVLO, or shutdown) the output is held under defined conditions.

Table 3 Truth table

IN+	IN-	OUT_SRC	OUT_SNK
L	L	Open	L
L	H	Open	L
H	L	H	Open
H	H	Open	L

The **undervoltage lockout** function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. The switch transistor is not switched on if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation. The UVLO level is set to a typical value of 8 V (with hysteresis) for normal level and superjunction MOSFETS.

3 Maximum ratings

Table 4 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive supply voltage	V_{DD}	-0.3	-	22	V	
Voltage at pins IN+, IN-	V_{IN}	-10	-	22	V	
Voltage at pins OUT, OUT_SRC, OUT_SNK	V_{OUT}	-0.3 -2	- -	V_{DD}+0.3 V_{DD}+2	V	Note [1] Repetitive pulse < 200 ns [2]
Reverse current peak at pins OUT, OUT_SRC/OUT_SNK	I_{SNK_rev} I_{SRC_rev}	- -	- -	-5 5	Apk	< 500 ns
ESD capability CDM	V_{ESD_CDM}	-	-	1.5	kV	ANSI/ESDA/JEDEC JS-002
ESD capability HBM	V_{ESD_HBM}	-	-	2.5	kV	ANSI/ ESDA/JEDEC JS-001
Operating temperature	T_{op}	-40	-	150	°C	Note [3]
Junction temperature	T_j	-40	-	150	°C	
Storage temperature	T_{stg}	-55	-	150	°C	

[1] Voltage spikes resulting from reverse current peaks are allowed.

[2] Values are verified by characterization on bench.

[3] Continuous operation above 125 °C may reduce life time.

4 Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case (top)	$R_{th,JC}$	-	81	-	K/W	The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
Thermal resistance, junction - ambient	$R_{th,JA}$	-	170	-	K/W	The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
Thermal resistance, junction - board	$R_{th,JB}$	-	52	-	K/W	The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
Soldering temperature	T_{sol}	-	-	260	°C	

5 Electrical characteristics

Unless otherwise noted, min./max. values of characteristics are the lower and upper limits respectively. They are valid within the full operating range. The supply voltage is V_{DD} = 12 V. Typical values are given at T_J = 25 °C.

Table 6 Operating and characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	8.6	-	20	V	
Logic input voltage	V_{IN}	-5	-	20	V	
Power Supply						
VDD quiescent current	I_{VDDqu1}	-	0.4	-	mA	OUT = high, V_{DD} = 12 V
VDD quiescent current	I_{VDDqu2}	-	0.37	-	mA	OUT = low, V_{DD} = 12 V
Undervoltage lockout						
Undervoltage lockout (UVLO) turn on threshold	$UVLO_{on}$	7.4	8	8.6	V	
Undervoltage lockout (UVLO) turn off threshold	$UVLO_{off}$	6.5	7	7.5	V	
UVLO threshold hysteresis	$UVLO_{hys}$	-	1	-	V	
Logic Inputs						
Input voltage threshold for transition LH	V_{INH}	1.9	2.1	2.3	V	
Input voltage threshold for transition HL	V_{INL}	0.8	1.0	1.2	V	
Input pull up resistor[1]	R_{INH}	-	400	-	kΩ	
Input pull down resistor[2]	R_{INL}	-	100	-	kΩ	
Static output characteristics						
High level (sourcing) output resistance	R_{on_SRC}	0.42	0.85	1.46	Ω	I_{SRC} = 50 mA
High level (sourcing) output current	I_{SRC_peak}	-	4.0	-[3]	A	
Low level (sinking) output resistance	R_{on_SNK}	0.18	0.35	0.64	Ω	I_{SNK} = 50 mA
Low level (sinking) output current	I_{SNK_peak}	-	-8.0	-[4]	A	

[1] Inputs with initial high logic level

[2] Inputs with initial low logic level

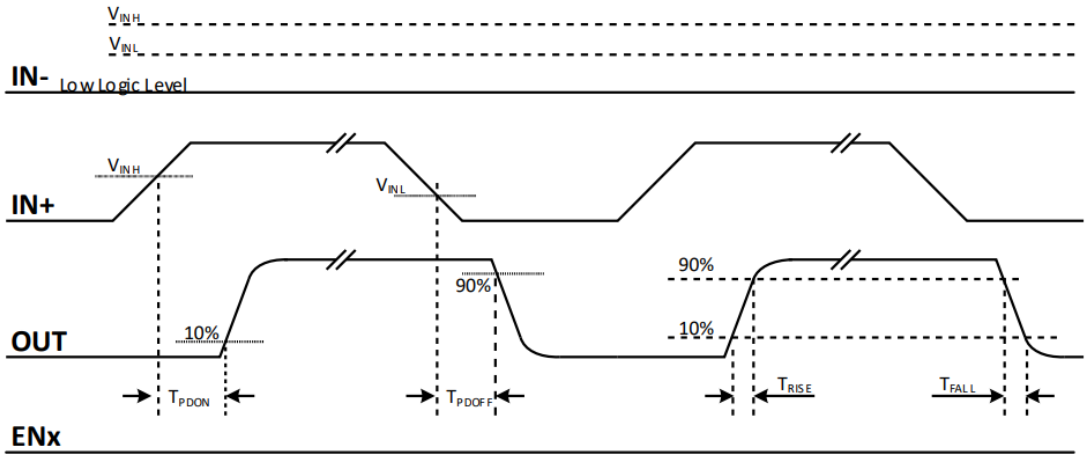
[3] Active limited by design at approx. 5.2 Apk, parameter is not subject to production test - verified by design / characterization, max. power dissipation must be observed

[4] Active limited by design at approx. -10.4 Apk, parameter is not subject to production test - verified by design / characterization, max. power dissipation must be observed

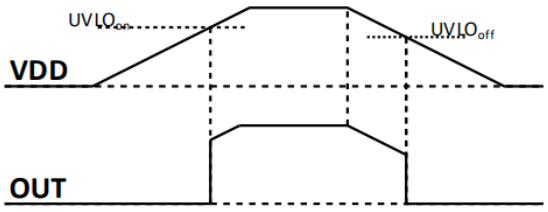
Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input to output propagation delay	$t_{pd(ON)}$	15	19	25	ns	C_{load} = 1.8 nF, V_{DD} = 12 V
Rise time	t_r	-	6.5	11	ns	C_{load} = 1.8 nF, V_{DD} = 12 V
Input to output propagation delay	$t_{pd(OFF)}$	15	19	25	ns	C_{load} = 1.8 nF, V_{DD} = 12 V
Fall time	t_f	-	4.5	9	ns	C_{load} = 1.8 nF, V_{DD} = 12 V
Minimum input pulse width that changes output state	T_{pw}	-	6	10	ns	C_{load} = 1.8 nF, V_{DD} = 12 V

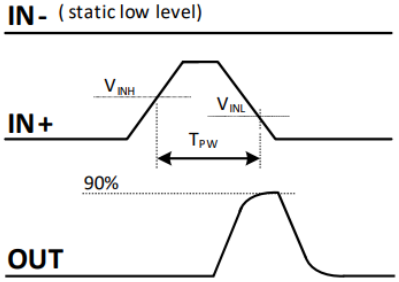
Definition of rise, fall and delay times for the inputs. This is valid for non-inverted and inverted control.



Undervoltage lockout function. Input INx drives OUT normally high



Minimum input pulse width that changes output state.



6 Electrical characteristics diagrams

Diagram 1: UVLO on/off characteristics

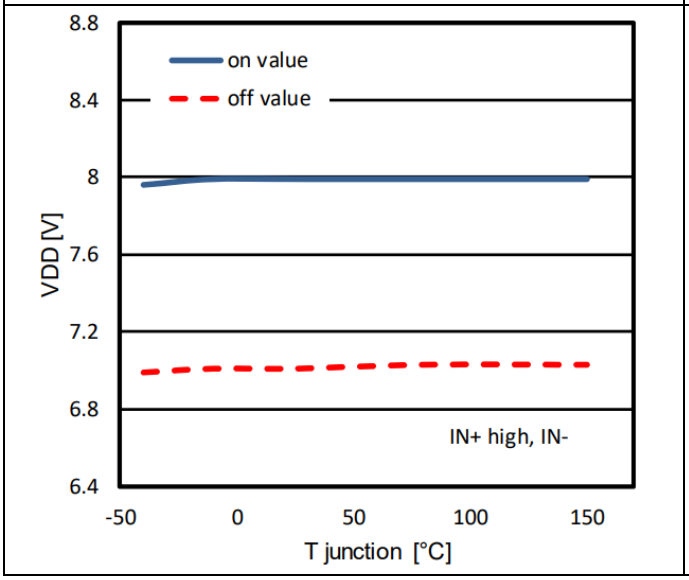


Diagram 2: UVLO Hysteresis

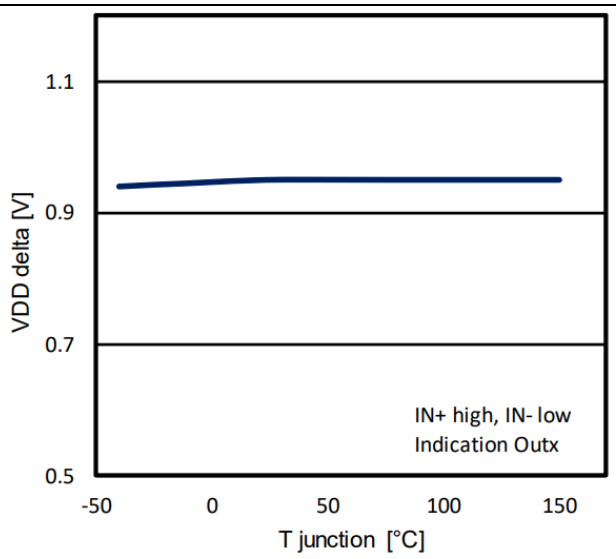


Diagram 3: Input (INx) characteristics

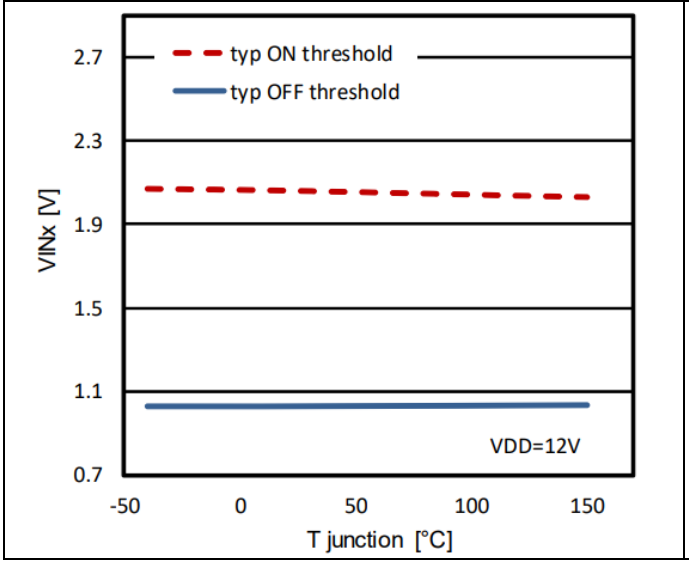


Diagram 4: Input hysteresis

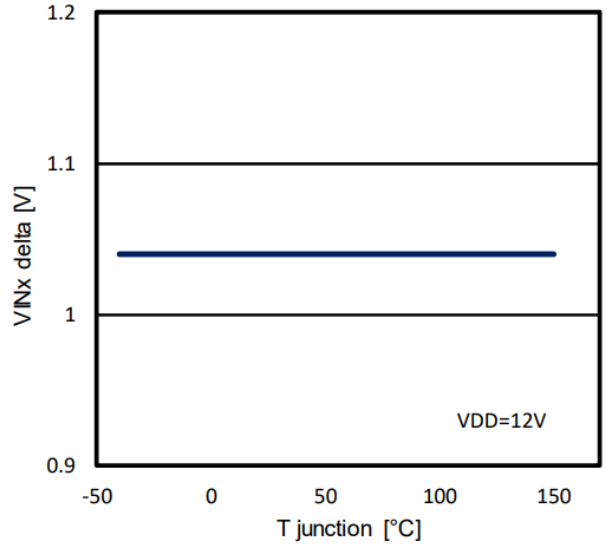


Diagram 5: Propagation delay (INx) on input 5V

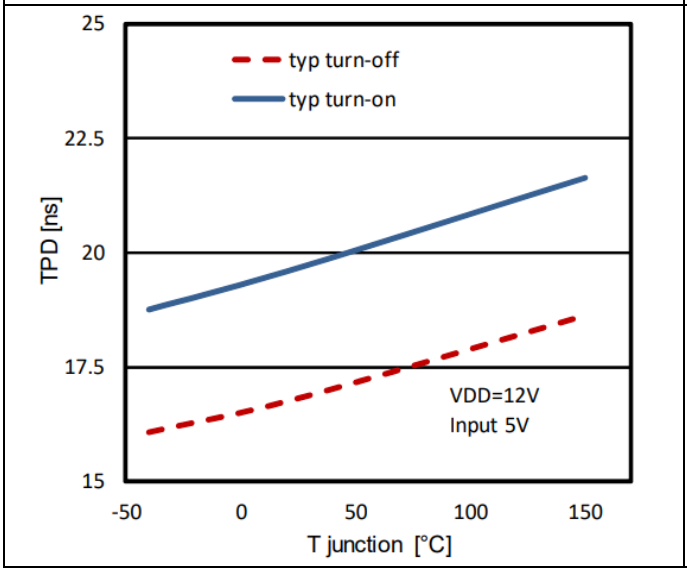


Diagram 6: Propagation delay (INx) on input 3.3V

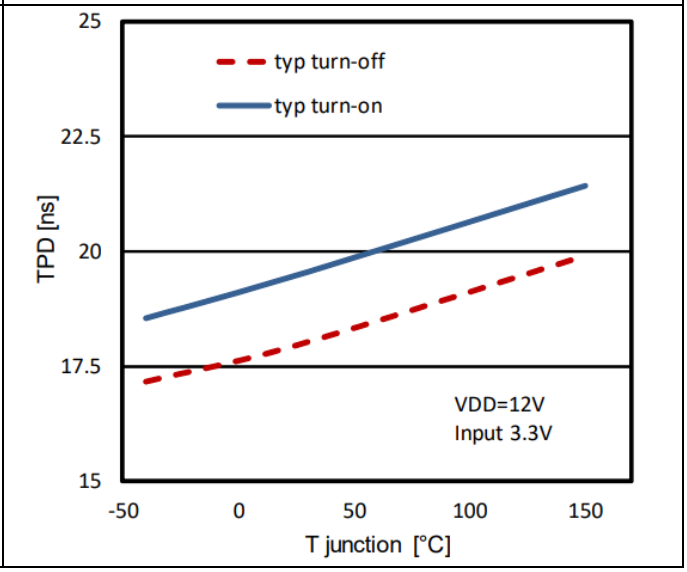


Diagram 7: Rise/fall times 10-90% with load on output

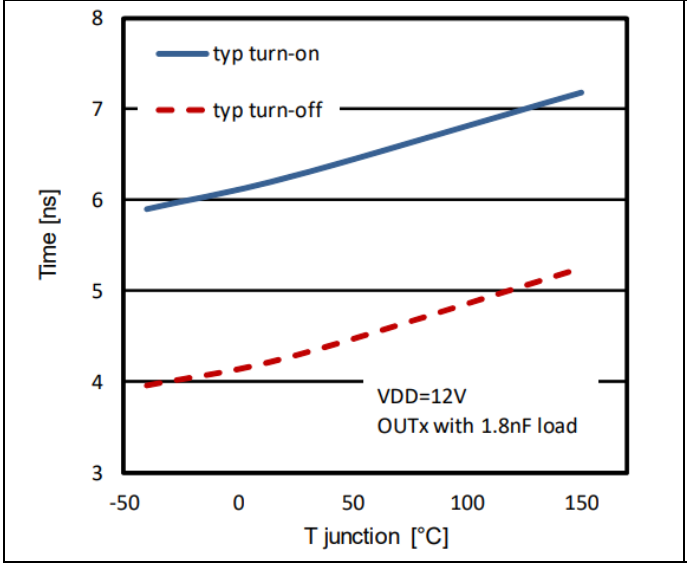
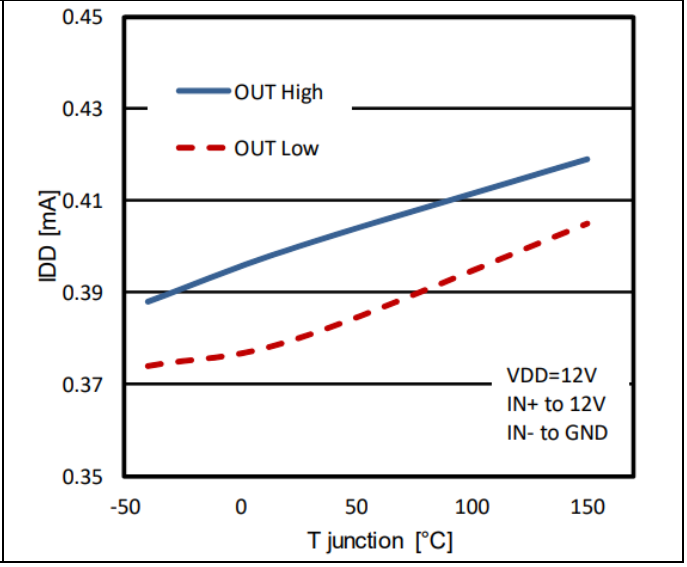


Diagram 8: Current consumption vs temperature



Electrical characteristics diagrams

Diagram 9: Current consumption vs operating supply VDD

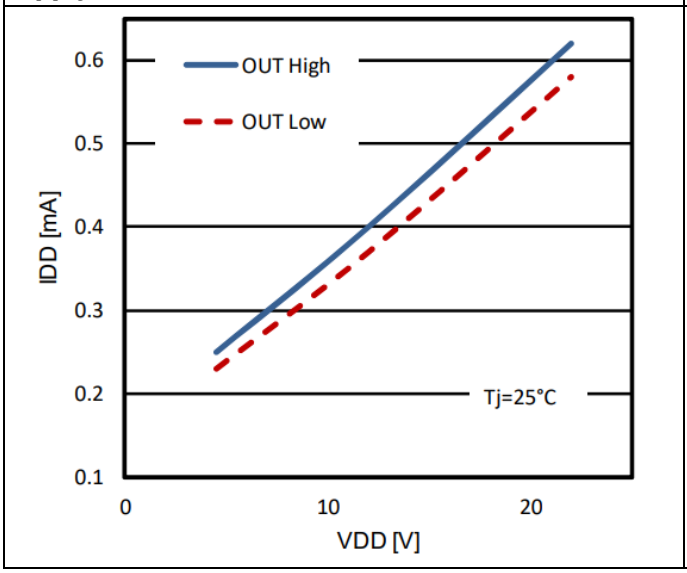


Diagram 10: Current consumption vs frequency

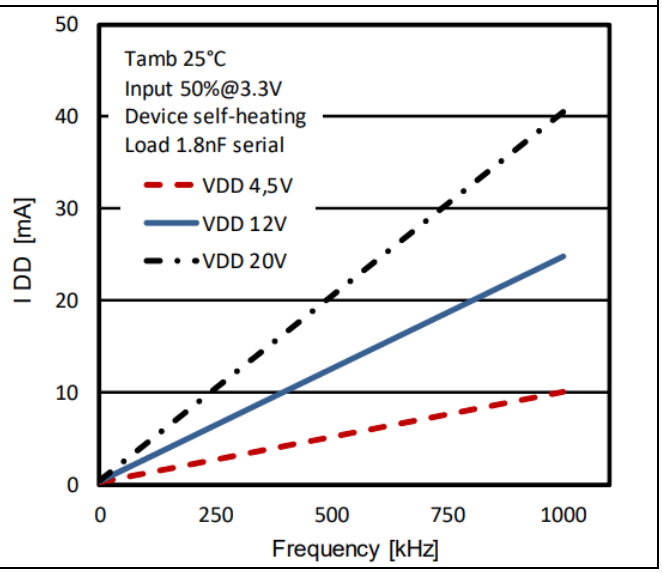


Diagram 11: Reverse current at OUTx with OUT LOW vs reverse voltage and resulting power

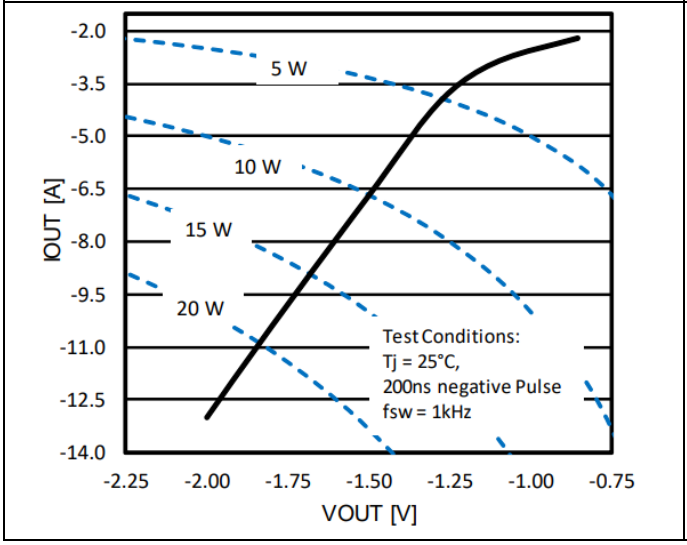
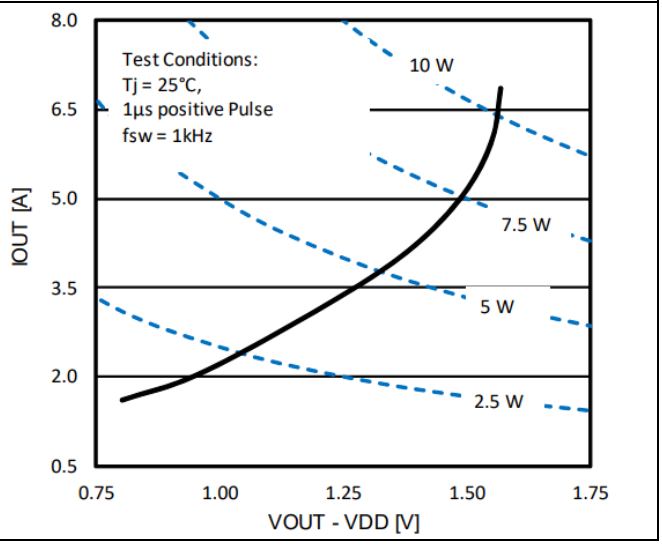
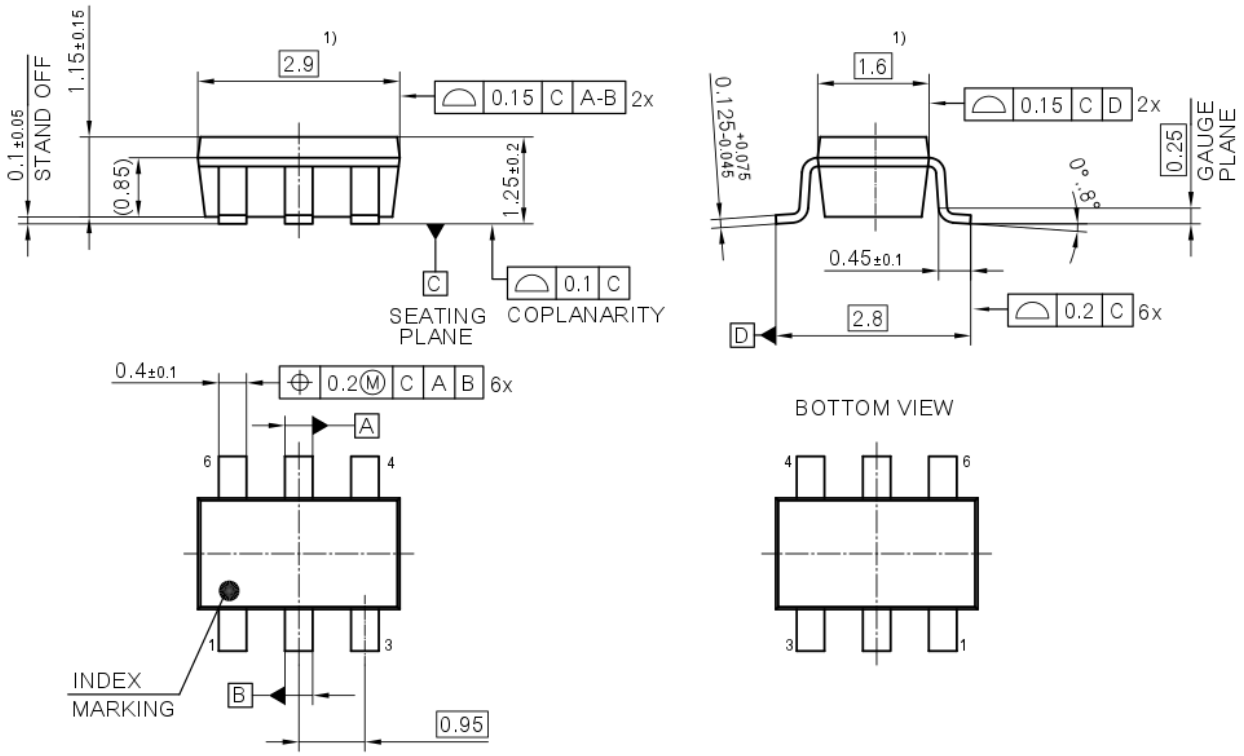


Diagram 12: Reverse current at output with OUT HIGH vs reverse voltage and resulting power



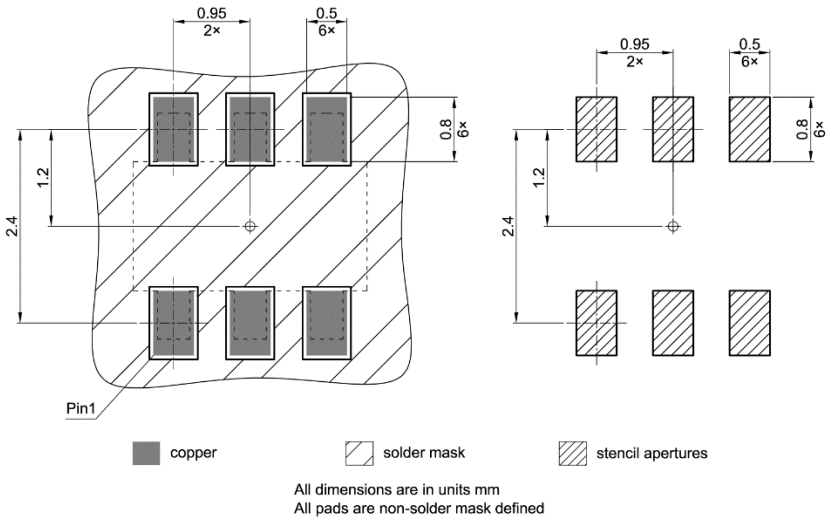
7 Package outlines and footprint



1) DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.15 MAX. PER SIDE

ALL DIMENSIONS ARE IN UNITS MM

THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [ ]



All dimensions are in units mm
All pads are non-solder mask defined

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