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As part of the acquisition of the non-optical analog/mixed-signal sensor portfolio from ams-OSRAM by Infineon, Infineon is in the process of rebranding all relevant documents. Due to the large volume of documents, this process will be completed in phases. In the interim, we are providing access to legacy ams-OSRAM documents under the terms of a trademark license agreement.

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**Contact:**

Infineon Technologies AG  
Am Campeon 1-15  
85579 Neubiberg  
Germany

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Email: [erratum@infineon.com](mailto:erratum@infineon.com)

# Product Document

# AS5132

## 360 Step (8.5 bit) Programmable High Speed Magnetic Position Sensor

### General Description

The AS5132 is a contactless magnetic position sensor for accurate angular measurement over a full turn of 360 degrees. It is a system-on-chip, combining integrated Hall elements, analog frontend and digital signal processing in a single device.

To measure the angle, only a simple two-pole magnet, rotating over the center of the chip is required.

The absolute angle measurement provides instant indication of the magnet's angular position with a resolution of 8.5 bit = 360 positions per revolution. This digital data is available as serial output over the interface and as a pulse width modulated (PWM) signal.

An additional U,V,W output can be used for a block commutation for a brushless DC motor. An incremental signal is available as an option.

In addition to the angle information, the strength of the magnetic field is also available as a 5-bit code.

A one time programmable (OTP) memory is used for permanent zero angle position programming. The magnet does not need to be aligned mechanically.

[Ordering Information](#) and [Content Guide](#) appear at end of datasheet.

### Key Benefits & Features

The benefits and features of AS5132, 360 Step (8.5 bit) Programmable High Speed Magnetic Position Sensor are listed below:

**Figure 1:**  
**Added Value of Using AS5132**

| Benefits                                                                                           | Features                                                                                                                                                       |
|----------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>Complete system-on-chip, no calibration required</li> </ul> | <ul style="list-style-type: none"> <li>360° contactless angular position sensing</li> </ul>                                                                    |
| <ul style="list-style-type: none"> <li>Multiple data output formats</li> </ul>                     | <ul style="list-style-type: none"> <li>Serial synchronous interface</li> <li>Pulse width modulated output (PWM)</li> <li>Incremental output formats</li> </ul> |

| Benefits                                                                                                                                                                             | Features                                                                                                                                                                                                               |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <ul style="list-style-type: none"> <li>• Ideal for applications in harsh environments due to magnetic sensing principle</li> </ul>                                                   | <ul style="list-style-type: none"> <li>• High reliability due to non-contact sensing</li> </ul>                                                                                                                        |
| <ul style="list-style-type: none"> <li>• Robust system, tolerant to horizontal misalignment, airgap variations, temperature variations and external magnetic stray fields</li> </ul> | <ul style="list-style-type: none"> <li>• Wide magnetic field input range: 20 – 80 mT (typical)</li> <li>• Wide temperature range: -40°C to 150°C</li> <li>• Fully automotive qualified to AEC-Q100, grade 0</li> </ul> |

## Applications

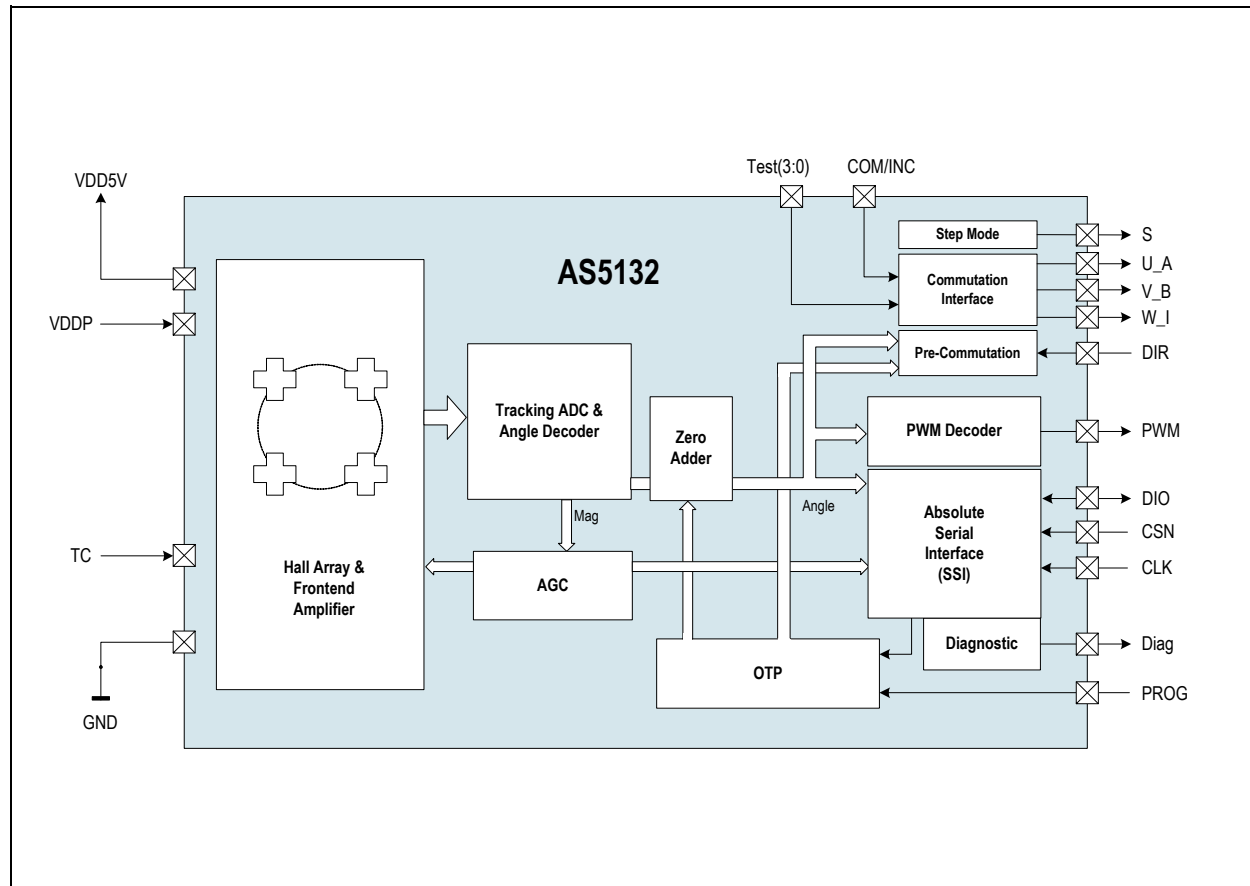
The AS5132 is suitable for:

- Contactless rotary position sensing
- Rotary switches (human machine interface)
- AC/DC motor position control
- Brushless DC motor position control

## Block Diagram

The functional blocks of this device are shown below:

**Figure 2:**  
**AS5132 Block Diagram**

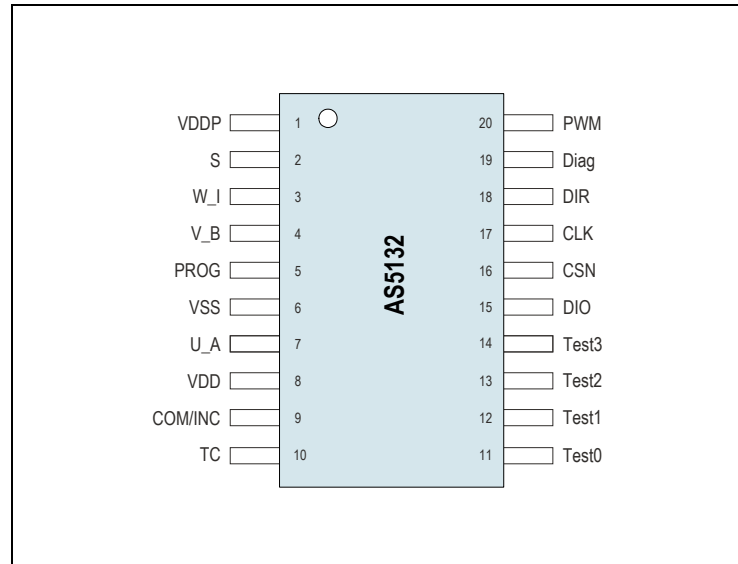


## Pin Assignment

The AS5132 pin assignments are described below.

**Figure 3:**  
**Pin Diagram**

**Pin Assignments (Top View):**  
Package drawing is not to scale.



**Figure 4:**  
**Pin Description**

| Pin Number | Pin Name  | Pin Type                        | Description                                                                                                           |
|------------|-----------|---------------------------------|-----------------------------------------------------------------------------------------------------------------------|
| 1          | VDDP      | Supply                          | Supply voltage for the selected pins <sup>(1)</sup>                                                                   |
| 2          | S         | Digital output                  | Step output (8mA, VDDP)                                                                                               |
| 3          | W_I       |                                 | Commutation output or incremental output                                                                              |
| 4          | V_B       |                                 |                                                                                                                       |
| 5          | PROG      | Analog Input / Output           | Programming voltage input. Do not connect this pin to VSS. Connectivity for programming see <a href="#">Figure 24</a> |
| 6          | VSS       | Supply                          | Supply ground                                                                                                         |
| 7          | U_A       | Digital output                  | Commutation output or incremental output                                                                              |
| 8          | VDD       | Supply                          | Positive supply voltage                                                                                               |
| 9          | COM / INC | Digital input / Schmitt-Trigger | Selection of the output mode. This pin is also used for external clock mode (VDDP)                                    |
| 10         | TC        | Analog input                    | Test pin. Connect to VSS in application                                                                               |

| Pin Number | Pin Name | Pin Type                        | Description                                                                                        |
|------------|----------|---------------------------------|----------------------------------------------------------------------------------------------------|
| 11         | Test0    | Analog input /output            | Test pin, selection of output format for incremental or step mode                                  |
| 12         | Test1    |                                 |                                                                                                    |
| 13         | Test2    |                                 |                                                                                                    |
| 14         | Test3    |                                 |                                                                                                    |
| 15         | DIO      | Bi-directional digital          | Data I/O for serial interface (VDDP)                                                               |
| 16         | CSN      | Digital input / Schmitt-Trigger | Chip select input (active low) (VDDP) (connected to a pull-up resistor if not used in application) |
| 17         | CLK      |                                 | Clock input for serial interface (VDDP)                                                            |
| 18         | DIR      |                                 | Input signal for the pre-commutation at start-up (VDDP)                                            |
| 19         | Diag     | Digital output / Open Drain     | Diagnostic output (open drain)                                                                     |
| 20         | PWM      | Digital output                  | PWM output (8mA, VDDP)                                                                             |

**Note(s):**

1. VDDP can be customized to the voltage levels of the peripheral circuitry to economize voltage level drivers.
2. Typ. CSN Pull\_up resistor of 10kOhm necessary. Floating state of a digital input is not allowed.

## Absolute Maximum Ratings

Stresses beyond those listed in [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5:**  
**Absolute Maximum Ratings**

| Symbol                                    | Parameter                          | Min                  | Max             | Units | Comments                                                                                                                                                                                                                                                                                 |
|-------------------------------------------|------------------------------------|----------------------|-----------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Electrical Parameters                     |                                    |                      |                 |       |                                                                                                                                                                                                                                                                                          |
| V <sub>DD</sub>                           | Supply voltage                     | -0.3                 | 7               | V     | Except during OTP programming                                                                                                                                                                                                                                                            |
| V <sub>DDP</sub>                          | DC supply voltage                  | 0.3                  | 7               | V     | Cannot be higher than V <sub>DD</sub> +0.3                                                                                                                                                                                                                                               |
| V <sub>IN</sub>                           | Input pin voltage                  | V <sub>SS</sub> -0.5 | V <sub>DD</sub> | V     |                                                                                                                                                                                                                                                                                          |
| I <sub>scr</sub>                          | Input current (latch up immunity)  | -100                 | 100             | mA    | Norm: EIA/JESD78 Class II Level A                                                                                                                                                                                                                                                        |
| Electrostatic Discharge                   |                                    |                      |                 |       |                                                                                                                                                                                                                                                                                          |
| ESD <sub>HBM</sub>                        | Electrostatic discharge            | ±2                   |                 | kV    | Norm: JESD22-A114E                                                                                                                                                                                                                                                                       |
| Temperature Ranges and Storage Conditions |                                    |                      |                 |       |                                                                                                                                                                                                                                                                                          |
| T <sub>strg</sub>                         | Storage temperature                | -55                  | 150             | °C    |                                                                                                                                                                                                                                                                                          |
| T <sub>body</sub>                         | Body temperature                   |                      | 260             | °C    | The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/JEDEC J-STD-020</i> “Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices”. The lead finish for Pb-free leaded packages is matte tin (100% Sn). |
| RH <sub>NC</sub>                          | Relative humidity (non-condensing) | 5                    | 85              | %     |                                                                                                                                                                                                                                                                                          |
| MSL                                       | Moisture sensitivity level         | 3                    |                 |       | Represents a maximum floor time of 168h                                                                                                                                                                                                                                                  |

## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) method.

$T_{AMB} = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ ,  $V_{DD} = 4.5\text{V}$  to  $5.5\text{V}$ , all voltages referenced to  $V_{SS}$ , unless otherwise noted.

## Operating Conditions

**Figure 6:**  
Operating Conditions

| Symbol    | Parameter                         | Conditions                                                                   | Min | Typ | Max | Units |
|-----------|-----------------------------------|------------------------------------------------------------------------------|-----|-----|-----|-------|
| $V_{DD}$  | Positive supply voltage           |                                                                              | 4.4 |     | 5.5 | V     |
| $V_{DDP}$ | Positive supply voltage periphery |                                                                              | 3.0 |     | 5.5 | V     |
| $I_{DD}$  | Operating current                 | No load on outputs. Supply current can be reduced by using stronger magnets. |     | 15  | 22  | mA    |

## System Parameters

**Figure 7:**  
System Parameters

| Symbol      | Parameter         | Conditions                                         | Min | Typ | Max         | Units                     |
|-------------|-------------------|----------------------------------------------------|-----|-----|-------------|---------------------------|
| N           | Resolution        |                                                    |     | 8.5 |             | Bit                       |
|             |                   |                                                    |     | 1   |             | Deg                       |
| $T_{PwrUp}$ | Power up time     |                                                    |     |     | $\leq 4100$ | $\mu\text{s}$             |
| $t_s$       | Tracking rate     | Step rate of tracking ADC;<br>1 step = $1^{\circ}$ |     |     | 5.2         | $\mu\text{s}/\text{step}$ |
| $INL_{cm}$  | Accuracy          | Centered magnet                                    | -2  |     | 2           | Deg                       |
|             |                   | Within horizontal displacement radius              | -3  |     | 3           |                           |
| $t_{delay}$ | Propagation delay | Internal signal processing time                    |     |     | 22          | $\mu\text{s}$             |
| TN          | Transition noise  | peak-peak                                          |     |     | 1.41        | Deg                       |

## Magnet Specifications

**Figure 8:**  
**Magnet Specifications**

| Symbol | Parameter             | Conditions                              | Min | Max    | Units |
|--------|-----------------------|-----------------------------------------|-----|--------|-------|
| $B_Z$  | Magnetic input range  | At die surface                          | 20  | 80     | mT    |
| $V_i$  | Magnet rotation speed | To maintain locked state <sup>(1)</sup> |     | 72,900 | rpm   |

**Note(s):**

- Maximum rotation speed is dependent on the internal time reference.  
Maximum value is calculated with lowest sequence over all operating conditions.

## Programming Parameters

**Figure 9:**  
**Programming Parameters**

| Symbol                | Parameter                       | Conditions                              | Min | Max | Units |
|-----------------------|---------------------------------|-----------------------------------------|-----|-----|-------|
| $V_{\text{PROG}}$     | Programming voltage             | Static voltage at pin PROG              | 8   | 8.5 | V     |
| $I_{\text{PROG}}$     | Programming current             | During programming                      |     | 100 | mA    |
| $T_{\text{ambPROG}}$  | Programming ambient temperature |                                         | 0   | 85  | °C    |
| $t_{\text{PROG}}$     | Programming time                |                                         | 2   | 4   | μs    |
| $V_{\text{R,prog}}$   | Analog readback voltage         | During analog readback mode at pin PROG |     | 0.5 | V     |
| $V_{\text{R,unprog}}$ |                                 |                                         | 2   | 3.5 |       |

## DC Characteristics of Digital Inputs

**Figure 10:**  
**CMOS Inputs COM/INC, CSN, CLK, DIO, DIR**

| Symbol            | Parameter                | Min                        | Max                        | Units | Note                 |
|-------------------|--------------------------|----------------------------|----------------------------|-------|----------------------|
| $V_{\text{IH}}$   | High level input voltage | $0.7 \cdot V_{\text{DDP}}$ | $V_{\text{DDP}}$           | V     | COM/INC refer to VDD |
| $V_{\text{IL}}$   | Low level input voltage  | 0                          | $0.3 \cdot V_{\text{DDP}}$ | V     |                      |
| $I_{\text{LEAK}}$ | Input leakage current    |                            | 1                          | μA    |                      |

## DC Characteristics of Digital Outputs

**Figure 11:**  
CMOS Outputs S, U\_A, V\_B, W\_I, PWM, DIO

| Symbol   | Parameter                 | Min      | Max     | Units | Note                                                                    |
|----------|---------------------------|----------|---------|-------|-------------------------------------------------------------------------|
| $V_{OH}$ | High level output voltage | VDDP-0.5 | VDDP    | V     | PWM and S have 8mA output load, DIO has 4mA output load.                |
|          |                           | VDD-0.5  | VDD     |       | U_A, V_B, W_I have 4mA output load.                                     |
| $V_{OL}$ | Low level output voltage  | 0        | VSS+0.4 | V     | PWM and S have 8mA output load, DIO, U_A, V_B, W_I has 4mA output load. |
| CL       | Capacitive load           |          | 35      | pF    |                                                                         |

## Timing Characteristics

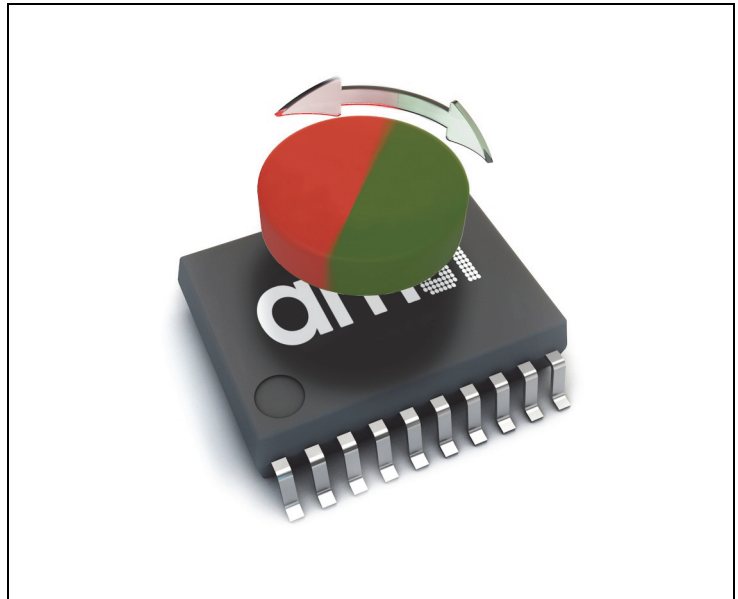
**Figure 12:**  
Timing Characteristics

| Symbol     | Parameter                                                                 | Min               | Typ | Max                    | Units |
|------------|---------------------------------------------------------------------------|-------------------|-----|------------------------|-------|
| $f_{CLK}$  | Clock frequency normal operation                                          |                   | 5   | 6                      | MHz   |
| $f_{CLKP}$ | Clock frequency during OTP programming                                    | 200               |     | 650                    | kHz   |
| $t_1$      | CSn to positive edge of CLK                                               | 150               |     |                        | ns    |
| $t_2$      | CSn to drive bus externally                                               | 0                 |     |                        | ns    |
| $t_3$      | Setup time command bit (data valid to positive edge of CLK)               | 50                |     |                        | ns    |
| $t_4$      | Hold time command bit (data valid after positive edge of CLK)             | 15                |     |                        | ns    |
| $t_5$      | Float time (positive edge of CLK for last command bit to bus float)       |                   |     | $0.5 * 1/f_{CLK}$      | ns    |
| $t_6$      | Bus driving time (positive edge of CLK for last command bit to bus drive) | $0.5 * 1/f_{CLK}$ |     |                        | ns    |
| $t_7$      | Data valid time (positive edge of CLK to bus valid)                       | $0.5 * 1/f_{CLK}$ |     | $0.5 * 1/f_{CLK} + 50$ | ns    |
| $t_8$      | Hold time data bit (data valid after positive edge of CLK)                | $0.5 * 1/f_{CLK}$ |     |                        | ns    |

| Symbol   | Parameter                                                                 | Min               | Typ | Max | Units   |
|----------|---------------------------------------------------------------------------|-------------------|-----|-----|---------|
| $t_9$    | Hold time CSn (positive edge of last CLK to negative edge of CSn)         | $0.5 * 1/f_{CLK}$ |     |     | ns      |
| $t_{10}$ | Bus floating time (positive edge of CSn to float bus)                     |                   |     | 50  | ns      |
| $t_{11}$ | Setup time data bit @ write access (data valid to positive edge of CLK)   | 50                |     |     | ns      |
| $t_{12}$ | Hold time data bit @ write access (data valid after positive edge of CLK) | 15                |     |     | ns      |
| $t_{13}$ | Bus floating time (positive edge of CSn to float bus)                     |                   |     | 50  | ns      |
| $t_{14}$ | CSn high time                                                             | 2                 |     |     | $\mu s$ |

## Detailed Description

**Figure 13:**  
**Typical Arrangement of AS5132 and Magnet**



## Synchronous Serial Interface (SSI)

The absolute angle data can be read out over the synchronous serial interface using the pins **CSN**, **DIO** and **CLK**. It is a bidirectional interface therefore a read or write access is possible. The organization of the protocol is byte wise and starts with the command byte followed by the data information.

**Figure 14:**  
Read / Write Serial Data Transmission

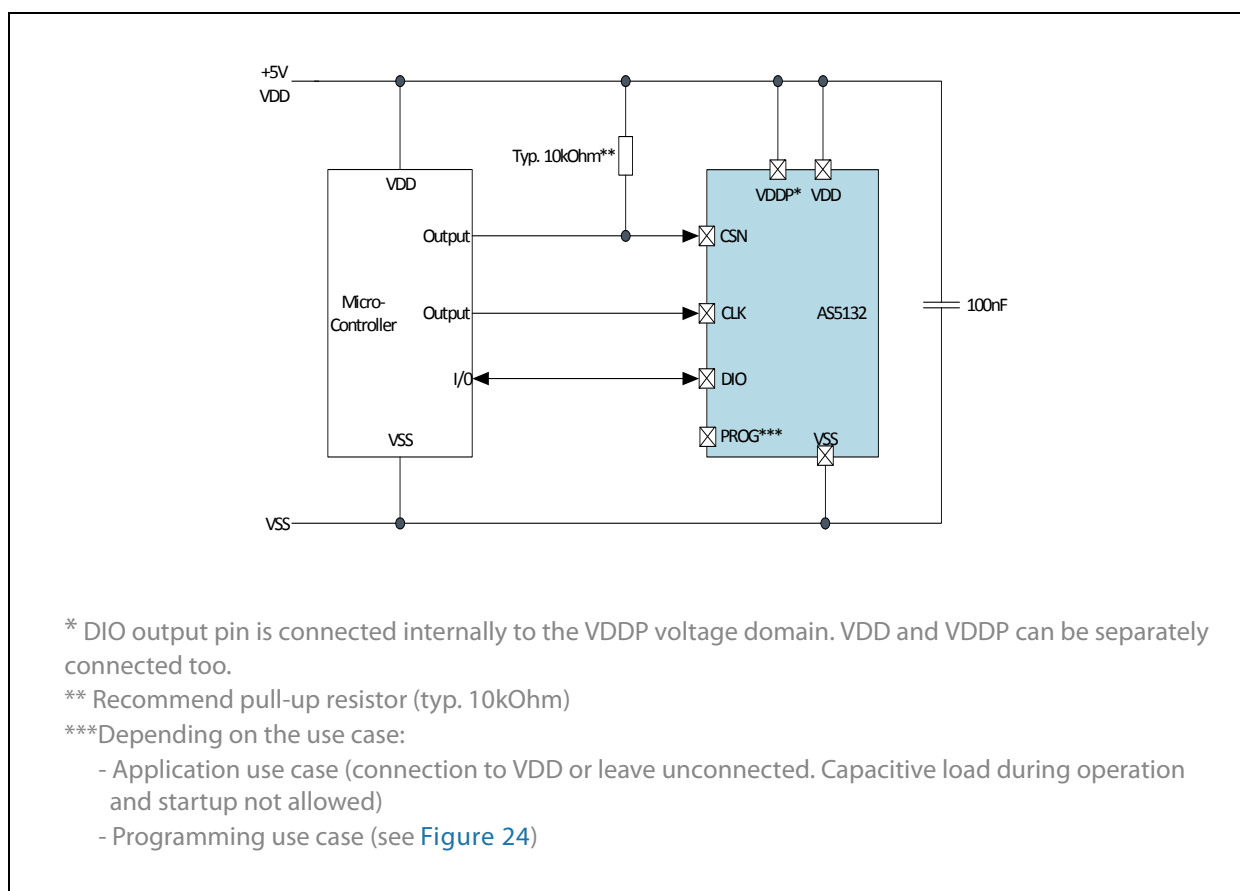


Figure 14 shows the connection of the AS5132 to a micro controller. Depending on the command byte are different access types possible. In normal mode the number of clocks is equal the number of data bits.

**Figure 15:**  
Data Organization of the SSI Protocol 16-Bit Data

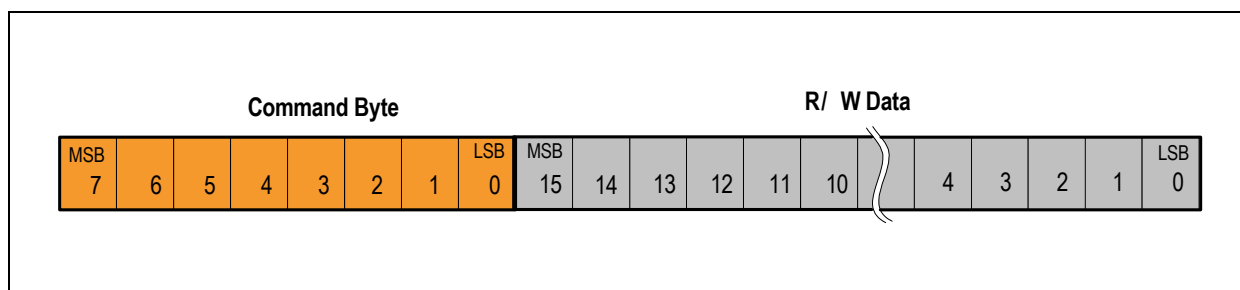
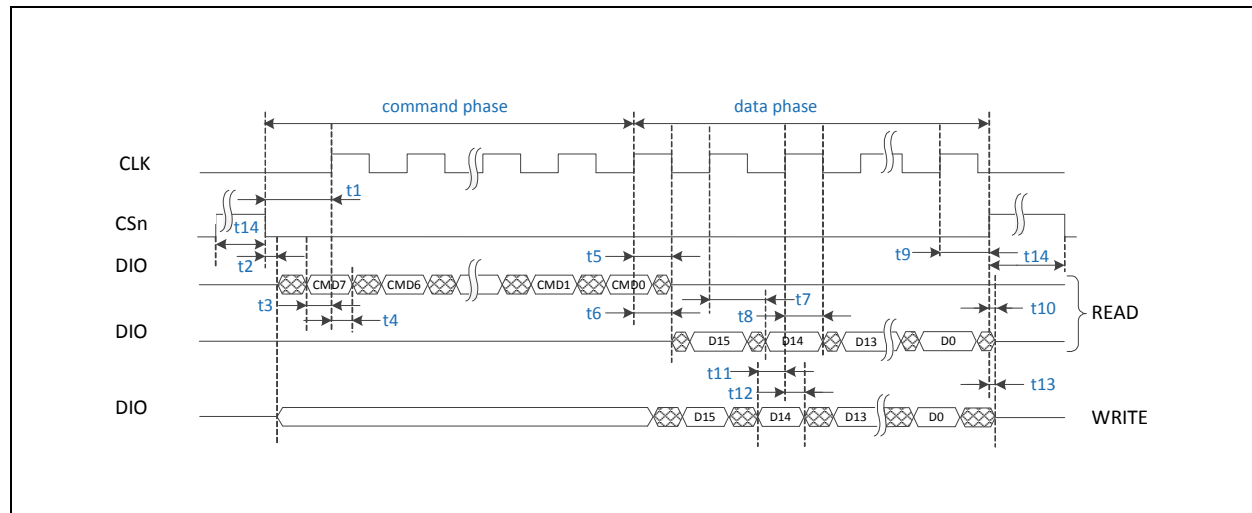


Figure 15 shows the organization of the data. The first section is used to setup the operating mode and the address. During write mode the micro controller drives the data line and generates in addition the CSn and CLK signal. Figure 16 shows SSI Read and write operations in normal mode.

**Figure 16:**  
**SSI Normal Read and Write Mode**



The first 8 command data bits are written by the microcontroller. After the command data the device takes over the **DIO** line and writes the data information. A high impedance phase must be considered before the device drives the output line.

### Commands of the SSI in Normal Mode

**Figure 17:**  
**Read/Write Interface Commands in Normal Mode**

| Command Name   | Command Data | Access Mode | MSB 15             | 14      | 13       | 12               | 11 | 10 | 9 | 8 | 7 | 6        | 5         | 4 | 3 | 2 | 1 | LSB 0 |   |
|----------------|--------------|-------------|--------------------|---------|----------|------------------|----|----|---|---|---|----------|-----------|---|---|---|---|-------|---|
| WRITE CONFIG   | 0001_0111    | write       |                    | GEN RST | Hyst Dis | PRE_COM_DYN<5:0> |    |    |   |   |   | MTC2     | MTC1      |   |   |   |   |       |   |
| SET MT COUNTER | 0001_0100    | write       | MT - COUNTER <8:0> |         |          |                  |    |    |   |   |   |          |           |   |   |   |   |       |   |
| EN PROG        | 1000_0100    | write       | 0                  | 1       | 1        | 0                | 0  | 1  | 0 | 1 | 0 | 1        | 1         | 1 | 0 | 0 | 0 | 0     |   |
| RD MT COUNTER  | 0000_0100    | read        | MT - COUNTER <8:0> |         |          |                  |    |    |   |   |   | EZ ERR   |           |   |   |   |   |       | P |
| RD_ANGLE       | 0000_0000    | read        | ANGLE <8:0>        |         |          |                  |    |    |   |   |   | LOCK ADC | AGC <5:1> |   |   |   |   | P     |   |

**Note(s):**

- Gray bits can be ignored by the user.

**GEN RST:** A HI generates a reset of the AS5132. GEN RST must be set to LO after reset.

**Hyst\_Dis:** Hysteresis disable.

**PRE\_COM\_DYN <5:0>:** Absolute dynamic pre-commutation value. Depending on the setup of the pole pairs, a mechanical angle offset can be adjusted. The range is 0 to 63 mechanical degrees (LSBs).

**MT-COUNTER <8:0>:** The multiturn counter can be set or read over the interface.

**EN PROG:** This command with the data content enables the access to the OTP register in extended mode. OTP Programming mode is only possible in extended mode with special connection Figure 24 on page 18.

**EZ ERR:** Indicates a wrong operation of the OTP memory after programming at room temperature. This bit is not intended for OTP diagnostic in the application over life time. This bit lose also validity over a time.

**ANGLE <8:0>:** Absolute angle information with angular true resolution (360 steps).

**LOCK ADC:** Indicates a locked ADC. An angle value is only valid in case of a locked ADC. During sleep mode is the LOCK ADC bit LO.

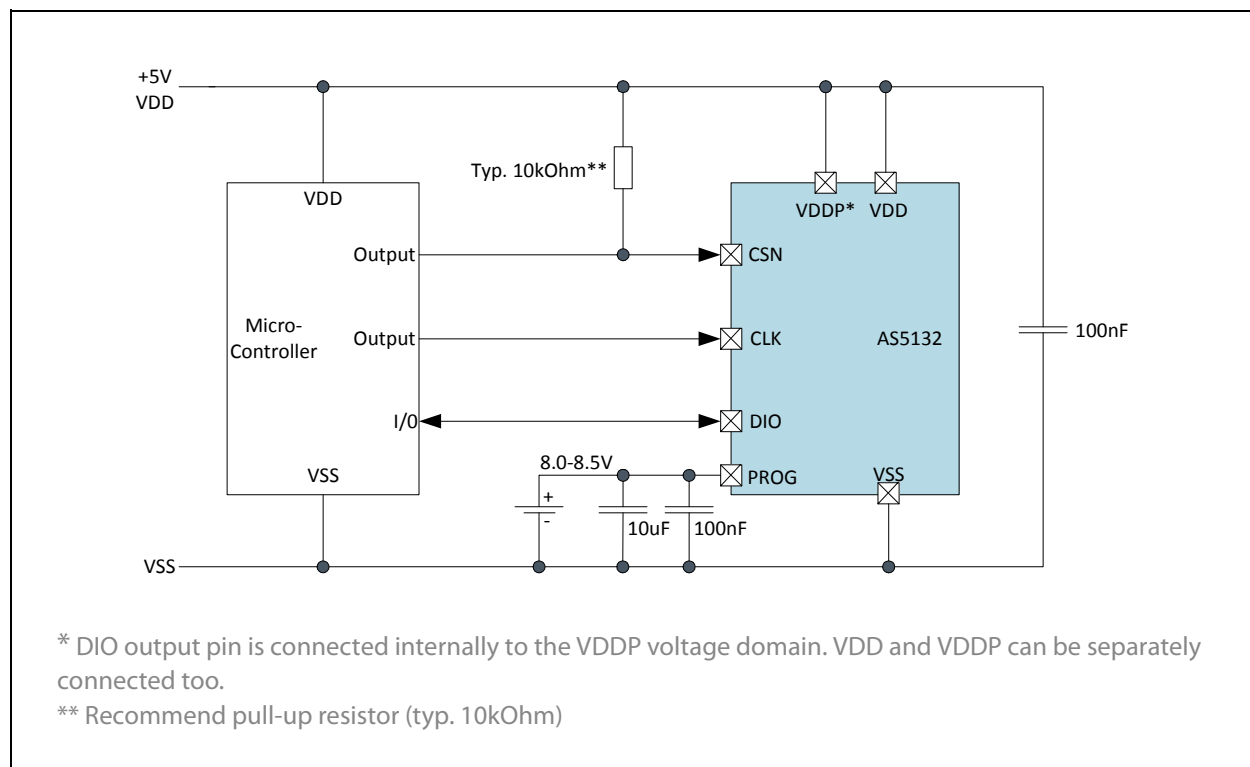
**AGC <5:1>:** Automatic gain control value indicates the magnetic field strength.

**P:** Parity information of the 15 data bits. Odd parity.

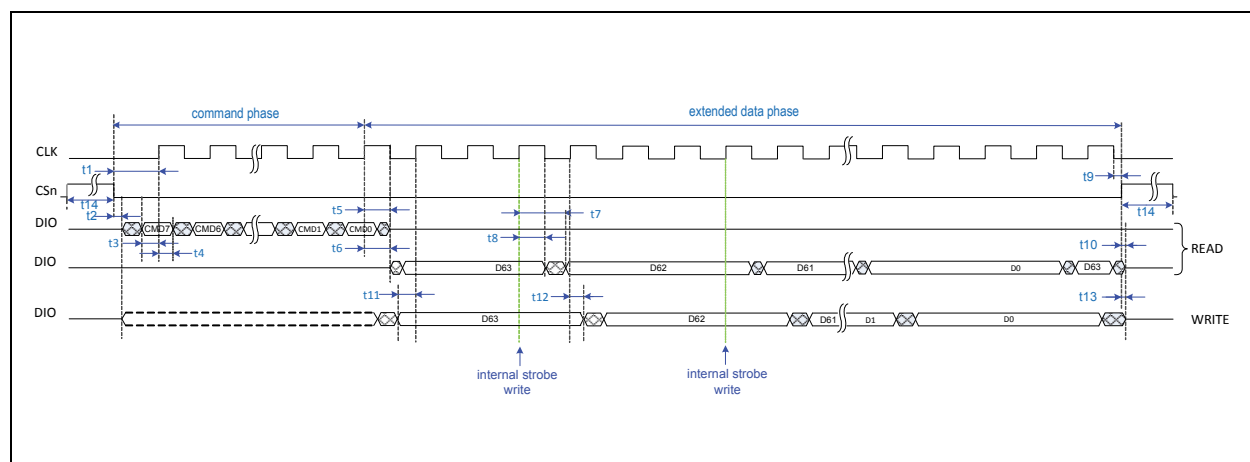
### Extended Synchronous Serial Interface Mode

The absolute angle data can be read out over the synchronous serial interface using the pins **CSN**, **DIO** and **CLK**. It is a bidirectional interface therefore a read or write access is possible. The organization of the protocol is byte wise and starts with the command byte followed by the data information.

**Figure 18:**  
Connectivity During Programming in Extended Mode



**Figure 19:**  
SSI Extended Read and Write Mode



In extended mode the digital interface requires four clocks per data bit. During this time the device is able to handle internal signals for special access.

**Figure 20:**  
**Read/Write Interface Commands in Extended Mode**

| Command Name | Command Data | Access Mode | MSB 63    | ... | 17 | 16                | 15 | 14          | 13                 | 12 | 11        | 10 | 9 | 8                | ... | LSB 0 |
|--------------|--------------|-------------|-----------|-----|----|-------------------|----|-------------|--------------------|----|-----------|----|---|------------------|-----|-------|
| WRITE OTP    | 0001_1111    | ext. write  | TST<46:0> |     |    | SENSITIVITY <1:0> |    | ext. CLK EN | PRE_COM_STAT <1:0> |    | UVW <2:0> |    |   | ZERO ANGLE <8:0> |     |       |
| PROG OTP     | 0001_1001    | ext. write  | TST<46:0> |     |    | SENSITIVITY <1:0> |    | ext. CLK EN | PRE_COM_STAT <1:0> |    | UVW <2:0> |    |   | ZERO ANGLE <8:0> |     |       |
| READ OTP     | 0000_1111    | ext. write  | TST<46:0> |     |    | SENSITIVITY <1:0> |    | ext. CLK EN | PRE_COM_STAT <1:0> |    | UVW <2:0> |    |   | ZERO ANGLE <8:0> |     |       |
| READ ANA     | 0000_1001    | ext. read   | TST<46:0> |     |    | SENSITIVITY <1:0> |    | ext. CLK EN | PRE_COM_STAT <1:0> |    | UVW <2:0> |    |   | ZERO ANGLE <8:0> |     |       |

**Note(s):**

1. TST is pre-programed by ams AG and used for test purpose.

**Programming Parameters**

**ZERO ANGLE <8:0>:** Zero position value. This value is permanent added to the internal absolute position. Use range 0 to 359.

**UVW <2:0>:** Setup of the number of pole pairs. In the step mode configuration, the bit UVW<2> is used to invert the step mode output signal.

**Figure 21:**  
**Possible Settings for UVW Outputs**

| UVW <2:0> |   |   | Number of Pole Pairs |
|-----------|---|---|----------------------|
| 0         | 0 | 0 | 1                    |
| 0         | 0 | 1 | 2                    |
| 0         | 1 | 0 | 3                    |
| 0         | 1 | 1 | 4                    |
| 1         | 0 | 0 | 5                    |
| 1         | 0 | 1 | 6                    |
| 1         | 1 | 0 | 6                    |
| 1         | 1 | 1 | 6                    |

**SENSITIVITY <1:0>:** Setup of the amplification within the internal signal path. The sensitivity adjustment can be used to center the AGC value at default conditions.

**Figure 22:**  
**Setup of the Sensitivity**

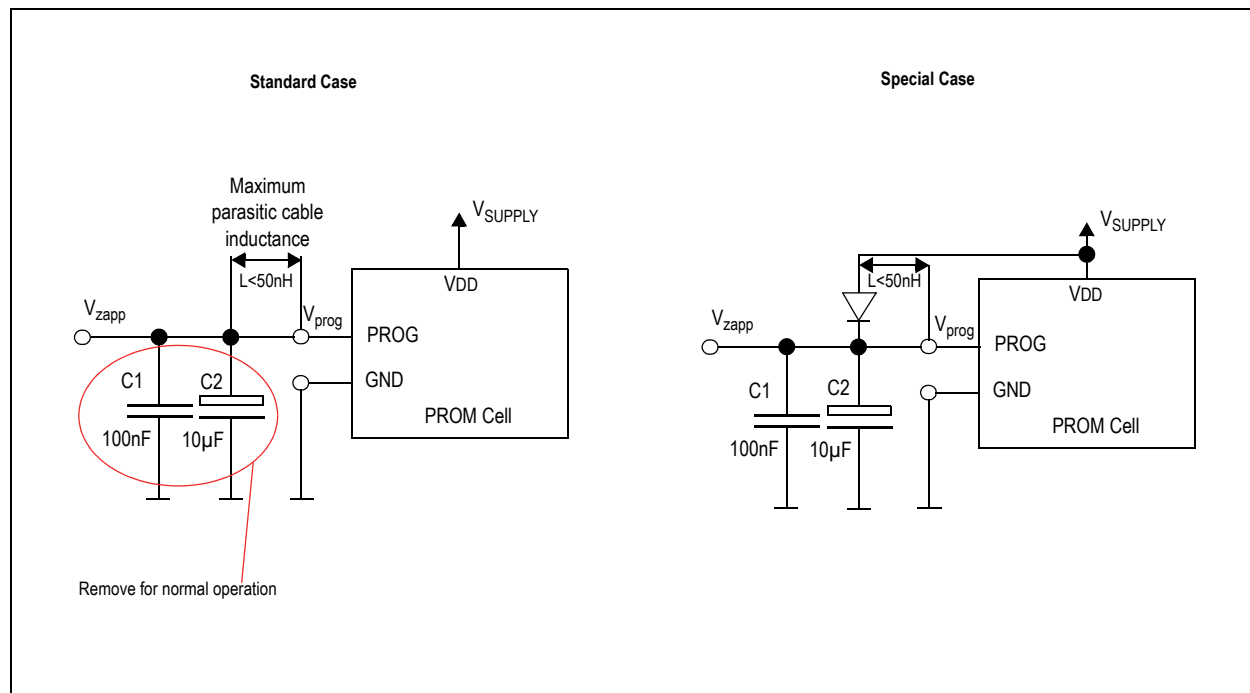
| SENSITIVITY <1:0> |   | Sensitivity Setting |      |      |
|-------------------|---|---------------------|------|------|
|                   |   | Min                 | Typ  | Max  |
| 0                 | 0 | 1.6                 | 1.65 | 1.75 |
| 0                 | 1 | 1.79                | 1.88 | 1.98 |
| 1                 | 0 | 2.01                | 2.11 | 2.22 |
| 1                 | 1 | 2.23                | 2.35 | 2.47 |

**Figure 23:**  
**Setup Parameters for the Static Pre-Commutation**

| PRE_COM_STAT <1:0> |   | Static Pre-commutation Value in Mechanical Degrees |
|--------------------|---|----------------------------------------------------|
| 0                  | 0 | 0                                                  |
| 0                  | 1 | 2                                                  |
| 1                  | 0 | 4                                                  |
| 1                  | 1 | 8                                                  |

**Ext. CLK EN:** Enables the external CLK mode for the PWM output. The external CLK mode is only possible in commutation mode. The state of the pin COM/INC is not considered in this case for mode selection.

**Figure 24:**  
**OTP Programming Connection**



The maximum capacitive load at PROG in normal operation should be less than 20pF. However, during programming the capacitors C1+C2 are needed to buffer the programming voltage during current spikes, but they must be removed for normal operation. To overcome this contradiction, the recommendation is to add a diode (4148 or similar) between PROG and V<sub>DD</sub> as shown in [Figure 24](#) (special case setup), if the capacitors can not be removed at final assembly.

Due to D1, the capacitors C1+C2 are loaded with V<sub>DD</sub>-0.7V at startup, hence not influencing the readout of the internal OTP registers. During programming the OTP, the diode ensures that no current is flowing from PROG (8V to 8.5V) to V<sub>DD</sub> (5V).

In the standard case (see [Figure 24](#)), the verification of a correct OTP readout must be done by analog readback. The special case setup provides the analog readback of the OTP as well.

As long as the PROG pin is accessible it is recommended to use standard setup. In case the PROG pin is not accessible at final assembly, the special setup is recommended.

### Programming Verification

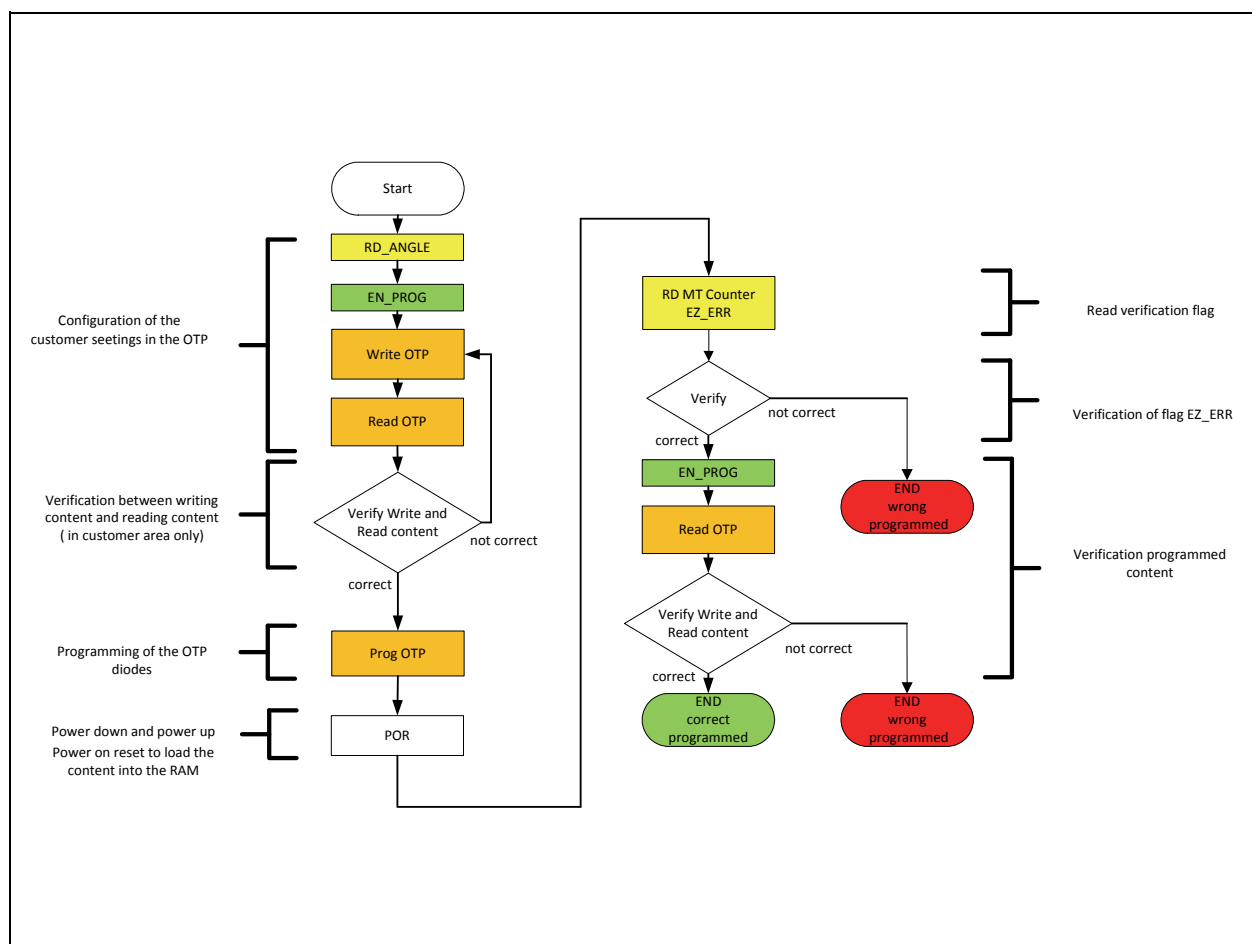
The verification of the OTP programming is mandatory using following methods:

**Digital Verification:** Checking the EZ\_ERR bit (0 = OK, 1 = error)

- Restricted to temperature range:  $25\text{ }^{\circ}\text{C} \pm 20\text{ }^{\circ}\text{C}$
- Right after the programming (max. 1 hour with same conditions  $25\text{ }^{\circ}\text{C} \pm 20\text{ }^{\circ}\text{C}$ )

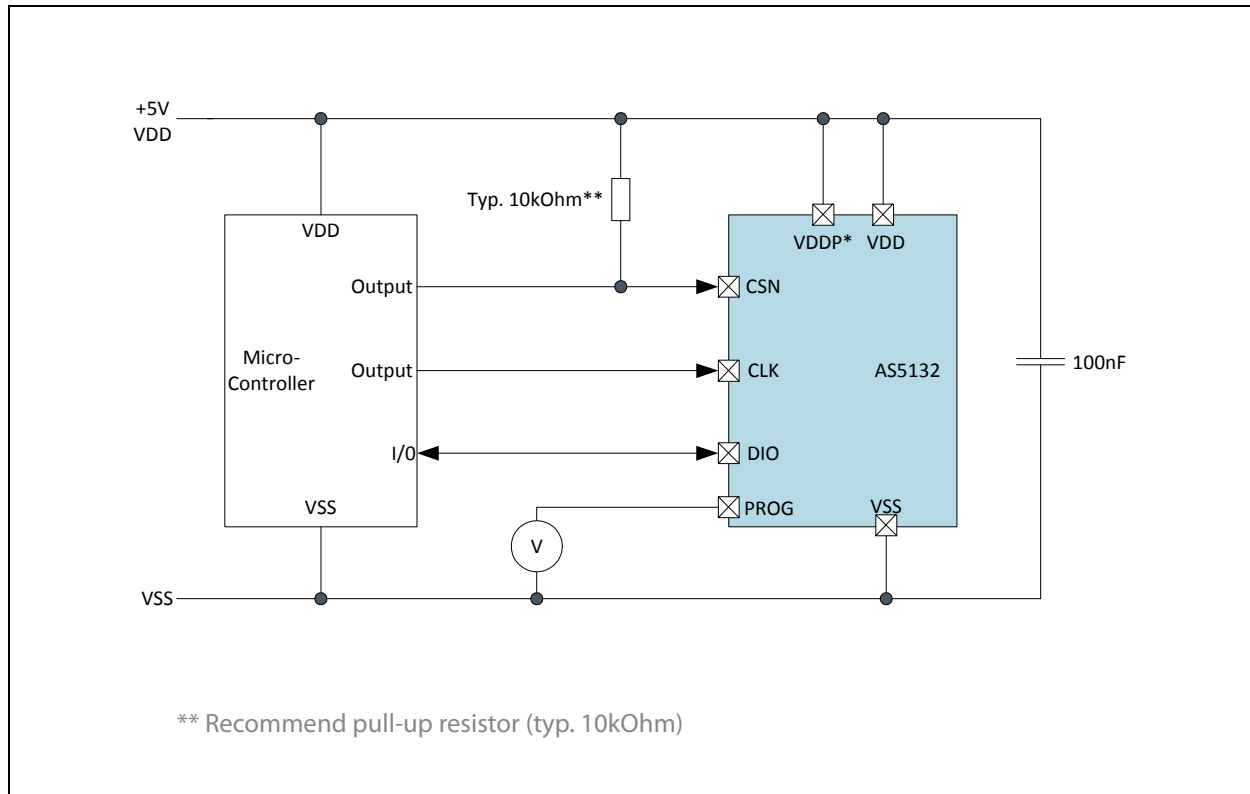
Figure 25 shows the correct digital verification flow. The EZ\_ERR bit is valid only after a power on reset. This bit becomes invalid after a OTP write or read access.

**Figure 25:**  
Programming & Digital Verification Flow



**Analog Verification:** By switching into Extended Mode and sending a READ ANA command, the pin PROG becomes an output sending an analog voltage with each clock representing a sequence of the bits in the OTP register (starting with D61). A voltage of <500mV indicates a correctly programmed bit ("1") while a voltage level between 2V and 3.5V indicates a correctly unprogrammed bit ("0"). Any voltage level in between indicates incorrect programming.

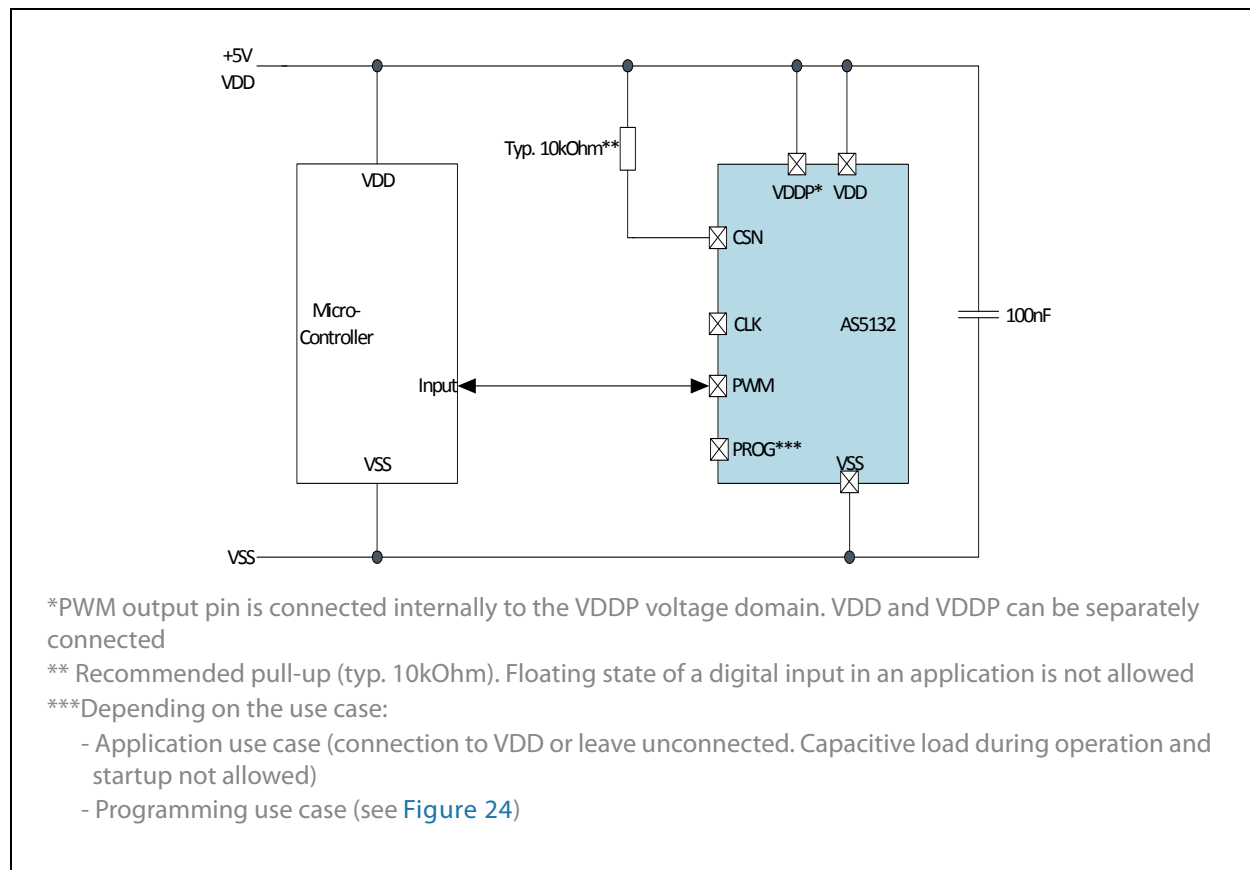
**Figure 26:**  
**Analog OTP Verification**



## Pulse Width Modulation (PWM) Output

The AS5132 provides a pulse width modulated output (PWM), whose duty cycle is proportional to the absolute angle position. [Figure 29](#) shows the output format. In case of an internal error the high pulse contains 12 steps. An error can be easily identified by the external microcontroller. The zero degree angle position is build with 16 steps (12 + 4) high and 359 steps low followed by 8 exit steps.

**Figure 27:**  
PWM Output



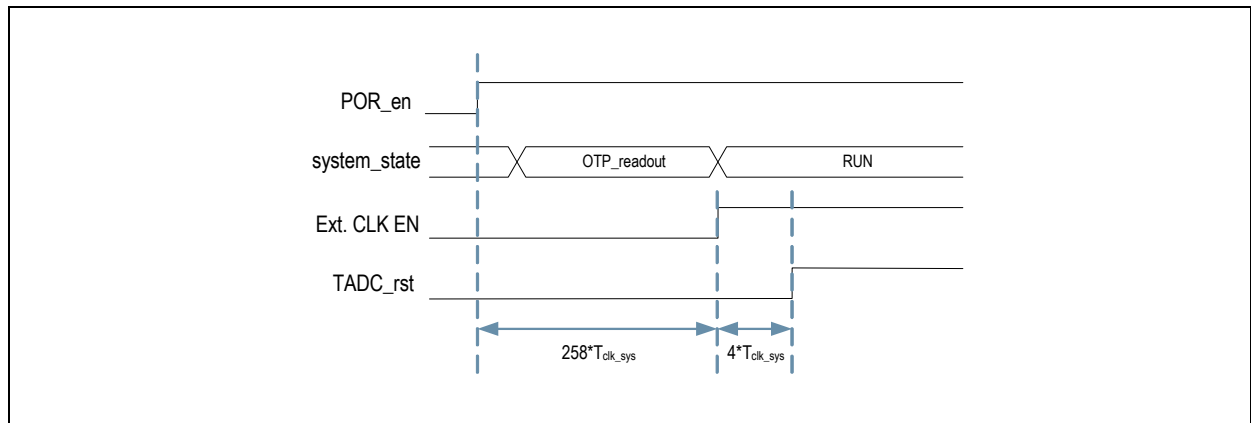
## PWM External Clock

The PWM period depends on the setting of the OTP bit **Ext. CLK EN**. By default the internal clock source is used as a reference. An external clock can be connected to the pin COM/INC.

In case Ext. CLK EN is set, the output-mode which is determined by the states of {COM/INC, Test3, Test2, Test1, Test0} [Figure 31](#) on page 23 during start-up is overwritten and U,V,W commutation mode signals are activated.

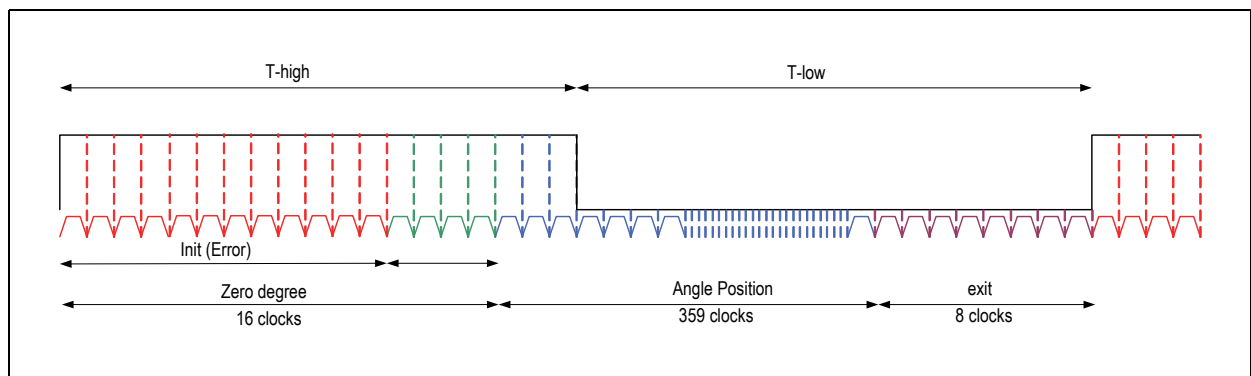
After internal power on reset (POR\_en), the OTP is read out. When the Ext. CLK EN is programmed successfully, the COM/INC pin is used as external clock for the PWM block. After 4 clock cycles of Ext. CLK EN, the reset of TADC (TADC\_rst) and the PWM block is released.

**Figure 28:**  
**Start-Up Procedure**



The reset for the PWM block is synchronized to the external PWM clock. This ensures a save reset also in case the external clock on COM/INC is already running during start-up.

**Figure 29:**  
**PWM Output Signal**



**Figure 30:**  
**PWM Timing with Internal and External CLK Source**

| Symbol       | Parameter           | Min               | Typ | Max | Unit    | Note                                       |
|--------------|---------------------|-------------------|-----|-----|---------|--------------------------------------------|
| $T_{PWMint}$ | PWM Period internal | 600               | 750 | 900 | $\mu s$ | Internal clock source                      |
| $T_{PWMext}$ | PWM Period external | $383 / CLK_{PWM}$ |     |     | $\mu s$ | External clock provided over COM / INC pin |
| $CLK_{PWM}$  | Clock external mode | 0                 |     | 766 | kHz     |                                            |

## Incremental Outputs

Two different incremental output modes are possible. Quadrature A/B mode and selectable Step Mode can be selected by the pins **TEST0**, **TEST1**, **TEST2**, **TEST3** and **COM / INC**.

**Figure 31:**  
Configuration of the Incremental Output Modes

| COM / INC | TEST3 | TEST2 | TEST1 | TEST0 | Output Mode                                 | Pin Assignment                                     |
|-----------|-------|-------|-------|-------|---------------------------------------------|----------------------------------------------------|
| 1         | 0     | 0     | 0     | 0     | Quadrature A/B/I Mode 90 pulses per channel | A → U_A<br>B → V_B<br>I → W_I<br>'0' → S           |
| 1         | 0     | 0     | 0     | 1     | Stepmode 24 pulses and Index width 2        | '0' → U_A<br>'0' → V_B<br>'0' → W_I<br>S_24_2 → S  |
| 1         | 0     | 0     | 1     | 0     | Stepmode 60 pulses and Index width 2        | '0' → U_A<br>'0' → V_B<br>'0' → W_I<br>S_60_2 → S  |
| 1         | 0     | 0     | 1     | 1     | Stepmode 90 pulses and Index width 2        | '0' → U_A<br>'0' → V_B<br>'0' → W_I<br>S_90_2 → S  |
| 1         | 0     | 1     | 0     | 0     | Stepmode 180 pulses and Index width 2       | '0' → U_A<br>'0' → V_B<br>'0' → W_I<br>S_180_2 → S |
| 0         | 0     | 0     | 0     | 0     | U,V,W Commutation Mode (OTP setting)        | U → U_A<br>V → V_B<br>W → W_I<br>'0' → S           |

**Note(s):**

1. The pin setting COM / INC has priority. In case of a low state the device is exclusively in the commutation mode. Not specified states of TEST3, TEST2, TEST1 and TEST0 in incremental mode will enable the quadrature A/B/I mode. This configuration is only read once at startup. It is not recommended to change the state during operation.

## Quadrature A/B Output

**Figure 32:**  
Incremental Output of the AS5132

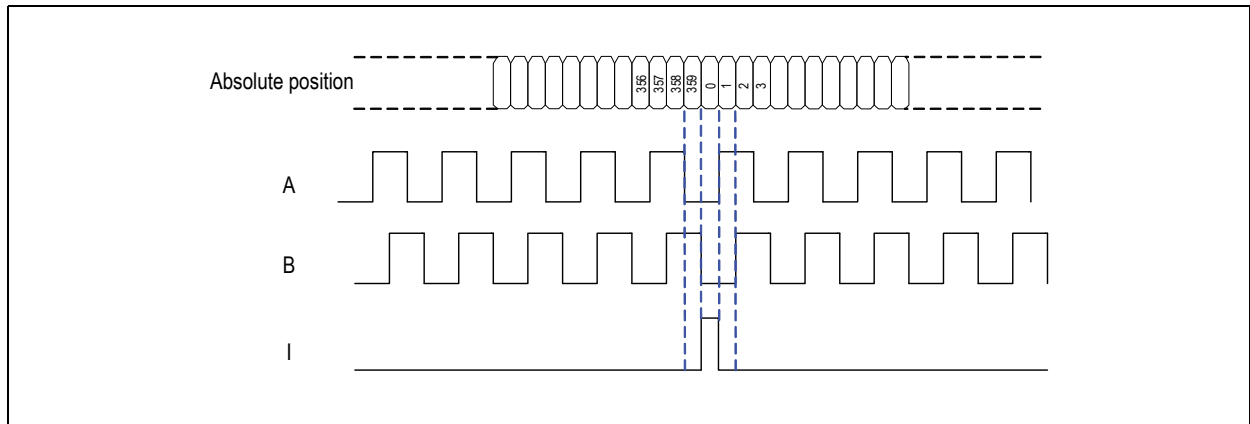
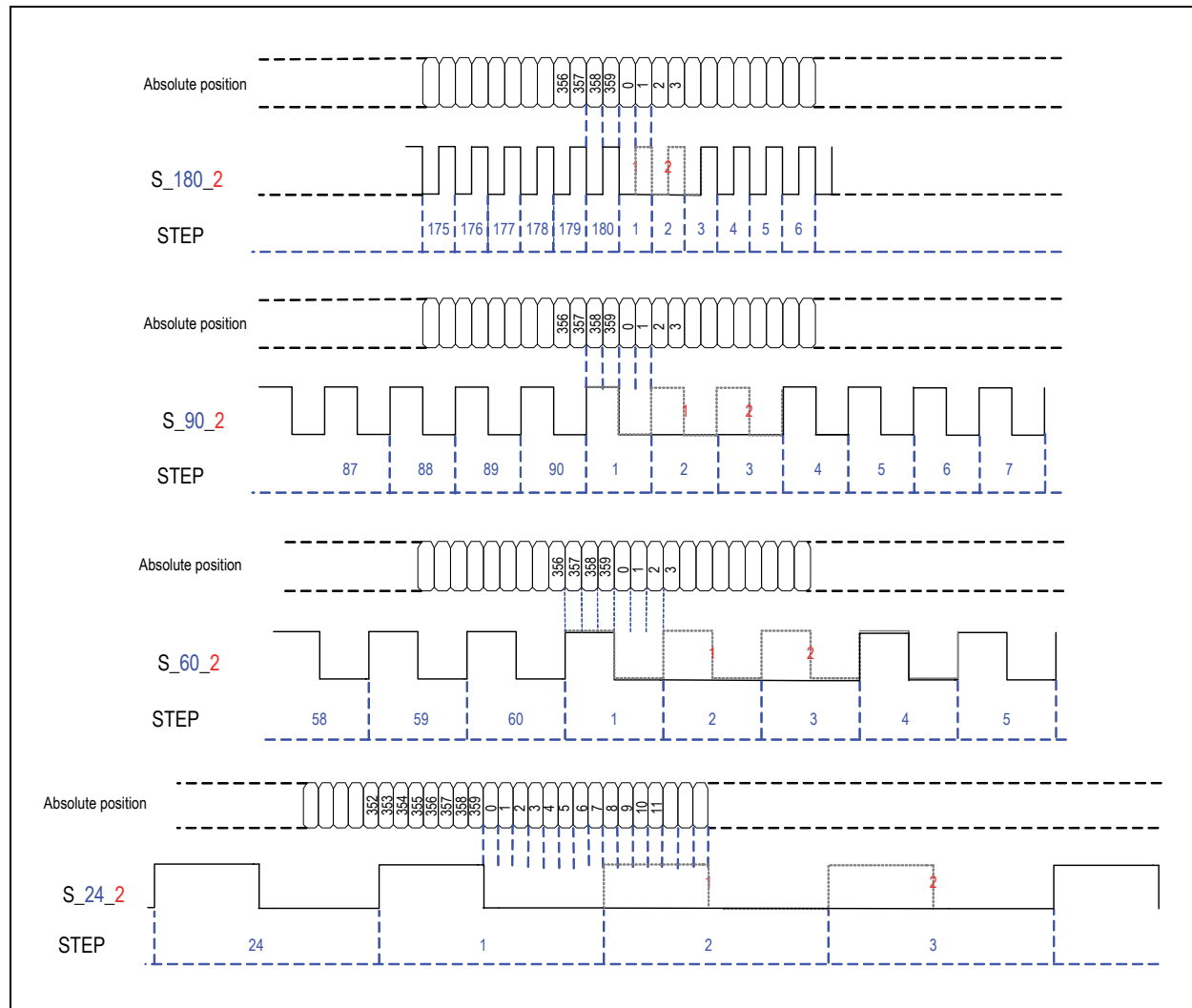


Figure 32 shows the two-channel quadrature output. The index position is mapped to the absolute mechanical zero position. The phase shift between channel A and B indicates the direction of the magnet movement. Channel A leads channel B at a clockwise rotation of the magnet (top view) by 90 electrical degrees. Channel B leads channel A at a counter-clockwise rotation.

### Step Output Mode

Step Output mode provides a specific combination of the **A** incremental signal and the index signal **I**. The number of pulse can be configured with the input pattern of the test input pins.

**Figure 33:**  
Step Mode of the AS5132 with Different Number of Pulses



### Pre-Commutation Function

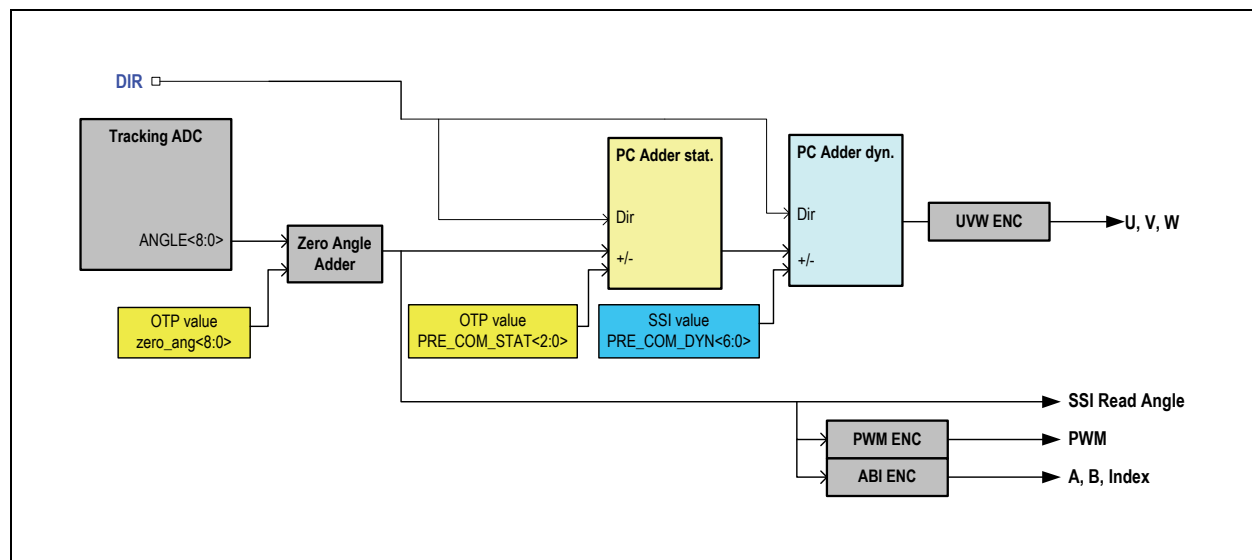
This feature can be used to optimize the torque characteristic at a certain speed of the BLDC motor. The output signals **U**, **V** and **W** can be shifted by a specific number of degrees back and forward. The AS5132 distinguish between the static and dynamic pre commutation value. The static value is similar to an additional zero programming and can be programmed only once. The dynamic value is stored in the interface register and can be changed during operation.

The pin **DIR** defines if the value of pre-commutation is added or subtracted. The dynamic commutation register will be set to zero after a rotation change indicated by the external pin **DIR**. Due to internal synchronization, the outputs U,V,W will change 3 internal clock cycles after the change of **DIR** input signal.

**Figure 34:**  
Definition of the Pre-Commutation Direction

| DIR | Rotation           | Consequence                                   |
|-----|--------------------|-----------------------------------------------|
| 0   | Clock wise         | PRE_COM values added to absolute angle        |
| 1   | Counter clock wise | PRE_COM values subtracted from absolute angle |

**Figure 35:**  
Block Diagram of the Pre-Commutation Function



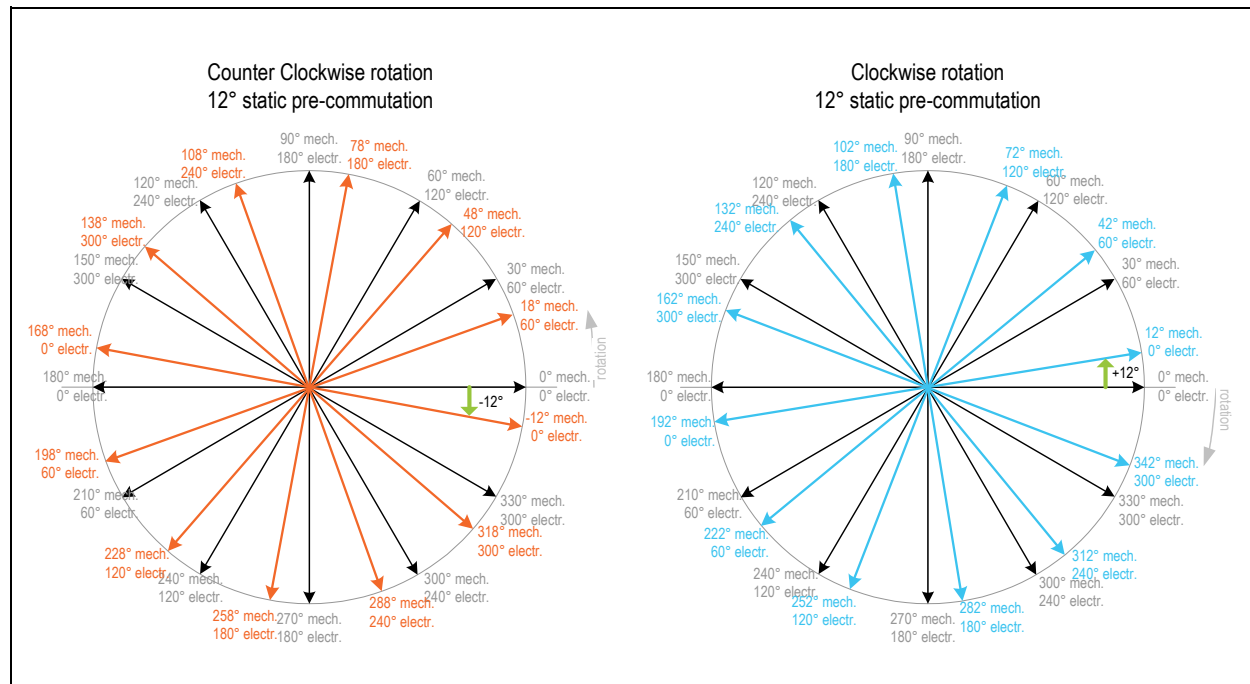
**Note(s):**

1. The dynamic pre-commutation is set to zero always if the direction is changed over the pin **DIR**. A new value **PRE\_COM\_DYN** must be written again. The static pre-commutation is always enabled and will shift the output.

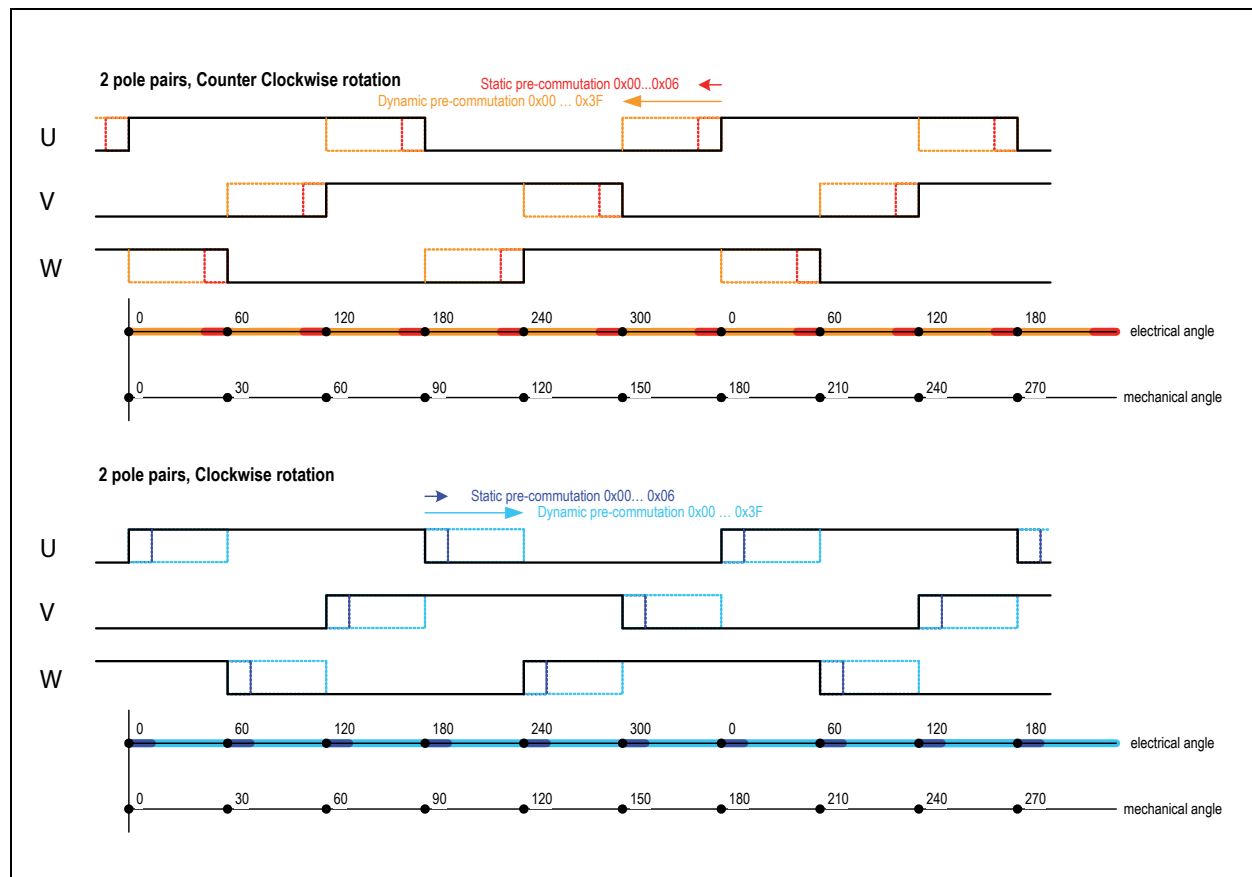
### Commutation Output UVW

The pre-commutation function is used only at the U,V,W output. [Figure 36](#) shows the transition on the outputs U,V,W in case of a two pole pair configuration. The static pre-commutation value was set to 12 degrees.

**Figure 36:**  
**UVW Output Transitions with Pre-Commutation**



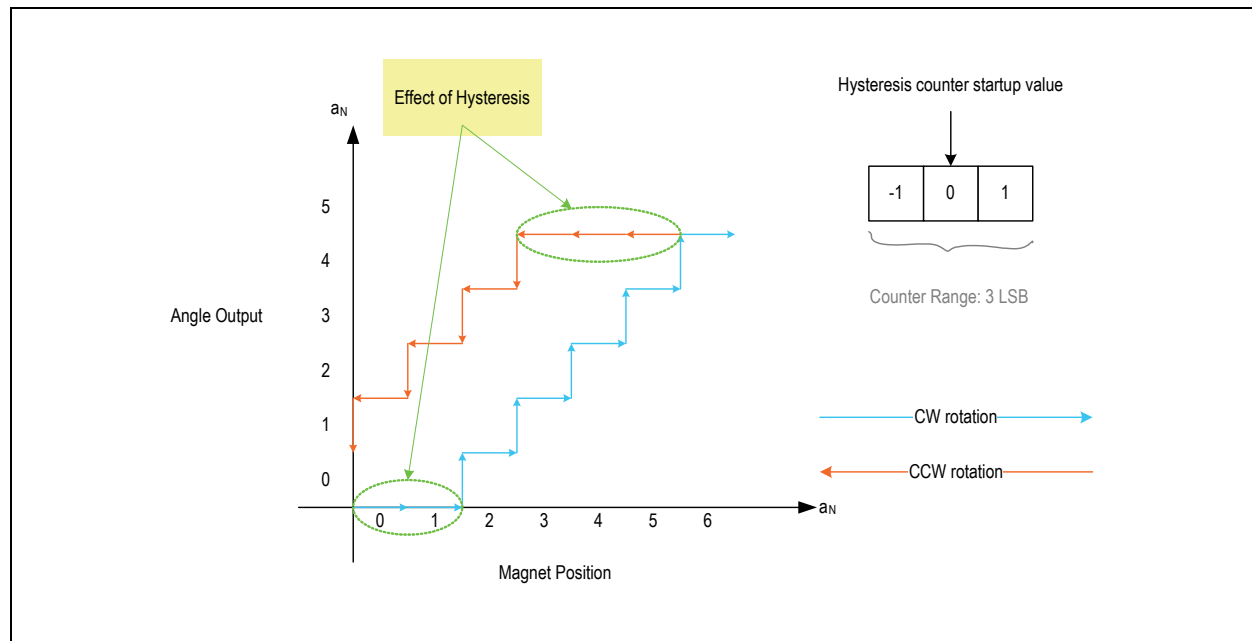
**Figure 37:**  
**Dynamic and Static Pre-Commutation**



### Hysteresis of the Incremental Outputs

A hysteresis is implemented to get a stable output value at the SSI command and to reduce jitter at the PWM and UVW outputs. At start up the hysteresis counter is at 0, the range is  $\pm 1$  LSB. The hysteresis can be deactivated by setting OTP bit **Hyst\_dis**.

**Figure 38:**  
Hysteresis of the Outputs



### Multi Turn Counter

A 9-bit register is used for counting the magnet's revolutions. With each zero transition in any direction, the output of a special counter is incremented or decremented. The initial value after reset is 0 LSB. Clockwise rotation gives increasing angle values and positive turn count. Counter clockwise rotation exhibits decreasing angle values and a negative turn count respectively.

The counter output can be reset by using command 20 – SET MT Counter. It is immediately reset by the rising clock edge of this bit. Any zero crossing between the clock edge and the next counter readout changes the counter value.

### High Speed Operation

The AS5132 is using a fast tracking ADC (TADC) to determine the angle of the magnet. The TADC is tracking the angle of the magnet with cycle time of  $2\mu\text{s}$  (typ. 1.4). Once the TADC is synchronized with the angle, it sets the LOCK bit in the status register. Once it is locked, it requires only one cycle [ $2\mu\text{s}$  (typ. 1.4)] to track the moving magnet. The AS5132 can operate in locked mode at rotational speeds up to max. 72,900 rpm.

**Propagation Delay**

The propagation delay is the time required from reading the magnetic field by the Hall sensors to calculating the angle and making it available on the serial or PWM interface. While the propagation delay is usually negligible on low speeds, it is an important parameter at high speeds. The longer the propagation delay, the larger becomes the angle error for a rotating magnet as the magnet is moving while the angle is calculated. The position error increases linearly with speed.

**Error Detection**

The following errors are detected by the system:

- Lock bit → The TADC has not yet found a valid angular position
- AGC alarm → The AGC <5:1> value is “1 1111 binary”. Magnetic field is too weak.

By default, Lock bit error should activate the error condition at the outputs. The AGC alarm is permanently available at the DIAG pin.

Error condition at commutation and incremental outputs:

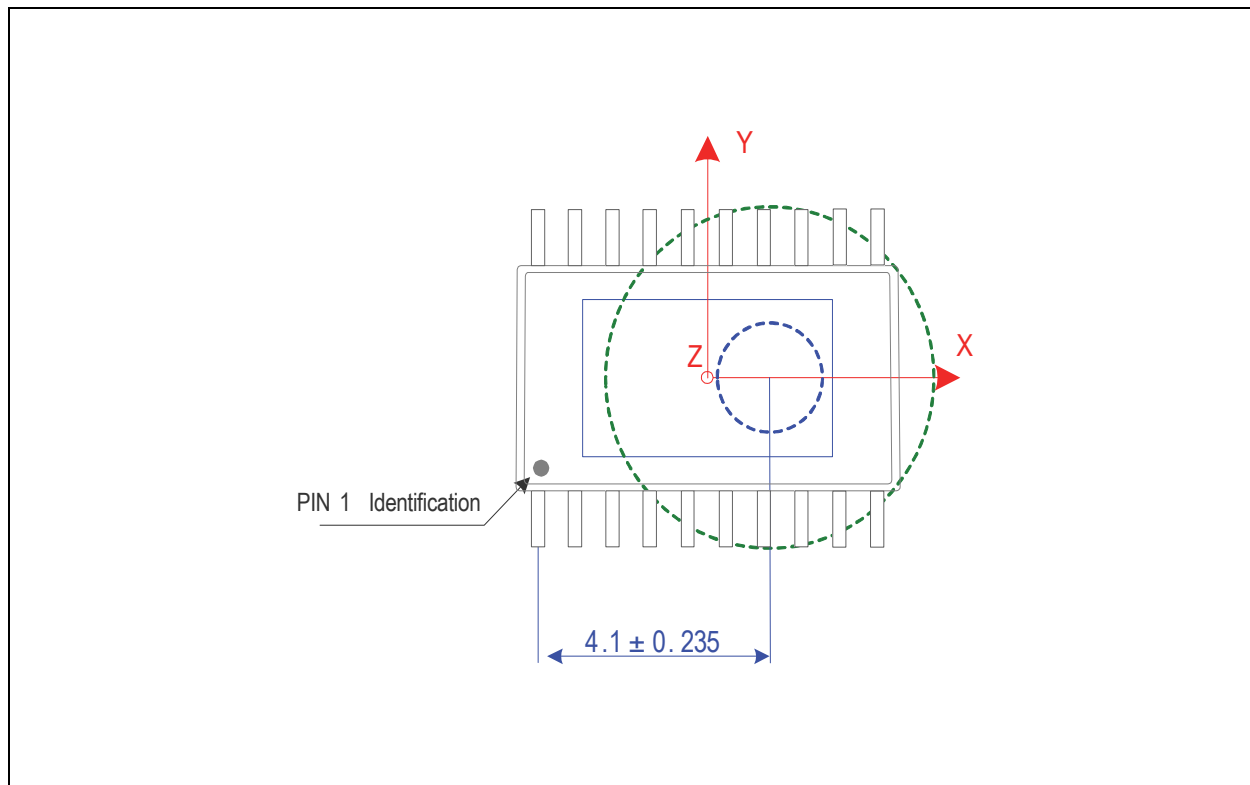
- U, V and W outputs all '0'
- A, B and I outputs all '1'

## Application Information

### Physical Placement of the Magnet

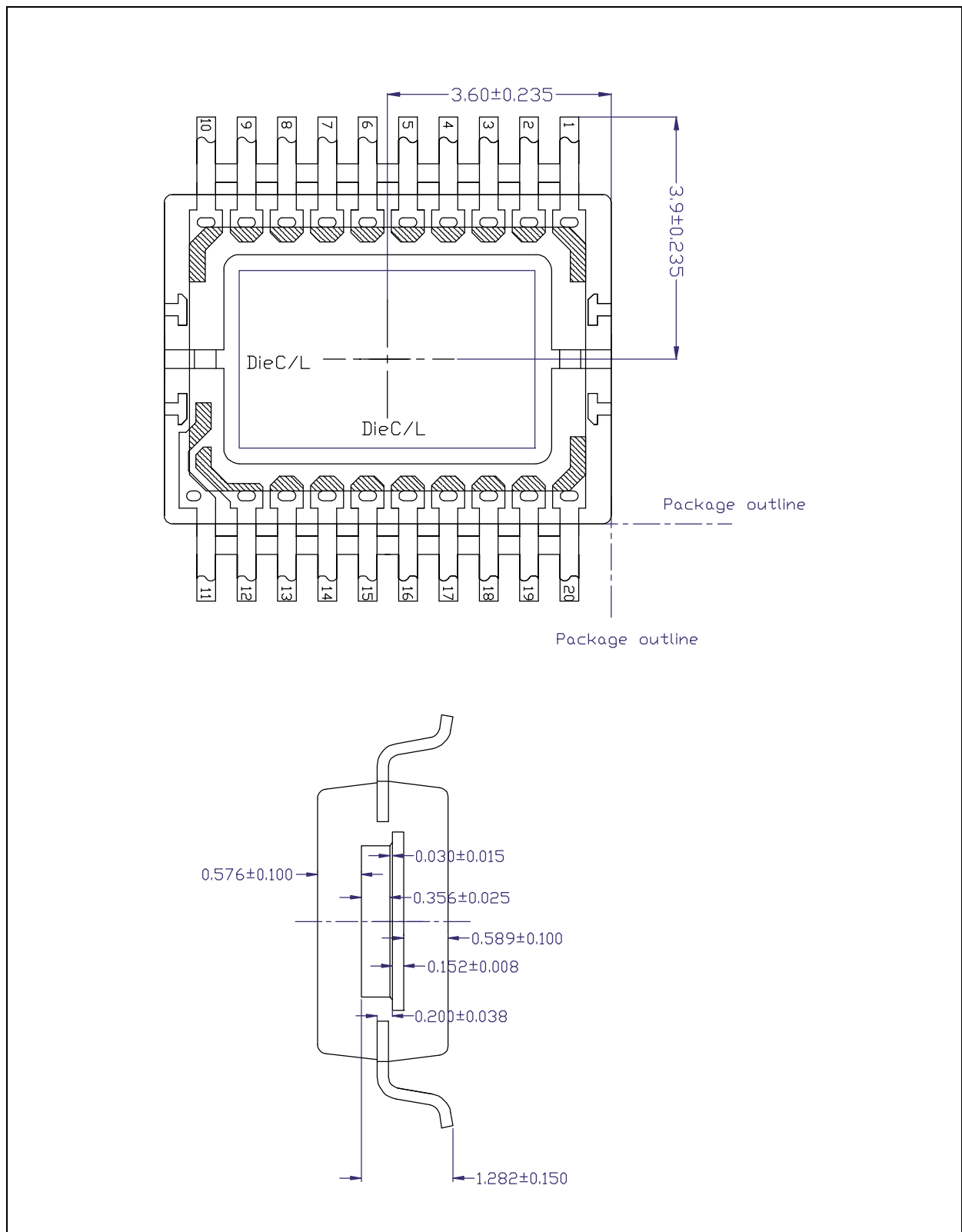
The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the IC package as shown in Figure 39.

**Figure 39:**  
Defined IC Center and Magnet Displacement Radius



The centre of the Hall sensor array is shifted by a constant value in x axis indicated by the blue circle. In the application it is important to refer to this point.

**Figure 40:**  
**Vertical Cross Section of SSOP-20**



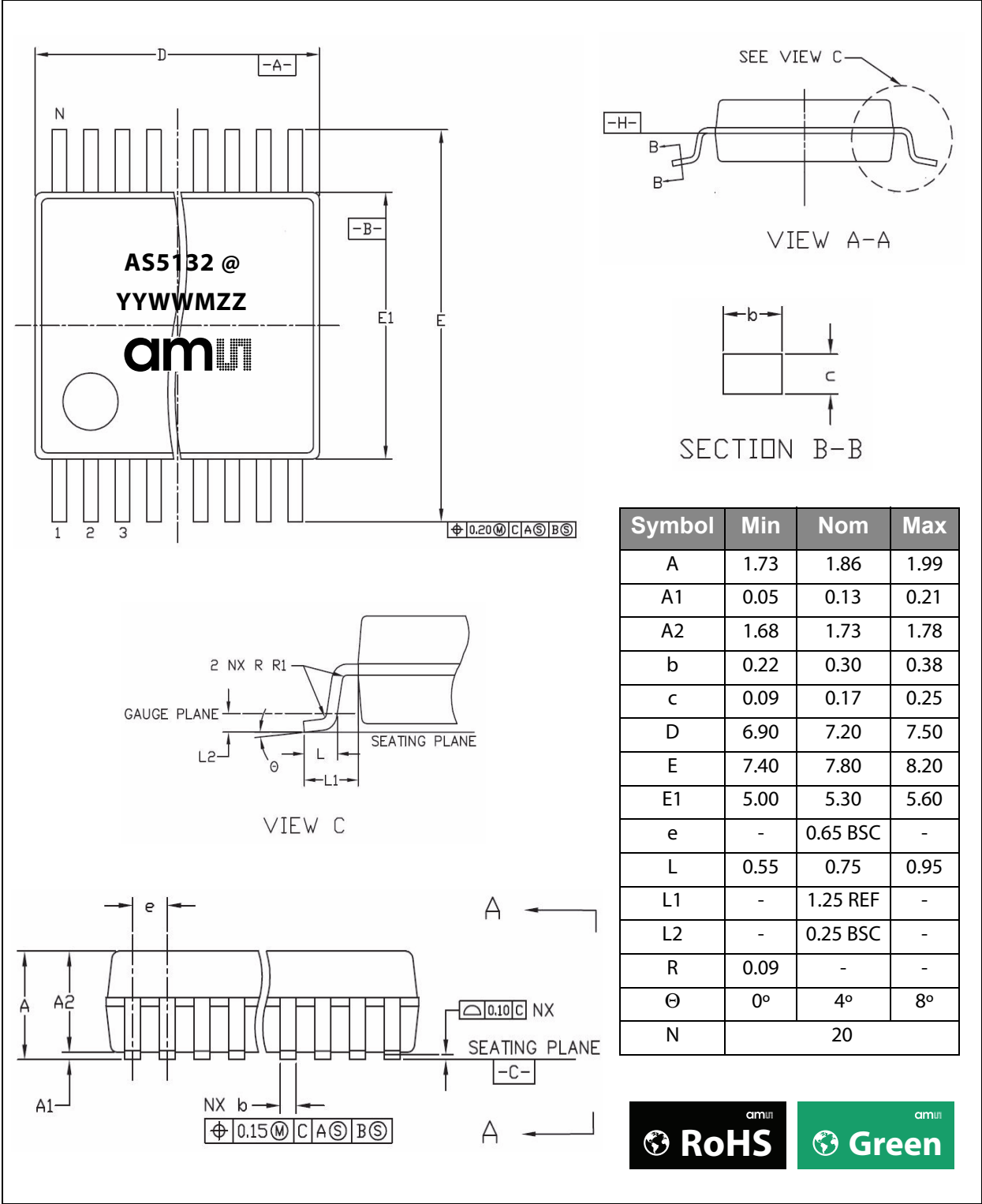
**Note(s):**

1. All dimensions in mm.
2. Die is slightly off centered.

Package Drawings & Markings

The device is available in a 20-Lead Shrink Small Outline package.

Figure 41:  
Package Drawings and Dimensions



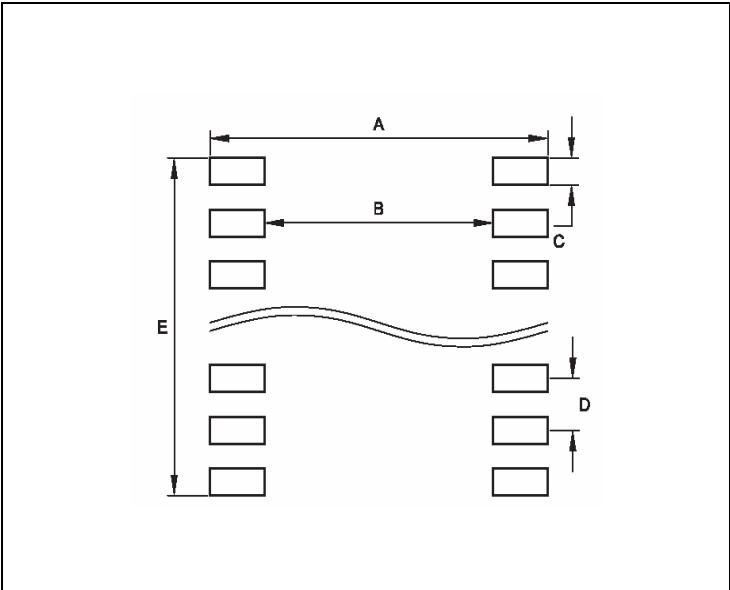
- Note(s):**
1. Dimensions and tolerancing conform to ASME Y14.5M-1994.
  2. All dimensions are in millimeters. Angles are in degrees.

Figure 42:  
Marking: @YYWMZZ

| @                 | YY                                        | WW                 | M                | ZZ                         |
|-------------------|-------------------------------------------|--------------------|------------------|----------------------------|
| Sublot identifier | Last two digits of the manufacturing year | Manufacturing week | Plant identifier | Assembly traceability code |

Recommended PCB Footprint

Figure 43:  
PCB Footprint



| Recommended Footprint Data |      |       |
|----------------------------|------|-------|
| Symbol                     | mm   | inch  |
| A                          | 9.02 | 0.355 |
| B                          | 6.16 | 0.242 |
| C                          | 0.46 | 0.018 |
| D                          | 0.65 | 0.025 |
| E                          | 6.31 | 0.248 |

## Ordering & Contact Information

The devices are available as the standard products shown in Figure 44.

**Figure 44:**  
**Ordering Information**

| Ordering Code | Package | Marking | Delivery Form               | Delivery Quantity |
|---------------|---------|---------|-----------------------------|-------------------|
| AS5132-HSST   | SSOP-20 | AS5132  | 13" Tape & Reel in dry pack | 2000              |
| AS5132-HSSM   | SSOP-20 | AS5132  | 7" Tape & Reel in dry pack  | 500               |

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### Headquarters

ams AG  
Tobelbaderstrasse 30  
8141 Premstaetten  
Austria, Europe

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| Product Preview          | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice                                                                    |
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## Revision Information

| Changes from 2-04 (2014-Sep-05) to current revision 2-06 (2016-Jan-26) | Page |
|------------------------------------------------------------------------|------|
| <b>2-04 (2014-Sep-05) to 2-05 (2016-Jan-22)</b>                        |      |
| Updated text under General Description section                         | 1    |
| Updated Figure 1                                                       | 1    |
| Updated Figure 4                                                       | 4    |
| Updated Figure 14                                                      | 12   |
| Updated text under Figure 17                                           | 13   |
| Updated Figure 18                                                      | 15   |
| Updated Programming Verification section                               | 19   |
| Updated Figure 27                                                      | 21   |
| <b>2-05 (2016-Jan-22) to 2-06 (2016-Jan-26)</b>                        |      |
| Updated Figure 4                                                       | 4    |
| Updated Figure 14                                                      | 12   |
| Updated Figure 27                                                      | 21   |

**Note(s):**

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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