Important notice on ams-OSRAM documents

**As part of the acquisition of the non-optical analog/mixed-signal sensor portfolio from ams-OSRAM by Infineon, Infineon is in the process of rebranding all relevant documents.
Due to the large volume of documents, this process will be completed in phases. In the interim, we are providing access to legacy ams-OSRAM documents under the terms of a trademark license agreement.**

The attached document is a legacy ams-OSRAM document and has not been rebranded to reflect the acquisition by Infineon.

Please note that:

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AS5048L

Magnetic Rotary Encoder (13-bit Angular Position Sensor)

General Description

The AS5048L is an easy to use 360° angle position sensor with a 13-bit digital output.

The IC measures the absolute position of the magnet's rotation angle and consists of Hall sensors, analog digital converter and digital signal processing. The absolute position information of the magnet is directly accessible over a PWM output and can be read out over a standard SPI interface.

The zero position can be programmed via SPI. This simplifies the assembly of the complete system because the zero position of the magnet does not need to be mechanically aligned. The sensor tolerates misalignment, air gap variations, temperature variations and as well external stray magnetic fields. This robustness and wide temperature range (-40°C up to 125°C) of the AS5048L makes the IC ideal for rotation angle sensing in harsh industrial and medical environments. An internal voltage regulator allows the AS5048L to operate at either 3.3 V or 5 V supplies.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5048L, Magnetic Rotary Encoder (13-bit Angular Position Sensor) are listed below:

Figure 1:
Added Value of Using AS5048L

Benefits	Features
Highest reliability and durability	Contactless rotary position sensor over 360°
Low material costs (no shielding)	Immune to external magnetic stray fields
High precision	13-bit core resolution
Easy to use	Standard SPI interface and PWM
No external programmer needed	Zero position programmable via SPI
Robust environmental tolerance	Temperature range: -40°C to 125°C

Applications

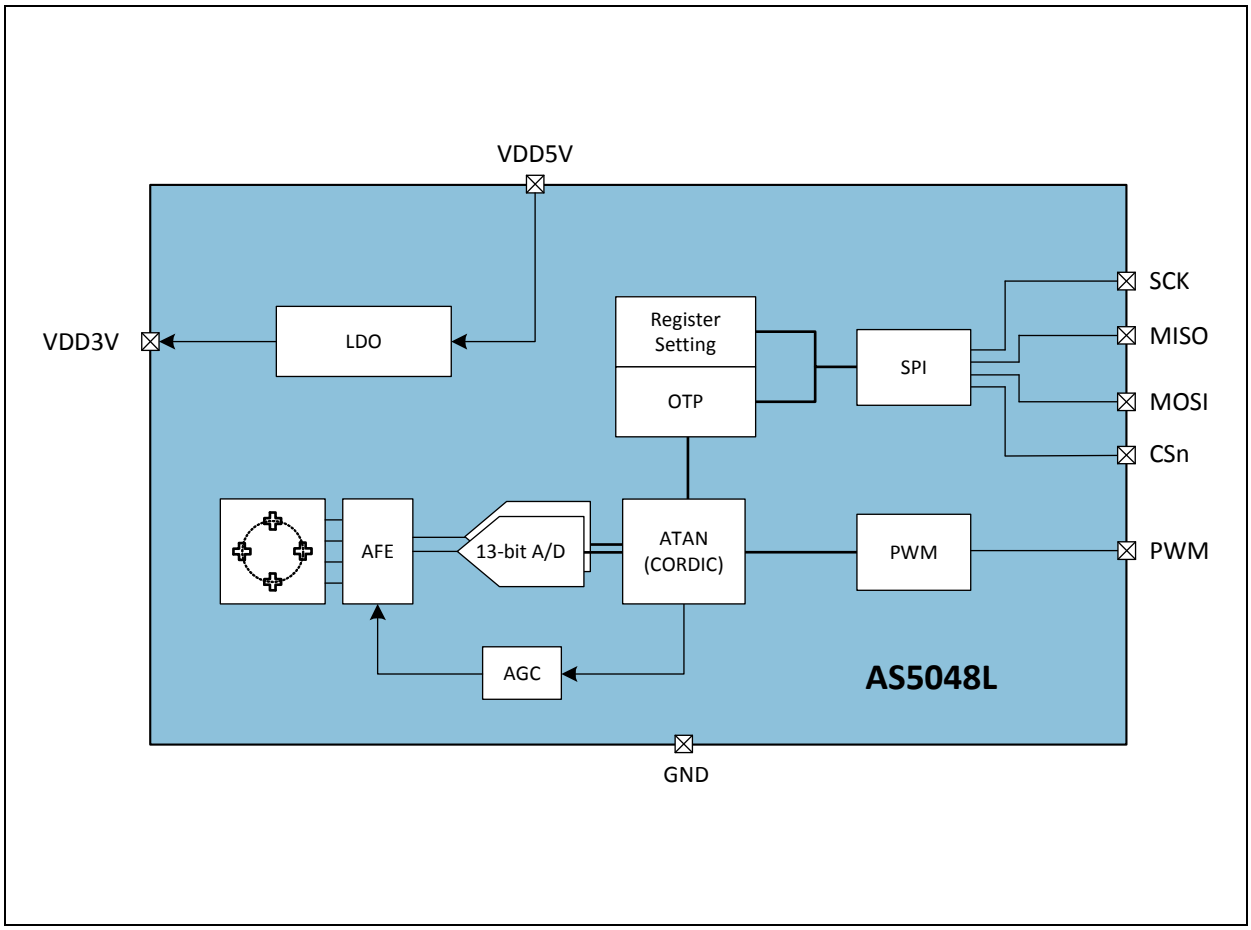
The applications of AS5048L include:

- Robotic joint position detection
- Industrial motor position control
- Medical robots and fitness equipment

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:
AS5048L Block Diagram



Pin Assignment

The AS5048L pin assignment is shown below.

Figure 3:
TSSOP14 Pin Configuration

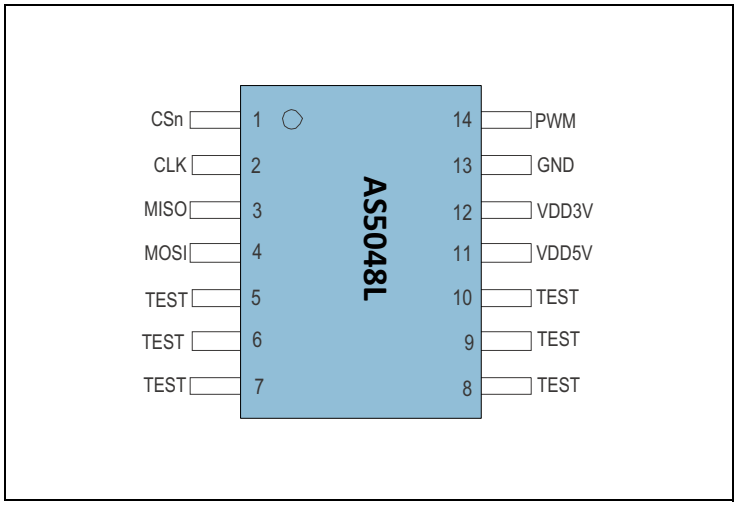


Figure 4:
TSSOP14 Pin Description for AS5048L

Pin	AS5048L	Pin Type	Description
1	CSn	Digital input with Schmitt trigger	SPI chip select - active low
2	CLK		SPI clock input
3	MISO	Digital I/O with Schmitt trigger in the input path	SPI master in/slave out
4	MOSI	Digital input with Schmitt trigger	SPI master out/slave in
5	TEST	Analog I/O	Test pins. These pins should be connected to GND.
6	TEST		
7	TEST		
8	TEST		
9	TEST		
10	TEST		
11	VDD5V	Supply pad	Positive Supply Voltage, 3.0 to 5.5 V
12	VDD3V		3.3V Regulator output; internally regulated from VDD. Connect to VDD for 3V supply voltage. 10µF capacitor to GND required in 5V operation mode
13	GND		Negative Supply Voltage (GND)
14	PWM	Digital output – push-pull	Pulse Width Modulation output

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
Electrical Parameters					
VDD5V	DC supply voltage at VDD5V pin	-0.3	7	V	
VDD3V	DC voltage at VDD3V pin	-0.3	5	V	
GND	DC voltage at GND pin	-0.3	0.3	V	
V_{IN}	Input pin voltage		VDD+0.3	V	
I_{SCR}	Input current (latchup immunity)	-100	100	mA	Norm: Jedec 78
Electrostatic Discharge					
ESD	Electrostatic discharge	± 2		kV	Norm: MIL 883 E method 3015
Power Dissipation					
P_T	Total power dissipation (all supplies and outputs)		150	mW	
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage temperature	-55	125	°C	
T_{BODY}	Package body temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 “Moisture Solid State Surface Mount Devices”. The lead finish from Pb-free leaded packages is matte tin (100%Sn)
RH_{NC}	Relative Humidity non-condensing	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168h

Electrical Characteristics

All in this specification defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

Operating Conditions

Figure 6:
Operating Conditions

Symbol	Parameter	Min	Max	Unit	Note
VDD5V	Positive supply voltage	4.5	5.5	V	5V Operation via LDO
VDD3V		3	3.6	V	LDO output voltage
VDDCORE	Positive core supply voltage	3	3.6	V	
T_{AMB}	Ambient temperature	-40	125	°C	
I_{SUP}	Supply Current		15	mA	

DC/AC Characteristics for Digital Inputs and Outputs

Figure 7:
DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit
CMOS Digital Input with Schmitt Trigger: CSn, CLK, MOSI				
V_{IH}	High level input voltage	0.7 * VDDCORE		V
V_{IL}	Low level input voltage		0.3 * VDDCORE	V
I_{LEAK}	Input leakage current		1	µA
CMOS Output: PWM, MISO				
V_{OH}	High level output voltage	VDDCORE - 0.5		V
V_{OL}	Low level output voltage		GND+0.4	V
C_L	Capacitive load		50	pF
I_{OUT}	Output current		4	mA

Electrical System Specifications

VDD5V = 5V, $T_{Ambient}$ = -40 to 125°C unless noted otherwise.

Figure 8:
System Specification

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bz	Magnetic input field		30	50	70	mT
f_{sample}	Output sampling rate		10.2	11.25	12.4	kHz
RES	Output Resolution			13		Bit
Noise	Sensor output noise	rms value			0.06	Deg
t_{prop}	System propagation delay		90.7	100	110.2	µs
f_{PWM}	PWM frequency		0.907	1	1.102	kHz
INL_{OPT} @25°C	Non-linearity, optimum placement of the magnet				± 0.8	Deg
INL OPT+TEMP	Non-linearity optimum placement of the magnet over the full Temperature Range				±1	Deg
INL DIS+TEMP	Non-linearity @ displacement of magnet and temperature -40°C to 125°C	Assuming N35H Magnet (D=8mm, H=3mm) 500um displacement in x and y z-distance @ 2000um			±1.2	Deg
$t_{startup}$	Startup Time				10	ms

Functional Description

The AS5048L is a magnetic Hall sensor system manufactured in a CMOS process. A lateral Hall sensor array is used to measure the magnetic field components perpendicular to the surface of the chip.

The integrated Hall sensors are placed around the center of the device and deliver a voltage representation of the magnetic flux Bz.

Through Sigma-Delta Analog-to-Digital Converter (ADC) and Digital Signal-Processing (DSP) algorithms, the AS5048L provides accurate high-resolution absolute angular position information. This is executed by a Coordinate Rotation Digital Computer (CORDIC) which calculates the angle and the magnitude of the Hall array signals.

A small diametrically magnetized (two-pole) standard magnet provides the angular position information. Depending on the system requirements different magnet diameters are possible. Additional flexibility is given by the wide range of the magnetic input range. The AS5048L can be combined with NeFeB, SmCo and alternative magnet materials e.g. hard ferrites.

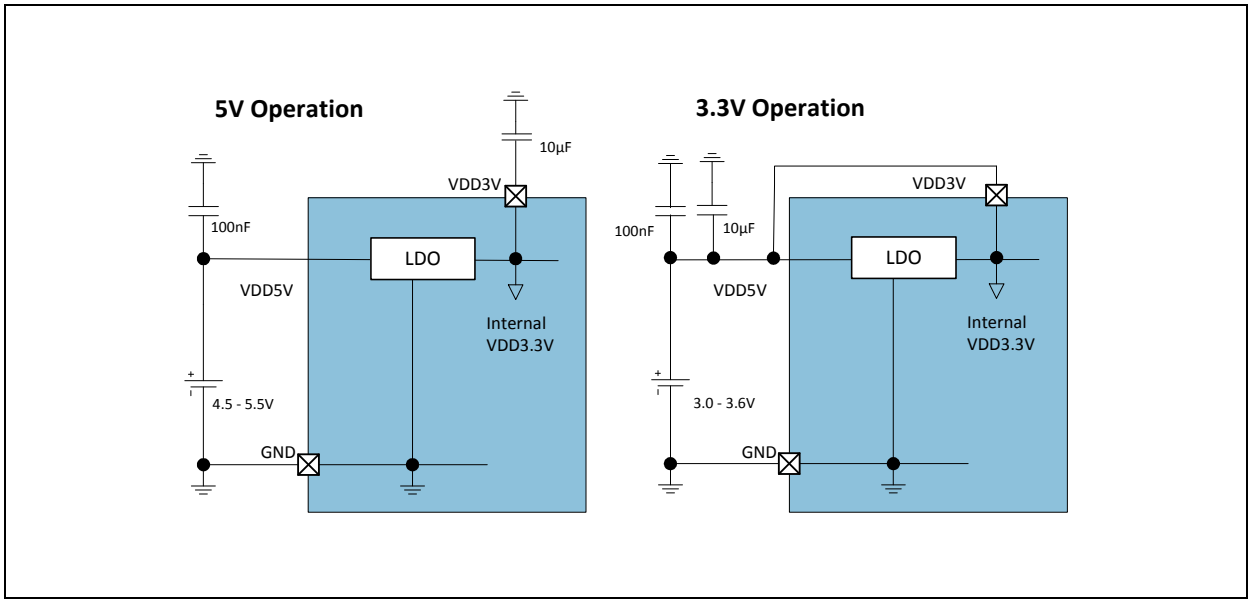
A simple programming of the zero position is possible over the digital interface. No additional programmer is needed. The AS5048L uses one time programmable (OTP) fuses for permanent programming of the user settings. The verification is possible over a simple digital readout of the OTP content.

Operation

Supply Voltage Configuration

The AS5048L operates at 5V ±10%, using an internal Low-Dropout (LDO) voltage regulator. Alternatively 3.3V operation is possible. The **VDD3V** output is intended for internal use only. **It must not be loaded with an external load.**

Figure 9:
Connections for 5V or 3.3V Supply Mode



Note(s) and/or Footnote(s):

1. The pin **VDD3V** must always be buffered by a 10 µF capacitor in 5V operation. It must not be left floating, as this may cause unstable internal supply voltages which may lead to larger output jitter of the measured angle.
   In 3V operation the **VDD3V** must be shorted to **VDD5V.** The ambient temperature T_{AMB} is limited to 125°C in this mode.

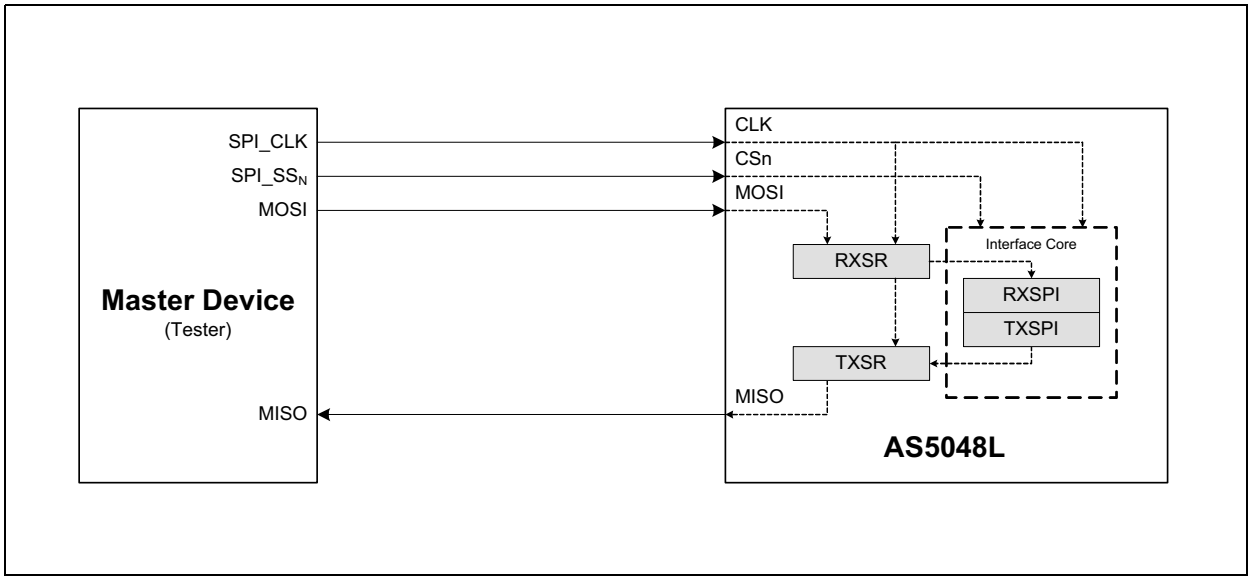
SPI Interface

The 16 bit SPI Interface enables read / write access to the register blocks and is compatible to a standard micro controller interface. The SPI is active as soon as **CSn** is pulled low. The AS5048L then reads the digital value on the **MOSI** (master out slave in) input with every falling edge of **CLK** and writes on its **MISO** (master in slave out) output with the rising edge. After 16 clock cycles **CSn** has to be set back to a high status in order to reset some parts of the interface core.

SPI Interface Signals (4-Wire Mode, Wire_mode = 1)

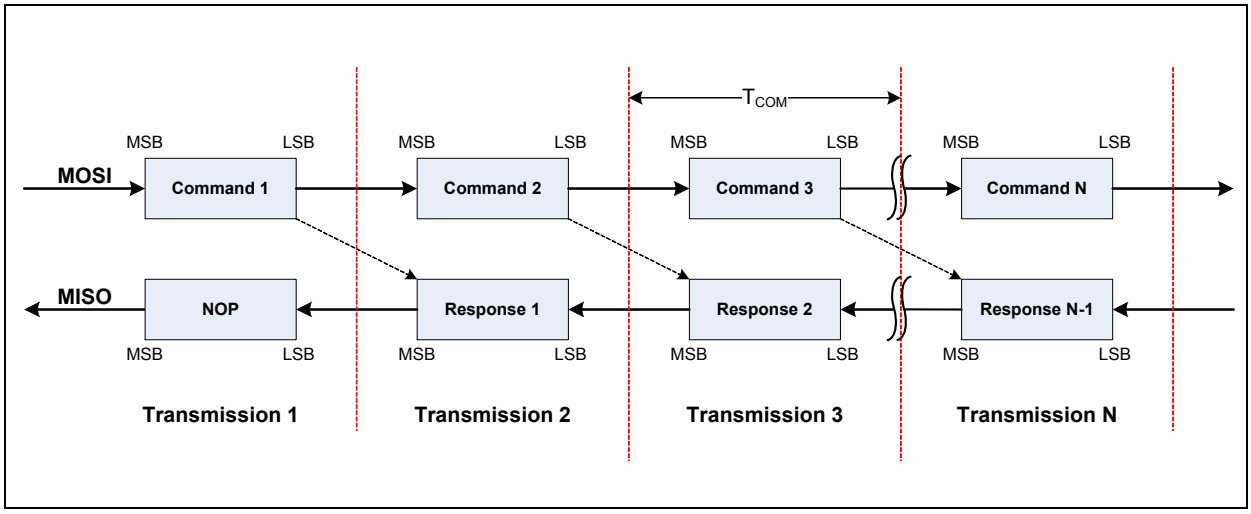
The AS5048L only supports slave operation mode. Therefore **CLK** for the communication as well as the **CSn** signal has to be provided by the test equipment. The following picture shows a basic interconnection diagram with one master and an AS5048L device and a principle schematic of the interface core.

Figure 10:
SPI Connection AS5048L with µC



Because the interface has to decode the sent command before it can react and provide data the response of the chip to a specific command applied at a time T can be accessed in the next transmission cycle ending at T + TCOM. The data are sent and read with **MSB first**. Every time the chip is accessed it is sending and receiving data.

Figure 11:
SPI Command/Response Data Flow



SPI Timing

Figure 12:
SPI Timing Diagram

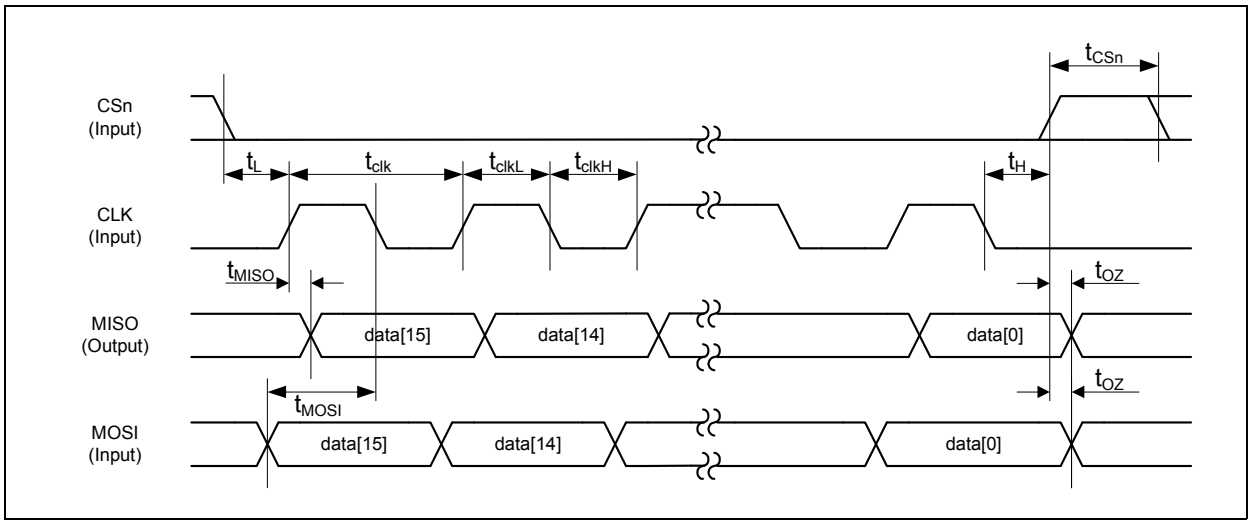


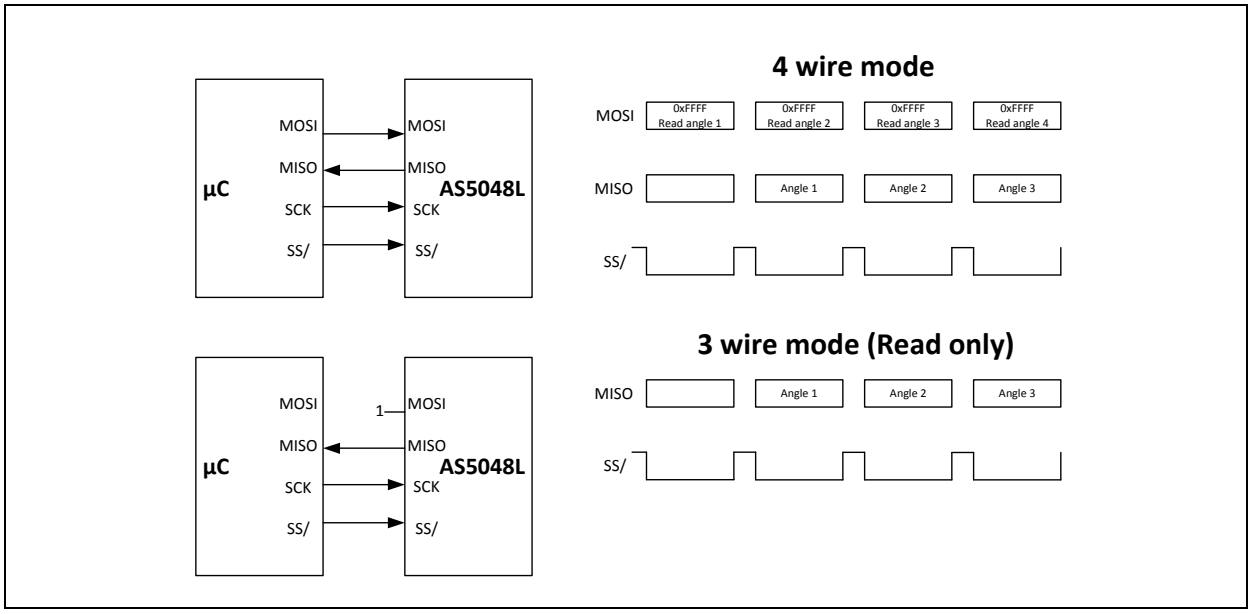
Figure 13:
SPI Timing Characteristics

Parameter	Description	Min	Max	Unit
t_L	Time between CSn falling edge and CLK rising edge	350		ns
T_{CLK}	Serial clock period	100		ns
t_{CLKL}	Low period of serial clock	50		ns
t_{CLKH}	High period of serial clock	50		ns
t_H	Time between last falling edge of CLK and rising edge of CSn	50		ns
T_{CSnH}	High time of CSn between two transmissions	350		ns
t_{MOSI}	Data input valid to clock edge	20		ns
t_{MISO}	CLK edge to data output valid		20	ns

SPI Connection to the Host µC

Single Slave Mode

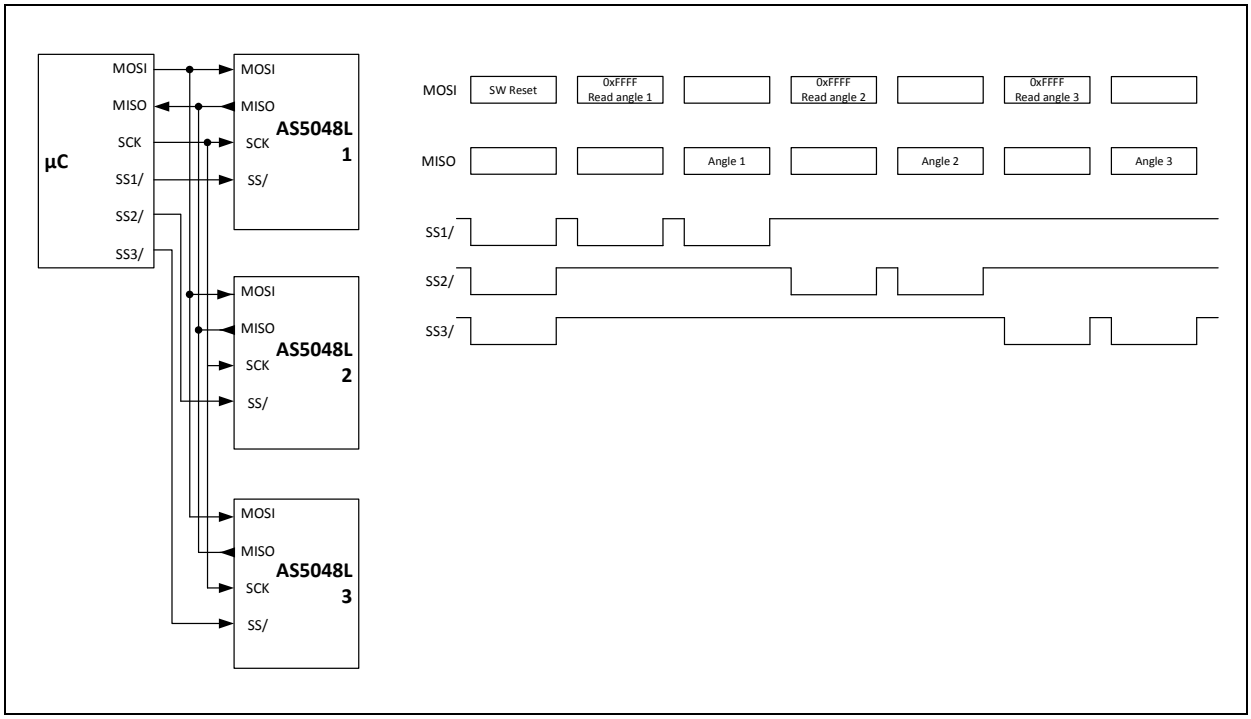
Figure 14:
Single Slave Mode



Single Slave Mode: This figure shows the SPI connection to the host µC using Single Slave Mode.

3 Wire Mode (read only)

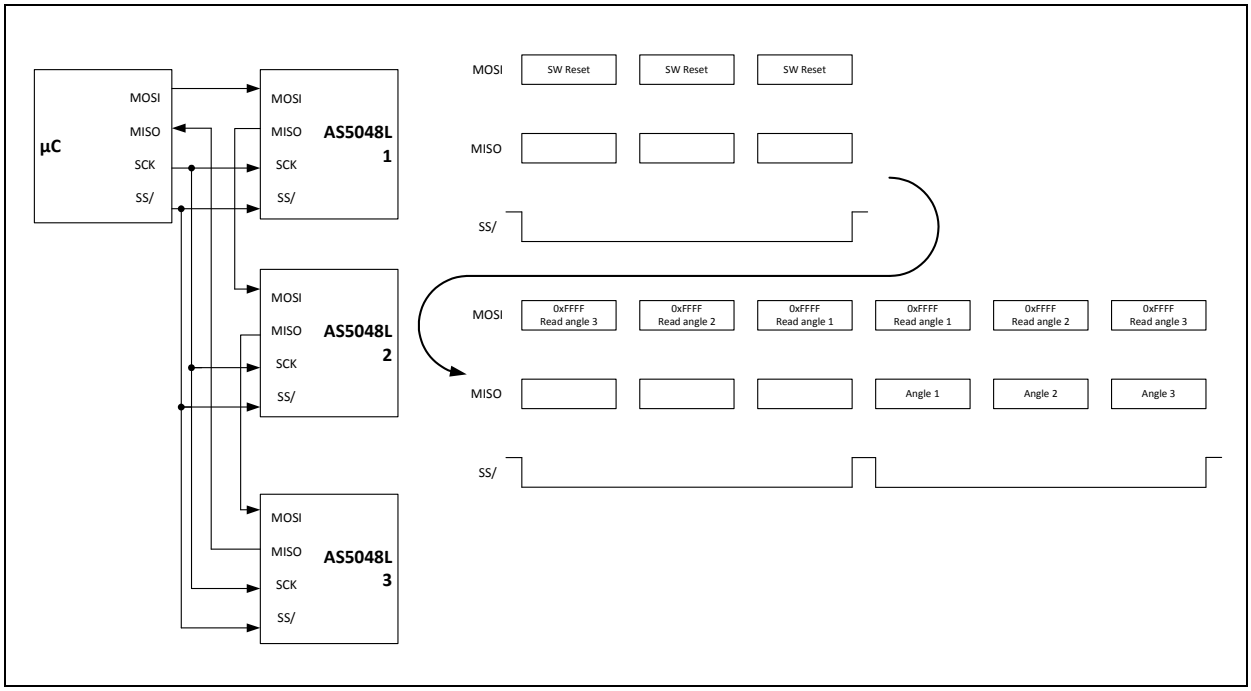
Figure 15:
Multiple Slave, n+3 Wire (Separate ChipSelect)



Multiple Slave, n+3 Wire (Separate ChipSelect): This figure shows the SPI connection to the host µC using 3 Wire mode.

Daisy Chain, 4 Wire

Figure 16:
Daisy Chain, 4 Wire



Daisy Chain, 4 Wire: This figure shows the SPI connection to the host µC using Daisy Chain, 4 wire mode.

SPI Communication Command Package

Every command sent to the AS5048L is represented with the following layout.

Figure 17:
SPI Command Package

Command Package																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	PAR	RWn	Address<13:0>													

Bit Definition & Description	
PAR	Parity bit (EVEN)
RWn	Indicates read(1) or write(0) command
Address	14 bit address code

Read Package (Value Read from AS5048L)

The read frame always contains two alarm bits, the parity and error flags and the addressed data of the previous read command.

Figure 18:
SPI Read Package

Read Package															
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	PAR	EF	Data<13:0>													
Bit Definition & Description																
PAR		Parity bit (EVEN)														
EF		Error flag indicating a transmission error in a previous host transmission														
Data		14 bit addressed data														

Write Data Package (Value Written to AS5048L)

The write frame is compatible to the read frame and contains two additional bits, parity flag and R flag.

If the previous command was a write command a second package has to be transmitted.

Figure 19:
SPI Write Data Package

Data Package															
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	PAR	R	Data <13:0>													
Bit Definition & Description																
PAR		Parity bit (EVEN)														
R		Has to be 0														
Data		14 bit data to write to former selected address														

Register Description

The register description for this device is shown below.

Note(s): To change a configuration, read out the register, modify only the desired bits and write the new configuration. Blank fields may contain factory settings.

Figure 20:
SPI Register Map

Address hex	Name	Access Type	Bit	Symbol	Default	Description
Control and Error Registers						
x0000	NOP	R	13 : 0	NOP	0	No operation dummy information
x0001	Clear Error Flag	R	13 : 3	Not used	n.a.	Error Register. All errors are cleared by access
			2	Parity Error	0	
			1	Command Invalid		
			0	Framing Error		
x0003	Programming Control	R/W	13 : 7	Not used	0	Programming control register. Programming must be enabled before burning the fuse(s). After programming is a verification mandatory. See programming procedure.
			6	Verify		
			5	Not used		
			4			
			3	Burn		
			2	Reserved		
			1			
			0	Programming Enable		

Address hex	Name	Access Type	Bit	Symbol	Default	Description
Programmable Customer Settings						
x0016	OTP Register Zero Position Hi	R/W + Program	13	Not used	0	Zero Position value high byte
			:			
			8			
			7	Zero Position <12>	0	
			:	:	:	
			0	Zero Position <5>	0	
x0017	OTP Register Zero Position Low 6 LSBs	R/W + Program	13	Not used	0	Zero Position remaining 5 lower LSB's
			:			
			6			
			5	Zero Position <4>	0	
			:	:	:	
			1	Zero Position <0>	0	
			0	Not used	0	

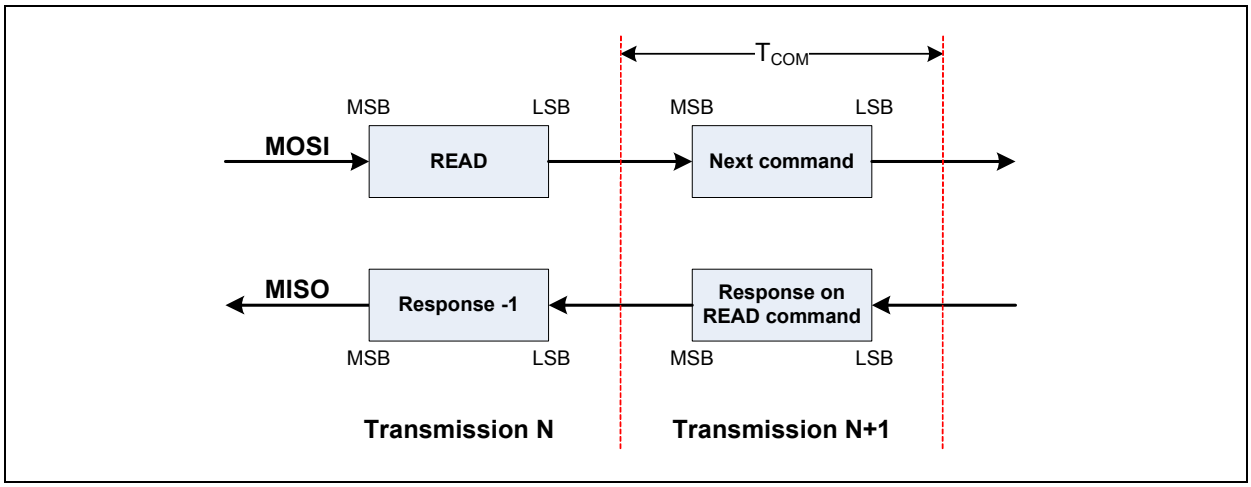
Address hex	Name	Access Type	Bit	Symbol	Default	Description
Readout Registers						
x3FFD	Diagnostics + Automatic Gain Control (AGC)	R	13	Not used	n.a.	Diagnostics flags
			12			
			11	Comp High	0	
			10	Comp Low	0	
			9	COF	0	
			8	OCF	1	
			7	AGC value<7>	1	Automatic Gain Control value. 0 decimal represents high magnetic field 255 decimal represents low magnetic field
			:	:	:	
			0	AGC value<0>	0	
x3FFE	Magnitude	R	13	Magnitude<12>	0	Magnitude information after ATAN calculation
			:	:	:	
			1	Magnitude<0>	0	
			0	Don't Care	0	
x3FFF	Angle	R	13	Angle <12>	0	Angle information after ATAN calculation and zero position adder
			:	:	:	
			1	Angle<0>	0	
			0	Don't Care	0	

SPI Interface Commands

READ Command

For a single *READ* command two transmission sequences are necessary. The first package written to the AS5048L contains the *READ* command **(MSB-1 high)** and the address the chip has to access, the second package transmitted to the AS5048L device can be *any command* the chip has to process next. The content of the desired register is available in the *MISO* register of the *master device* at the end of the second transmission cycle.

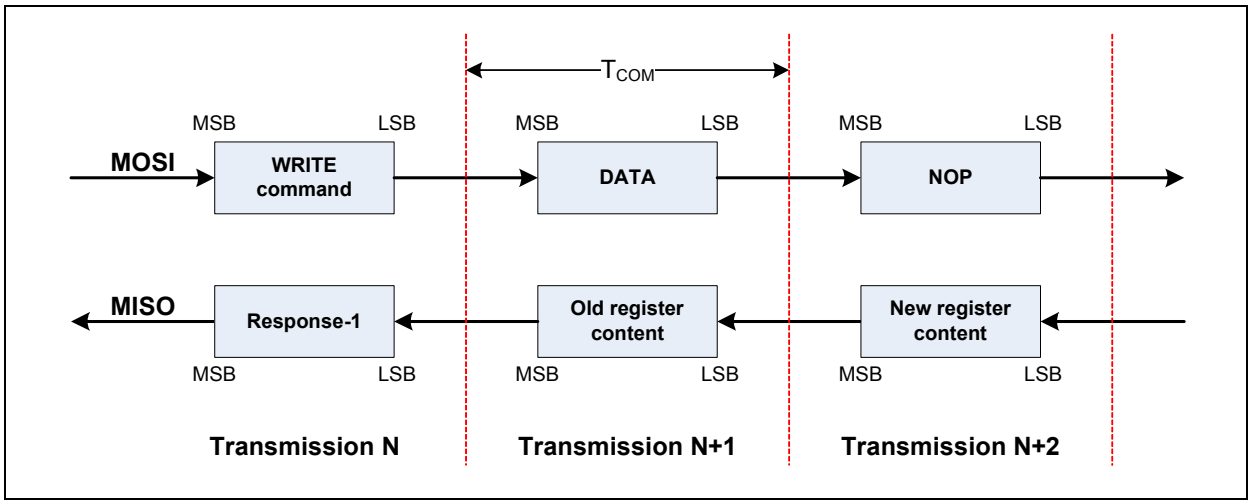
Figure 21:
READ Command



WRITE Command

A single *WRITE* command takes two transmission cycles. With a NOP command after the WRITE command you can verify the sent data with three transmission cycles because the data will be send back during the following command.

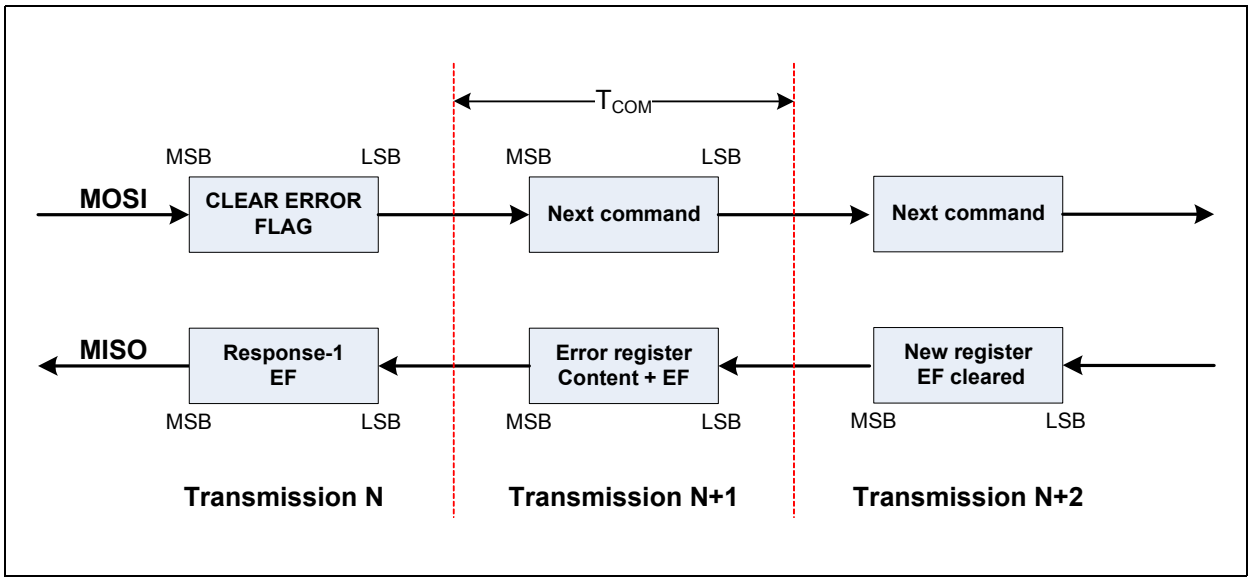
Figure 22:
WRITE Command



CLEAR ERROR FLAG Command

The *CLEAR ERROR FLAG* command is implemented as *READ* command. This command clears the *ERROR FLAG* which is contained in every *READ* frame. Before the *ERROR FLAG* is cleared the error register content comes back with the information which error type was occurred. On the next new *READ* register the *ERROR FLAG* is cleared.

Figure 23:
CLEAR ERROR FLAG Command



The package necessary to perform a *CLEAR ERROR FLAG* is built up as follows.

Figure 24:
CLEAR ERROR FLAG Command Frame

CLEAR ERROR FLAG Command																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	PAR	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Possible conditions which force the ERROR FLAG to be set:

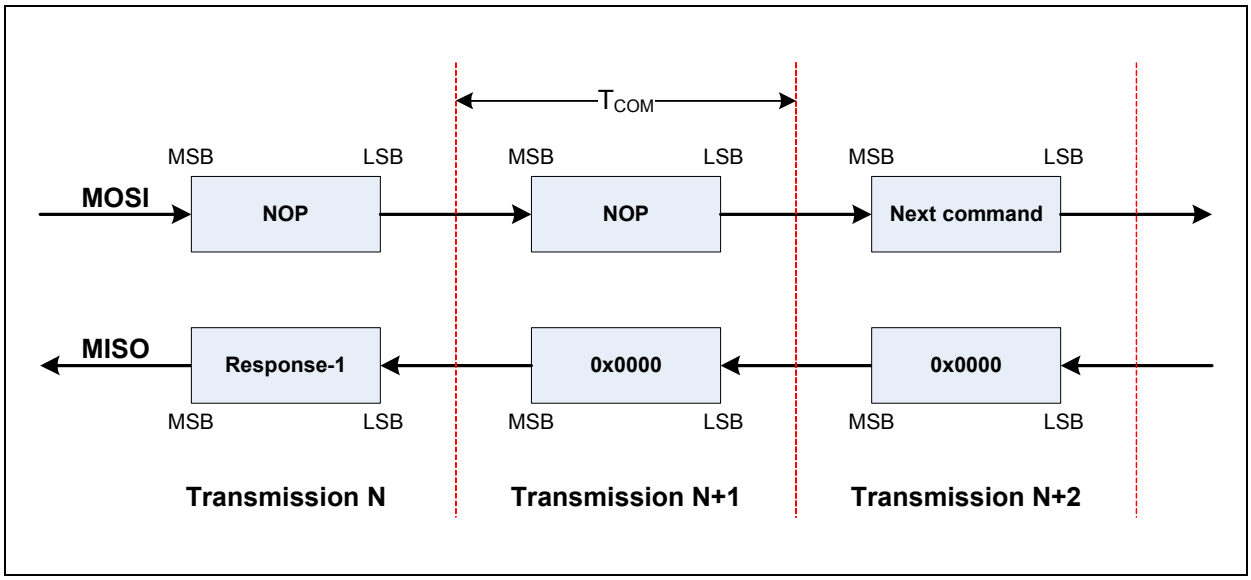
- Wrong parity
- Wrong number of clocks (no full transmission cycle or too many clocks)
- Invalid command
- Frame error

Note(s): If the error flag is set to high because of a communication problem the flag remains set until it will be cleared by the *CLEAR ERROR FLAG* command.

NOP Command

The *NOP* command represents a dummy write to the AS5048L.

Figure 25:
NOP Command



The NOP command frame looks like follows.

Figure 26:
NOP Command Frame

NOP Command																
Bit	**MSB**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**LSB**
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The chip's response on this command is 0x0000

PWM Interface

The AS5048L provides a pulse width modulated output (PWM), whose duty cycle is proportional to the measured angle. The PWM frequency is internally trimmed to an accuracy of ±10% over full temperature range. This tolerance can be cancelled by measuring the complete duty cycle.

The PWM signal consists of different sections:

- Init:
  12 clocks → PWM = 'high'
- Error_n:
  4 clocks → PWM = 'not(system_error)'
- Data:
  4095 clocks → PWM = 'angle_zero' / 'low' (in case of error)
- Exit:
  8 clocks → PWM = 'low'

In case of an error the data section is set to zero.

Figure 27:
PWM Format

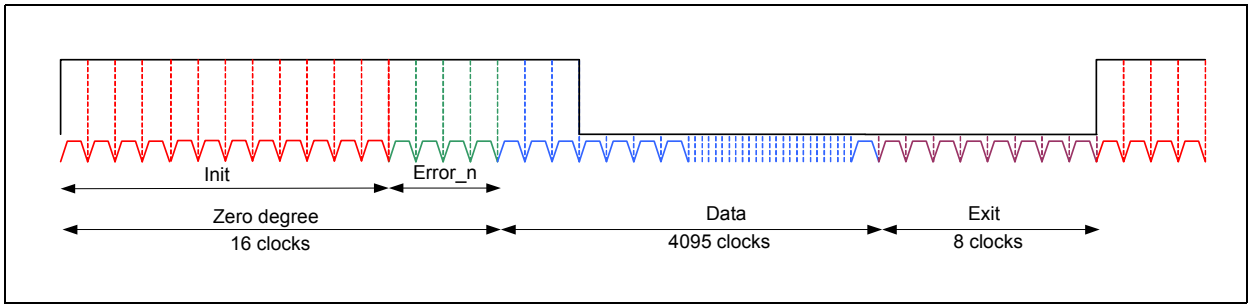


Figure 28:
PWM Period and Resolution

Parameter	Symbol	Value	Unit
PWM Frequency	F_PWM	1	KHz
PWM Pulse period	T_PWM	4119	bit

Application Information

Programming the AS5048L

Programming of the Zero Position: The absolute angle position can be permanent programmed over the interface. This could be useful for random placement of the magnet on the rotation axis. A readout at the mechanical zero position can be performed and written back into the IC. With permanent programming the position is non-reversible stored in the IC. This programming can be performed only once.

To simplify the calculation of the zero position it is only needed to write the value in the IC which was read out before from the angle register.

Programming Sequence with Verification: To program the zero position is needed to perform following sequence:

1. Write 0 into OTP zero position register to clear
2. Read angle information
3. Write previous read angle position into OTP zero position register

Now the zero position is set.
If you want to burn it to the OTP register send:

4. Set the Programming Enable bit in the OTP control register
5. Set the Burn bit to start the automatic programming procedure
6. Read angle information (equals to 0)
7. Set the Verify bit to load the OTP data again into the internal registers
8. Read angle information (equals to 0)

The programming can either be performed in 5V operation using the internal LDO, or in 3V operation but using a minimum supply voltage of 3.3V. In case of 3V operation, also a 10µF capacitor is required on the VDD3 pin.

Diagnostic Functions of the AS5048L

The AS5048L provides diagnostics functions of the IC and also diagnostic functions of the magnetic input field

Following diagnostic flags are available:

See Figure 20 register address x3FFD

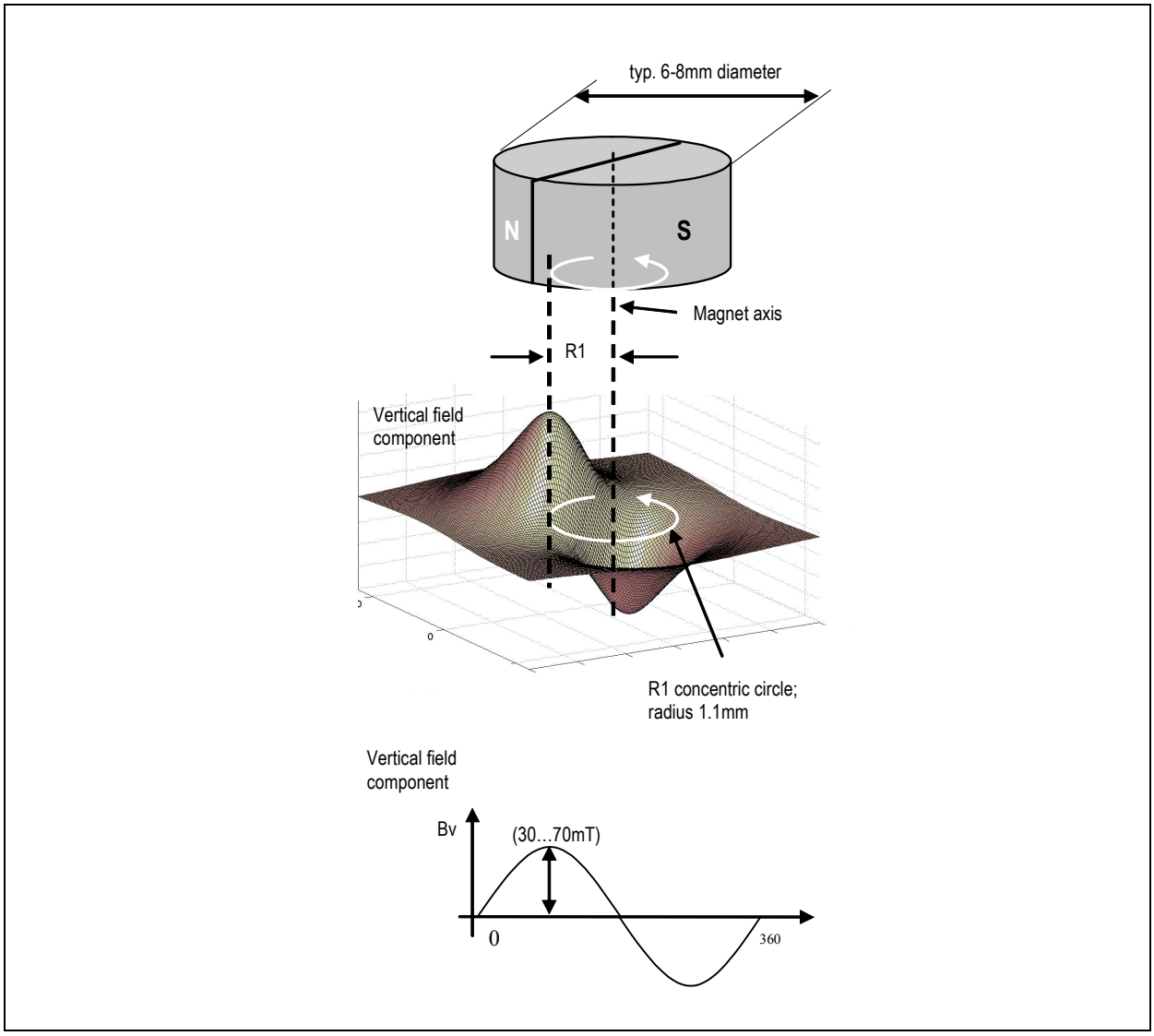
- **OCF** (**O**ffset **C**ompensation **F**inished), logic high indicates the finished Offset Compensation Algorithm. After power up the flag remains always to logic high.
- **COF** (**C**ordic **O**ver**f**low), logic high indicates an out of range error in the CORDIC part. When this bit is set, the angle and magnitude data is invalid. The absolute output maintains the last valid angular value.
- **COMP low**, indicates a high magnetic field. It is recommended to monitor in addition the magnitude value.
- **COMP high**, indicated a weak magnetic field. It is recommended to monitor the magnitude value.

Choosing the Proper Magnet

The AS5048L works with a variety of different magnets in size and shape. A typical magnet could be 6-8 mm in diameter and ≥2.5mm in height The magnetic field strength perpendicular to the die surface has to be in the range of ±30mT … ±70mT (peak).

The magnet's field strength should be verified using a gauss-meter. The magnetic flux B_Z at a given distance, along a concentric circle with a radius of 1.1mm (R1), should be in the range of ±30mT… ±70mT.

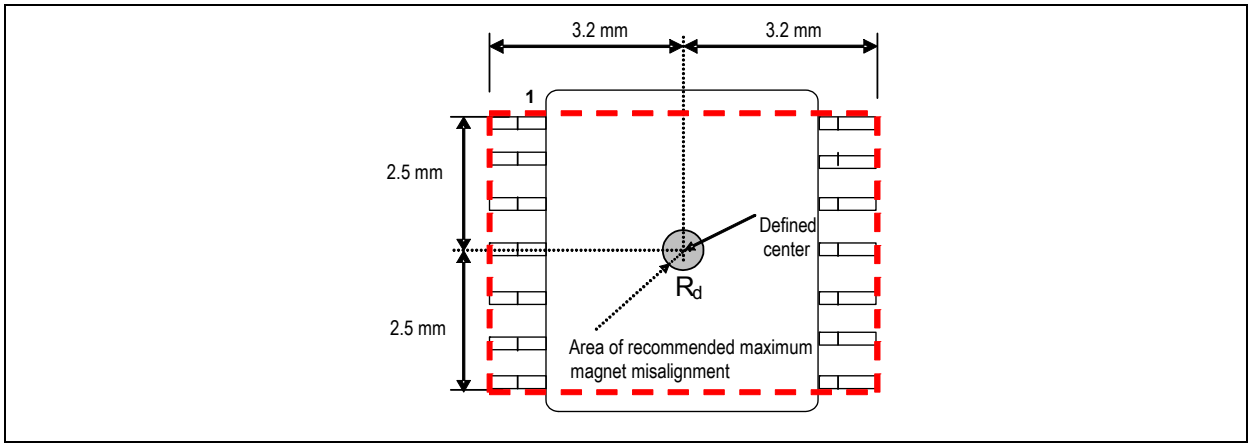
Figure 29:
Typical Magnet and Magnetic Flux Distribution



Physical Placement of the Magnet

The best linearity can be achieved by placing the center of the magnet exactly over the defined center of the chip as shown in the drawing below:

Figure 30:
Defined Chip Center and Magnet Displacement Radius



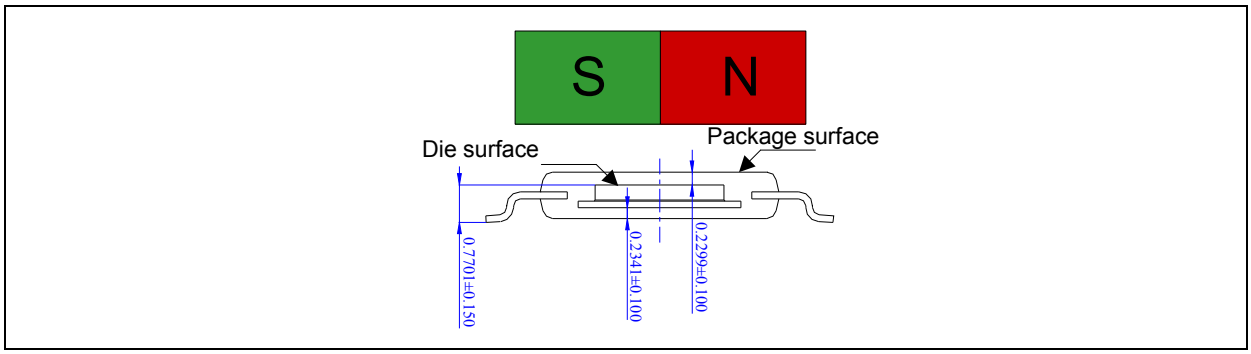
Magnet Placement

The magnet's center axis should be aligned within a displacement radius R_d of 0.25 mm (larger magnets allow more displacement e.g. 0.5 mm) from the defined center of the IC.

The magnet may be placed below or above the device. The distance should be chosen such that the magnetic field on the die surface is within the specified limits The typical distance "z" between the magnet and the package surface is 0.5mm to 2.5mm, provided the use of the recommended magnet material and dimensions (6mm x 3mm). Larger distances are possible, as long as the required magnetic field strength stays within the defined limits.

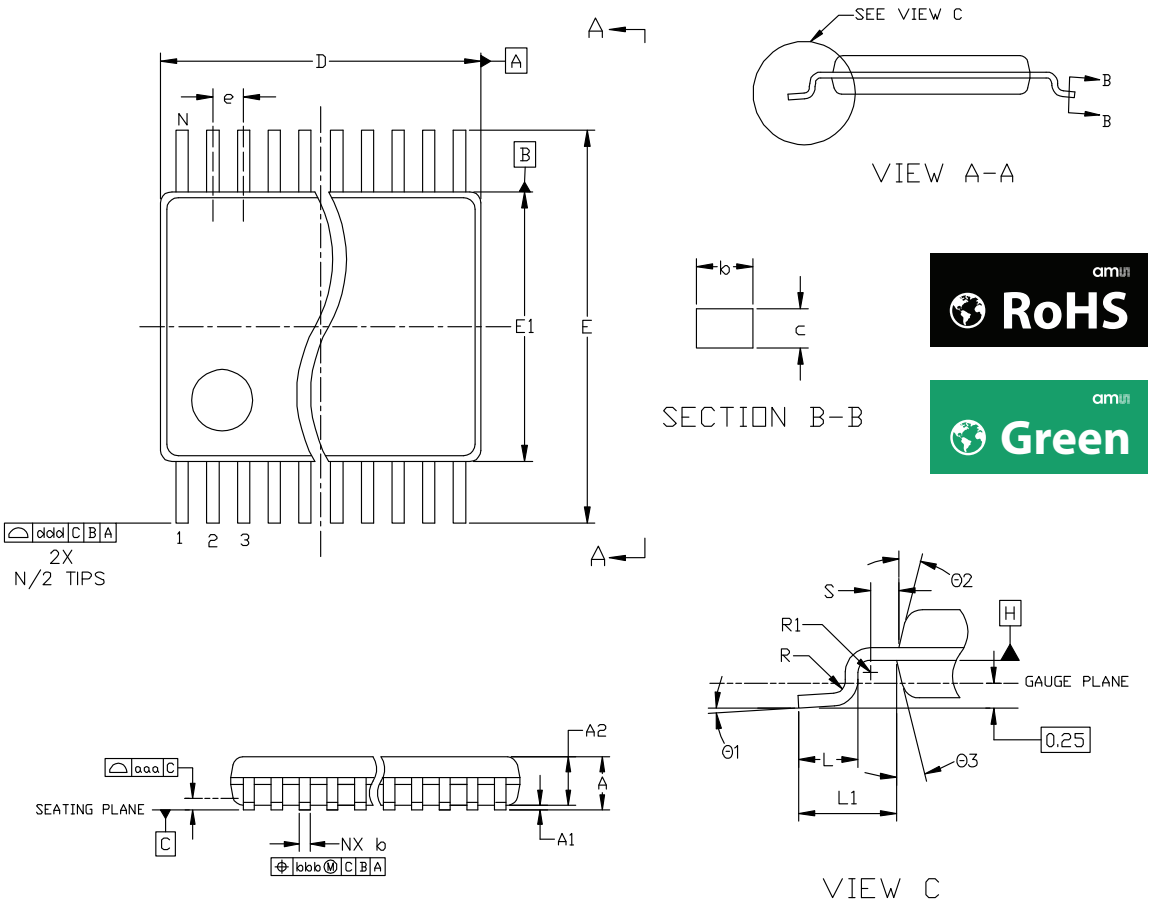
However, a magnetic field outside the specified range may still produce usable results, but the out-of-range condition will be indicated by indication flags.

Figure 31:
Vertical Placement of the Magnet



Package Drawings & Markings

Figure 32:
14-Lead Thin Shrink Small Outline Package TSSOP-14



Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	5.00	5.10
E	-	6.40 BSC	-
E1	4.30	4.40	4.50
e	-	0.65 BSC	-
L	0.45	0.60	0.75
L1	-	1.00 REF	-

Symbol	Min	Nom	Max
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ1	0°	-	8°
θ2	-	12 REF	-
θ3	-	12 REF	-
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.05	-
ddd	-	0.20	-
N		14	

Note(s) and/or Footnote(s):

1. Dimensioning & toleranceing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.

Figure 33:
Package Marking for AS5048L

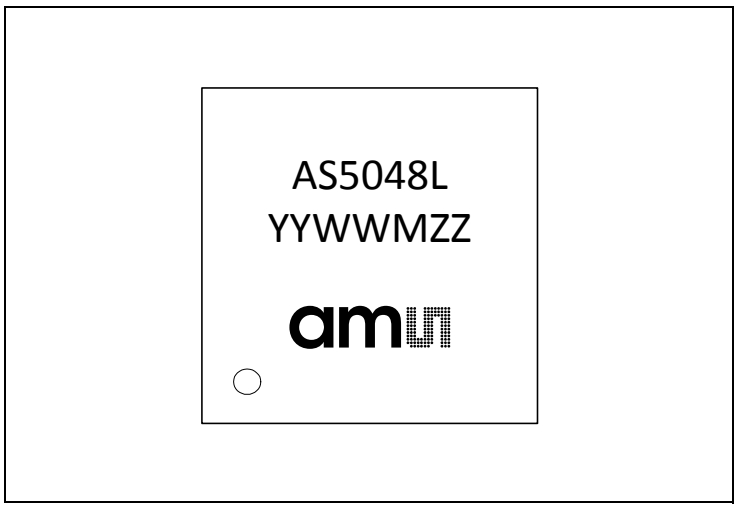


Figure 34:
Package Code YYWWMZZ

YY	WW	M	ZZ
Last two digits of the year	Manufacturing week	Plant identifier	Letters for free traceability

Ordering & Contact Information

Figure 35:
Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS5048L-HTSP	TSSOP-14	AS5048L	13" Tape & Reel in dry pack	4500
AS5048L-HTSM	TSSOP-14	AS5048L	7" Tape & Reel in dry pack	500

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Document Status	Product Status	Definition
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Revision Information

Changes from 1-01 (2015-Mar-04) to current revision 1-02 (2015-May-21)	Page
Updated Figure 35 (Ordering Information)	27

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

Content Guide