EiceDRIVER™ Compact

6EDM2003L06 Family

Integrated 3 Phase Gate Driver

Chip product

Industrial Power Control

Never stop thinking

6EDM2003L06

Revision History:	**2014-11**	Rev. 2.4
Previous Version:	2.3	
p. 15	revised quality disclaimer	

Edition 2014-11

Published by

Infineon Technologies AG

81726 München, Germany

Attention please!

The information given in this data sheet shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Table of Contents:

1 Overview 4
1.1 Features 4
1.2 Product family 4
1.3 Description 4

2 Pin Configuration and Description 5
2.1 Description 7
2.1.1 HIN1,2,3 and LIN1,2,3 (Low side and high side control pins) 7
2.1.2 /FAULT (Fault feedback) 7
2.1.3 ITRIP (Over-current detection function) 7
2.1.4 VCC and VSS (Low side supply) 7
2.1.5 VB1,2,3 and VS1,2,3 (High side supplies) 7
2.1.6 LO1,2,3 and HO1,2,3 (Low and High side outputs) 8

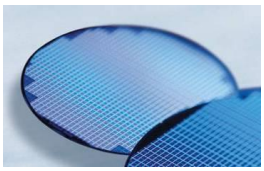
3 Electrical parameters 9
3.1 Absolute Maximum Ratings 9
3.2 Required Operation Conditions 10
3.3 Operating Range 10
3.4 Static Logic function Table 10
3.5 Static Parameters 11
3.6 Dynamic Parameters 14

4 Quality disclaimer 15

5 Timing Diagrams 16

6EDM2003L06 family

3-PHASE BRIDGE DRIVER IGBT/MOS



Chip product

1 Overview

1.1 Features

- Thin-film-SOI-technology
- Insensitivity of the bridge output to negative transient voltages up to -50V given by SOI-technology
- Maximum blocking voltage +600V
- Power supply of the high side drivers via boot strap
- Integrated bootstrap functionality
- Separate control circuits for all six drivers
- CMOS and LSTTL compatible input (positive logic)
- Signal interlocking of every phase to prevent cross-conduction
- Detection of over-current and under-voltage supply
- 'shut down' of all switches during error conditions
- 65µs delay for fault clear after over current detection

1.2 Product family

Table 1: Members of the product family

Sales code	best to use with Infineon chip type
6EDM2003L06-F06	IGC04R60D
6EDM2003L06-F10	IGC05R60D
6EDM2003L06-F15	IGC07R60D
6EDM2003L06-F20	IGC10R60D
6EDM2003L06-F30	SIGC10T60S

1.3 Description

The 6EDM2003L06 family is a full bridge driver family to control power devices like MOSFETs or IGBTs in 3-phase systems with a maximum blocking voltage of +600V. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch up may occur at all temperature and voltage conditions.

The six independent drivers are controlled at the low-side using six different CMOS resp. LSTTL compatible signals, down up to 3.3V logic. The device includes an under-voltage detection unit with hysteresis characteristic (ca 12.1V/10.4V) and an over-current detection. The current switch-off level can be adjusted by connecting a resistor network (Fig.1) at the pin ITRIP. Both error conditions (under-voltage and over-current) lead to a definite shut-down off all six switches. An error signal is provided at the FAULT open drain output pin. The blocking time after over-current is fixed internally by 65us. Because of system safety reasons a 360ns interlocking time has been realized. There is internal bootstrap diode between pins VCC and VBx in order to provide power supply of the high side.

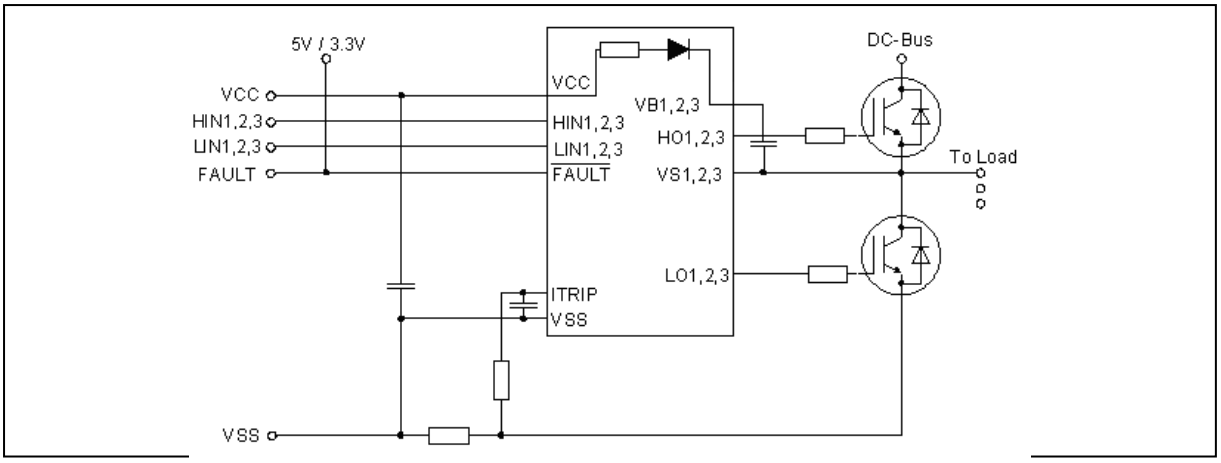


Figure 1: Typical Application

2 Pin Configuration and Description

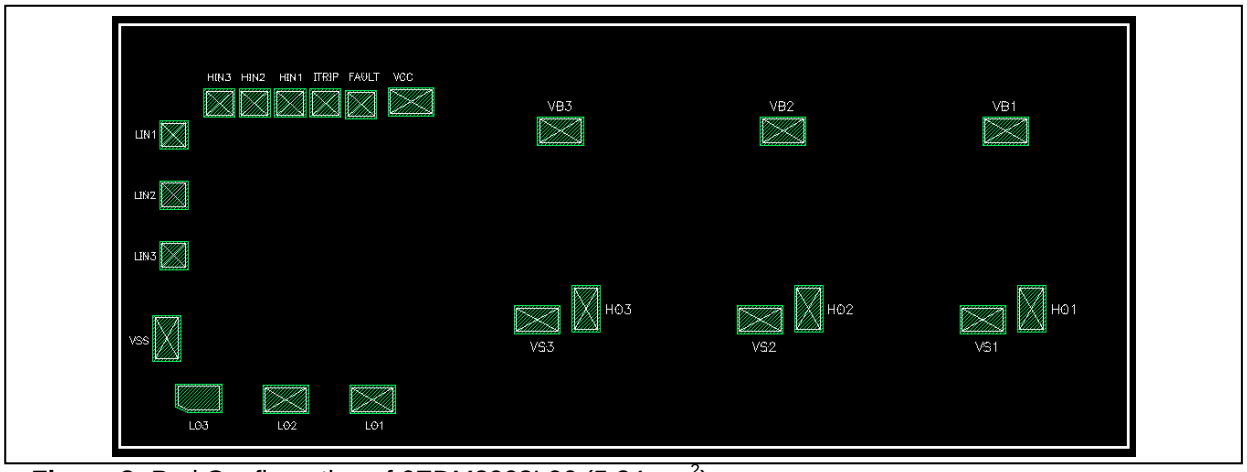


Figure 2: Pad Configuration of 6EDM2003L06 (5.24mm^2)

Table 2: Pad dimensions and positions

		Pad Center		
Pad Name	**Active Pad Dimension (x,y)**	**x**	**y**	**Voltage Domain**
LIN3	80x80	183	649	1
LIN2	80x80	183	854	1
LIN1	80x80	183	1058	1
HIN3	90x80	337	1165	1
HIN2	90x80	457	1165	1
HIN1	90x80	577	1165	1
ITRIP	90x80	697	1165	1
FAULT	90x80	818	1161	1
VCC	140x80	988	1170	1
VB3	140x80	1494	1071	4

VB2	140x80	2249	1071	3
VB1	140x80	3006	1071	2
HO1	80x140	3093	469	2
VS1	140x80	2927	432	2
HO2	80x140	2337	469	3
VS2	140x80	2172	432	3
HO3	80x140	1581	469	4
VS3	140x80	1416	432	4
LO1	140x80	857	160	1
LO2	140x80	562	160	1
LO3	140x80	267	166	1
VSS	80x140	158	368	1

Chip corners (excluding kerf of 72µm x 72µm): bottom left: x=0, y=0;right upper: x=3420, y=1430

Voltage stress between the voltage domains 1,2,3,4 max. 600V.

Voltage stress within each voltage domain max. 20V.

Table 3: Mechanical Parameters

Raster size of die	3492 x 1502	µm x µm
Area total / active	5,24 / 4,89	mm²
Thickness	280	µm
Wafer size	200	mm
Max. possible chips per wafer	5199	pcs
Passivation frontside (Note 1)	Polyimide	
Backside (Note 2)	Grinded silicon	
Reject ink dot diameter	Min. 0.6 max 1.2	mm

Note 1: Filler material inside the mould compound with sharp edges may harm the passivation.
Note 2: Chip must be bonded onto an isolated area

Table 4: Pad Description

Symbol	Description
VCC	Low side positive power supply
VSS	Low side negative power supply
HIN1,2,3	High side logic input (positive logic)
LIN1,2,3	Low side logic input (positive logic)
/FAULT	Indicates over-current and under-voltage (negative logic, open-drain output)
ITRIP	Analog input for over-current shutdown, activates FAULT and RCIN to VSS
VB1,2,3	High side positive power supply
HO1,2,3	High side gate driver output
VS1,2,3	High side negative power supply
LO1,2,3	Low side gate driver output

2.1 Description

2.1.1 HIN1,2,3 and LIN1,2,3 (Low side and high side control pins)

These pins are active high and they are responsible for HO1,2,3 and LO1,2,3 out-of-phase commutation. The schmitt-trigger input threshold of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs.

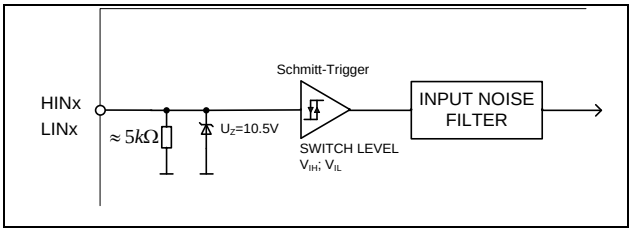


Figure 3: Input pin structure

An internal pull-down resistor of about 5 kΩ is pre-biases the input during supply start-up. Input schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses according to Figure 4.

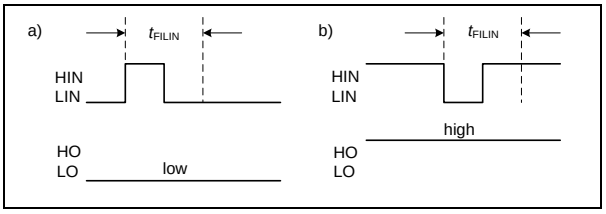


Figure 4: Input filter timing diagram

It is anyway recommended for proper work of the driver not to provide input pulse-width lower than 1us.

It provides additionally an anti-shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3). When two inputs of a same leg are activated, only one leg output is activated, so that the leg is kept steadily in a safe state.

A dead-time insertion of typ. 360ns is also provided, in order to reduce cross-conduction of the external power switches.

2.1.2 /FAULT (Fault feedback)

/Fault pin is an active low open-drain output indicating the status of the gate driver (see Figure 5). The pin is active (i.e. forces LOW voltage level) when one of the following conditions occur:

- Under-voltage condition of VCC supply: In this case the fault condition is released as soon as the supply voltage condition returns in the normal operation range (please refer to VCC pin description for more details).
- Over-current detection (ITRIP): The fault condition is latched until current trip condition is finished.

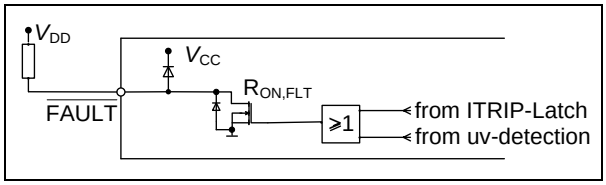


Figure 5: /Fault pin structure

2.1.3 ITRIP (Over-current detection function)

It provides an over-current detection function by connecting the ITRIP input with the motor current feedback. The ITRIP comparator threshold (typ. 0.47V) is referenced to VSS ground. A input noise filter (typ.: $t_{ITRIPMIN}$ = 530ns) prevents the driver to detect false over-current events.

Over-current detection generates a hard shut down of all outputs of the gate driver and provides a latched fault feedback at /FAULT pin.

The blocking time after over-current is fixed internally by 65us typically.

2.1.4 VCC and VSS (Low side supply)

VCC is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground as well as the under-voltage detection circuit and output power stage.

The under-voltage circuit enables the device to operate at power on when a typical supply voltage V_{CCUV+} = 12.1 V is present.

The IC shuts down all the gate drivers power outputs, when the VCC supply voltage is below V_{CCUV-} = 10.4 V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

2.1.5 VB1,2,3 and VS1,2,3 (High side supplies)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter/source voltage.

The integrated bootstrap diode structures supply sufficiently the individual high side section due to the low power consumption. However, additional external bootstrap circuits are possible

Under-voltage detection operates with a rising supply threshold of typical V_{BSUV+} = 12.1 V and a falling threshold of V_{CCUV-} = 10.4 V. Please refer to Figure 9 of the datasheet for device operating area as a function of the supply voltage.

2.1.6 LO1,2,3 and HO1,2,3 (Low and High side outputs)

Low side and high side power outputs are specifically designed for pulse operation such as gate drive of IGBT and MOSFET devices. Low side outputs (i.e. LO1,2,3) are state triggered by the respective inputs (LIN1,2,3), while high side outputs (i.e. HO1,2,3) are edge triggered by the respective inputs (HIN1,2,3).

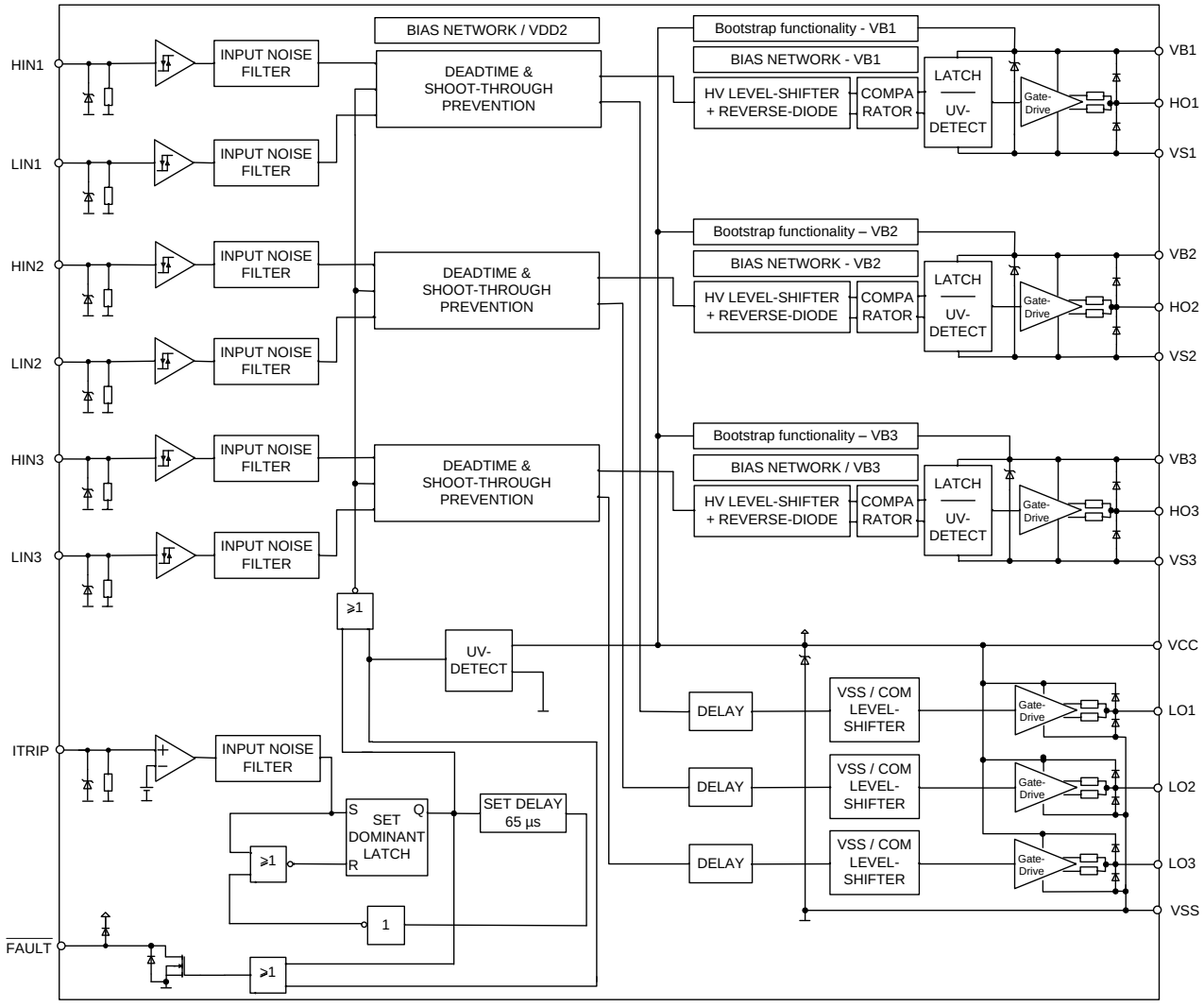


Figure 6: Block diagram

3 Electrical parameters

3.1 Absolute Maximum Ratings

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. (T_A=25°C)

Symbol	Definition	Min.	Max.	Unit
V_S	High side offset voltage (Note 1)	-	600	V
	High side offset voltage (t_p<500ns, Note 1)	V_{CC} -V_{BS} - 50	-	
V_B	High side offset voltage (Note 1)	V_{CC} - 6	620	
	High side offset voltage (t_p<500ns, Note 1)	V_{CC} - 50	-	
V_{BS}	High side floating supply voltage (V_B vs. V_S)	-1	20	
V_{HO}	High side output voltage (V_{HO} vs. V_S)	-0.5	V_B + 0.5	
V_{CC}	Low side supply voltage (internally clamped)	-1	20	
V_{LO}	Low side output voltage	-0.5	V_{CC} +0.5	
V_{IN}	Input voltage LIN,HIN,ITRIP	-1.0	10	
V_{FLT}	FAULT output voltage	-0.5	V_{CC} + 0.5	
P_D	Total power dissipation (to package) Note 2	-	1.0	W
R_{thJA}	Thermal resistance (junction to ambient) Note 3	-	60	K/W
T_J	Junction temperature	-	125	°C
T_S	Storage temperature	-40	150	
d*Vs*/dt	offset voltage slew rate		50	V/ns

Note :The minimal value for ESD immunity is 1.0kV (Human Body Model). ESD immunity inside pins connected to the low side (VCC, HINx, LINx, FAULT, ITRIP, VSS, LOx) and pins connected inside each high side itself (VBx, HOx, VSx) is guaranteed up to 1.5kV (Human Body Model).

Note 1 : Insensitivity of bridge output to negative transient voltage up to –50V is not subject to production test – verified by design / characterization. Please consider the total power dissipation at internal bootstrap diode in case VCC-VB>0.8V.

Note 2: Consistent power dissipation of all outputs. Total power dissipation depends on mounting conditions.

Note 3: The thermal resistance can is dependent on the mounting technology. It is in the responsibility of the customer to verify and to guarantee proper conditions.

3.2 Required Operation Conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. (T_A=25°C)

Symbol	Definition	Min.	Max.	Unit
V_B	High side offset voltage (Note 1)	11.1	620	V
V_{CC}	Low side supply voltage	10	20	

Note 1 : Logic operational for V_B (V_B vs. V_{SS}) > 11,1V

3.3 Operating Range

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. (T_A=25°C)

Symbol	Definition	Min.	Max.	Unit
V_S	High side floating supply offset voltage	V_{CC} -V_{BS}-0.5	550	V
V_{BCC}	High side floating supply offset voltage (V_B vs. V_{CC}, statically, Note 1, Note 2)	-0.5	550	
V_{BS}	High side floating supply voltage (V_B vs. V_S)	13	17.5	
V_{HO}	High side output voltage (V_{HO} vs. V_S)	0	V_{BS}	
V_{LO}	Low side output voltage	0	17.5	
V_{CC}	Low side supply voltage	13	17.5	
V_{IN}	Logic input voltages LIN,HIN,ITRIP	0	5	
V_{FLT}	FAULT output voltage	0	V_{CC}	
t_{IN}	Pulse width for ON or OFF (Note 3)	1	-	µs
T_A	Ambient temperature	-40	95	°C

Note 2 : All input pins (HINx, LINx) and ITRIP pin are internally clamped with a 10.5V zener diode.

Note 3 : In case of input pulse width at LINx and HINx below 1µs the input pulse can not be transmitted properly

3.4 Static Logic function Table

VCC	VBS	ITRIP	FAULT	LO1,2,3	HO1,2,3
<V_{CCUV-}	X	X	0	0	0
15V	<V_{BSUV-}	0V	High imp	LIN1,2,3	0
15V	15V	> $V_{IT,TH+}$	0	0	0
15V	15V	0V	High imp	LIN1,2,3	HIN1,2,3

3.5 Static Parameters

V_{CC} = V_{BS} = 15V unless otherwise specified. (T_A=25°C)

Symbol	Definition	Min.	Typ.	Max.	Unit	Test Conditions
V_{IH}	Logic "1" input voltage (LIN,HIN)	1.7	2.1	2.4	V	
V_{IL}	Logic "0" input voltage (LIN,HIN)	0.7	0.85	1.1		
$V_{IT,TH+}$	ITRIP positive going threshold	390	470	550	mV	
$V_{IT,HYS}$	ITRIP input hysteresis	45	70			
V_{OH}	Output voltage (high level, V_{CC}-V_O or V_{BS}-V_O)				V	I_O = 20mA
	6EDM2003L06-F30		1.4	2.1		
	6EDM2003L06-F20	-	0.78	1.3		
	6EDM2003L06-F15	-	1.08	1.66		
	6EDM2003L06-F10	-	2.00	2.80		
	6EDM2003L06-F06	-	3.30	4.45		
V_{OL}	Output voltage (low level, VO-Vss or VO-VS)					I_O = -20mA
	6EDM2003L06-F30	-	0.24	0.38		
	6EDM2003L06-F20	-	0.3	0.48		
	6EDM2003L06-F15	-	0.4	0.6		
	6EDM2003L06-F10	-	0.5	0.72		
	6EDM2003L06-F06	-	0.77	1.05		
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply under-voltage positive going threshold	11.0	12.1	12.8		
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply under-voltage negative going threshold	9.5	10.4	11.0		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply under-voltage lockout hysteresis	1.2	1.7	-		
I_{LVS+}	High side leakage current betw. VS and VSS	-	0.5	5	µA	T_j=25°C,V_S = 600V
I_{LVS+}[1]	High side leakage current betw. VS and VSS	-	10	-	µA	T_j=125°C,V_S = 600V
I_{LVS-}[1]	High side leakage current between VSx and VSy (x=1,2,3 and y=1,2,3)	-	10	-		T_j=125°C V_{Sx} - V_{Sy} =600V
I_{QBS1}	Quiescent V_{BS} supply current (VB only)	-	300	500		HO=low
I_{QBS2}	Quiescent V_{BS} supply current (VB only)	-	360	550		HO=high
I_{QCC1}	Quiescent V_{CC} supply current (VCC only)	-	0.37	0.8	mA	V_{Bx}=50V, V_{LIN}/V_{HIN} =float.
I_{QCC2}	Quiescent V_{CC} supply current (VCC only)	-	0.33	0.8	mA	V_{Bx}=50V, V_{LIN}=0V, V_{HIN}=5V
I_{QCC3}	Quiescent V_{CC} supply current (VCC only)	-	0.52	1.0	mA	V_{Bx}=50V, V_{LIN}=5V, V_{HIN}=0V

[1] Parameter is not subject to production test – verified by design / characterization

Symbol	Definition	Min.	Typ.	Max.	Unit	Test Conditions
I_{LIN+}	Input bias current	-	0.92	1.3	mA	V_{LIN}=5V
I_{LIN-}	Input bias current	-	2	-	µA	V_{LIN}=0V
I_{HIN+}	Input bias current	-	0.92	1.3	mA	V_{HIN}=5V
I_{HIN-}	Input bias current	-	2	-	µA	V_{HIN}=0V
I_{ITRIP+}	Input bias current (ITRIP=high)		65	120	µA	V_{ITRIP}=5V
I_{O+}	Mean output current for load capacity charging in range from 3V(20%) to 6V(40%)				mA	C_L=10nF
	6EDM2003L06-F30	75	120	-		
	6EDM2003L06-F20	109	180	-		
	6EDM2003L06-F15	96	148	-		
	6EDM2003L06-F10	63	89	-		
	6EDM2003L06-F06	40	53	-		
I_{O-}	Mean output current for load capacity discharging in range from 12V(80%) to 9V(60%)				mA	C_L=10nF
	6EDM2003L06-F30	250	365	-		
	6EDM2003L06-F20	245	360	-		
	6EDM2003L06-F15	240	330	-		
	6EDM2003L06-F10	235	300	-		
	6EDM2003L06-F06	175	245	-		
$R_{ON,FLT}$	FAULT low on resistance of the pull down transistors	-	50	90	Ω	V_{FAULT}=0.5V
R_{G_ON}[1]	Additional on gate resistance of output				Ω	
	6EDM2003L06-F30	-	45	-		
	6EDM2003L06-F20	-	15	-		
	6EDM2003L06-F15	-	30	-		
	6EDM2003L06-F10	-	80	-		
	6EDM2003L06-F06	-	150	-		
R_{G_OFF}[1]	Additional off gate resistance of output				Ω	
	6EDM2003L06-F30	-	1.4	-		
	6EDM2003L06-F20	-	5	-		
	6EDM2003L06-F15	-	10	-		
	6EDM2003L06-F10	-	15	-		
	6EDM2003L06-F06	-	30	-		

[1] Parameter is not subject to production test – verified by design / characterization

Symbol	Definition	Min.	Typ.	Max.	Unit	Test Conditions
V_{F_BSD}	Bootstrap diode forward voltage between VCC and VB	-	1.0	1.3	V	I_F=0.5mA
$I_{F\_BSD\_1}$	Bootstrap diode forward current between VCC and VB	30	55	80	mA	V_F=4V
$I_{F\_BSD\_2}$	Bootstrap diode forward current between VCC and VB	50	82	120	mA	V_F=5V
R_{BSD}	Bootstrap diode resistance between V_F=4V and V_F=5V	22	36	50	Ω	V_{F1}=4V, V_{F2}=5V

3.6 Dynamic Parameters

V_{CC} = V_{BS} =15V, V_S = V_{SS} , unless otherwise specified. (T_A=25°C)

Symbol	Definition	Min.	Typ.	Max.	Unit	Test Condition
t_{on}	Turn-on propagation delay	400	555	800	ns	$V_{LIN/HIN}$=5V
t_{off}	Turn-off propagation delay	400	560	800		$V_{LIN/HIN}$=0V
t_r	Turn-on rise time (CL=1nF)					$V_{LIN/HIN}$=5V
	6EDM2003L06-F30	-	105	160		
	6EDM2003L06-F20	-	64	106		
	6EDM2003L06-F15	-	83	127		
	6EDM2003L06-F10	-	150	200		
	6EDM2003L06-F06	-	240	330		
t_f	Turn-off fall time (CL=1nF)					$V_{LIN/HIN}$=0V
	6EDM2003L06-F30	-	24	40		
	6EDM2003L06-F20	-	31	45		
	6EDM2003L06-F15	-	36	50		
	6EDM2003L06-F10	-	43	54		
	6EDM2003L06-F06	-	58	77		
t_{ITRIP}	Shutdown propagation delay ITRIP	650	1000	1400		V_{ITRIP}=2V
$t_{ITRIPMIN}$	Input filter time ITRIP	270	530	780		
t_{FLT}	Propagation delay ITRIP to FAULT	-	730	1000		
t_{FILIN}	Input filter time at LIN, HIN for turn on and off	140	290	-	ns	$V_{LIN/HIN}$=0V&5V
t_{FLTCLR}	Fault clear time after ITRIP-fault	40	65	100	µs	$V_{LIN/HIN}$ = 0 & 5V
DT	Dead time	200	360	-	ns	V_{ITRIP}=0V, $V_{LIN/HIN}$ = 0 & 5V
MT_{ON}	Matching delay ON, max(ton)-min(ton), ton are applicable to all 6 driver outputs	-	20	100		external dead time->500ns
MT_{OFF}	Matching delay OFF, max(toff)-min(toff), toff are applicable to all 6 driver outputs	-	20	100		external dead time->500ns
PM	Output pulse width matching. PW_{in}-PW_{out}		20	150		PW_{in}>1µs

4 Quality disclaimer

The described properties and parameters must be confirmed by specific qualification in the final system. The results of the qualification must be open to Infineon. Otherwise Infineon does not give any design release or warranty.

We recommend to avoid in particular:

- during die separation - unwanted mechanical stress on the wafer, wear out of the cutting blade or any other cutter misconfiguration possibly causing cracks, chipping and/or delamination of the passivation;

- during/after die attachment – die attach delamination causing possibly unwanted high thermal resistance, unwanted mechanical stress, or reduced electrical conductivity;

- during/after die attachment – die attach voids causing possibly unwanted high thermal resistance, unwanted mechanical stress, or reduced electrical conductivity;

- during/after die attachment – unwanted ion migration possibly causing unwanted leakage or electrical modification of the device;

- during/after die attachment – unwanted ion migration causing possibly unwanted leakage or unwanted electrical modification of the device;

- during/after die attachment – unwanted increase of thermal conductivity possibly causing unwanted overheating of the device;

- during electrical interconnect, in particular wire bonding – mechanical overstress possibly causing sheared wires and/or damaged pads;

- during electrical interconnect, in particular wire bonding – lacking bond integrity, in particular non sticking interconnects on pads possibly causing unwanted misfunction of the device and/or unwanted leakages;

- during encapsulation of the device – unwanted shrink or extension of the mould compound possibly causing corrosion;

- during encapsulation of the device – unwanted ion migration causing unwanted leakage or unwanted electrical modification of the device;

- during encapsulation of the device – unsuitable mould, unsuitable moulding processes possibly causing potentially wire sweep of electrical interconnects;

- during encapsulation of the device – sharp moudl filler components possibly causing penetration of the passivation, hence unwanted environmental influences like corrosion or ion migration etc.

- during encapsulation of the device – unsuitable mould with unsuitable thermal conductivity possibly causing overheating of the device, resulting in damage of single or multiple transistors/diodes causing non functionality of the device, uncluding unwanted leakages;

- during encapsulation of the device – unwanted low creepage distances, possibly bringing about the risk of high voltage avalanche breakthroughs;

- during encapsulation of the device – unsuitable mould and/or mouldling processes possibly causing delamination, resulting in overheating, leackages, shorts, open accessible voltage carrying parts, shortend lifetime etc.

- during encapsulation of the device – unsuitable thermal behaviour of encapsulation (expansion/shrinking, state change) possibly resulting in overheating, sheared wire, openly accessible voltage carrying parts.

5 Timing Diagrams

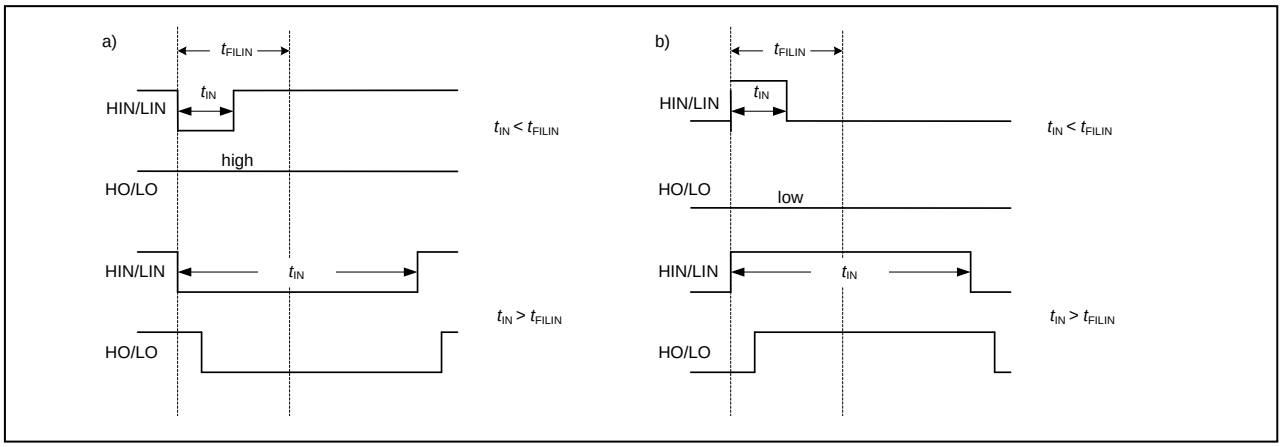


Figure 7: Timing of short pulse suppression

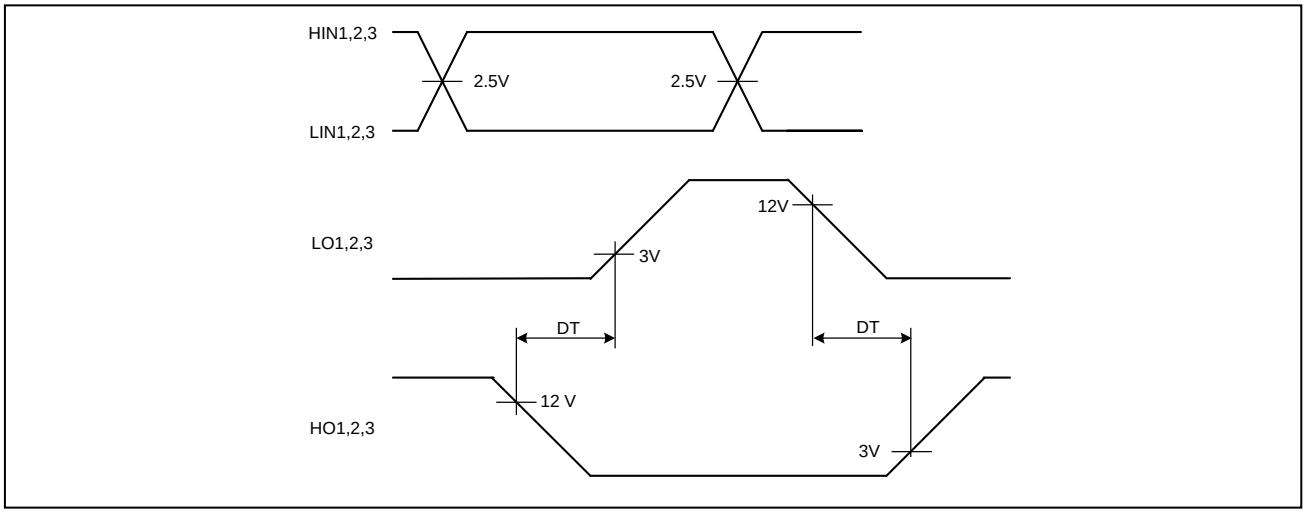


Figure 8: Timing of internal dead time

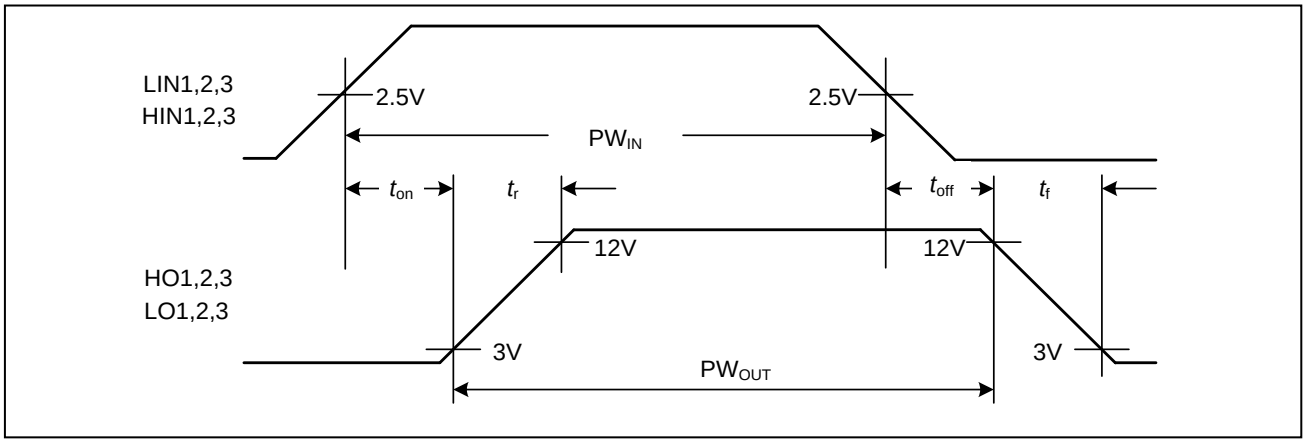


Figure 9: Input to output propagation delay times and switching times definition

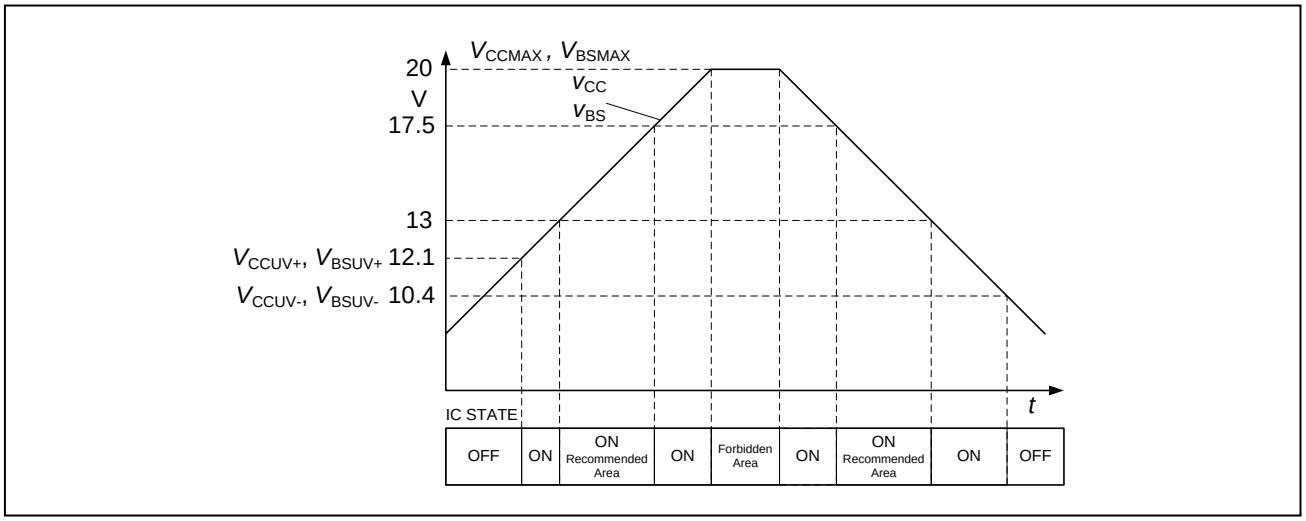


Figure 10: Operating Areas

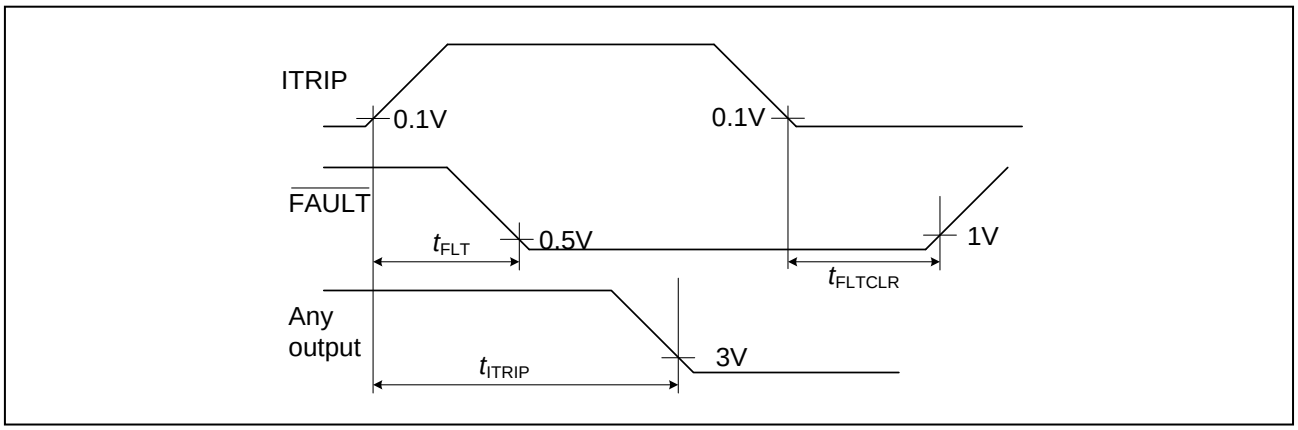


Figure 11: ITRIP-timing, fault clear and /FAULT-timing

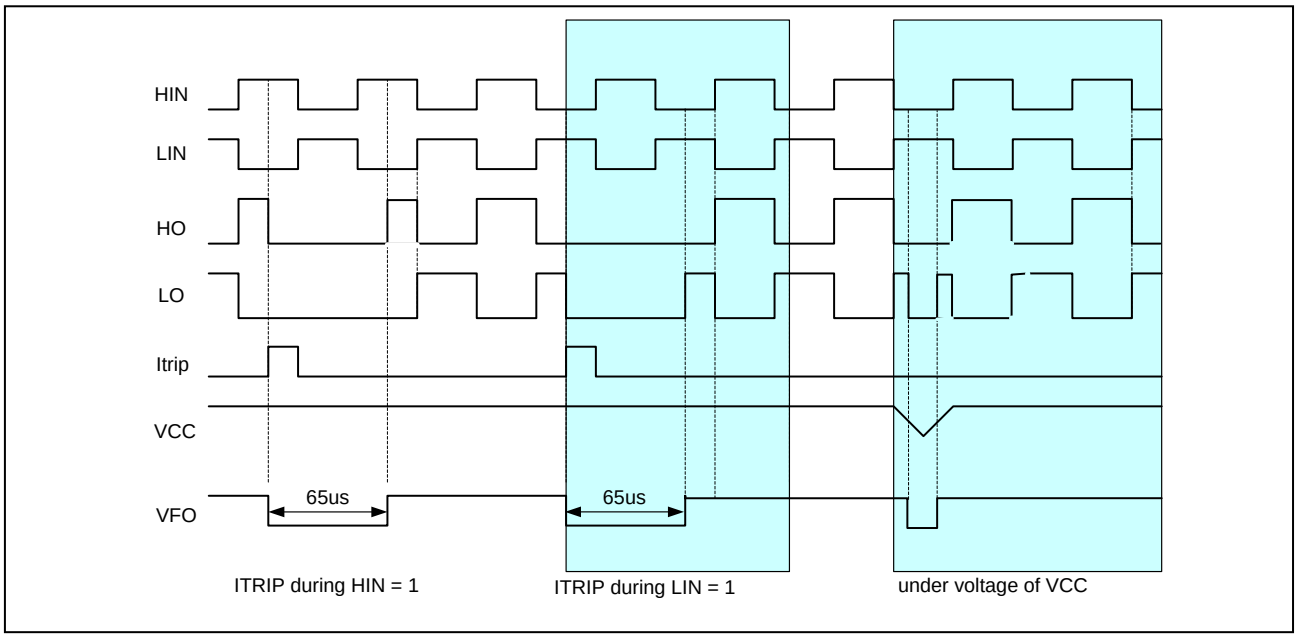


Figure 12: Protective timing chart