6ED2230S12C

1200 V Three Phase Gate Driver with Integrated Bootstrap Diode and OCP

Features

- Infineon Thin-Film-SOI technology
- Fully operational to +1200 V
- Integrated Ultra-fast Bootstrap Diode
- Floating channel designed for bootstrap operation Output source/sink current capability +0.35 A / -0.65 A
- Tolerant to negative transient voltage up to -100 V
    - (Pulse width is up to 700 ns) given by SOI-technology
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V input logic compatible
- Over current protection with ±5% ITRIP threshold
- Fault reporting, automatic Fault clear and Enable function on the same pin (RFE)
- Matched propagation delay for all channels
- Integrated 460 ns deadtime protection
- Shoot-through (cross-conduction) protection

Product summary

V_{OFFSET}	≤ 1200 V
V_{CC}	= 13 V - 20 V
$I_{O+/-}$ (typ.)	= 0.35 A/0.65 A
$t_{on/off}$ (typ.)	= 700 ns/650 ns
Deadtime (typ.)	= 460 ns

Package

Bare die

RoHS

Potential applications

- Motor Control, Pumps, Fans
- Air Conditioning

Product validation

Ready for validation in industrial applications according to the relevant tests of IEC 60747 and 60749 or alternatively JEDEC JESD47, JESD22 and J-STD-020.

Description

The 6ED2230S12C is a high voltage, high speed power MOSFET and IGBT with three independent high side and low side referenced output channels for three phase applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or TTL outputs, down to 3.3 V logic. An over-current protection (OCP) function which terminates all six outputs can also be derived from this resistor. An open drain FAULT signal is provided to indicate that an over-current or undervoltage shutdown has occurred. Fault conditions are cleared automatically after a delay programmed externally via an RC network. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 1200 V. Propagation delays are matched to simplify the HVIC's use in high frequency applications.

(Refer to Lead Assignments for correct pin configuration). This diagram shows electrical connections only. Please refer to Application Notes & Design Tips for proper circuit board layout.

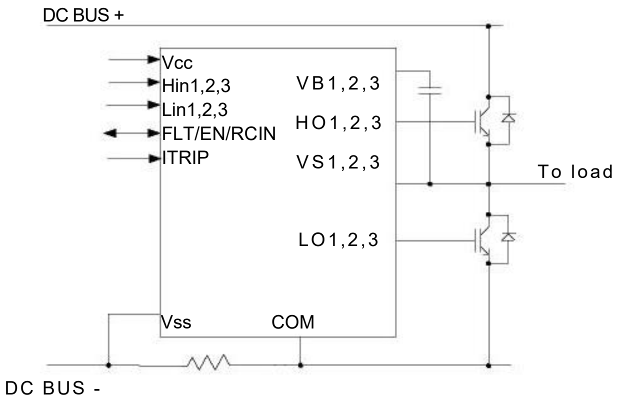

Figure 1 Typical connection diagram

Base part number	Package type	Form	Minimum package quantity *	Orderable part number
6ED2230S12C (1)	Horizontal Frame Shipper	Wafer on film	13230	6ED2230S12CX7SA1

*minimum order quantity equivalent to 5 wafers.

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[1] Also available as 6ED2230S12T in DSO-24 package (DSO-28 without 4 pins). Please contact Infineon for more information.

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1 Block diagram

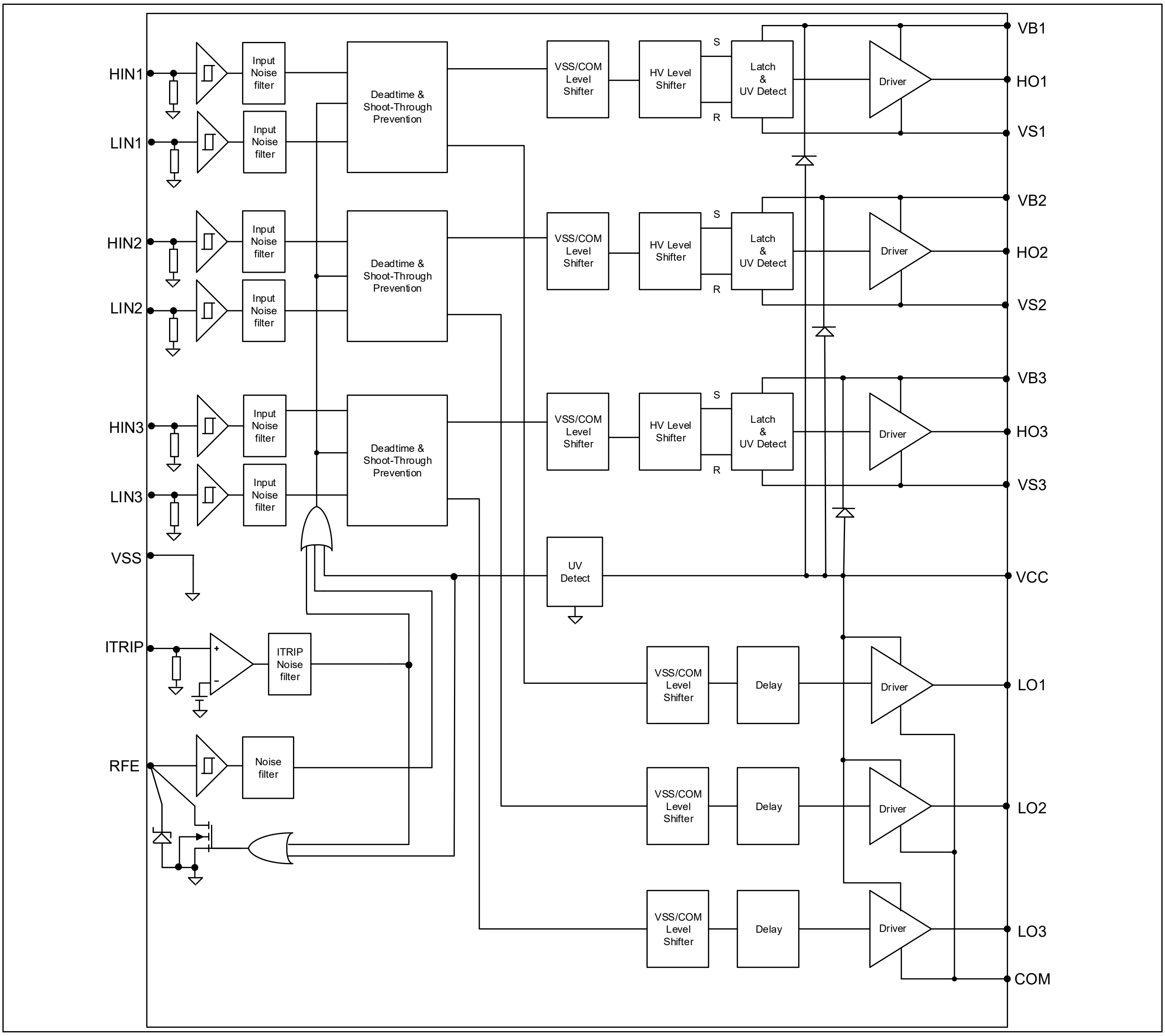


Figure 2 **Functional block diagram**

2 Pad definition and assignment

Table 1 Pad Definitions

Symbol	Description
HIN1,2,3	Logic input for high side gate driver output (HO), in phase
LIN1,2,3	Logic input for low side gate driver output (LO), in phase
$V_{B1,2,3}$	High side floating supply
HO1,2,3	High side gate drive output
$V_{S1,2,3}$	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return
V_{SS}	Logic ground
ITRIP	Analog input for over-current shutdown. When active, ITRIP shuts down outputs and activates RFE low. When ITRIP becomes inactive, RFE stays active low for an externally set time t_{FLTCLR}, then automatically becomes inactive (open-drain high impedance).
RFE	Integrated fault reporting function like over-current (ITRIP), or low-side undervoltage lockout and the fault clear timer. This pin has negative logic and an open-drain output. The use of over-current protection requires the use of external components.

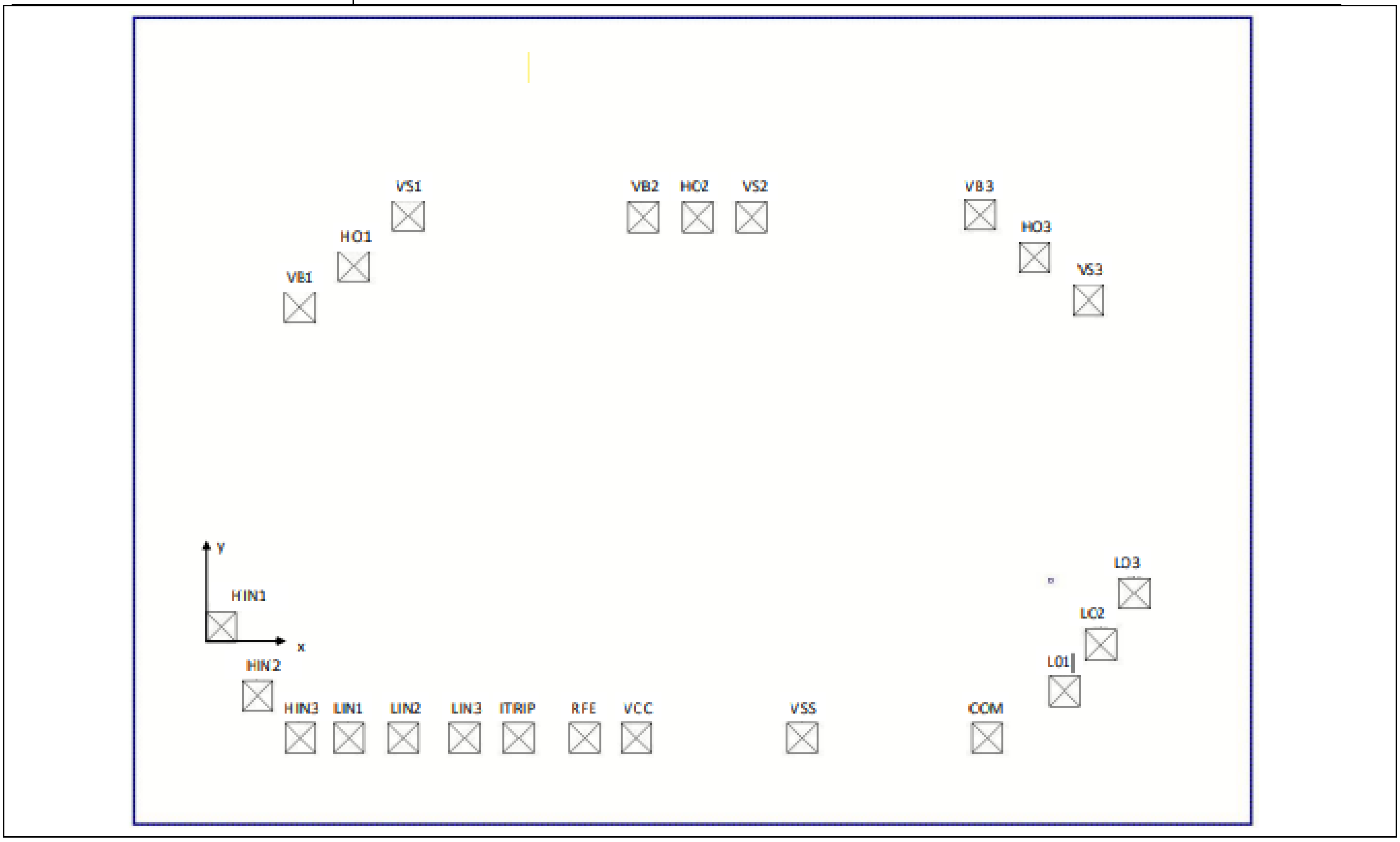
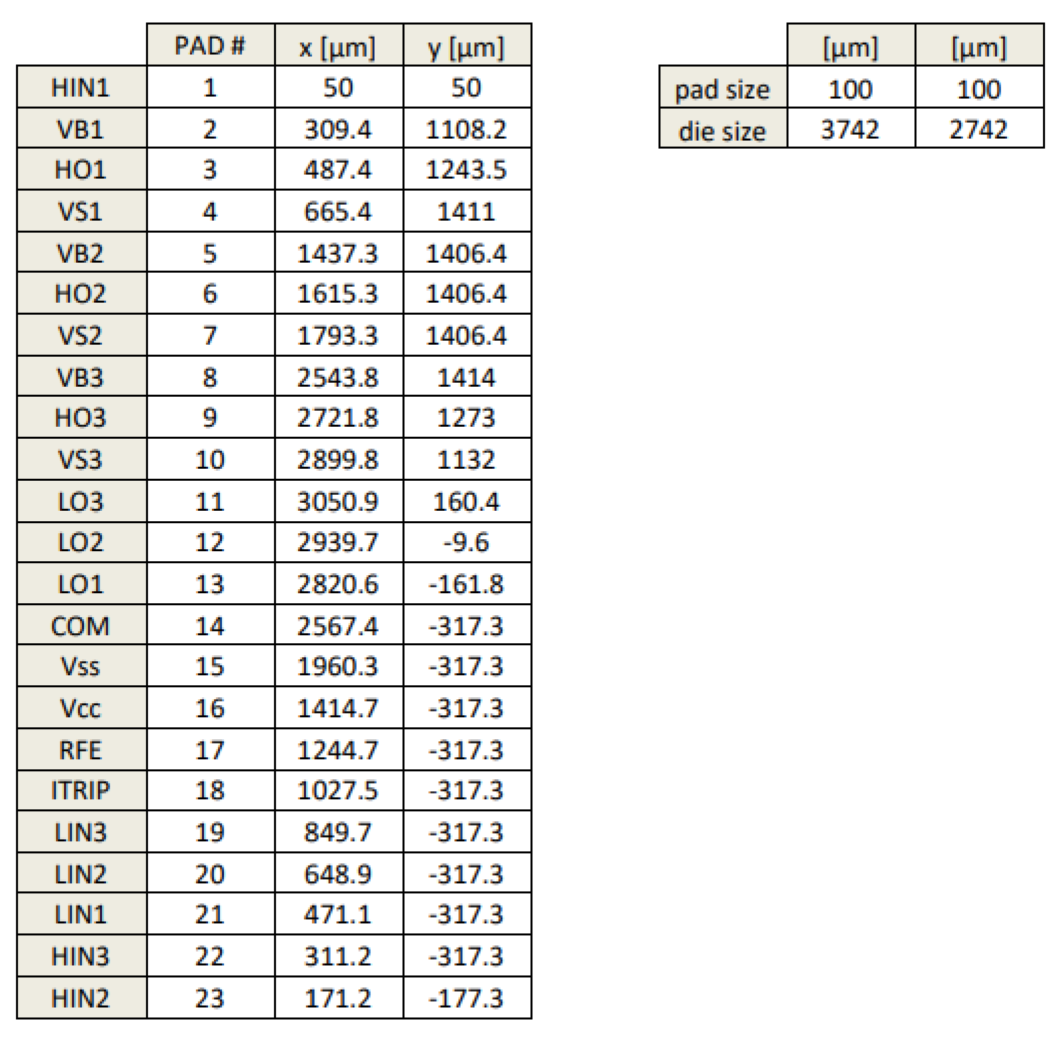


Figure 3 Pad Assignments



	PAD #	x [µm]	y [µm]
HIN1	1	50	50
VB1	2	309.4	1108.2
HO1	3	487.4	1243.5
VS1	4	665.4	1411
VB2	5	1437.3	1406.4
HO2	6	1615.3	1406.4
VS2	7	1793.3	1406.4
VB3	8	2543.8	1414
HO3	9	2721.8	1273
VS3	10	2899.8	1132
LO3	11	3050.9	160.4
LO2	12	2939.7	-9.6
LO1	13	2820.6	-161.8
COM	14	2567.4	-317.3
Vss	15	1960.3	-317.3
Vcc	16	1414.7	-317.3
RFE	17	1244.7	-317.3
ITRIP	18	1027.5	-317.3
LIN3	19	849.7	-317.3
LIN2	20	648.9	-317.3
LIN1	21	471.1	-317.3
HIN3	22	311.2	-317.3
HIN2	23	171.2	-177.3

	[µm]	[µm]
pad size	100	100
die size	3742	2742

Figure 4 Pad Coordinates

Table 1 Die Parameter

Parameter		**Unit**
Raster size of die	3742 x 2742	µm x µm
Area total / active	10.261	mm^2
Thickness	280	µm
Wafer size	200	mm
Max. possible chips per wafer	2646	pcs
Passivation front side	Polyimide	
Backside (Note 2)	Grinded silicon	
Pad metal composition	Ti/TiN/AlCu	
Pad metal thickness	1.1	µm
Reject ink dot diameter	Min. 0.6 Max 1.2	mm
Sawing street	62	µm

Note1: Filler material inside the mould compound with sharp edges may harm the passivation.
Note2: Chip must be bonded onto an electrically insulated area

3 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Table 2 **Absolute maximum ratings**

Parameter	**Symbol**	**Values**		**Unit**	**Note or Test Condition**
		Min.	**Max.**		
Low side supply voltage	V_{CC}	-0.3	25	V	—
Logic input voltage (LIN, HIN, RFE, ITRIP)	V_{IN}	V_{SS} - 5	V_{CC} + 0.3	V	—
High-side floating well supply voltage	$V_{B1,2,3}$	-0.3	1225	V	—
High-side floating well supply return voltage	$V_{S1,2,3}$	$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	V	—
Floating gate drive output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	V	—
Low-side output voltage	$V_{LO1,2,3}$	- 0.3	V_{CC} + 0.3	V	—
Logic ground	V_{SS}	V_{CC} - 25	V_{CC} + 0.3	V	—
Allowable VS offset supply transient relative to COM	dV_S/dt	—	50	V/ns	—
Junction temperature	T_J	—	150	°C	—
Storage temperature	T_S	-55	150	°C	—

4 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supplies of (V_{CC} - COM) = (V_B - V_S) = 15 V.

Table 3 **Recommended operating conditions**

Parameter	Symbol	Values		Unit	Note or Test Condition
		Min.	Max.		
Low-side supply voltage	V_{CC}	13	20	V	—
Logic input voltage (LIN, HIN, ITRIP)	V_{IN}	VSS	VSS + 5	V	—
RFE logic input voltage	V_{RFE}	VSS	VCC	V	—
High-side floating well supply voltage	$V_{B1,2,3}$	VS1,2,3 + 12	VS1,2,3 + 20	V	—
High-side floating well supply offset voltage	$V_{S1,2,3}$	COM – 8	900	V	[1]
Transient High-side floating well supply offset voltage	V_{St}	-100	1000	V	[2]
Floating gate drive output voltage	$V_{HO1,2,3}$	VS1,2,3	VB1,2,3	V	—
Low-side output voltage	$V_{LO1,2,3}$	0	VCC	V	—
Logic ground	V_{SS}	- 5	5	V	—
Ambient temperature	T_A	-40	125	°C	—

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[1] Logic operation for VS of –8 V to 1200 V. Logic state held for V_S of –8 V to –V_{BS}

[2] In case VCC > VB there is an additional power dissipation in the internal bootstrap diode between pins VCC and VBx. Insensitivity of bridge output to negative transient voltage up to –100 V is not subject to production test – verified by design / characterization.

5 Electrical characteristics

5.1 Static electrical characteristics

(VCC - COM) = (VB - VS) = 15 V. TA = 25 °C unless otherwise specified. The VIN and IIN parameters are referenced to COM. The V_O and I_O parameters are referenced to respective V_S and COM and are applicable to the respective output leads HO or LO. The VCCUV parameters are referenced to COM. The VBSUV parameters are referenced to VS.

Table 4 **Static electrical characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
V_{BS} supply under voltage positive threshold	V_{BSUV+}	—	10.4	—	V	—
V_{BS} supply under voltage negative threshold	V_{BSUV-}	—	9.4	—	V	—
V_{BS} supply under voltage hysteresis	V_{BSUVHY}	—	1	—	V	—
V_{CC} supply under voltage positive threshold	V_{CCUV+}	—	11.4	—	V	—
V_{CC} supply under voltage negative threshold	V_{CCUV-}	—	10.4	—	V	—
V_{CC} supply under voltage hysteresis	V_{CCUVHY}	—	1	—	V	—
High level output voltage drop, V_{BIAS}- V_O	V_{OH}	—	0.35	—	V	I_o = 20 mA
Low level output voltage drop, VO	V_{OL}	—	0.15	—	V	I_o = 20 mA
Logic “1” input voltage	V_{IH}	2.3	—	—	V	—
Logic “0” input voltage	V_{IL}	—	—	0.7	V	—
RFE positive going threshold	V_{RFE+}	1.7	1.9	2.3	V	—
RFE negative going threshold	V_{RFE-}	0.7	0.9	1.1	V	—
ITRIP positive going threshold	V_{ITRIP+}	0.475	0.500	0.525	V	—
ITRIP negative going threshold	V_{ITRIP-}	0.425	0.450	0.475	V	—
ITRIP hysteresis	$V_{ITRIP HYS}$	—	0.050	—	V	—
High-side floating well offset supply leakage	I_{LK}	—	—	50	µA	V_B = V_S = 1200 V
Quiescent V_{BS} supply current	I_{QBS}	—	175	250	µA	V_{IN} = 0 V or 5 V
Quiescent V_{CC} supply current	I_{QCC}	—	1000	1500	µA	V_{IN} = 0 V or 5 V
Mean output current for load capacity charging from 3 V (20%) to 6 V (40%)	$I_{O+ mean}$	200	300	—	mA	C = 22 nF
Mean output current for load capacity discharging fromn10.5 V (70%) to 7.5 V (50%)	$I_{O- mean}$	400	600	—	mA	C = 22 nF

Table 4 Static electrical characteristics (continued)

(VCC - COM) = (VB - VS) = 15 V. TA = 25 °C unless otherwise specified. The VIN and IIN parameters are referenced to COM. The VO and IO parameters are referenced to respective VS and COM and are applicable to the respective output leads HO or LO. The VCCUV parameters are referenced to COM. The VBSUV parameters are referenced to VS.

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output high short circuit pulsed current	I_{O+}	—	350	—	mA	V_O = 0 V PW ≤ 1 µs
Output low short circuit pulsed current	I_{O-}	—	650	—	mA	V_O = 15 V PW ≤ 1 µs
Logic “1” Input bias current (RFE)	I_{RFE+}	—	0	1	µA	V_{RFE} = 3.3 V
Logic “0” Input bias current (RFE)	I_{RFE-}	1	0	—	µA	V_{RFE} = 0 V
Logic “1” Input bias current (LIN, HIN)	I_{IN+}	—	1000	1250	µA	V_{IN} = 5 V
Logic “0” Input bias current (LIN, HIN)	I_{IN-}	—	—	1	µA	V_{IN} = 0 V
Logic “1” Input bias current (ITRIP)	I_{ITRIP+}	—	15	25	µA	V_{IN} = 1 V
Logic “0” Input bias current (ITRIP)	I_{ITRIP-}	—	—	1	µA	V_{IN} = 0 V
Bootstrap diode on resistance	R_{BS}	—	120	150	Ω	—
Bootstrap diode forward voltage drop	V_{FBSD}	—	0.9	—	V	I_o = 300 mA
RFE mos resistance	$R_{ON, RFE}$	—	40	60	Ω	—

Please refer to Application Section for integrated bootstrap diode description.

5.2 Dynamic electrical characteristics

V_{CC} = V_B = 15 V, V_S = COM, T_A = 25 °C, and C_L = 1000 pF unless otherwise specified.

Table 5 **Dynamic electrical characteristics**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Turn-on propagation delay	t_{ON}	500	700	900	ns	
Turn-off propagation delay	t_{OFF}	450	650	850	ns	
Turn-on rise time	t_R	—	35	—	ns	
Turn-off fall time	t_F	—	20	—	ns	
Dead time, LO turn-off to HO turn-on & HO turn-off to LO turn-on	DT	300	460	700	ns	
Delay matching time (t_{ON}, t_{OFF})	MT	—	—	130	ns	

Table 5 **Dynamic electrical characteristics (continued)**

$V_{CC} = V_B = 15$ V, V_S = COM, $T_A = 25$ °C, and $C_L = 1000$ pF unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Enable low to output shutdown propagation delay	t_{EN}	—	600	—	ns	
Input filter time (LIN, HIN, EN)	$T_{FIL,IN}$	200	350	500	ns	
FAULT clear time (R = 2 MΩ, C = 1 nF)	T_{FLTCLR}	—	1.9	—	ms	VDD = 3.3V
ITRIP to output shutdown propagation delay	T_{ITRIP}	—	750	1250	ns	$V_{ITRIP} = 1$ V
ITRIP blanking time	T_{BL}	—	500	—	ns	
ITRIP to FAULT propagation delay	T_{FLT}	450	650	900	ns	

6 Application information and additional details

Information regarding the following topics are included as subsections within this section of the datasheet.

- IGBT/MOSFET gate drive
- Switching and timing relationships
- Deadtime
- Matched propagation delays
- Input logic compatibility
- Undervoltage lockout protection
- Shoot-Through protection
- Enable input
- Fault reporting and programmable fault clear timer
- Over-Current protection
- Truth table: Undervoltage lockout, ITRIP, and ENABLE
- Advanced input filter
- Short-Pulse / Noise rejection
- Integrated bootstrap diodes
- Negative Vs transient SOA
- PCB layout tips
- Additional documentation

6.1 IGBT/MOSFET gate drive

The 6ED2230S12C HVICs are designed to drive MOSFET or IGBT power devices. Figure 5 and Figure 6 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as IO. The voltage that drives the gate of the external power switch is defined as VHO for the high-side power switch and VLO for the low-side power switch; this parameter is sometimes generically called VOUT and in this case does not differentiate between the high-side or low-side output voltage.

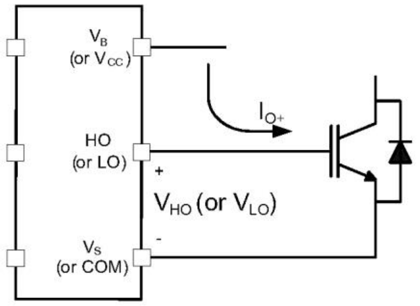


Figure 5 **HVIC sourcing current**

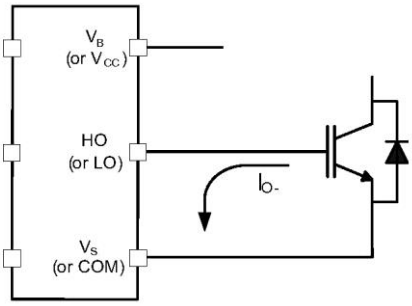


Figure 6 HVIC sinking current

6.2 Switching and timing relationships

The relationships between the input and output signals of the 6ED2230S12C are illustrated below in Figure 7. From these figures, we can see the definitions of several timing parameters (i.e., PWIN, PWOUT, tON, tOFF, tR, and tF) associated with this device.

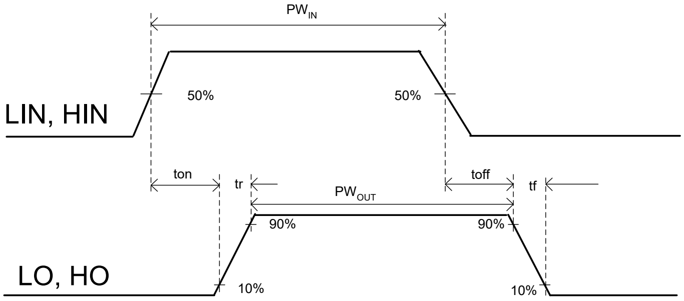


Figure 7 Switching timing waveforms _ Input/output timing diagram

Figure 8 and Figure 9 illustrate the timing relationships of some of the functionality of the 6ED2230S12C; this functionality is described in further detail later in this document. During interval A of Figure 8 the HVIC has received the command to turn-on both the high- and low-side switches at the same time; as a result, the shoot-through protection of the HVIC has. HVIC is keeping on output channel that is already on ignoring the 2nd input signal.

Interval B of Figure 8 and Figure 9 shows that the signal on the ITRIP input pin has gone from a low to a high state; as a result, all of the gate drive outputs have been disabled (i.e., see that HO has returned to the low state; LO is also held low), and a fault condition is reported on the RFE pin, which goes 0V. Once the ITRIP input has returned to the low state, the output will remain disabled and the fault condition reported until the voltage on the RFE pin charges up to VRFE+ threshold; the charging characteristics are dictated by the RC network attached to the RFE pin. After fault clear time HVIC is waiting for a new input signal on LIN/HIN before activate the output stage (LO/HO).

During interval C of Figure 8 and Figure 10, we can see that the RFE pin has been pulled low (as is the case when the driver IC has received a command from the control IC to shutdown); these results in the outputs (HO and LO) being held in the low state until the RFE pin is pulled high. After an enable event HVIC will wait for a new input signal on LIN/HIN before activate the output stage (LO/HO).

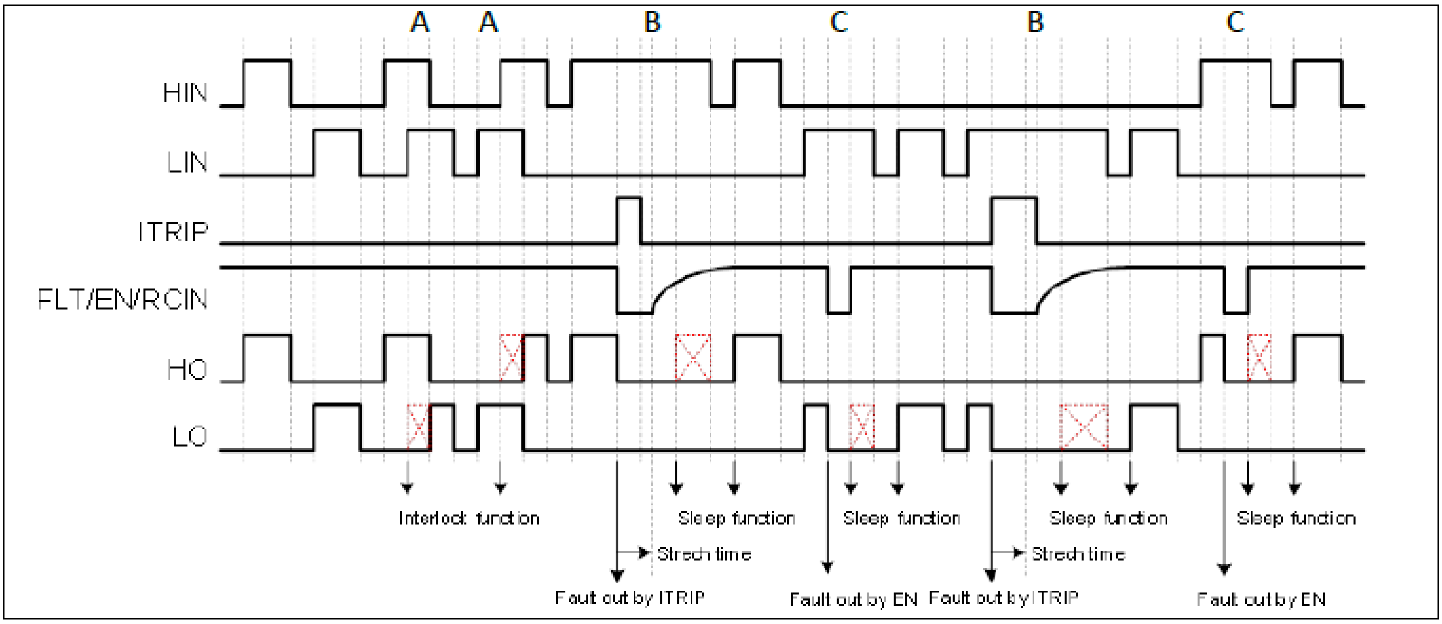


Figure 8 **Input/output timing diagram**

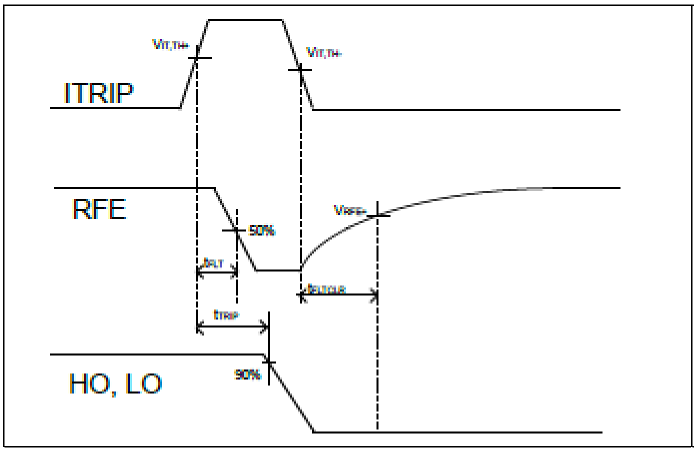


Figure 9 **Detailed view of B interval**

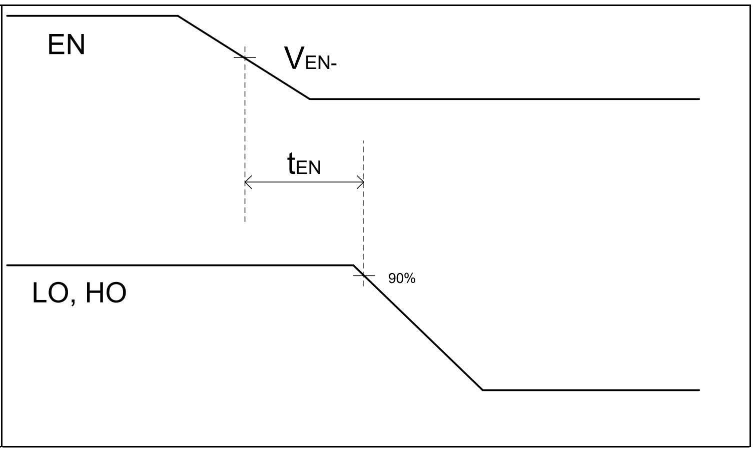
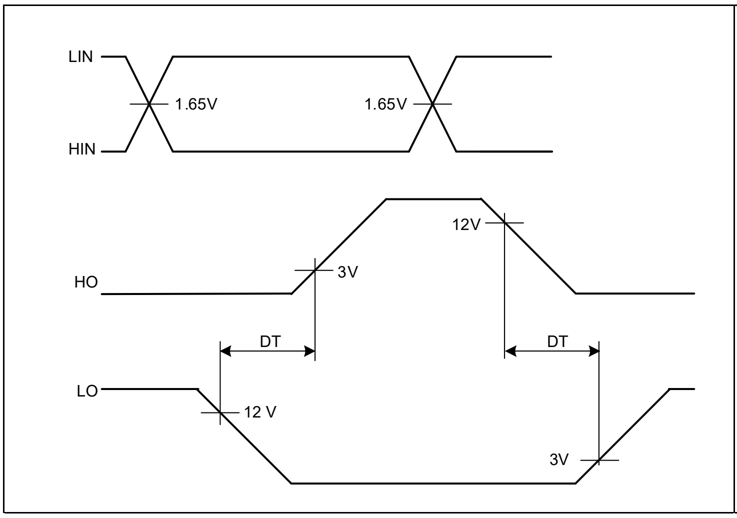


Figure 10 **Detailed view of C interval**

6.3 Deadtime and matched propagation delays

The 6ED2230S12C features integrated deadtime protection circuitry. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserter whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver. Figure 11 illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of 6ED2230S12C is matched with respect to the high- and low-side outputs. Figure 12 defines the two deadtime parameters (i.e., DTLO-HO and DTHO-LO); the deadtime matching parameter (MDT) associated with the 6ED2230S12C specifies the maximum difference between DTLO-HO and DTHO-LO.



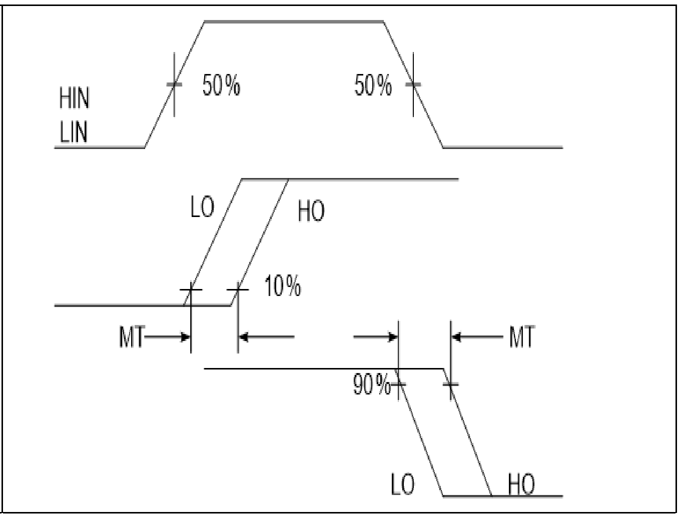


Figure 11 **Dead Time Definitions**

Figure 12 **Delay Matching Waveform Definitions**

The 6ED2230S12C is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., t_{ON}, t_{OFF}) for both the low-side channels and the high-side channels; the maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay (t_{ON}) of the 6ED2230S12C is matched to the propagation turn-on delay (t_{OFF}).

6.4 Input logic compatibility

The inputs of this IC are compatible with standard CMOS and TTL outputs. The 6ED2230S12C has been designed to be compatible with 3.3V and 5V logic-level signals. Figure 13 illustares an input signal to the 6ED2230S12C, its input threshold values, and the logic state of the IC as a result of the input signals.

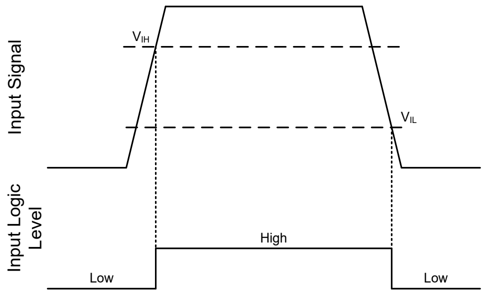


Figure 13 **HIN & LIN input thresholds**

6.5 Undervoltage lockout

This HVIC provides undervoltage lockout protection on both the VCC (logic and low-side circuitry) power supply and the VBS (high-side circuitry) power supply. Figure 14 is used to illustrate this concept; VCC (or VBS) is plotted over time and as the waveform crosses the UVLO threshold (VCCUV+/- or VBSUV+/-) the undervoltage protection is enabled or disabled.

Upon power-up, should the VCC voltage fail to reach the VCCUV+ threshold, the IC will not turn-on. Additionally, if the VCC voltage decreases below the VCCUV- threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high- and low-side gate drive outputs, and the FAULT pin will transition to the low state to inform the controller of the fault condition.

Upon power-up, should the VBS voltage fail to reach the VBSUV threshold, the IC will not turn-on. Additionally, if the VBS voltage decreases below the VBSUV threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

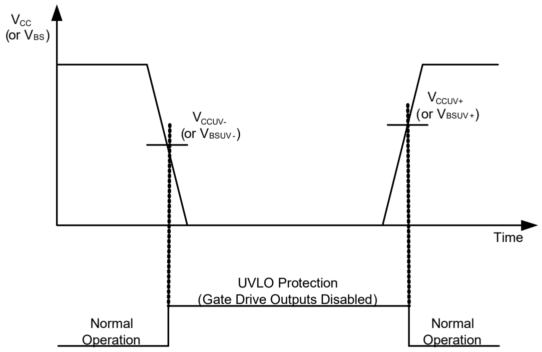


Figure 14 UVLO protection

6.6 Shoot-through protection

The 6ED2230S12C is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). Figure 15 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time.

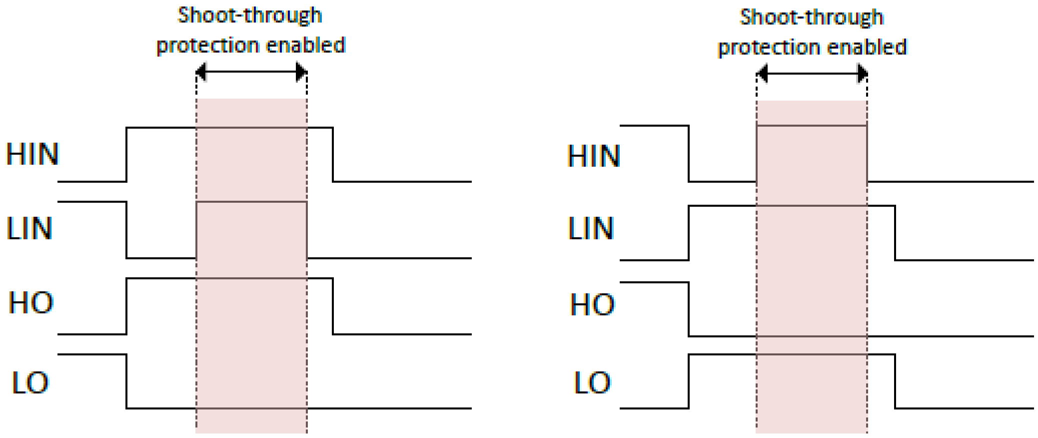


Figure 15 Illustration of shoot-through protection circuitry

6.7 Enable, Fault reporting and programmable fault clear timer

The 6ED2230S12C provides an enable functionality that allows it to shutdown or enable the HVIC and also provides an integrated fault reporting output along with an adjustable fault clear timer. There are two situations that would cause the IC to report a fault via the RFE pin. The first is an undervoltage condition of VCC and the second is if the over-current feature has recognized a fault. Once the fault condition occurs, the RFE pin is internally pulled to VSS and the fault clear timer is activated. The RFE output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the RFE pin will return to its external pull-up voltage.

The length of the fault clear time period (t_{FLTCLR}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{RFE} and C_{RFE}. Figure 16 shows that R_{RFE} is connected between the external supply (V_{DD})[1] and the RFE pin, while C_{RFE} is placed between the RFE and VSS pins.

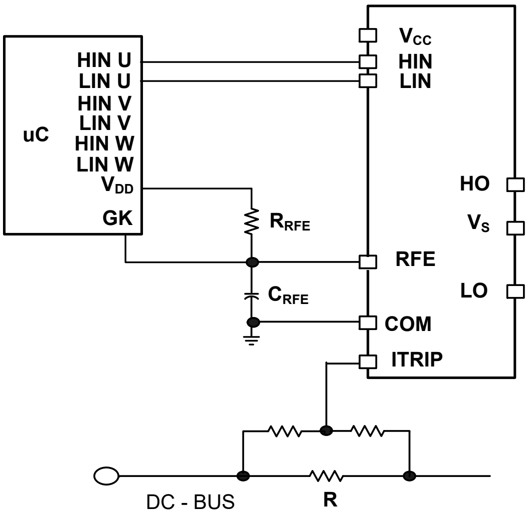


Figure 16 Programming the fault clear timer

The design guidelines for this network are shown in Table 6

Table 6 Design guidelines

C_{RFE}	≤1 nF
	Ceramic
R_{RFE}	0.5 MΩ to 2 MΩ
	>> $R_{ON,\,RCIN}$

The length of the fault clear time period can be determined by using the formula below.

$v_C(t) = V_{f^*}(1-e^{-t/RC})$

$t_{FLTCLR} = -\,(R_{RF^*}C_{RF})\ {}^*\ln\,(1-V_{RF+}/V_{DD}) + 160\text{us}$

The voltage on the RF pin should not exceed the VDD of the uC power supply.

[1] In case VDD is higher than 5V, the R_{RFE} resistor needs to be at least 200 kΩ in order to limit the IC power dissipation.

6.8 Over-current protection

The 6ED2230S12C is equipped with an over-current feature (ITRIP input pin). This functionality can sense over-current events in the DC- bus. Once the HVIC detects an over-current event, the outputs are shutdown, and RFE is pulled to VSS.

The level of current at which the over-current protection is initiated is determined by the resistor network (i.e., R_0, R_1, and R_2) connected to ITRIP as shown in Figure 17, and the ITRIP threshold (VITRIP+). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select R_0, R_1, and R_2 such that the voltage at node V_X reaches the over-current threshold $_{(VITRIP+)}$ at that current level.

$V_{ITRIP+} = R_0 * I_{DC-}(R_1/(R_1+R_2))$

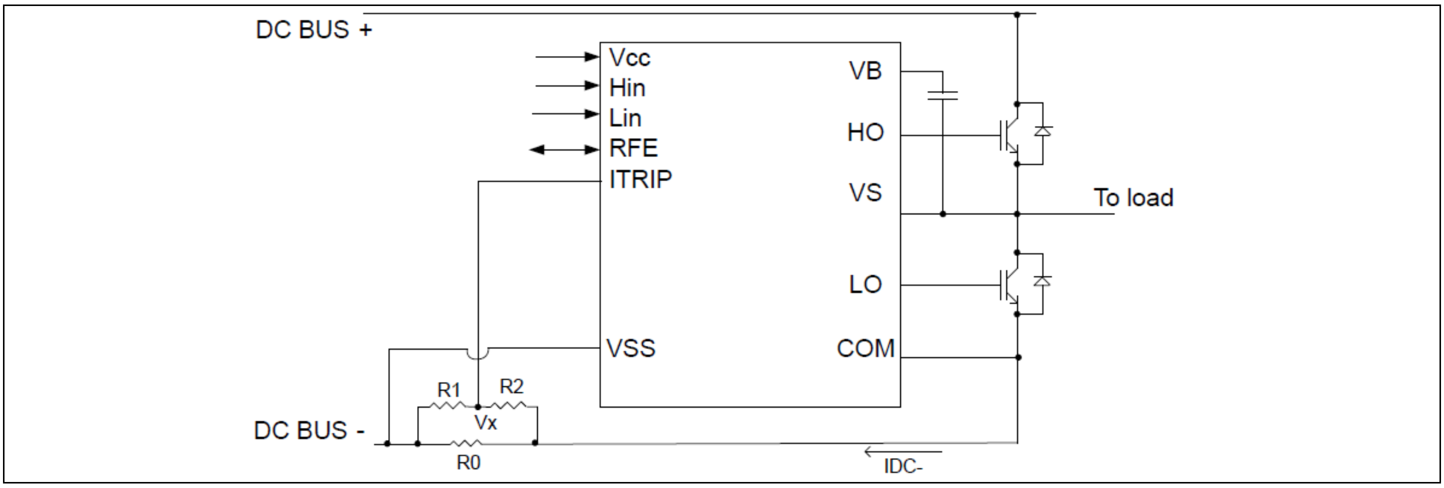


Figure 17 **Programming the over-current protection**

For example, a typical value for resistor R_0 could be 50 mΩ. The voltage of the ITRIP pin should not be allowed to exceed 5 V; if necessary, an external voltage clamp may be used.

6.9 Truth table: Undervoltage lockout, ITRIP and enable

Table 7 provides the truth table for the 6ED2230S12C. The first line shows that the UVLO for VCC has been tripped; the RFE output has gone low and the gate drive outputs have been disabled. VCCUV is not latched in this case and when VCC is greater than VCCUV, the FAULT output returns the driver is functional.

The second case shows that the UVLO for VBS has been tripped and that the high-side gate drive outputs have been disabled. After VBS exceeds the VBSUV threshold, HO will stay low until the HVIC input receives a new rising transition of HIN. The third case shows the normal operation of the HVIC. The fourth case illustrates that the ITRIP trip threshold has been reached and that the gate drive outputs have been disabled. This condition is stored in the external RC network waiting for fault clear time. The last case shows when the HVIC has received an enable command through the RFE input to shutdown; as a result, the gate drive outputs have been disabled.

Table 7 6ED2230S12C UVLO, ITRIP, FLT/EN/RCIN

	VCC	VBS	ITRIP	RFE	LO	HO
UVLO V_{CC}	$<V_{CCUV}$	—	—	0	0	0
UVLO V_{BS}	15 V	$<V_{BSUV}$	0 V	HIGH	LIN	0
Normal operation	15 V	15 V	0 V	HIGH	LIN	HIN
ITRIP fault	15 V	15 V	$>V_{ITRIP+}$	0	0	0
Enable command	15 V	15 V	0 V	HIGH	0	0
Disable	15 V	15 V	0 V	0	0	0

6.10 Advanced input filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the HVIC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN and LIN inputs. The working principle of the new filter is shown in Figure 18.

Figure 18 shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$.

Figure 19 shows the advanced input filter and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

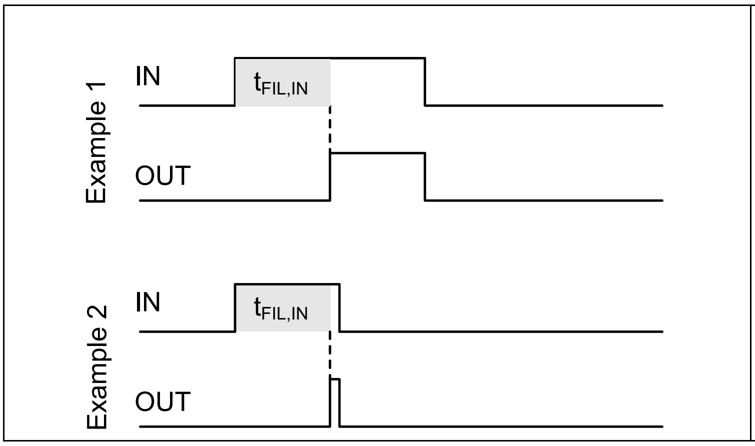


Figure 18 Typical input filter

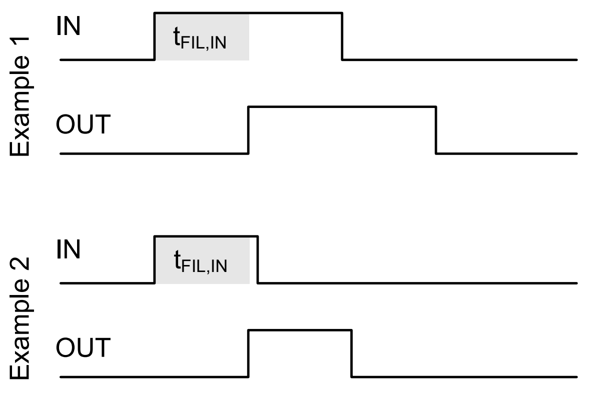


Figure 19 Advanced input filter

6.11 Short-Pulse / Noise Rejection

This device's input filter provides protection against short-pulses (e.g., noise) on the input lines. If the duration of the input signal is less than $t_{FIL,IN}$, the output will not change states. Example 1 of Figure 20 shows the input and output in the low state with positive noise spikes of durations less than $t_{FIL,IN}$; the output does not change states. Example 2 of Figure 20 shows the input and output in the high state with negative noise spikes of durations less than $t_{FIL,IN}$; the output does not change states.

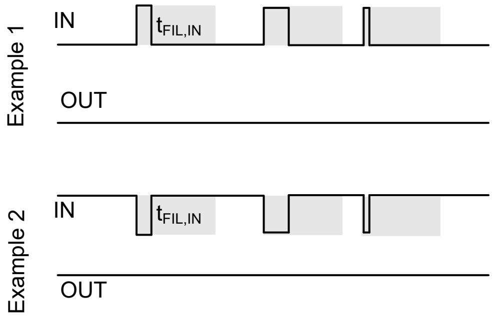


Figure 20 Noise rejecting input filters

6.12 Integrated bootstrap diode

An ultra-fast bootstrap diode is monolithically integrated for establishing the high side supply. The differential resistor of the diode helps to avoid extremely high inrush currents when initially charging the bootstrap capacitor. The integrated diode with its resistance helps save cost and improve reliability by reducing external components as shown below Figure 21.

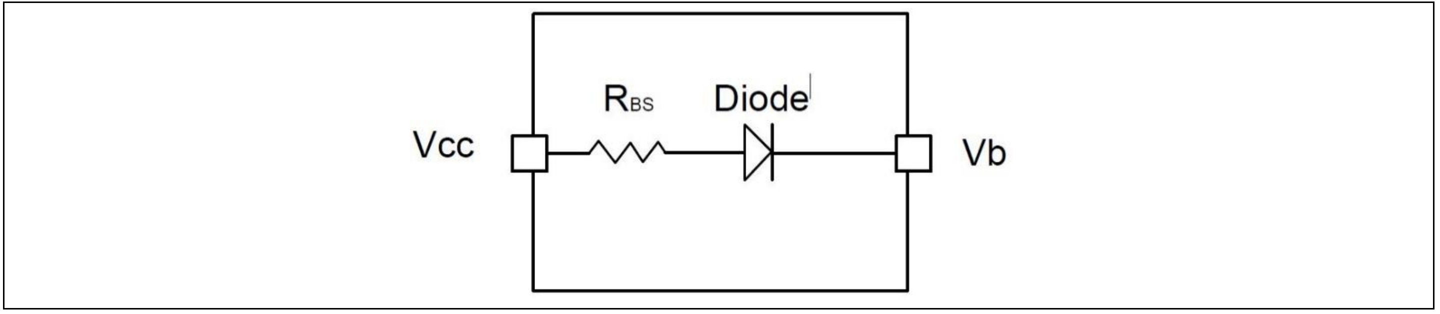


Figure 21 6ED2230S12C with integrated components

The low ohmic current limiting resistor provides essential advantages over other competitor devices with high ohmic bootstrap structures. A low ohmic resistor such as in the 6ED2230S12C allows faster recharching of the bootstrap capacitor during periods of small duty cycles on the low side transistor. The bootstrap diode is usable for all kind power electronic converters. The bootstrap diode is a real pn-diode and is temperature robust. It can be used at high temperatures with a low duty cycle of the low side transistor.

The bootstrap diode of the 6ED2230S12C works with all control algorithms of modern power electronics, such as trapezoidal or sinusoidal motor drives control.

6.13 Tolerance to negative VS transient

A common problem in today's high-power switching converters is the transient response of the switch node's voltage as the power switches transition on and off quickly while carrying a large current. A typical 3-phase inverter circuit is shown in Figure 22, here we define the power switches and diodes of the inverter.
If the high-side switch (e.g., the IGBT Q1 in Figure 23 A) and Figure 23-B) switches from on to off, while the U phase current is flowing to an inductive load, a current commutation occurs from high-side switch (Q1) to the diode (D2) in parallel with the low-side switch of the same inverter leg. At the same instance, the voltage node V_{S1}, swings from the positive DC bus voltage to the negative DC bus voltage.

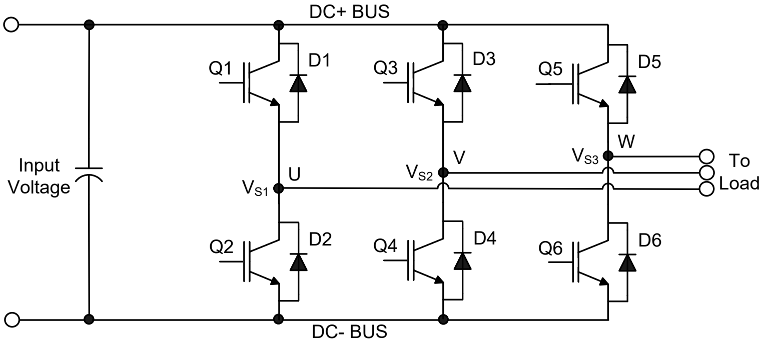


Figure 22 Three phase inverter

Also, when the V phase current flows from the inductive load back to the inverter (see Figure 23 C) and Figure 23 D)), and Q4 IGBT switches on, the current commutation occurs from D3 to Q4. At the same instance, the voltage node, V_{S2}, swings from the positive DC bus voltage to the negative DC bus voltage.

However, in a real inverter circuit, the VS voltage swing does not stop at the level of the negative DC bus, rather it swings below the level of the negative DC bus. This undershoot voltage is called “negative V_S transient”

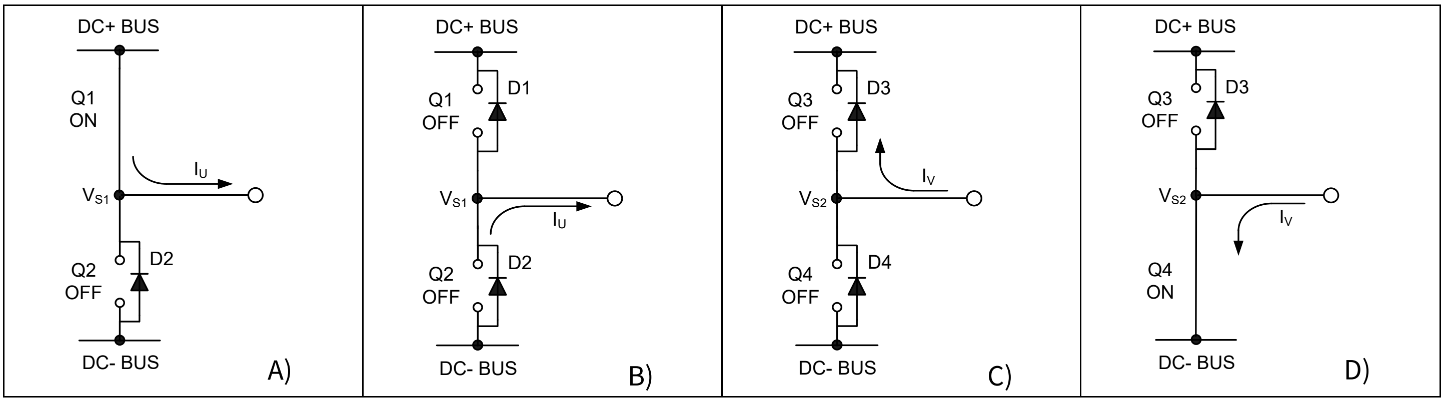


Figure 23 **A) Q1 conducting** **B) D2 conducting** **C) D3 conducting** **D) Q4 conducting**

The circuit shown in Figure 24 A) depicts one leg of the three phase inverter; Figure 24 B) and Figure 24 C)show a simplified illustration of the commutation of the current between Q1 and D2. The parasitic inductances in the power circuit from the die bonding to the PCB tracks are lumped together in L_C and L_E for each IGBT. When the high-side switch is on, V_{S1} is below the DC+ voltage by the voltage drops associated with the power switch and the parasitic elements of the circuit. When the high-side power switch turns off, the load current momentarily flows in the low-side freewheeling diode due to the inductive load connected to V_{S1} (the load is not shown in these figures). This current flows from the DC- bus (which is connected to the COM pin of the HVIC) to the load and a negative voltage between V_{S1} and the DC- Bus is induced (i.e., the COM pin of the HVIC is at a higher potential than the V_S pin).

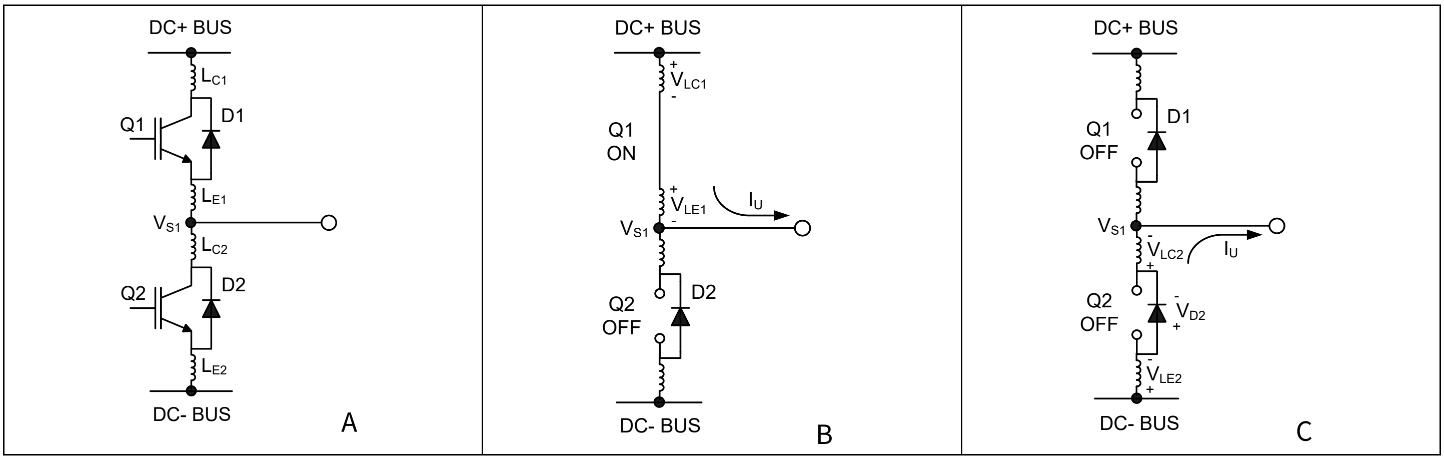


Figure 24 **Figure A shows the Parasitic Elements. Figure B shows the generation of V_S positive. Figure C shows the generation of V_S negative**

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative Vs transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the 6ED2230S12C's robustness can be seen in Figure 25 where the 6ED2230S12C Safe Operating Area is shown at VBS=15V based on repetitive negative Vs spikes. A negative Vs transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; viceversa unwanted functional anomalies or permanent damage to the IC do not appear if negative Vs transients fall inside the SOA.

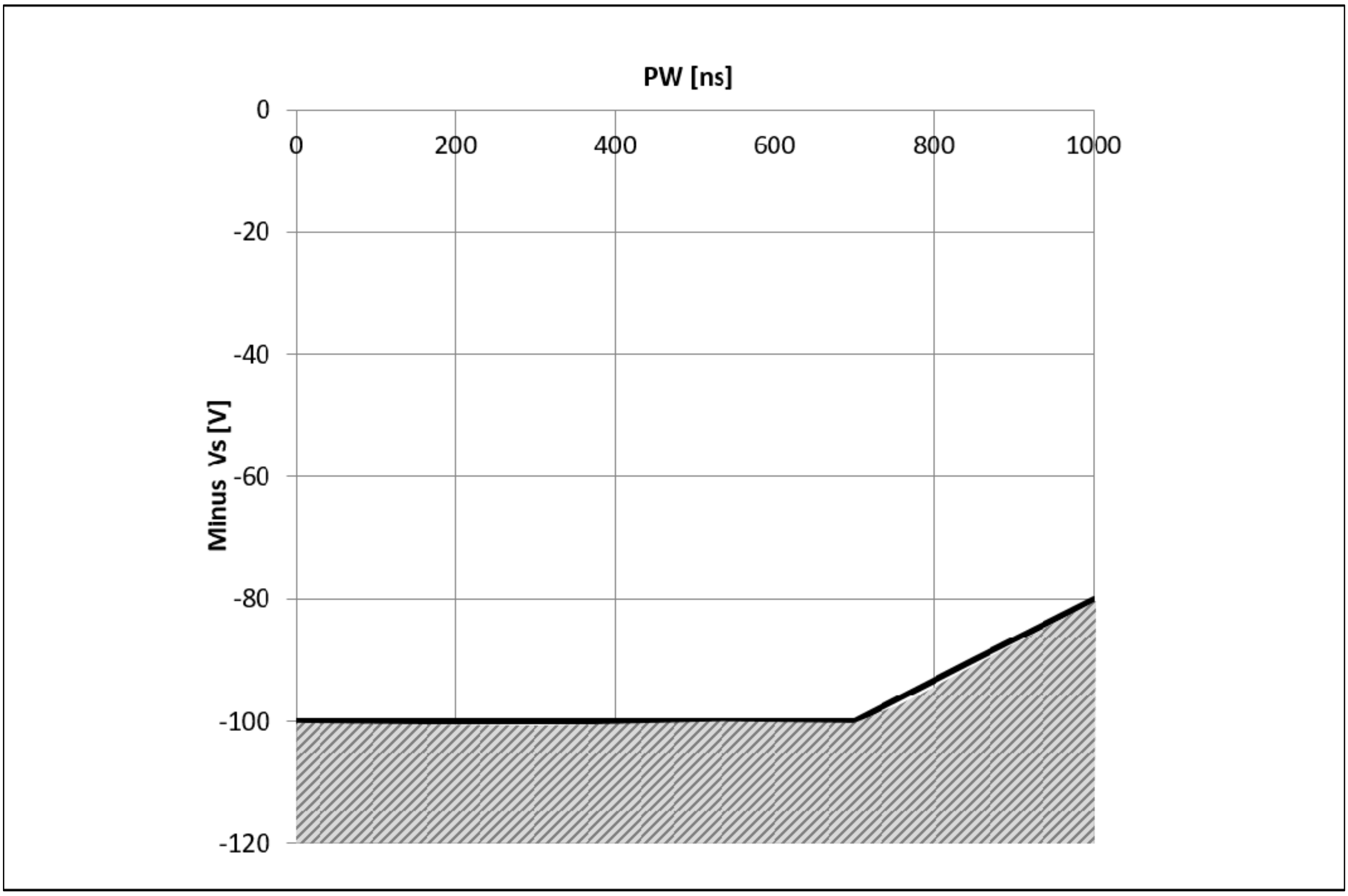


Figure 25 Negative Vs transient SOA for 6ED2230S12C @ VBS=15V

Even though the 6ED2230S12C has been shown to be able to handle these large negative Vs transient conditions, it is highly recommended that the circuit designer always limit the negative Vs transients as much as possible by careful PCB layout and component use.

6.14 PCB layout tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 26). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

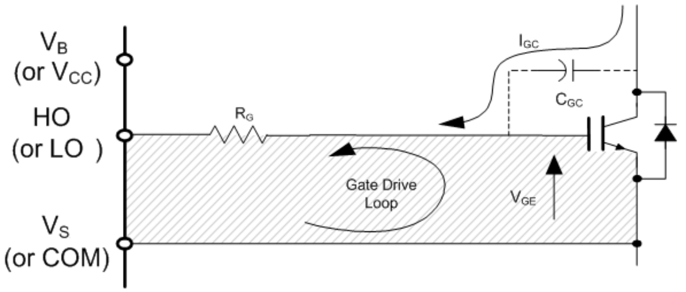


Figure 26 **Avoid antenna loops**

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the VCC and COM pins. A ceramic 1µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. In order to avoid such conditions, it is recommended to 1) minimize the high-side emitter to low-side collector distance, and 2) minimize the low-side emitter to negative bus rail stray inductance. However, where negative VS spikes remain excessive, further steps may be taken to reduce the spike. This includes placing a resistor (5 Ω or less) between the VS pin and the switch node (see Figure 27), and in some cases using a clamping diode between COM and V_S (see Figure 28). See DT04-4 at www.infineon.com for more detailed explanations.

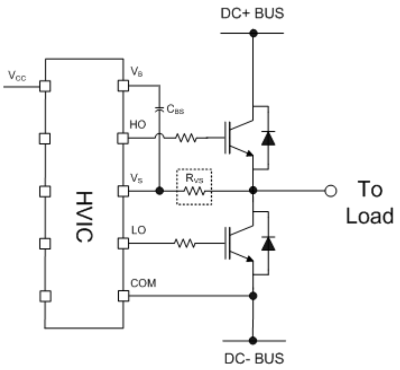


Figure 27 **Resistor between the VS pin and the switch node**

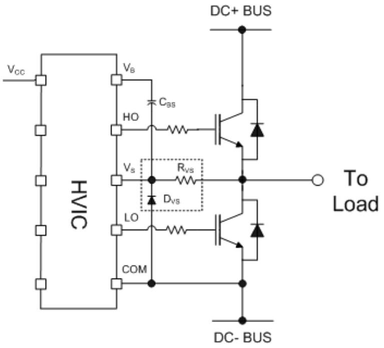


Figure 28 **Clamping diode between COM and V_S**

6.15 Related products

Table 8

Product	Description
Gate Driver ICs	
IR2214SS	1200 V Half-bridge gate driver with integrated dead-time, desaturation detection (DESAT), soft over-current shutdown, synchronized shutdown, two-stage turn-on for di/dt control, separate pull-up/pull-down output drive pins, matched propagation delays, and independent UVLO with hysteresis.
IR2213S	1200 V High and Low side gate driver with cycle by cycle shutdown logic, independent UVLO with hysteresis, matched propagation delays, and separate logic and power grounds.
IR2238Q	1200 V Three-phase motor controller with integrated programmable dead-time, desaturation detection (DESAT), brake chopper driver with protection, soft over-current shutdown, synchronized shutdown, hard shutdown, two-stage turn-on for dI/dt control, separate pull-up/pull-down output drive pins, matched propagation delays, and independent UVLO with hysteresis.
Power Switches	
IKW15N120BH6 **IKW40N120CS6**	High Speed 1200 V, 15 A/40 A/75 A hard-switching TRENCHSTOPTM IGBT6 co-packed with a very soft and fast recovery anti-parallel diode in a TO247 package/TO247PLUS 3pin package
IKW08T120 **IKW15N120T2** **IKW25N120T2** **IKW40N120T2**	The 1200 V, 8 A/15 A/25 A/40 A hard-switching TRENCHSTOPTM IGBT3 co-packed with free-wheeling diode in a TO247 package, provides significant improvement of static as well as dynamic performance of the device, due to combination of trench-cell and fieldstop concept.
IKQ40N120CT2	Infineon introduces the new package TO-247PLUS for 1200 V IGBT with increasing amounts of silicon in smaller, space saving packages with 40 A/50 A/75 A.
FP15R12W1T4 **FP15R12W2T4** **FP35R12W2T4**	EasyPIMTM 1B/2B 1200 V, 15 A/35 A PIM IGBT module with fast Trench/Fieldstop IGBT Emitter Controlled 4 diode and NTC.
FP15R12W1T4_B11	EasyPIMTM 1B 1200 V, 15 A PIM IGBT module with fast Trench/Fieldstop IGBT4, Emitte Controlled 4 diode, NTC and PressFIT Contact Technology.
FS25R12W1T4 **FS35R12W1T4**	EasyPACKTM 1B 1200 V, 25 A/35 A sixpack IGBT module with Trench/Fieldstop IGBT4, Emitter Controlled 4 diode and NTC.
FS25R12W1T4_B11	EasyPACKTM 1B 1200 V, 25 A sixpack IGBT module with Trench/Fieldstop IGBT4, Emitter Controlled 4 diode, NTC and PressFIT Contact Technology.
iMOTION™ Controllers	
IRMCK099	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
IMC101T	High performance Motor Control IC for variable speed drives based on field-oriented control (FOC) of permanent magnet synchronous motors (PMSM).

7 Qualification information

Table 8 **Qualification information**[1]

Qualification Level		Industrial[2] *Note: This family of ICs has passed JEDEC’s Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.*	
Moisture Sensitivity Level		DSO-24	MSL3[3], 260 °C (per IPC/JEDEC J-STD-020)
ESD	Human Body Model	Class 2 (per JEDEC standard JESD22-A114)	
	Charged Device Model	Class C4 (per JEDEC standard JS-022-2014)	
IC Latch-Up Test		Class II Level A (per JESD78)	
RoHS Compliant		Yes	

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[1] Qualification standards can be found at Infineon’s web site ***www.infineon.com***

[2] Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

[3] Higher MSL ratings may be available for the specific package types listed here. Please contact your Infineon sales representative for further information.

8 Additional documentation and resources

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

Application Notes:
Understanding HVIC Datasheet Specifications
HV Floating MOS-Gate Driver ICs
Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs
Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

Design Tips:
Using Monolithic High Voltage Gate Drivers
Alleviating High Side Latch on Problem at Power Up
Keeping the Bootstrap Capacitor Charged in Buck Converters
Managing Transients in Control IC Driven Power Stages
Simple High Side Drive Provides Fast Switching and Continuous On-Time

8.1 Infineon online forum resources

The Gate Driver Forum is live at Infineon Forums (www.infineonforums.com). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver Forum also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the Gate Driver Forum and learn the nuances of efficiently driving a power switch in any given power electronic application.

Revision history

Document version	Date of release	Description of changes
1.0	2025-10-22	First Release Version

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