EiceDRIVER™

2EDN752x/2EDN852x

Features

Fast, precise, strong and compatible

- Highly efficient SMPS enabled by 5 ns fast slew rates and 17 ns propagation delay precision for fast MOSFET and GaN switching
- 1 ns channel-to-channel propagation delay accuracy enables safe use of two channels in parallel
- Two independent 5 A channels enable numerous deployment options
- Industry standard packages and pinout ease system-design upgrades

The new Reference in Ruggedness

- 4.2 V and 8 V UVLO (Under Voltage Lock Out) options ensure instant MOSFET protection under abnormal conditions
- -10 V control and enable input robustness delivers crucial safety margin when driving pulse-transformers or driving MOSFETs in through hole packaging
- 5 A reverse current robustness eliminates the need for output protection circuitry.

Typical Applications

- Server SMPS
- TeleCom SMPS
- DC-to-DC Converter
- Bricks
- Power Tools
- Industrial SMPS
- Motor Control
- Solar SMPS

Example Topologies

- Single and interleaved PFC
- LLC, ZVS with pulse transformer
- Synchronous Rectification

Description

The 2EDN752x/2EDN852x is an advanced dual-channel driver. It is suited to drive logic and normal level MOSFETs and supports OptiMOS™, CoolMOS™, Standard Level MOSFETs, Superjunction MOSFETs, as well as IGBTs and GaN Power devices.

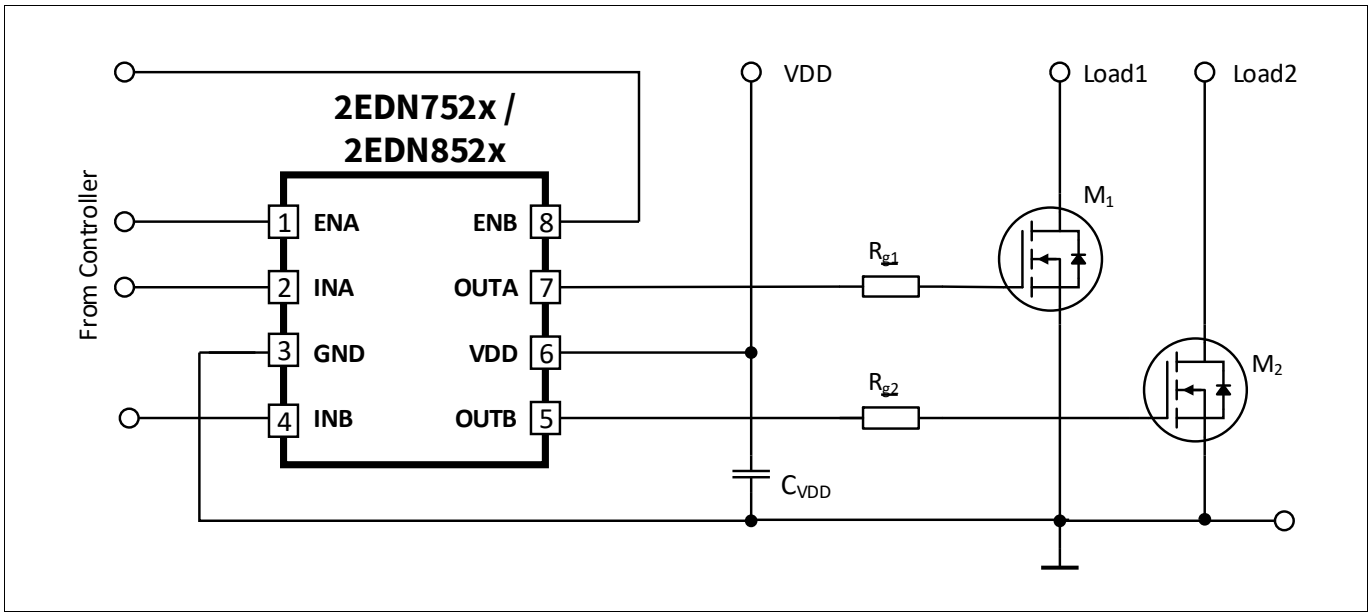
Features

The control and enable inputs are LV-TTL compatible (CMOS 3.3 V) with an input voltage range from -5 V to +20 V. -10 V input pin robustness protects the driver against latch-up or electrical overstress which can be induced by parasitic ground inductances. This greatly enhances system stability.

4.2 V and 8 V UVLO (Under Voltage Lock Out) options ensure instant MOSFET and GaN protection under abnormal conditions. Under such circumstances, this UVLO mechanism provides crucial independence from whether and when other supervisors circuitries detect abnormal conditions.

Each of the two outputs is able to sink and source 5 A currents utilizing a true rail-to-rail stage. This ensures very low on resistance of 0.7 Ω up to the positive and 0.55 Ω down to the negative rail respectively. Very tight channel to channel delay matching, typ. 1 ns, permits parallel use of two channels, leading to a source and sink capability of 10 A. Industry leading reverse current robustness eliminates the need for Schottky diodes at the outputs and reduces the bill-of-material.

The pinout of the 2EDN family is compatible with the industry standard. Two different control input options, direct and inverted, offer high flexibility. Three package variants, DSO 8-pin, TSSOP 8-pin, WSON 8-pin, allow optimization of PCB board space usage and thermal characteristics.



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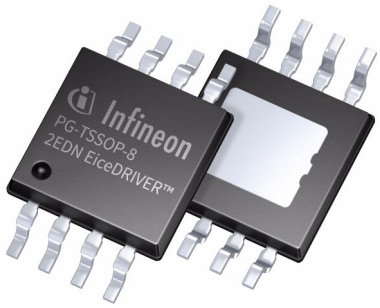
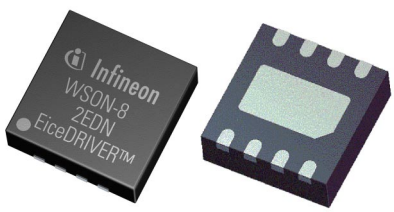
1 Product Versions

The 2EDN752x/2EDN852x are available in 2 different logic, 2 different undervoltage lockout and 3 package versions.

Table 1 Product Versions

Package	Type. UVLO	Control Input	Part Number	IC Topside Marking Code
PG-DSO-8				
	4.2V	direct	2EDN7524F	2N7524AF EiceDRIV XXHYYWW
		inverted	2EDN7523F	2N7523AF EiceDRIV XXHYYWW
	8V	direct	2EDN8524F	2N8524AF EiceDRIV XXHYYWW
		inverted	2EDN8523F	2N8523AF EiceDRIV XXHYYWW
PG-TSSOP-8				
	4.2V	direct	2EDN7524R	2N7524 AR_XXX HYYWW
		inverted	2EDN7523R	2N7523 AR_XXX HYYWW
	8V	direct	2EDN8524R	2N8524 AR_XXX HYYWW
		inverted	2EDN8523R	2N8523 AR_XXX HYYWW
PG-WSON-8				
	4.2V	direct	2EDN7524G	2N7524 AG_XXX HYYWW
		inverted	2EDN7523G	2N7523 AG_XXX HYYWW

1.1 Logic Versions

The 2 logic versions are indicated by the variable x in the product version 2EDNy52x:

- x=3: inverting input logic
- x=4: non-inverting / direct input logic

The logic relations between inputs, enable pins and outputs are given in **Table 2** for the inverting and non-inverting version 2EDNx523 and 2EDNx524. The state of the driving output is defined by the state of the respective input, if the enable inputs ENA and ENB are high (or left open). A logic “low” at an enable input or an undervoltage lockout event, due to low voltage at V_{DD}, causes the respective output to be low too, regardless of the input signal.

Functional description is shown in **Chapter 3** (**Block Diagram**) and **Chapter 4** (**Input Configurations**).

Table 2 Logic Table

Inputs					Output Inverting		Output Standard	
ENA	**ENB**	**INA**	**INB**	**UVLO[1)]**	**OUTA**	**OUTB**	**OUTA**	**OUTB**
x	x	x	x	active	L	L	L	L
L	L	x	x	inactive	L	L	L	L
H	L	L	x	inactive	H	L	L	L
H	L	H	x	inactive	L	L	H	L
L	H	x	L	inactive	L	H	L	L
L	H	x	H	inactive	L	L	L	H
H	H	L	L	inactive	H	H	L	L
H	H	H	L	inactive	L	H	H	L
H	H	L	H	inactive	H	L	L	H
H	H	H	H	inactive	L	L	H	H

1) Inactive means that VDD is above UVLO threshold voltage and release logic to control output stage.
Active means that UVLO disable active the output stages.

1.2 Package Versions

The logic and UVLO versions are available in 3 different packages.

- a standard PG-DSO-8 (designated by “F”)
- a small PG-TSSOP-8 (designated by “R”)
- a leadless PG-WSON-8 (designated by “G”)

Drawings can be viewed in **Chapter 9** (**Outline Dimensions**).

2 Pin Configuration and Description

The pin configuration for all input versions of 2EDN7524F, 2EDN7523F, 2EDN8524F and 2EDN8523F in the PG-DSO-8 package is shown in **Figure 1**. Drawings can be viewed in **Chapter 9** (**PG-DSO-8**).

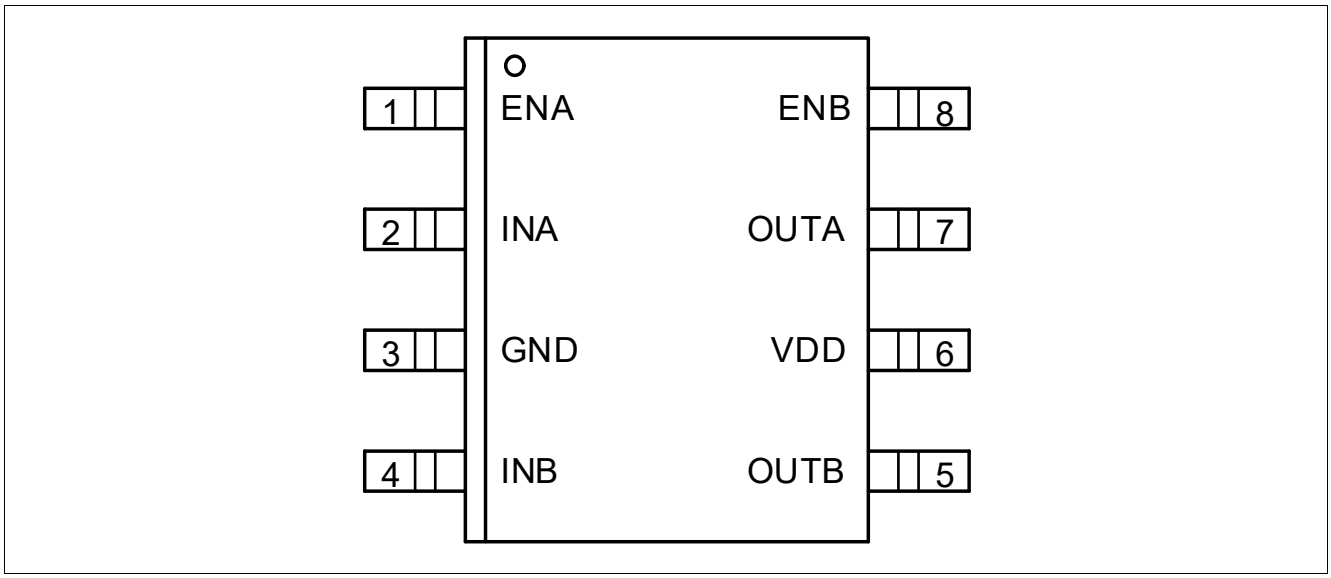


Figure 1 Pin Configuration PG-DSO-8, Top View

Table 3 Pin Configuration 2EDN7524F, 2EDN7523F, 2EDN8524F and 2EDN8523F in the PG-DSO-8 Package

Pin	Symbol	Description
1	ENA	Enable input channel A Logic input; if ENA is high or left open, OUTA is controlled by INA; ENA low causes OUTA low
2	INA	Input signal channel A Logic input, controlling OUTA (inverting or non-inverting)
3	GND	Ground
4	INB	Input signal channel B Logic input, controlling OUTB (inverting or non-inverting)
5	OUTB	Driver output channel B Low-impedance output with source and sink capability
6	VDD	Positive supply voltage Operating range 4.5 V/8.6V to 20 V
7	OUTA	Driver output channel A Low-impedance output with source and sink capability
8	ENB	Enable input channel B Logic Input; if ENB is high or left open, OUTB is controlled by INB; ENB low causes OUTB low

The pin configuration for all input versions of 2EDN7524R, 2EDN7523R, 2EDN8524R and 2EDN8523R in the PG-TSSOP-8 package is shown in **Figure 2**. Drawings can be viewed in **Chapter 9** (**PG-TSSOP-8**).

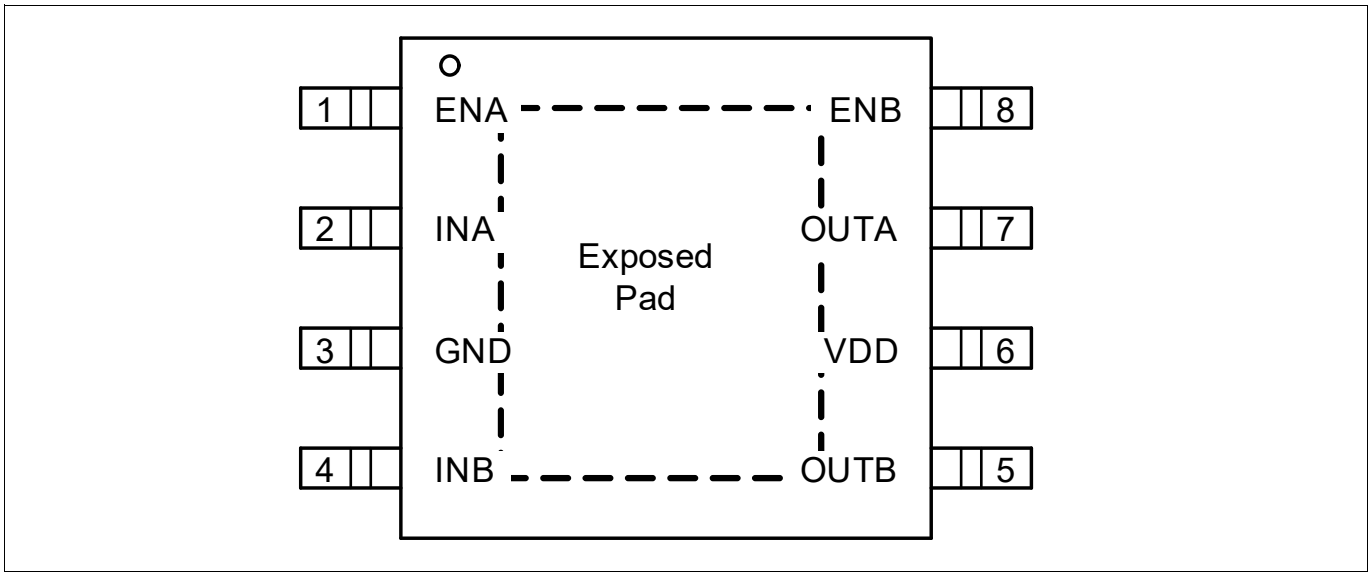


Figure 2 Pin Configuration PG-TSSOP-8, Top View

Table 4 Pin Configuration 2EDN7524R, 2EDN7523R, 2EDN8524R and 2EDN8523R in the PG-TSSOP-8 Package

Pin	Symbol	Description
1	ENA	Enable input channel A Logic input; if ENA is high or left open, OUTA is controlled by INA; ENA low causes OUTA low
2	INA	Input signal channel A Logic input, controlling OUTA (non-inverting)
3	GND	Ground[1)]
4	INB	Input signal channel B Logic input, controlling OUTB (non-inverting)
5	OUTB	Driver output channel B Low-impedance output with source and sink capability
6	VDD	Positive supply voltage Operating range 4.5 V/8.6V to 20 V
7	OUTA	Driver output channel A Low-impedance output with source and sink capability
8	ENB	Enable input channel B Logic Input; if ENB is high or left open, OUTB is controlled by INB; ENB low causes OUTB low

1) Exposed Pad sink of PG-TSSOP-8 packages has to be connected to GND pin.

The pin configuration for direct input versions of 2EDN7524G and 2EDN7523G in the PG-WSON-8 package is shown in **Figure 3**. Drawings can be viewed in **Chapter 9** (**PG-WSON-8**).

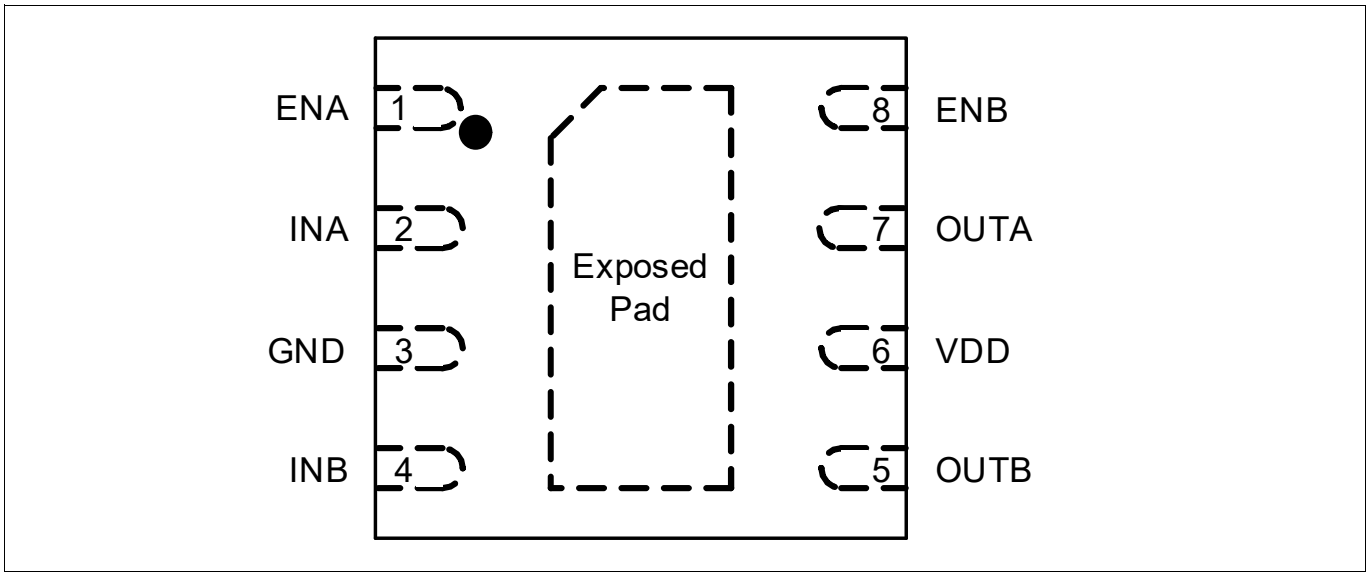


Figure 3 Pin Configuration PG-WSON-8, Top View

Table 5 Pin Configuration 2EDN7524G and 2EDN7523G in the PG-WSON-8 Package

Pin	Symbol	Description
1	ENA	Enable input channel A Logic input; if ENA is high or left open, OUTA is controlled by INA; ENA low causes OUTA low
2	INA	Input signal channel A Logic input, controlling OUTA (non-inverting)
3	GND	Ground[1)]
4	INB	Input signal channel B Logic input, controlling OUTB (non-inverting)
5	OUTB	Driver output channel B Low-impedance output with source and sink capability
6	VDD	Positive supply voltage Operating range 4.5 V/8.6V to 20 V
7	OUTA	Driver output channel A Low-impedance output with source and sink capability
8	ENB	Enable input channel B Logic Input; if ENB is high or left open, OUTB is controlled by INB; ENB low causes OUTB low

1) Exposed Pad of PG-WSON-8 packages has to be connected to GND pin.

3 Block Diagram

A simplified functional block diagram for the non-inverted / direct version is given in **Figure 4**. Please refer to the functional description section for more details in **Chapter 4**.

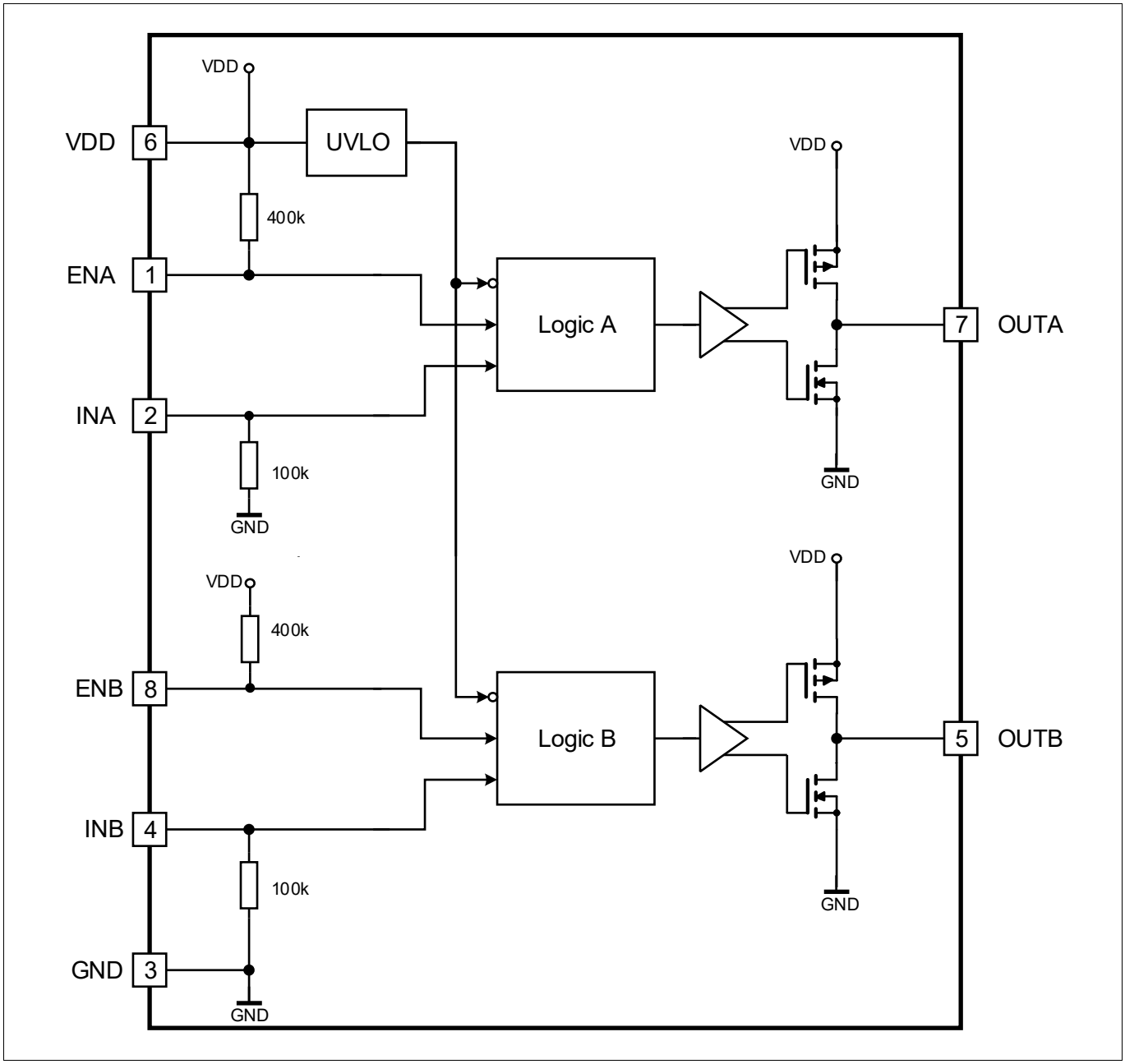


Figure 4 Block Diagram, direct input, pull-up/pull-down resistor configuration

Block Diagram

A simplified functional block diagram for the inverted version is given in **Figure 5**. Please refer to the functional description section for more details in **Chapter 4**.

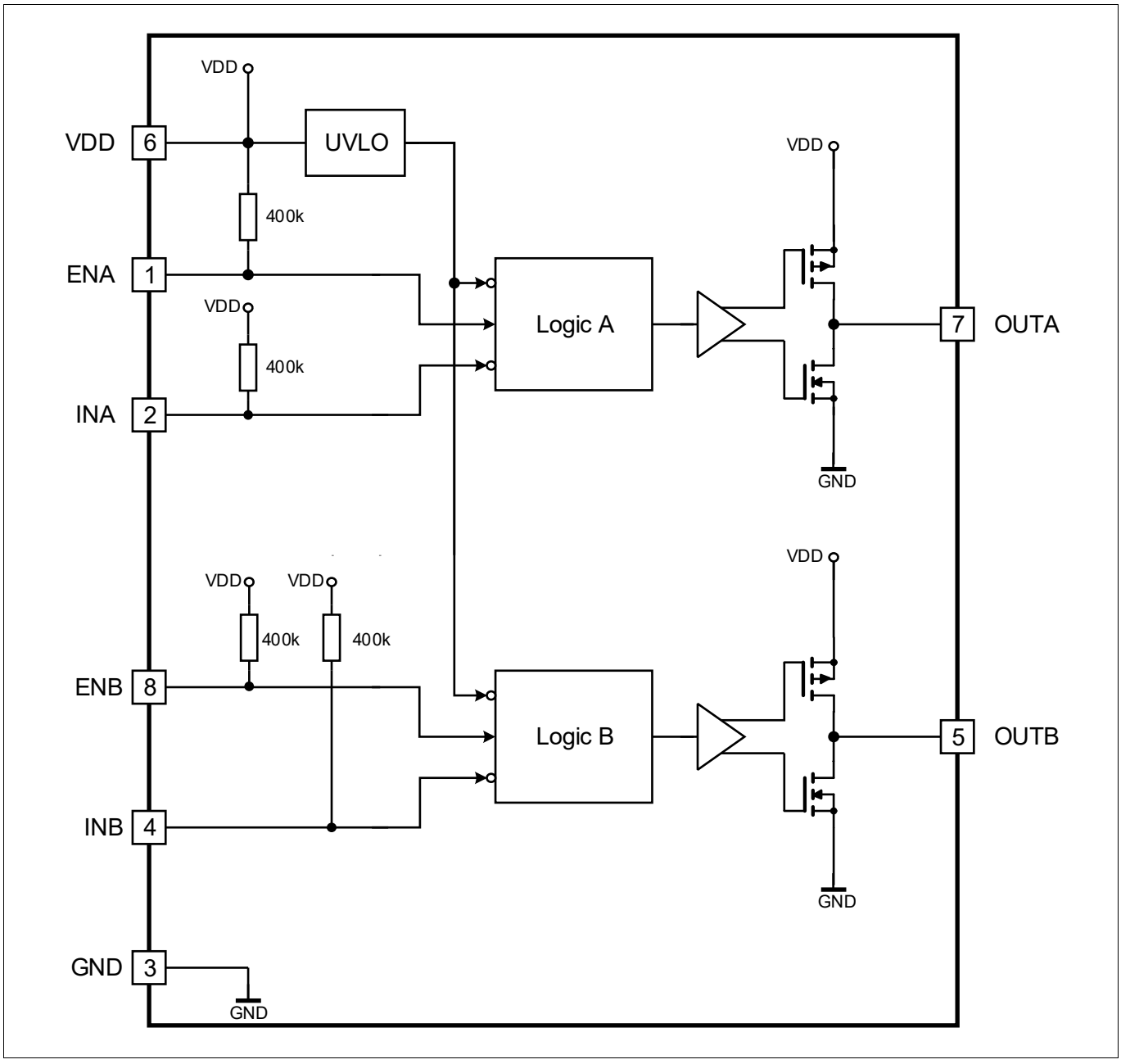


Figure 5 Block Diagram, inverting input, pull-up/pull-down resistor configuration

4 Functional Description

4.1 Introduction

The 2EDN752x/2EDN852x is a fast dual-channel driver for low-side switches. Two true rail-to-rail output stages with very low output impedance and high current capability are chosen to ensure highest flexibility and cover a high variety of applications.

The focus on robustness at the input and output side additionally gives this device a safety margin in critical abnormal situations. An extended negative voltage range protects input pins against ground shifts. No current flows over the ESD structure in the IC during a negative input level. All outputs are robust against reverse current. The interaction with the power MOSFET, even reverse reflected power will be handled by the strong internal output stage.

All inputs are compatible with LV-TTL signal levels. The threshold voltages with a typical hysteresis of 1.1 V are kept constant over the supply voltage range.

Since the 2EDN752x/2EDN852x aims particularly at fast-switching applications, signal delays and rise/fall times have been minimized. Special effort has been made towards minimizing delay differences between the 2 channels to very low values of typically 1 ns.

4.2 Supply Voltage

The maximum supply voltage is 20 V. This high voltage can be valuable in order to exploit the full current capability of 2EDN752x/2EDN852x when driving very large MOSFETs. The minimum operating supply voltage is set by the undervoltage lockout function to a typical default value of 4.2 V or of 8 V. This lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation.

4.3 Input Configurations

As described in **Chapter 1**, 2EDN752x/2EDN852x is available in 2 different configurations with respect to the logic configuration of the 4 input pins (input plus enable).

The enable inputs are internally pulled up to a logic high voltage, i.e. the driver is enabled with these pins left open. The direct PWM inputs are internally pulled down to a logic low voltage. This prevents a switch-on event during power up and a not driven input condition. Version with inverted PWM input have an internal pull up resistor to prevent unwanted switch-on.

All inputs are compatible with LV-TTL levels and provide a hysteresis of 1.1 V typ. This hysteresis is independent of the supply voltage.

All input pins have a negative extended voltage range. This prevents cross current over single wires during GND shifts between signal source (controller) and driver input.

4.4 Driver Outputs

The two rail-to-rail output stages realized with complementary MOS transistors are able to provide a typical 5 A of sourcing and sinking current. This driver output stage has a shoot through protection and current limiting behavior. After a switching event, current limitation is raised up to achieve the typical current peak for an excellent fast reaction time of the following power MOS transistor.

The output impedance is very low with a typical value below 0.7 Ω for the sourcing p-channel MOS and 0.5 Ω for the sinking n-channel MOS transistor. The use of a p-channel sourcing transistor is crucial for achieving true rail-to-rail behaviour and avoiding a source follower's voltage drop.

Gate Drive Outputs held active low in case of floating inputs ENx, INx or during startup or power down once UVLO is not exceeded. Under any situation, startup, UVLO or shutdown, outputs are held under defined conditions.

4.5 Undervoltage Lockout (UVLO)

The Undervoltage Lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO threshold voltage. Thus it can be guaranteed, that the switch transistor is not switched on if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation.

The UVLO level is set to a typical value of 4.2 V / 8 V (with hysteresis). UVLO of 4.2 V is normally used for logic level based MOSFETs. For higher level, like standard and high voltage superjunction MOSFETS, an UVLO voltage of typical 8 V is available.

5 Characteristics

The absolute maximum ratings are listed in **Table 6**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Absolute Maximum Ratings

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Positive supply voltage	V_{VDD}	-0.3	–	22	V	–
Voltage at pins INA, INB, ENA, ENB	V_{IN}	-10	–	22	V	–
Voltage at pins OUTA, OUTB	V_{OUT}	-0.3	–	V_{VDD}+0.3	V	Note[1]
		-2	–	V_{VDD}+0.3	V	Repetitive pulse <200 ns[2]
Reverse current peak at pins OUTA, OUTB	I_{SNKREV} I_{SRCREV}		–	-5 5	A_{pk}	< 500 ns
Junction temperature	T_J	-40	–	150	°C	–
Storage temperature	T_S	-55	–	150	°C	–
ESD capability	V_{ESD}	–	–	1.5	kV	Charged Device Model (CDM) [3]
ESD capability	V_{ESD}	–	–	2.5	kV	Human Body Model (HBM) [4]

1) Voltage spikes resulting from reverse current peaks are allowed.
2) Values are verified by characterization on bench.
3) According to JESD22-C101.
4) According to JESD22-A114.

5.2 Thermal Characteristics

Table 7 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction-ambient [1]	R_{thJA25}	–	125	–	K/W	PG-DSO-8, T_{amb} = 25°C
Thermal resistance junction-case (top) [2]	R_{thJC25}	–	66	–	K/W	PG-DSO-8, T_{amb} = 25°C
Thermal resistance junction-board [3]	R_{thJB25}	–	62	–	K/W	PG-DSO-8, T_{amb} = 25°C
Characterization parameter junction-top [4]	Ψ_{thJC25}	–	16	–	K/W	PG-DSO-8, T_{amb} = 25°C
Characterization parameter junction-board [5]	Ψ_{thJB25}	–	55	–	K/W	PG-DSO-8, T_{amb} = 25°C

Table 7 Thermal Characteristics (continued)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction-ambient 1)	R_{thJA25}	–	64	–	K/W	PG-TSSOP-8, T_{amb} = 25°C
Thermal resistance junction-case (top) 2)	R_{thJP25}	–	56	–	K/W	PG-TSSOP-8, T_{amb} = 25°C
Thermal resistance junction-board 3)	R_{thJB25}	–	55	–	K/W	PG-TSSOP-8, T_{amb} = 25°C
Characterization parameter junction-top 4)	Ψ_{thJC25}	–	9	–	K/W	PG-TSSOP-8, T_{amb}=25°C
Characterization parameter junction-board 5)	Ψ_{thJB25}	–	13	–	K/W	PG-TSSOP-8, T_{amb} = 25°C
Thermal resistance junction-ambient 1)	R_{thJA25}	–	61	–	K/W	PG-WSON-8, T_{amb} = 25°C
Thermal resistance junction-case (top) 2)	R_{thJP25}	–	54	–	K/W	PG-WSON-8, T_{amb} = 25°C
Thermal resistance junction-board 3)	R_{thJB25}	–	52	–	K/W	PG-WSON-8, T_{amb} = 25°C
Characterization parameter junction-top 4)	Ψ_{thJC25}	–	8	–	K/W	PG-WSON-8, T_{amb} = 25°C
Characterization parameter junction-board 5)	Ψ_{thJB25}	–	11	–	K/W	PG-WSON-8, T_{amb} = 25°C

1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
4) The characterization parameter junction-top, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Rth, using a procedure described in JESD51-2a (sections 6 and 7).
5) The characterization parameter junction-board, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining Rth, using a procedure described in JESD51-2a (sections 6 and 7).

5.3 Operating Range

Table 8 Operating Range

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{VDD}	4.5	–	20	V	Min. defined by UVLO
Logic input voltage	V_{IN}	-5	–	20	V	–
Junction temperature	T_J	-40	–	150	°C	1)

1) Continuous operation above 125 °C may reduce life time.

5.4 Electrical Characteristics

Unless otherwise noted, min./max. values of characteristics are the lower and upper limits respectively. They are valid within the full operating range. The supply voltage is V_{VDD}= 12 V. Typical values are given at T_J=25°C.

Table 9 Power Supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VDD quiescent current	I_{VDDQU1}	0.5	0.7	1.2	mA	OUT = high, V_{VDD} = 12 V
VDD quiescent current	I_{VDDQU2}	0.3	0.48	0.7	mA	OUT = low, V_{VDD} = 12 V

Table 10 Undervoltage Lockout for Logic Level MOSFET

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{ON}$	3.9	4.2	4.5	V	–
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{OFF}$	3.6	3.9	4.2	V	–
UVLO threshold hysteresis	$UVLO_{HYS}$	–	0.3	–	V	–

Table 11 Undervoltage Lockout for Standard and Superjunction MOSFET Version

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout (UVLO) turn on threshold	$UVLO_{ON}$	7.4	8.0	8.6	V	–
Undervoltage Lockout (UVLO) turn off threshold	$UVLO_{OFF}$	6.5	7.0	7.5	V	–
UVLO threshold hysteresis	$UVLO_{HYS}$	–	1.0	–	V	–

Table 12 Logic Inputs INA, INB, ENA, ENB

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{INH}	1.98	2.1	2.2	V	–
Input voltage threshold for transition HL	V_{INL}	0.95	1.02	1.1	V	–
Input pull up resistor[1)]	R_{INH}	–	400	–	kΩ	–
Input pull down resistor[2)]	R_{INL}	–	100	–	kΩ	–

1) Inputs with initial high logic level.
2) Inputs with initial low logic level.

Table 13 Static Output Caracteristics (see Figure 7)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High Level (Sourcing) Output Resistance	R_{ONSRC}	0.35	0.7	1.2	Ω	I_{SRC} = 50mA
High Level (Sourcing) Output Current	$I_{SRCPEAK}$	–	5.0	1)	A	–
Low Level (Sinking) Output Resistance	R_{ONSNK}	0.28	0.55	1.0	Ω	I_{SNK} = 50mA
Low Level (Sinking) Output Current	$I_{SNKPEAK}$	–	-5.0	2)	A	–

1) Active limited by design at approx. 6.5Apk, parameter is not subject to production test - verified by design/characterization, max. power dissipation must be observed.

2) Active limited by design at approx. -6.5Apk, parameter is not subject to production test - verified by design/characterization, max. power dissipation must be observed.

Table 14 Dynamic Characteristics (see Figure 6, Figure 7, Figure 8 and Figure 9)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input/Enable to output propagation delay	t_{PDlh}	15	17	23	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V; low to high transition at Input/Enable
Input/Enable to output propagation delay	t_{PDhl}	15	19	23	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V high to low transition at Input/Enable
Input/Enable to output propagation delay mismatch between the two channels on the same IC	Δt_{PD}	–	–	2	ns	–
Rise Time	t_{RISE}	–	5.3	10 1)	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Fall Time	t_{FAll}	–	4.5	10 1)	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V
Minimum input pulse width that changes output state	t_{PW}	–	–	15 1)	ns	C_{LOAD}= 1.8 nF, V_{VDD}= 12 V

1) Parameter verified by design, not tested in production.

6 Timing Diagrams

Figure 6 shows the definition of rise, fall and delay times for the inputs of the non-inverting / direct version (with Enable pin high or open).

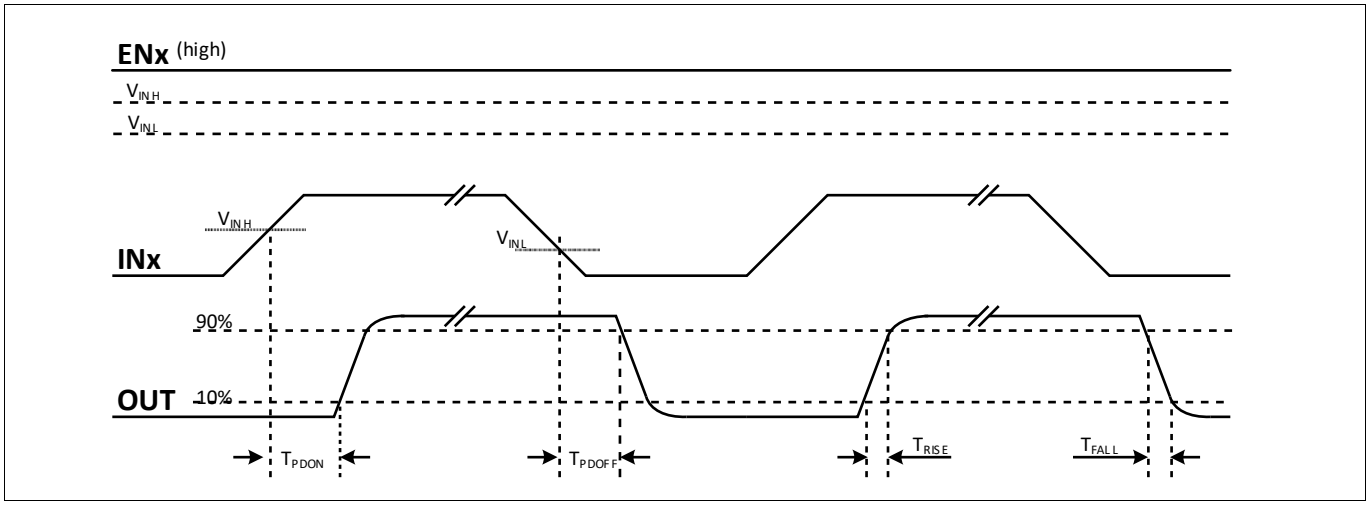


Figure 6 Propagation delay, rise and fall time, non-inverted

Figure 7 shows the definition of rise, fall and delay times for the inputs of the inverting version (with enable pins high or open).

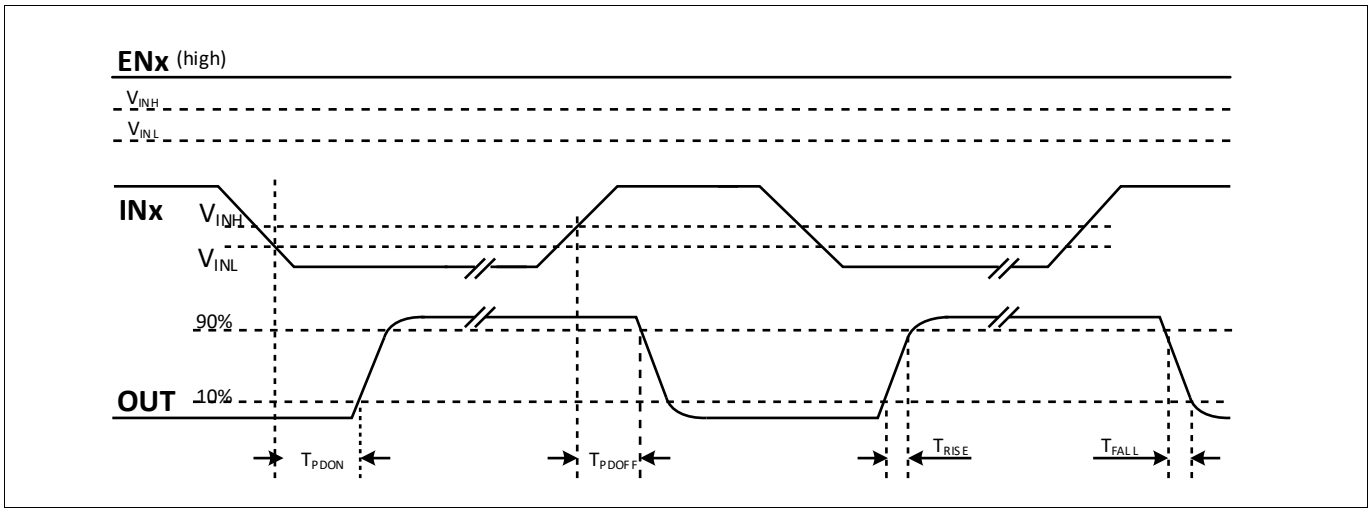


Figure 7 Propagation delay, rise and fall Time, inverted

Figure 8 illustrates the undervoltage lockout function.

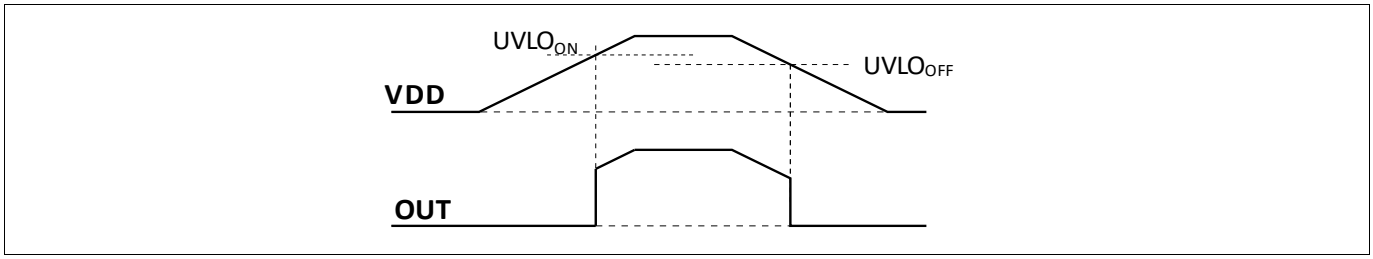


Figure 8 UVLO behaviour, input ENx and INx drives OUTx normally high

Figure 9 illustrates the minimum input pulse width that changes output state.

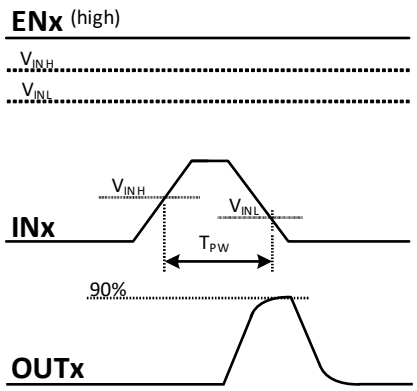


Figure 9 TPW, minimum input pulse width that changes output state

7 Typical Characteristics

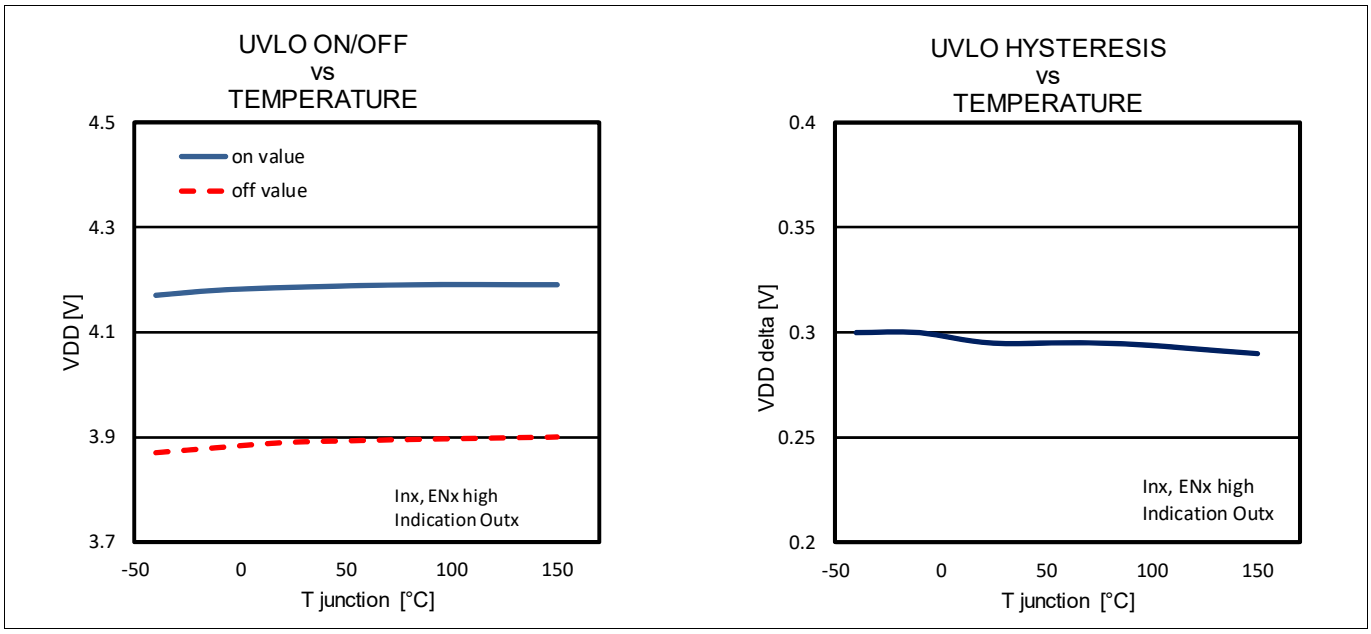


Figure 10 Undervoltage lockout 2ED7x (4.2V)

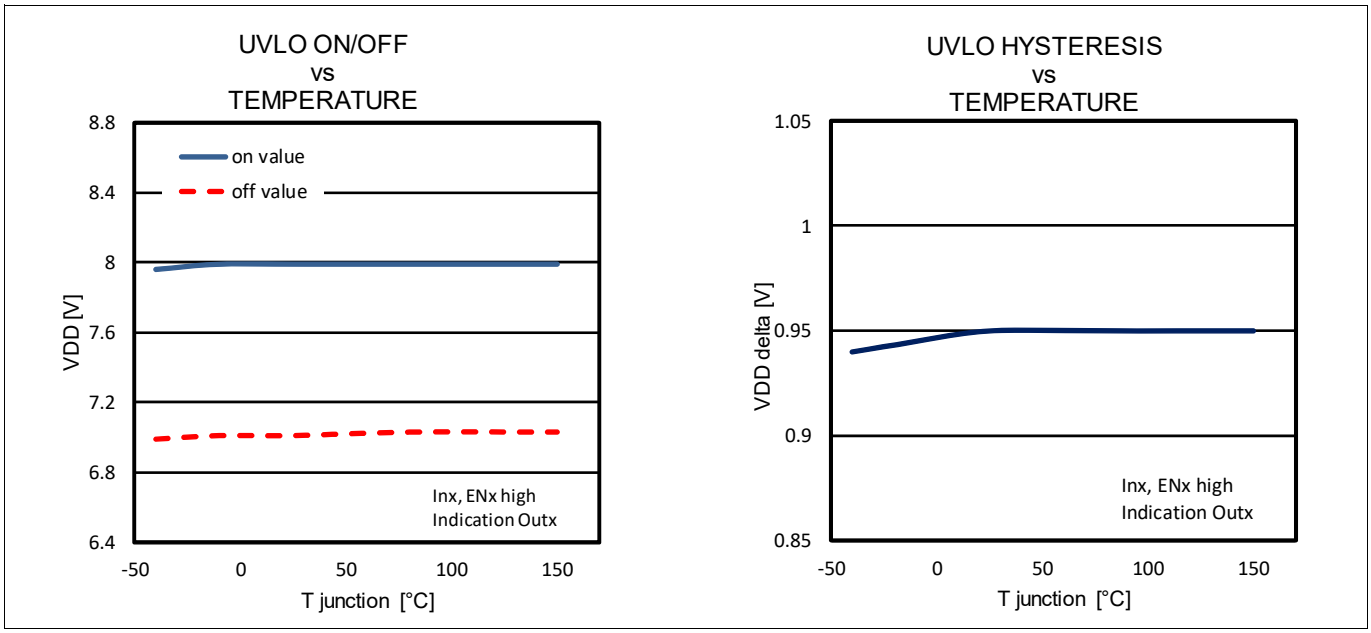


Figure 11 Undervoltage lockout 2ED8x (8V)

Typical Characteristics

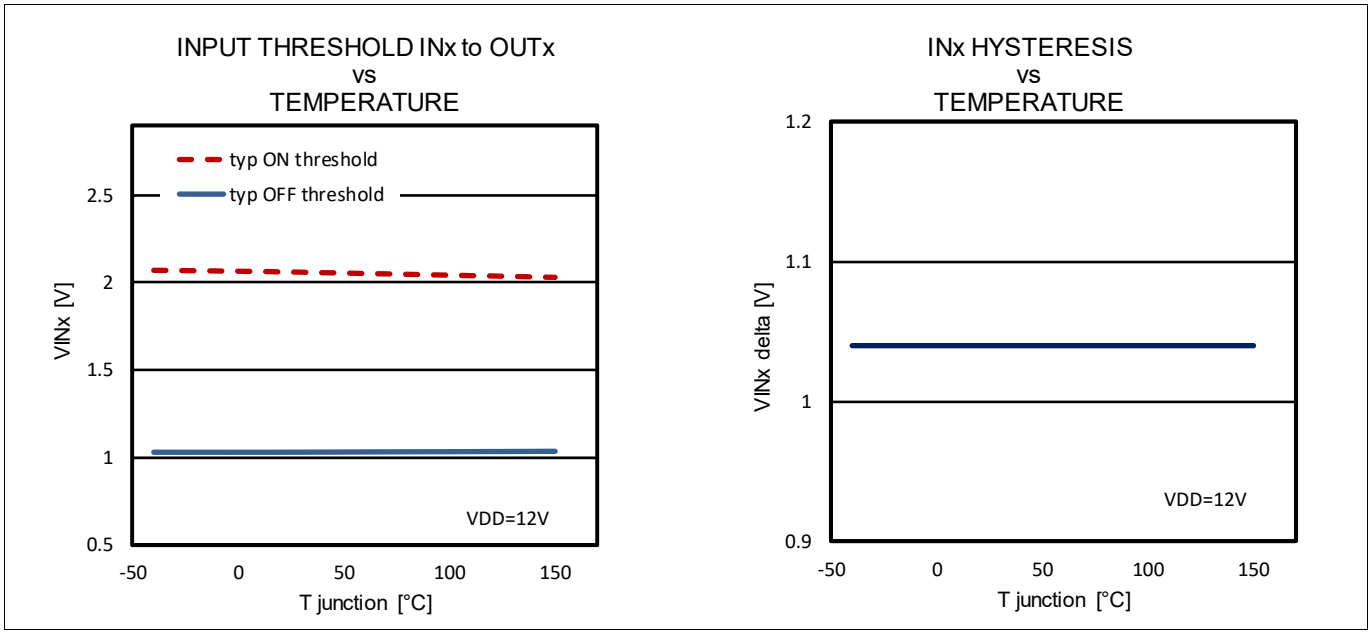


Figure 12 Input (INx) characteristic

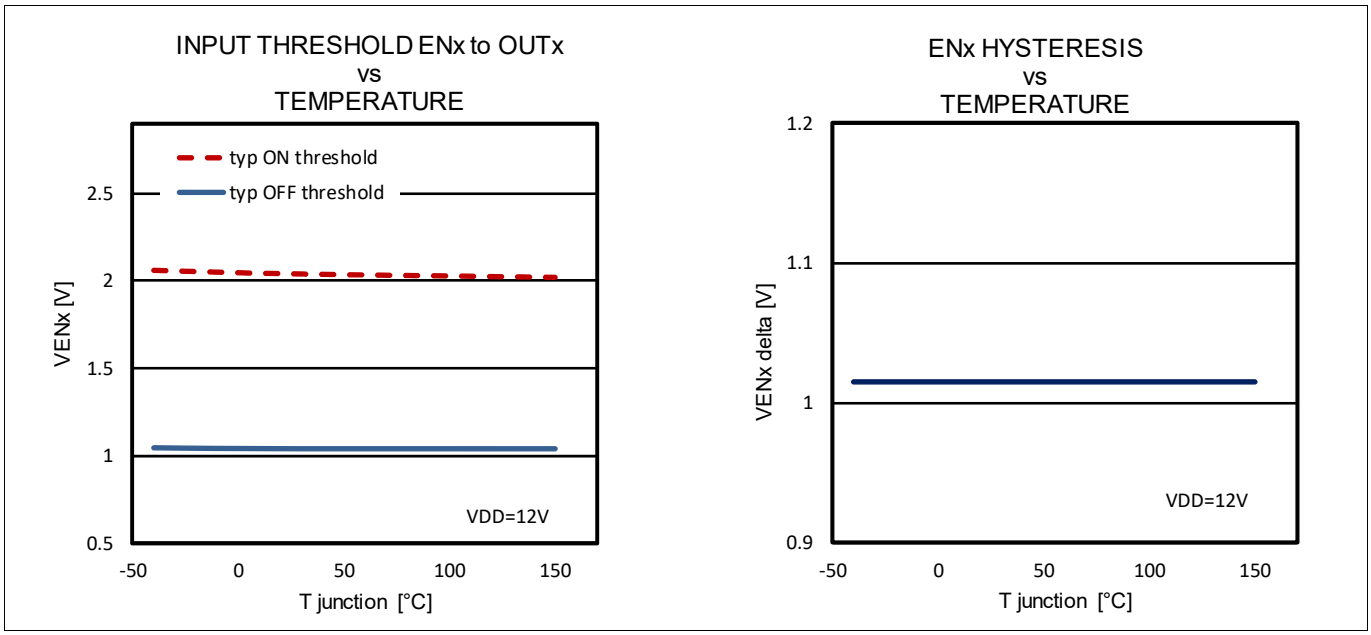


Figure 13 Input (ENx) characteristic

Typical Characteristics

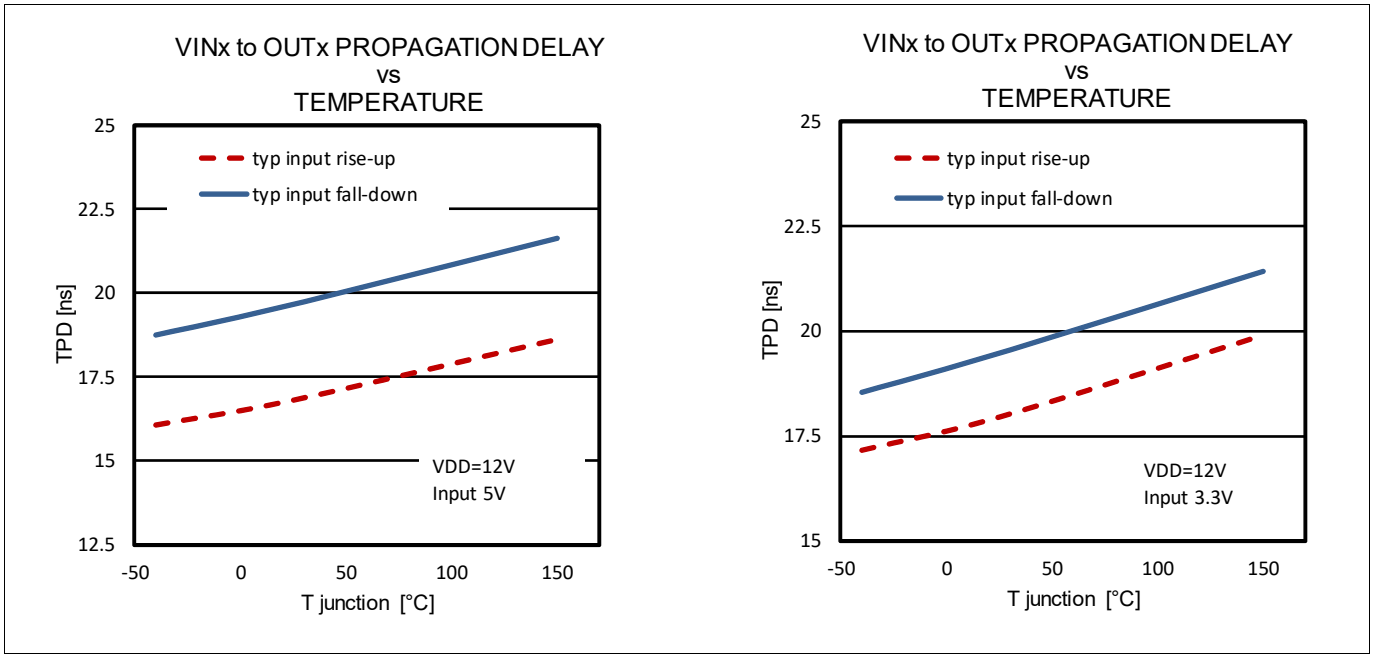


Figure 14 Propagation delay (INx) on different input logic levels (see Figure 6)

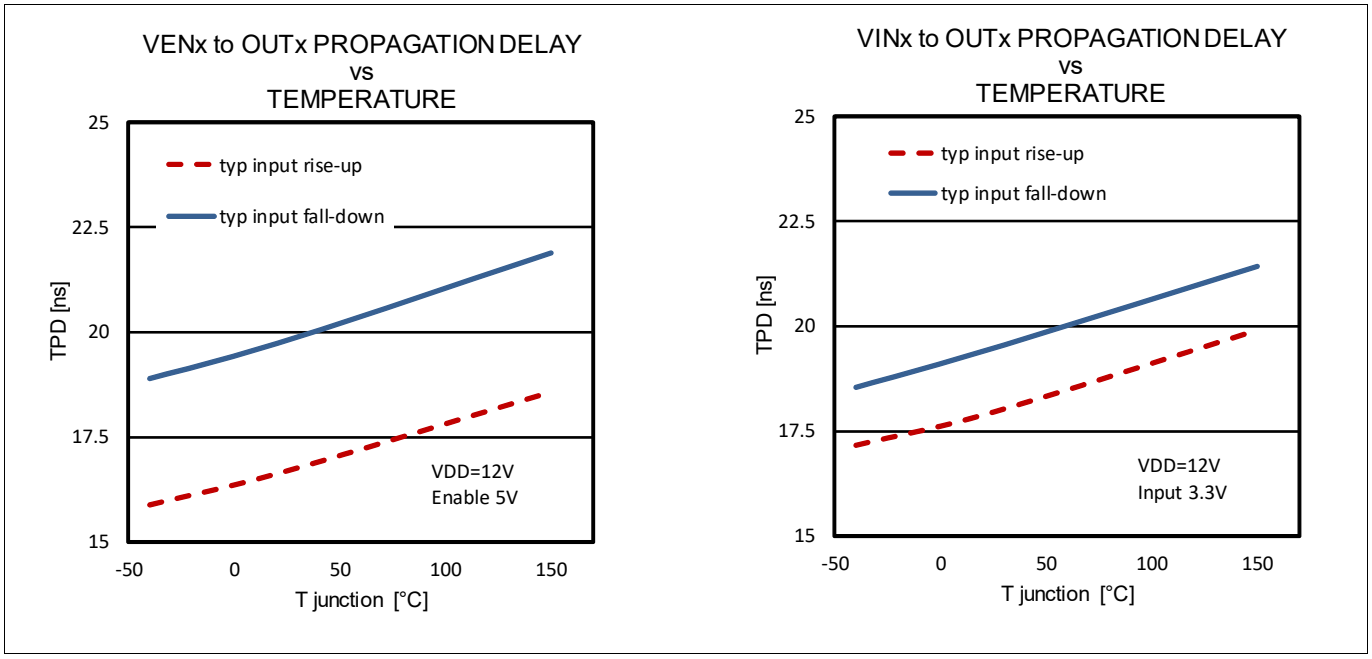


Figure 15 Propagation delay (ENx) on different input logic levels (see Figure 6)

Typical Characteristics

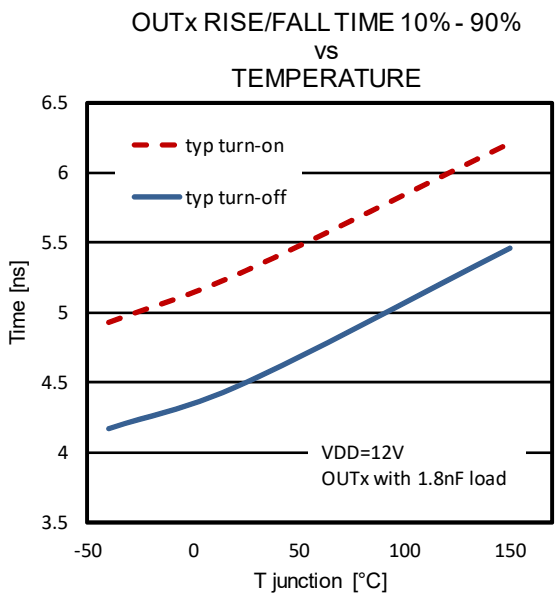


Figure 16 Rise / fall times with load on output (see Figure 6)

Typical Characteristics

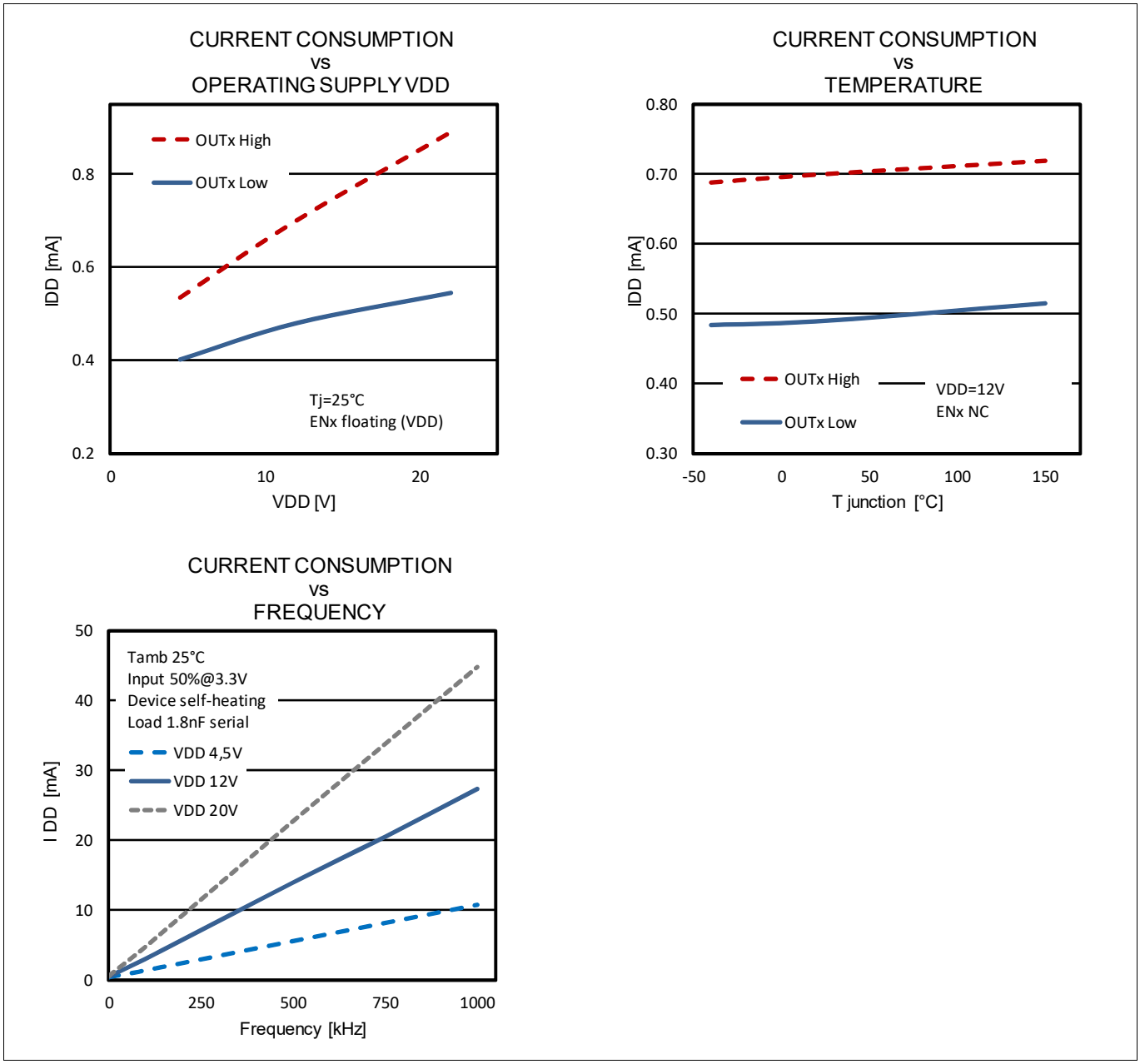


Figure 17 Power consumption related to temperature, supply voltage and frequency

Typical Characteristics

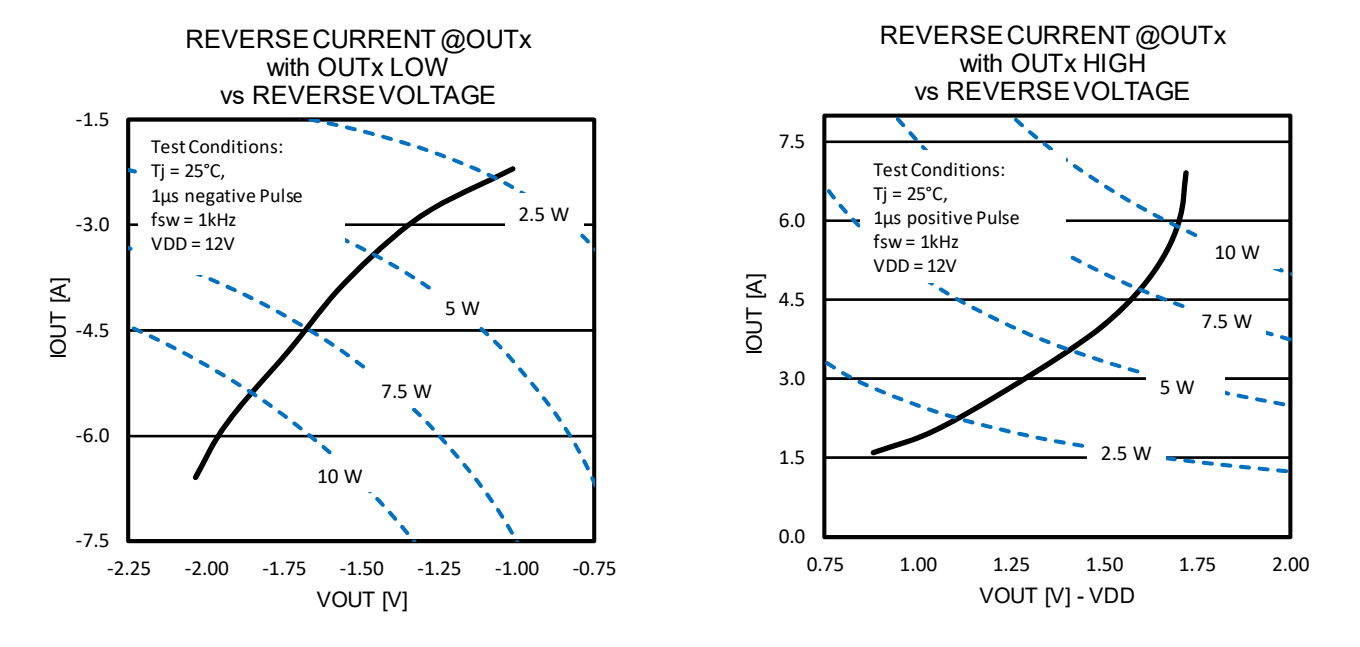


Figure 18 Output OUTx with reverse current and resulting power dissipation

8 Application Information

Note: The following information is given as a hint for the implementation of the device only and should not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

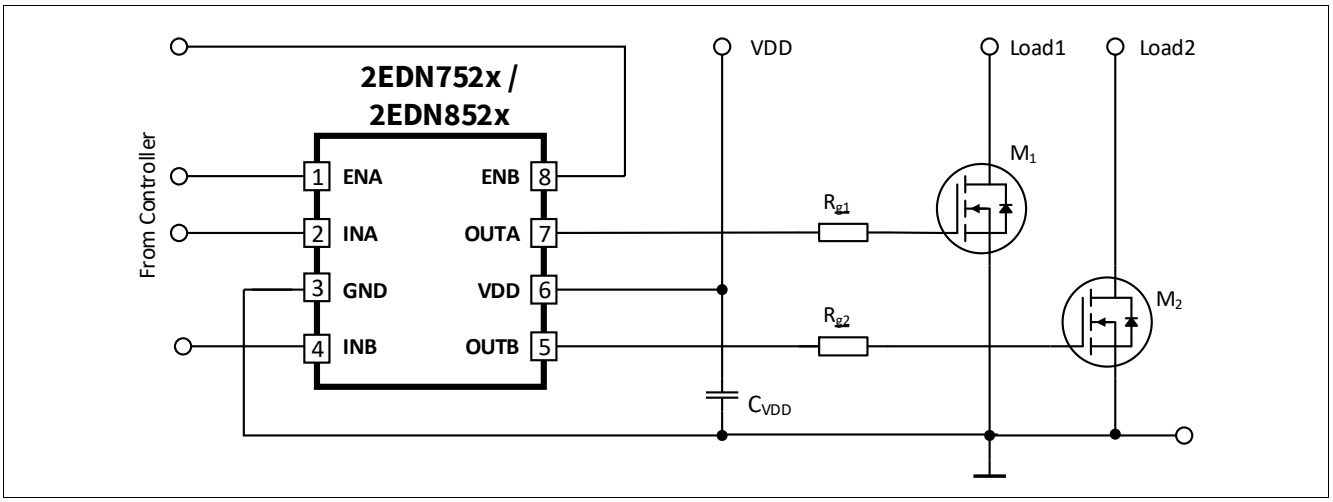


Figure 19 Typical application

The 2EDN752x/2EDN852x is a high-performance dual-channel driver designed for low-side switches. Each output channel can sink and source 5 A currents, thanks to its true rail-to-rail stage. This results in very low on-resistance values of 0.7 Ω up to the positive rail and 0.55 Ω down to the negative rail.

The tight channel-to-channel delay matching of 1 ns (typical) allows for parallel use of the two channels, providing a combined source and sink capability of 10 A. However, when using the channels in parallel mode, be aware that there may be differences in the input threshold voltage level between the two channels, which can cause delays and shoot-through in the output, especially when slow dV/dt input signals are used. To avoid cross-conduction currents in the device output stages, the rise and fall times of the input signals must be less than 100 ns (10 to 90 percent). This ensures optimal performance and reliability when using the 2EDN752x/2EDN852x dual-channel driver.

In the 2EDN752x/2EDN852x family, when the gate driver input is triggered, it generates an internal load current spike that disrupts the internal regulation supply. This internal supply controls the output switches, and its disturbance can exacerbate the shoot-through in each channel. When the intervals between input triggers are sufficiently large, the internal regulation supply can fully recover to its initial value, and the disturbance does not increase the shoot-through inside each channel. However, in implementations with very high input duty cycles, the intervals between input triggers become very small, and the disturbance of the internal regulation supply can cause ringing in the main supply.

Extra care is needed when driving the two input channels in parallel, as this increases the amount of disturbance in the internal supply and the amount of ringing on the internal VDD. This is why failures occur only at the extremes when transitioning the input signal duty cycle from low to high (and vice versa). To prevent these issues, ensure that the time between input triggers (rising or falling threshold) or the minimum input pulse width is more than 15 ns.

By adhering to these guidelines, you can optimize the performance and reliability of the 2EDN752x/2EDN852x dual-channel driver in your low-side switch applications.

8.1 Further application information

For further information you may contact **www.infineon.com/gate-driver**

9 Outline Dimensions

Note: For further information on package types, recommendation for board assembly, please go to: ***http://www.infineon.com/cms/en/product/technology/packages/****.*

9.1 PG-DSO-8

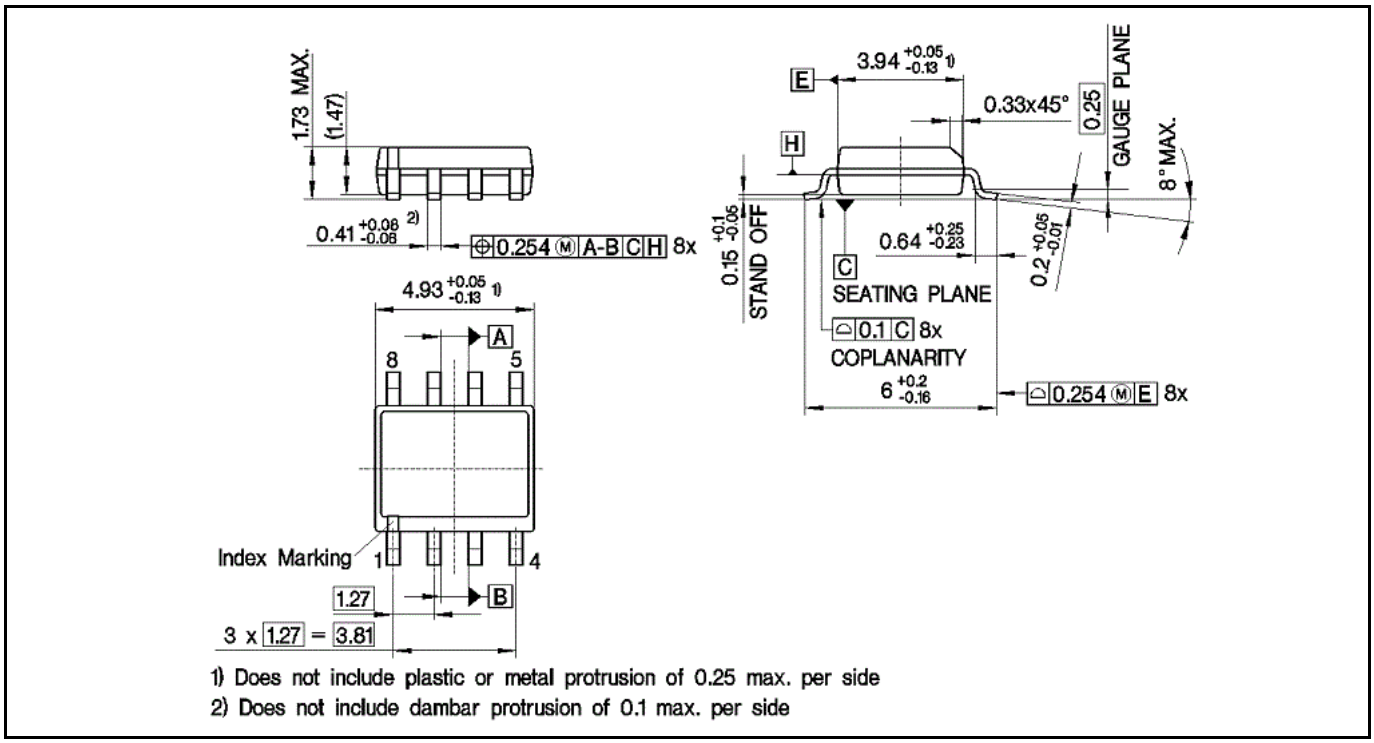


Figure 20 PG-DSO-8 outline

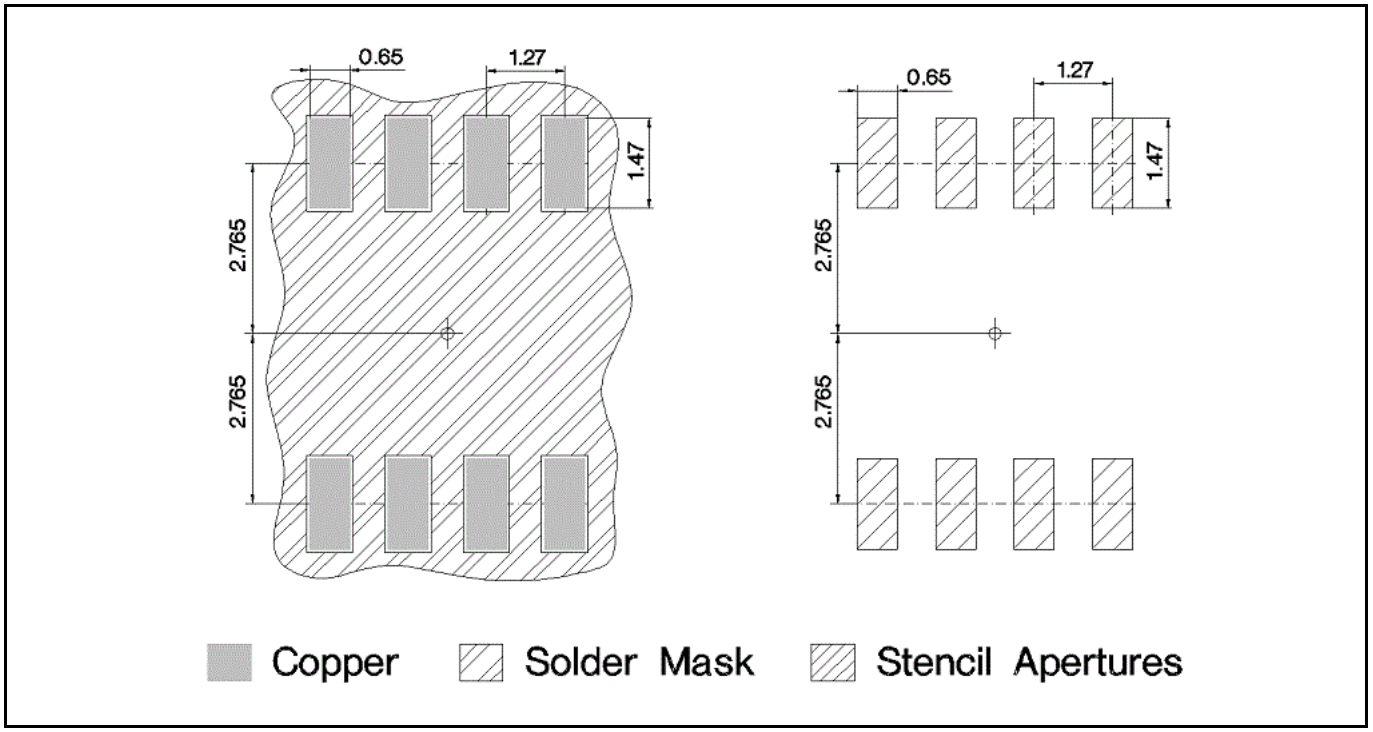


Figure 21 PG-DSO-8 footprint

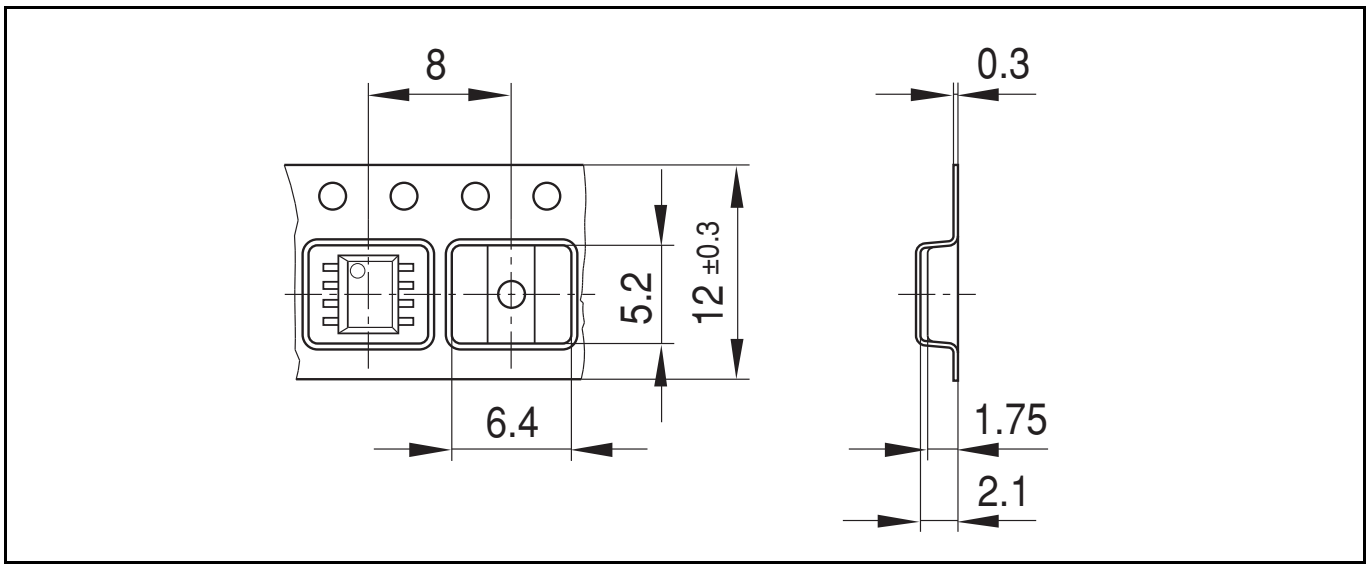


Figure 22 PG-DSO-8 packaging

9.2 PG-TSSOP-8

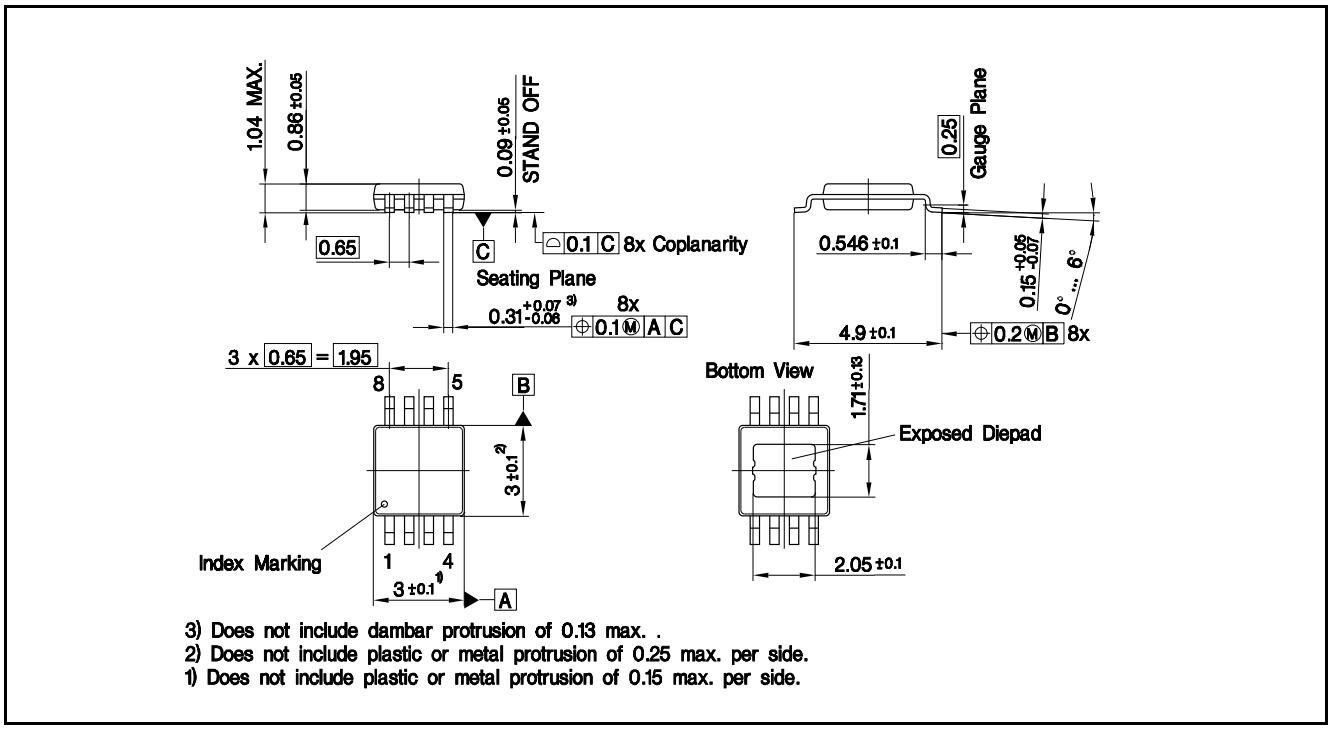


Figure 23 PG-TSSOP-8 outline

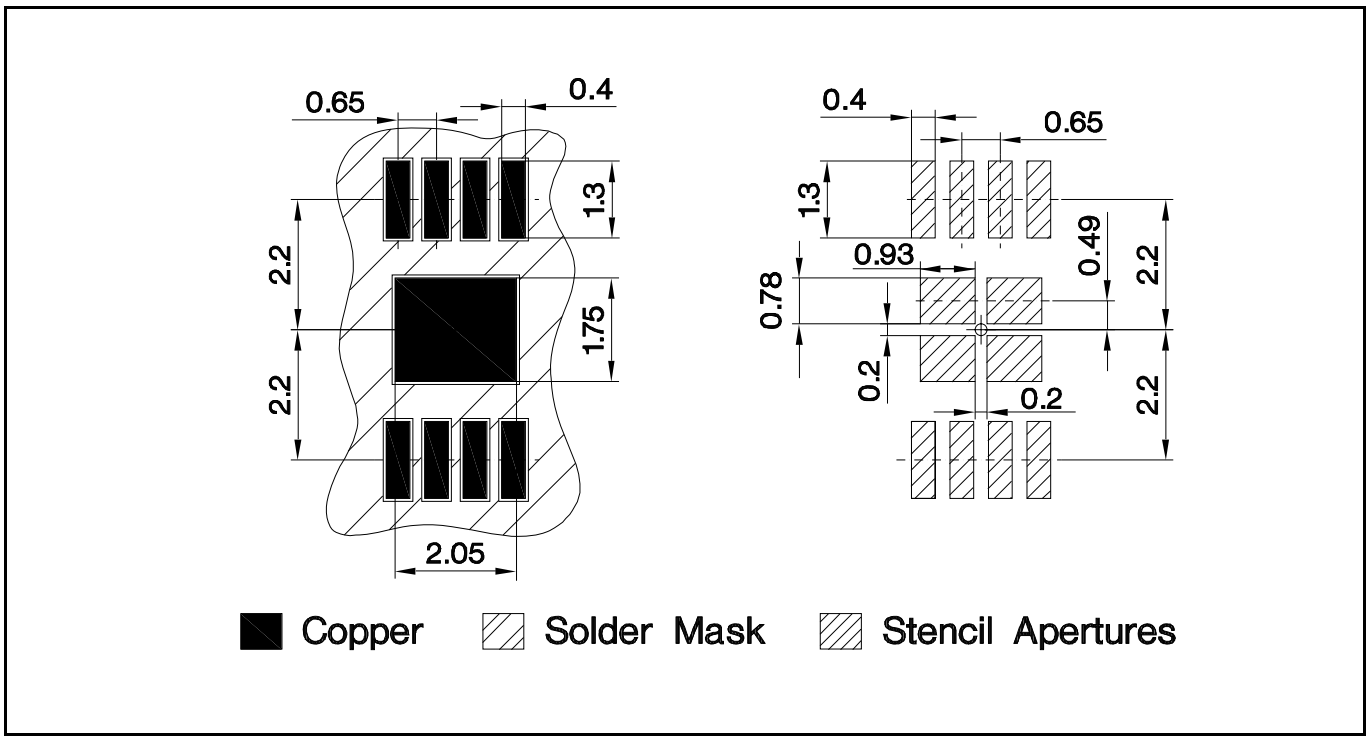


Figure 24 PG-TSSOP-8 footprint

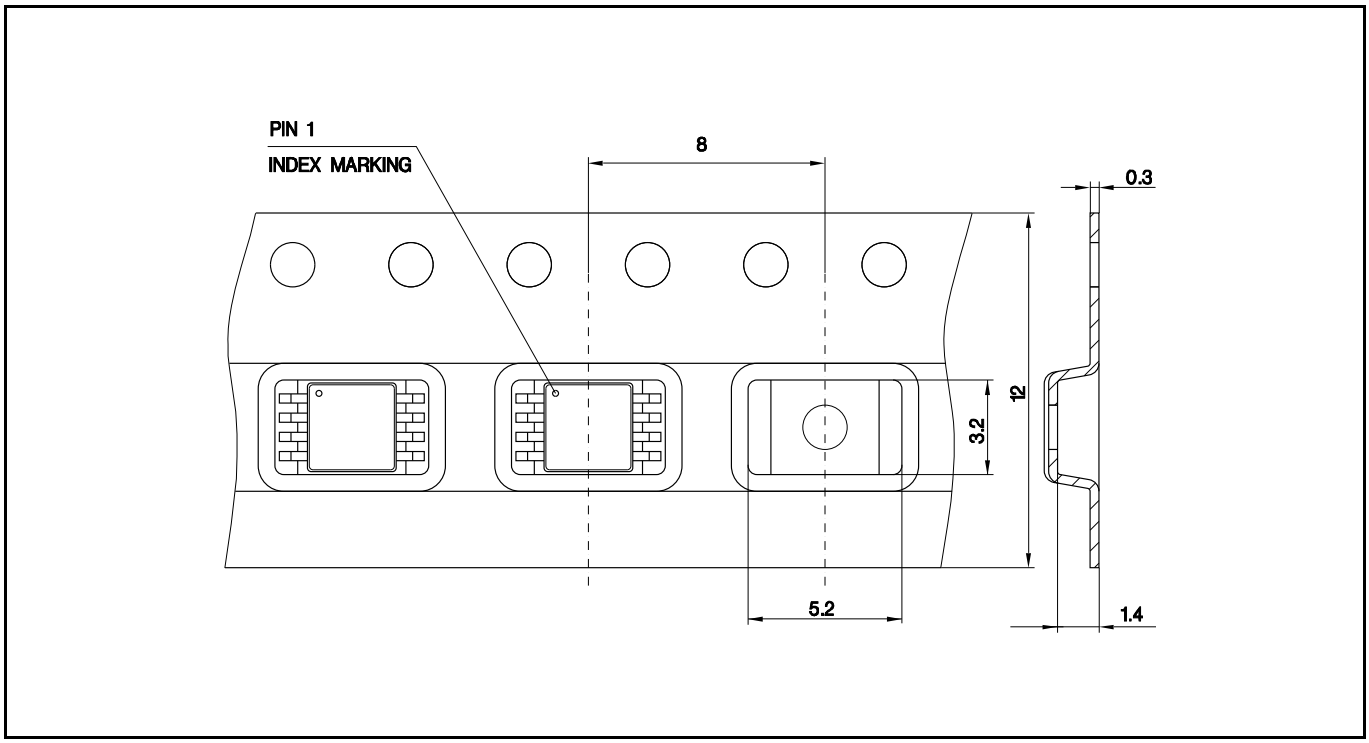


Figure 25 PG-TSSOP-8 packaging

9.3 PG-WSON-8

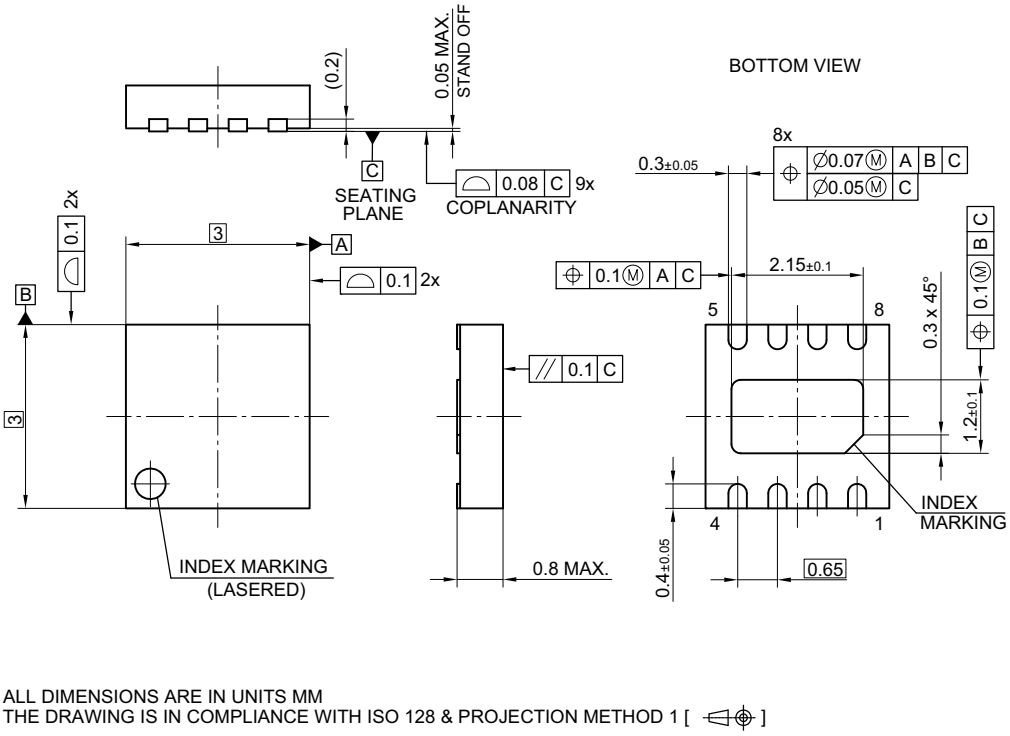


Figure 26 PG-WSON-8 outline

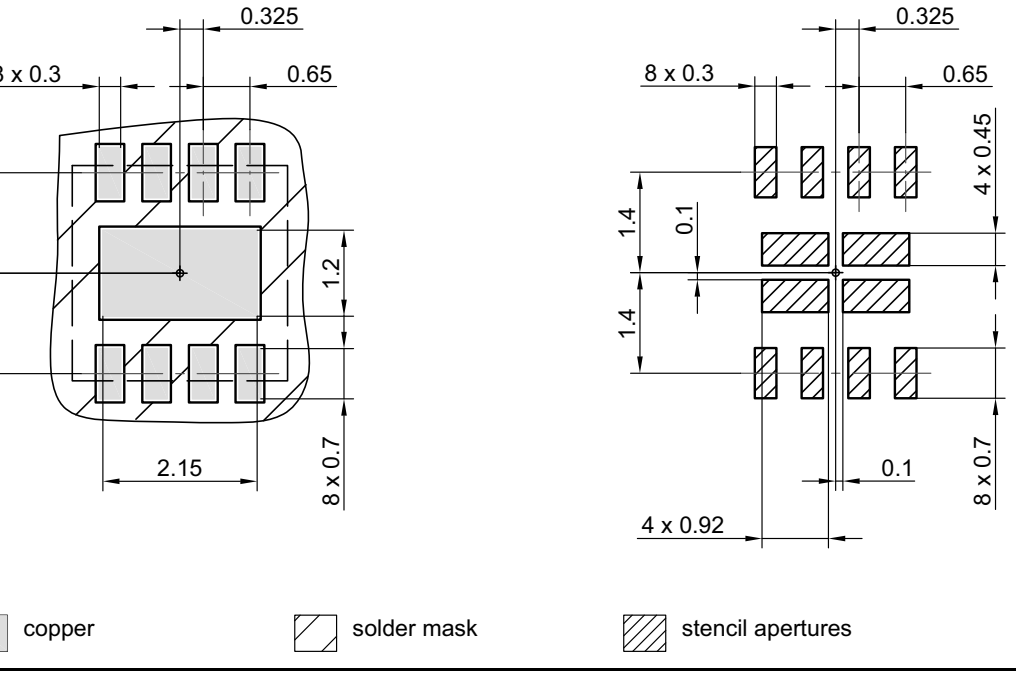


Figure 27 PG-WSON-8 footprint

Outline Dimensions

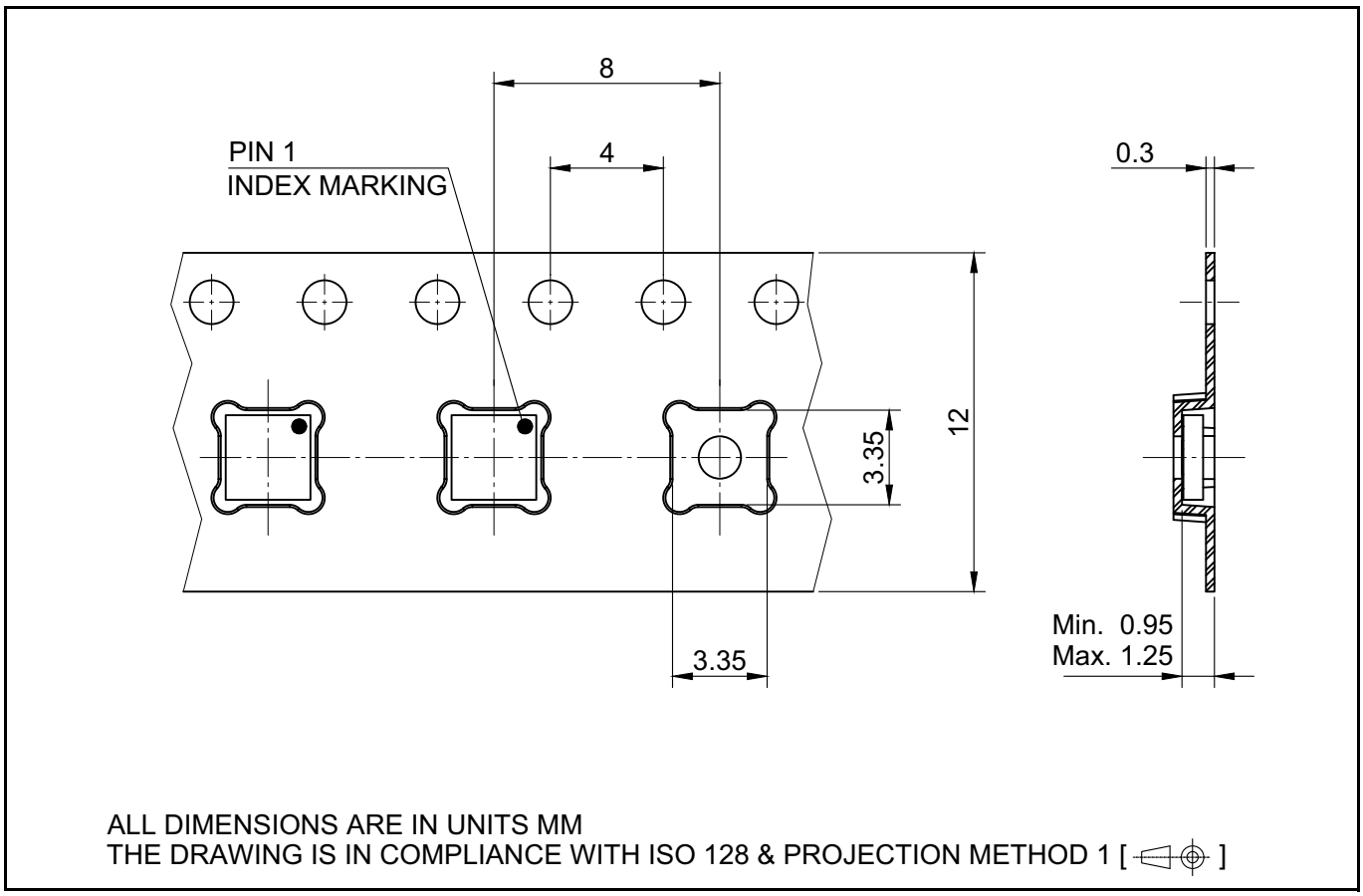


Figure 28 PG-WSON-8 packaging

10 Revision History

Revision	Date	Changes
Rev. 2.7	2025-03-18	Updated package name to suit standard in whole document **Table 14**: Updated Parameter “Minimum input pulse width that changes output state” **Table 14**: Updated to symbols of Dynamic Characteristics to comply with Standard International units for time → t **Chapter 8**: Added Application information
Rev. 2.6	2021-07-23	Updated packaging diagram **Figure 28** and package name for PG-WSON-8
Rev. 2.5	2018-04-20	Update package diagram for PG-WSON-8
Rev. 2.4	2017-08-18	Updated from Rev. 2.3. Correct typo (V_{OUT} [V] - V_{DD}) **Figure 18**. Add detail for test condition (V_{DD} = 12V) **Figure 18** Add min. voltage reference for OUTA, OUTB in reverse current condition. (Note 1) **Table 6**

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