EiceDRIVER™ 2EDL90xG3

120 V current sensing integrated common footprint gate driver for Si and GaN

Features

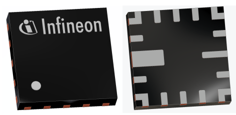
- Junction isolated dual-channel floating output driver
- 4 A source (Si) / 1.6 A source (GaN) output current capability
- 6 A sink output current capability
- Integrated bootstrap diode
- 5 V gate clamp for safe and optimal GaN driving
- 120 V absolute maximum voltage on HB and LB supplies (reference to GND)
- 3.3 V logic compliant PWM input
- 4 V to 16 V gate driver supply voltage (Si)
- 4 V to 13.2 V gate driver supply voltage (GaN)
- UVLO for HB, LB and VDD supplies
- 15 ns typical propagation delay
- 6 ns to 100 ns configurable deadtime or turn-on delay time
- Integrated current sense amplifier for DCR or shunt based current sensing
- Support wide range of power topologies: HVBuck, Hybrid SC, 3 levels Buck, HV Series Cap Buck, Switch Cap Converter, HBCD
- Specified from -40 °C to 125 °C operating junction temperature range
- Offered in TSNP-16 (3 mm x 3 mm)
- Lead free RoHS compliant package

Potential applications

- Intermediate bus converters for AI servers
- 48 V/ 54 V down conversion for datacom and telecom
- 800V / +/-400V LLC converters (secondary side)
- Multiphase interleaved buck converters (ILVB)
- Hybrid switched capacitor converters (HSCC)

Product validation

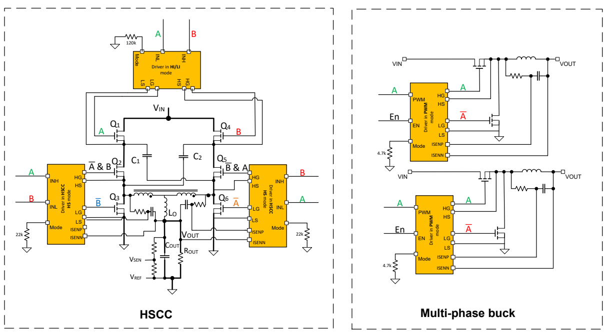
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.



Description

The 2EDL90xG3 gate driver is designed to drive dual high-side, dual low-side or half-bridge configurations of Si MOSFETs or enhancement mode GaN transistors. It offers two completely floating outputs gate drivers, especially useful for switched-capacitor and multi-level topologies. The floating high-side drivers are capable of driving a high-side MOSFET or GaN up to 120 V absolute maximum voltage. A 5 V gate clamp circuit is implemented for optimal GaN driving. The driver provides 5 configurable input modes(tri-state single PWM mode, HSCC HS mode, HSCC LS mode, Hi/Li inverted mode and Hi/Li mode), which can be selected by a simple pull down resistor. The inputs of the driver is 3.3 V logic compatible. The input stage can be directly connected to the microcontroller ground for maximizing signal integrity. Undervoltage lockout (UVLO) on the two floating output supplies forces the corresponding outputs low in case of insufficient supply. The driver is integrated with current sense amplifier with a common input voltage up to 35 V, which supports both DCR current sensing and shunt resistor current sensing. It is available in 16 pins 3 mm x 3 mm package.

Typical application diagram



Device information

Part number	Driver type
2EDL900G3	Si driver
2EDL901G3	GaN driver

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1 Block diagram

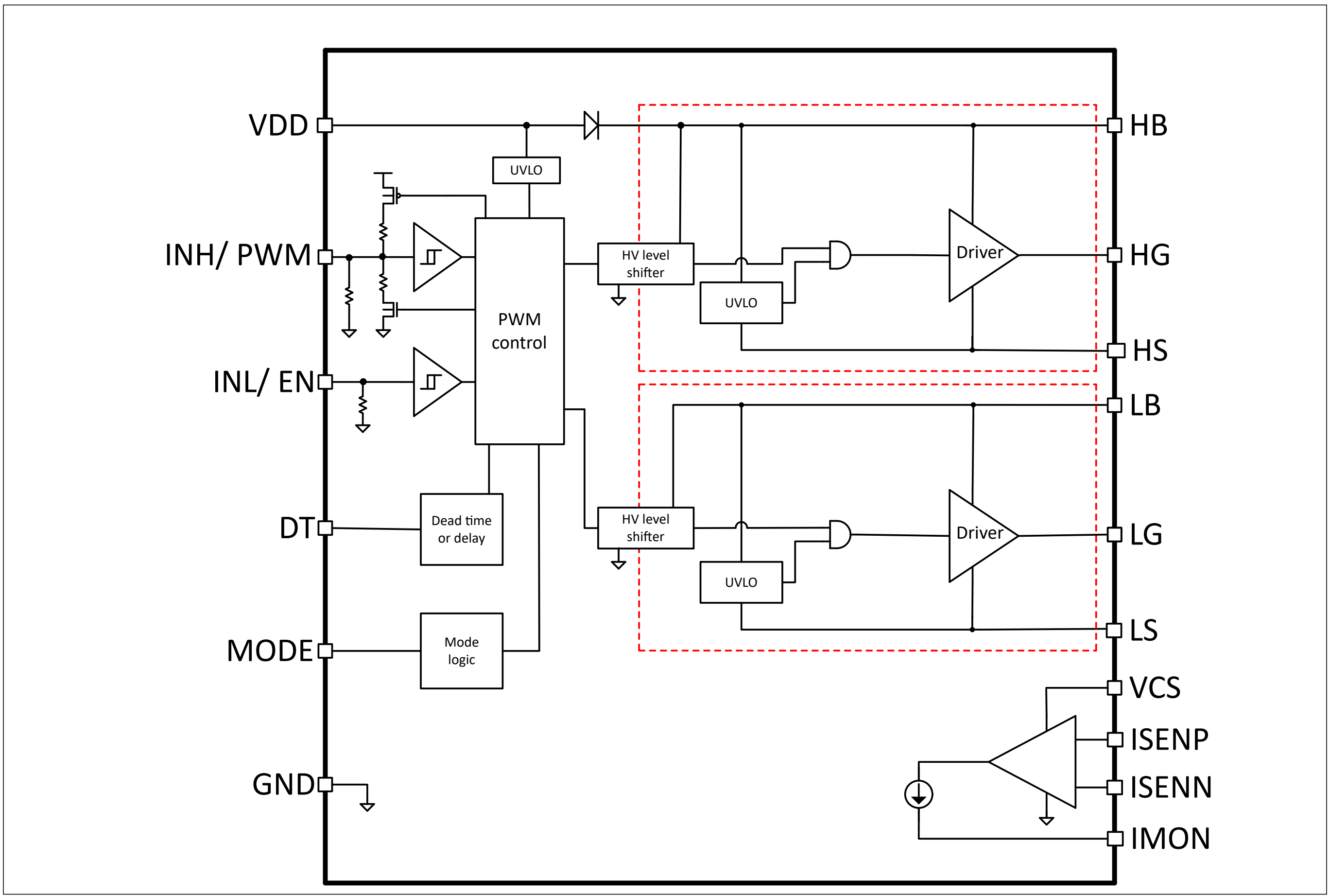

Figure 1 **Block Diagram 2EDL900G3**

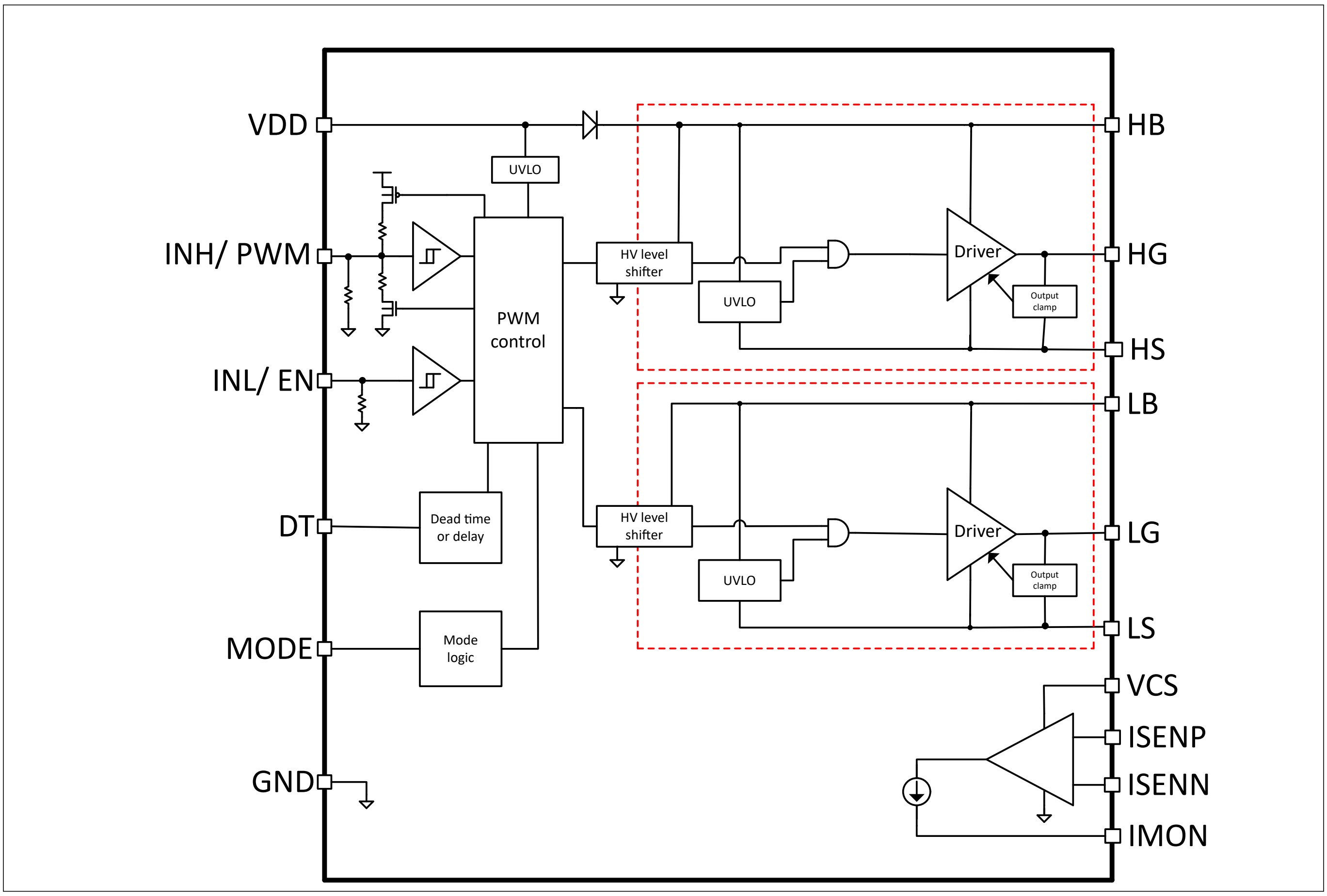

Figure 2 **Block Diagram 2EDL901G3**

2 Pin configuration

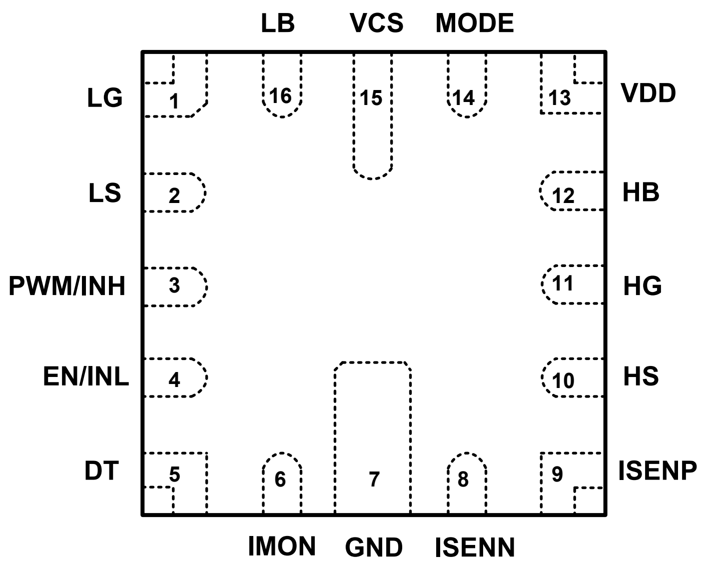

Figure 3 **2EDL90xG3 TSNP 3x3 (top view)**

Table 1 **Pin description of 2EDL90xG3**

Pin name	Pin #	Function
LG	1	Low side output drive to power switch gate
LS	2	Low side gate drive reference ground
INH/PWM	3	- Hi/Li input config: high side driver logic input - Single input config: PWM input
INL/EN	4	- Hi/Li input config: low side driver logic input - Single PWM input config: enable
DT	5	Programmable deadtime or turn on delay with pull down resistor - Deadtime configure for tri-state PWM mode - Turn on delay for Hi/Li mode and Hi/Li inverted mode - Deadtime configure for HSCC mode
IMON	6	Current reporting with inductor DCR sensing and shunt resistor sensing - Current type report
GND	7	Ground
ISENN	8	Inductor DCR current sense, negative input
ISENP	9	Inductor DCR current sense, positive input
HS	10	High side gate drive reference ground
HG	11	High side output drive to MOSFET gate
HB	12	High side (bootstrap) supply voltage, reference to HS pin
VDD	13	Analog input supply voltage

(table continues...)

Table 1 (continued) Pin description of 2EDL90xG3

Pin name	Pin #	Function
MODE	14	MODE configure with pull down resistor - Tri-state single PWM mode - HSCC HS mode - HSCC LS mode - Hi/Li inverted mode - Hi/Li mode
VCS	15	Power supply for current sensing amplifier
LB	16	Low side (bootstrap) supply voltage, reference to LS pin

3 Functional description

The 2EDL90xG3 gate driver is designed to drive dual high-side, dual low-side or half-bridge configurations of Si MOSFETs or enhancement mode GaN transistors. It offers two completely floating outputs gate drivers, especially useful for switched-capacitor and multi-level topologies. The floating high-side drivers are capable of driving a high-side MOSFET or GaN up to 120 V absolute maximum voltage. A 5 V gate clamper circuit is implemented for optimal GaN driving. The driver provides 5 configurable input modes(tri-state single PWM mode, HSCC HS mode, HSCC LS mode, Hi/Li inverted mode and Hi/Li mode), which can be selected by a simple pull down resistor. The inputs of the driver is 3.3 V logic compatible. The input stage can be directly connected to the microcontroller ground for maximizing signal integrity. Undervoltage lockout (UVLO) on the two floating output supplies forces the corresponding outputs low in case of insufficient supply. The driver is integrated with current sense amplifier with a common input voltage up to 35 V, which supports both DCR current sensing and shunt resistor current sensing. It is available in 16 pins 3 mm x 3 mm package.

The following sections describe the key functionalities.

The 2EDL90xG3 provides 5 configurable input modes by a simple pull down resistor on MODE pin. Connecting capacitor to the MODE pin must be avoided.

Table 2 Input mode selection

Mode name	Conditions on the MODE pin	Tri-state pull-up & pull-down resistors	Configurable deadtime or turn-on delay
Tri-state single PWM mode	<13.2 kΩ	Enabled	Deadtime
HSCC HS mode	20 kΩ - 25 kΩ	Enabled	Deadtime
HSCC LS mode	37.5 kΩ - 42.5 kΩ	Enabled	Deadtime
Hi/Li inverted mode	63.75 kΩ - 68.75 kΩ	Disabled	Turn-on delay
Hi/Li mode	>105 kΩ	Disabled	Turn-on delay

The deadtime in PWM mode or HSCC modes and the turn-on delay in Hi/ Li mode or Hi/ Li inverted mode can be configured by a pull-down resistor on DT pin, which is set with the equation of t_{dt} [ns] = 0.5 x R_{DT} [kΩ] + 2 ns. The configurable deadtime or turn-on delay time is in the range of 6 ns to 102 ns. It is recommended to use the resistor with 1% accuracy in the range of 8 kΩ to 200 kΩ and to place the resistor close to the DT pin. Connecting capacitor to the DT pin must be avoided.

Note: If $R_{DT} < 1.5$ kΩ, the deadtime/ delay generation block is bypassed, which means 0 ns deadtime/ delay is set. If $R_{DT} > 300$ kΩ, LG = HG = 0.

In Hi/Li input mode, the 2EDL90xG3 device responds independently to the two inputs signals (INH and INL) according to the following truth table.

INH	INL	HG	LG
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

The input pull-down resistance has a value of 200 kΩ typical on INH pin and INL pin. The pull-down resistor on DT pin sets the turn-on delay of the two output channels.

In Hi/Li inverted input mode, the 2EDL90xG3 device responds independently to the two inputs signals (INH and INL) according to the following truth table.

INH	INL	HG	LG

0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	0

The input pull-down resistance has a value of 200 kΩ typical on INH pin and INL pin. The pull-down resistor on DT pin sets the turn-on delay of the two output channels.

In HSCC HS mode shown in HSCC HS configuration, the 2EDL90xG3 device responds to the two inputs signals (INH and INL) according to the following truth table.

INH	INL	HG	LG
0	0	0	1
0	1	1	0
High-Z	x	0	0
1	0	0	1
1	1	0	0

The input pull-down resistance has a value of 200 kΩ typical on INH pin and INL pin. Additionally, the tri-state buffer and 10 kΩ pull-up and pull-down resistors on INH pin are activated in HSCC HS mode. The pull-down resistor on DT pin sets the deadtime between the two output channels.

Note: in HSCC HS mode, if the duty cycle is more than 50% and the overlapping time of INL and INH is more than the deadtime, the overlapping time is used as deadtime.

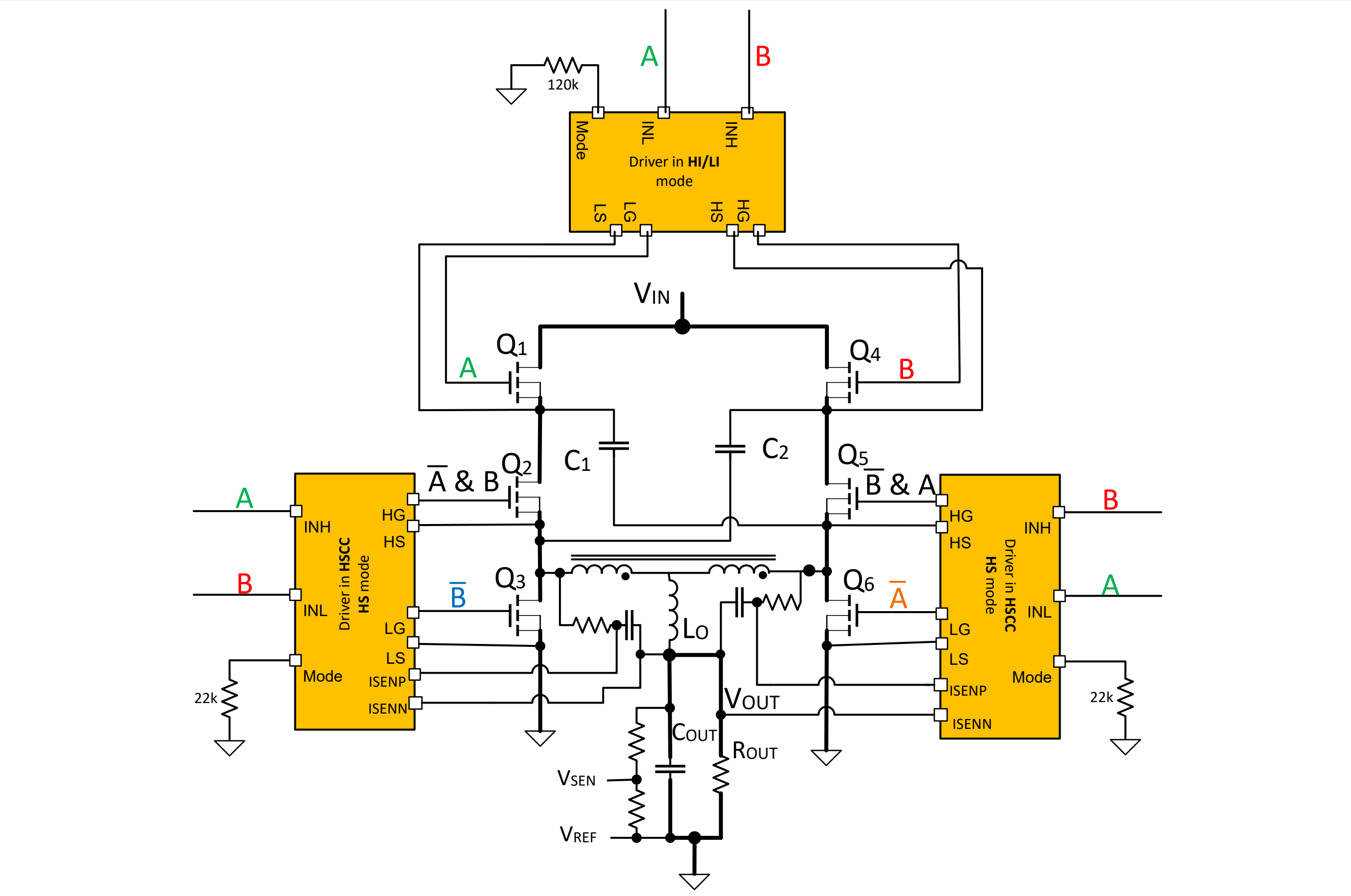

Figure 4 **HSCC HS configuration**

In HSCC LS mode shown in HSCC LS configuration, the 2EDL90xG3 device responds to the two inputs signals (INH and INL) according to the following truth table.

INH	INL	HG	LG
0	0	0	0
0	1	0	1
High-Z	x	0	0
1	0	1	0
1	1	1	0

The input pull-down resistance has a value of 200 kΩ typical on INH pin and INL pin. Additionally, the tri-state buffer and 10 kΩ pull-up and pull-down resistors on INH pin are activated in HSCC LS mode. The pull-down resistor on DT pin sets the deadtime between the two output channels.

Note: In HSCC LS mode, if the duty cycle is more than 50% and the overlapping time of INL and INH is more than the deadtime, the overlapping time is used as deadtime.

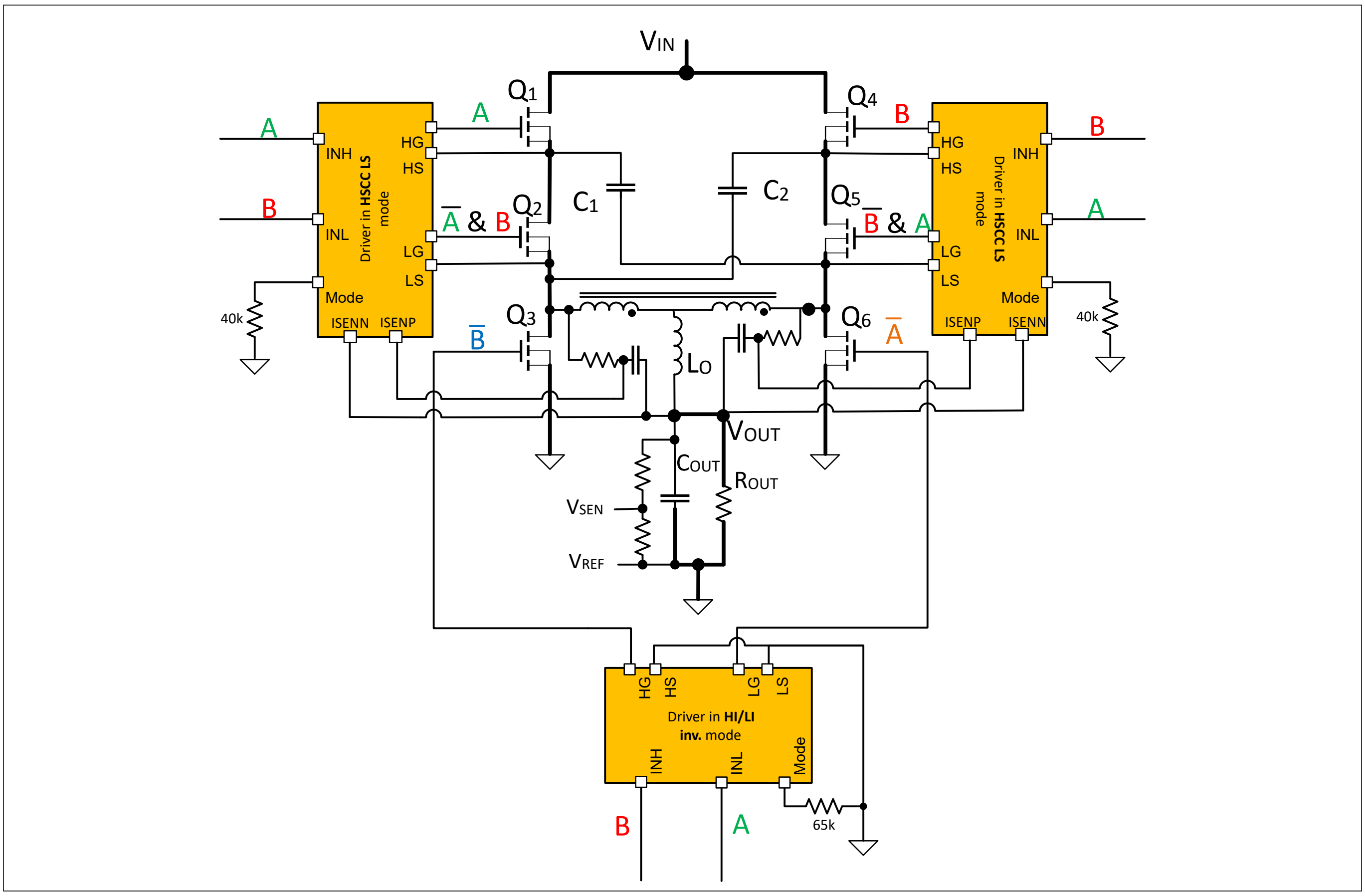

Figure 5 **HSCC LS configuration**

In tri-state single PWM mode shown in Tri-state single PWM configuration, the 2EDL90xG3 device responds independently to the two inputs signals (PWM and EN) according to the following truth table.

EN	PWM	HG	LG
0	0	0	0
0	1	0	0
0	High-Z	0	0
1	0	0	1
1	1	1	0
1	High-Z	0	0

The input pull-down resistance has a value of 200 kΩ typical on PWM pin and EN pin. Additionally, the tri-state buffer and 10 kΩ pull-up and pull-down resistors on PWM pin are activated in tri-state single PWM mode. The pull-down resistor on DT pin sets the deadtime between the two output channels.

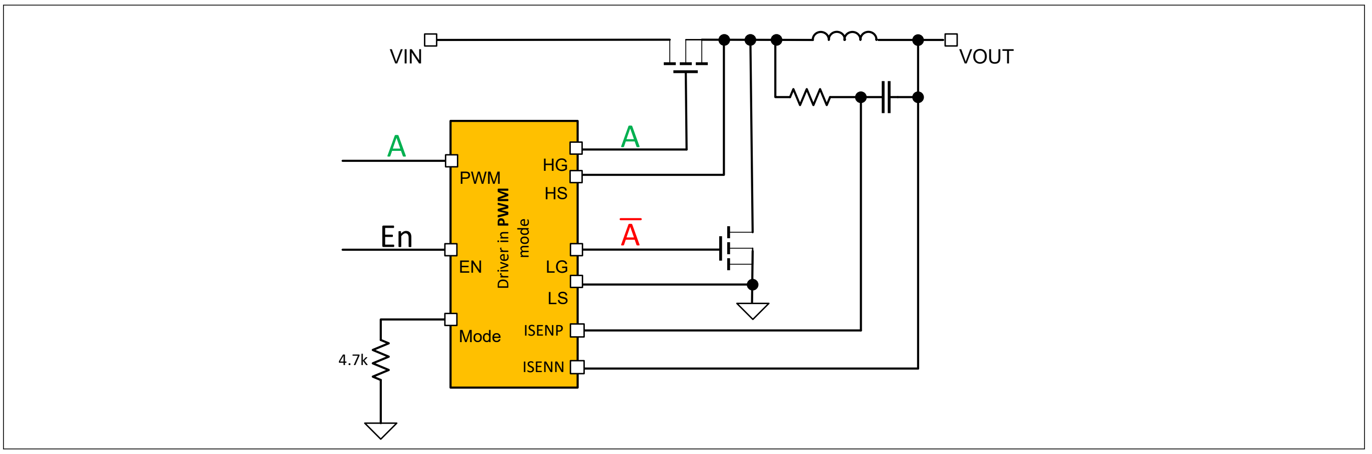

Figure 6 **Tri-state single PWM configuration**

Undervoltage lockout (UVLO)

The UVLO function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO rising threshold voltage. Thus it ensures that the power MOSFET is not switched on if the driving voltage is too low to completely switch on the device, thereby avoiding excessive power dissipation. The UVLO level is set to a typical value of 3.8 V with 0.2 V hysteresis for supply voltage (V_{HB-HS} and V_{LB-LS}) .

Current sense amplifier

The current sense amplifier is intended to sense the voltage across a low ohmic shunt resistor or across the RC network installed across an output inductor. For inductor DCR based current sensing shown in Inductor DCR current sensing, the RC network must be tuned to the same time constant as the L/DCR time constant, the voltage across the capacitor is then proportional to the current through the inductor. The current sense amplifier is configured as unity gain. With the external RSEN resistor, the sensing current gain is set by the DCR/RSEN. The reporting current IMON = IL * (DCR/RSEN), which can be transmitted to the digital controller. For shunt resistor based current sensing shown in Shunt resistor current sensing, the reporting current IMON = I * (RSHUNT/RSEN). For both Inductor DCR current sensing and Shunt resistor current sensing, it is recommended to use 1.2V V_{REF}. Typically, the V_{REF} supply comes from the controller or external supply. In order to measure the positive and negative current, the V_{REF} supply must have both source and sink capability. The Rs resistor together with the V_{REF} supply convert the IMON current to the voltage which is read by the controller. In order to filter out certain amount of switching noise, it is recommended to place a low pass filter capacitor C_F between IMON pin and Rs resistor.

Please connect VCS, ISENP, ISENN and IMON to GND if the current sense amplifier is not used.

Note: VCS supply must be always higher than ISENP and ISENN during power up and power down.

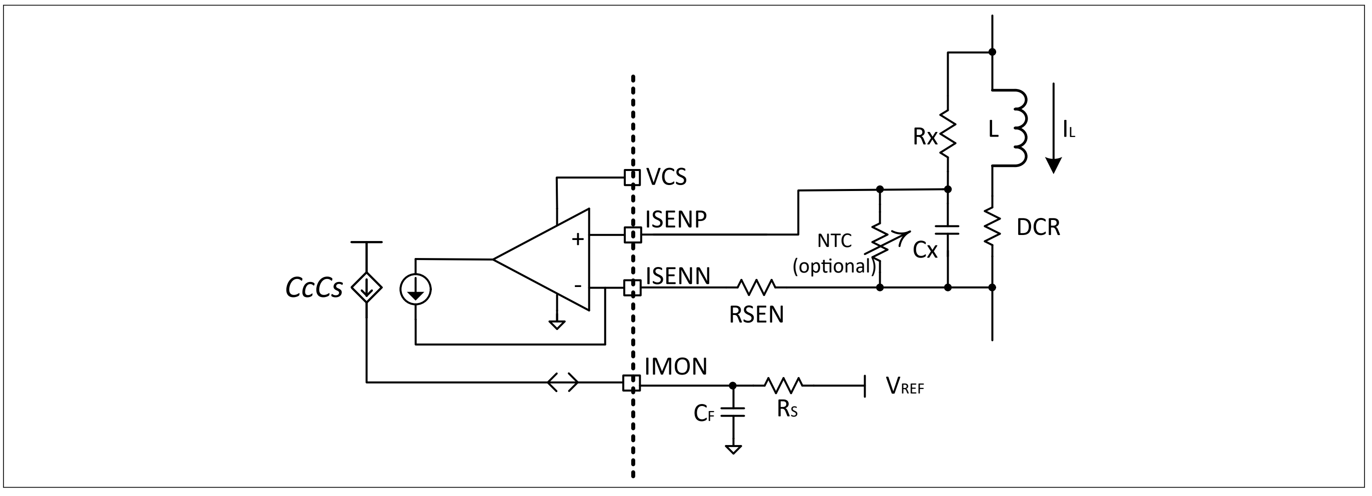

Figure 7 **Inductor DCR current sensing**

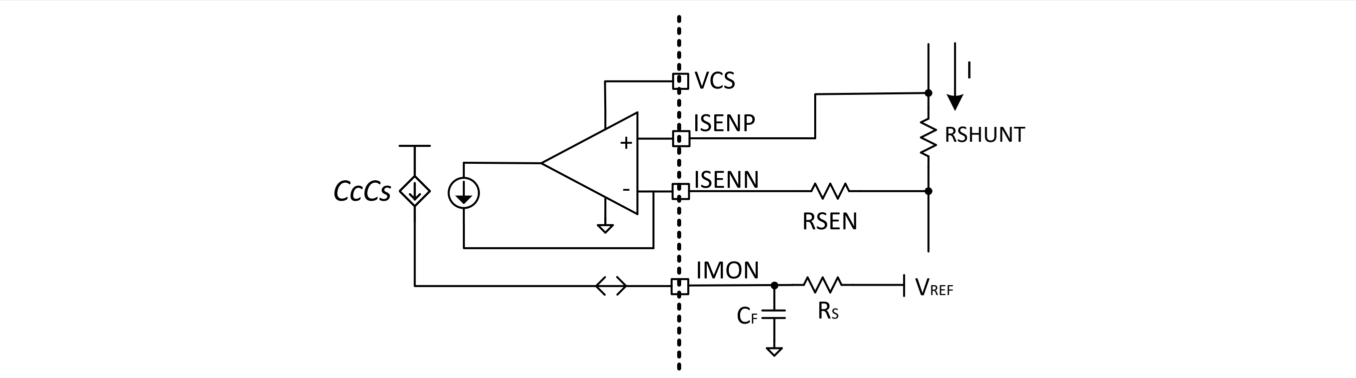

Figure 8 Shunt resistor current sensing

4 General product characteristics

4.1 Absolute maximum ratings

Table 3 Absolute Maximum Ratings

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. All voltage parameters are referenced to GND unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD input supply voltage (Si)	V_{DD}	-0.3	–	17	V	
VDD input supply voltage (GaN)	V_{DD}	-0.3	-	13.5	V	
Floating output supply voltage (Si)	V_{HB-HS}, V_{LB-LS}	-0.3	–	17	V	Referenced to V_{HS} and V_{LS}
Floating output supply voltage (GaN)	V_{HB-HS}, V_{LB-LS}	-0.3	-	13.5	V	Referenced to V_{HS} and V_{LS}
HB and LB voltage	V_{HB}, V_{LB}	-0.3	–	120	V	25 °C to 150 °C [1)]
HB and LB voltage	V_{HB}, V_{LB}	-0.3	-	105	V	-40 °C to 150 °C [1)]
HS and LS voltage	V_{HS}, V_{LS}	-5	–	V_{HB} + 0.3 V_{LB} + 0.3	V	
HS and LS voltage (Repetitive pulse)	V_{HS}, V_{LS}	V_{HB} - 17 V_{LB} - 17	–	V_{HB} + 0.3 V_{LB} + 0.3	V	< 100 ns [2)]
INH, INL, DT input voltage	V_{INH}, V_{INL}, V_{DT}	-0.3	–	4	V	
Output voltage on HG	V_{HG}	V_{HS} - 0.3	–	V_{HB} + 0.3	V	Referenced to V_{HS}
Output voltage on HG (Repetitive pulse)	V_{HG}	V_{HS} - 2	–	V_{HB} + 0.3	V	Referenced to V_{HS}, < 100 ns [2)]

(table continues...)

Table 3 (continued) Absolute Maximum Ratings

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. All voltage parameters are referenced to GND unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output voltage on LG	V_{LG}	V_{LS} - 0.3	–	V_{LB} + 0.3	V	Referenced to V_{LS}
Output voltage on LG (Repetitive pulse)	V_{LG}	V_{LS} - 2	–	V_{LB} + 0.3	V	Referenced to V_{LS}, < 100 ns [2]
VCS input supply voltage	V_{CS}	-0.3		70	V	CSA power supply
MODE input voltage	V_{MO}	-0.3	–	3.6	V	
ISENN, ISENP voltage	V_{SN} V_{SP}	-0.3	–	41	V	
ISENP - ISENN voltage	V_{DIF_ISEN}	-3.6		3.6	V	
IMON voltage	V_{IMON}	-0.3	–	3.6	V	
Peak reverse current on HG and LG	I_{OR}	–	–	5	A	[2] [3]
Input current on INH and INL	I_{INH}, I_{INL}	-40	-	100	mA	V_{DD} =15 V
Operating junction temperature	T_J	-40	–	150	°C	
Storage temperature	T_S	-55	–	150	ºC	

1) Verified with VDD supplied within the recommended operating voltage range.
2) Not subject to production test. Verified by design/characterization.
3) For < 500 ns pulses.

4.2 ESD ratings

Table 4 ESD ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HBM	V_{ESD_HBM}	-1	-	1	kV	According to ANSI/ESDA/JEDEC specification JS-001
CDM	V_{ESD_CDM}	-500	-	500	V	According to ANSI/ESDA/JEDEC specification JS-002

4.3 Recommended operating conditions

Table 5 Recommended Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to V_{GND} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDD input supply voltage(Si)	V_{DDI}	4	–	15	V	
VDD input supply voltage(GaN)	V_{DD}	4	–	13.2	V	
VCS input supply voltage	V_{CS}	5V + V_{ISENP} / V_{ISENN}	–	65	V	CSA power supply. VCS supply must be always higher than V_{ISENP} / V_{ISENN} during power up and power down.
Floating supply voltage(Si)	V_{HB-HS}, V_{LB-LS}	4	-	16	V	Referenced to V_{HS} and V_{LS}
Floating supply voltage(GaN)	V_{HB-HS}, V_{LB-LS}	4	-	13.2	V	Referenced to V_{HS} and V_{LS}
HB and LB voltage	V_{HB}, V_{LB}	V_{HS} + 4 V_{LS} + 4 V_{GND} + 2	–	V_{HS} + 16 V_{LS} + 16	V	Referenced to GND
HS and LS voltage	V_{HS}, V_{LS}	-2	–	100	V	Referenced to GND

(table continues...)

Table 5 (continued) Recommended Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to V_{GND} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HS and LS voltage (Repetitive pulse)	V_{HS}, V_{LS}	V_{HB} -16 V_{LB} -16	–	100	V	< 100 ns
INH, INL, DT input voltage	V_{INH}, V_{INL}, V_{DT}	0	–	3.6	V	
MODE input voltage	V_{MO}	0	–	3	V	
Output voltage on HG (Si)	V_{HG}	0	–	16	V	Referenced to V_{HS}
Output voltage on HG (GaN)	V_{HG}	0	–	5.5	V	Referenced to V_{HS}
Output voltage on LG (Si)	V_{LG}	0	–	16	V	Referenced to V_{LS}
Output voltage on LG (GaN)	V_{LG}	0	–	5.5	V	Referenced to V_{LS}
ISENN, ISENP voltage	V_{SN} V_{SP}	0	–	35	V	
IMON voltage	V_{IMON}	0	–	2.7	V	
HS and LS slew rate	dV_{HS}/dt , dV_{LS}/dt	–	–	50	V/ns	
Junction temperature range	T_J	-40	–	125	°C	

4.4 Thermal characteristics

Table 6 Thermal mechanical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction-to-case (bottom) thermal resistance	R_{thJC_B}	-	21	-	°C/W	1) 2)

(table continues...)

Table 6 (continued) Thermal mechanical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction-to-case (top) thermal resistance	R_{thJC_T}	-	34	-	°C/W	[1] [2]
Junction-to-ambient thermal resistance	R_{thJA}	-	74	-	°C/W	Device soldered on PCB [1] [2]
Junction-to-board thermal resistance	R_{thJB}	-	15.6	-	°C/W	Device soldered on PCB [1] [2]

1) Not subject to production test, specified by design.
2) Specified value is according to Jedec JESD51-5 /-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu).

4.5 Electrical characteristics

Table 7 Electrical characteristics

Unless otherwise specified: $V_{DD} = V_{HB} = V_{LB} = 6$ V, $V_{HS} = V_{LS} = V_{GND} = 0$ V, Hi/ Li mode. The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current						
VDD quiescent current	I_{VDDQ1}	-	3.5		mA	V_{INH} and V_{INL} = 0 V, with $R_{\_DTC}$ = GND, Hi/ Li mode, V_{SENP}=5V(common mode), V_{SENP} -V_{SENN}=0 mV, V_{CS}=48 V
VCS quiescent current	I_{VCSQ}	-	900	-	uA	V_{CS} = 48 V, V_{SENP} - V_{SENN} = 10 mV
VDD operating current	I_{VDDO}	-	3.8	5	mA	F_{SW} = 500 kHz, C_{LOAD} = 0 nF, with $R_{\_DTC}$ = low, PWM mode, V_{SENP} -V_{SENN}=10 mV
HB quiescent current(Si)	I_{VHB}	-	75		uA	V_{INH} and V_{INL} = 0 V
HB quiescent current(GaN)	I_{VHB}	-	180	-	uA	V_{INH} and V_{INL} = 0 V
HB operating current(Si)	I_{VHBO}	-	2		mA	V_{INL} = 0V, V_{INH} at F_{SW} = 500 kHz, V_{LB} = 0V, C_{LOAD} = 0 nF
HB operating current(GaN)	I_{VHBO}	-	17		mA	V_{INL} = 0V, V_{INH} at F_{SW} = 500 kHz, V_{LB} = 0V, C_{LOAD} = 5 nF

(table continues...)

Table 7 (continued) Electrical characteristics

Unless otherwise specified: $V_{DD} = V_{HB} = V_{LB} = 6$ V, $V_{HS} = V_{LS} = V_{GND} = 0$ V, Hi/ Li mode. The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25°C$.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HB to GND leakage current	$I_{VHB-GND}$	–	0.1	8	uA	$V_{DD} = V_{INH} = V_{INL} = 0$ V, $V_{HS} = V_{HB} = 120$ V All reference to GND
LB quiescent current(Si)	I_{VLB}	–	75		uA	V_{INH} and $V_{INL} = 0$ V
LB quiescent current(GaN)	I_{VLB}	–	180		uA	V_{INH} and $V_{INL} = 0$ V
LB operating current(Si)	I_{VLBO}	–	1.2		mA	$V_{INH} = 0$V, V_{INL} at $F_{sw} = 500$ kHz, $V_{HB} = 0$V, $C_{load} = 0$ nF
LB operating current(GaN)	I_{VLBO}	–	17		mA	$V_{INH} = 0$V, V_{INL} at $F_{sw} = 500$ kHz, $V_{HB} = 0$V, $C_{load} = 5$ nF
LB to GND leakage current	$I_{VLB-GND}$	–	0.1	8	uA	$V_{DD} = V_{INH} = V_{INL} = 0$ V, $V_{LS} = V_{LB} = 120$ V
INH and INL independent (Hi/ Li) input						
INH and INL/ EN input voltage rising threshold	V_{IR}	-	-	2.6	V	INH and INL independent input control.
INH and INL/ EN input voltage falling threshold	V_{IF}	1.8	-	-	V	INH and INL independent input control.
INH and INL/ EN input voltage hysteresis	V_{IH}	-	0.4	-	V	INH and INL independent input control.
INH and INL/ EN input pull down resistance	R_{INH}, R_{INL}	100	200	300	kΩ	INH and INL independent input control.
Tri-state PWM input						
Middle to high level threshold	V_{IR_MH}	-	-	2.6	V	
High to middle level threshold	V_{IF_HM}	2.1	-	-	V	

(table continues...)

Table 7 (continued) Electrical characteristics

Unless otherwise specified: V_{DD} = V_{HB} = V_{LB} = 6 V, V_{HS} = V_{LS} = V_{GND} = 0 V, Hi/ Li mode. The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at T_C = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Middle/ high level hysteresis	V_{IH_MH}	-	40	-	mV	
Low to middle level threshold	V_{IR_LH}	-	-	1.2	V	
Middle to low level threshold	V_{IF_ML}	0.8	-	-	V	
Low/ middle level hysteresis	V_{IH_LM}	-	40	-	mV	
Tri-state PWM input pull-up and pull-down resistance	R_{PWM}	-	10	-	kΩ	Tri-level PWM input control.
PWM open circuit voltage	V_{PWMOP}	-	1.6	-	V	Tri-state PWM input
VDD Undervoltage lockout (UVLO)						
VDD UVLO rising threshold	V_{DDIR}	-	3.8	-	V	
VDD UVLO falling threshold	V_{DDIF}	-	3.6	-	V	
VDD UVLO hysteresis	V_{DDH}	-	0.2		V	
HB, LB Undervoltage lockout (UVLO)						
HB, LB UVLO rising threshold	V_{HBR}, V_{LBR}	-	3.83	-	V	Referenced to HS, LS
HB, LB UVLO falling threshold	V_{HBF}, V_{LBF}	-	3.68	-	V	Referenced to HS, LS
HB, LB UVLO hysteresis	V_{HBH} , V_{LBH}	-	0.15	-	V	
HB Gate driver						
High level output voltage	V_{HGH}	-	0.063	-	V	I_{HG} = -100 mA , V_{HGH} = V_{HB} - V_{HG}

(table continues...)

Table 7 (continued) Electrical characteristics

Unless otherwise specified: $V_{DD} = V_{HB} = V_{LB} = 6$ V, $V_{HS} = V_{LS} = V_{GND} = 0$ V, Hi/ Li mode. The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Low level output voltage	V_{HGL}	-	0.029	-	V	$I_{HG} = 100$ mA
Peak pull-up current(Si)	I_{HG_PUS}	-	4	-	A	$V_{HG} = 0$ V , [1]
Peak pull-up current(GaN)	I_{HG_PUG}		1.6		A	$V_{HB_HS} = 5$V [1]
Peak pull-down current(Si)	I_{HG_PL}	-	6	-	A	$V_{HG} = 6$ V [1]
Peak pull-down current(GaN)	I_{HG_PL}	-	6	-	A	$V_{HG} = 5$ V [1]
Output clamp capability	I_{HG_CLAMP}	-	10	-	mA	V_{HB} = open, $V_{HG} = 1$ V
LB Gate driver						
High level output voltage	V_{LGH}	-	0.063	-	V	$I_{LG} = -100$ mA , $V_{LGH} = V_{LB} - V_{LG}$
Low level output voltage	V_{LGL}	-	0.029	-	V	$I_{LG} = 100$ mA
Peak pull-up current(Si)	I_{LG_PUS}	-	4	-	A	$V_{LG}=0$V , [1]
Peak pull-up current(GaN)	I_{LG_PUG}	-	1.6	-	A	$V_{LB_LS} = 5$V [1]
Peak pull-down current(Si)	I_{LG_PL}	-	6	-	A	$V_{LG}=6$ V [1]
Peak pull-down current(GaN)	I_{LG_PL}	-	6	-	A	$V_{LG}=5$ V [1]
Output clamp capability	I_{LG_CLAMP}	-	10	-	mA	V_{LB} = open, $V_{LG} = 1$ V

1) Not subject to production test. Verified by design/characterization.

4.6 Switching characteristics

Table 8 Switching characteristics

Unless otherwise specified: $V_{DD} = V_{HB} = V_{LB} = 6$ V, $V_{HS} = V_{LS} = V_{GND} = 0$ V. The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25°C$.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Propagation delays						
Rising propagation delay(HG/LG ON)	t_{DR_A} , t_{DR_B}	-	18	25	ns	Hi/ Li mode, C_{load} = 0nF, $V_{HB} = V_{LB}$ = 6 V, from the rising input threshold at INH/INL to 10% of the output voltage Rising propagation delay INH to HG and INL to LG.
Falling propagation delay(HG/LG OFF)	t_{DFA} , t_{DFB}	-	14	25	ns	Hi/ Li mode, C_{load} = 0 nF , $V_{HB} = V_{LB}$ = 6 V, from the falling input threshold at INH/INL to 90% of the output voltage Falling propagation delay INH to HG and INL to LG.
Rising propagation delay(PWM mid to high)	t_{D_PMH}	-	33	40	ns	PWM mode, Cload = 0nF , 50%-50%, $V_{HB} = V_{LB}$ = 6 V Rising propagation delay PWM mid to high. Signal is driven by MCU.
Falling propagation delay(PWM high to mid)	t_{D_PHM}	-	32	40	ns	PWM mode, Cload = 0nF , 50%-50%, $V_{HB} = V_{LB}$ = 6 V Falling propagation delay PWM high to mid. Signal is driven by MCU.
Rising propagation delay(PWM low to mid)	t_{D_PLM}	-	33	40	ns	PWM mode, Cload = 0nF , 50%-50%, $V_{HB} = V_{LB}$ = 6 V Rising propagation delay PWM low to mid. Signal is driven by MCU.
Falling propagation delay(PWM mid to low)	t_{D_PML}	-	32	40	ns	PWM mode, Cload = 0nF , 50%-50%, $V_{HB} = V_{LB}$ = 6 V Rising propagation delay PWM mid to low. Signal is driven by MCU.
Delay matching						
Prop delay matching ON	t_{DMON}	-5	0	5	ns	Between HG rising and LG rising, Hi/ Li mode
Prop delay matching OFF	t_{DMOFF}	-5	0	5	ns	Between HG falling and LG falling, Hi/ Li mode

(table continues...)

Table 8 (continued) Switching characteristics

Unless otherwise specified: $V_{DD} = V_{HB} = V_{LB} = 6$ V, $V_{HS} = V_{LS} = V_{GND} = 0$ V. The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Output rise and fall time						
HG, LG rise time (Si)	t_{RA}, t_{RB}	-	4.5	-	ns	C_{load} = 1 nF , 10%-90% [1)]
HG, LG fall time (Si)	t_{FA}, t_{FB}	-	4.5	-	ns	C_{load} = 1 nF , 10%-90% [1)]
HG, LG rise time (Si)	t_{R1A}, t_{R1B}	-	55	-	ns	C_{load} = 25 nF , 10%-90% [1)]
HG, LG fall time (Si)	t_{F1A}, t_{F1B}	-	40	-	ns	C_{load} = 25 nF , 10%-90% [1)]
HG, LG rise time (GaN)	t_{R1A}, t_{R1B}	-	15.5	-	ns	C_{load} = 5 nF , 10%-90% [1)]
HG, LG fall time (GaN)	t_{F1A}, t_{F1B}	-	6.5	-	ns	C_{load} = 5 nF , 10%-90% [1)]
Deadtime or turn-on delay time (Deadtime from LG/HG falling to 50% to HG/LG rising to 50%. Turn-on delay from INH/INL rising of 50% HG/LG rising to 50%.)						
Deadtime / turn-on delay time	t_{D1}	-	0	-	ns	RDT < 2 kΩ, recommend 1% accuracy resistor [1)]
Deadtime / turn-on delay time	t_{D2}	3	6	9	ns	RDT = 8 kΩ, recommend 1% accuracy resistor [1)]
Deadtime / turn-on delay time	t_{D3}	8.4	12	15.6	ns	RDT = 20 kΩ, recommend 1% accuracy resistor [1)]
Deadtime / turn-on delay time	t_{D4}	15	21.5	28	ns	RDT = 39 kΩ, recommend 1% accuracy resistor [1)]
Deadtime / turn-on delay time	t_{D5}	36.4	52	67.6	ns	RDT = 100 kΩ, recommend 1% accuracy resistor
Deadtime / turn-on delay time	t_{D6}	71.4	102	132.6	ns	RDT = 200 kΩ, recommend 1% accuracy resistor [1)]
Mode selection						
Tri-state PWM mode	R_{TPWM}	-	-	13.2	kΩ	Pull-down resistor on MODE pin, recommend 1% accuracy resistor

(table continues...)

Table 8 (continued) Switching characteristics

Unless otherwise specified: $V_{DD} = V_{HB} = V_{LB} = 6$ V, $V_{HS} = V_{LS} = V_{GND} = 0$ V. The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25°C$.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HSCC HS mode	R_{HSCCH}	20	-	25	kΩ	Pull-down resistor on MODE pin, recommend 1% accuracy resistor
HSCC LS mode	R_{HSCCL}	37.5	-	42.5	kΩ	Pull-down resistor on MODE pin, recommend 1% accuracy resistor
Hi/ Li invert mode	R_{HLI}	63.75	-	68.75	kΩ	Pull-down resistor on MODE pin, recommend 1% accuracy resistor
Hi/ Li mode	R_{HL}	105	-	-	kΩ	Pull-down resistor on MODE pin, recommend 1% accuracy resistor
Current sense amplifier						
Transconductance	G_{m1}	4.8	5	5.2	uA/mV	R_{SNS}= 200 Ω, 0V<V_{CM}<35V, V_{ISENP} -V_{ISENN}=100mV
Transconductance	G_{m2}	4.8	5	5.2	uA/mV	R_{SNS}= 200 Ω, 5 V<V_{CM}<35 V, V_{ISENP} -V_{ISENN} = -100 mV
IMON maximum output current	I_{MON_M}	-600	-	750	uA	
Common mode voltage	V_{CM1}	0	-	35	V	Positive current sensing
Common mode voltage	V_{CM2}	5	-	35	V	Negative current sensing
Bandwidth	f_{BW}	1	5	-	MHz	[1)]
Gate clamp(GaN)						
HG, LG output voltage in driving GaN	V_{HG}, V_{LG}	4.5	5	5.5	V	The effective clamp voltage at the gate of GaN switch depends on gate loop parasitic inductance, gate resistance and Qg of GaN switch.
Bootstrap diode						
High current forward voltage	V_{DFW}	-	0.85	1.2	V	I_{VDD_HB} = 100mA
Low current forward voltage	V_{DFWL}	-	0.45	0.85	V	I_{VDD_HB} = 100uA
Dynamic resistance	R_{DD}	-	0.5	-	Ω	$R_{DD} = \Delta V_{DD}/\Delta I_{VDD\_HB}$, I_{VDD_HB} = 80 mA and 100 mA

(table continues...)

Table 8 (continued) Switching characteristics

Unless otherwise specified: $V_{DD} = V_{HB} = V_{LB} = 6$ V, $V_{HS} = V_{LS} = V_{GND} = 0$ V. The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Reverse bias leakage	I_{DLK}	-	0.1	-	uA	$V_{HB} = V_{HS} = 100$ V, $V_{DD} = 0$ V
Reverse recovery time	t_{RR}	-	10	-	ns	100mA forward to 100V reverse [1)]
Miscellaneous						
Minimum input pulse width that changes output (Si)	t_{PWS}	-	10	-	ns	$C_{load} = 0$ nF
Driver switching frequency (GaN)	f_{SWG}	100	-	-	kHz	For $V_{DD} < 7.5$V [1)]
Gate driver startup time (Si)	t_{STUP_DRV}	-	20	-	µs	The time duration from VDD UVLO rising to 99% settled of IMON current [1)]
Gate driver startup time (GaN)	t_{STUP_DRV2}	-	25	-	us	[1)]
HB-HS and LB-LS rising slew rate	$dVxB\text{-}xS/dt$	-	-	160	V/µs	[1)]
VCS rising slew rate	dV_{VCS}/dt	-	-	10	V/µs	[1)]
VDD rising slew rate	dV_{VDD}/dt	-	-	16	V/µs	[1)]

1) Not subject to production test. Verified by design/characterization.

5 Application information

The 2EDL90xG3 can be used as a dual high-side driver or a dual low-side driver or a half-bridge driver. A typical application example of HV buck is given in HV buck with 2EDL90xG3, where the 2EDL901G3 can be used to drive the high-side GaN HEMT Q1 and the low-side GaN HEMT Q2. Alternatively, the 2EDL900G3 can be used to drive the high-side Si MOSFET Q1 and the low-side Si MOSFET Q2. To ensure the optimal performance of 2EDL90xG3 in the application circuit, the following points be must be taken care during application design:

1. In GaN application, to mitigate any potential induced turn-on of Q2 at high dv/dt in GaN application, a small gate source capacitor (C33) is recommended.
2. In GaN application, to mitigate any coupled noise to the HG pin due to large board parasitic, a small capacitor C40 (<1nF) is recommended to be placed close to HG-HS pins.
3. To reduce the overshot or ringing at switching node, a small high side gate resistor (R7) is recommended.
4. To reduce the inrush bootstrap current during startup, a small current limit resistor (R2) is recommended.
5. The EN pin has maximum input voltage of 4 V. A dedicated enable signal is recommended or a resistor divider (R3) must be placed if EN pin is short to VDD.
6. To reduce the noise coupling at the IMON readout circuitry, a small noise filter capacitor (C30) is recommended. The ground of IMON readout circuitry must be separated from the switching power ground.
7. To avoid any saturation of IMON maximum output current capability, the RSEN resistor (R10) must be chosen properly based on the current sensing gain calculation equation from Current sense amplifier block.

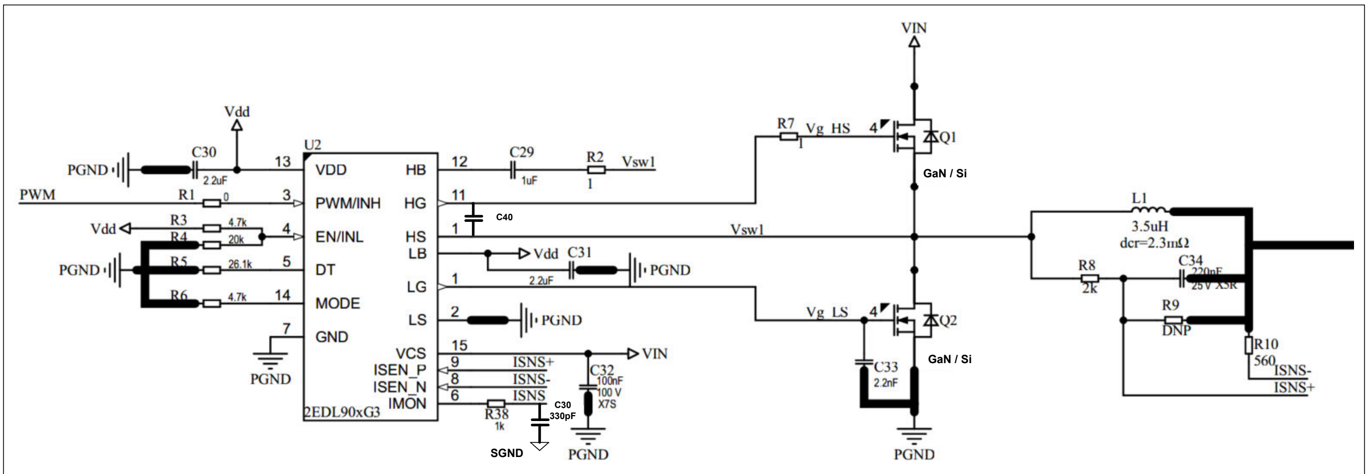

Figure 9 **HV buck with 2EDL90xG3**

6 PCB layout guidelines

To maximize the performance of EiceDRIVERTM 2EDL90xG3, below are some recommendations on how to optimize the PCB layout:

- Use a low-ESR decoupling capacitors on VDD-GND, HB-HS and LB-LS and placed the capacitors as close as possible to the corresponding pins of the driver.
- An option for a series boot resistor is recommended to control the high-side switch slew rate and therefore the low-side switch overshoot. The boot loop path, including the HB capacitor, boot diode and boot series resistor(option), should be as small as possible. Boot capacitor must be placed as close as possible to the HB pin of the driver.
- It is recommended to have an external boot diode placement for high dv/dt application.
- Placement for the gate resistor is also recommended to control the switching speed of the switch. Both the gate resistor and the switch should be placed as close as possible to the driver to minimize the gate loop inductance.
- Use a copper plane underneath the exposed GND pad of the driver and connect it to the buried copper plane(s) with multiple thermal vias for better heat dissipation into the PCB.
- The connection of the HS and LS of the driver to its corresponding switching nodes should be as short and wide as possible and avoid connecting it directly through the high switching current path.
- HG and LG traces should be as short and wide as possible
- Avoid letting the INH, INL, DT and MODE signal traces to come close to high dV/dT traces which might induce significant noise.
- The ISENN, ISENP and IMON should not be placed near any high speed switching lines.

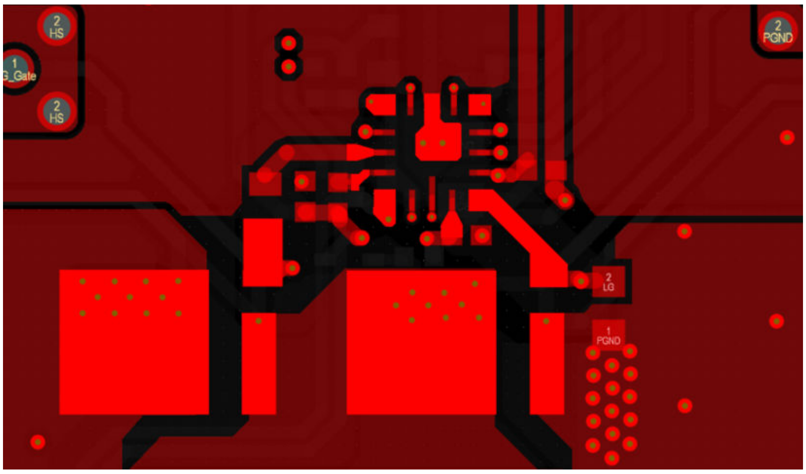

Figure 10 PCB layout example in a half-bridge configuration

7 Package information

Notes

1. For further information on package types, recommendation for board assembly, please go to: www.infineon.com\packages

7.1 Product variants

Part number	Driver type	Package	Body size
2EDL900G3	Si	TSNP-16	3 mm x 3 mm
2EDL901G3	GaN	TSNP-16	3 mm x 3 mm

7.2 Ordering information

Base part number	Package type	Standard pack		Orderable part number	Marking code
		Form	Quantity		
2EDL900G3	PG-TSNP-16-5	Tape and Reel	5000	2EDL900G3XTMA1	XXXZZ900G3H
2EDL901G3	PG-TSNP-16-5	Tape and Reel	5000	2EDL901G3XTMA1	XXXZZ901G3H

7.3 Outline and footprint dimensions

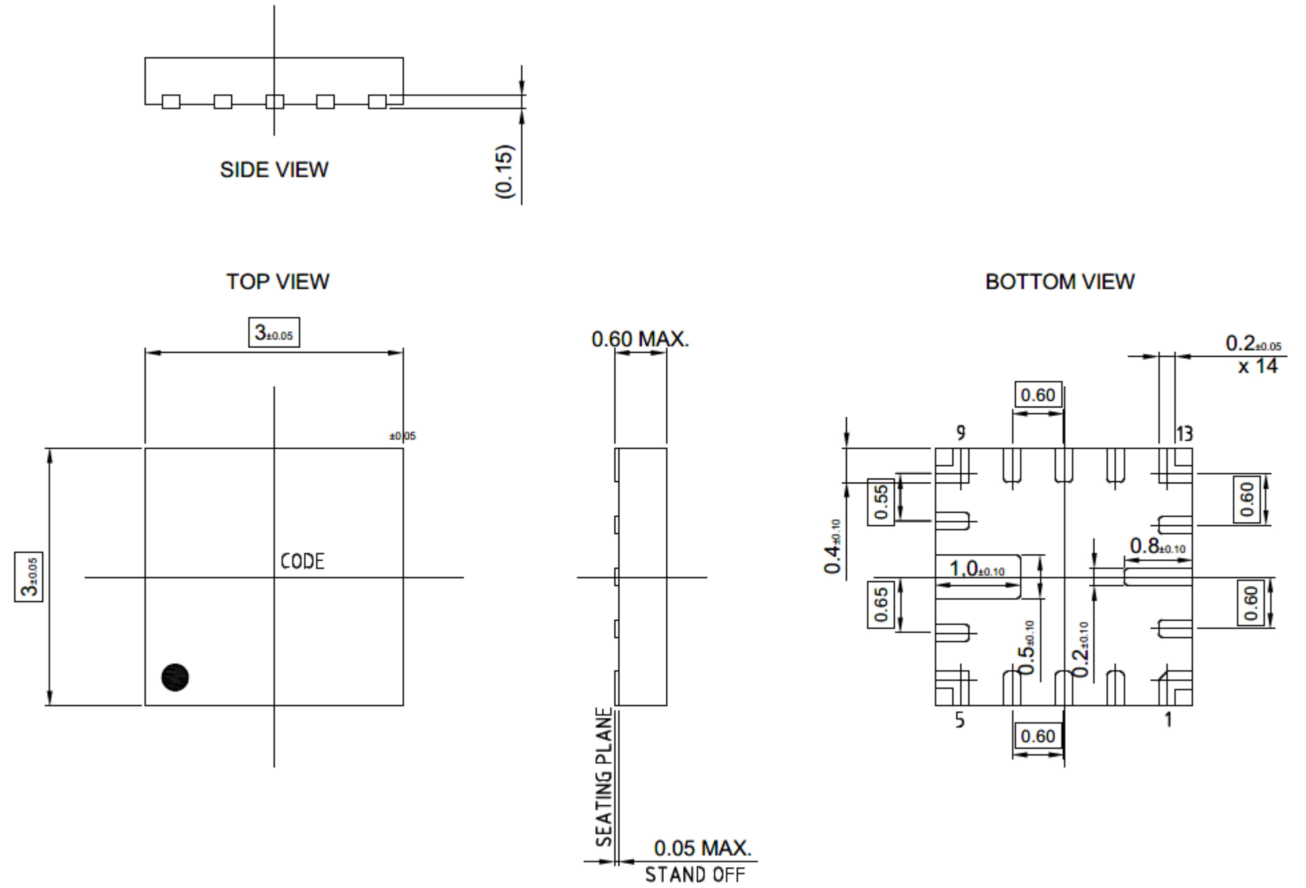

Figure 11 **TSNP-16 outline dimensions**

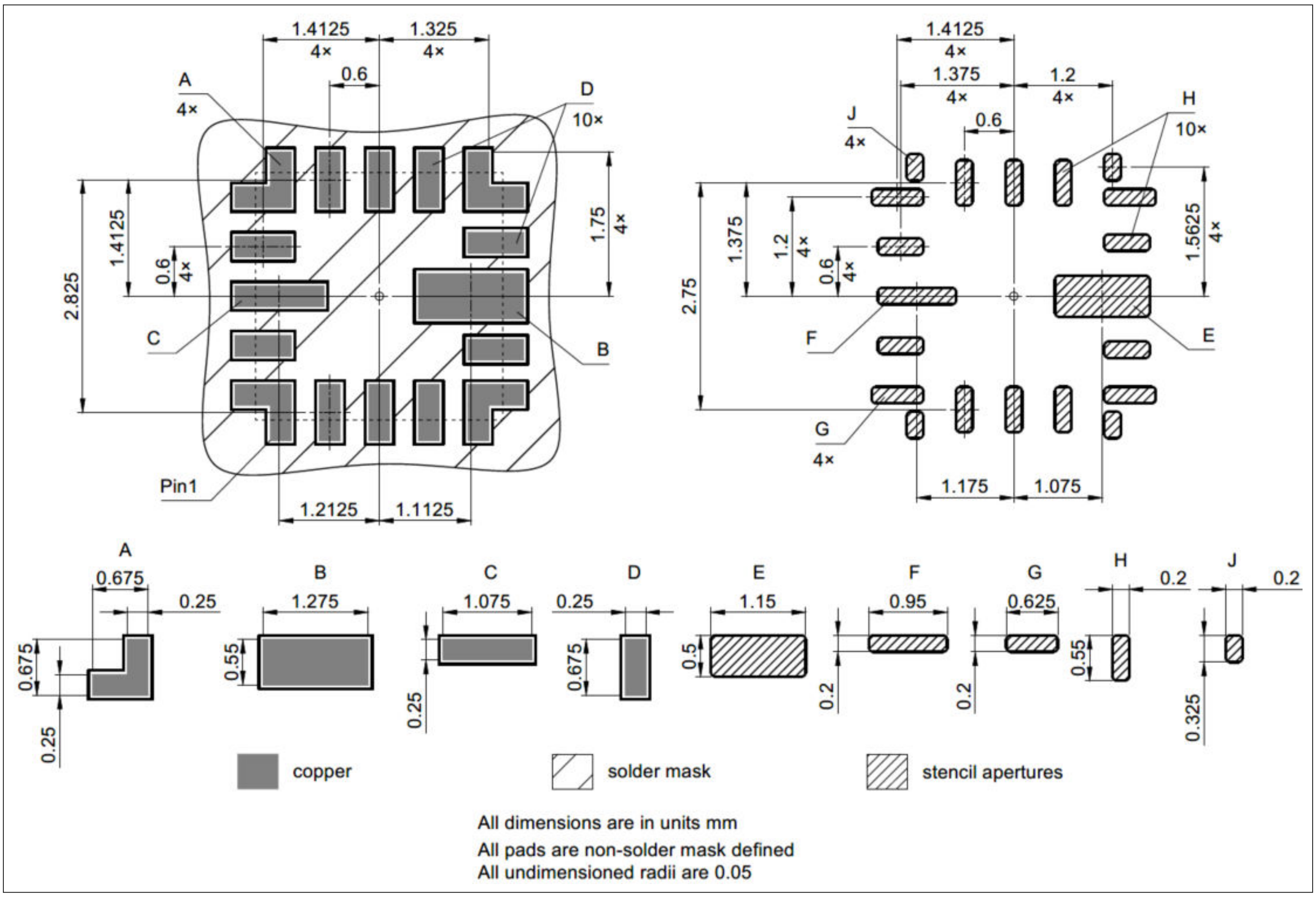

Figure 12 TSNP-16 footprint dimensions

7.4 Tape and reel

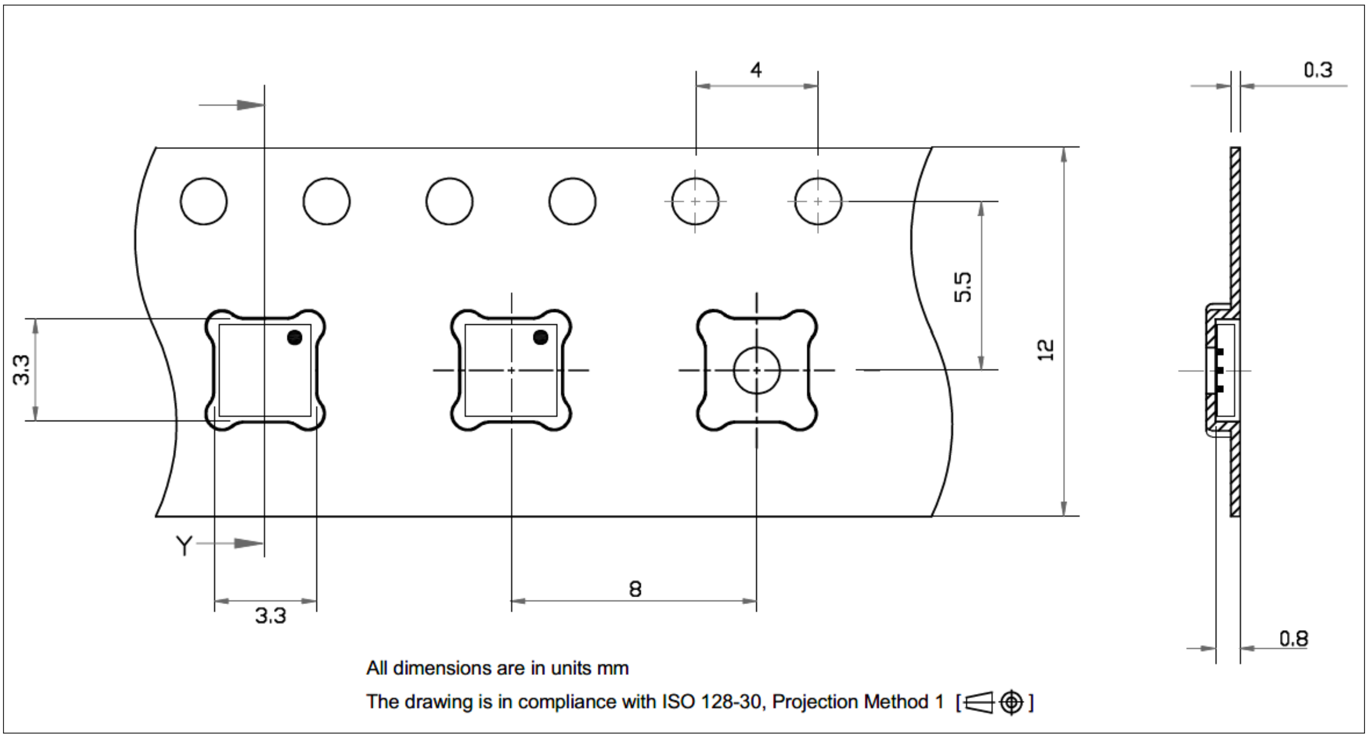

Figure 13 TSNP-16 Tape and reel

8 Revision history

Revision	Date	Description of changes
0.1	2025-05-30	Initial release
0.2	2026-02-11	Preliminary datasheet release
1.0	2026-04-01	Final datasheet release

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