EiceDRIVER™ 2EDL6014AC-G2D

120 V, 4 A, junction-isolated, dual channel floating output gate driver IC

Features

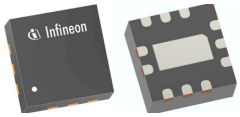
- Junction isolated dual-channel floating output driver
- 4 A source / 6 A sink output current capability
- Driver output current starving to limit the inrush current during system startup
- 120 V absolute maximum voltage on VDDA and VDDB
- 3.3 V and 5 V compliant input pins
- -5 A output pin reverse current capability
- -12 V absolute maximum negative voltage on GNDA/GNDB
- 4 V to 16 V gate supply voltage operating range
- UVLO for VDDA and VDDB
- 20 ns typical propagation delay
- 1 ns typical delay matching
- Support operating frequency up to 2 MHz
- >0.5 mm creepage between high voltage domain and low voltage domain
- Specified from -40 °C to 125 °C operating junction temperature range
- Universal application: dual high-side, dual low-side and half-bridge driver
- Offered in QFN-12 (2.2 x 2.2) with exposed thermal pad
- Lead free RoHS compliant package

Potential applications

- Intermediate bus converters for AI servers
- 48 V/54 V down conversion for data center and telecom
- 3 or multi-level buck converters
- Switched capacitor converters
- Motor drive and humanoid robotics

Product validation

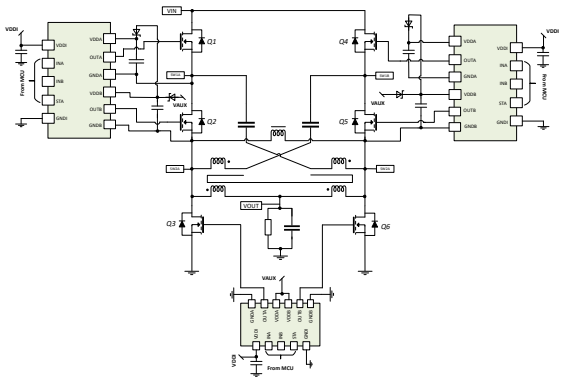
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22



Description

The 2EDL6014AC-G2D gate driver is designed to drive dual high-side, dual low-side or half-bridge MOSFETs. It offers two completely floating outputs gate drivers, especially useful for switched-capacitor and multi-level topologies. The floating high-side drivers are capable of driving a high-side MOSFET operating up to 120 V voltage. It provides full 4 A source and 6 A sink current driving capability. The inputs of the driver are 3.3 V and 5 V logic compatible. 2EDL6014AC, with separate INA and INB input pins, allows controlling the two channels independently, while adding deglitch filtering for higher noise immunity. The input stage can be directly connected to the microcontroller ground for maximizing signal integrity. Undervoltage lockout (UVLO) on the two floating output supplies forces the corresponding outputs low in case of insufficient supply. It is available in WQFN-12 pins 2.2 mm x 2.2 mm package.

Typical application diagram



Device information

Part number	Package	Body size
2EDL6014AC-G2D	WQFN-12	2.2 mm x 2.2 mm

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1 Block diagram

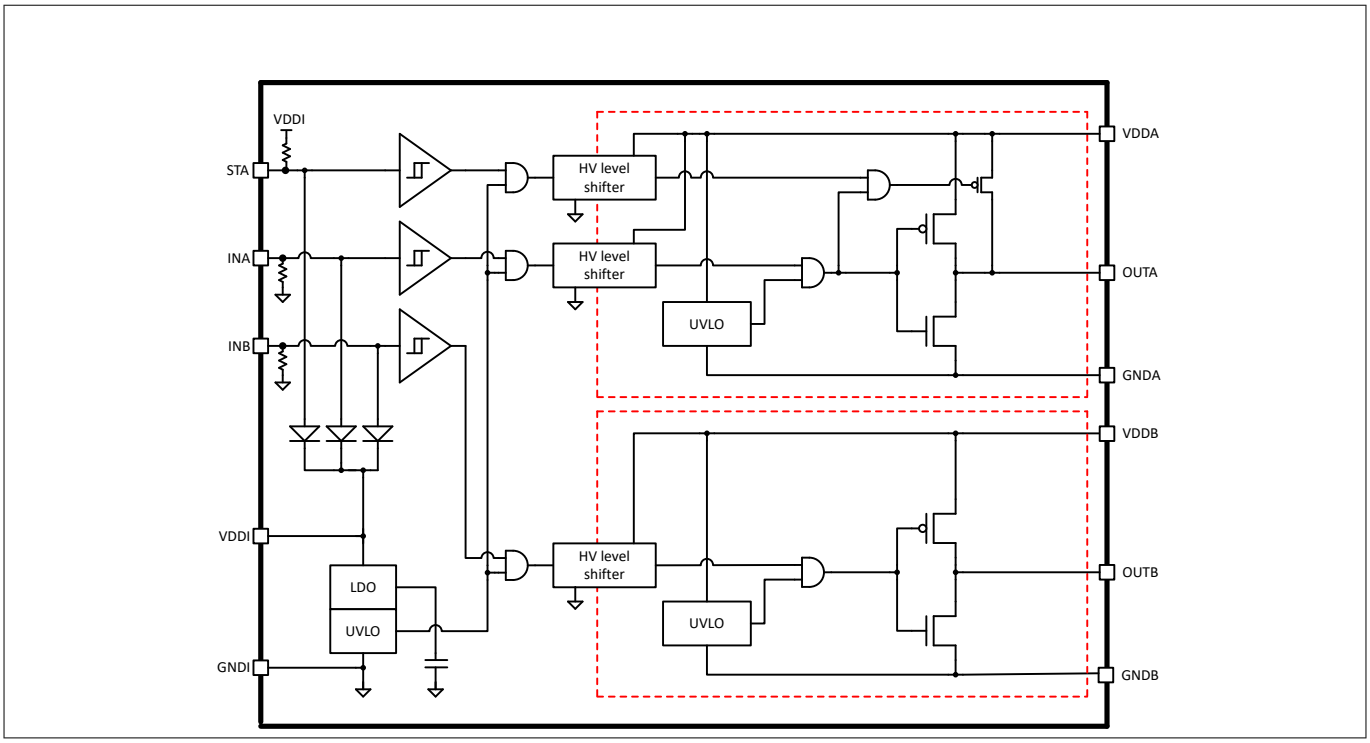

Figure 1 Block diagram of 2EDL6014AC-G2D

2 Pin configuration

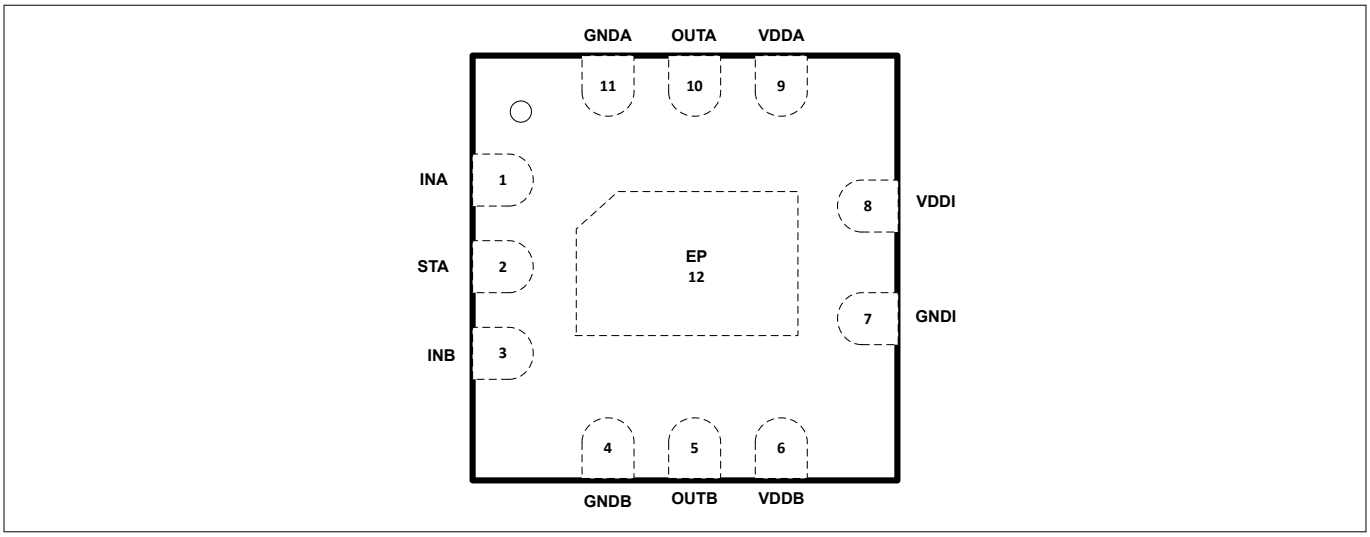

Figure 2 **2EDL6014AC-G2D WQFN-12 2.2 x 2.2 (top view)**

Table 1 **Pin description of 2EDL6014AC-G2D**

Pin name	Pin #	Function
INA	1	Input control for channel A.
STA	2	Adjustable pull-up strength of channel A. When the STA pin is low, only a fraction of the output pull-up stage in channel A is enabled. When the STA pin is high, the full output stage is enabled. The reduced pull-up current and full pull-up current are described in electrical characteristic table.
INB	3	Input control for channel B.
GNDB	4	Ground for output channel B. Kelvin-connect GNDB to the corresponding MOSFET source pin for high noise immunity.
OUTB	5	Driver source and sink current output for channel B.
VDDB	6	Driver supply for output channel B. An external capacitor must be tied between this pin and GNDB and placed as close to the IC as possible
GNDI	7	Chip ground (ground of the input control)
VDDI	8	Supply voltage for the input side. An external capacitor must be tied between this pin and GND and placed as close to the IC as possible.
VDDA	9	Driver supply for output channel A. An external capacitor must be tied between this pin and the GNDA pin and placed as close to the IC as possible.
OUTA	10	Driver source and sink current output for channel A.
GNDA	11	Ground for output channel A. Kelvin-connect GNDA to the corresponding MOSFET source pin for high noise immunity.
EP	12	Exposed thermal pad. The exposed thermal pad must be connected to GNDI. The exposed thermal pad must be soldered properly for rated thermal performance.

3 Functional description

The 2EDL6014AC-G2D gate driver is designed to drive two high-side MOSFETs. It offers two completely floating outputs gate drivers, especially useful for switched-capacitor and multi-level topologies. The floating high-side drivers are capable of driving a high-side MOSFET operating up to 120 V voltage. It provides full 4 A source and 6 A sink current driving capability. The inputs of the driver are 3.3 V and 5 V logic compatible. 2EDL6014AC, with separate INA and INB input pins, allows controlling the two channels independently. The input stage can be directly connected to the microcontroller ground for maximizing signal integrity. Undervoltage lockout (UVLO) on the input supply and on the two floating output supplies forces the corresponding outputs low in case of insufficient supply. It is available in WQFN-12 pins 2.2 mm x 2.2 mm package.

The following sections describe the key functionalities.

Supply voltage

The absolute maximum supply voltage($V_{DDA\text{-}GNDA}$ and $V_{DDB\text{-}GNDB}$) is 17 V. The minimum operating supply voltage is set by the UVLO function of V_{DDA} and $V_{DDB.}$ This lockout function protects power MOSFETs from running into linear mode with subsequent high power dissipation. If VDDI supply is present, the peak voltage of INA, INB and STA must be lower than or equal to VDDI. Hence, it is recommended to share the same power supply for VDDI and the digital controller.

Input stage

The 2EDL6014AC-G2D device responds independently to the two inputs signals (INA and INB) according to the following truth table.

Table 2 Truth table

INA	INB	OUTA	OUTB
L	L	L	L
H	L	H	L
L	H	L	H
H	H	H	H

The input pull-down resistance has a value of 200 kΩ typical.

Driver outputs

The strong 4 A source and 6 A sink current capability of both the low-side and high-side output allows for faster switching of the power MOSFETs thus leading to lower switching losses. The ultra-low pull-down resistances keep the gate of the power MOSFETs off during fast transient events thus avoiding dV/dt induced turn-on. The output stage is implemented using a PMOS for the pull-up and NMOS for the pull-down.

Adjustable pull-up strength function of channel A output

The pull-up output stage of channel A driver is split into fraction M and fraction N. For hybrid switch capacitor converter(HSC) design, it is recommended to connect power good signal to the STA pin. The INA input (PWM) turns ON only the fraction M of the pull-up output stage of channel A, when STA pin is set to low. This slows down the turn-on of the output device during system startup, which limits the inrush current flowing into the flying capacitor. When the system startup is finished, the digital controller asserts a high level power good signal, which sets the STA pin to high. For the next cycle, the whole (M+N) pull-up transistor is turned ON whenever INA is high. If the adjustable pull-up strength function is not used, please pull up the STA pin to VDDI.

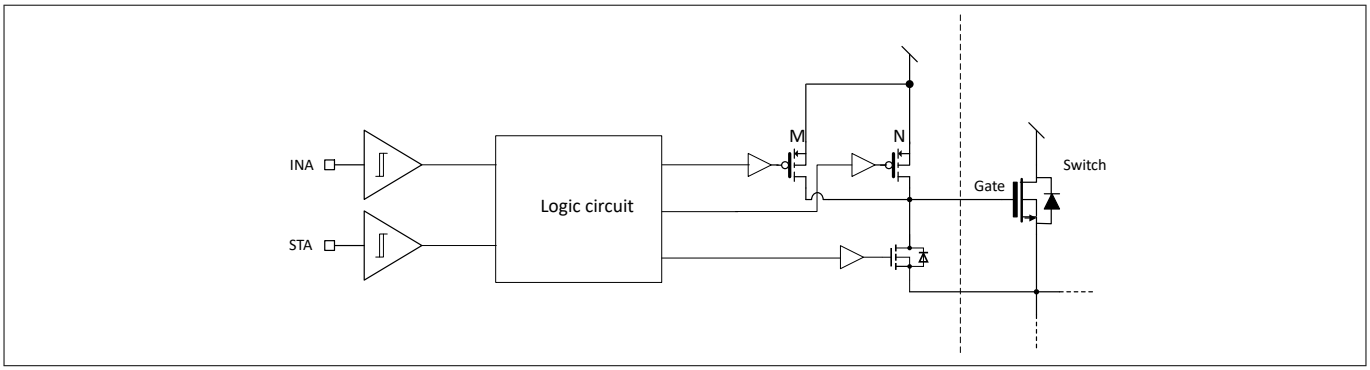

Figure 3 Adjustable pull-up strength block diagram

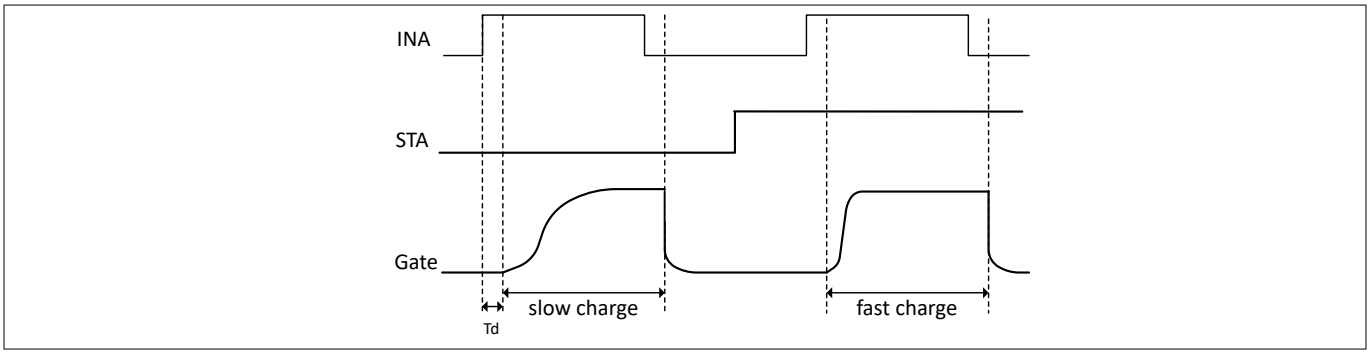

Figure 4 Adjustable pull-up strength signal timing

Under voltage lockout (UVLO)

The UVLO function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO rising threshold voltage. Thus it ensures that the power MOSFET is not switched on if the driving voltage is too low to completely switch on the device, thereby avoiding excessive power dissipation. The UVLO level is set to a typical value of 3.82 V with 0.17 V hysteresis for supply voltage ($V_{DDA-GNDA}$ and $V_{DDB-GNDB}$) .

Minimum input pulse

The device responds to input level according to the truth table in input control section as long as the logic signal complies with the minimum pulse width requirement. A signal pulse longer than the minimum allowable input pulse width gives a valid output. Any output in response to shorter pulses or glitches should be disregarded and filtered out by the user. Under all allowable operation above input minimum pulse width of 10 ns, the output behaves one to one to the input with minimal pulse width distortion.

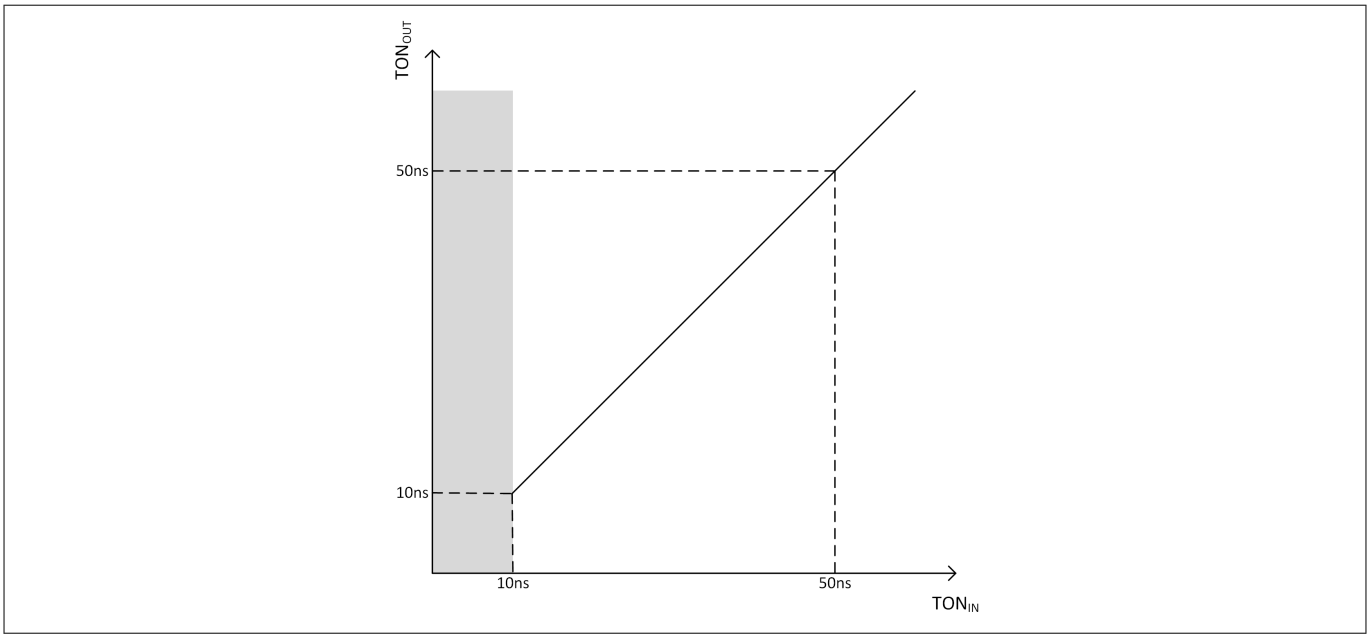

Figure 5 **Minimum input pulse width: input-output on-time transfer function**

4 General product characteristics

4.1 Absolute maximum ratings

Table 3 Absolute Maximum Ratings

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. All voltage parameters are referenced to GNDI unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDDI input supply voltage	V_{DDI}	-0.3	–	6	V	
Floating output supply voltage	$V_{DDA-GNDA}$, $V_{DDB-GNDB}$	-0.3	–	17	V	Referenced to V_{GNDA} and V_{GNDB}
VDDA and VDDB voltage	V_{DDA}, V_{DDB}	-0.3	–	120	V	1)
GNDA and GNDB voltage	VGNDA, V_{GNDB}	-5	–	V_{DDA} + 0.3 V_{DDB} + 0.3	V	
GNDA and GNDB voltage (Repetitive pulse)	V_{GNDA}, V_{GNDB}	V_{DDA} - 17 V_{DDB} - 17	–	V_{DDA} + 0.3 V_{DDB} + 0.3	V	< 100 ns 2)
INA, INB and STA input voltage	V_{INA}, V_{INB}, V_{STA}	-0.3		V_{DDI}+ 0.3	V	The max voltage of INA, INB and STARVE must be less than or equal to VDDI voltage.
Output voltage on OUTA	V_{OUTA}	V_{GNDA} - 0.3	–	V_{DDA} + 0.3	V	Referenced to V_{GNDA}
Output voltage on OUTA (Repetitive pulse)	V_{OUTA}	V_{GNDA} - 2	–	V_{DDA} + 0.3	V	Referenced to V_{GNDA}, < 100 ns 2)
Output voltage on OUTB	V_{OUTB}	V_{GNDB} - 0.3	–	V_{DDB} + 0.3	V	Referenced to V_{GNDB}
Output voltage on OUTB (Repetitive pulse)	V_{OUTB}	V_{GNDB} - 2	–	V_{DDB} + 0.3	V	Referenced to V_{GNDB}, < 100 ns 2)

(table continues...)

Table 3 (continued) Absolute Maximum Ratings

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. All voltage parameters are referenced to GNDI unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Peak reverse current on OUTA and OUTB	I_{OR}	–	–	5	A	2) 3)
Operating junction temperature	T_J	-40	–	150	°C	
Storage temperature	T_S	-55	–	150	°C	

1) Verified with VDDI supplied within the recommended operating voltage range.
2) Not subject to production test. Verified by design/characterization.
3) For < 500 ns pulses.

4.2 ESD ratings

Table 4 ESD ratings

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HBM	V_{ESD_HBM}	-1	-	1	kV	According to ANSI/ESDA/JEDEC specification JS-001
CDM	V_{ESD_CDM}	-500	-	500	V	According to ANSI/ESDA/JEDEC specification JS-002

4.3 Recommended operating conditions

Table 5 Recommended Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to V_{GND} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDDI supply voltage	V_{DDI}	2.97	3.3	5.5	V	
Floating supply voltage	$V_{DDA-GNDA}$, $V_{DDB-GNDB}$	4	-	16	V	Referenced to V_{GNDA} and V_{GNDB}

(table continues...)

Table 5 (continued) Recommended Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to V_{GND} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDDA and VDDB voltage	V_{DDA}, V_{DDB}	V_{GNDA} + 4 V_{GNDB} + 4 V_{GNDI} + 2	–	V_{GNDA} + 16 V_{GNDB} + 16	V	referenced to GNDI
GNDA and GNDB voltage	V_{GNDA}, V_{GNDB}	-2	–	100	V	referenced to GNDI
GNDA and GNDB voltage (Repetitive pulse)	V_{GNDA}, V_{GNDB}	V_{DDA} - 16 V_{DDB} - 16	–	100	V	< 100 ns
INA, INB and STA input voltage	V_{INA}, V_{INB}, V_{STA}	0	–	V_{DD} + 0.3	V	
Output voltage on OUTA	V_{OUTA}	0	–	16	V	Referenced to V_{GNDA}
Output voltage on OUTB	V_{OUTB}	0	–	16	V	Referenced to V_{GNDB}
GNDA and GNDB slew rate	dV_{GNDA}/dt, dV_{GNDB}/dt	–	–	50	V/ns	
Junction temperature range	T_J	-40	–	125	°C	

4.4 Thermal characteristics

Table 6 Thermal mechanical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction-to-case (bottom) thermal resistance	R_{thJC_B}	-	4.1	-	°C/W	*1) 2)*

(table continues...)

Table 6 (continued) Thermal mechanical characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction-to-case (top) thermal resistance	R_{thJC_T}	-	118	-	°C/W	1) 2)
Junction-to-ambient thermal resistance	R_{thJA}	-	67.8	-	°C/W	Device soldered on PCB 1) 2)
Junction-to-board thermal resistance	R_{thJB}	-	22.3	-	°C/W	Device soldered on PCB 1) 2)

1) Not subject to production test, specified by design.
2) Specified value is according to Jedec JESD51-5 /-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable one thermal via (Æ = 0.3 mm) is under the exposed pad.

4.5 Electrical characteristics

Table 7 Electrical characteristics

Unless otherwise specified: $V_{DDA} = V_{DDB} = 6$ V, $V_{GNDA} = V_{GNDB} = V_{GNDI} = 0$ V, ($V_{DDI} = 3.3$ V). The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current						
VDDI quiescent current	I_{VDDI}	-	60	400	uA	V_{INA} and $V_{INB} = 0$ V
VDDA quiescent current	I_{VDDA}	-	65	100	uA	V_{INA} and $V_{INB} = 0$ V
VDDA operating current	I_{VDDAO}	-	0.7	1.2	mA	$V_{INB} = 0$V, V_{INA} at $F_{SW} = 500$ kHz, $V_{DDB} = 0$V, $V_{STARVE} = 3.3$V, $C_{LOAD} = 0$ nF
VDDA to GNDI leakage current	$I_{VDDA-GNDI}$	–	0.1	8	uA	$V_{DDI} = V_{INA} = V_{INB} = 0$ V, $V_{GNDA} = V_{VDDA} = 120$ V All reference to GNDI
VDDB quiescent current	I_{VDDB}	–	65	100	uA	V_{INA} and $V_{INB} = 0$ V

(table continues...)

Table 7 (continued) Electrical characteristics

Unless otherwise specified: $V_{DDA} = V_{DDB} = 6$ V, $V_{GNDA} = V_{GNDB} = V_{GNDI} = 0$ V, ($V_{DDI} = 3.3$ V). The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VDDB operating current	I_{VDDBO}	–	0.7	1.2	mA	V_{INA} = 0V, V_{INB} at F_{sw} = 500 kHz, V_{DDA} = 0V, C_{load} = 0 nF
VDDB to GNDI leakage current	$I_{VDDB-GNDI}$	–	0.1	8	uA	$V_{DDI} = V_{INA} = V_{INB} = 0$ V, $V_{GNDB} = V_{VDDB} = 120$ V
Input						
Input voltage rising threshold	V_{IR}	-	-	2.4	V	INA, INB and STA input voltage rising threshold
Input voltage falling threshold	V_{IF}	0.8	-	-	V	INA, INB and STA input voltage falling threshold
Input voltage hysteresis	V_{IH}	-	1.1	-	V	INA, INB and STA input voltage hysteresis
INA and INB input pull down resistance	R_{INA}, R_{INB}	100	200	300	kΩ	INA and INB input
STA input pull up resistance	R_{INS}	100	200	300	kΩ	
VDDA, VDDB Undervoltage lockout (UVLO) LL-FET/ GaN						
VDDA, VDDB UVLO rising threshold	V_{DDAR}, V_{DDBR}	3.66	3.82	3.98	V	Referenced to GNDA, GNDB
VDDA, VDDB UVLO falling threshold	V_{DDAF}, V_{DDBF}	3.5	3.65	3.8	V	Referenced to GNDA, GNDB
VDDA, VDDB UVLO hysteresis	V_{DDAH} , V_{DDBH}	-	0.17	-	V	
VDDA Gate driver						
High level output voltage	V_{OUTAH}	-	0.074	-	V	I_{OUTA} = -100 mA , V_{STA} = high or open, $V_{OUTAH} = V_{DDA} - V_{OUTA}$

(table continues...)

Table 7 (continued) Electrical characteristics

Unless otherwise specified: V_{DDA} = V_{DDB} = 6 V, V_{GNDA} = V_{GNDB} = V_{GNDI} = 0 V, (V_{DDI} = 3.3 V). The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at T_C = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High level output voltage in reduced pull-up strength mode	V_{OUTAHS}	-	0.54	-	V	I_{OUTA} = -100 mA , V_{STA} = low, V_{OUTAH} = V_{DDA} - V_{OUTA}
Low level output voltage	V_{OUTAL}	-	0.04	-	V	I_{OUTA} = 100 mA
Peak pull-up current	I_{OUTA_PU}	-	4	-	A	V_{OUTA} = 0 V, STA= high or open[1)]
Peak pull-up current in reduced driver strength mode	I_{OUTA_STA}	-	500	-	mA	V_{OUTA} = 0 V, STA = low [1)]
Peak pull-down current	I_{OUTA_PL}	-	6	-	A	V_{OUTA} = 6 V [1)]
Output clamp capability	I_{OUTA_CLAMP}	-	10	-	mA	V_{DDA} < UVLO, V_{OUTA} = 1 V
VDDB Gate driver						
High level output voltage	V_{OUTBH}	-	0.074	-	V	I_{OUTB} = -100 mA , V_{OUTBH} = V_{DDB} - V_{OUTB}
Low level output voltage	V_{OUTBL}	-	0.04	-	V	I_{OUTB} = 100 mA
Peak pull-up current	I_{OUTB_PU}	-	4	-	A	V_{OUTB}=0V , [1)]
Peak pull-down current	I_{OUTB_PL}	-	6	-	A	VOUTB=6 V [1)]
Output clamp capability	I_{OUTB_CLAMP}	-	10	-	mA	V_{DDB} < UVLO, V_{OUTB} = 1 V

1) Not subject to production test. Verified by design/characterization.

4.6 Switching characteristics

Table 8 Switching characteristics

Unless otherwise specified: $V_{DDA} = V_{DDB} = 6$ V, $V_{GNDA} = V_{GNDB} = V_{GNDI} = 0$ V, ($V_{DDI} = 3.3$ V). The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Propagation delays						
Rising propagation delay	t_{DR_A}, t_{DR_B}	-	20	27	ns	C_{load} = 0nF , 50%-50%, VDDA = VDDB = 6 V Rising propagation delay INA to OUTA and INB to OUTB. Including INA and INB input deglitch time.
Falling propagation delay	t_{DFA}, t_{DFB}	-	20	27	ns	C_{load} = 0 nF , 50%-50%, VDDA = VDDB = 6 V Falling propagation delay INA to OUTA and INB to OUTB. Including INA and INB input deglitch time.
Delay matching						
Delay matching ON	t_{DMON}	-2	0	2	ns	Between OUTA rising and OUTB rising. VDDA = VDDB = 6 V.
Delay matching OFF	t_{DMOFF}	-2	0	2	ns	Between OUTA falling and OUTB falling. VDDA = VDDB = 6 V.
Output rise and fall time						
OUTA, OUTB rise time	t_{RA}, t_{RB}	-	4.2	-	ns	C_{load} = 1 nF , 10%-90% 1)
OUTA rise time in reduced pull-up strength mode	t_{RAS}	-	17.7	-	ns	C_{load} = 1 nF , 10%-90% 1)
OUTA, OUTB rise time	t_{R1A}, t_{R1B}	-	53	-	ns	C_{load} = 25 nF , 10%-90%
OUTA, OUTB fall time	t_{FA}, t_{FB}	-	3.8	-	ns	C_{load} = 1 nF , 10%-90% 1)
OUTA, OUTB fall time	t_{F1A}, t_{F1B}	-	36	-	ns	C_{load} = 25 nF , 10%-90% 1)
Miscellaneous						
INA, INB input deglitch time	t_{DGLA}, t_{DGLB}	-	3	-	ns	1)
STA input deglitch time	t_{DGL}	50	75	100	ns	1)

(table continues...)

Table 8 (continued) Switching characteristics

Unless otherwise specified: V_{DDA} = V_{DDB} = 6 V, V_{GNDA} = V_{GNDB} = V_{GNDI} = 0 V, (V_{DDI} = 3.3 V). The minimum and maximum limits are valid over the full operating range and are ensured by characterization and statistical correlation. Typical values are tested at T_C = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Minimum input pulse width that changes output	t_{PW}	-	10	-	ns	C_{load} = 0 nF

1) Not subject to production test. Verified by design/characterization.

5 Typical characteristics

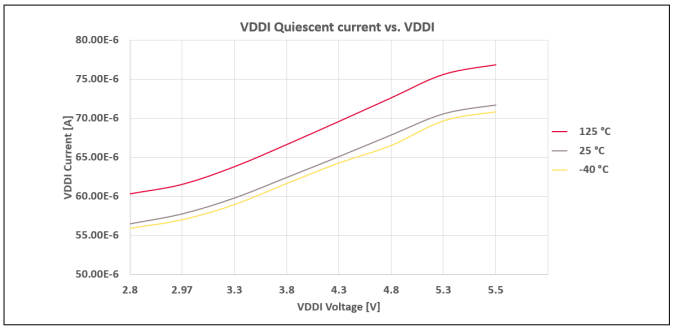

Figure 6 **VDDI quiescent current vs. VDDI voltage**

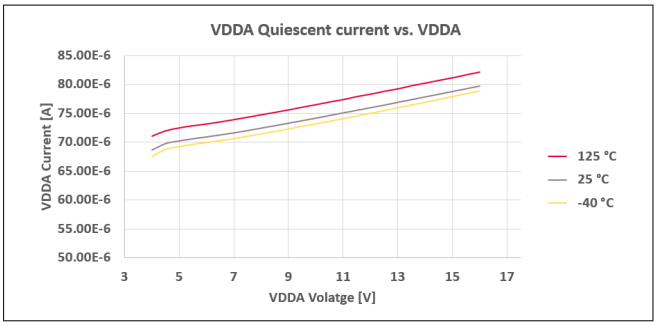

Figure 7 **VDDA quiescent current vs. VDDA voltage**

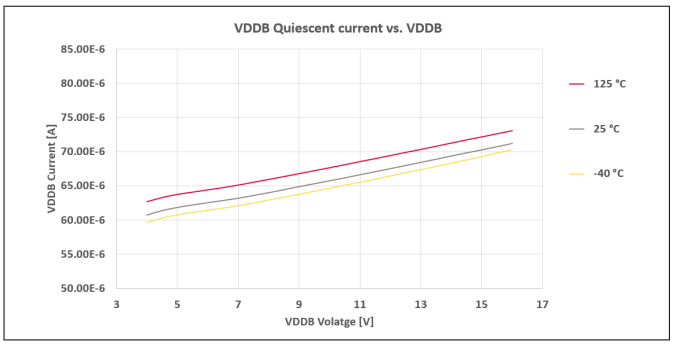

Figure 8 **VDDB quiescent current vs. VDDB voltage**

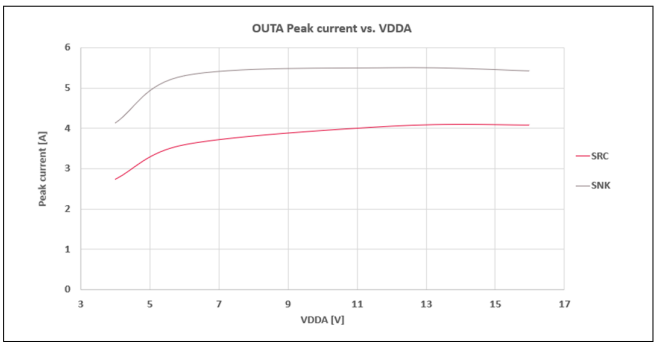

Figure 9 **OUTA peak currents vs. VDDA voltage**

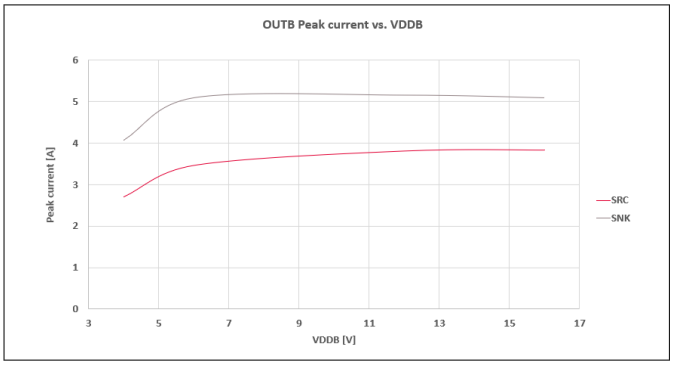

Figure 10 **OUTB peak currents vs. VDDB voltage**

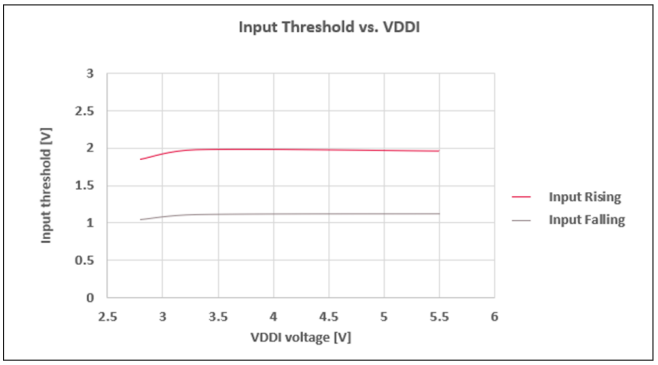

Figure 11 **Input thresholds vs. VDDI voltage**

5 Typical characteristics

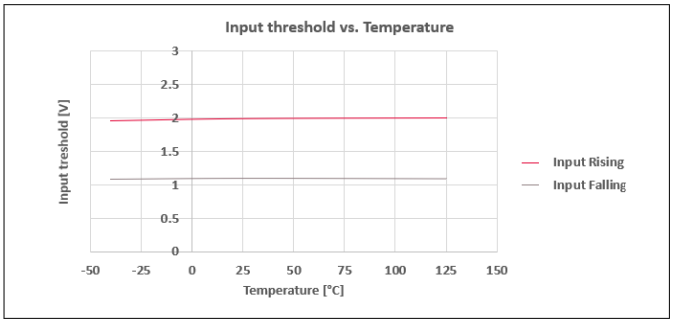

Figure 12 **Input thresholds vs. temperature**

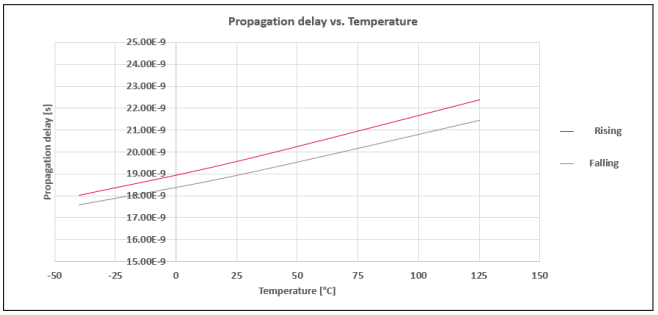

Figure 13 **Propagation delays vs. temperature**

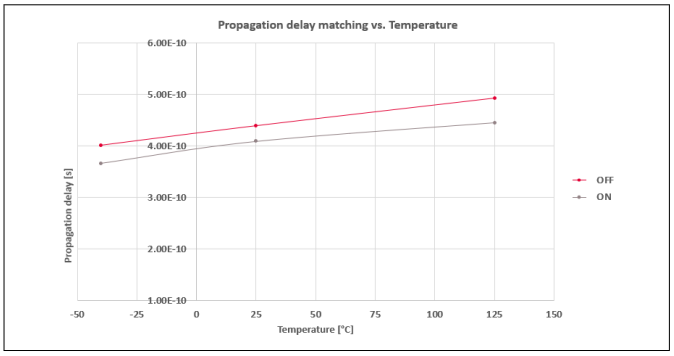

Figure 14 **Delay mismatches vs. temperature**

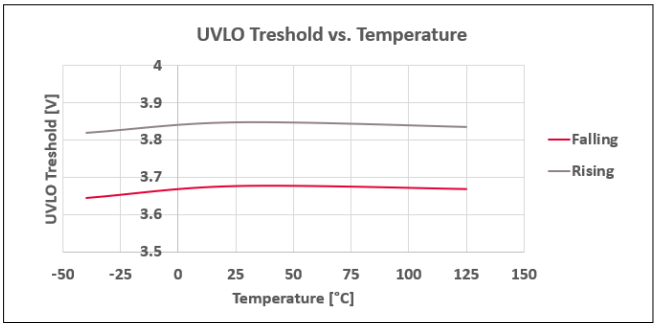

Figure 15 **VDDA/ VDDB UVLO vs. temperature**

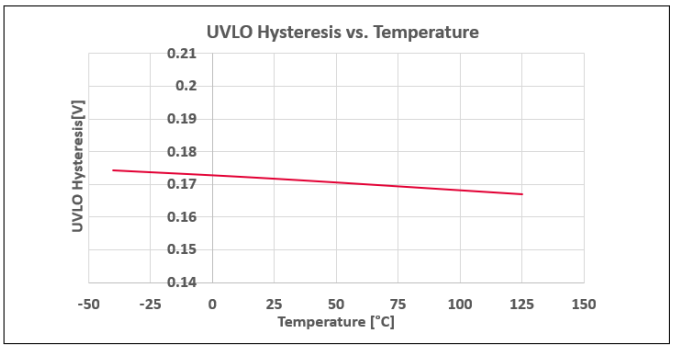

Figure 16 **VDDA/ VDDB UVLO hysteresis vs. temperature**

6 Application information

6.1 Typical application

The 2EDL6014AC can be used as a dual high-side driver or a dual low-side driver or a half-bridge driver. A typical application example of hybrid switched-capacitor converter (HSC) is given in Figure 17, where two 2EDL6014AC are used to drive four high-side MOSFETs(Q1, Q2, Q4 and Q5) and one 2EDL6014AC is used to drive two low-side MOSFETs(Q3 and Q6).

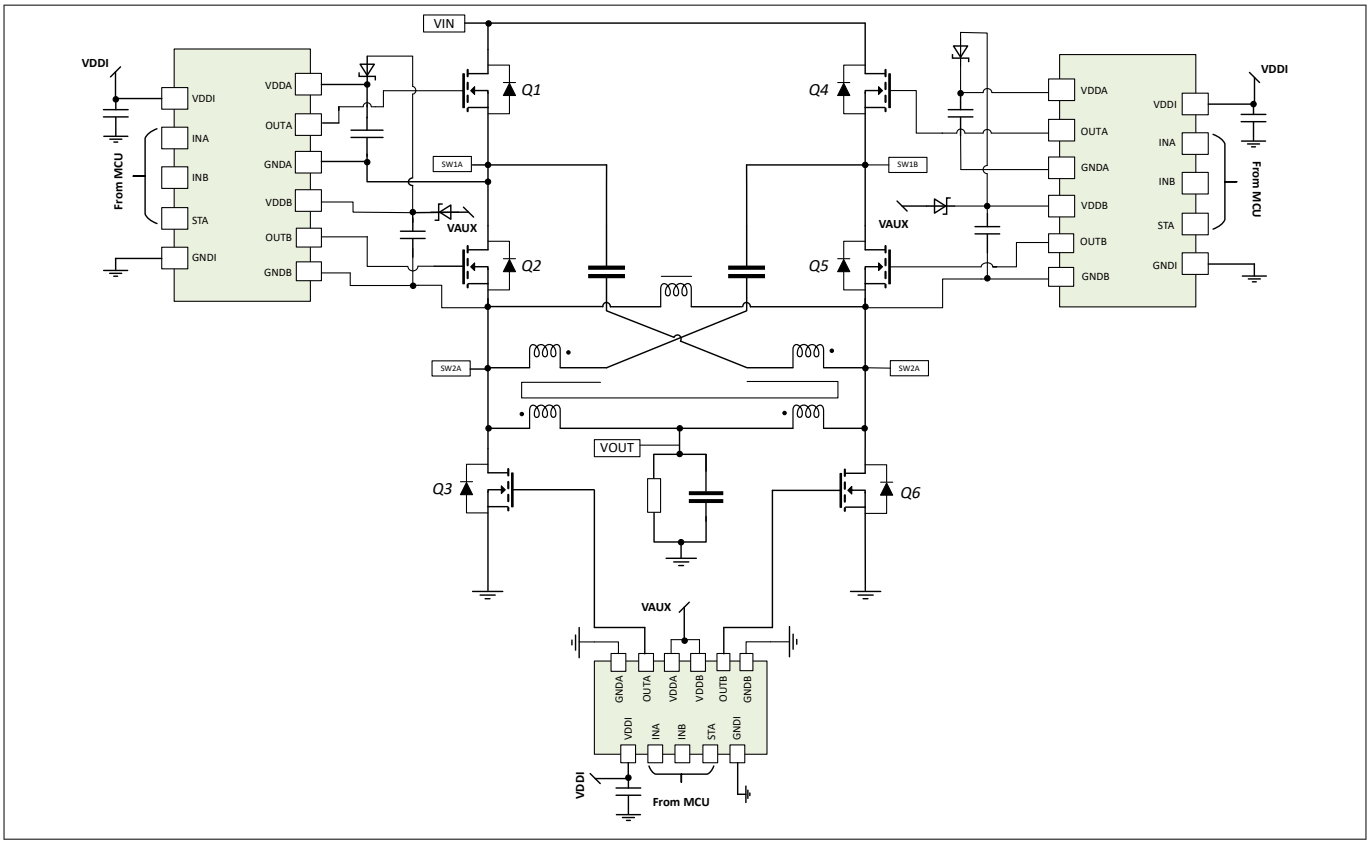

Figure 17 Hybrid switched-capacitor converter (HSC) with 2EDL6014AC-G2D

6.2 Design guidelines

In a half-bridge configuration, a high-side bias which is referenced to the switch node is needed in order to drive the gate of the high-side mosfet. One of the most common solutions, due to its simplicity and low cost, is the usage of a bootstrap circuit consisting of a diode and a capacitor as seen in Figure 18. However, this method imposes limitation on the power converter's duty cycle due to the requirement of recharging the bootstrap capacitor. This limitation can be mitigated through the proper selection of the bootstrap components.

The bootstrap circuit operation is defined by two main periods:

Charging period: When the low-side MOSFET(Q2) is ON and the high-side MOSFET(Q1) is OFF, the switch node SW is pulled to ground creating a charging path for the bootstrap capacitor(Cboot) through the Vdd bypass capacitor(CVdd) and the bootstrap diode.

Discharging period: When the low-side MOSFET(Q2) is turned OFF and the high-side MOSFET(Q1) starts conducting, the switch node SW is pulled to the high voltage Vbus, thus the bootstrap diode gets reverse biased. The bootstrap capacitor (Cboot) then discharges some of its stored charges to the gate of the high-side mosfet as well as to other contributing factors such as the mosfet's gate-source leakage current, floating

section quiescent current, floating section leakage current and the bootstrap diode reverse bias leakage current.

A typical waveform of the voltage across Cboot as a function of time is shown in Figure 19 where the different contributions have been distinguished. The voltage across Cboot increases during the charging period and then it falls with a high negative dV/dt as it charges the gate of the high-side MOSFET(Q1). The Cboot voltage continues to drop but with a much lower slope because only the high-side bias current and some leakage current is discharing the Cboot during this phase.

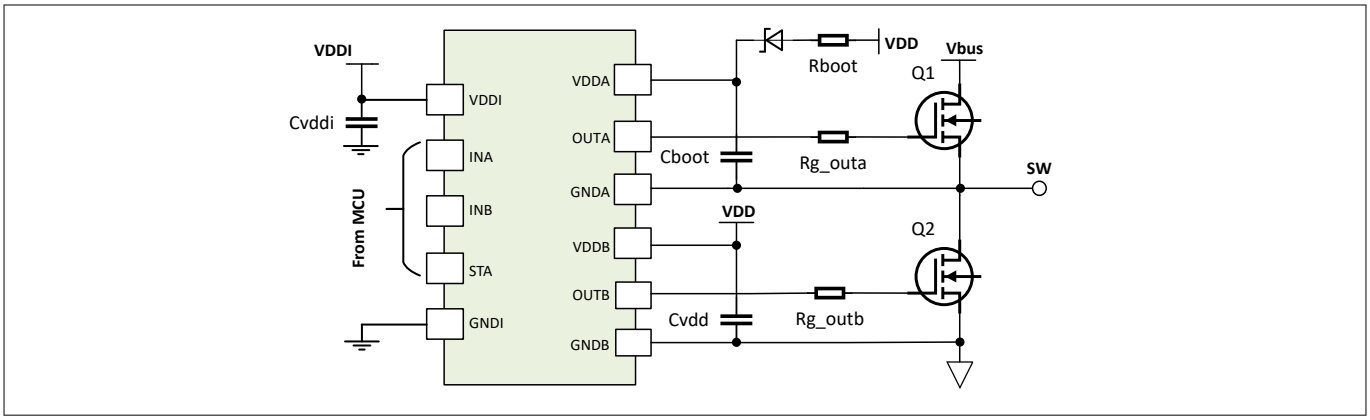

Figure 18 Half-bridge driver with 2EDL6014AC

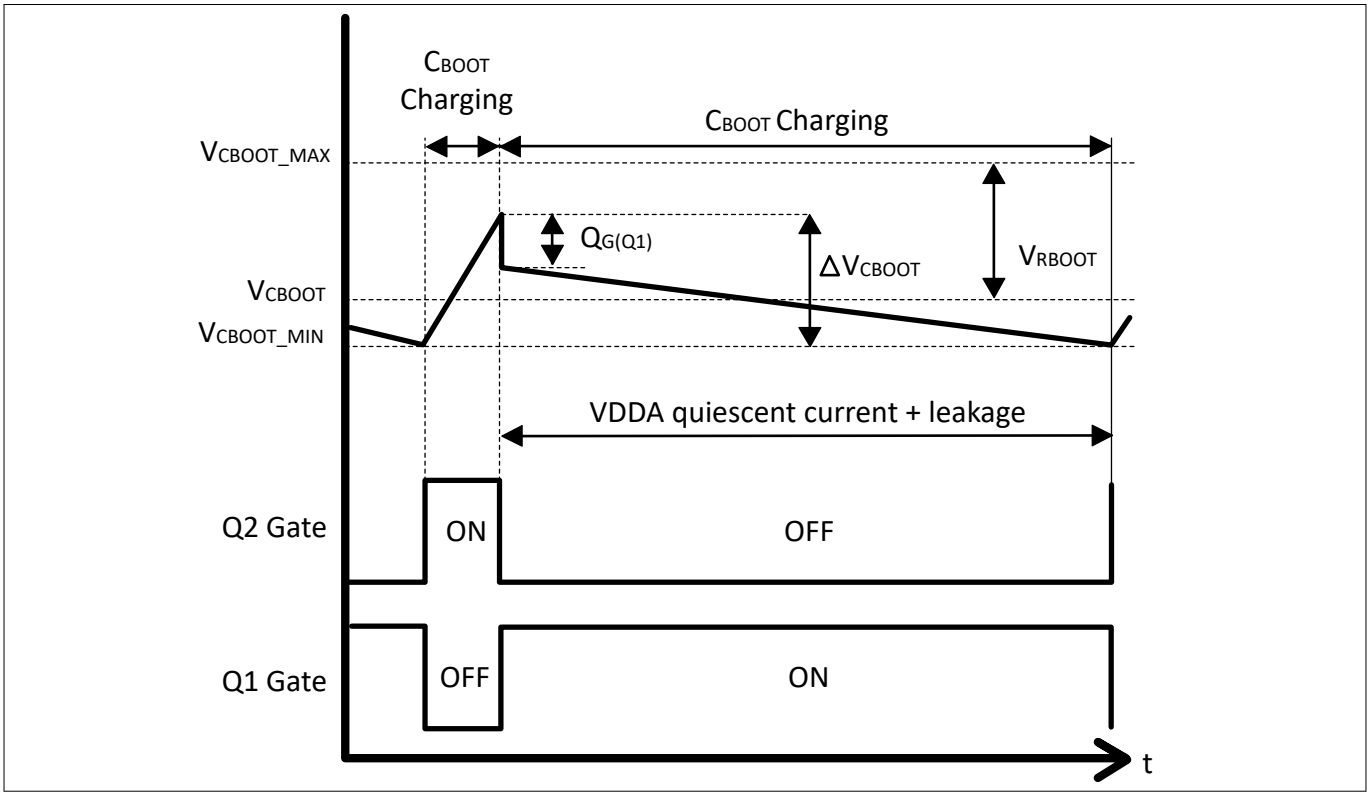

Figure 19 C_{BOOT} typical waveform

6.2.1 Selection of bootstrap capacitor

The bootstrap capacitor provides the necessary charge to drive the high-side MOSFET and thus it needs to be sized in such a way that the maximum voltage drop across this capacitor does not fall below the VDDA UVLO threshold during transient and normal operations. First, determine the maximum allowable voltage drop (ΔV_{Cboot_max}) when the high-side MOSFET (Q1) is on, which is given by the following formula:

$$\Delta V_{Cboot\_max} = V_{DD} - V_{FH} - V_{DDBR} - V_{DDBH}$$

Equation 1

Where:

V_{DD} = Gate driver supply voltage
V_{FH} = Bootstrap diode forward voltage drop at high current (worst case)
V_{DDBR} = VDDB UVLO rising threshold
V_{DDBH} = VDDB UVLO threshold hysteresis

Next, determine the total charge (Q_T) that must be delivered by the bootstrap capacitor at maximum duty cycle. As mentioned, there are several factors that contribute to the discharge of the bootstrap capacitor such as the Q1's total gate charge, Q1's gate-source leakage current, VDDB quiescent current, VDDB leakage current, bootstrap diode reverse bias leakage current and bootstrap capacitor leakage current (if using an electrolytic capacitor). For sake of simplicity, only Q1's total gate charge and VDDB quiescent and leakage current are considered as the other sources of leakage are negligible in comparison.

$$Q_T = Q_G + \frac{I_{VDDB}}{F_{sw}} + I_{VDDB-GNDI} \times \frac{D_{max}}{F_{sw}}$$

Equation 2

Where:

Q_G = high-side MOSFET (Q1) total gate charge
I_{VDDB} = VDDB maximum quiescent current
$I_{VDDB-GNDI}$ = VDDB to GNDI leakage current
D_{max} = maximum duty cycle
F_{sw} = switching frequency

The minimum bootstrap capacitor value can then be calculated using the formula:

$$C_{boot\_min} \geq \frac{Q_T}{\Delta V_{Cboot\_max}}$$

Equation 3

6.2.2 Selection of bypass capacitor

If the reference ground for VDDI and VDDA are different, we use a dedicated DC voltage supply for each. Normally, a flybuck converter as auxilliary circuit will do the job for the isolation. The VDDA bypass capacitor provides the charge for the bootstrap capacitor during the charging period. Selection of VDDA capacitor for 2EDL6014AC plays an important role in terms of stability of the gate driver especially during system startup condition. During system startup, VDDA rises from 0 V until it reaches V_{DDAR}. During this time, all internal circuitry nodes of the gate driver are floating. When V_{DDAR} is reached, the gate driver takes some settling time in order that all internal nodes to respond to its correct potential level. If the slew rate of the VDD is high, leakage voltage may appear on the outputs and may falsely turn-on the power switches. This is where the VDDA capacitor value plays a great role as capacitance is proportional to slew rate. The longer the rise time, the lower

leakage voltage seen on the output. It is therefore recommended to use a VDDA and VDDI capacitor with a minimum value of 100 nF to ensure that no false turn on the power switch will occur.

6.2.3 Selection of bootstrap resistor

In order to limit the bootstrap current during startup, it is suggested to series a bootstrap resistor. It limits the current in the external bootstrap diode during startup when the bootstrap capacitor is initially completely discharged. The peak current through this resistor is given by:

$$I_{Pk\_Rboot} = \frac{V_{DD} - V_{FH}}{R_{boot}}$$

Equation 4

The bootstrap resistor together with the bootstrap capacitor introduces a time constant and should be sized appropriately to achieve the desired start-up time. For this calculation, it is assumed that the bootstrap capacitor is fully charged after 4 time constant. With this, R_{boot} can be calculated using the following formula:

$$R_{boot} \leq \frac{t_{min}}{4 \times C_{boot}}$$

Equation 5

Where:

t_{min} = minimum on time of the mid-side MOSFET (Q2)

6.2.4 Selection of external bootstrap diode

For high dV/dT applications, a fast recovery or schottky diode with low forward voltage drop is recommended in order to minimize the losses and leakage current. It should be chosen such that it can handle the peak transient current from Equation (4) during start-up conditions and the blocking voltage rating should be higher than the maximum input voltage (V_{in}) with enough derating.

6.2.5 Selection of gate resistor

The turn-on and turn-off external gate resistors control the turn-on and turn-off current of the gate driver. It provides an external way to control the switching speed of the MOSFET for purposes such as voltage overshoot control, ringing reduction, EMI mitigation, spurious turn-on protection, shoot –through protection etc. The following formulas show the effect of the external gate resistor to the output current capability of the gate driver.

$$I_{OUTBSRC} = \frac{V_{DDA} - V_F}{R_{PUOUTB} + R_{G\_OUTB} + R_{G\_int}}$$

Equation 6

$$I_{OUTBSNK} = \frac{V_{DDA} - V_F}{R_{PDOUTB} + R_{G\_OUTB} + R_{G\_int}}$$

Equation 7

$$I_{OUTASRC} = \frac{V_{DDA}}{R_{PUOUTA} + R_{G\_OUTA} + R_{G\_int}}$$

Equation 8

$$I_{OUTASNK} = \frac{V_{DDA}}{R_{PDOUTA} + R_{G\_OUTA} + R_{G\_int}}$$

Equation 9

Where:

$I_{OUTBSRC}$ = OUTB peak source current
$I_{OUTBSNK}$ = OUTB peak sink current
$I_{OUTASRC}$ = OUTA peak source current
$I_{OUTASNK}$ = OUTA peak sink current
R_{PUOUTB} = OUTB pull-up resistance
R_{PDOUTB} = OUTB pull-down resistance
R_{PUOUTA} = OUTA pull-up resistance
R_{PDOUTA} = OUTA pull-down resistance
V_{DDA} = Gate driver supply voltage for VDDA pin
V_F = Bootstrap diode forward voltage drop
R_{G_OUTB} = OUTB external gate resistance
R_{G_OUTA} = OUTA external gate resistance
R_{G_int} = MOSFET internal gate resistance

6.3 PCB layout guidelines

To maximize the performance of EiceDRIVER™ 2EDL6014AC-G2D, below are some recommendations on how to optimize the PCB layout:

- Use a low-ESR decoupling capacitors on VDDI-GNDI, VDDA-GNDA and VDDB-GNDB and placed it as close as possible to the corresponding pins of the driver
- An option for a series boot resistor is recommended to control the uppermost-side MOSFET slew rate and therefore the mid-side MOSFET overshoot. The boot loop path including the VDDA capacitor, boot diode, boot series resistor and boot capacitor should be as small as possible
- It is recommended to have an external boot diode placement for high dv/dt application.
- Placement for the gate resistor is also recommended to control the switching speed of the MOSFET. Both the gate resistor and the MOSFET should be placed as close as possible to the driver to minimize the gate loop inductance.
- Use a copper plane underneath the exposed GNDI pad of the driver and connect it to the buried copper plane(s) with multiple thermal vias for better heat dissipation into the PCB.
- The connection of the GNDA and GNDB of the driver to its corresponding switching nodes should be as short and wide as possible and avoid connecting it directly through the high switching current path.
- OUTA and OUTB traces should be as short and wide as possible
- Avoid letting the INA and INB signal trace to come close to high dV/dT traces which might induce significant noise.

7 Package information

Notes

1. For further information on package types, recommendation for board assembly, please go to: www.infineon.com\packages

Notes

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7.1 Ordering information

Base part number	Package type	Standard pack		Orderable part number	Marking code
		Form	Quantity		
2EDL6014AC-G2D	WQFN11-2.2x2.2	Tape and Reel			2EDL60YXX

7.2 Outline dimensions

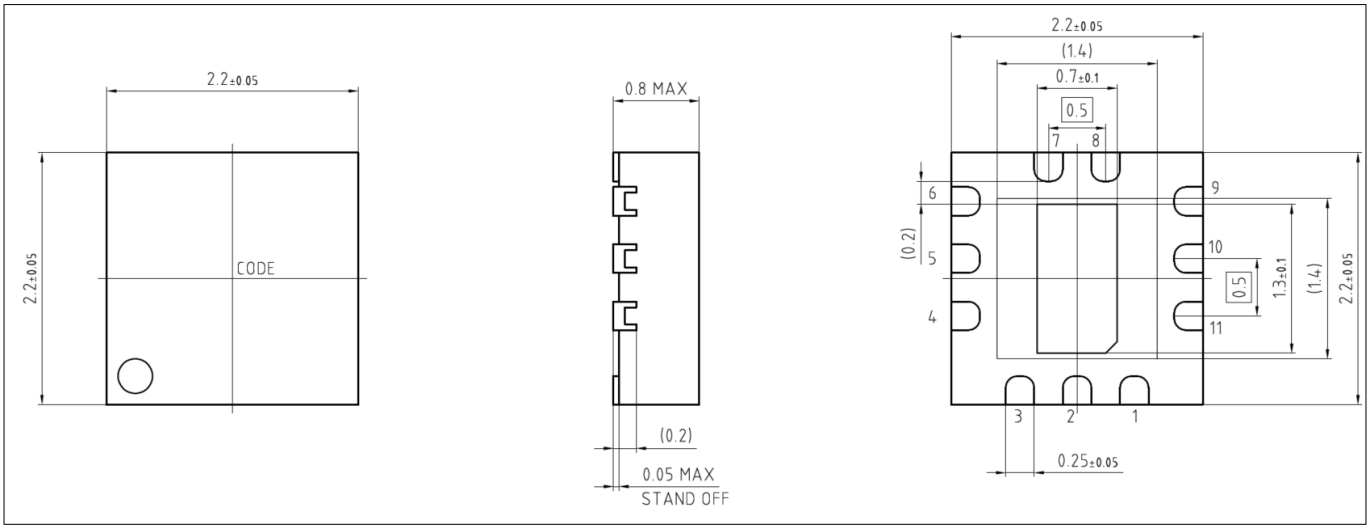

Figure 20 WQFN-12 outline dimensions

7.3 Footprint dimensions

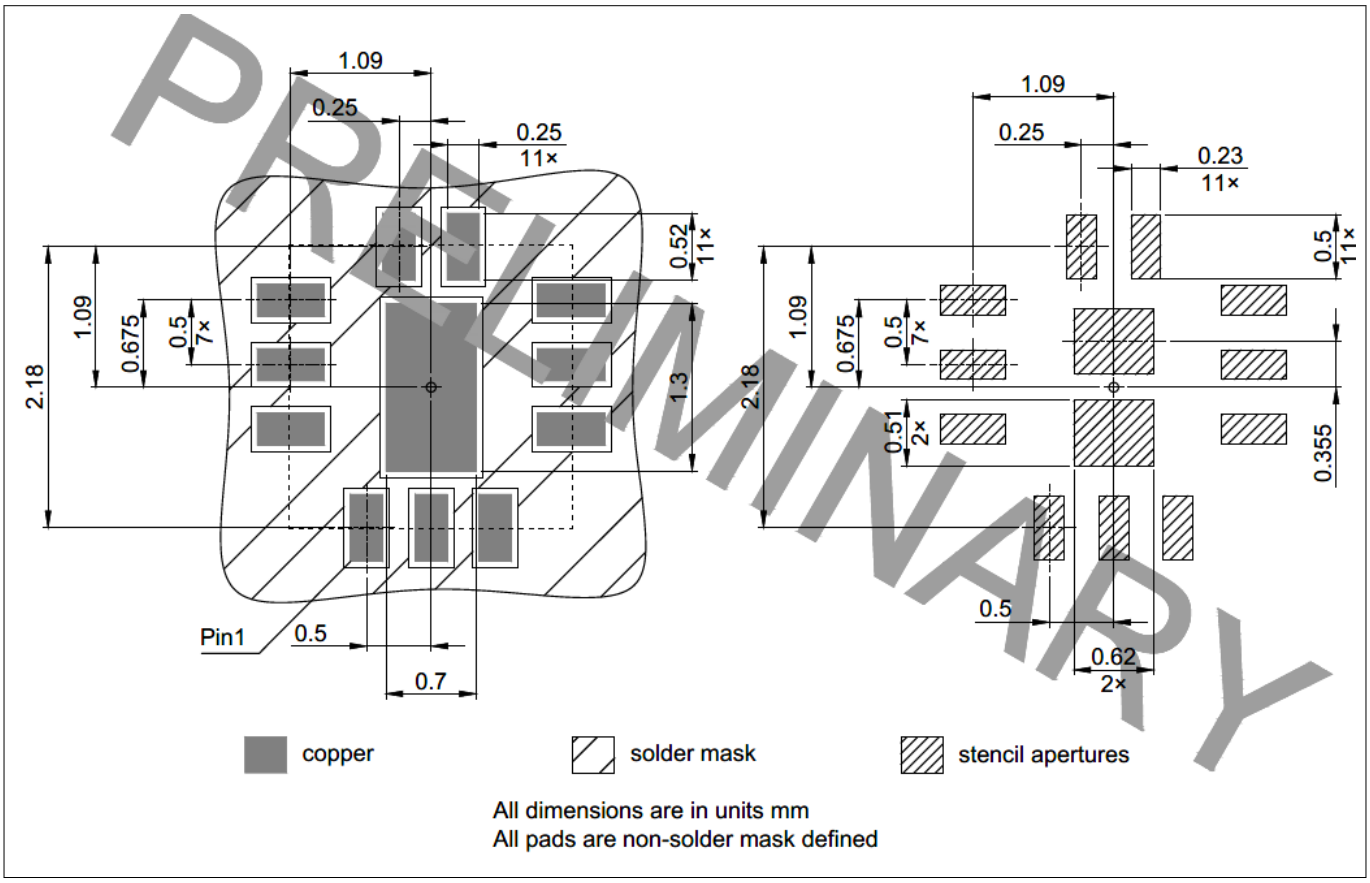

Figure 21 WQFN-12 footprint dimensions

8 Revision history

Revision	Date	Description of changes
0.1	2024-11-01	Initial release
0.2	2025-01-09	Added device marking
0.3	2025-01-30	Renamed the pin name
0.4	2025-08-20	Added e-pad description
0.5	2025-12-09	Preliminary datasheet release

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Edition 2026-03-10

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference
IFX-odn1721216502433

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