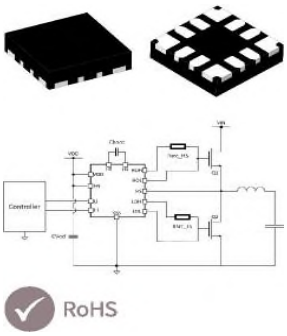
120 V, 1.5 A and 4 A, half-bridge GaN and LL MOSFET driver IC



Features

- Dual independent inputs
- UVLO for both high- and low-side drivers
- Integrated bootstrap switch
- Active bootstrap switch to avoid bootstrap capacitor overcharging during deadtime
- Absolute maximum bootstrap voltage of 120 V
- Split outputs for adjustable turn-on/turn-off driving strength
- 4 A/4 A (2EDL5014AA), 1.5 A/4 A (2EDL5012AA) and 1.5 A/1.5 A (2EDL5011AA) peak source/
sink current capability
- Built-in active Miller clamp
- 20 ns typical propagation delay
- 1 ns typical propagation delay matching
- 4.5 V to 5.5 V supply voltage operating range
- Offered in TSNP-12 2x2 package

Potential applications

- Telecom/Datacom half- and full-bridge power converters
- Buck converters
- Two switch forward converters
- Active clamp forward converters
- Class D amplifiers
- Class D wireless charging

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The 2EDL501XAA-U2D is a half-bridge gate driver designed to drive both the high-side and the low-side enhancement mode GaN transistors as well as logic level MOSFETs in a synchronous buck or half-bridge configuration. The floating high-side driver is capable of driving a high-side GaN or MOSFET operating up to 120 V bootstrap voltage. The high-side bias voltage is generated using a bootstrap technique via the internal bootstrap switch which is controlled by the low side PWM. An active clamp mechanism is implemented to avoid overcharging the bootstrap capacitor during deadtime and thus from exceeding the maximum allowable gate to source voltage rating of GaN transistors. The inputs of the driver are TTL logic compatible and can withstand input voltage of up to 7 V. The gate outputs are split to provide flexibility in adjusting the turn on and turn off strength independently and an active miller clamp is implemented on both outputs to avoid induced turn-on phenomenon.

2EDL5012AA provides 1.5 A peak source and 4 A peak sink current capability while 2EDL5011AA and 2EDL5014AA provides 1.5 A and 4 A peak respectively for both source and sink current. The 2EDL501XAA-U2D is available in TSNP-12 pins 2 mm x 2 mm package.

Part number	Peak source/sink current	Package
2EDL5011AA-U2D	1.5 A/1.5 A	PG-TSNP-12-6, 2 x 2 mm
2EDL5012AA-U2D	1.5 A/4 A	PG-TSNP-12-6, 2 x 2 mm
2EDL5014AA-U2D	4 A/4 A	PG-TSNP-12-6, 2 x 2 mm

Table 1 Device information

Table of contents

1 Pin configuration and description

1.1 Pin configuration

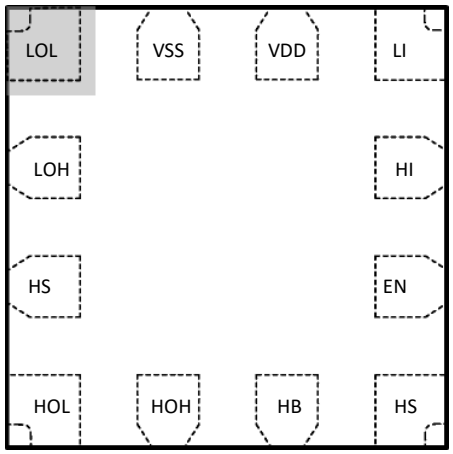


Figure 3 PG-TSNP-12-6, Top transparent view

1.2 Pin description

Table 3 Pin description

Pin number	Symbol	Description
1	LOL	Low-side gate driver sink current output
2	LOH	Low-side gate driver source current output
3,7	HS	High-side source connection, internally connected
4	HOL	High-side gate driver sink current output
5	HOH	High-side gate driver source current output
6	HB	High-side gate driver bootstrap rail
8	EN	Enable input. When this pin is high or left-open, it enables the driver. If pulled low, it disables the driver
9	HI	High-side PWM input
10	LI	Low-side PWM input
11	VDD	5 V gate drive supply
12	VSS	Ground return

2 Block diagram

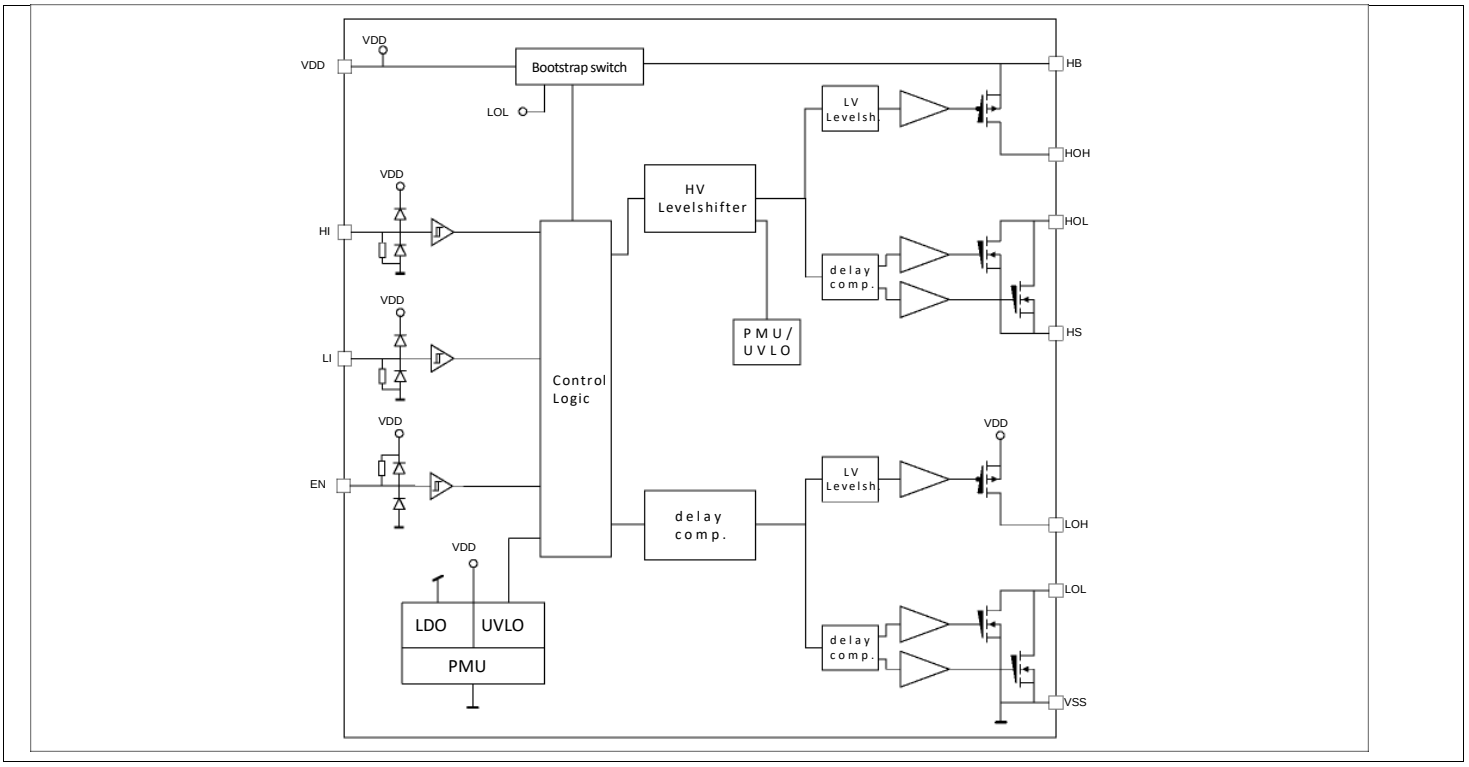


Figure 4 Block diagram

3 Functional description

The 2EDL501XAA-U2D is a fast half-bridge driver for both high-side and low-side enhancement mode GaN transistors as well as logic level MOSFETs in a synchronous buck or half-bridge configuration. The output stages with very low output impedance and high current capability are chosen to ensure highest flexibility and cover a wide range of applications. The focus on robustness at the input and output side additionally gives this device a safety margin in critical abnormal situations. All outputs are robust against reverse current. The interaction with the power switch, even reverse reflected power will be handled by the strong internal output stage. All inputs are compatible with LV_TTL signal levels. Since the 2EDL501XAA-U2D aims at fast-switching applications, signal delays and rise/fall times have been minimized. Special effort has been made towards minimizing delay differences between the high-side and low-side to values of typically 1 ns.

3.1 Input stage

2EDL501XAA features independent inputs LI and HI which control the LO and HO outputs respectively. The input signal is transferred non-inverted to the corresponding gate driver output. All inputs are compatible with LV-TTL threshold levels and provide a hysteresis of typically 1.2 V. The hysteresis is independent of the supply voltage VDD. The HI and LI inputs are internally pulled down with a 200 kΩ typical pull-down resistor. In case the controller signals have an undefined state during the power-up sequence, the gate driver outputs are forced to the "off" state (low). The input signals are filtered to avoid pulses with a duration shorter than typically 3.5 ns from being propagated to the output. Table 4 shows the truth table of the device once the two UVLOs are above the rising threshold. In case the VDD-VSS voltage or HB-HS voltage is below the UVLO threshold, the corresponding output is low.

Table 4 Truth table

EN	LI	HI	LO	HO
L	L	L	L	L
	H	L	L	L
	L	H	L	L
	H	H	L	L
H	L	L	L	L
	H	L	H	L
	L	H	L	H
	H	H	H	H

3.2 Enable

The EN pin enables or disables the outputs of the driver. The outputs are active when the voltage at the EN pin is above the rising threshold and are disabled when the EN pin voltage falls below the falling threshold. An internal 200 kΩ pull-up resistor connects the EN pin to VDD thus leaving the EN pin floating enables the outputs. If the EN pin is not needed, it is recommended to connect it to VDD especially for high-noise system. Externally pulling the EN pin to ground disables the outputs. The EN input stage has built-in hysteresis for enhanced noise immunity.

3.3 Supply voltage and undervoltage lockout (UVLO)

The absolute maximum supply voltage is 7 V for both VDD and HB-HS and the minimum operating supply voltage is set by the under voltage lockout function. The under voltage lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO rising threshold voltage. Thus, it can be guaranteed that the switch transistor is not switched on if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation. The UVLO level is set to a typical value of 3.9 V for VDD and 3.7 V for HB-HS. The maximum value of the rising edge is the value that ensures all the device among the production will be turned on during startup; that means designers have to provide a voltage higher than 4.1 V for VDD and 3.9 V for HB-HS to turn on all the devices in the production of their equipment within the specified temperature range. On the

opposite side, the minimum voltage necessary to switch off all the devices is the minimum of the falling edge. Therefore to be sure that all the devices in production are turned off in the specified temperature range, a voltage lower than 3.5 V for VDD and 3.3 V for HB-HS has to be provided. A 200 mV hysteresis is implemented on both supplies to ensure some margin on noise effect like false turn off. For instance, a negative glitch smaller than the hysteresis does not have an effect on the device preventing an unwanted turn off.

3.4 Unpowered gate clamp

The unpowered gate clamp circuit ensures that the driver outputs are pulled low when there is no sufficient supply voltage applied to the driver (below UVLO). When the voltage on the output stage (LOL/HOL) reached 1 V, the gate clamp circuit sinks 100 mA peak current for the low-side and 10 mA peak current for the high-side. If the supply voltage is already sufficient (above UVLO), the gate clamp circuit is deactivated.

3.5 Active bootstrap switch

Generating the high-side supply voltage can be done via the internal bootstrap switch. If the low-side input PWM is high and the low-side output reaches about 1.7 V, the bootstrap switch turns ON after a delay of about 14.5 ns and connects to the VDD rail thus allowing the bootstrap capacitor to be charged. When supplying the high-side driver using this bootstrap technique, it is necessary to regulate the bootstrap capacitor voltage when driving a GaN transistor to avoid exceeding its maximum allowable gate-to-source voltage which is usually at 6 V to 7 V. Overcharging of the bootstrap capacitor can easily occur during the deadtime of the converter where the low-side GaN operates in the third quadrant. During the third quadrant operation, the voltage drop (V_{SD}) across the GaN is usually higher compared with a MOSFET's body diode drop which causes a significant negative voltage on the HS pin. To solve this problem, the bootstrap switch turns OFF about 1.5 ns before the low-side output goes low thereby avoiding the overcharge of the bootstrap capacitor. Due to the way the bootstrap switch is implemented, the bootstrap switch turn on time is reduced typically by 16 ns compared with the low-side input PWM pulse width with a maximum reduction of 40 ns at 5 V VDD supply voltage and across the full operating temperature range.

3.6 Driver outputs

The strong peak source current capability of 1.5 A (2EDL5011AA and 2EDL5012AA) and 4 A (2EDL5014AA) and strong peak sink current capability of 1.5 A (2EDL5011AA) and 4 A (2EDL5012AA and 2EDL5014AA) allow for faster switching of the power device thus leading to lower switching losses. The output impedance is very low with a typical value of 1.7 Ω (2EDL5011AA and 2EDL5012AA) and 0.7 Ω (2EDL5014AA) for the sourcing p-channel MOS and 1.2 Ω (2EDL5011AA) and 0.47 Ω (2EDL5012AA and 2EDL5014AA) for the sinking n-channel MOS transistor. The output is split to provide flexibility in adjusting the turn-on and turn-off strength independently. Gate drive outputs are held low in case of floating inputs V_{HI}, V_{LI} or during startup or power down once UVLO is not exceeded. Under UVLO condition, the outputs can still be actively pulled down if the supply voltage is > 1.25 V.

3.7 Active Miller clamp

Active Miller clamp feature is added on both the low-side and high-side output to provide immunity against induced turn-on caused by high dv/dt or high di/dt event. The peak sink current increases by 5 A when the gate to source voltage falls below the miller clamp activation threshold of 1 V typical, as can be seen in the LO/HO source and sink current vs. output voltage graph in the Typical characteristics section, with an equivalent total pull-down resistance of 0.32 Ω for 2EDL5011AA and 0.27 Ω for both 2EDL5012AA and 2EDL5014AA after a 5 ns activation delay time.

3.8 Minimum ON time

The device responds to input level according to the truth table in the input stage section as long as the logic signal complies with the minimum pulse width requirement. Signal pulse longer than the minimum allowable input pulse yields valid output. Any output in response to shorter pulses or glitches must be disregarded and filtered out by the user. Under all allowable operation above the shortest input pulse width of 10 ns, the output behaves one to one to the input with minimal pulse width distortion.

4 General product characteristics

4.1 Absolute maximum ratings

Table 5 Absolute maximum ratings

Stresses above the values listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. All voltage parameters are referenced to V_{SS} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply input voltage	V_{DD}	-0.3	–	7	V	–
High-side supply voltage	V_{HB-HS}	-0.3	–	7	V	Referenced to V_{HS}
High-side bootstrap voltage	V_{HB}	-0.3	–	120	V	1)
Phase voltage	V_{HS}	-5	–	V_{HB} + 0.3	V	1) V_{HB-HS} = 5 V
HI, LI and EN input voltage	V_{HI}, V_{LI}, V_{EN}	-0.3	–	V_{DD} + 0.3	V	–
Output voltage on LOL, LOH	V_{LOL}, V_{LOH}	-0.3	–	V_{DD} + 0.3	V	–
Output voltage on HOL, HOH	V_{HOL}, V_{HOH}	V_{HS} - 0.3	–	V_{HB} + 0.3	V	–
Operating junction temperature	T_J	-40	–	150	°C	–
Storage temperature	T_S	-55	–	150	°C	–
ESD robustness (HBM)	V_{ESD_HBM}	-2	–	2	kV	Human Body Model sensitivity as per ANSI/ESDA/ JEDEC JS-001
ESD robustness (CDM)	V_{ESD_CDM}	-1	–	1	kV	Charged Device Model sensitivity as per ANSI/ESDA/ JEDEC JS-002

1) Not subject to production test. Verified by design/characterization.

4.2 Recommended operating conditions

Table 6 Recommended operating conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to V_{SS} unless otherwise specified..

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply input voltage	V_{DD}	4.5	5	5.5	V	–
High-side supply voltage	V_{HB-HS}	4	5	5.5	V	Referenced to V_{HS}
High-side bootstrap voltage	V_{HB}	-0.3	–	110	V	–
Phase voltage	V_{HS}	-5	–	V_{HB} - V_{DD}	V	V_{HB-HS} = 5 V

(table continues...)

Table 6 (continued) Recommended operating conditions

The following operating conditions must not be exceeded to ensure correct operation and reliability of the device. All voltage parameters are referenced to V_{SS} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HI, LI and EN input voltage	V_{HI}, V_{LI}, V_{EN}	0	–	V_{DD}	V	–
Low-side output voltage	V_{LOL}, V_{LOH}	0	–	V_{DD}	V	–
High-side output voltage	V_{HOL}, V_{HOH}	V_{HS}	–	V_{HB}	V	–
HS slew rate	$HS_{dV/dT}$	–	–	100	V/ns	–
Junction temperature range	T_J	-40	–	125	°C	–

4.3 Thermal resistance

Table 7 Thermal resistance

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction-to-case thermal resistance	R_{thJC}	–	19	–	°C/W	Bottom
Junction-to-case thermal resistance	R_{thJC}	–	95	–	°C/W	Top
Junction-to-board thermal resistance	R_{thJB}	–	50	–	°C/W	–
Junction-to-ambient thermal resistance	R_{thJA}	–	66	–	°C/W	1) Device soldered on PCB

1) Device on 76.2 mm x 76.2 mm x 1.5 mm epoxy PCB FR4 (JEDEC 2s2p) with thermal vias. PCB vertical in still air.

4.4 Electrical characteristics

Table 8 Electrical characteristics

Unless otherwise specified: $V_{DD} = V_{HB} = 5$ V, $V_{HS} = V_{SS} = 0$ V and no load on the outputs. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Supply current

Parameter	Symb	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction-to-case thermal	R_{thJC}	–	19	–	°C/W	Bottom
VDD operating current	$'_{OVDD}$	–	3.8	4.4	mA	$f_{sw} = 500$ kHz, $C_{load} = 1$ nF
HB quiescent current	$'_{QHB}$	–	100	150	µA	V_{LI}, V_{HI} and $V_{EN} = 0$ V
HB operating current	$'_{OHB}$	–	3.2	4.2	mA	$f_{sw} = 500$ kHz, $C_{load} = 1$ nF

(table continues...)

Table 8 (continued) Electrical characteristics

Unless otherwise specified: V_{DD} = V_{HB} = 5 V, V_{HS} = V_{SS} = 0 V and no load on the outputs. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at T_C = 25°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HB to VSS leakage current	I_{QHBS}	–	0.1	10	µA	V_{HS} = V_{HB} = 100 V V_{LI} = V_{HI} = V_{EN} = 0 V
HI and LI input						
Input voltage rising threshold	V_H	1.9	2.25	2.55	V	–
Input voltage falling threshold	V_L	0.9	1.1	1.4	V	–
Input voltage hysteresis	V_{HYS}	–	1.2	–	V	–
Input pull down resistance	R_{IN}	100	200	300	kI	–
Enable						
Enable input rising threshold	V_{EN}	1.9	2.25	2.55	V	–
Enable input falling threshold	V_{DIS}	0.9	1.1	1.4	V	–
Enable voltage hysteresis	V_{ENHYS}	–	1.2	–	V	–
Enable pull up resistance	R_{EN}	100	200	300	kI	–
Enable high delay	t_{ENH_LO}, t_{ENH_HO}	–	20	35	ns	V_{EN} = 2.8 V
Enable low delay	t_{ENL_LO}, t_{ENL_HO}	–	20	35	ns	V_{EN} = 0 V
Undervoltage lockout						
VDD UVLO rising threshold	V_{DDR}	3.7	3.9	4.1	V	–
VDD UVLO falling threshold	V_{DDF}	3.5	3.7	3.9	V	–
VDD UVLO threshold hysteresis	V_{DDH}	–	0.2	–	V	–
VHB UVLO rising threshold	V_{HBR}	3.5	3.7	3.9	V	–
VHB UVLO falling threshold	V_{HBF}	3.3	3.5	3.7	V	–
VHB UVLO threshold hysteresis	V_{HBH}	–	0.2	–	V	–
Bootstrap switch						
Bootstrap switch high current forward voltage	V_{DH}	–	0.56	0.93	V	I_{VDD-HB} = 100 mA
Bootstrap switch low current forward voltage	V_{DL}	–	1	10	mV	I_{VDD-HB} = 100 uA
Bootstrap switch resistance	R_{BS}	–	5.6	9.3	I	I_{VDD_HB} = 100 mA

(table continues...)

Table 8 (continued) Electrical characteristics

Unless otherwise specified: V_{DD} = V_{HB} = 5 V, V_{HS} = V_{SS} = 0 V and no load on the outputs. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at T_C = 25°C.

Low-side gate driver

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Peak source current	$'_{LSRC}$	–	1.5	–	A	1) V_{LOH} = 0 V, 2EDL5011AA and
Peak source current	$'_{LSRC}$	–	4	–	A	1) V_{LOH} = 0 V, 2EDL5014AA
Peak sink current	$'_{LSNK}$	–	4	–	A	1) V_{LOL} = 5 V, 2EDL5012AA and
Peak sink current	$'_{LSNK}$	–	1.5	–	A	1) V_{LOL} = 5 V, 2EDL5011AA
Pull up resistance	R_{LPU}	–	1.7	2.95	Ω	$'_{LOH}$ = -100 mA, 2EDL5011AA and 2EDL5012AA
Pull up resistance	R_{LPU}	–	0.7	1	Ω	$'_{LOH}$ = -100 mA, 2EDL5014AA
Pull down resistance	R_{LPD}	–	0.47	0.75	Ω	2) $'_{LOL}$ = 100 mA, 2EDL5012AA and 2EDL5014AA
Pull down resistance	R_{LPD}	–	1.2	2	Ω	2) $'_{LOL}$ = 100 mA, 2EDL5011AA
Output clamp capability	$'_{OUTL\_CLAMP}$	-	100	-	mA	V_{DD} = open, V_{LOL} = 1 V
High-side gate driver						
Peak source current	$'_{HSRC}$	–	1.5	–	A	1) V_{HOH} = 0 V, 2EDL5011AA and 2EDL5012AA
Peak source current	$'_{HSRC}$	–	4	–	A	1) V_{HOH} = 0 V, 2EDL5014AA
Peak sink current	$'_{HSNK}$	–	4	–	A	1) V_{HOL} = 5 V, 2EDL5012AA and 2EDL5014AA
Peak sink current	$'_{HSNK}$	–	1.5	–	A	1) V_{HOL} = 5 V, 2EDL5011AA
Pull up resistance	R_{HPU}	–	1.7	2.9	Ω	$'_{HOH}$ = -100 mA, 2EDL5011AA and 2EDL5012AA
Pull up resistance	R_{HPU}	–	0.65	0.95	Ω	$'_{HOH}$ = -100 mA, 2EDL5014AA
Pull down resistance	R_{HPD}	–	0.47	0.75	Ω	2) $'_{HOL}$ = 100 mA, 2EDL5012AA and 2EDL5014AA
Pull down resistance	R_{HPD}	–	1.2	2	Ω	2) $'_{HOL}$ = 100 mA, 2EDL5011AA
Output clamp capability	$'_{OUTH\_CLAMP}$	–	10	–	mA	V_{DD} = open, V_{HOL} = 1 V
Output Miller clamp (LOL and HOL)						
Miller clamp activation threshold	V_{MILLER}	–	1	–	V	1)
Miller clamp activation delay	t_{MILLER}	–	5	11	ns	1)

(table continues...)

Table 8 (continued) Electrical characteristics

Unless otherwise specified: $V_{DD} = V_{HB} = 5$ V, $V_{HS} = V_{SS} = 0$ V and no load on the outputs. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Peak sink current during Miller clamp activation	$'_{SNK\_OFF}$	–	9	–	A	1) V_{LOL}, V_{HOL} = 5 V, 2EDL5012AA and 2EDL5014AA
Peak sink current during Miller clamp activation	$'_{SNK\_OFF}$	–	6.5	–	A	1) V_{LOL}, V_{HOL} = 5 V, 2EDL5011AA
Pull down resistance during Miller clamp activation	R_{PD_OFF}	–	0.27	0.45	Ω	$'_{LOL}$, $'_{HOL}$ = 100 mA, 2EDL5012AA and 2EDL5014AA
Pull down resistance during Miller clamp activation	R_{PD_OFF}	–	0.32	0.55	Ω	$'_{LOL}$, $'_{HOL}$ = 100 mA, 2EDL5011AA

1) Not subject to production test. Verified by design/characterization.

2) Verified by design.

4.5 Switching characteristics

Table 9 Switching characteristics

Unless otherwise specified: $V_{DD} = V_{HB} = 5$ V, $V_{HS} = V_{SS} = 0$ V and no load on the outputs. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Propagation delay and delay matching

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
LO rising propagation delay	t_{LLH}	–	20	35	ns	C_{load} = 0, LI rising to LOH rising
LO falling propagation delay	t_{LHL}	–	20	35	ns	C_{load} = 0, LI falling to LOL falling
HO rising propagation delay	t_{HLH}	–	20	35	ns	C_{load} = 0, HI rising to HOH rising
HO falling propagation delay	t_{HHL}	–	20	35	ns	C_{load} = 0, HI falling to HOL falling
Delay matching LO on and HO off	t_{DMON}	–	1	3.5	ns	Between LO rising and HO falling
Delay matching LO off and HO on	t_{DMOFF}	–	1	3.5	ns	Between LO falling and HO rising

(table continues...)

Table 9 (continued) Switching characteristics

Unless otherwise specified: V_{DD} = V_{HB} = 5 V, V_{HS} = V_{SS} = 0 V and no load on the outputs. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at T_C = 25°C.

Output rise and fall time

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
HO rise time	t_{HRC}	–	6.5	–	ns	1) C_{load} = 1 nF, 10% to 90%, 2EDL5011AA and 2EDL5012AA
HO rise time	t_{HRC}	–	3.9	–	ns	1) C_{load} = 1 nF, 10% to 90%, 2EDL5014AA
LO rise time	t_{LRC}	–	6.7	–	ns	1) C_{Load} = 1 nF, 10% to 90%, 2EDL5011AA and 2EDL5012AA
LO rise time	t_{LRC}	–	4.1	–	ns	1) C_{Load} = 1 nF, 10% to 90%, 2EDL5014AA
HO fall time	t_{HFC}	–	4.1	–	ns	1) C_{Load} = 1 nF, 90% to 10%, 2EDL5012AA and 2EDL5014AA
HO fall time	t_{HFC}	–	6.2	–	ns	1) C_{Load} = 1 nF, 90% to 10%, 2EDL5011AA
LO fall time	t_{LFC}	–	4.1	–	ns	1) C_{Load} = 1 nF, 90% to 10%, 2EDL5012AA and 2EDL5014AA
LO fall time	t_{LFC}	–	6.2	–	ns	1) C_{Load} = 1 nF, 90% to 10%, 2EDL5011AA
Shortest input pulse width transferred to the output	t_{PW}	–	5	10	ns	-

5 Timing diagrams

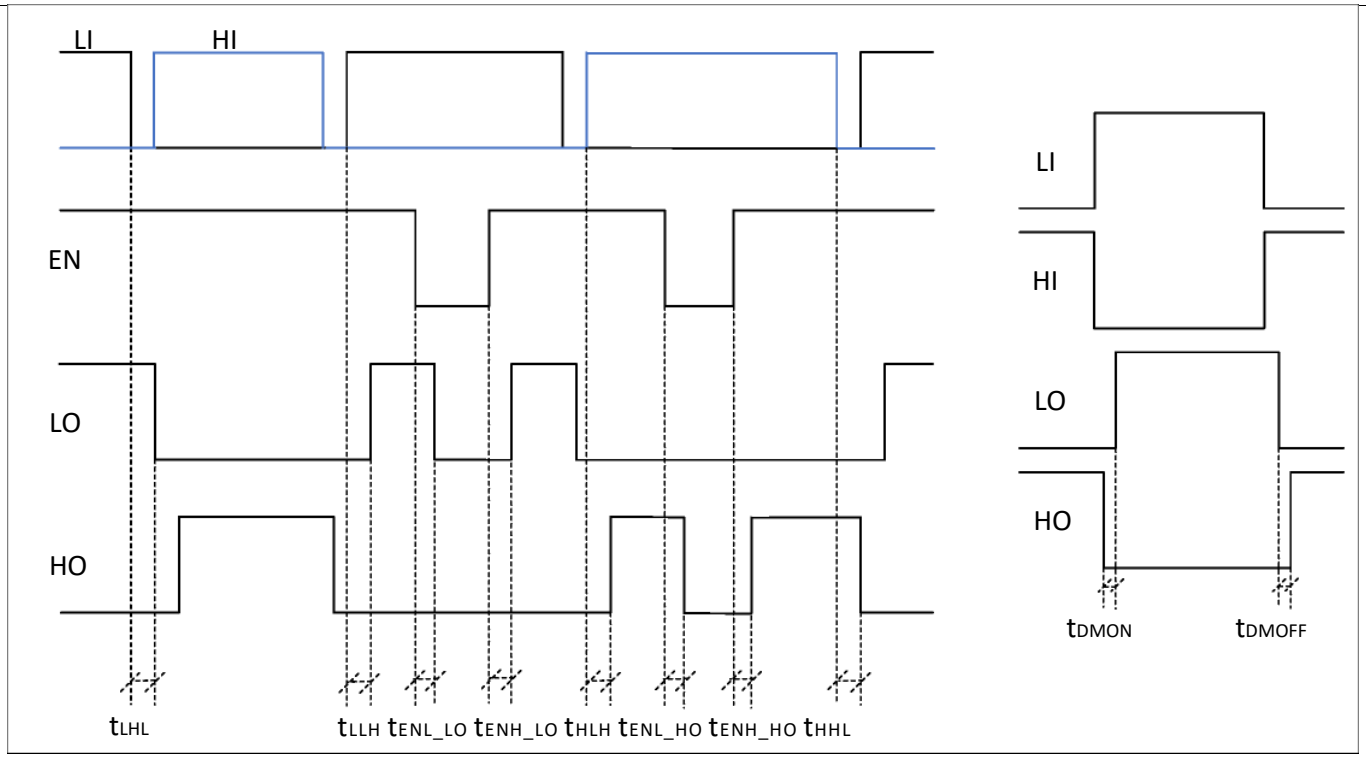


Figure 5 Propagation delay and delay matching timing diagrams

6 Typical characteristics

Unless otherwise specified: V_{DD} = V_{HB} = 5 V, V_{HS} = V_{SS} = 0 V, T_C = 25°C and no load on the outputs.

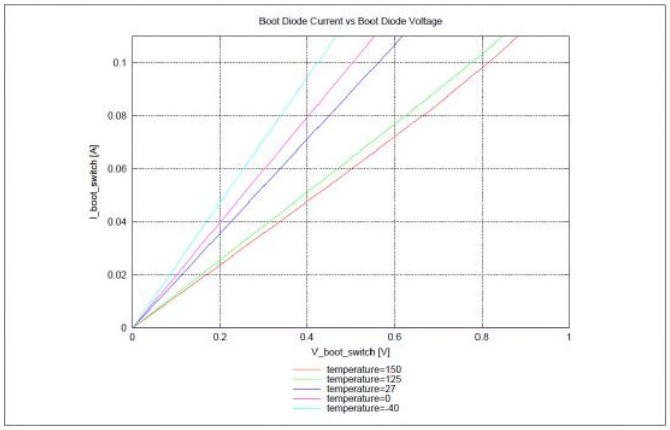


Figure 6 Bootstrap switch current vs. voltage

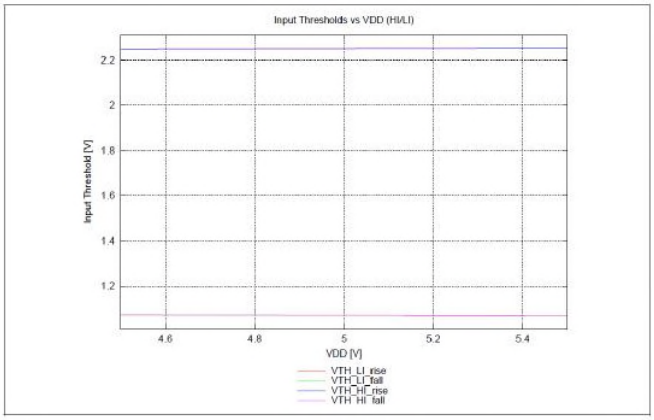


Figure 7 Input threshold vs. VDD

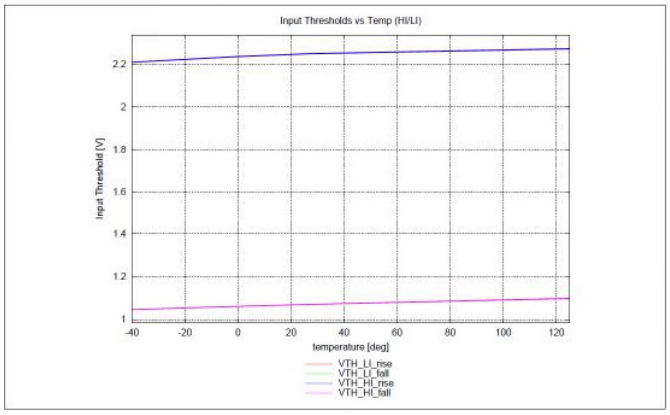


Figure 8 Input threshold vs. Temperature

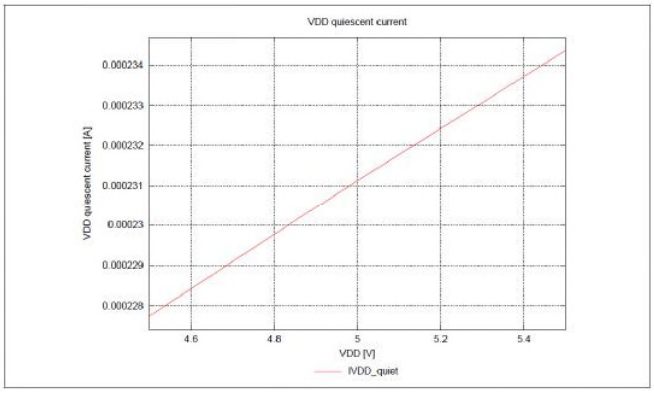


Figure 9 VDD Quiescent current vs. VDD

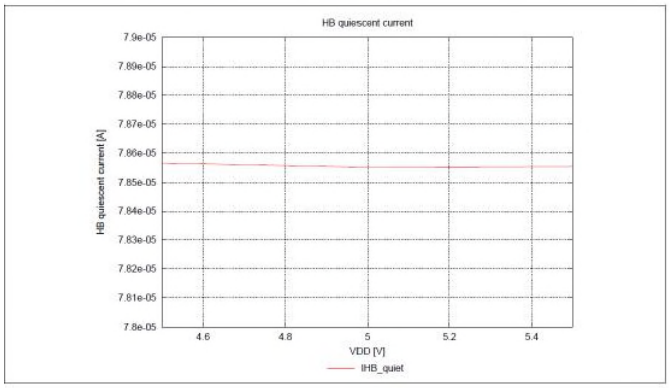


Figure 10 HB Quiescent current vs. VDD

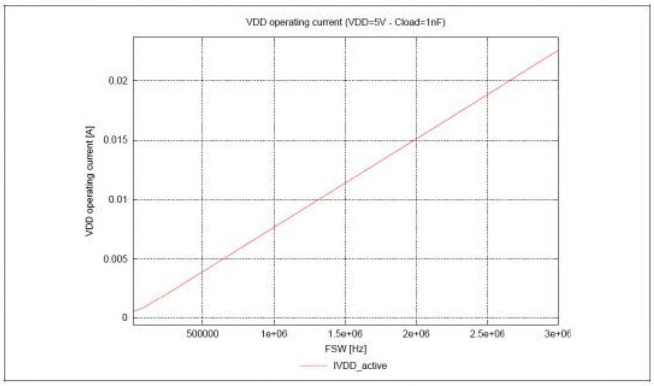


Figure 11 VDD Operating current vs. Frequency

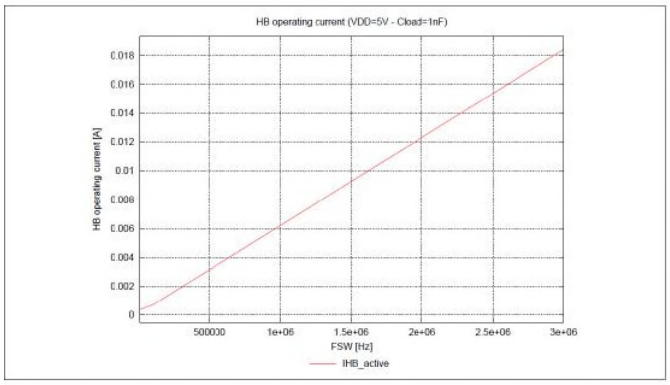


Figure 12 HB Operating current vs. Frequency

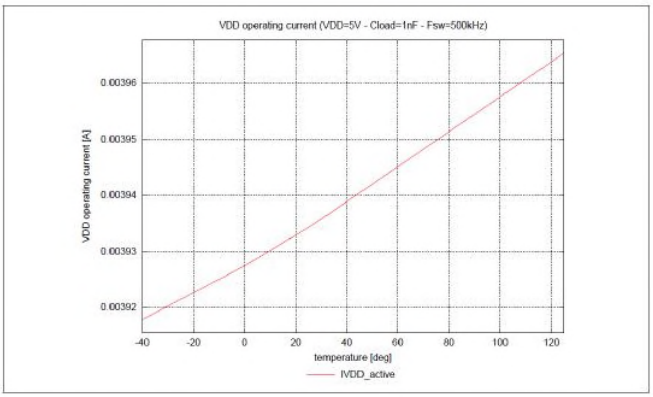


Figure 13 VDD Operating current vs. Temperature

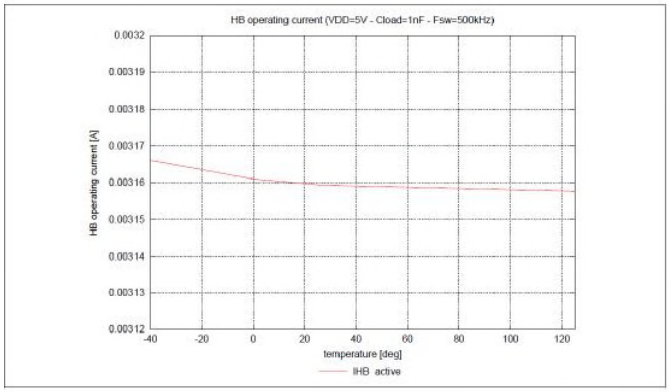


Figure 14 HB Operating current vs. Temperature

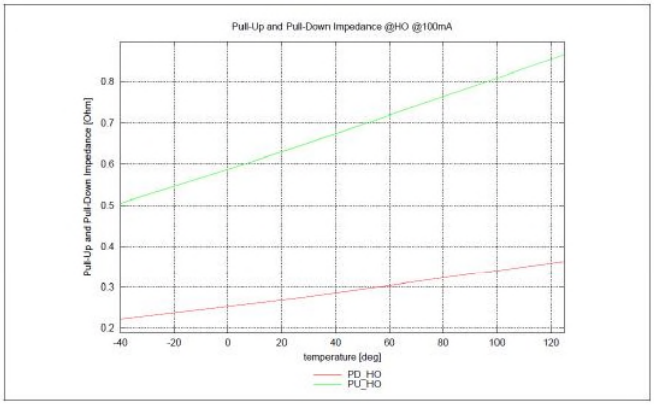


Figure 15 HO Pull-up and pull-down resistance vs. Temperature (2EDL5014AA)

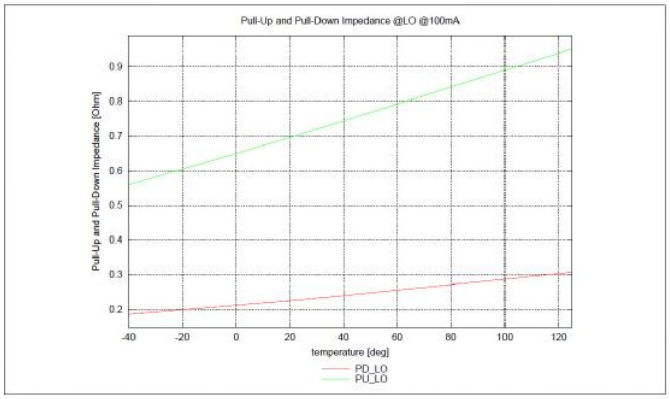


Figure 16 LO Pull-up and pull-down resistance vs. Temperature (2EDL5014AA)

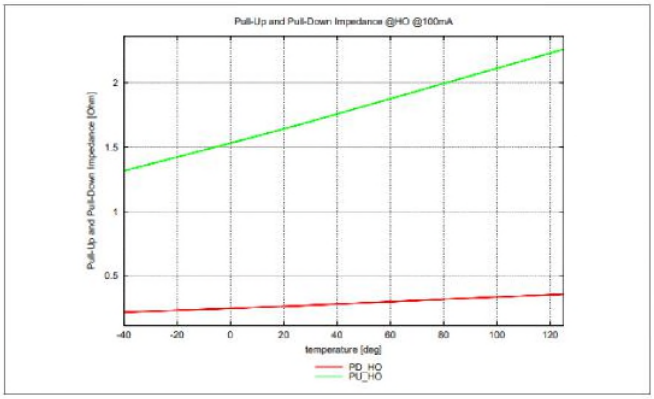


Figure 17 HO Pull-up and pull-down resistance vs. Temperature (2EDL5012AA)

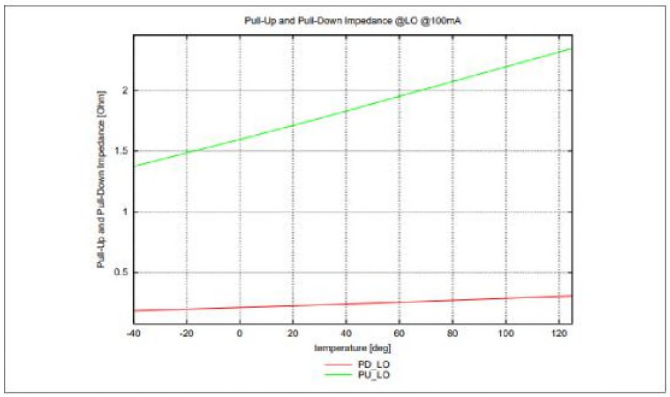


Figure 18 **LO Pull-up and pull-down resistance vs. Temperature (2EDL5012AA)**

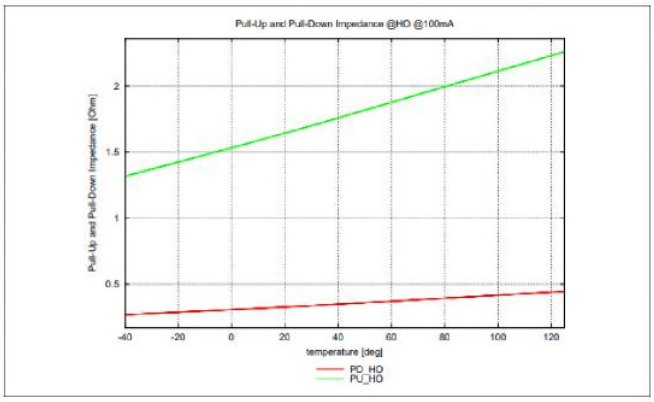


Figure 19 **HO Pull-up and pull-down resistance vs. Temperature (2EDL5011AA)**

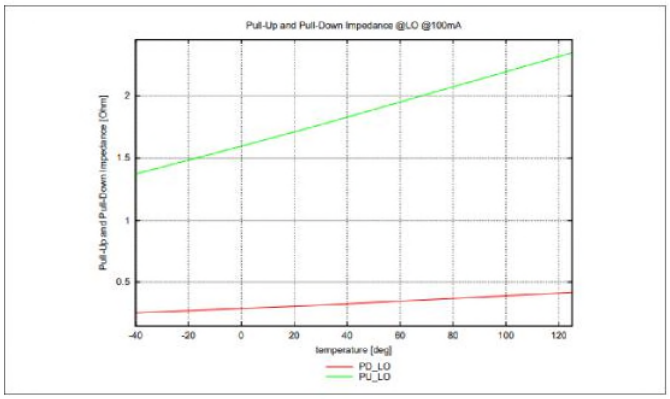


Figure 20 **LO Pull-up and pull-down resistance vs. Temperature (2EDL5011AA)**

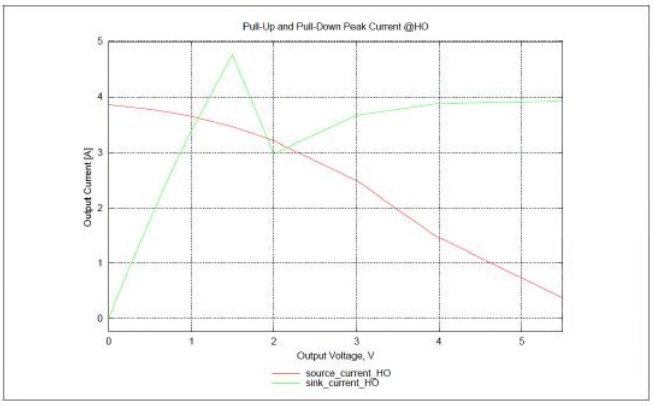


Figure 21 **HO Source and sink current vs. Output voltage (2EDL5014AA)**

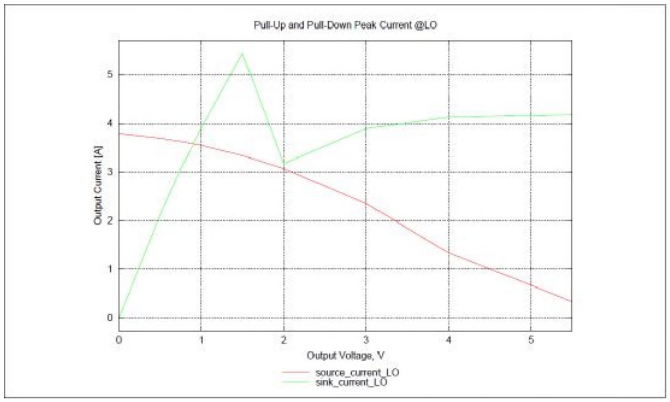


Figure 22 **LO Source and sink current vs. Output voltage (2EDL5014AA)**

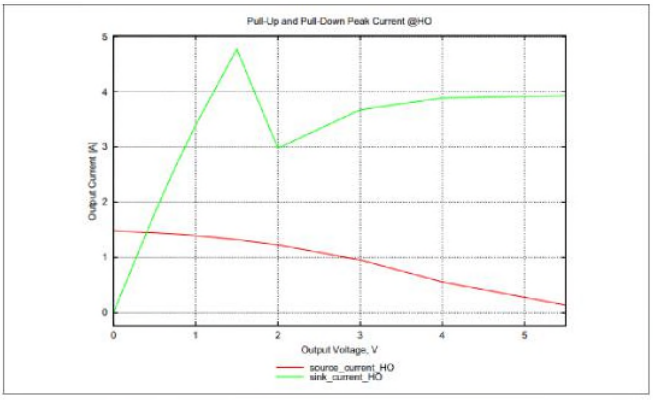


Figure 23 **HO Source and sink current vs. Output voltage (2EDL5012AA)**

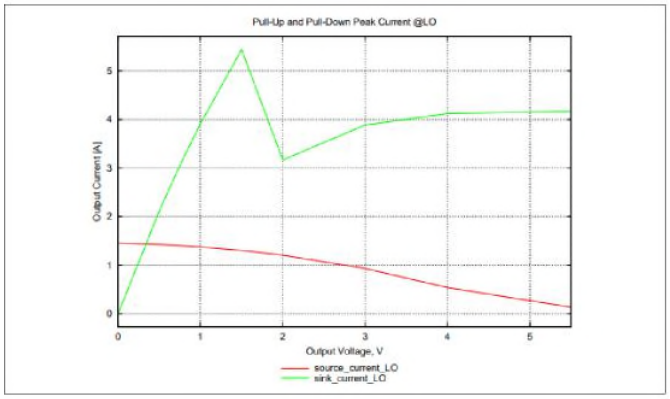


Figure 24 **LO Source and sink current vs. Output voltage (2EDL5012AA)**

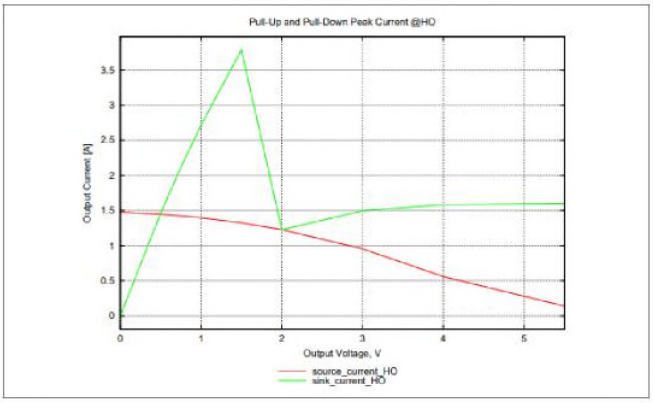


Figure 25 **HO Source and sink current vs. Output voltage (2EDL5011AA)**

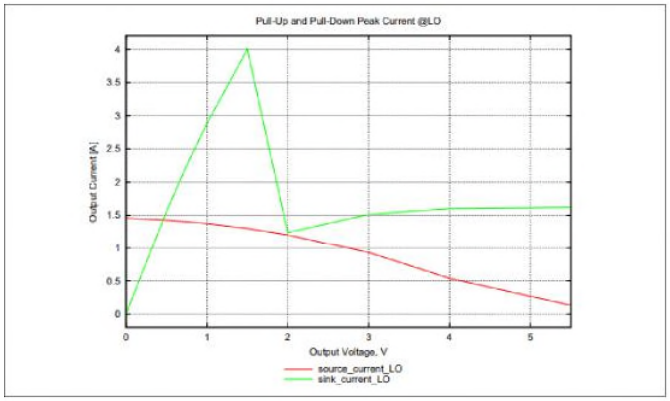


Figure 26 **LO Source and sink current vs. Output voltage (2EDL5011AA)**

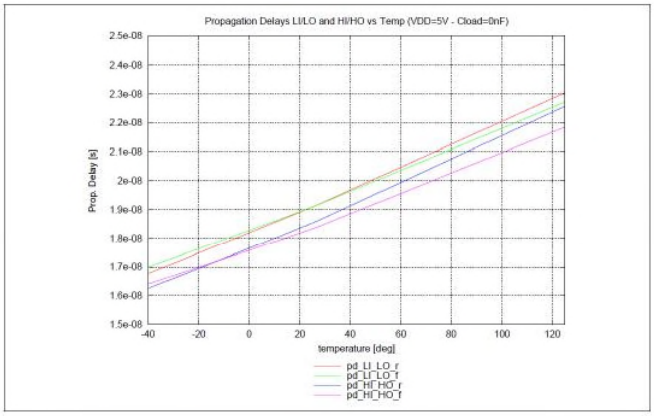


Figure 27 **Propagation delay vs. Temperature**

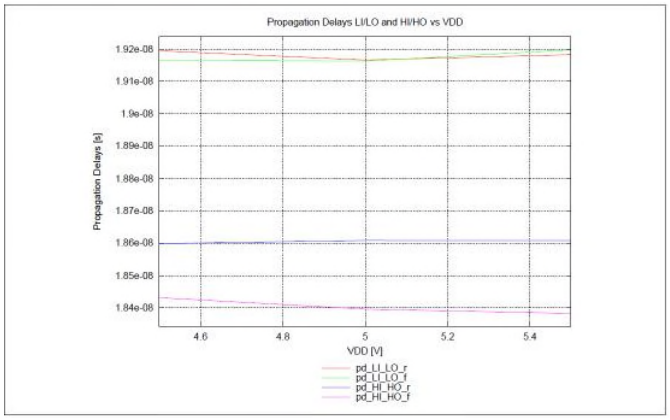


Figure 28 **Propagation delay vs. VDD**

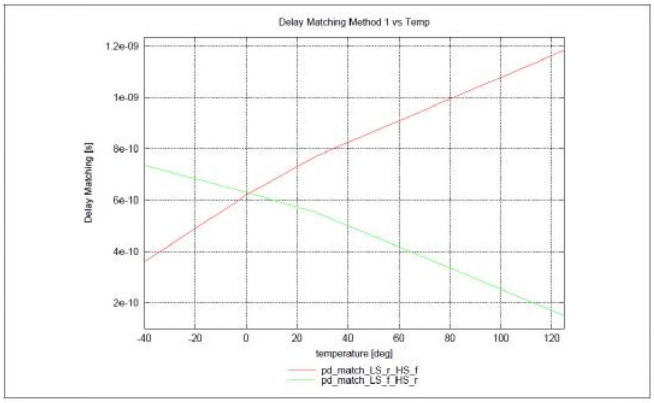


Figure 29 **Propagation delay matching vs. Temperature**

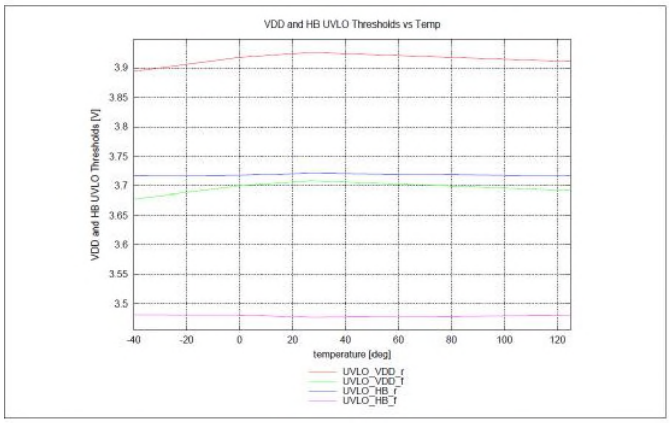


Figure 30 **UVLO Threshold vs. Temperature**

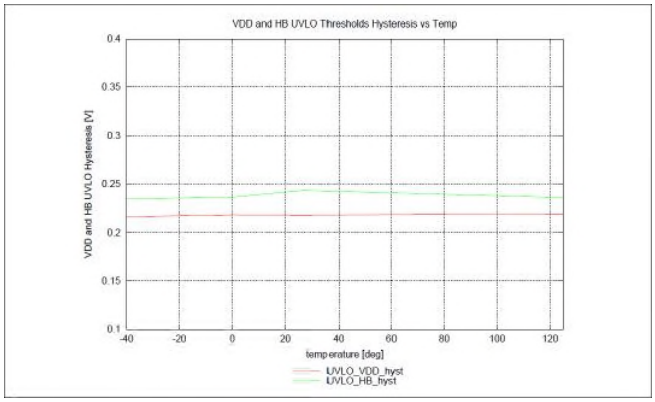


Figure 31 **UVLO Threshold hysteresis vs. Temperature**

7 Application information

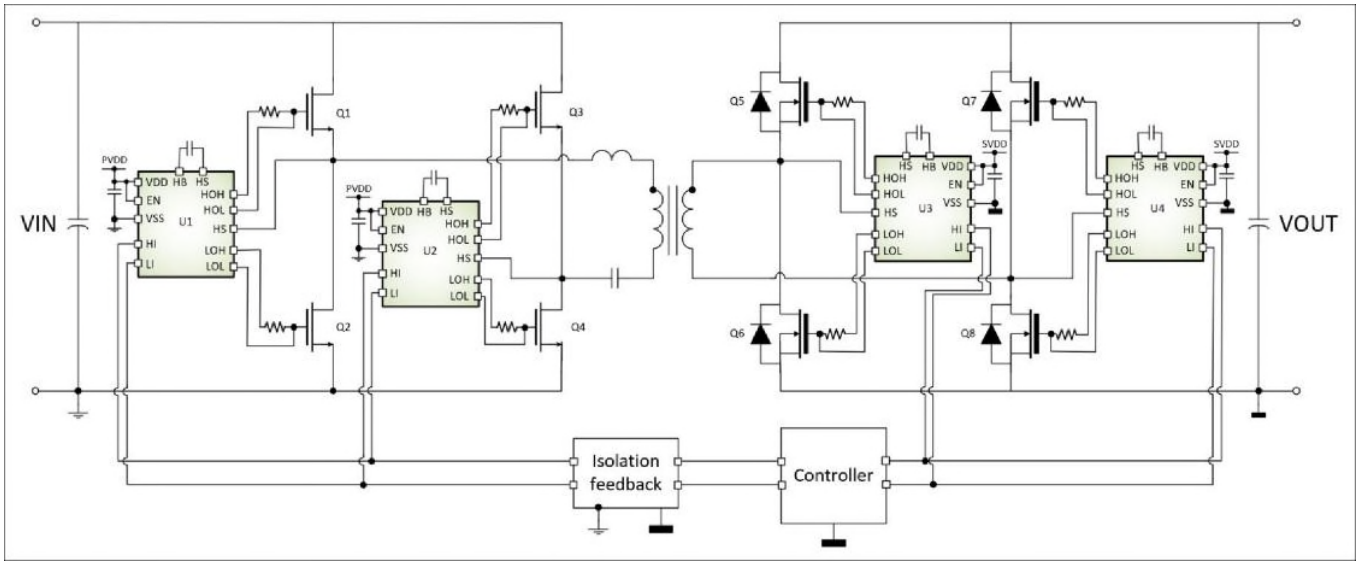


Figure 32 Typical application - full-bridge LLC

7.1 Design guidelines

In a half-bridge configurations, a high-side bias which is referenced to the switch node is needed in order to drive the gate of the high-side transistor. One of the most common solutions due to its simplicity and low cost is the usage of a bootstrap circuit consisting of a bootstrap switch (internal to the driver) and a capacitor as seen in Figure 33. However, this method imposes limitation on the power converter's duty cycle due to the requirement of recharging the bootstrap capacitor. This limitation can be mitigated through the proper selection of the bootstrap components.

The bootstrap circuit operation is defined by two main periods:

Charging period: When the low-side transistor (Q2) is ON and the high-side transistor (Q1) is OFF, the switch node/HS pin is pulled to ground creating a charging path for the bootstrap capacitor (C_{boot}) through the V_{DD} bypass capacitor (C_{VDD}) and the bootstrap switch (internal to the driver).

Discharging period: When the low-side transistor (Q2) is OFF and the high-side transistor (Q1) is ON, the switch node/HS pin is pulled to the high voltage V_{IN} and since the low-side PWM is low, the bootstrap switch will be disconnected from the VDD rail. The bootstrap capacitor (C_{boot}) discharges some of its stored charges to the gate of the high-side transistor as well as to other contributing factors such as the transistor's gate-source leakage current, floating section quiescent current, floating section leakage current and the bootstrap diode reverse bias leakage current.

Typical waveform for the voltage across C_{boot} as a function of time is shown in Figure 34 where the various contributions have been distinguished. The voltage across C_{boot} increases during the charging period and then it drops with a high negative dV/dt as it charges the gate of the high-side transistor (Q1). After which, the C_{boot} voltage continues to drop but with a much lower slope because only the high-side bias current and some leakage current is discharing the C_{boot} during this phase.

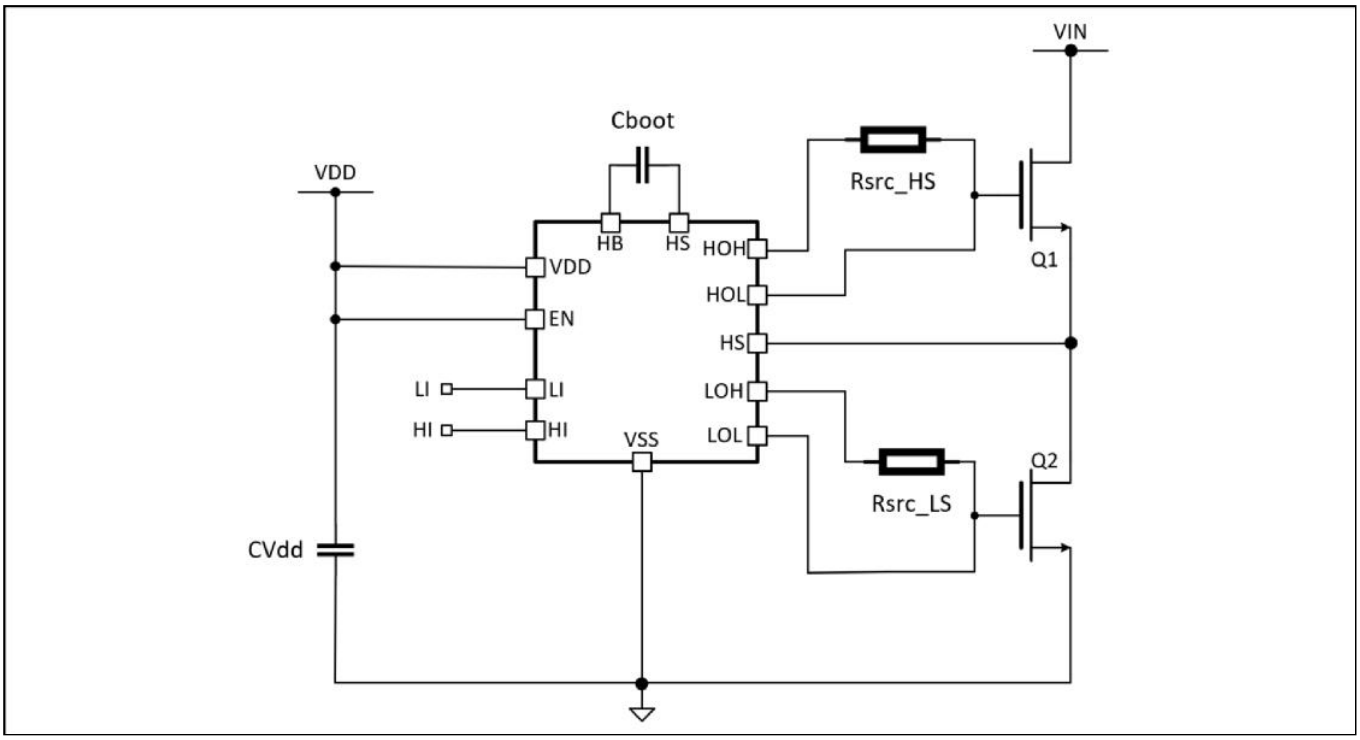


Figure 33 Gate drive circuitry to drive GaN HEMTs in a half-bridge configuration

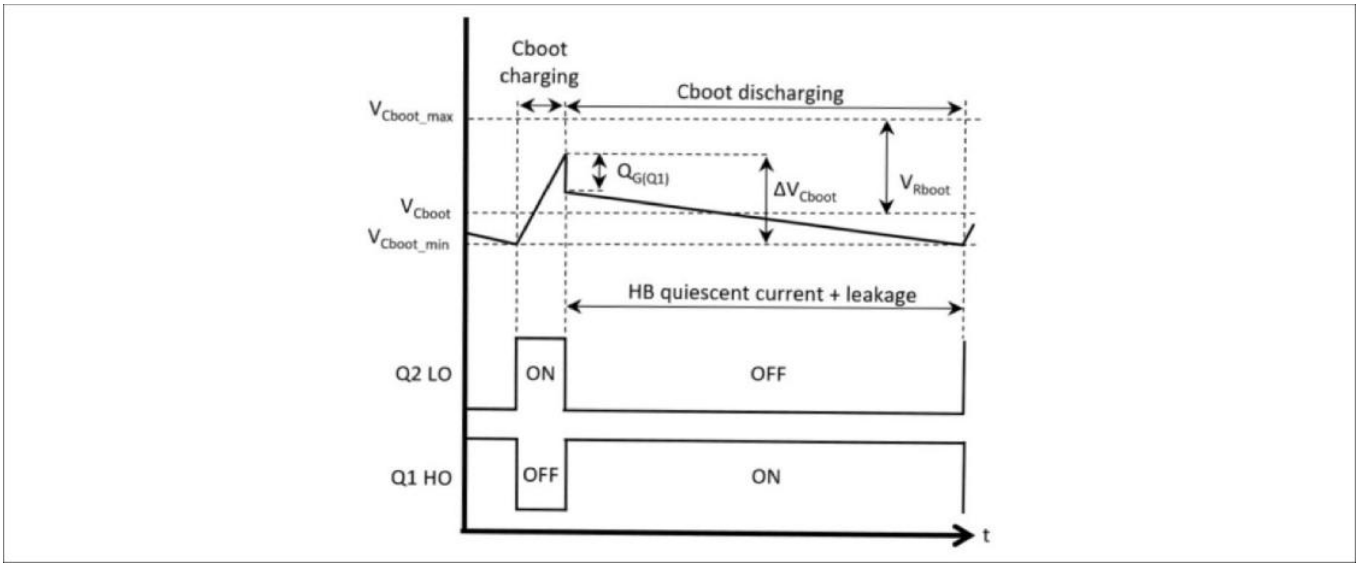


Figure 34 Typical $_{Cboot}$ waveform

7.1.1 Selection of bootstrap capacitor

The bootstrap capacitor provides the necessary charge to drive the high-side transistor and thus it needs to be sized in such a way that the maximum voltage drop across this capacitor does not fall below the high-side UVLO threshold during transient and normal operations. First, determine the maximum allowable voltage drop $_{(\Delta VCboot\_max)}$ when the high-side transistor (Q1) is on which is given by the following formula:

$$\Delta V_{Cboot\_max} = V_{DD} - V_F - V_{HBR} - V_{HBH} \quad (1)$$

Where:

V_{DD} = Gate driver supply voltage
V_F = Bootstrap switch forward voltage drop
V_{HBR} = HB UVLO rising threshold
V_{HBH} = HB UVLO threshold hysteresis

Next, determine the total charge $_{(QBOOT)}$ that must be delivered by the bootstrap capacitor at maximum duty cycle. As mentioned, there are several factors that contribute to the discharge of the bootstrap capacitor such as the Q1's total gate charge, Q1's gate-source leakage current, HB quiescent current, HB leakage current and bootstrap capacitor leakage current (if using an electrolytic capacitor). For sake of simplicity, only Q1's total gate charge and HB quiescent and leakage current are considered as the other sources of leakage are negligible in comparison.

$$Q_{BOOT} = Q_G + \frac{I_{HB}}{f_{sw}} + I_{HBS} \times \frac{D_{max}}{f_{sw}} \quad (2)$$

Where:

Q_G = high-side transistor (Q1) total gate charge
$'_{HB}$ = HB maximum quiescent current
$'_{HBS}$ = HB to VSS leakage current
D_{max} = maximum duty cycle
f_{sw} = switching frequency

The minimum bootstrap capacitor value can then be calculated using the formula:

$$C_{boot\_min} \geq \frac{Q_{BOOT}}{\Delta V_{Cboot\_max}} \quad (3)$$

7.1.2 Selection of VDD bypass capacitor

The VDD bypass capacitor provides the gate charge (Q_G) to drive the transistors, as well as additional power consumption by the driver itself. It should be placed as close as possible to the VDD and VSS pins of the gate driver. The minimum value for this bypass capacitor can be calculated based on the maximum allowable voltage ripple (ΔV_{DD_max}) in the design. This ripple should be minimized such that the lowest possible VDD is above the UVLO limit of the gate driver as well as above the safe driving voltage of the transistor. In a half-bridge configuration, the VDD bypass capacitor also provides the charge $_{(QBOOT)}$ for the bootstrap capacitor during the charging period. Therefore, sized the VDD bypass capacitor much larger than the bootstrap capacitor. The minimum value can be calculated as

$$C_{VDD} \gg \frac{Q_G + Q_{BOOT}}{\Delta V_{DD\_max}} \quad (4)$$

In practice, this capacitance value must be increased somewhat to account for dc bias effects in the capacitor and other non-idealities in the circuit.

7.1.3 Selection of bootstrap resistor

The bootstrap resistor limits the current in the bootstrap switch during start-up when the bootstrap capacitor is initially completely discharged. The peak current through this resistor is given by:

$$I_{Pk\_Rboot} = \frac{V_{DD} - V_F}{R_{boot}} \quad (5)$$

The bootstrap resistor together with the bootstrap capacitor introduces a time constant and must be sized appropriately to achieve the desired start-up time. For this calculation, it is assumed that the bootstrap capacitor is fully charged after 4 time constant. With this, R_{boot} can be calculated using the following formula:

$$R_{boot} \leq \frac{t_{mifl}}{4 \times C_{boot}} \quad (6)$$

Where:

t_{min} = minimum on time of the low-side transistor (Q2)

7.1.4 Selection of external bootstrap diode

The 2EDL501XAA-U2D has an integrated bootstrap switch with active bootstrap clamp feature to avoid overcharging the bootstrap capacitor which is useful when driving GaN HEMTs. Therefore, it is not recommended to use an external bootstrap diode if this feature is needed unless there is an external circuit that can regulate the bootstrap capacitor voltage. If an external bootstrap diode is needed in the application such as when operating at very high switching frequency or with large high-side gate charge requirement, a fast recovery or Schottky diode with low forward voltage drop is recommended to minimize the losses and leakage current. It must be chosen such that it can handle the peak transient current from Equation (5) during start-up conditions, and the blocking voltage rating must be higher than the maximum input voltage $_{(VIN)}$ with enough derating.

7.1.5 Selection of gate resistor

The turn-on and turn-off external gate resistors control the turn-on and turn-off current of the gate driver providing an external way to control the switching speed of the transistor for purposes such as voltage overshoot control, ringing reduction, EMI mitigation, spurious turn-on protection, shoot –through protection etc. The following formulas show the effect of the external gate resistor to the output current capability of the gate driver.

$$I_{HSRC} = \frac{V_{DD} - V_F}{R_{PUH} + R_{G\_HS} + R_{G\_iflt}} \quad (7)$$

$$I_{HSNK} = \frac{V_{DD} - V_F}{R_{PDH} + R_{G\_HS} + R_{G\_iflt}} \quad (8)$$

$$I_{LSRC} = \frac{V_{DD}}{R_{PUL} + R_{G\_LS} + R_{G\_iflt}} \quad (9)$$

$$I_{LSNK} = \frac{V_{DD}}{(10)\ R_{PDL} + R_{G\_LS} + R_{G\_int}}$$

Where:

I_{HSRC} = High-side peak source current
I_{HSNK} = High-side peak sink current
I_{LSRC} = Low-side peak source current
I_{LSNK} = Low-side peak sink current
R_{PUH} = High-side pull-up resistance
R_{PDH} = High-side pull-down resistance
R_{PUL} = Low-side pull-up resistance
R_{PDL} = Low-side pull-down resistance
V_{DD} = Gate driver supply voltage
V_F = Bootstrap switch forward voltage drop
R_{G_HS} = High-side external gate resistance
R_{G_LS} = Low-side external gate resistance
R_{G_int} = MOSFET internal gate resistance

It is important to consider that the peak current may not reach this level during a fast switching transition, as is typical with GaN transistors. It is also worth noting that this peak current cannot exceed the specified peak source/ sink current of the gate driver, as the pull-up and pull-down transistors within the driver saturate at that current. The use of an external gate resistor in the sink path is not recommended for most designs as it limits the effectiveness of the active Miller clamp feature.

7.1.6 Driving HI and LI with the same PWM state

The 2EDL501XAAU2D has two independent inputs but due to the way that the bootstrap switch is controlled, driving the two inputs with the same PWM state is not recommended when used in a full-bridge or similar topology with diagonal driving configuration. Consider the full-bridge circuit in Figure 35, if both HI and LI are driven low at the same time there is no charging path for the bootstrap capacitor since the bootstrap switch is disconnected from the VDD rail when LI is low. If both HI and LI are driven high at the same time, reverse current flows from HB pin to VDD pin since the bootstrap switch is turned ON when LI is high.

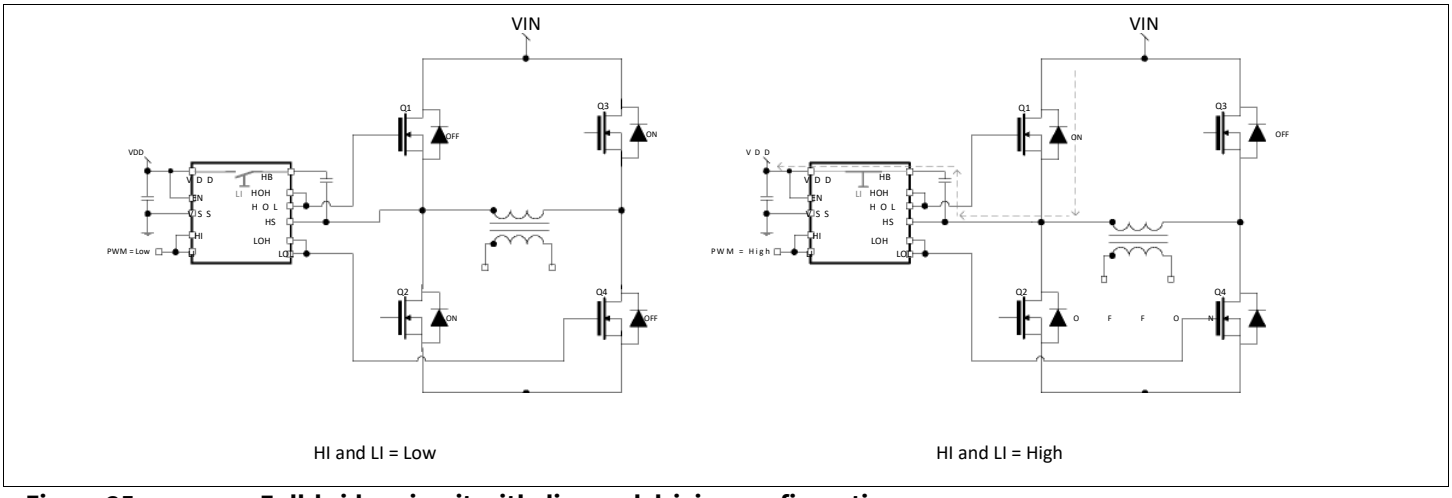


Figure 35 Full-bridge circuit with diagonal driving configuration

7.2 PCB Layout guidelines

The EiceDRIVER™ 2EDL501XAA-U2D is offered in a low inductance TSNP package which is beneficial for fast switching such as in GaN applications, as it reduces the parasitic inductance on the gate drive loop. In order to fully maximize the performance of 2EDL501XAA-U2D, below are some recommendations on how to optimize the PCB layout:

- Minimize the gate loop inductance by placing the driver as close as possible to the switching transistors
- Use a low-ESR decoupling capacitors on VDD-GND and HB-HS and placed it as close as possible to the VDD-GND and HB-HS pins of the driver. If possible, place the decoupling capacitors on the same side of the PCB as the driver
- All high current traces (LOL, LOH, HOL, HOH, VDD, HB, HS and VSS) must be as short and wide as possible and copper pours are recommended over traces when the design allows
- Connection to the HS pin of the driver from the high-side transistor source and low-side transistor drain must be as short and wide as possible to reduce the parasitic inductance which can cause excessive negative transient voltage on the driver. Also, avoid connecting the HS pin directly through the high-side transistor switching current path. Same rules apply when connecting the VSS pin of the driver to the source of the low-side transistor
- To optimize heat spreading, electrical shielding and magnetic field cancellation, a VSS-connected copper plane must be placed directly underneath the IC (PCB layer directly below the IC) as well as all components encompassed by the gate driving loop (for example, bypass capacitors, gate and source pads of the transistors)
- To avoid interference between the power loop and gate loops, separate shielding layers must be used for each loop, even if they are both connected to the same net
- It is not recommended to put an external gate resistor in the sink path (LOL and HOL) as it limits the effectiveness of the active miller clamp feature

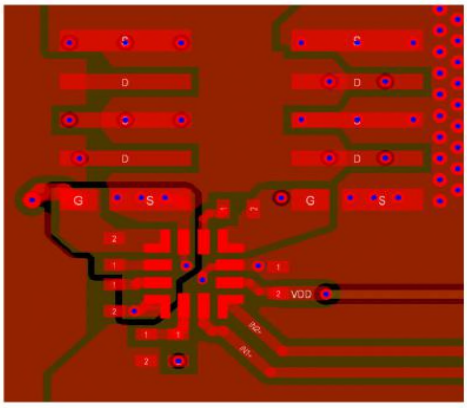


Figure 36 Layout example in a half-bridge configuration

8 Package information

8.1 Ordering information

Base part number	Package type	Standard pack		Orderable part number	Marking code
		Form	Quantity		
2EDL5011AA-U2D	PG-TSNP-12-6	Tape and reel	5000	–	–
2EDL5012AA-U2D	PG-TSNP-12-6	Tape and reel	5000	–	–
2EDL5014AA-U2D	PG-TSNP-12-6	Tape and reel	5000	–	–

8.2 Outline dimensions

For further information on package types, recommendation for board assembly, refer to:
www.infineon.com\packages

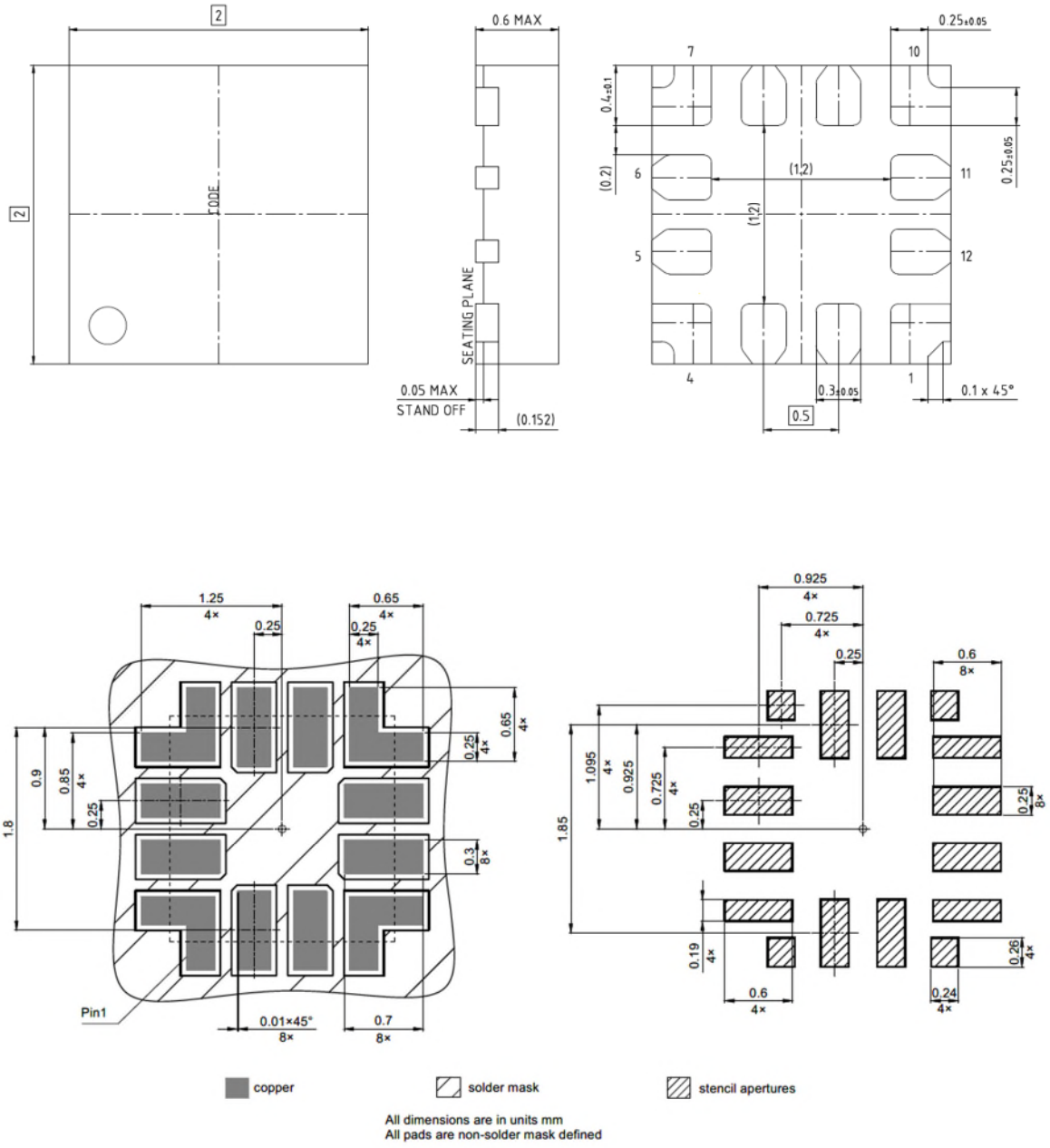


Figure 37 PG-TSNP-12-6 Outline dimensions

8.3 Tape and reel

To be updated:

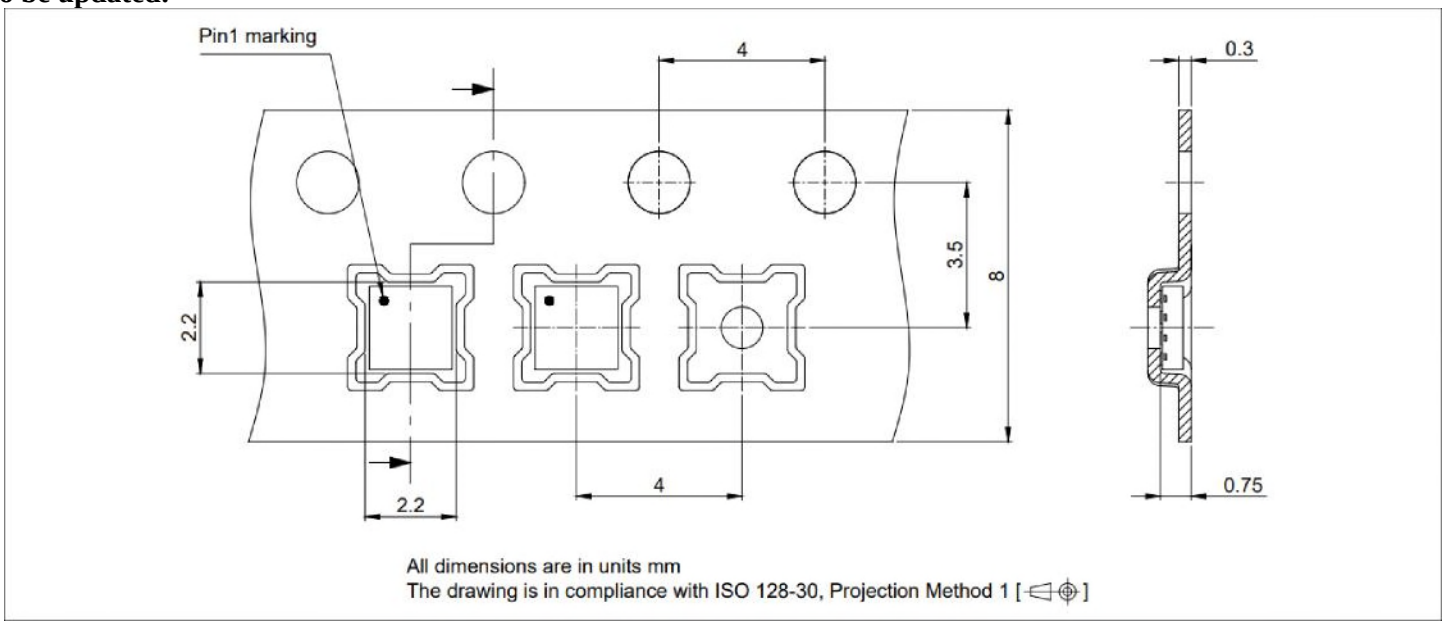


Figure 38 PG-TSNP-12-6 Tape and reel

Green Product (RoHS-compliant)

To meet the worldwide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020). Further information on packages: www.infineon.com/packages

8.4 Package drawing

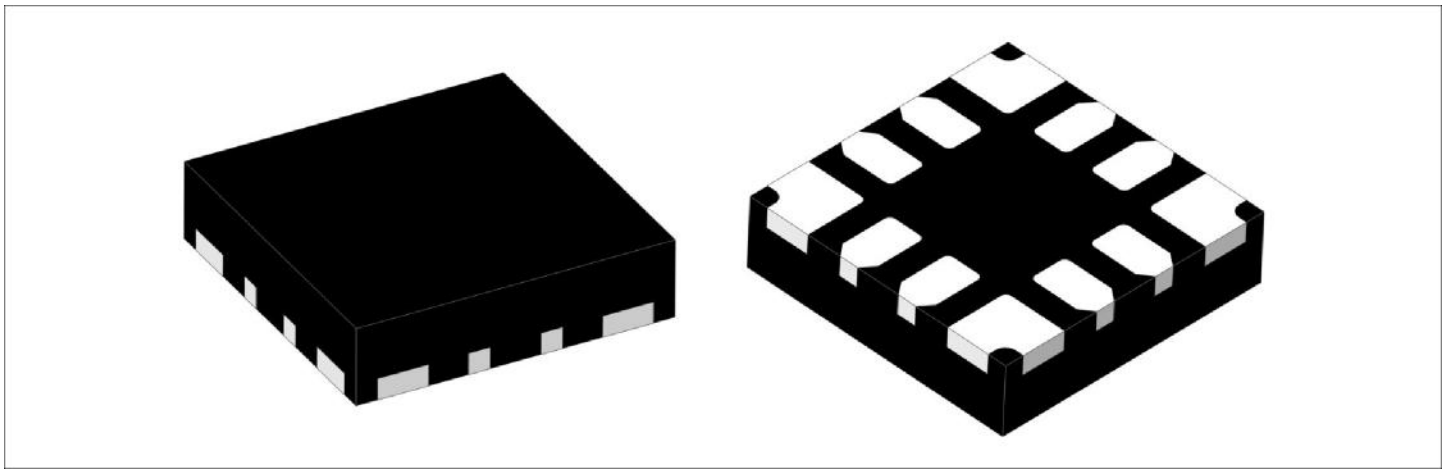


Figure 39 PG-TSNP-12-6 3D drawing

9 Revision history

Document version	Date of release	Description of changes
Rev 1.0	2025-12-09	Updated package dimensions and added PCB stencil information
Rev. 0.5	2025-06-17	**1.** Updated device information in the cover page and updated pin description and functional description **2.** Updated thermal resistance table **3.** Updated PCB layout drawing in the PCB layout guideline section. Updated active bootstrap switch description in the functional description section. Updated package name to PG-TSNP-12-6 **4.** Updated high-side output clamp capability to 100 mA and updated driver outputs functional description **5.** Updated SantaCruz block diagram to reflect the EN pull-up resistor **6.** Updated electrical characteristics table and added separate EN rising/falling threshold and hysteresis voltage for SantaCruz variants **7.** Updated block diagram (discrete) **8.** Updated Typical characteristics section **9.** Updated absolute maximum rating, recommended operating conditions, electrical and switching characteristics table **10.** Set Thermal shutdown parameters to internal **11.** Added 2EDL5011AA and 2EDL5012AA graphs in the Typical characteristics section **12.** Added $t_{POWERDOWN}$ (power down time) parameter in the switching characteristic table (for SantaCruz).
Rev. 0.4	2024-12-10	**1.** Updated cover page, package outline dimensions, package 3D drawing and pin configuration drawing
Rev. 0.3	2024-12-03	**1.** Added the 3rd discrete variant description
Rev. 0.2	2024-11-11	**1.** Modified according to the review feedback **2.** Added 3rd discrete (1.5A/1.5A) in the variants list and modified the structure
Rev. 0.1	2024-10-25	Initial version

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