2EDL2582F65

650 V Half Bridge Gate Driver with Integrated DESAT Protection

Features

- Infineon thin-film-SOI technology
- Fully operational to +650 V
- Floating channel designed for bootstrap operation
- Integrated DESAT protection
- Output source/sink current capability +2.5 A / -2.5 A
- Integrated Ultra-fast, low $R_{DS(ON)}$ Bootstrap Diode
- Tolerant to negative transient voltage up to -100 V (Pulse width is up 300 ns) given by SOI technology
- dV/dt immune ±50 V
- Maximum supply voltage of 25 V
- Undervoltage lockout for both channels
- Integrated dead-time with interlocking function
- 3.3 V and 5 V input logic compatible
- RoHS compliant

Product summary

V_{S_OFFSET}	= 650 V max.
$I_{O+/-}$ (typ.)	= +2.5 A / -2.5 A
V_{OUT}	= 12.5 V – 20 V
Delay Matching	= 10 ns max.
Deadtime (typ.)	= 75 ns
$t_{on/off}$ (typ.)	= 55 ns / 55 ns

Package

PG-DSO-8

Potential applications

- Motor drives, General purpose inverters
- Refrigeration compressors
- Half-bridge and full-bridge converters in offline AC-DC power supplies for telecom and lighting

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Ordering information

Table 1 Order information

Base part number	Package type	Standard pack		Orderable part number
		Form	Quantity	
2EDL2582F65	PG-DSO-8	Tape and Reel	2500	2EDL2582F65XUMA1

Description

The 2EDL2582F65 is a half bridge gate driver IC, designed to drive IGBT, Si and SiC MOSFET power switches. With its integrated DESAT circuit, the 2EDL2582F65 offers unique short circuit protection in a low-cost DSO-8 package, while maintaining pin-to-pin compatibility with other half bridge gate drivers. Its floating channel can be used to drive a power switch in the high-side configuration which operates up to 650 V, with output current of +2.5 A / -2.5 A and propagation delay of 55ns typical. Based on Infineon's 2nd generation SOI technology, there is excellent ruggedness and noise immunity with capability to maintain operational logic at negative transient voltages up to -100 V. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction with built in interlock lock logic to prevent shoot-through.

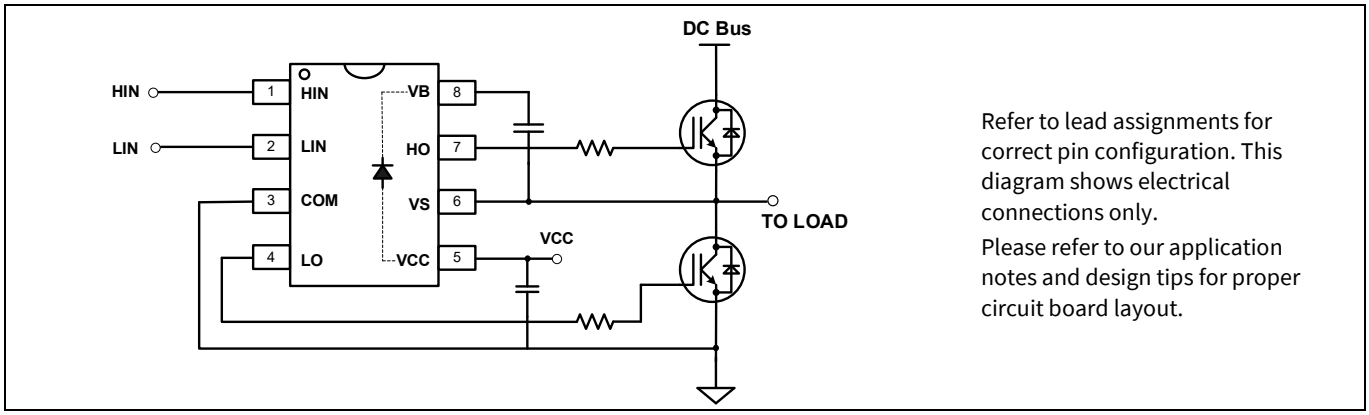

Figure 1 Typical application diagram

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1 Block diagram

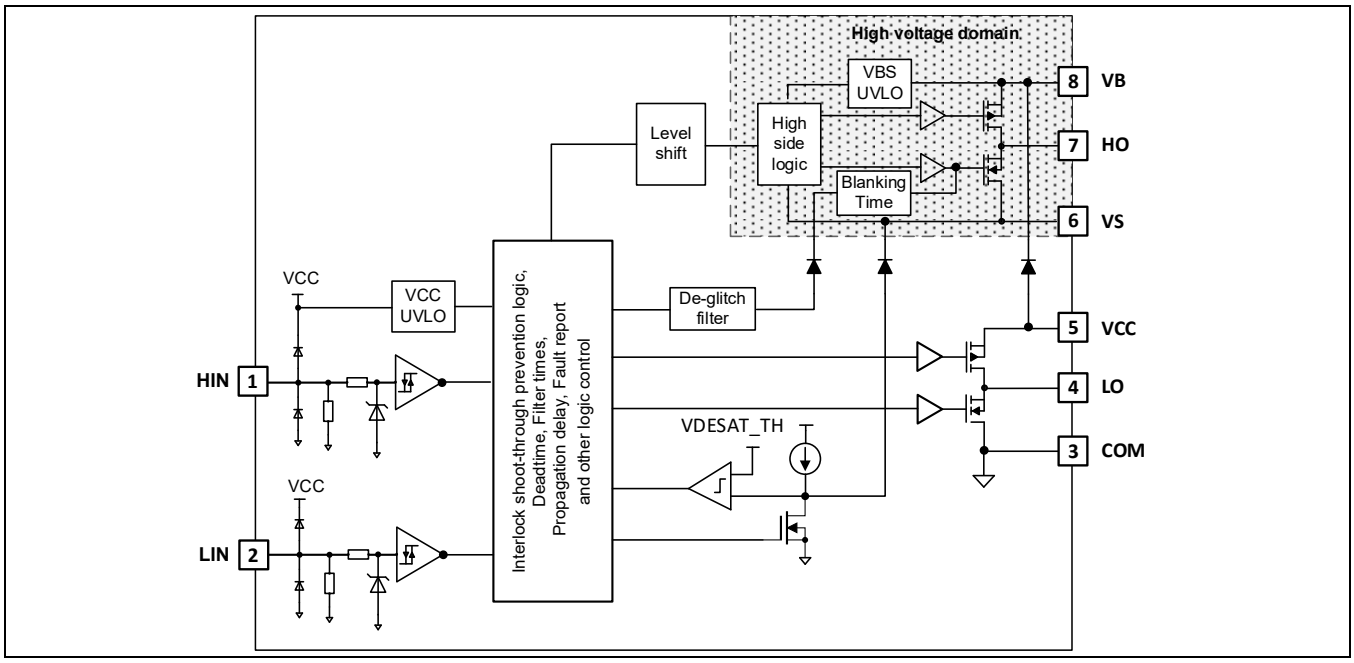


Figure 2 Functional block diagram

2 Pin configuration and functionality

2.1 Pin configuration

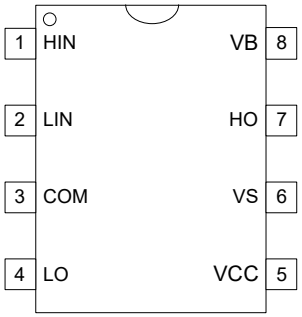


Figure 3 2EDL2582F65 lead assignments PG-DSO-8 (top view)

2.2 Pin functionality

Table 2 2EDL2582F65 lead definitions

Pin no.	Name	Function
1	HIN	Logic input for high-side gate driver output (HO), in phase. Schmitt trigger inputs with hysteresis and pull down
2	LIN	Logic input for low-side gate driver output (LO), in phase. Schmitt trigger inputs with hysteresis and pull down
3	COM	Low-side gate drive return
4	LO	Low-side driver output
5	VCC	Low-side and logic supply voltage
6	VS	High voltage floating supply return and DESAT sense
7	HO	High-side driver output
8	VB	High-side gate drive floating supply

3 Electrical parameters

3.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. All parameters are valid for T_A = 25°C unless otherwise specified.

Table 3 Absolute maximum ratings

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating well supply voltage[1]	-0.5	675	V
V_S	High-side floating well supply return voltage	-0.5	650	
V_{BS}	Floating gate drive voltage supply voltage	-1	25	
V_{HO}	Floating gate drive output voltage	V_S – 0.5	V_B + 0.5	
V_{CC}	Low side supply voltage	-0.5	25	
V_{LO}	Low-side output voltage	-0.5	V_{CC} + 0.5	
V_{IN}	Logic input voltage	-0.5	V_{CC} + 0.5	
dV_S/dt	Allowable V_S offset supply transient	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq$ +25 °C	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	—	200	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	260	

[1] In case $V_{CC} > V_B$ there is an additional power dissipation in the internal bootstrap diode between pins V_{CC} and V_B in case of activated bootstrap diode.

3.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested at (V_{CC} – COM) = (V_B – V_S) = 15 V and T_A = 25°C unless otherwise specified.

Table 4 Recommended operating conditions

Symbol	**Definition**	**Min**	**Max**	**Units**
V_B	High-side floating well supply voltage	V_S + V_{BSUV+}	V_S + 20	V
V_S	High-side floating well supply offset voltage	0	650	
V_{BS}	High-side supply voltage	V_{BSUV+}	20	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
V_{CC}	Low-side supply voltage	V_{CCUV+}	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	5.5	
T_A	Ambient temperature	-40	125	°C

3.3 Static electrical characteristics

(V_{CC} – COM) = (V_B – V_S) = 15 V, and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to COM and are applicable to the respective input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM/VS and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Table 5 Static electrical characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	10.9	11.6	12.3	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	10.0	10.7	11.4		
V_{BSUVHY}	V_{BS} supply undervoltage hysteresis	0.5	0.9	—		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	10.9	11.6	12.3		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	10.0	10.7	11.4		
V_{CCUVHY}	V_{CC} supply undervoltage hysteresis	0.5	0.9	—		
I_{LK}	High-side floating well offset supply leakage	—	1	12.5	µA	V_B = V_S = 650 V
I_{LK}	High-side floating well offset supply leakage[1]	—	10	—		T_J = 125 °C, V_S = 650 V
I_{QBS}	Quiescent V_{BS} supply current	100	180	280		
I_{QCC}	Quiescent V_{CC} supply current	300	550	800		
V_{OH}	High level output voltage drop, V_{BIAS}-V_O	—	50	130	mV	I_O = 20 mA
V_{OL}	Low level output voltage drop, V_O	—	40	100		
I_{o+}	Peak output current turn-on[1]	—	2.5	—	A	V_O = 0 V PW = 1 µs
I_{o+_mean}	Mean output current from 3 V (20%) to 6 V (40%)	1.65	2.2	—		C_L = 22 nF
I_{o-}	Peak output current turn-off[1]	—	2.5	—		V_O = 15 V PW = 1 µs
I_{o-_mean}	Mean output current from 12 V (80%) to 9 V (60%)	1.65	2.2	—		C_L = 22 nF
V_{IH}	Logic “1” input voltage	1.7	2.1	2.4	V	
V_{IL}	Logic “0” input voltage	0.7	0.9	1.1		
I_{IN+}	Input bias current (Output = High)	7.5	16.5	30	µA	V_{IN} = 3.3 V
I_{IN-}	Input bias current (Output = Low)	—	0	—		V_{IN} = 0 V
V_{FBSD}	Bootstrap diode forward voltage between Vcc and V_B	—	1	1.2	V	IF=0.3 mA
I_{FBSD}	Bootstrap diode forward current between Vcc and V_B	55	100	—	mA	V_{CC}-V_B=4 V
R_{BSD}	Bootstrap diode resistance	15	25	40	Ω	V_{F1}=4 V, V_{F2}=5 V
V_{DESAT}	VS-COM DESAT threshold	7	8	9	V	

[1] Not subjected to production test, verified by characterization.

3.4 Dynamic electrical characteristics

(V_{CC} – COM) = (V_B – V_S) = 15 V, T_A = 25°C and C_L = 1nF unless otherwise specified.

Table 6 Dynamic electrical characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	—	55	80	ns	IN 50% rise to OUT 10% rise
t_{OFF}	Turn-off propagation delay	—	55	80		IN 50% fall to OUT 90% fall
t_R	Turn-on rise time	—	15	30		OUT 10% to OUT 90%
t_F	Turn-off fall time	—	15	30		OUT 90% to OUT 10%
MT	Delay matching time (HS & LS turn-on/off)[1]	—	—	10		external dead time > 500 ns
DT	Dead time	30	75	140		$V_{LIN/HIN}$ = 0 & 3.3 V
MDT	Dead time matching time	—	—	25		external dead time 0 ns
t_{FLTR_UVBS}	VBS undervoltage glitches filter time[1]	—	1	—	us	
$t_{DESAT\_LEB\_HS}$	High side DESAT leading edge blanking time	0.65	0.92	1.35	us	
$t_{DESAT\_LEB\_LS}$	Low side DESAT leading edge blanking time	0.9	1.35	1.85		
$t_{DESAT\_FLTR\_HS}$	High side DESAT filter time	125	200	265	ns	
$t_{DESAT\_FLTR\_LS}$	Low side DESAT filter time	75	150	205		
$t_{DESAT\_OUT\_HS}$	High side DESAT to OUT LOW delay	—	—	375		V_S low to 90% HO falling
$t_{DESAT\_OUT\_LS}$	Low side DESAT to OUT LOW delay	—	—	375		V_S low to 90% LO falling
t_{FLTCLR}	Fault-clear time	—	1	—	ms	

[1] Not subjected to production test, verified by characterization.

4 Application information and additional details

4.1 Off-state diagnosis (Phase to ground short protection)

Figure 4 and Figure 5 show, at normal startup when VCC goes up, VS node will be charged up by internal bootstrap diode and CBS by VCC.

When VCC is higher than V_{CCUV+}, the gate driver goes into VS node sense mode. In this mode, while keeping HO / LO low and DESAT NMOS off, voltage of VS node is checked. If the phase (VS node) is shorted to COM (or any voltage less than V_{DESAT}), the gate drive triggers protection and goes into fault mode. Otherwise, if the VS node is not shorted to COM, then VS ≥ V_{DESAT}, the gate driver is ready for normal operation.

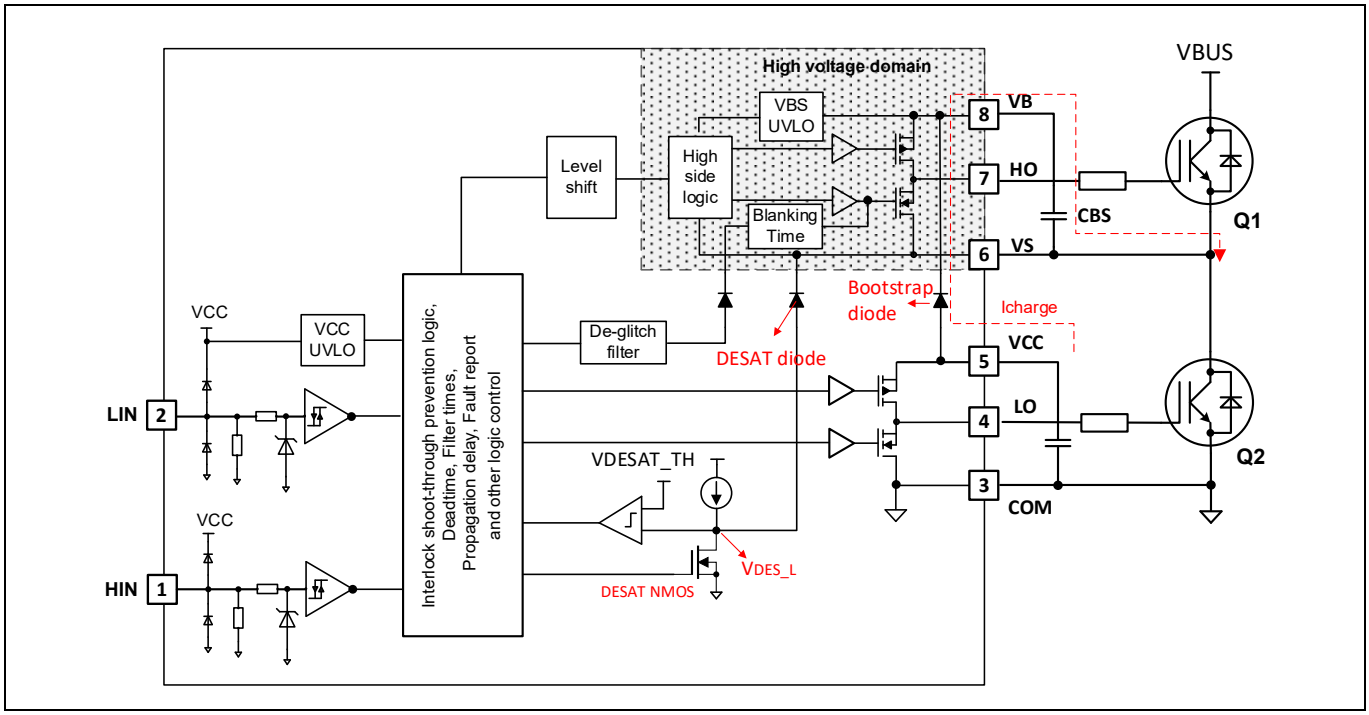


Figure 4 Off-state diagnosis block diagram

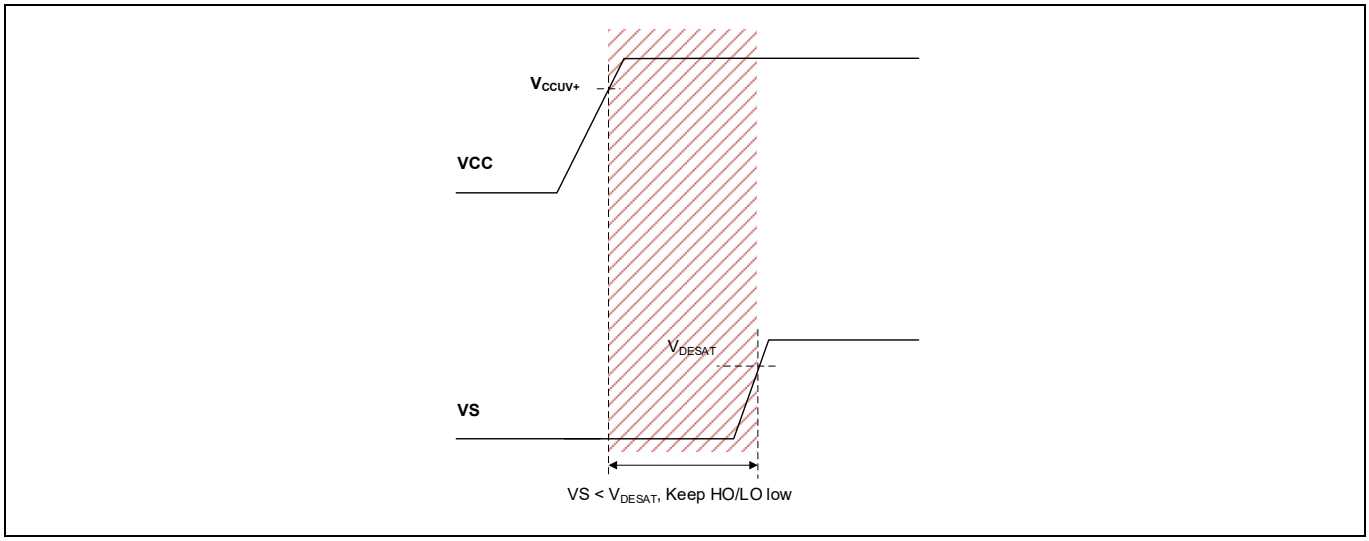


Figure 5 Off-state diagnosis timing diagram

4.2 Low side DESAT protection

The IC provides standard low side DESAT protection. In normal operation, when LIN / LO is high, low side power switch Q2 turns on, VS voltage goes to low (V_{CE_ON} of Q2), so VDES_L is clamped to VF (forward voltage of DESAT diode) and V_{CE_ON} of Q2, which is lower than V_{DESAT}, so no DESAT protection will be triggered.

But if VS voltage is higher than V_{DESAT} after internal DESAT leading edge blanking time ($t_{DESAT\_LEB\_LS}$) and filter time ($t_{DESAT\_FLTR\_LS}$), the gate driver triggers DESAT protection and goes into fault mode.

This fault condition will be automatically cleared in about 1 ms (t_{FLTCLR}).

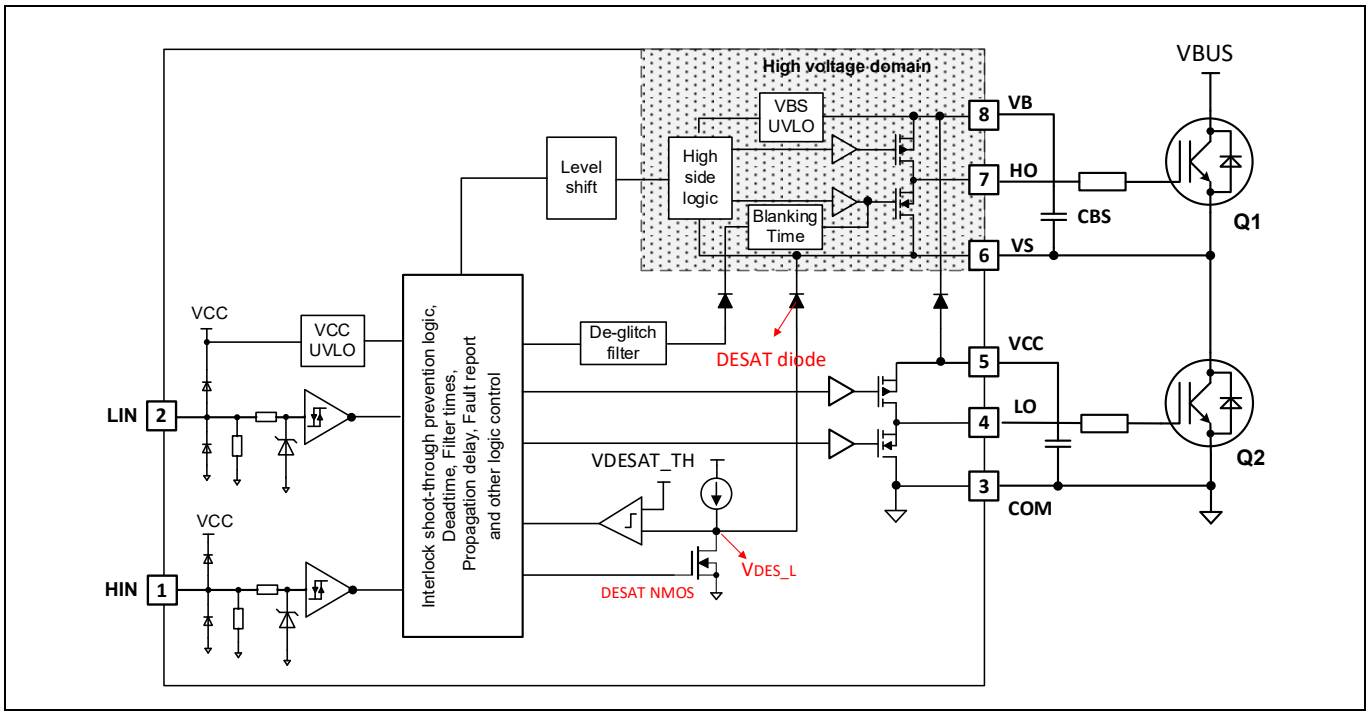


Figure 6 Low side DESAT protection block diagram

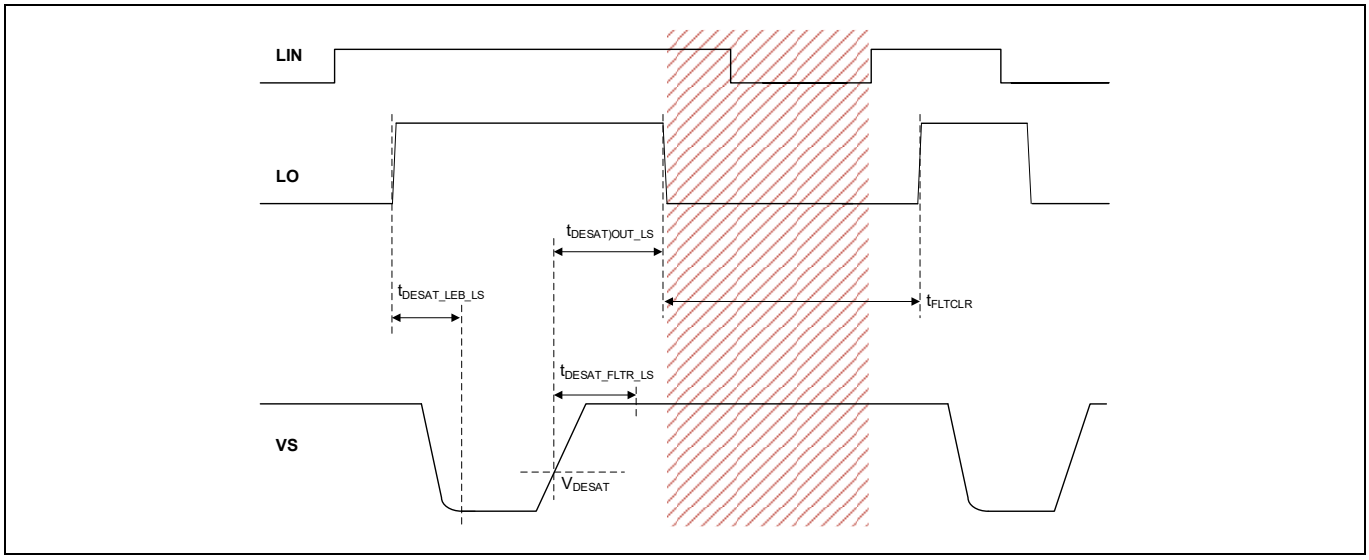


Figure 7 Low side DESAT protection timing diagram

4.3 High side DESAT protection

The IC also provides high side DESAT protection. In normal operation, when HIN / HO is high, high side power switch Q1 turns on. VS voltage goes to high (VBUS – V_{CE_ON} of Q1), therefore no fault signal is transferred to the low side. But if phase is shorted to ground (VS is shorted to COM), VS is low while HO is high, indicating a fault condition. In this case, after the internal DESAT leading edge blanking time ($t_{DESAT\_LEB\_HS}$) and filter time ($t_{DESAT\_FLTR\_HS}$), the fault signal is transferred to the low side by bit transfer diode and goes into fault mode. Both high side and low side are off.

This fault condition will be automatically cleared in about 1 ms (t_{FLTCLR}).

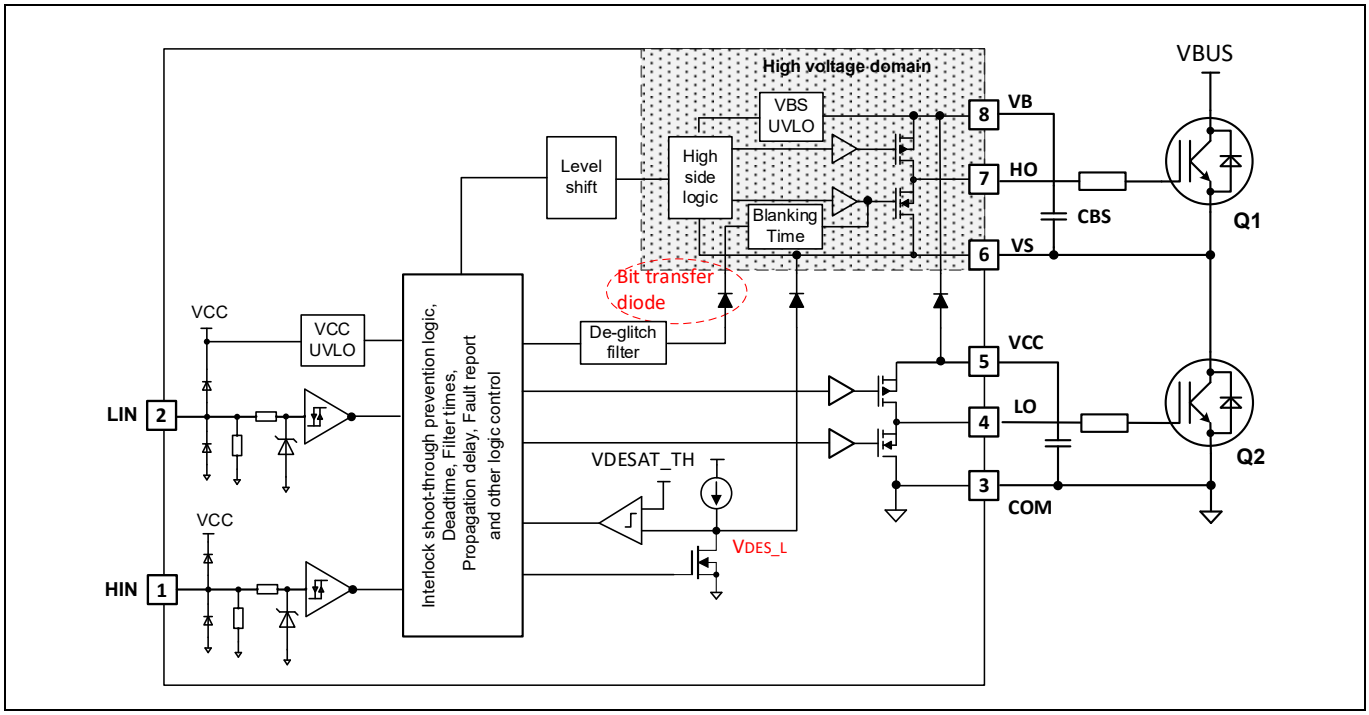


Figure 8 High side DESAT protection block diagram

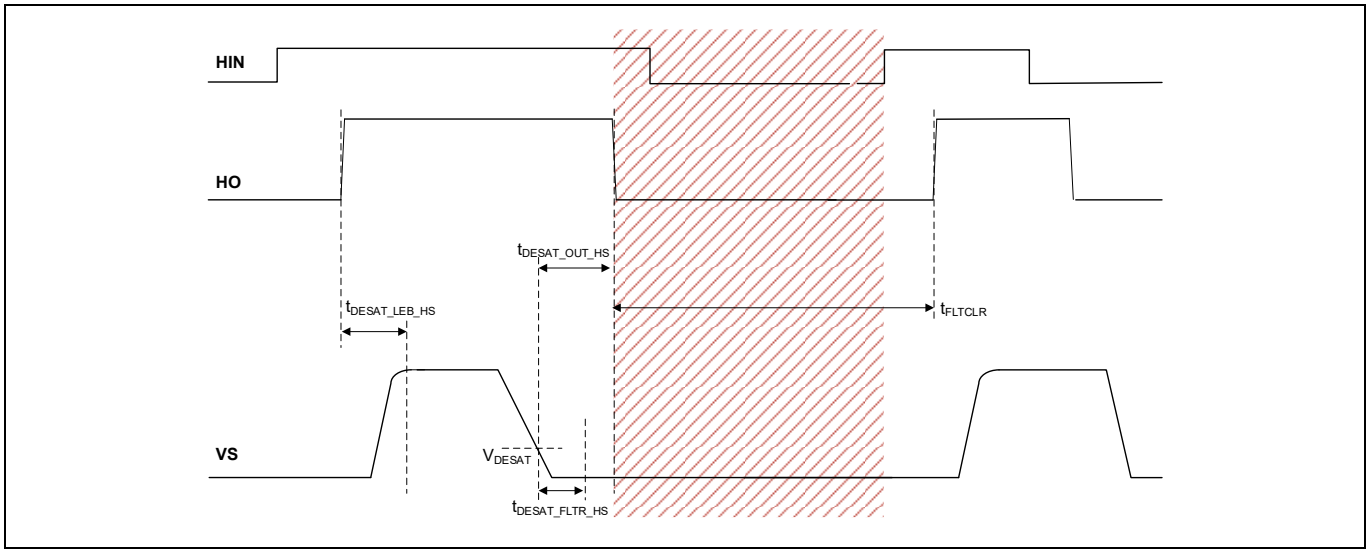


Figure 9 High side DESAT protection timing diagram

4.4 Input/output logic diagram

The relationship between the input and output signals of the 2EDL2582F65 is illustrated below in Figure 10. Note that the input stage has integrated interlock logic to prevent shoot-through operation of the outputs.

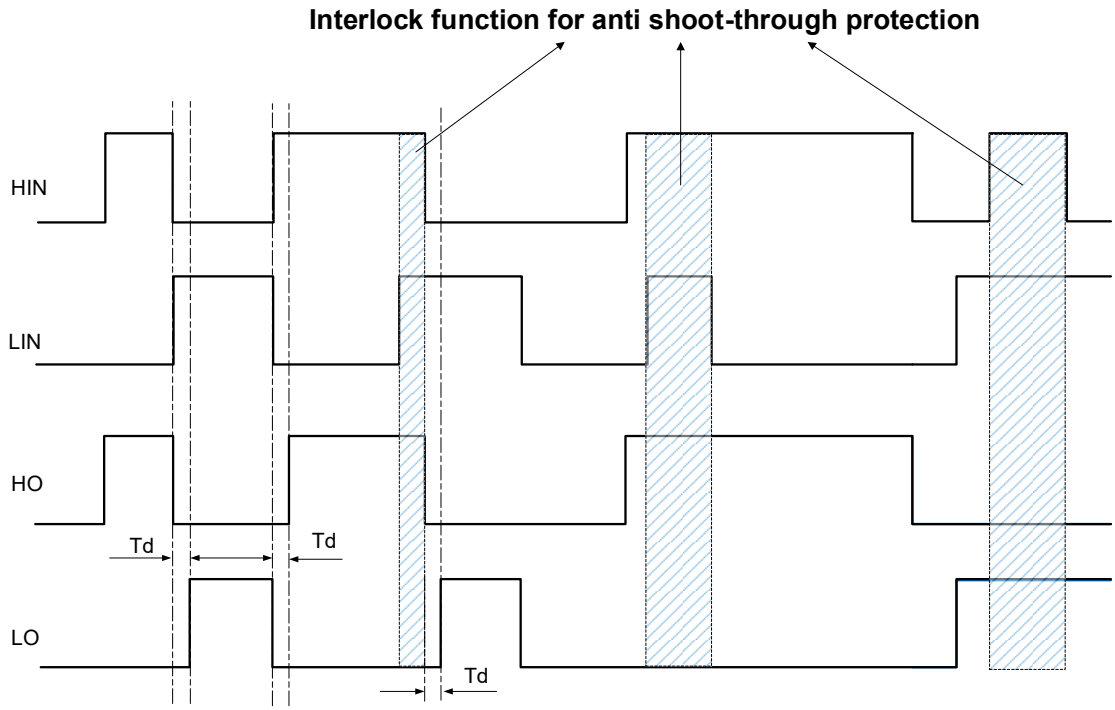


Figure 10 Input/output logic diagram

4.5 NTSOA – Negative Transient Safe Operating Area

In a typical motor drive system, dV/dt is typically designed to be in the range of 3-5 V/ns. The negative VS transient voltage can exceed this range during some events such as short circuit and over-current shutdown, when di/dt is greater than in normal operation.

Infineon's HVICs have been designed for the robustness required in many of today's demanding applications. An indication of the 2EDL2582F65's robustness can be seen in Figure 11, where the 2EDL2582F65 Safe Operating Area is shown at V_{BS}=15 V based on repetitive negative transient voltage spikes. A negative transient voltage falling in the grey area (outside SOA) may lead to IC permanent damage; vice versa unwanted functional anomalies or permanent damage to the IC do not appear if negative VS transients fall inside the SOA.

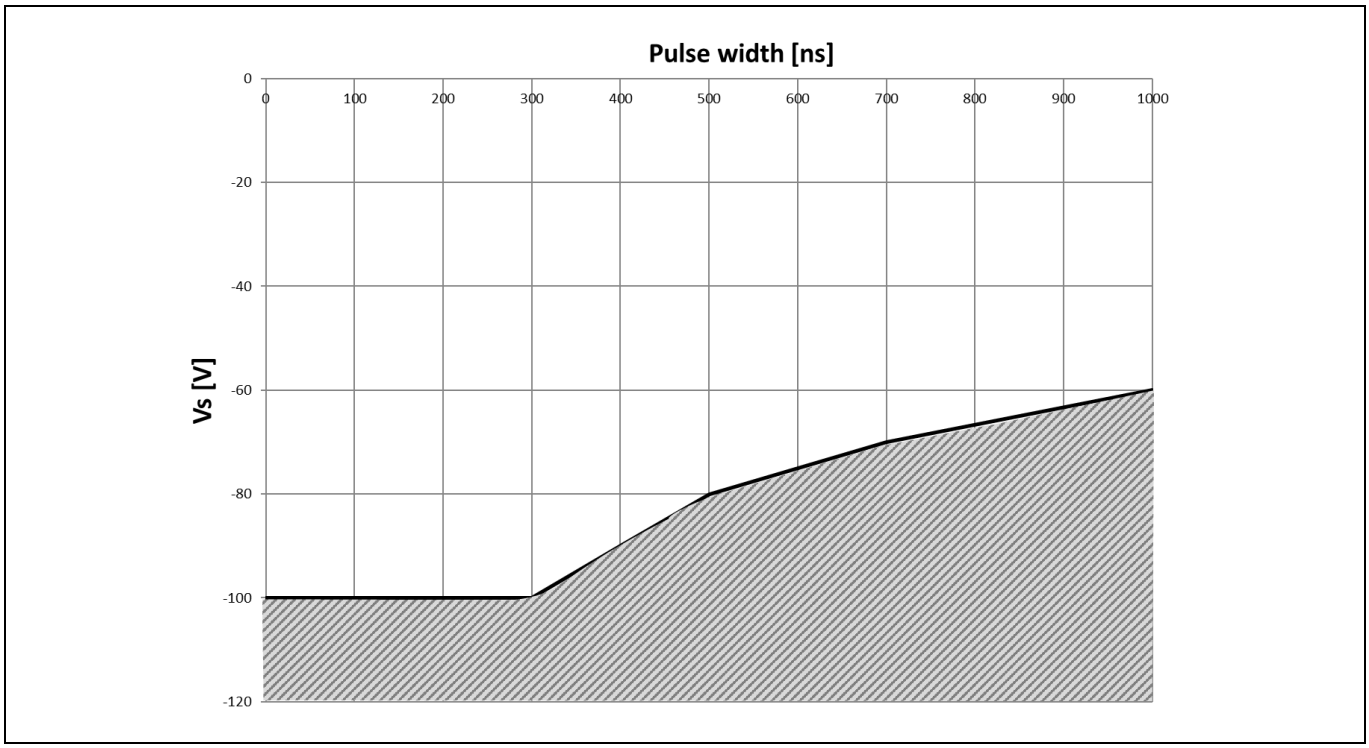


Figure 11 Negative transient voltage SOA on VS pin for 2EDL2582F65 @ VBS = 15 V

Even though the 2EDL2582F65 has been shown to be able to handle these large negative transient voltage conditions, it is highly recommended that the circuit designer always limit the negative transient voltage on VS pin as much as possible by careful PCB layout and component use.

5 Qualification information[1]

Table 7 Qualification information

Qualification level		Industrial[2] Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.
Moisture sensitivity level		MSL3, 260°C (per IPC/JEDEC J-STD-020E)
ESD	**Charged device model**	Class C3 (1.0 kV) (per ANSI/ESDA/JEDEC JS-002-2018)
	Human body model	Class 2 (2.0 kV) (per ANSI/ESDA/JEDEC JS-001-2017)
RoHS compliant		Yes

[1] Qualification standards can be found at Infineon's web site www.infineon.com
[2] Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

6 Related products

Table 8 Related products

Product	Description
Gate Driver Ics	
1ED2127S65F	EiceDRIVER™ 650 V high-side gate driver IC with over current protection (OCP), multi-function RCIN/Fault/Enable (RFE) and integrated bootstrap diode (BSD).
2ED2101(3/4)S06F	EiceDRIVER™ 650 V high speed, high-side and low-side gate driver with typical 0.29 A source and 0.7 A sink currents in DSO-8 package for driving power MOSFETs and IGBTs.
6EDL04x065xR	EiceDRIVER™ 650 V 2nd generation 3 phase gate driver with a typical 0.165 A source and 0.375 A sink current in DSO-28 and TSSOP-25 package for IGBTs and MOSFETs.
Power Switches	
IKW20N65ET7	650 V, 20 A IGBT with anti-parallel diode in TO-247 package.
IPAN60R210PFD7S	600V CoolMOS™ PFD7 superjunction MOSFET in TO-220 FullPAK narrow-lead package.
IMW65R050M2H	CoolSiC™ MOSFET 650 V G2 in TO-247-4 package, 50 mΩ.
iMOTION™ Controllers	
IMC101T	High performance Motor Control IC for variable speed drives based on field oriented control (FOC) of permanent magnet synchronous motors (PMSM).

7 Package information DSO-8

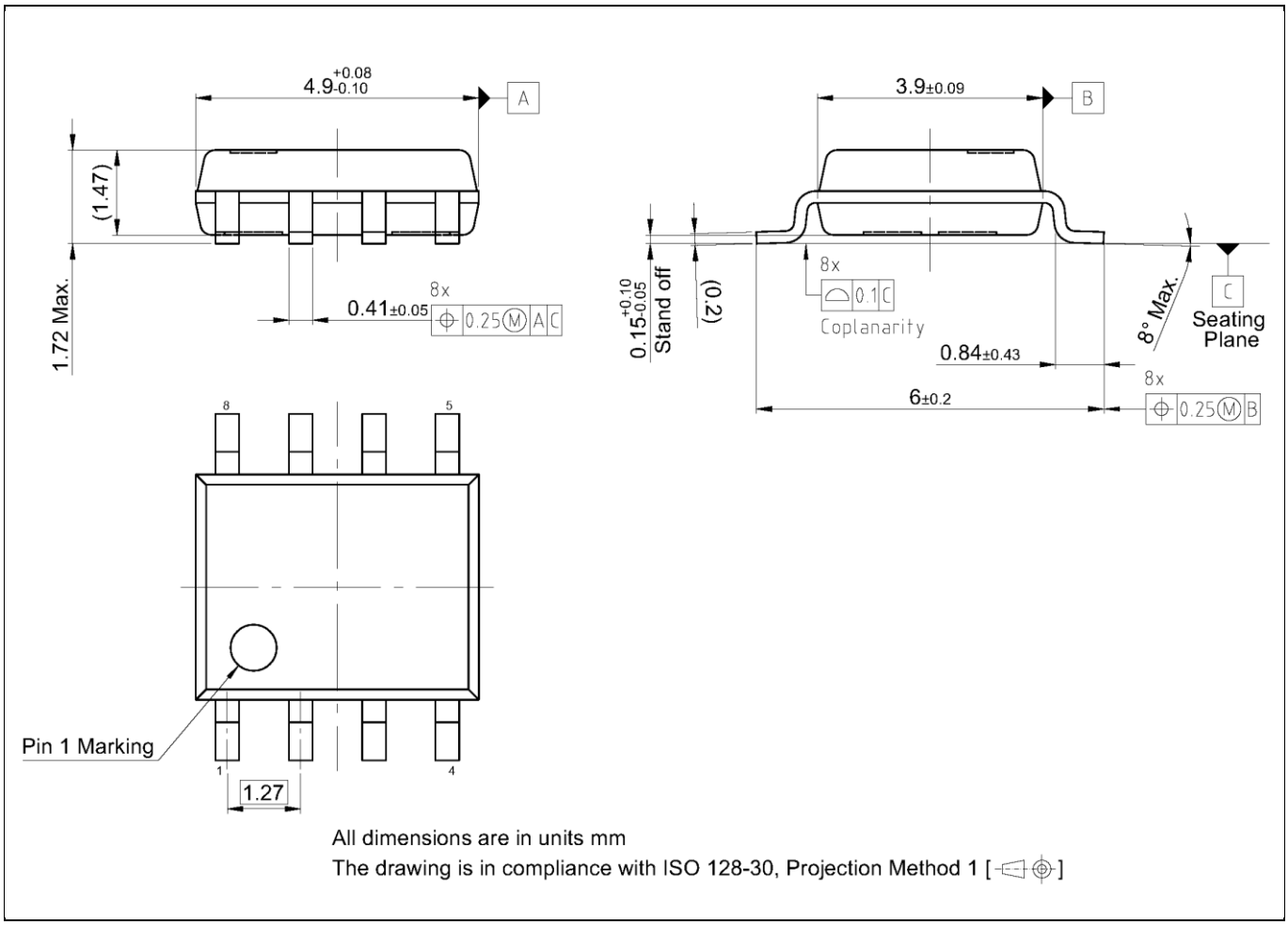
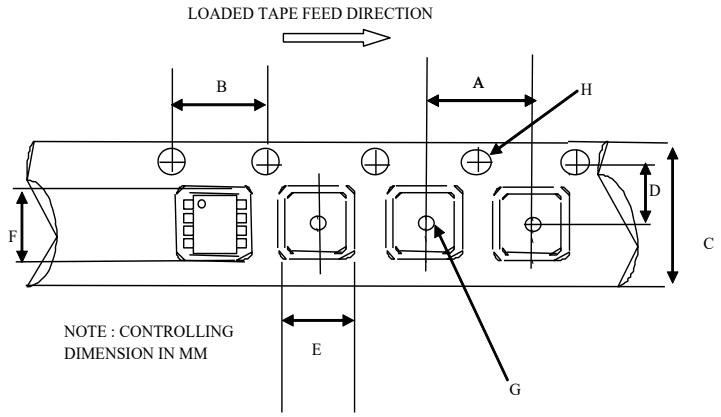
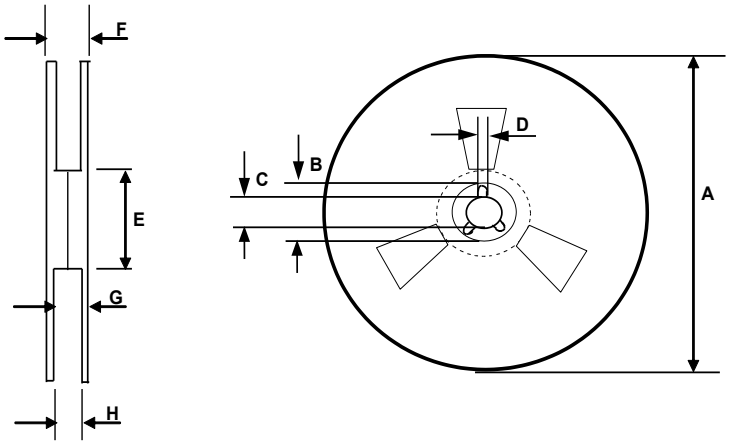


Figure 12 PG-DSO-8 Package drawing



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Figure 13 PG-DSO-8 Tape and reel details

8 Part marking information

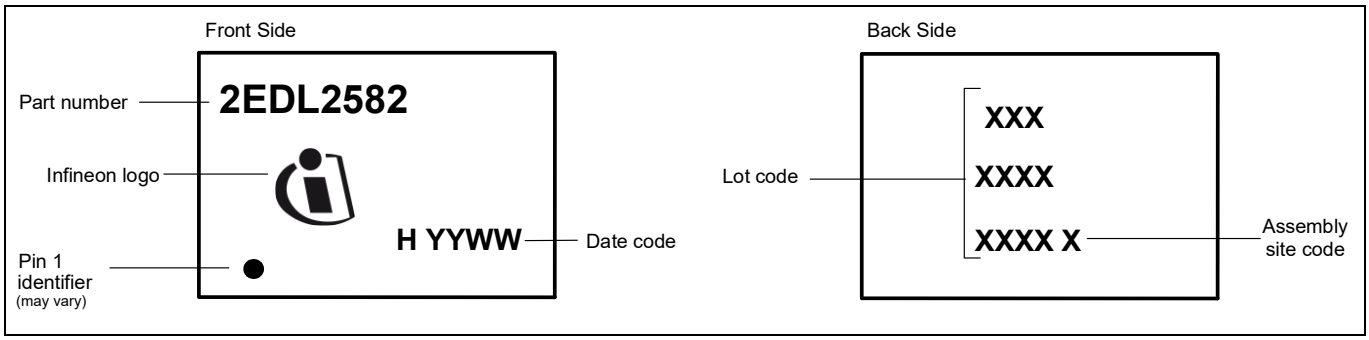


Figure 14 PG-DSO-8 marking information

9 Additional documentation and resources

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them. Below is a short list of some of these documents.

Application Notes:

- Understanding HVIC Datasheet Specifications
- HV Floating MOS-Gate Driver ICs
- Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs
- Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

Design Tips:

- Using Monolithic High Voltage Gate Drivers
- Alleviating High Side Latch on Problem at Power Up
- Keeping the Bootstrap Capacitor Charged in Buck Converters
- Managing Transients in Control IC Driven Power Stages
- Simple High Side Drive Provides Fast Switching and Continuous On-Time

9.1 Infineon online forum resources

The Gate Driver Forum is live at Infineon Forums (www.infineonforums.com). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver Forum also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the Gate Driver Forum and learn the nuances of efficiently driving a power switch in any given power electronic application.

10 Revision history

Document version	Date of release	Description of changes
1.5	2026-04-30	Initial public release at infineon.com

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