EiceDRIVER™ 1ED3330MC12M Enhanced (1ED-F4)

Datasheet

1ED3330MC12M

Technical documents | Kits and boards | Support

Single-channel isolated gate driver IC with DESAT, Soft-off, and CLAMP driver

Features

RoHS

Green

- Integrated protection features, such as short-circuit protection (DESAT), soft-off, active Miller clamp driver, and active shutdown
- For use with 600 V/650 V/1200 V/1700 V/2300 V IGBTs, Si and SiC MOSFETs
- Full-sized PMOS for high performance driving at Miller plateau
- Separate source and sink outputs with 12 A typical peak output current
- 35 V absolute maximum output supply voltage VCC2
- Undervoltage lockout for SiC MOSFETs
- 75 ns short propagation delay (typ.) and tight IC-to-IC propagation delay matching
- Very fast DESAT detection and notification
- 3.3 V and 5 V input supply voltage VCC1
- Suitable for operation at high ambient temperature and in fast switching applications
- High common-mode transient immunity CMTI > 200 kV/µs
- DSO-16 wide body package with 8 mm creepage
- Safety certification:
  - UL 1577 (planned) with $V_{ISO,test}$ = 6840 V (rms) for 1 s, V_{ISO} = 5700 V (rms) for 60 s
  - Reinforced insulation according to IEC 60747-17 (planned) with V_{IORM} = 1767 V (peak, reinforced)

Potential applications

- EV charging stations
- Industrial motor drives - compact, standard, premium, servo drives
- Solar inverters, e.g. for 1500 V (DC) systems
- UPS systems
- High voltage DC-DC converter and DC-AC inverter
- Welding
- Commercial and agricultural vehicles (CAV)
- Commercial air-conditioning (CAC)
- High-voltage isolated DC-DC converters
- Isolated switch mode power supplies (SMPS)

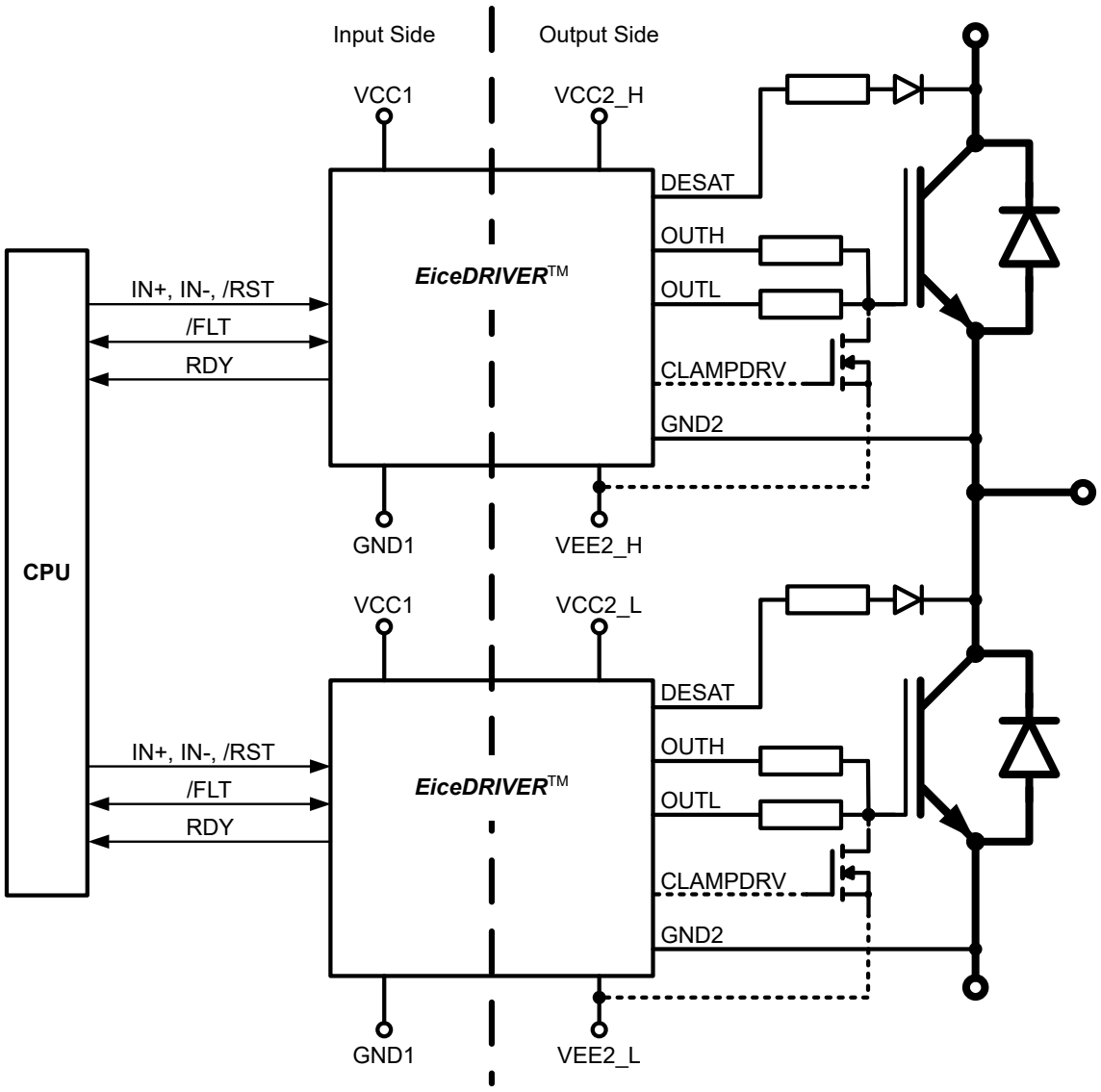
Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The 1ED3330 (1ED-F4) is a EiceDRIVER™ Enhanced single channel galvanically isolated gate driver IC with integrated protection features such as short circuit protection, active Miller clamp driver, and active shutdown for IGBT, MOSFET and SiC MOSFET in a DSO-16 wide body package. The product provides a typical output current up to 12 A.

All logic pins are 3.3 V and 5 V CMOS-compatible and can be directly connected to a microcontroller. Data transfer across the galvanic isolation is realized by the integrated Coreless Transformer (CT) technology.



Type	Package	Marking
1ED3330MC12M	PG-DSO-16	3330MC12

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1 Block diagram reference

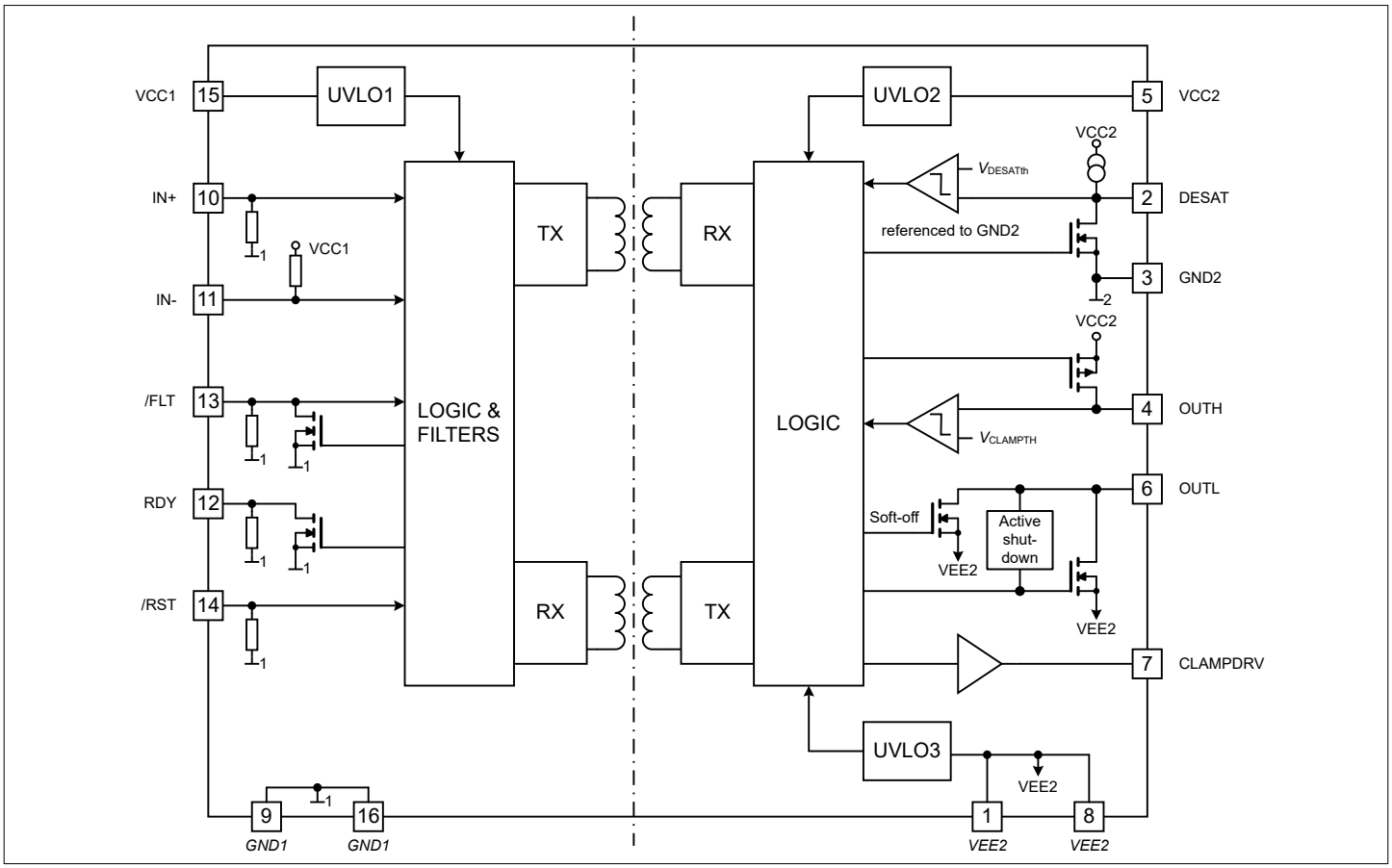


Figure 1 Block diagram

2 Pin configuration and functionality

2.1 Pin configuration

Table 1 Pin configuration

Pin No.	Name	Function
1	*VEE2*	Negative power supply output side
2	*DESAT*	Short circuit protection
3	*GND2*	Signal ground output side
4	*OUTH*	Driver charge output
5	*VCC2*	Positive power supply output side
6	*OUTL*	Driver discharge output
7	*CLAMPDRV*	Miller clamp driver
8	*VEE2*	Negative power supply output side
9	*GND1*	Ground input side

(table continues...)

Table 1 (continued) Pin configuration

Pin No.	Name	Function
10	*IN+*	Non-inverting driver input
11	*IN-*	Inverting driver input
12	*RDY*	Ready output
13	*/FLT*	Fault input and output, low active
14	*/RST*	Reset input, low active
15	*VCC1*	Positive power supply input side
16	*GND1*	Ground input side

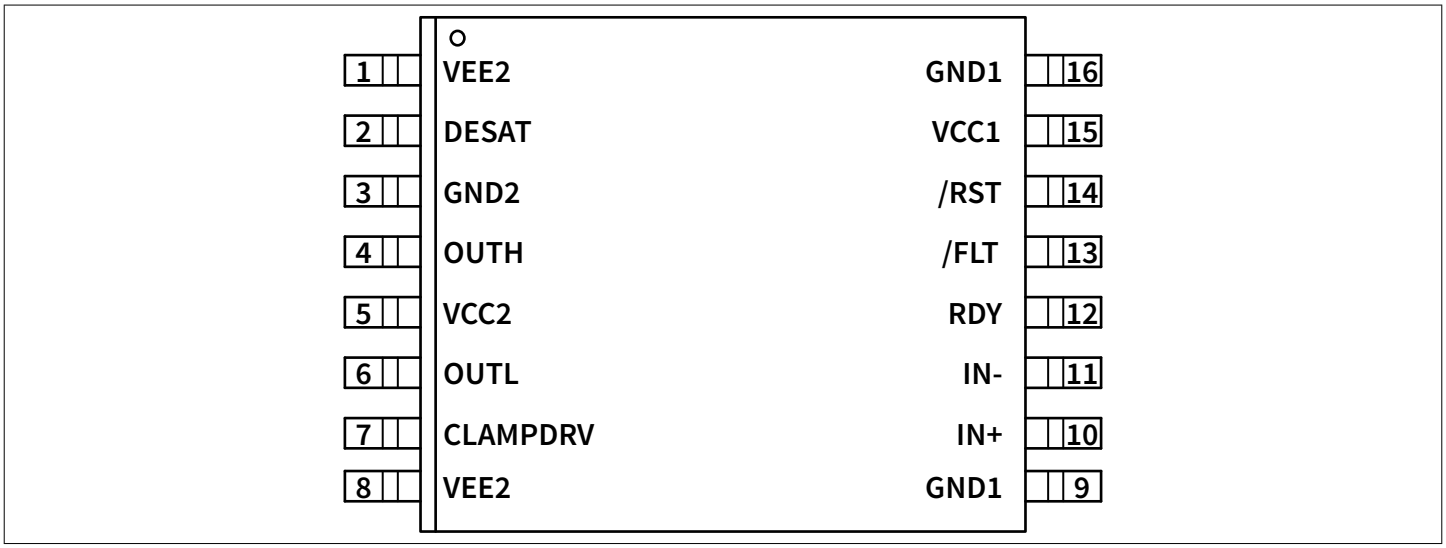


Figure 2 PG-DSO-16 (top view)

2.2 Pin functionality

GND1

Ground connection of the input side.

***IN+* non-inverting driver input**

IN+ control signal for the driver output if *IN-* is set to low. The driver output is on if *IN+* = high and *IN-* = low.

A minimum pulse width is defined to make the IC robust against glitches at *IN+*. An internal pull-down resistor ensuring the output to be low if the IN+ pin is left floating.

***IN-* inverting driver input**

IN- control signal for driver output if *IN+* is set to high. The driver output is on if *IN+* = high and *IN-* = low.

A minimum pulse width is defined to make the IC robust against glitches at *IN-*. An internal pull-up resistor ensuring the output to be low if the IN- pin is left floating.

***/RST* reset input**

Function 1: Enable/shutdown of the input side. The driver output is off if */RST* = low. A minimum pulse width is defined to make the IC robust against glitches at */RST*.

Function 2: Resets the DESAT-fault-state of the gate driver IC if */RST* is low for a time longer than t_{RST}. An internal pull-up resistor for initial start-up. Please connect to an appropriate fault reset logic.

/FLT fault input and output

Function 1: */FLT* input to shut down the driver output. A minimum pulse width is defined to make the IC robust against glitches at */FLT*. A weak pull-down ensures safe state no operation if pin is not actively pulled-up by external resistor.

Function 2: Open-drain output to report a latched DESAT fault of the power transistor, */FLT* is low if DESAT event occurs.

RDY ready status

Open-drain output together with an external pull-up resistor reports the correct operation of the device. The driver sets *RDY* to high if both the input and output side are above the UVLO level, the over-temperature protection is inactive, and the internal signal transmission is operational.

VCC1

5 V or 3.3 V power supply of the input side.

VEE2

Negative power supply pins of the output side.

DESAT desaturation detection input

Monitoring of the IGBT saturation voltage (V_{CE}) to detect DESAT caused by short circuits. The DESAT monitoring becomes active after the gate driver output has turned on and the defined leading edge blanking time has elapsed. If the V_{CE} voltage rises above the defined DESAT detection threshold value $V_{DESATth}$ for longer than the DESAT filter time $t_{DESATfilt}$, the DESAT protection is activated. The power switch is turned off and the DESAT event gets reported via */FLT*. The overall blanking time is adjustable by an external capacitor.

CLAMPDRV Miller clamp driver

Ties the gate voltage to *VEE2* through an external clamp transistor after the power transistor has been switched off. During turn-off, the gate voltage is monitored at *OUTH* and the clamp driver output is activated when the gate voltage goes below V_{CLAMP} (related to *VEE2*). Connect the gate of a n-channel MOSFET to this pin and the drain directly to the gate of the power switch. Finally connect the MOSFET source to *VEE2*.

GND2 reference ground

Signal reference ground of the output side.

OUTH driver output

Output pin to charge the power transistor gate. The pin is pulled to *VCC2*. In normal operating mode *OUTH* is controlled by *IN+*, *IN-*, */RST*, and */FLT*. During error mode (UVLO, over temperature protection, internal signal transmission, or DESAT) and off state the *OUTH* is high impedance.

OUTL driver output

Output pin to discharge the power transistor gate. The pin is pulled to *VEE2*. In normal operating mode *OUTL* is controlled by *IN+*, *IN-*, */RST*, and */FLT*. During error mode the driver turns off with the following behavior:

- *OUTL* pulls down to *VEE2* (UVLO, over temperature protection, or internal signal transmission)
- *OUTL* pulls down using the soft-off current I_{SOFF0} (DESAT)

VCC2

Positive power supply pin of the output side.

3 Functional description

3.1 Introduction

The 1ED3330 is an advanced gate driver for IGBTs, Si and SiC MOSFETS. The included control and protection functions enable the design of highly reliable systems.

The driver consists of two galvanically isolated parts. The input side can be directly connected to a standard 3.3 V or 5 V DSP or microcontroller with CMOS input/output and the output side is connected to the high voltage side.

The rail-to-rail driver output provides a clamping path for the power transistor gate voltage during short circuit conditions. So, an increase of short circuit current due to the feedback via the Miller capacitance can be reduced, depending on the gate resistor. Additionally, the rail-to-rail output reduces power dissipation.

The device also includes IGBT short circuit protection (DESAT) with */FLT* status output.

The *RDY* status output reports that the gate driver IC is supplied properly and is ready to operate.

3.2 Supply

The driver 1ED3330 is designed to support bipolar supply with a negative supply lower than -3 V.

The gate driver is typically supplied with a positive voltage of 15 V at *VCC2* and a negative voltage of -8 V at *VEE2*, please refer to Figure 3. Negative supply prevents a dynamic turn on.

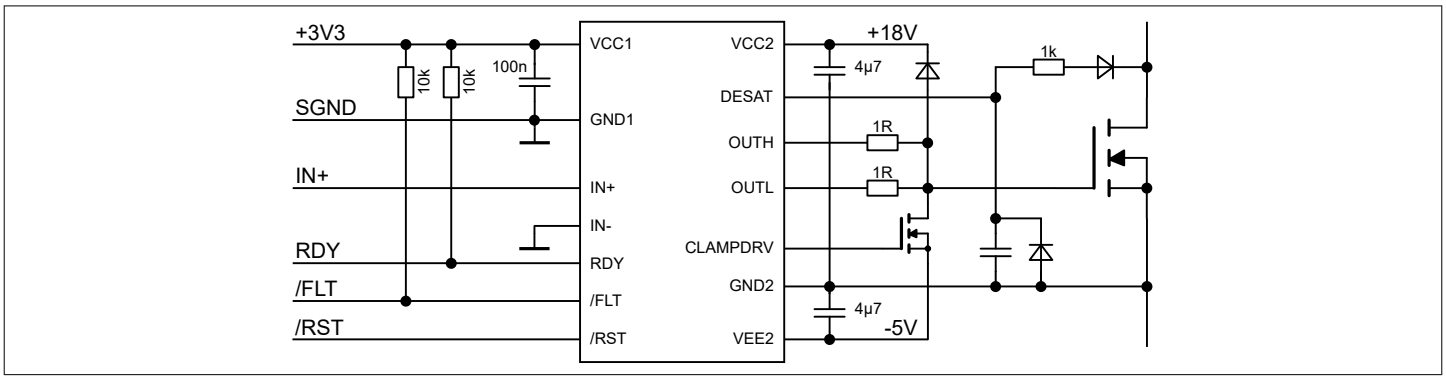


Figure 3 Application example bipolar supply

3.2.1 Undervoltage lockout (UVLO)

To ensure correct switching of the power transistor the gate driver IC is equipped with an input side and two output side undervoltage lockout circuits. Refer to the diagrams showing the undervoltage lockout function of *VCC1* Figure 4, *VCC2* Figure 5, and *VEE2* Figure 6.

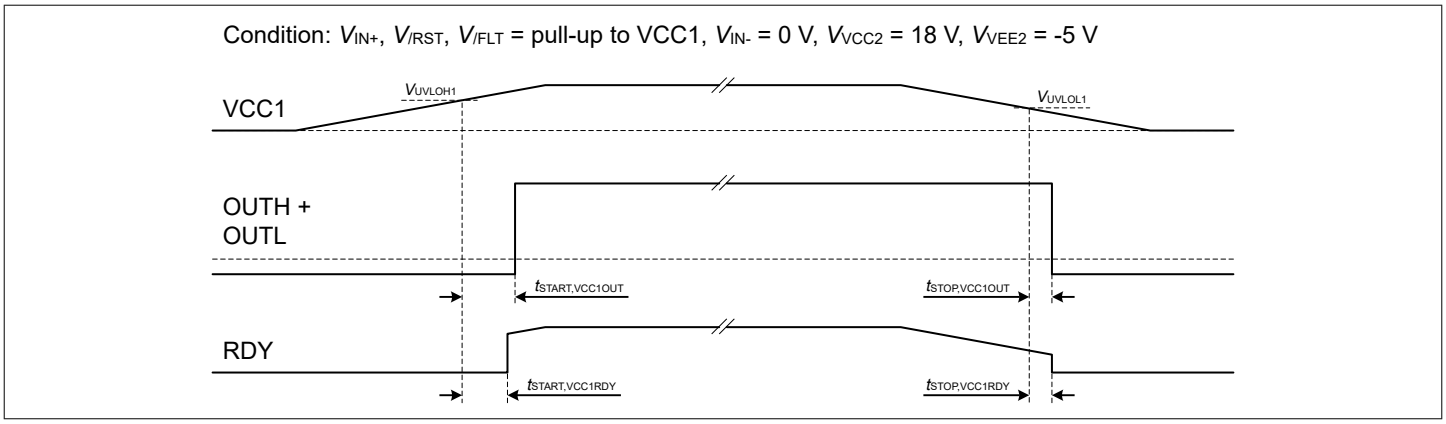


Figure 4 UVLO1

If the power supply voltage *VCC1* of the input side drops below V_{UVLOL1} a turn-off signal is sent to the output side before the input side powers down. The power transistor is switched off and the signals at *IN+* and *IN-* are ignored as long as *VCC1* is below the power-up voltage V_{UVLOH1}.

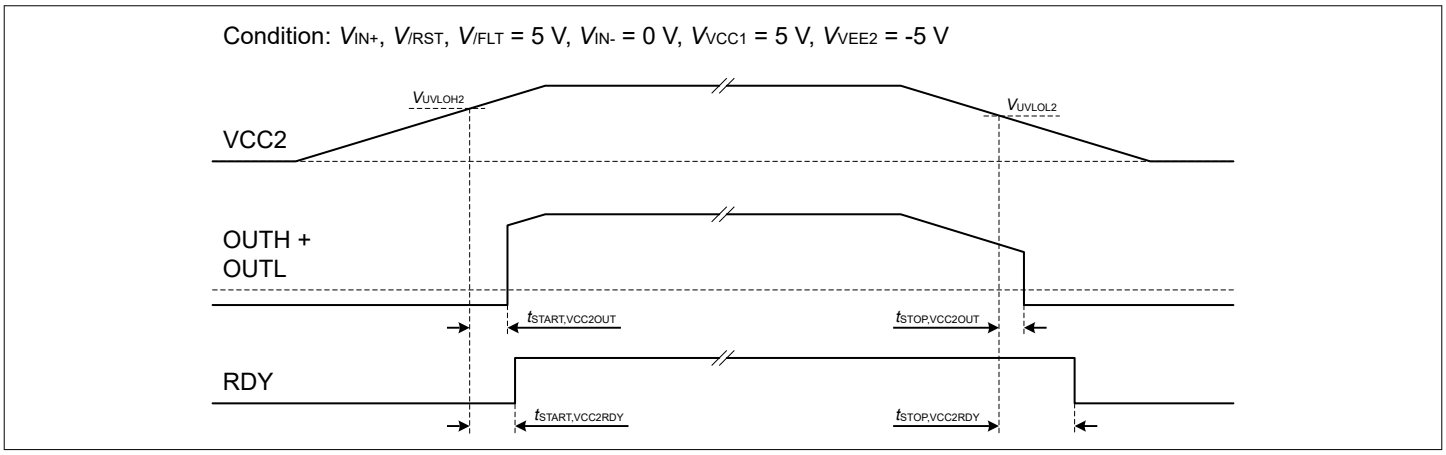


Figure 5 UVLO2

If the power supply voltage *VCC2* of the output side goes below V_{UVLOL2} the power transistor is switched off and signals from the input side are ignored as long as *VCC2* stays below the power-up voltage V_{UVLOH2}.

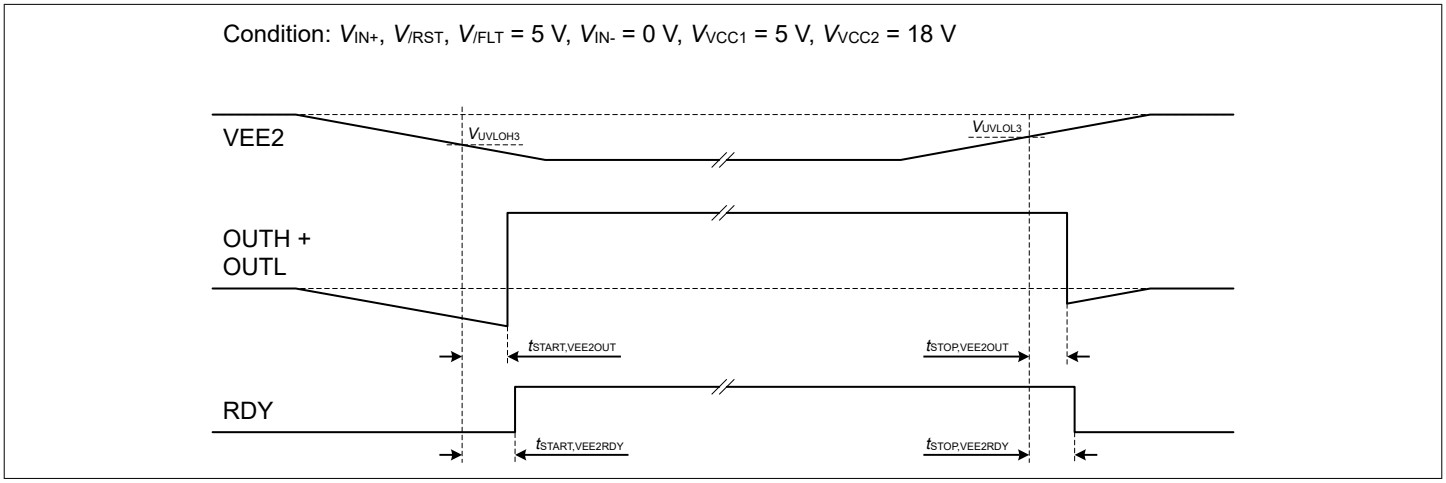


Figure 6 UVLO3

If the power supply voltage of *VEE2* of the output side goes above V_{UVLOL3} the power transistor is switched off. Signals from the input side are ignored as long as *VEE2* stays above the power-up voltage V_{UVLOH3}.

3.3 Input side logic pins

3.3.1 Non-inverting and inverting inputs

There are two possible input modes to control the power switch.

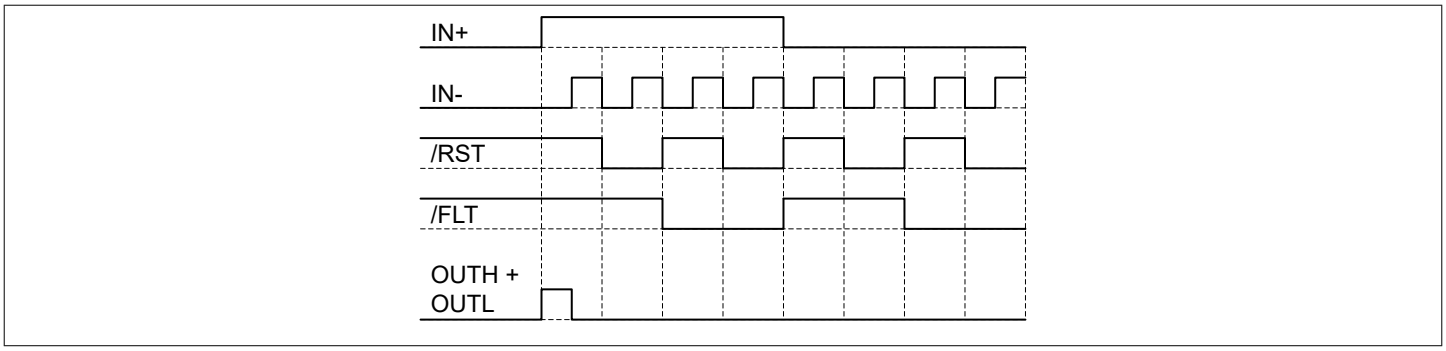


Figure 7 Typical switching behavior

In the non-inverting mode *IN+* controls the driver output while *IN-* is set to low. In the inverting mode *IN-* controls the driver output while *IN+* is set to high.

Logic: *OUTL*/*OUTH* = *IN+* AND NOT(*IN-*) AND */RST* AND */FLT*

A minimum input pulse width is defined to filter occasional glitches.

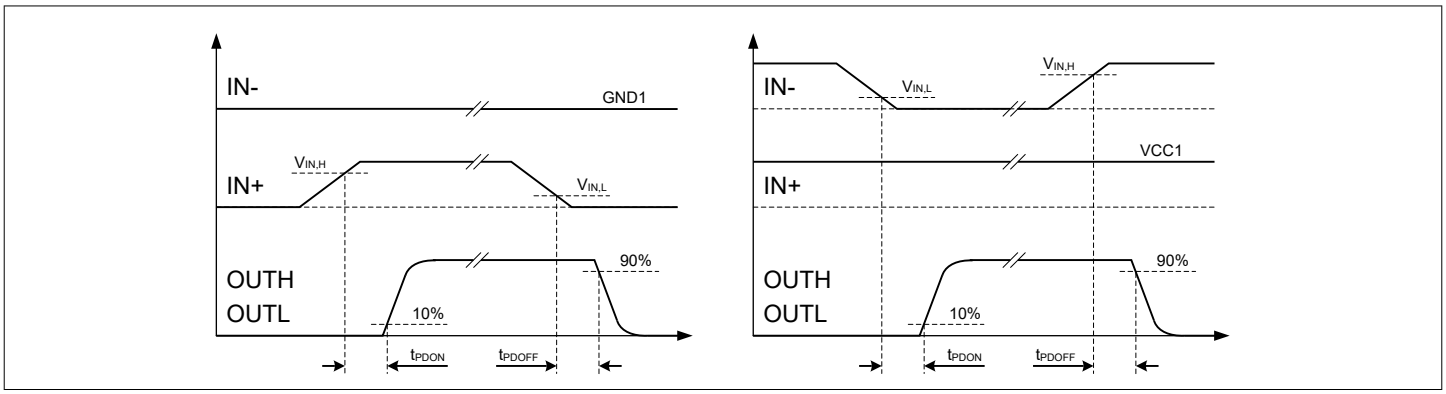


Figure 8 Propagation delay time *IN+* and *IN-*

The output will react with the propagation delay time after change of the input signals. Figure 8 shows the propagation delay time of the individual PWM input pins.

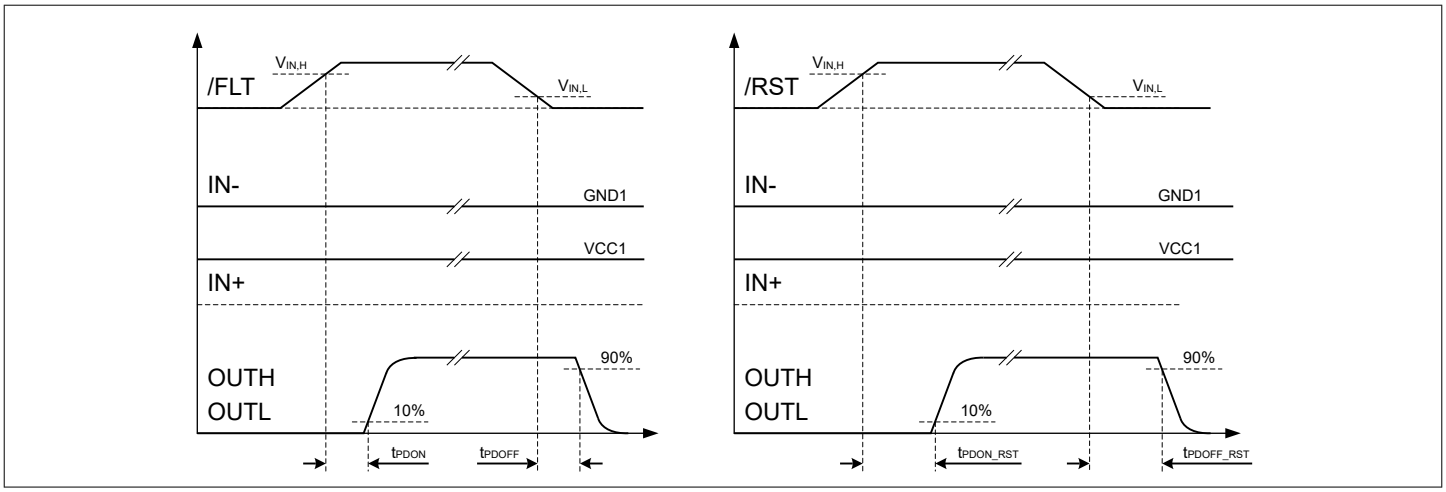


Figure 9 Propagation delay time */FLT* and */RST*

The propagation delay of the */FLT* is equal to the input *IN* propagation delay. The */RST* pin propagation delay differ from the regular PWM input pins to ensure stronger filtering.

3.3.2 Ready status output *RDY*

The *RDY* output shows the status of the following internal protection features:

- UVLO of the input side
- UVLOs for *VCC2* and *VEE2* of the output side
- Internal signal transmission (watchdog)

  During normal operation the internal signal transmission is monitored by a watchdog timer. If the transmission fails for a given time, the IGBT is switched off and the *RDY* output reports an internal error
- Over temperature protection (OTP) of the output side
- Ready to clear latched fault status after DESAT event

It is not necessary to reset the *RDY* signal since its state only depends on the status of the former mentioned protection signals.

3.3.3 Reset

The reset */RST* is in charge of setting back the */FLT* output. If */RST* is low longer than a given time t_{RST}, */FLT* will be cleared at the rising edge of */RST*, refer to Figure 11 otherwise, it will remain unchanged.

The reset (*/RST* to low for longer than t_{RST}) after DESAT event can only be performed after *RDY* is released to high. This indicates that the gate of the external power switch is completely discharged and the power switch has turned off.

The reset */RST* works as enable/shutdown of the input logic, refer to Figure 7.

3.3.4 Fault signal

The primary function of the */FLT* pin is to signal a DESAT event to the microcontroller. After a DESAT detection it takes the gate driver typically 60 ns to pull the */FLT* pin to low.

Additionally the pin acts as an input to trigger a hard switch-off at the output when pulled to low externally. By combining multiple */FLT* pins of these gate driver ICs together as a single signal, all gate driver ICs will switch-off in case a single driver detects a DESAT event.

3.4 Driver output

The output driver stage uses only complementary MOSFETs to provide a rail-to-rail output. This feature permits that tight control of gate voltage, during on-state and short circuit, as long as a stable driver supply voltage is maintained.

Due to the low internal voltage drop, switching behavior of the power switch is predominantly governed by the gate resistor. Furthermore, it reduces the power dissipated by the driver.

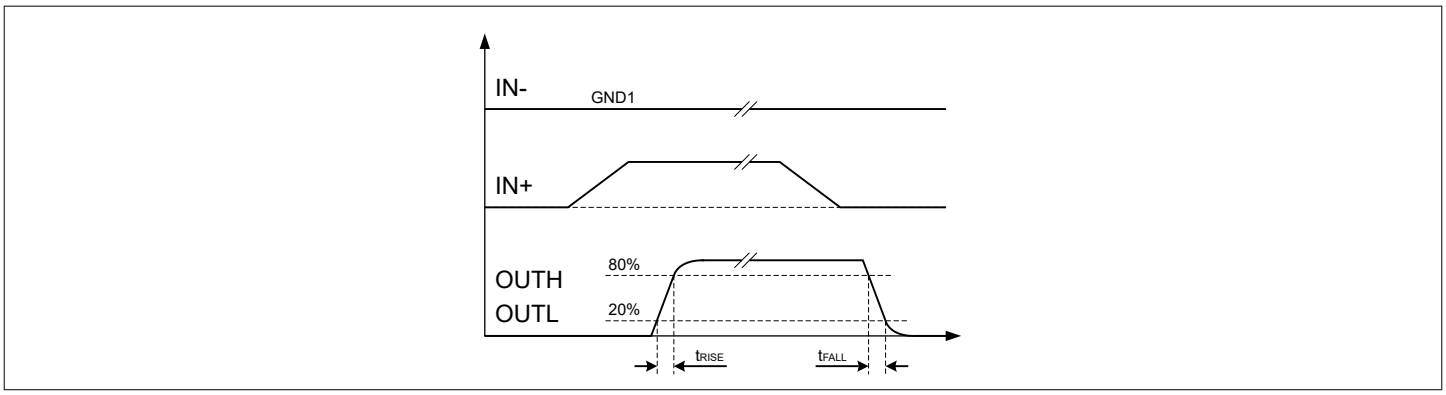


Figure 10 Rise and fall times

The outputs are not able to instantaneous change their level. The individual switch-on and switch-off duration is specified by the parameter t_{RISE} and t_{FALL}.

3.5 Protection features

3.5.1 Short-circuit protection (DESAT)

A short-circuit protection (DESAT) ensures the protection of the power switch during short-circuit. When the *DESAT* voltage rises and stays above the DESAT detection threshold of 9 V for longer than the DESAT filter time, the output is driven low using the soft-off switch-off method. Further, the */FLT* output is activated after *DESAT* to */FLT*off delay.

The DESAT signal is filtered using an enhanced asymmetric up/reset filter to improve ruggedness against false DESAT triggering.

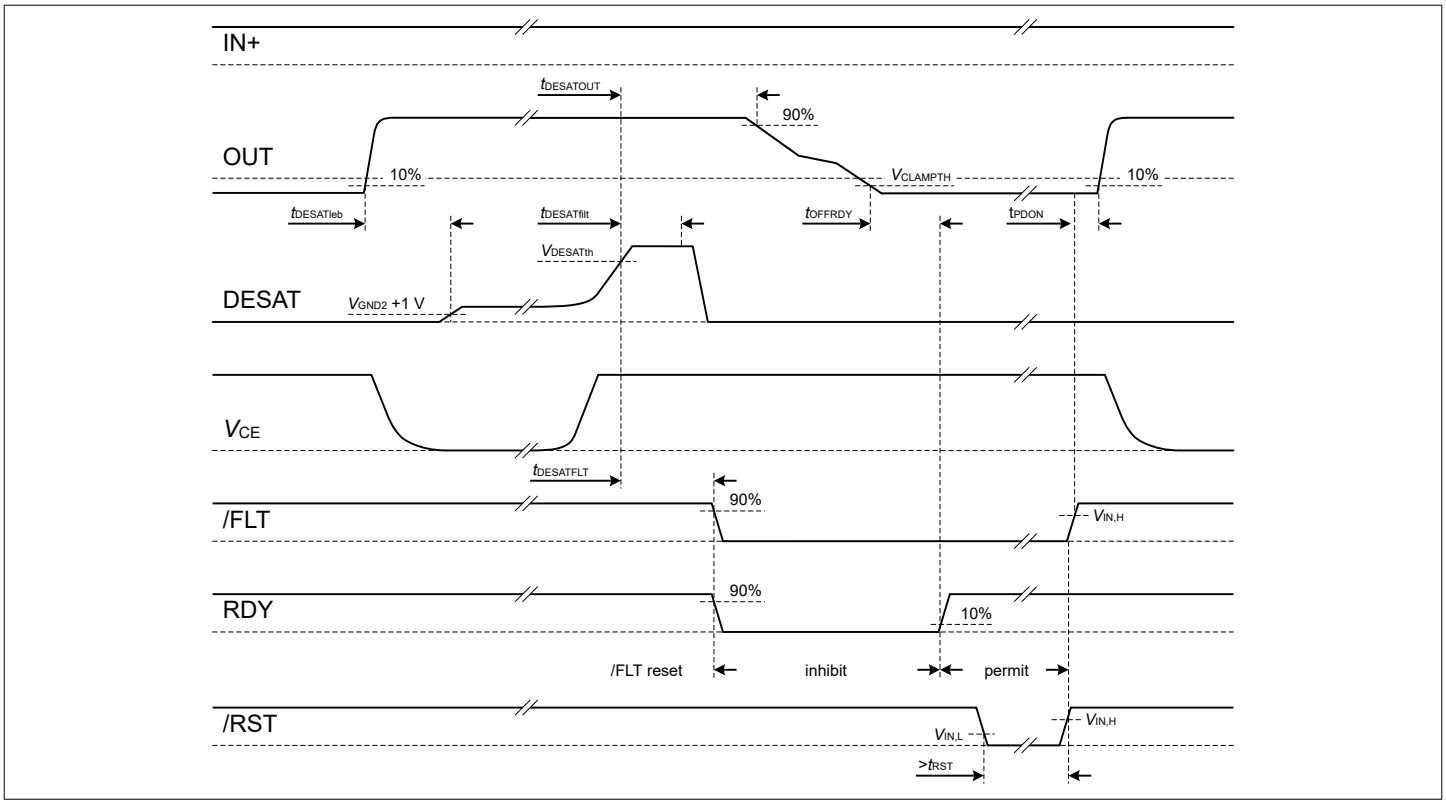


Figure 11 DESAT soft-off behavior and timings

The leading edge blanking time is used to allow enough time for the power switch to reach saturation levels. The *DESAT* level rise time is influenced by a precise internal current source and an external capacitor.

3.5.2 Active Miller clamp

The gate driver IC is equipped with an active Miller clamp function to prevent the switch experiencing a parasitic turn-on in fast switching applications.

After a turn-off command the gate driver IC follows the implemented sequence:

1. Discharge of the gate while monitoring the voltage level at the *OUTH* pin
2. Detection of the *OUTH* voltage to be less than the CLAMP threshold level $V_{CLAMPTH}$
3. Filtering of the detection to avoid false CLAMP activation and not to influence regular turn-off behavior
4. Activating clamp function to keep the switch gate at *VEE2* level

Pre-driver output

The CLAMP function is implemented as a pre-driver with limited output voltage, to clamp the switch gate with an external transistor for high clamping current. Depending on the external MOSFET a Miller current clamping up to 20 A can be reached.

The external small signal n-channel MOSFET transistor in combination with the pre-driver output enables clamping of high gate currents. Connect the MOSFET between the *CLAMPDRV* output, *VEE2* pin, and the switch gate. The clamping MOSFET has to be placed close to the switch gate to minimize track resistance and inductance.

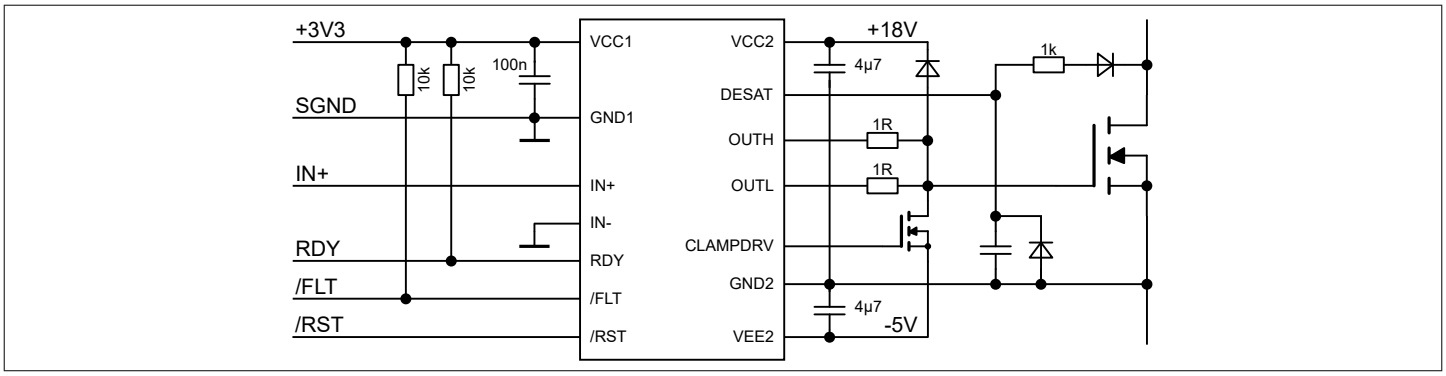


Figure 12 Application example with bipolar supply and CLAMP pre-driver output

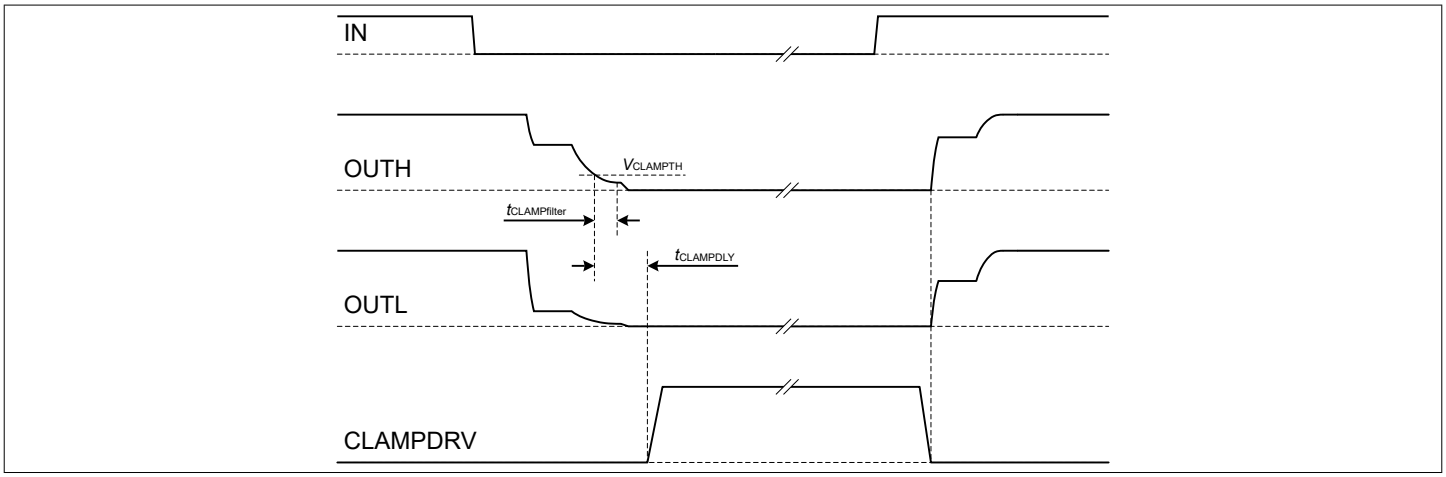


Figure 13 Clamp pre-driver output behavior

3.5.3 Active shutdown

The active shut-down feature ensures a safe power transistor off-state if the output side is not connected to the power supply. The power transistor gate is clamped by *OUTL* to *VEE2*.

4 Electrical parameters

4.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Operating the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device reliability may be affected by exposure to absolute-maximum-rated conditions for extended periods of time.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power supply input side voltage	V_{VCC1}	-0.3		6.5	V	V_{VCC1} - V_{GND1}
Positive power supply output side voltage	V_{VCC2}	-0.3		35	V	V_{VCC2} - V_{GND2}
Negative power supply output side voltage	V_{VEE2}	-35		0.3	V	V_{VEE2} - V_{GND2}
Differential power supply output side voltage	V_{DVMAX2}	-0.3		35	V	V_{VCC2} - V_{VEE2}
Gate driver source output voltage	V_{OUTH}	V_{VCC2} - 35		V_{VCC2} + 0.3	V	
Gate driver sink output voltage	V_{OUTL}	V_{VEE2} - 0.3		V_{VEE2} + 35	V	
Dynamic CLAMPDRV voltage	V_{CLPDRV}	V_{VEE2} - 0.3		15	V	for 1 µs, vs. VEE2
DESAT voltage	V_{DESAT}	- 0.3		V_{VCC2} + 0.3	V	
Logic input pin voltages (IN+, IN-, /RST)	V_{IN}	-0.3		6.5	V	
Logic pin voltages, open drain (/FLT, RDY)	V_{FLT}, V_{RDY}	- 0.3		6.5	V	
Logic output currents, open drain (/FLT, RDY)	I_{FLT}, I_{RDY}			50	mA	
Input to output offset voltage	V_{OFFSET}			2300	V	1) $V_{OFFSET} = \lvert V_{GND2} - V_{GND1} \rvert$
ESD robustness - human body model	$\lvert V_{ESD,HBM} \rvert$			4	kV	2)
ESD robustness - charged device model	*ESD,CDM*			TC1500		3)
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{Stg}	-55		150	°C	
Power dissipation (input side)	$P_{D,IN}$			33	mW	4) T_A = 85 °C
Power dissipation (output side)	$P_{D,OUT}$			738	mW	4) 5) T_A = 85 °C
Power dissipation, total	P_D			771	mW	4) 5) T_A = 85 °C

1) for functional operation only
2) According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).
3) According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = test condition in volt)

4) IC total power dissipation derating linearly with 11.9 mW/K above 85°C
5) With R_{thJA} according to JESD 51-7 standard, 2s2p and a metallization of 70 / 35 / 35 / 70 [µm]

4.2 Thermal parameter

Table 3 Thermal parameter

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Thermal resistance junction to ambient	R_{thJA}		84.3		K/W	1) T_A = 85 °C, P_D = 771 mW
Characterization parameter junction to package top	Ψ_{Jtop}		13		K/W	1) T_A = 85 °C, P_D = 771 mW

1) According to JESD 51-7 standard, 2s2p and a metallization of 70 / 35 / 35 / 70 [µm], $P_{D,IN}$ = 33 mW, $P_{D,OUT}$ = 738 mW

4.3 Recommended operating conditions

Table 4 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power supply input side voltage	V_{VCC1}	3.0		5.5	V	V_{VCC1} - V_{GND1}
Positive power supply output side voltage	V_{VCC2}	14		32	V	V_{VCC2} - V_{GND2}, 1ED3330
Negative power supply output side voltage	V_{VEE2}	-10		-2.85	V	V_{VEE2} - V_{GND2}, 1ED3330
Differential power supply output side voltage	V_{DVMAX2}	16.85		32	V	V_{VCC2} - V_{VEE2}, 1ED3330
Logic input voltages (IN+, IN-, / FLT, /RST)	V_{IN}	-0.3		5.5	V	
DESAT voltage	V_{DESAT}	-0.3		V_{VCC2} + 0.3	V	
Ambient temperature	T_A	-40		125	°C	
Junction temperature	T_J	-40		150	°C	

4.4 Electrical characteristics

The electrical characteristics include the spread of values over supply voltages and temperatures within the recommended operating conditions. Electrical characteristics are tested in production at T_A = 25 °C. Typical values represent the median values measured at V_{VCC1} = 5.0 V, V_{VCC2} = 18 V, V_{VEE2} = -5 V, and T_A = 25 °C. Minimum and maximum values in characteristics are verified by characterization/design. This is valid for all electrical characteristics unless specified otherwise.

4.4.1 Power supply

Table 5 Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UVLO1 threshold input side (on)	V_{UVLOH1}		2.83	3.0	V	V_{VCC1} - V_{GND1}
UVLO1 threshold input side (off)	V_{UVLOL1}	2.5	2.61		V	V_{VCC1} - V_{GND1}
UVLO1 hysteresis input side	V_{HYS1}	0.17	0.22	0.27	V	V_{UVLOH1} - V_{UVLOL1}
UVLOL1 filter (off)	$t_{UVLOL1ft}$	400	600	900	ns	1)
Quiescent current input side	I_{Q1}			3	mA	2) , 3)
Operating current input side	I_{O1}			3	mA	4)
UVLO2 threshold output side (on)	V_{UVLOH2}		13.6	14	V	V_{VCC2} - V_{GND2}
UVLO2 threshold output side (off)	V_{UVLOL2}	12.15	12.55		V	V_{VCC2} - V_{GND2}
UVLO2 hysteresis output side	V_{HYS2}		1.05		V	V_{UVLOH2} - V_{UVLOL2}
UVLOL2 filter (off)	$t_{UVLOL2ft}$	0.5	0.75	1	µs	1)
Quiescent current output side, ON state	$I_{QVCC2,ON}$			3	mA	2)
Quiescent current output side, OFF state	$I_{QVCC2,OFF}$			2.1	mA	3)
Operating current output side	I_{OVCC2}			3	mA	4)
UVLO3 threshold output side (on)	V_{UVLOH3}	-2.85	-2.7	-2.5	V	V_{VEE2} - V_{GND2}
UVLO3 threshold output side (off)	V_{UVLOL3}	-1.7	-1.5	-1.3	V	V_{VEE2} - V_{GND2}
UVLO3 hysteresis output side	V_{HYS3}		1.2		V	V_{UVLOL3} - V_{UVLOH3}
UVLOL3 filter (off)	$t_{UVLOL3ft}$	6	8	11	µs	1)

1) Parameter is not subject to production test - verified by design/characterization.
2) V_{VCC1} = 5 V, V_{VCC2} = 18 V, V_{VEE2} = - 5 V, *IN+* = High, *IN-* = Low, *OUT* = High, *RDY*, */RST*, */FLT* = High, V_{DESAT} = 0 V
3) V_{VCC1} = 5 V, V_{VCC2} = 18 V, V_{VEE2} = - 5 V, *IN+* = Low, *IN-* = High, *OUT* = Low, *RDY*, */RST*, */FLT* = High, V_{DESAT} = 0 V
4) V_{VCC1} = 5 V, V_{VCC2} = 18 V, V_{VEE2} = - 5 V, *IN+* = 50 kHz, 50%, *IN-* = Low, *RDY* = High, */FLT* = High, C_L = 100 pF, V_{DESAT} = 0 V

4.4.2 Logic input and output

Table 6 Logic input and output

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input low threshold voltage IN+, IN-, /RST, /FLT	$V_{IN,L}$	0.3 * V_{VCC1}			V	
Input high threshold voltage IN+, IN-, /RST, /FLT	$V_{IN,H}$			0.7 * V_{VCC1}	V	
Input hysteresis voltage IN+, IN-, /RST, /FLT	$V_{IN,HYS}$	0.1 * V_{VCC1}			V	
Input pull-up resistance IN-	R_{IN-}	34	45	56	kΩ	V_{IN-} = *GND1*

(table continues...)

Table 6 (continued) Logic input and output

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input pull-down resistance IN+, /RST	R_{IN+}, R_{RST}	42	56	70	kΩ	V_{IN+}, V_{RST} = V_{VCC1}
Input pull-down resistance RDY, /FLT	R_{RDY}, R_{FLT}	330	450	565	kΩ	V_{RDY}, V_{FLT} = *GND1*
Output low voltage RDY, /FLT	V_{RDYL}, V_{FLTL}			300	mV	I_{SINK} = 10 mA

4.4.3 Gate driver

Table 7 Gate driver

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High level output peak current	I_{OUTH}	7	12		A	IN+ = High, IN- = Low 1) 2)
Low level output peak current	I_{OUTL}	7	13		A	IN+ = High, IN- = Low 1) 2)
High level output on resistance	$R_{DSON,H}$	0.15	0.45	1.05	Ω	I_{OUTH} = 0.2 A
Low level output on resistance	$R_{DSON,L}$	0.1	0.25	0.55	Ω	I_{OUTL} = 0.2 A

1) V_{VCC2} = 18 V, V_{VEE2} = -5 V, C_L = 100 nF, R_L = 0.1 Ω
2) Parameter is not subject to production test - verified by design/characterization

4.4.4 Active Miller clamp

Table 8 Active Miller clamp

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Clamp threshold voltage	$V_{CLAMPTH}$	V_{VEE2} + 2	V_{VEE2} + 2.4	V_{VEE2} + 2.8	V	
Clamp filter time	$t_{CLAMPfilter}$	18		30	ns	
Clamp activation delay	$t_{CLAMPDLY}$			70	ns	$V_{OUTH} \le V_{CLAMPTH}$ to $V_{CLAMPDRV} \ge V_{VEE2}$ + 2 V, $C_{CLAMPDRV}$, C_{LOAD} = 100 pF
Clamp driver high level output peak current	$I_{CLAMPDH}$	0.15	0.27		A	$R_{CLAMPDRV}$ = 1 Ω 1) 2)
Clamp driver low level output peak current	$I_{CLAMPDL}$	1	1.5		A	$R_{CLAMPDRV}$ = 1 Ω 1) 2)
Clamp driver high level output voltage	$V_{CLAMPDH}$	V_{VEE2} +6	V_{VEE2} +8	V_{VEE2} +10	V	V_{VCC2} = 18 V, V_{VEE2} = -5 V, I_{LOAD} = 0 mA
Low level clamp driver on resistance	$R_{DSON,CLP}$	0.4	1	2.2	Ω	I_{CLAMPL} = 0.1 A

1) Parameter is not subject to production test - verified by design/characterization
2) V_{VCC2} = 18 V, V_{VEE2} = -5 V, $C_{CLAMPDRV}$ = 100 nF

4.4.5 Dynamic characteristics

Table 9 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input to output propagation delay ON for IN+, IN-, /FLT	t_{PDON}	61	73	85	ns	V_{VCC2} - V_{VEE2} = 23 V, C_L = 100 pF
Input to output propagation delay OFF for IN+, IN-, /FLT	t_{PDOFF}	61	74	85	ns	V_{VCC2} - V_{VEE2} = 23 V, C_L = 100 pF
Input to output propagation delay distortion IN+	$\lvert t_{PDISTO,IN+} \rvert$		0	6	ns	1) $\lvert t_{PDOFF} - t_{PDON} \rvert$
Input to output propagation delay distortion IN-	$\lvert t_{PDISTO,IN-} \rvert$		0	6	ns	1) $\lvert t_{PDOFF} - t_{PDON} \rvert$
Input to output, part to part skew	t_{SKEW}			6	ns	2) C_L = 100 pF
Input to output, part to part skew plus	t_{SKEW+}		0	8	ns	3) C_L = 100 pF
Input pulse suppression filter time	t_{IPSF}	26	33	40	ns	4)
/RST input pulse suppression time (filter time)	$t_{RSTfilt}$	180		330	ns	V_{VCC1} = 3.3 V
Input-side start-up time	$t_{START,VCC1OUT}$, $t_{START,VCC1RDY}$		2.5	10	µs	5) IN+ = High, C_L = 100pF, fast V_{VCC1} ramp, OUTH, RDY 10%
Output-side start-up time	$t_{START,VCC2OUT}$, $t_{START,VCC2RDY}$		5	12	µs	5) IN+ = High, C_L = 100 pF, fast V_{VCC2} ramp, OUTH, RDY 10%
Output-side start-up time	$t_{START,VEE2OUT}$, $t_{START,VEE2RDY}$	0.1		2.2	µs	5) IN+ = High, C_L = 100 pF, fast V_{VEE2} ramp, OUTH, RDY 10%
Input-side deactivation time	$t_{STOP,VCC1OUT}$, $t_{STOP,VCC1RDY}$		2.5	10	µs	5) IN+ = High, IN- = Low, ramp VCC1 = 3.3 V to 0 V, C_L = 100pF, OUTH, RDY to 90%
Output-side VCC2 to OUT deactivation time	$t_{STOP,VCC2OUT}$	0.5		1.2	µs	5) IN+ = High, IN- = Low, ramp V_{VCC2} = 18 V to 0 V, C_L = 100 pF
Output-side VEE2 to OUT deactivation time	$t_{STOP,VEE2OUT}$	0.2 + $t_{UVLOL3ft}$		1 + $t_{UVLOL3ft}$	µs	5) IN+ = High, IN- = Low, ramp V_{VEE2} = -5 V to 0 V, C_L = 100 pF
Rise time	t_{RISE}			20	ns	V_{VCC2} = 18 V, V_{VEE2} = -5 V, C_L = 1 nF, V_{OUTH} rising from 20% to 80%
Rise time	t_{RISE}		65	90	ns	V_{VCC2} = 18 V, V_{VEE2} = -5 V, C_L = 20 nF, R_L = 1 Ω, V_{OUTH} rising from 10% to 90%, valid only for 1ED3330, rise time measured at C_L 5)

(table continues...)

Table 9 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Fall time	t_{FALL}			20	ns	V_{VCC2} = 18 V, V_{VEE2} = -5 V, C_L = 1 nF, V_{OUTL} falling from 80% to 20%
Fall time	t_{FALL}		60	85	ns	V_{VCC2} = 18 V, V_{VEE2} = -5 V, C_L = 20 nF, R_L = 1 Ω, V_{OUTL} falling from 90% to 10%, valid only for 1ED3330, Fall time measured at C_L 5)
Common-mode transient immunity	$\lvert CM_{Static} \rvert$	200			kV/µs	@ V_{CM} = 1.5 kV5)
Dynamic common-mode transient immunity	$\lvert CM_{Dynamic} \rvert$	200			kV/µs	V_{CM} = 1.5 kV; *IN-* tied to *GND1*; *IN+* = 10 MHz square wave5)

1) Value at same ambient temperature and operating conditions.
2) Difference in propagation delay for an ON or OFF command driven by the same input pin (IN+ or IN-, not a mix of the two pins) and same edge. Value at same ambient temperature and operating conditions. This parameter was previously called input to output, part to part propagation delay variation.
3) The parameter gives the difference between the ON propagation delay of one driver and the OFF propagation delay of another driver and any input combination of the input signals IN+, IN- at same ambient temperature and operating condition.
4) Input pulses shorter than $t_{IPSF,min}$ will always be suppressed, input pulses longer than $t_{IPSF,max}$ will always be propagated.
5) Parameter is not subject to production test - verified by design/characterization

4.4.6 Soft-off

Table 10 Soft-off

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Soft-off current	I_{SOFF0}	770	1100	1430	mA	V_{OUTL} = V_{VEE2} + 4 ... 20 V 1) 2)
Soft-off time-out time	t_{SOFFTO}	$t_{DESATfilt}$ + 2.6	$t_{DESATfilt}$ + 2.9	$t_{DESATfilt}$ + 3.1	µs	3)

1) V_{VCC2} = 18 V, V_{VEE2} = -5 V, C_L = 22 nF , R_L = 1 Ω
2) Parameter is not subject to production test - verified by design/characterization.
3) V_{VCC2} = 18 V, V_{VEE2} = -5 V, C_L = 22 nF , R_L = 1 Ω

4.4.7 Desaturation protection

Table 11 Desaturation protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DESAT threshold level	$V_{DESATth}$	8.54	9	9.46	V	V_{VCC2} = 18 V, V_{VEE2} = -5 V

(table continues...)

Table 11 (continued) Desaturation protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
DESAT capacitor charge current	I_{DESATC}	425	500	575	µA	V_{VCC2} = 18 V, V_{VEE2} = -5 V, V_{DESAT}-V_{GND2} = 0 V
DESAT clamp current	$I_{DESATCLAMP}$	90	150		mA	V_{VCC2} = 18 V, V_{VEE2} = -5 V, V_{DESAT} - V_{GND2} = 6 V
DESAT sense voltage divider resistance	R_{DVD}		750		kΩ	between DESAT and GND2
DESAT clamp on resistance	$R_{DSOND,L}$		7	14	Ω	I_{DESAT} = 70 mA
Leading edge blanking	$t_{DESATleb}$	25	40	50	ns	1) V_{OUTH} rising 10% to V_{DESAT} rising 1 V
DESAT filter time	$t_{DESATfilt}$	75	100	125	ns	1)
DESAT sense to /FLT delay	$t_{DESATFLT}$			$t_{DESATfilt}$ + 75	ns	$V_{DESAT} \geq V_{DESATth}$ rising to V_{FLTL} = 90 % falling, I_{FLT} = 10 mA, C_{FLT} = 100 pF
DESAT sense to soft-off delay	$t_{DESATOUT}$			$t_{DESATfilt}$ + 150	ns	$V_{DESAT} \geq V_{DESATth}$ rising to V_{OUTL} 90%, C_L = 100 pF
DESAT OUTH low to RDY delay	t_{OFFRDY}	0.2		30	µs	1)
DESAT to soft-off discharge time	$t_{DESATSOO0}$	$t_{DESATfilt}$ + 350	$t_{DESATfilt}$ + 470	$t_{DESATfilt}$ + 700	ns	I_{SOFF0} 2)
Fault-clear time	t_{RST}	800			ns	RDY = high, /FLT = low

1) Parameter is not subject to production test - verified by design/characterization
2) $V_{DESAT} \geq V_{DESATth}$ rising to $V_{OUTL} = V_{VEE2}$ + 5 V, C_L = 22 nF, OUTH connected to OUTL, V_{VCC2} = 18 V, V_{VEE2} = -5 V

4.4.8 Active shut down

Table 12 Active shut down

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Active shut down voltage	V_{ACTSD}			1.8	V	V_{OUTL} - V_{VEE2}, I_{OUTL} = 1 A, *VCC2* open, *OUTH* connected to R_G

4.4.9 Over temperature protection

Table 13 Over temperature protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Over temperature protection temperature	T_{OTPOFF}	155	165	175	°C	1)
Over temperature protection release level	T_{OTPREL}	135	145	155	°C	1)

(table continues...)

Table 13 (continued) Over temperature protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Over temperature protection hysteresis	T_{OTPHYS}		20		°C	1)

1) Parameter is not subject to production test - verified by design/characterization

5 Insulation characteristics (IEC 60747-17, UL 1577) for PG-DSO-16 package

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

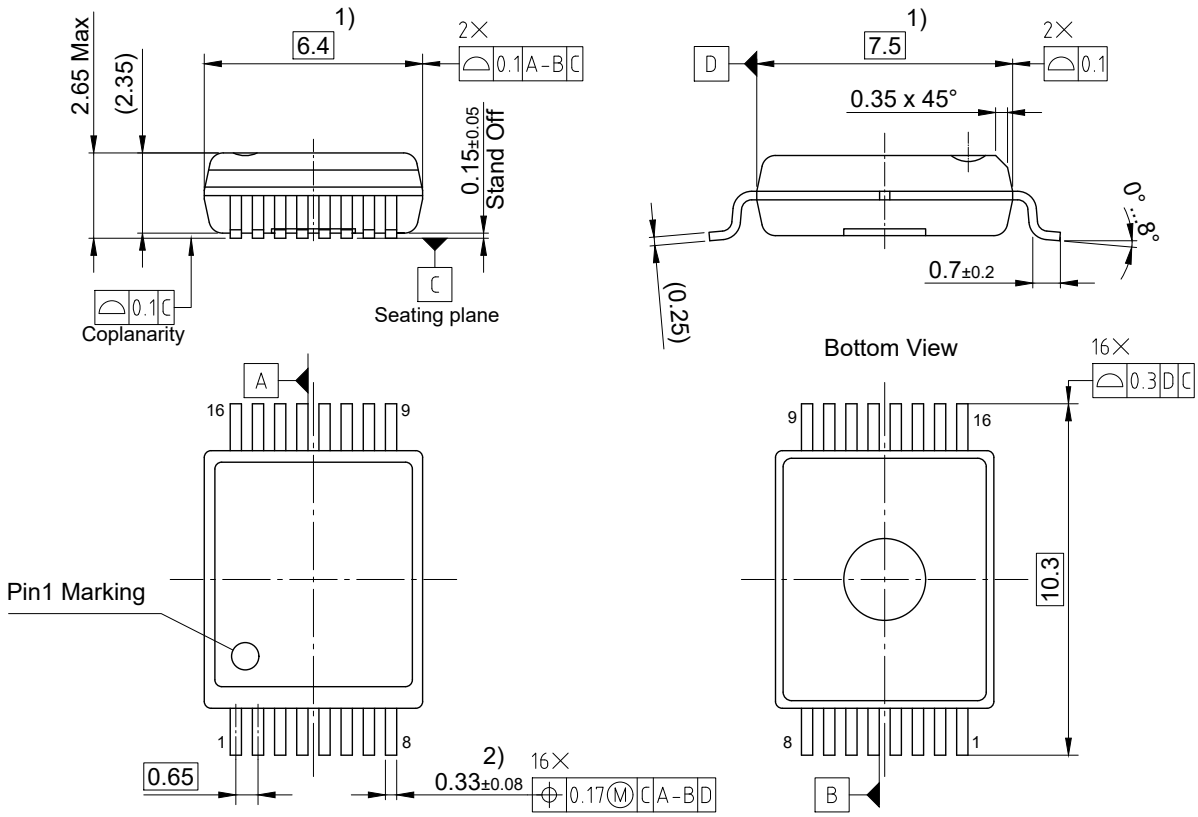
Table 14 Insulation specification for PG-DSO-16 package

Description	Symbol	Characteristic	Unit
Safety limiting values			
Maximum ambient safety temperature	T_S	150	°C
Maximum input-side power dissipation at T_A = 25°C[1)]	P_{SI}	100	mW
Maximum output-side power dissipation at T_A = 25°C[2)]	P_{SO}	1380	mW
Package specific insulation characteristics			
External clearance	*CLR*	> 8	mm
External creepage	*CPG*	> 8	mm
Comparative tracking index	*CTI*	> 400	–
Isolation capacitance	C_{IO}	1.7	pF
Reinforced insulation according to IEC 60747-17 (planned)			
Installation classification per IEC 60664-1, Table F.1 for rated mains voltage ≤ 150 V (rms) for rated mains voltage ≤ 300 V (rms) for rated mains voltage ≤ 600 V (rms) for rated mains voltage ≤1000 V (rms)		 I-IV I-IV I-III I-II	–
Climatic classification		40/125/21	–
Pollution degree (IEC 60664-1)		2	–
Apparent charge, method a $V_{pd(ini),a} = V_{IOTM}$, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_{ini} = 1 min, t_m = 10 s	q_{pd}	< 5	pC
Apparent charge, method b $V_{pd(ini),b} = V_{IOTM} \times 1.2$, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_{ini} = 1 s, t_m = 1 s	q_{pd}	< 5	pC
Isolation resistance at $T_{A,max}$; V_{IO} = 500 V_{DC}, T_A = 125°C	R_{IO}	> 10^{11}	Ω
Isolation resistance at T_S; V_{IO} = 500 V_{DC}, T_S = 150°C	R_{IO_S}	> 10^9	Ω
Maximum rated transient isolation voltage	V_{IOTM}	8000	V (peak)
Maximum repetitive isolation voltage	V_{IORM}	1767	V (peak)
Maximum working isolation voltage	V_{IOWM}	1250	V (rms)
Impulse voltage	V_{IMP}	8000	V (peak)
Maximum surge isolation voltage for reinforced isolation; $V_{TEST} \geq V_{IMP} \times 1.3$	V_{IOSM}	11000	V (peak)
Recognized under UL 1577 (planned)			
Insulation withstand voltage (60 s)	V_{ISO}	5700	V (rms)
Insulation test voltage (1 s)	$V_{ISO,TEST}$	6840	V (rms)

1) IC total power dissipation is derated linearly with 11.9 mW/K above 25°C; With R_{thJA} according to JESD 51-7 standard, 2s2p and a metallization of 70 / 35 / 35 / 70 µm

2) IC total power dissipation is derated linearly with 11.9 mW/K above 25°C; With R_{thJA} according to JESD 51-7 standard, 2s2p and a metallization of 70 / 35 / 35 / 70 µm

6 Package outline



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 14 PG-DSO-16 - 300 mil 16-pin fine pitch package

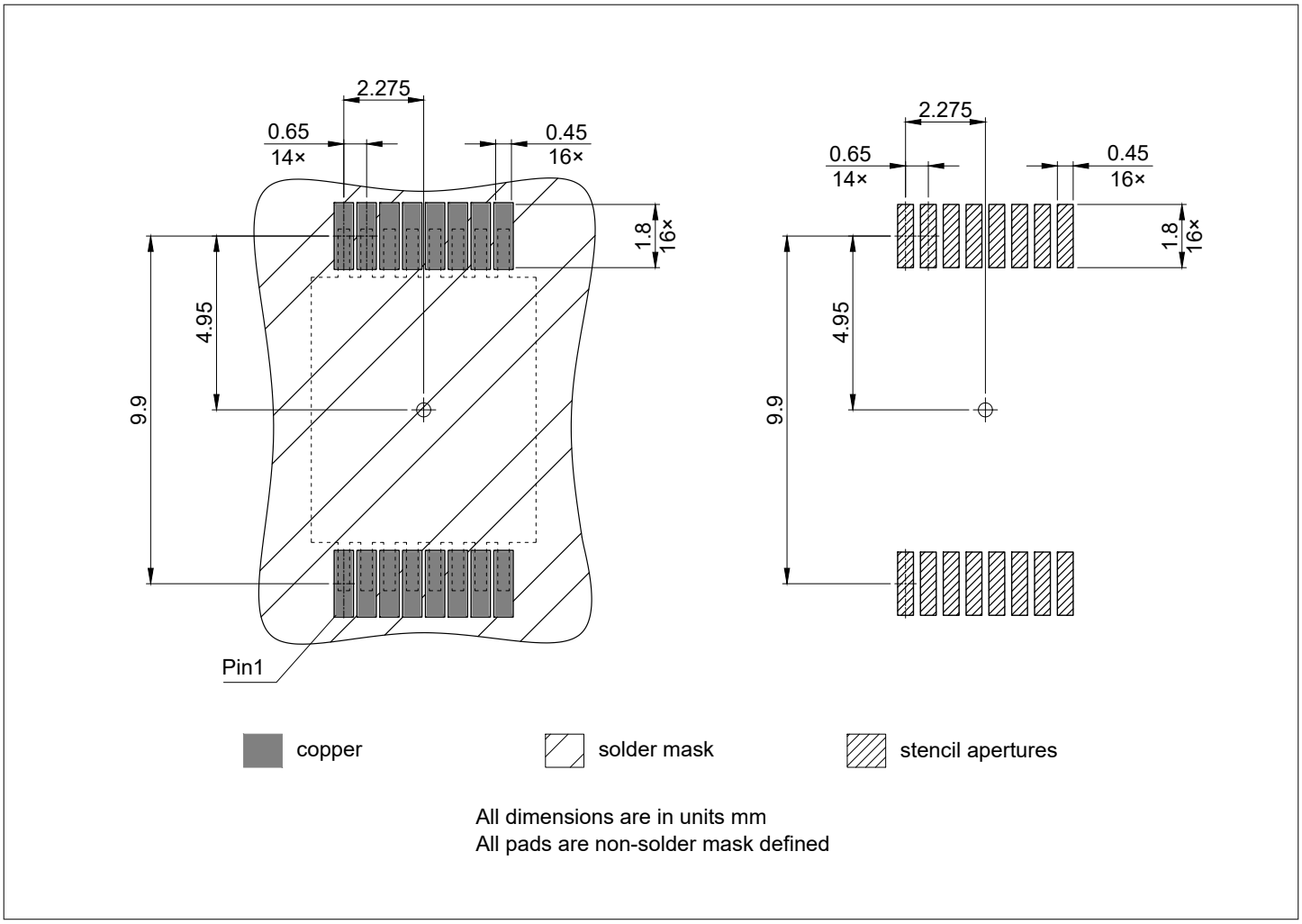


Figure 15 Footprint

Revision history

Document version	Date of release	Description of changes
v1.00	2025-07-11	Update for final block diagram and electrical characteristics; editorial changes
v0.50	2025-02-18	First public version

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