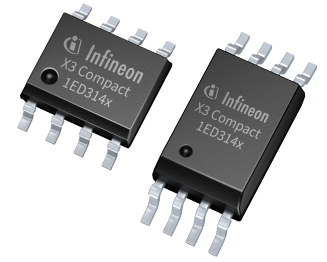


Single-channel isolated gate driver IC

Features

- Single-channel galvanically isolated coreless transformer based gate driver
- Separate outputs, output UVLO referenced to GND2 or adjustable output UVLO options
- For use with 600 V/650 V/1200 V/1700 V/2300 V IGBTs, Si and SiC MOSFETs
- Up to 6.5 A typical peak output current
- Pure-PMOS sourcing stage for optimal turn-on efficiency
- 40 ns propagation delay with 7 ns part-to-part matching (skew)
- 35 V absolute maximum output supply voltage
- Very high (best-in-class) common-mode transient immunity CMTI > 300 kV/μs
- Active shutdown and short circuit clamping
- 150 mil DSO-8 and 300 mil LDSO-8 packages with CTI > 600
- 3.3 V and 5 V input supply voltage
- Suitable for operation at high ambient temperature and in fast switching applications
- UL 1577 certification $V_{ISO} = 3.0$ kV (rms) for 1 min (File E311313) for 1ED314xMU12F
- UL 1577 certification $V_{ISO} = 5.7$ kV (rms) for 1 min (File E311313), and IEC 60747-17 ($V_{IORM} = 1767$ V) (Certificate no. 40055138) for 1ED314xMC12H



Potential applications

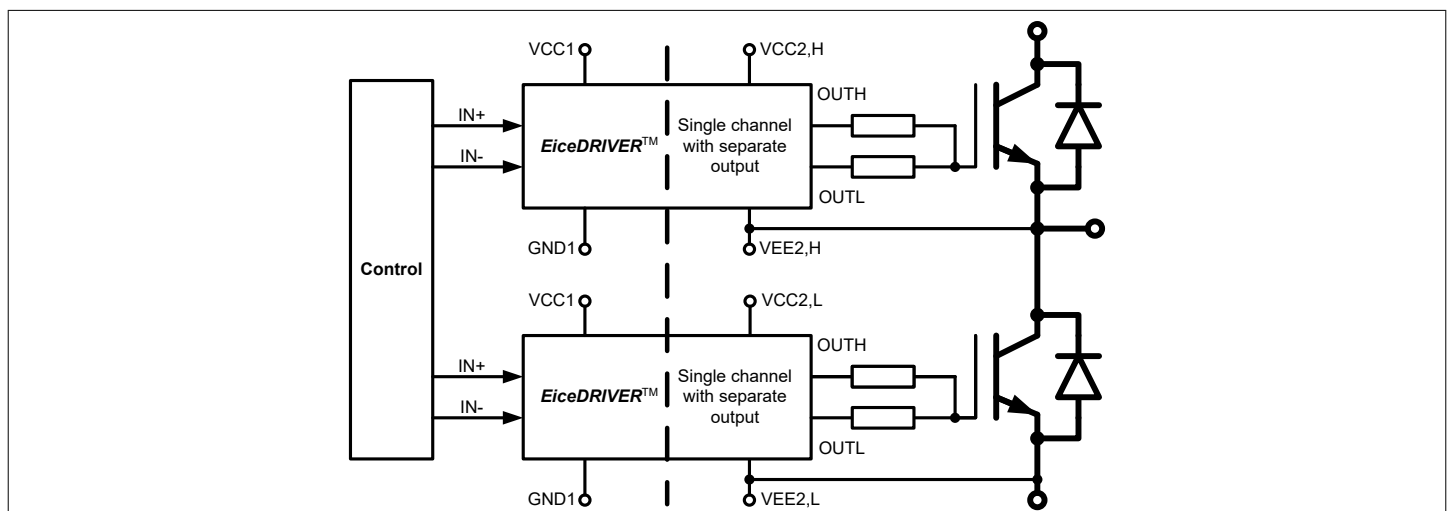
- EV charging
- UPS and energy storage systems
- Solar inverters
- Server and telecom switched mode power supplies (SMPS)
- AC and brushless DC motor drives
- Commercial heating, ventilation and air conditioning (HVAC) systems

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The EiceDRIVER™ 1ED314xMx12x gate driver ICs are high-performance galvanically isolated single-channel gate drivers designed for driving IGBTs, MOSFETs and SiC MOSFETs. The gate driver ICs are available in a 150-mil, 8-pin package (1ED314xMU12F) and a 300-mil, 8-pin package (1ED314xMC12H). They provide a typical output current of up to 6.5 A. The input logic pins operate on a wide input voltage range of 3 V to 6.5 V using CMOS threshold levels to support 3.3 V microcontrollers. Data transfer across the isolation barrier is realized by the coreless transformer technology. All variants have input and output undervoltage lockout (UVLO) and active shutdown.



Typical application diagram for variants with separate sink and source terminals

Description

Table 1 Ordering information for the 150-mil package

Product type	Typical UVLO (V_{UVLOL2}/V_{UVLOH2})	Typical output current source/sink	Output configuration	UL 1577 Certification	Package marking
1ED3140MU12F	8.5 V / 9.3 V	6 A / 6.5 A	Separate outputs	E311313	3140MU12
1ED3141MU12F	11.0 V / 12.0 V	6 A / 6.5 A	Separate outputs	E311313	3141MU12
1ED3142MU12F	12.5 V / 13.6 V	6 A / 6.5 A	Separate outputs	E311313	3142MU12

Table 2 Ordering information for the 300-mil package

Product type	Typical UVLO (V_{UVLOL2}/V_{UVLOH2})	Typical output current source/sink	Output configuration	UL 1577 Certification	IEC 60747-17 Certification	Package marking
1ED3141MC12H	11.0 V / 12.0 V	6 A / 6.5 A	Separate outputs	E311313	40055138	3141MC12
1ED3142MC12H	12.5 V / 13.6 V	6 A / 6.5 A	Separate outputs	E311313	40055138	3142MC12
1ED3143MC12H	11.0 V / 12.0 V	6 A / 6.5 A	UVLO referenced to <i>GND2</i>	E311313	40055138	3143MC12
1ED3144MC12H	12.5 V / 13.6 V	6 A / 6.5 A	UVLO referenced to <i>GND2</i>	E311313	40055138	3144MC12
1ED3145MC12H	Adjustable	6 A / 6.5 A	Adjustable UVLO	E311313	40055138	3145MC12

Table 3 Related evaluation boards

Board name	Gate driver	Power transistor	Short description
EVAL-1ED3142MU12F-SIC	1ED3142MU12F	IMZA120R020M1H	Half-bridge board with 1ED3142MU12F gate drivers, paired with CoolSiC™ in PG-TO-247-4 package
EVAL-1ED3142MC12H-SIC	1ED3142MC12H	IMZA120R020M1H	Half-bridge board with 1ED3142MC12H gate drivers, paired with CoolSiC™ in PG-TO-247-4 package
EVAL-1ED3144MC12H-SIC	1ED3144MC12H	IMZA120R020M1H	Half-bridge board with 1ED3144MC12H gate drivers, paired with CoolSiC™ in PG-TO-247-4 package
EVAL-1ED3145MC12H-SIC	1ED3145MC12H	IMZA120R020M1H	Half bridge board with 1ED3145MC12H gate drivers, paired with CoolSiC™ in PG-TO-247-4 package

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1 Block diagram reference

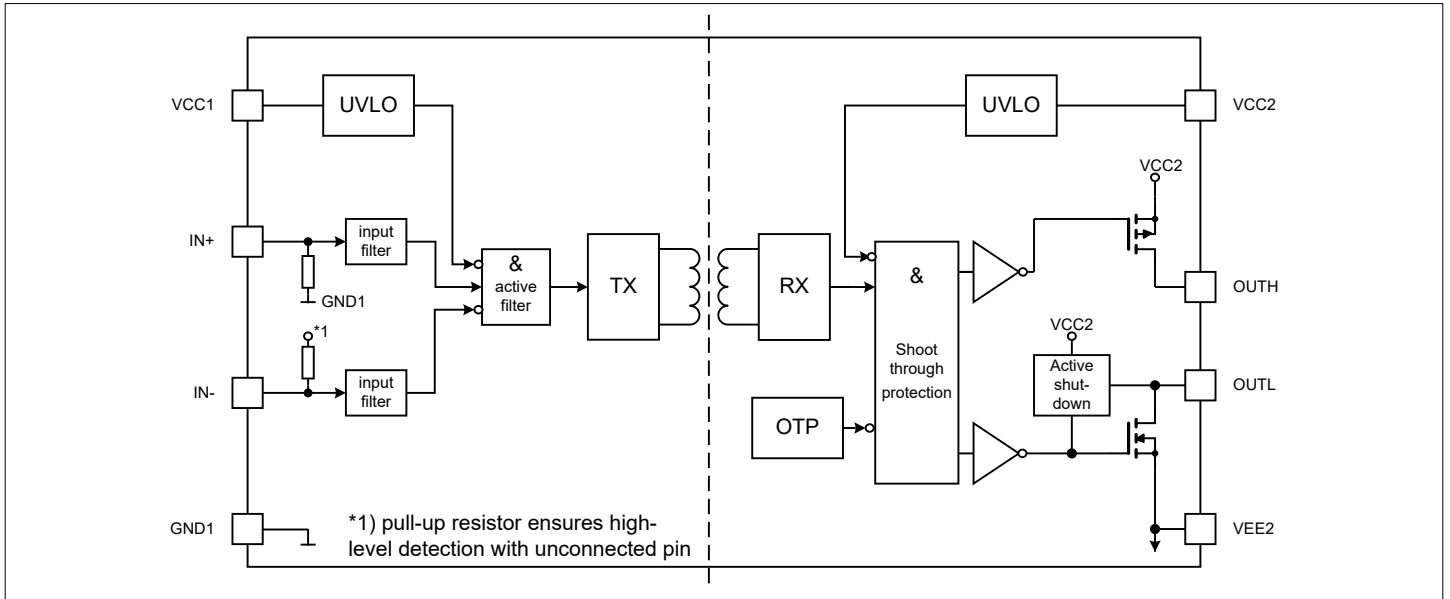


Figure 2 Block diagram for variants with separate sink and source pins (1ED3140, 1ED3141 and 1ED3142)

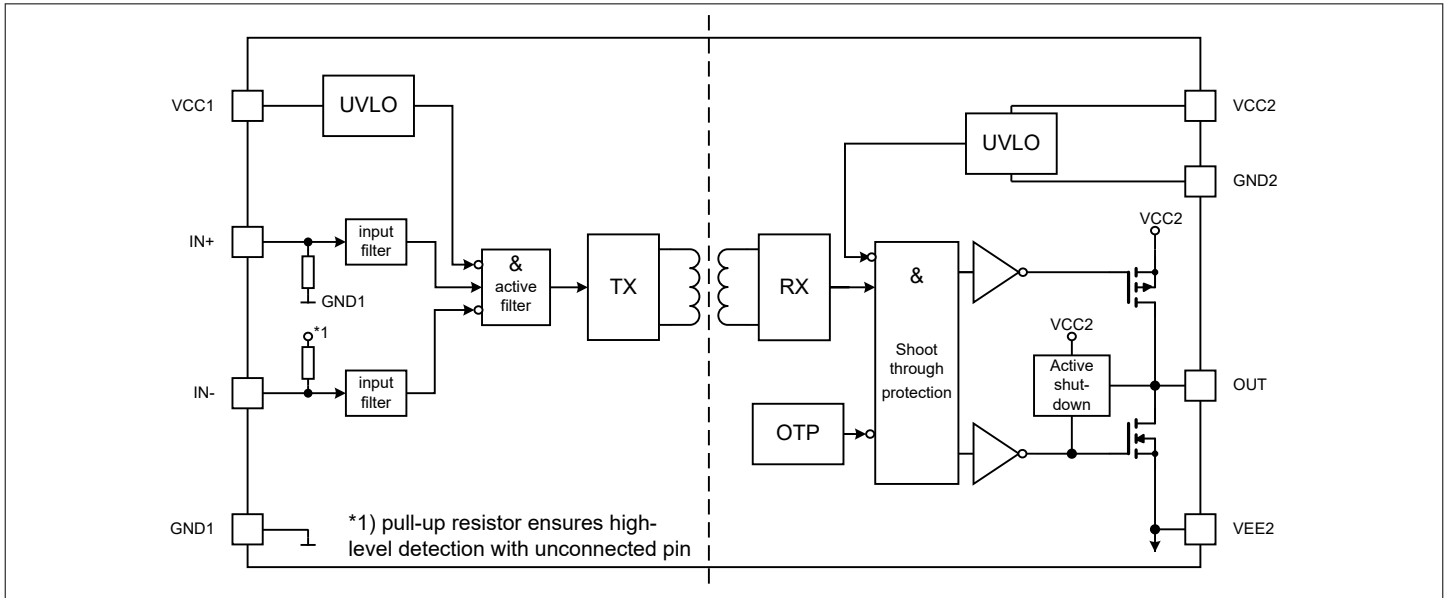


Figure 3 Block diagram for variants with GND2 pin (1ED3143 and 1ED3144)

1 Block diagram reference

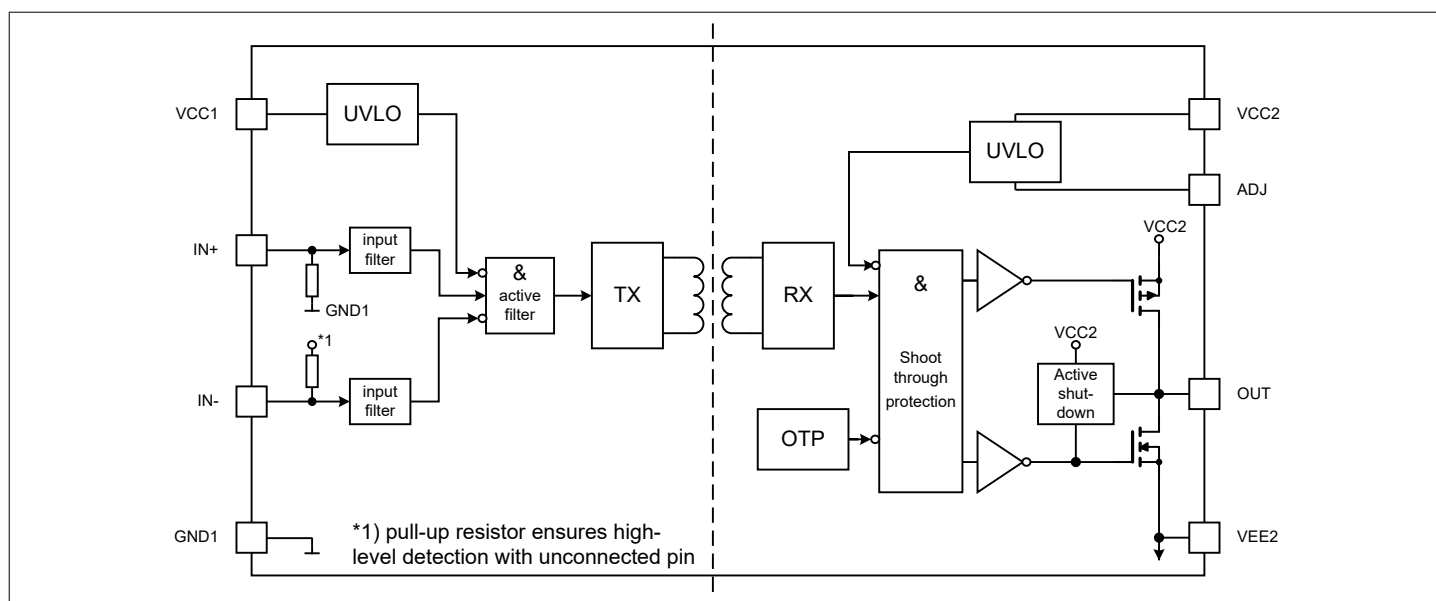


Figure 4 Block diagram for variants with ADJ pin (1ED3145)

2 Pin configuration and description

Table 4 Pin configuration for 1ED3140, 1ED3141 and 1ED3142

Pin No.	Name	Function
1	VCC1	Positive power supply input side
2	IN+	Non-inverted driver input (active high)
3	IN-	Inverted driver input (active low)
4	GND1	Input side ground
5	VCC2	Positive power supply output side
6	OUTH	Driver sourcing output
7	OUTL	Driver sinking output
8	VEE2	Output side ground

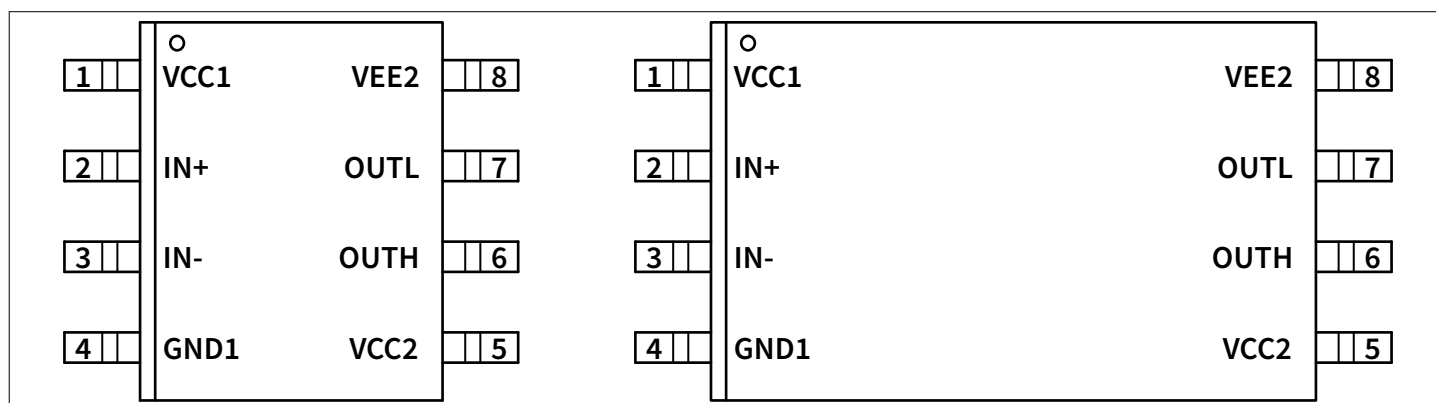


Figure 5 Pinout for 1ED3140, 1ED3141 and 1ED3142 (top view)

2 Pin configuration and description

Table 5 Pin configuration for 1ED3143 and 1ED3144

Pin No.	Name	Function
1	VCC1	Positive power supply input side
2	IN+	Non-inverted driver input (active high)
3	IN-	Inverted driver input (active low)
4	GND1	Input side ground
5	VCC2	Positive power supply output side
6	OUT	Driver sourcing and sinking output
7	GND2	Signal ground output side
8	VEE2	Negative power supply output side

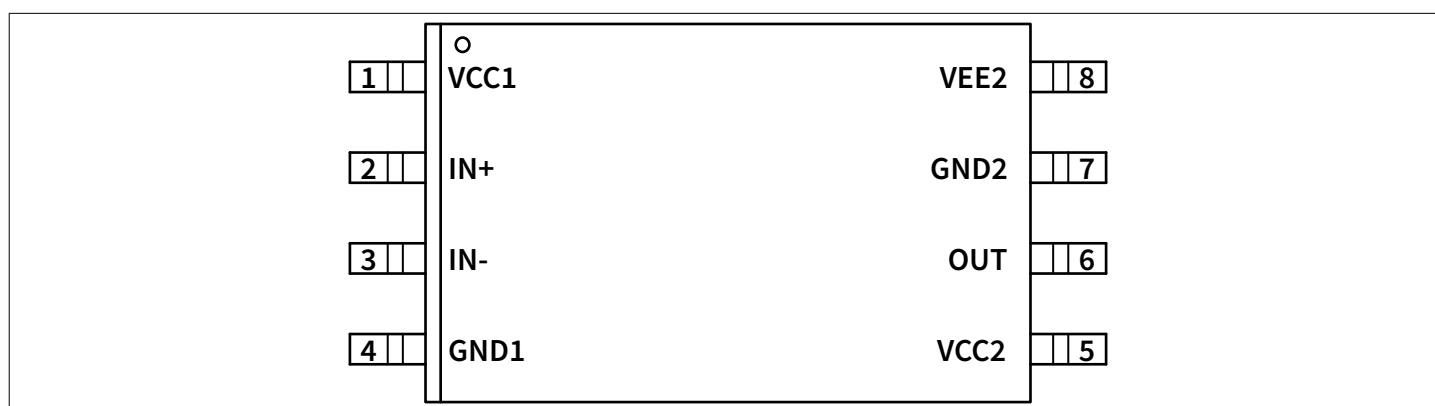


Figure 6 Pinout for 1ED3143 and 1ED3144 (top view)

2 Pin configuration and description

Table 6 Pin configuration for 1ED3145

Pin No.	Name	Function
1	VCC1	Positive power supply input side
2	IN+	Non-inverted driver input (active high)
3	IN-	Inverted driver input (active low)
4	GND1	Input side ground
5	VCC2	Positive power supply output side
6	OUT	Driver sourcing and sinking output
7	ADJ	Adjustable UVLO input
8	VEE2	Output side ground

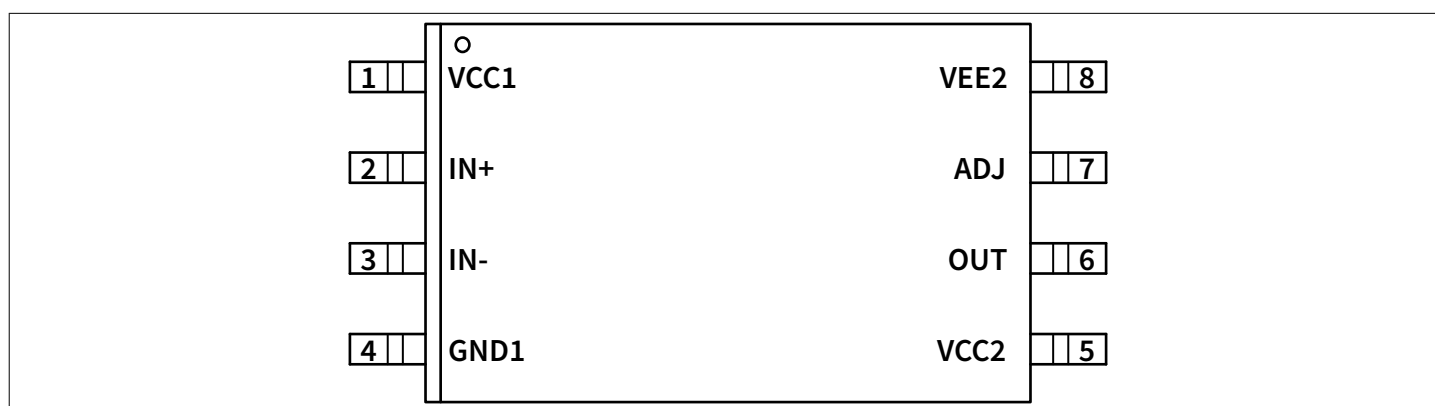


Figure 7 Pinout for 1ED3145 (top view)

Pin description

- **VCC1**: Input supply voltage. Connect to 3.3 V or 5 V and decouple with a capacitor to **GND1**. Use a low-ESR and low-ESL capacitor placed as close to the device as possible
- **GND1**: Input ground. All the input side signals, **VCC1**, **IN+** and **IN-** are referenced to this ground
- **IN+**: Non-inverted control signal for driver output. An internal filter provides robustness against noise at **IN+**. If left open, an internal, weak pull-down resistor pulls this pin to a low state, as shown in [Figure 2](#)
- **IN-**: Inverted control signal for driver output. An internal filter provides robustness against noise at **IN-**. If left open, an internal, weak pull-up resistor pulls this pin to a high state, as shown in [Figure 2](#)
- **VCC2**: Output positive power supply rail. Connect a decoupling capacitor from this pin to **VEE2**. Use a low-ESR and low-ESL capacitor placed as close to the device as possible
- **VEE2**: Output negative supply rail for gate drivers with **GND2** pin and output ground for gate drivers without **GND2** pin. In case of a bipolar supply (positive and negative voltage referred to IGBT emitter or MOSFET source), this pin should be connected to the negative supply voltage
- **OUTH**: Driver sourcing output pin used to charge the gate of the external transistor (IGBT or MOSFET). During the ON-state, this output is connected to **VCC2**. This output is controlled by **IN+** and **IN-** and is turned off by an UVLO event
- **OUTL**: Driver sinking output pin used to discharge the gate of the external transistor (IGBT or MOSFET). During the OFF-state, this output is connected to **VEE2**. This output is controlled by **IN+** and **IN-**. In case of an UVLO event, **OUTL** is actively pulled low. If the gate driver output is not supplied, the active shutdown circuit keeps the output voltage at a low level
- **OUT**: Combined driver sourcing and sinking output pin used to charge and discharge the gate of the external transistor (IGBT or MOSFET). During the ON-state, this output is connected to **VCC2** and during the OFF-state this output is connected to **VEE2**. The output is controlled by **IN+** and **IN-**. In case of an UVLO event, this output is turned off and the active shut down keeps the output voltage at a low level

2 Pin configuration and description

- *GND2*: Reference for the output side positive and negative power supply voltages. This pin is connected to the IGBT emitter or the MOSFET source. *GND2* is the reference for the output side UVLO levels
- *ADJ*: UVLO threshold levels adjustment on the output side. The resistor voltage divider between *VCC2* and gate drive common ground (IGBT emitter or MOSFET source) is connected to this pin to set the UVLO levels

3 Electrical characteristics and parameters

3.1 Absolute maximum ratings

Table 7 Absolute maximum ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Operating the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device reliability may be affected by exposure to absolute-maximum-rated conditions for extended periods of time.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power supply input side voltage	V_{VCC1}	-0.3		17	V	$V_{VCC1} - V_{GND1}$
Power supply output side voltage	V_{VCC2}	-0.3		35	V	$V_{VCC2} - V_{VEE2}$
Positive power supply output side voltage	V_{VCC2}	-0.3		35	V	$V_{VCC2} - V_{GND2}$, valid only for 1ED3143 and 1ED3144
Negative power supply output side voltage	V_{VEE2}	-35		0.3	V	$V_{VEE2} - V_{GND2}$, valid only for 1ED3143 and 1ED3144
Gate driver output voltage	V_{OUT}	$V_{VEE2} - 0.3$		$V_{VCC2} + 0.3$	V	valid only for 1ED3143, 1ED3144 and 1ED3145
Gate driver source output voltage	V_{OUTH}	$V_{VCC2} - 35$		$V_{VCC2} + 0.3$	V	valid only for 1ED3140, 1ED3141 and 1ED3142
Gate driver sink output voltage	V_{OUTL}	$V_{VEE2} - 0.3$		$V_{VEE2} + 35$	V	valid only for 1ED3140, 1ED3141 and 1ED3142
Logic input voltages (IN+, IN-)	V_{IN}	-0.3		6.5	V	
Dynamic logic input voltages (IN+, IN-)	V_{INDYN}	-5		15	V	¹⁾ $t_{IN} < 100$ ns, $d < 0.01$
Adjustable UVLO input	V_{ADJ}	$V_{VCC2} + 0.3$		$V_{VCC2} - 6$	V	valid only for 1ED3145
Input to output offset voltage	V_{OFFSET}			2300	V	²⁾ $V_{OFFSET} = V_{VEE2} - V_{GND1} $
ESD robustness - human body model	$ V_{ESD,HBM} $			4	kV	³⁾
ESD robustness - charged device model	ESD,CDM			TC1500		⁴⁾
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{Stg}	-55		150	°C	

PG-DSO-8-72 (150-mil)

Power dissipation (input side)	$P_{D,IN}$			100	mW	⁵⁾ $T_A = 85$ °C
Power dissipation (output side)	$P_{D,OUT}$			500	mW	⁶⁾ $T_A = 85$ °C
Thermal resistance junction to ambient	$R_{THJA,OUT}$			129	K/W	$T_A = 85$ °C, 2s2p - no vias, $P_J = 500$ mW
Characterization parameter junction to package top	Ψ_{Jtop}			6.1	K/W	$T_A = 85$ °C, 2s2p - no vias, $P_J = 500$ mW

(table continues...)

3 Electrical characteristics and parameters

Table 7 (continued) Absolute maximum ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only. Operating the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device reliability may be affected by exposure to absolute-maximum-rated conditions for extended periods of time.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
PG-LDSO-8-1 [300-mil]						
Power dissipation (input side)	$P_{D,IN}$			100	mW	7) $T_A = 85\text{ °C}$
Power dissipation (output side)	$P_{D,OUT}$			550	mW	8) $T_A = 85\text{ °C}$
Thermal resistance junction to ambient	$R_{thJA,OUT}$			113	K/W	$T_A = 85\text{ °C}$, 2s2p - no vias, $P_J = 550\text{ mW}$
Characterization parameter junction to package top	Ψ_{Jtop}			5.7	K/W	$T_A = 85\text{ °C}$, 2s2p - no vias, $P_J = 550\text{ mW}$

- 1) Parameter is not subject to production test - verified by design/characterization
- 2) For functional operation only
- 3) According to ANSI/ESDA/JEDEC-JS-001-2017 (discharging a 100 pF capacitor through a 1.5 kΩ series resistor).
- 4) According to ANSI/ESDA/JEDEC-JS-002-2014 (TC = test condition in volt)
- 5) IC input-side power dissipation is derated linearly with 7.75 mW/°C above 137.1 °C
- 6) IC output-side power dissipation is derated linearly with 7.75 mW/°C above 85 °C
- 7) IC input-side power dissipation is derated linearly with 8.85 mW/°C above 138.7 °C
- 8) IC output-side power dissipation is derated linearly with 8.85 mW/°C above 87.8 °C

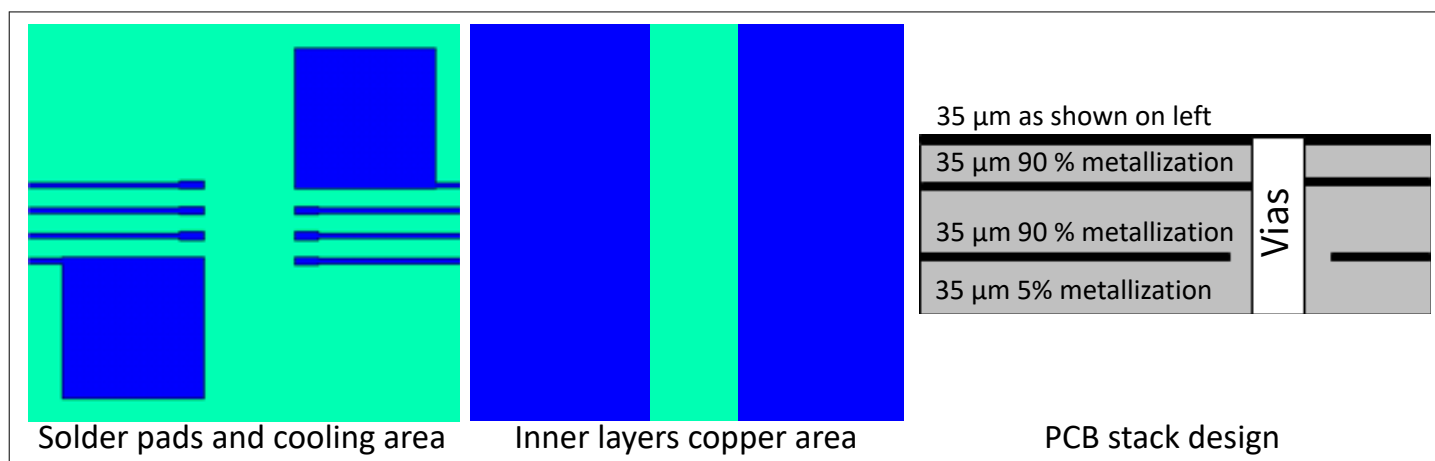


Figure 8 Reference layout for thermal data

This PCB layout represents the reference layout used for the thermal characterization of the 150 mil package.

3.2 Recommended operating conditions

Table 8 Recommended operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power supply input side voltage	V_{VCC1}	3.0		15	V	$V_{VCC1} - V_{GND1}$

(table continues...)

Table 8 (continued) Recommended operating conditions

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Power supply output side voltage	V_{VCC2}	9.6		32	V	$V_{VCC2} - V_{VEE2}$, 1ED3140
Power supply output side voltage	V_{VCC2}	12.35		32	V	$V_{VCC2} - V_{VEE2}$, 1ED3141
Power supply output side voltage	V_{VCC2}	14		32	V	$V_{VCC2} - V_{VEE2}$, 1ED3142
Power supply output side voltage	V_{VCC2}	4.35		32	V	$V_{VCC2} - V_{VEE2}$, 1ED3145
Positive power supply output side voltage	V_{VCC2}	12.35		32	V	$V_{VCC2} - V_{GND2}$, 1ED3143
Positive power supply output side voltage	V_{VCC2}	14		32	V	$V_{VCC2} - V_{GND2}$, 1ED3144
Negative power supply output side voltage	V_{VEE2}	-16		0	V	$V_{VEE2} - V_{GND2}$, 1ED3143 and 1ED3144
Logic input voltages (IN+, IN-)	V_{IN}	-0.3		5.5	V	
Ambient temperature	T_A	-40		125	°C	
Junction temperature	T_J	-40		150	°C	

3.3 Electrical characteristics

The electrical characteristics include the spread of values over supply voltages and temperatures within the recommended operating conditions. Electrical characteristics are tested in production at $T_A = 25\text{ °C}$. Typical values represent the median values measured at $V_{VCC1} = 3.3\text{ V}$, $V_{VCC2} - V_{VEE2} = 15\text{ V}$, and $T_A = 25\text{ °C}$. For 1ED3143 and 1ED3144 $V_{VEE2} - V_{GND2} = 0\text{ V}$. Minimum and maximum values in characteristics are verified by characterization/design. This is valid for all electrical characteristics unless specified otherwise.

3.3.1 Power supply

Table 9 Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
UVLO threshold input side (on)	V_{UVLOH1}		2.86	3.0	V	$V_{VCC1} - V_{GND1}$
UVLO threshold input side (off)	V_{UVLOL1}	2.5	2.66		V	$V_{VCC1} - V_{GND1}$
UVLO hysteresis input side	V_{HYS1}	0.1	0.2		V	$V_{UVLOH1} - V_{UVLOL1}$
Quiescent current input side	I_{Q1}			1.1	mA	IN+ = Low, IN- = Low
Quiescent current output side, ON state	$I_{Q2,ON}$			1.35	mA	IN+ = High, IN- = Low, $V_{VCC2} - V_{VEE2} = 15\text{ V}$
Quiescent current output side, OFF state	$I_{Q2,OFF}$			1.0	mA	IN+ = Low, IN- = High, $V_{VCC2} - V_{VEE2} = 15\text{ V}$

1ED3140

UVLO threshold output side (on)	V_{UVLOH2}		9.3	9.6	V	$V_{VCC2} - V_{VEE2}$
UVLO threshold output side (off)	V_{UVLOL2}	8.25	8.55		V	$V_{VCC2} - V_{VEE2}$
UVLO hysteresis output side	V_{HYS2}		0.75		V	$V_{UVLOH2} - V_{UVLOL2}$

(table continues...)

Table 9 (continued) Power supply

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
1ED3141						
UVLO threshold output side (on)	V_{UVLOH2}		12	12.35	V	$V_{VCC2} - V_{VEE2}$
UVLO threshold output side (off)	V_{UVLOL2}	10.7	11.05		V	$V_{VCC2} - V_{VEE2}$
UVLO hysteresis output side	V_{HYS2}		0.95		V	$V_{UVLOH2} - V_{UVLOL2}$
1ED3142						
UVLO threshold output side (on)	V_{UVLOH2}		13.6	14	V	$V_{VCC2} - V_{VEE2}$
UVLO threshold output side (off)	V_{UVLOL2}	12.15	12.55		V	$V_{VCC2} - V_{VEE2}$
UVLO hysteresis output side	V_{HYS2}		1.05		V	$V_{UVLOH2} - V_{UVLOL2}$
1ED3143						
UVLO threshold output side (on)	V_{UVLOH2}		12	12.35	V	$V_{VCC2} - V_{GND2}$
UVLO threshold output side (off)	V_{UVLOL2}	10.7	11.05		V	$V_{VCC2} - V_{GND2}$
UVLO hysteresis output side	V_{HYS2}		0.95		V	$V_{UVLOH2} - V_{UVLOL2}$
1ED3144						
UVLO threshold output side (on)	V_{UVLOH2}		13.6	14	V	$V_{VCC2} - V_{GND2}$
UVLO threshold output side (off)	V_{UVLOL2}	12.15	12.55		V	$V_{VCC2} - V_{GND2}$
UVLO hysteresis output side	V_{HYS2}		1.05		V	$V_{UVLOH2} - V_{UVLOL2}$
1ED3145						
Adjustable UVLO threshold output side (on)	$V_{ADJ,UVLOH2}$		2	2.07	V	$V_{VCC2} - V_{ADJ}$
Adjustable UVLO threshold output side (off)	$V_{ADJ,UVLOL2}$	1.78	1.84		V	$V_{VCC2} - V_{ADJ}$
Adjustable UVLO hysteresis output side	$V_{ADJ,HYS2}$		0.16		V	$V_{ADJ,UVLOH2} - V_{ADJ,UVLOL2}$
ADJ leakage current	$I_{Q,ADJ}$	2.4	3	3.6	μA	$V_{ADJ} = V_{VCC2} - 3\text{ V}$

3.3.2 Logic input

Table 10 Logic input

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
IN+, IN- low input threshold voltage	$V_{IN,L}$	1.1			V	
IN+, IN- high input threshold voltage	$V_{IN,H}$			2.5	V	
IN+, IN- low/high hysteresis	$V_{IN,HYS}$	0.5	0.8		V	
IN+, IN- input current	I_{IN}			100	μA	$V_{VCC1} = 5\text{ V}, V_{IN} \leq V_{VCC1}$
IN+ pull down resistor	$R_{IN,PD}$		75		k Ω	
IN- pull up resistor	$R_{IN,PU}$		75		k Ω	

3.3.3 Gate driver

Table 11 Gate driver

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High level output peak current	I_{OUTH}	3.5	6		A	¹⁾ $V_{VCC2} - V_{VEE2} = 15\text{ V}$, $IN+ = \text{High}$, $IN- = \text{Low}$, $C_L = 100\text{ nF}$
High level output on resistance	$R_{DSON,H}$	0.3	0.9	2.1	Ω	$I_{OUTH} = 0.1\text{ A}$
Low level output peak current	I_{OUTL}	3.5	6.5		A	¹⁾ $V_{VCC2} - V_{VEE2} = 15\text{ V}$, $IN+ = \text{Low}$, $IN- = \text{High}$, $C_L = 100\text{ nF}$
Low level output on resistance	$R_{DSON,L}$	0.2	0.5	1.1	Ω	$I_{OUTL} = 0.1\text{ A}$
Short circuit clamp voltage between OUT(H) and VCC2	V_{CLP_OUTH}			1.0	V	$V_{OUT(H)} - V_{VCC2}$, $I_{OUTH} = -500\text{ mA}$, $t < 10\text{ }\mu\text{s}$, $IN+ = \text{High}$, $IN- = \text{Low}$
Clamp voltage between VEE2 and OUT(L)	V_{CLP_OUTL}			1.0	V	$V_{VEE2} - V_{OUT(L)}$, $I_{OUTL} = -500\text{ mA}$, $t < 10\text{ }\mu\text{s}$, $IN+ = \text{Low}$, $IN- = \text{High}$

¹⁾ Parameter is not subject to production test - verified by design/characterization

3.3.4 Dynamic characteristics

Table 12 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input to output propagation delay ON	t_{PDON}	34	40	50	ns	$V_{VCC2} - V_{VEE2} = 15\text{ V}$, $C_L = 100\text{ pF}$, valid only for 1ED3140, 1ED3141, 1ED3143 and 1ED3145
Input to output propagation delay ON	t_{PDON}	34	40	50	ns	$V_{VCC2} - V_{VEE2} = 18\text{ V}$, $C_L = 100\text{ pF}$, valid only for 1ED3142 and 1ED3144
Input to output propagation delay OFF	t_{PDOFF}	34	40	50	ns	$V_{VCC2} - V_{VEE2} = 15\text{ V}$, $C_L = 100\text{ pF}$, valid only for 1ED3140, 1ED3141, 1ED3143 and 1ED3145
Input to output propagation delay OFF	t_{PDOFF}	34	40	50	ns	$V_{VCC2} - V_{VEE2} = 18\text{ V}$, $C_L = 100\text{ pF}$, valid only for 1ED3142 and 1ED3144
Input to output propagation delay distortion IN+	$ t_{PDISTO,IN+} $		0	3	ns	¹⁾ $ t_{PDOFF} - t_{PDON} $
Input to output propagation delay distortion IN-	$ t_{PDISTO,IN-} $		0	5	ns	¹⁾ $ t_{PDOFF} - t_{PDON} $
Input to output, part to part skew	t_{SKEW}			7	ns	¹⁾²⁾ $C_L = 100\text{ pF}$, valid for same input pin and edge
Input to output, part to part skew plus	t_{SKEW+}		0	8	ns	¹⁾ $C_L = 100\text{ pF}$, valid for opposite output edge and any input combination

(table continues...)

Table 12 (continued) Dynamic characteristics

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Input pulse suppression time (filter time)	t_{INFLT}	16			ns	shorter pulses will not propagate to the output
Minimum input pulse width	$t_{IN,min}$	27			ns	
Rise time	t_{RISE}			20	ns	$V_{VCC2} - V_{VEE2} = 15\text{ V}$, $C_L = 1\text{ nF}$, valid only for 1ED3140, 1ED3141 and 1ED3145
Rise time	t_{RISE}			20	ns	$V_{VCC2} - V_{VEE2} = 18\text{ V}$, $C_L = 1\text{ nF}$, valid only for 1ED3142 and 1ED3144
Fall time	t_{FALL}			20	ns	$V_{VCC2} - V_{VEE2} = 15\text{ V}$, $C_L = 1\text{ nF}$, valid only for 1ED3140, 1ED3141, 1ED3143 and 1ED3145
Fall time	t_{FALL}			20	ns	$V_{VCC2} - V_{VEE2} = 18\text{ V}$, $C_L = 1\text{ nF}$, valid only for 1ED3142 and 1ED3144
Input-side start-up time	$t_{START,VCC1}$		2.5	10	μs	³⁾ $IN+ = \text{High}$, $IN- = \text{Low}$, $V_{VCC2} > V_{UVLOH2}$, $C_L = 100\text{ pF}$
Input-side deactivation time	$t_{STOP,VCC1}$		2.5	10	μs	³⁾ $IN+ = \text{High}$, $IN- = \text{Low}$, $V_{VCC2} > V_{UVLOH2}$, $C_L = 100\text{ pF}$
Output-side start-up time	$t_{START,VCC2}$		5	10	μs	³⁾ $IN+ = \text{High}$, $IN- = \text{Low}$, $V_{VCC1} > V_{UVLOH1}$, $C_L = 100\text{ pF}$, valid for all products except 1ED3145
Output-side start-up time	$t_{START,VCC2}$		8	13	μs	³⁾ $IN+ = \text{High}$, $IN- = \text{Low}$, $V_{VCC1} > V_{UVLOH1}$, $C_L = 100\text{ pF}$, valid only for 1ED3145
Output-side deactivation time	$t_{STOP,VCC2}$	0.5		1.5	μs	³⁾ $IN+ = \text{High}$, $IN- = \text{Low}$, $V_{VCC1} > V_{UVLOH1}$, $C_L = 100\text{ pF}$, valid for all products except 1ED3145
Output-side deactivation time	$t_{STOP,VCC2}$	1.5		4	μs	³⁾ $IN+ = \text{High}$, $IN- = \text{Low}$, $V_{VCC1} > V_{UVLOH1}$, $C_L = 100\text{ pF}$, valid only for 1ED3145
High-level common-mode transient immunity	$ CM_H $	300			$\text{kV}/\mu\text{s}$	³⁾ $V_{CM} = 1500\text{ V}$; $IN-$ tied to $GND1$; $IN+$ tied to $VCC1$
Low-level common-mode transient immunity	$ CM_L $	300			$\text{kV}/\mu\text{s}$	³⁾ $V_{CM} = 1500\text{ V}$; $IN-$ tied to $VCC1$; $IN+$ tied to $GND1$

- 1) value at same ambient temperature and operating conditions.
- 2) this parameter was previously called input to output, part to part propagation delay variation
- 3) Parameter is not subject to production test - verified by design/characterization

3.3.5 Active shut down

Table 13 Active shut down

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Active shut down voltage	V_{ACTSD}			1.8	V	$V_{OUTL} - V_{VEE2}$, $I_{OUTL} = 500$ mA, $VCC2$ open, $OUTH$ connected to R_G
Active shut down voltage	V_{ACTSD}			1.8	V	$V_{OUT} - V_{VEE2}$, $I_{OUTL} = 500$ mA, $VCC2$ open

3.3.6 Overtemperature protection

Table 14 Overtemperature protection

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Overtemperature protection temperature	T_{OTPOFF}		165	175	°C	1)
Overtemperature protection hysteresis	T_{OTPHYS}		10		°C	1)

1) Parameter is not subject to production test - verified by design/characterization

4 Insulation characteristics (UL 1577) for PG-DSO-8 (150 mil) package

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 15 Insulation specification for PG-DSO-8 (150 mil) package

Description	Symbol	Characteristic	Unit
Safety limiting values			
Maximum ambient safety temperature	T_S	150	°C
Maximum input-side power dissipation at $T_A = 25^\circ\text{C}^{1)}$	P_{SI}	100	mW
Maximum output-side power dissipation at $T_A = 25^\circ\text{C}^{2)}$	P_{SO}	970	mW
Package specific insulation characteristics			
External clearance	CLR	> 4	mm
External creepage	CPG	> 4	mm
Comparative tracking index	CTI	> 600	–
Isolation capacitance	C_{IO}	1	pF
Overvoltage category per IEC 60664-1 Table F.1			
for rated mains voltage ≤ 150 V (rms)		I-IV	–
for rated mains voltage ≤ 300 V (rms)		I-III	
for rated mains voltage ≤ 600 V (rms)		I-II	
for rated mains voltage ≤ 1000 V (rms)		I	
Recognized under UL 1577			
Insulation withstand voltage (60 s)	V_{ISO}	3000	V (rms)
Insulation test voltage (1 s)	$V_{ISO,TEST}$	3600	V (rms)

1) IC input-side power dissipation is derated linearly at 7.75 mW/°C above 137.1 °C

2) IC output-side power dissipation is derated linearly at 7.75 mW/°C above 25 °C

5 Insulation characteristics (IEC 60747-17, UL 1577) for PG-LDSO-8 (300 mil) package

This coupler is suitable for rated insulation only within the given safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 16 Insulation specification for PG-LDSO-8 (300 mil) package

Description	Symbol	Characteristic	Unit
Safety limiting values			
Maximum ambient safety temperature	T_S	150	°C
Maximum input-side power dissipation at $T_A = 25^\circ\text{C}^{1)}$	P_{SI}	100	mW
Maximum output-side power dissipation at $T_A = 25^\circ\text{C}^{2)}$	P_{SO}	1006	mW
General			
External clearance	CLR	> 8	mm
External creepage	CPG	> 8	mm
Comparative tracking index	CTI	> 600	–
Isolation capacitance	C_{IO}	< 1	pF
Overvoltage category according to IEC 60664-1, Table F.1 for rated mains voltage ≤ 300 V (rms) for rated mains voltage ≤ 600 V (rms) for rated mains voltage ≤ 1000 V (rms)		I-IV I-IV I-III	–
Reinforced insulation according to IEC 60747-17 (Certificate no. 40055138)			
Climatic classification		40/125/21	–
Apparent charge, method a $V_{pd(ini),a} = V_{IOTM}$, $V_{pd(m)} = 1.6 \times V_{IORM}$, $t_{ini} = 1$ min, $t_m = 10$ s	q_{pd}	< 5	pC
Apparent charge, method b $V_{pd(ini),b} = V_{IOTM} \times 1.2$, $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_{ini} = 1$ s, $t_m = 1$ s	q_{pd}	< 5	pC
Isolation resistance at $T_{A,max}$; $V_{IO} = 500 V_{DC}$, $T_A = 125^\circ\text{C}$	R_{IO}	$> 10^{11}$	Ω
Isolation resistance at T_S ; $V_{IO} = 500 V_{DC}$, $T_S = 150^\circ\text{C}$	R_{IO_S}	$> 10^9$	Ω
Maximum rated transient isolation voltage	V_{IOTM}	8000	V (peak)
Maximum repetitive isolation voltage	V_{IORM}	1767	V (peak)
Maximum working isolation voltage	V_{IOWM}	1250	V (rms)
		1767	V (DC)
Impulse voltage	V_{IMP}	8000	V (peak)
Maximum surge isolation voltage for reinforced insulation; $V_{TEST} \geq V_{IMP} \times 1.3$	V_{IOSM}	11000	V (peak)
Recognized under UL 1577 (File E311313)			
Insulation withstand voltage (60 s)	V_{ISO}	5700	V (rms)
Insulation test voltage (1 s)	$V_{ISO,TEST}$	6840	V (rms)

1) IC input-side power dissipation is derated linearly at 8.85 mW/°C above 138.7 °C

2) IC output-side power dissipation is derated linearly at 8.05 mW/°C above 25 °C

6 Typical characteristics

Unless otherwise noted, the measurements are done with $V_{VCC1} = 3.3\text{ V}$, 100 nF capacitor connected between V_{CC1} and $GND1$, 4.7 μF capacitor between V_{CC2} and $VEE2$.

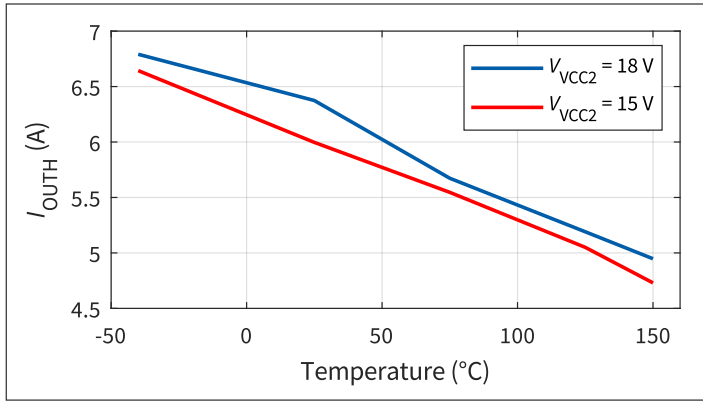


Figure 9 High level output peak current vs. temperature

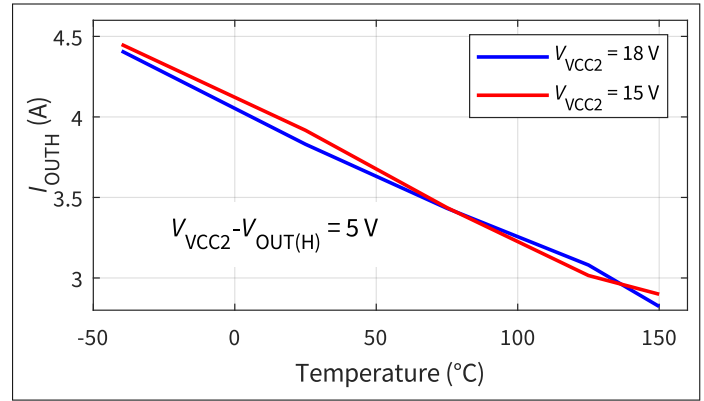


Figure 10 High level output current with $V_{VCC2} - V_{OUT(H)} = 5\text{ V}$ vs. temperature

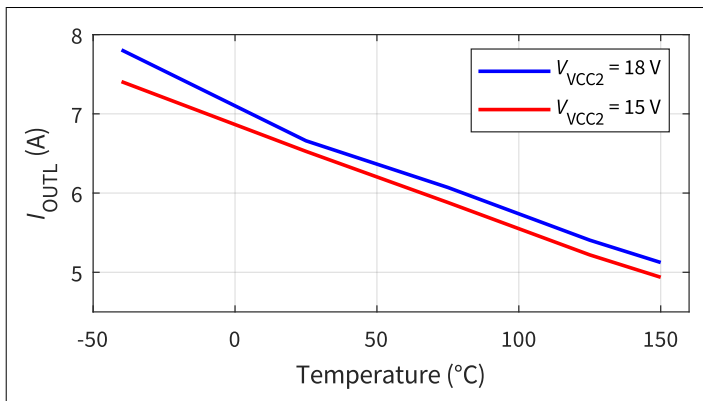


Figure 11 Low level output peak current vs. temperature

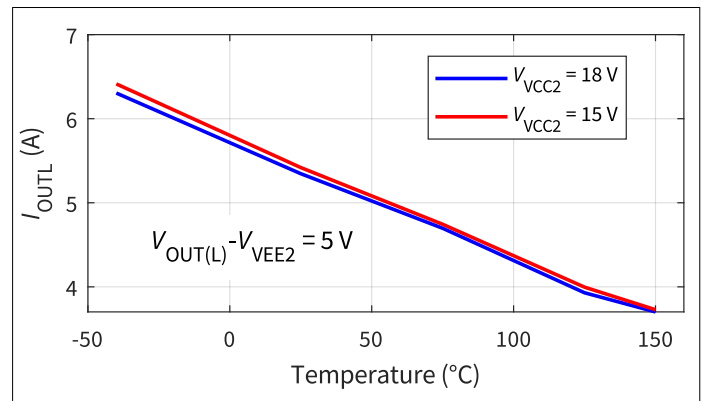


Figure 12 Low level output current with $V_{OUT(L)} - V_{VEE2} = 5\text{ V}$ vs. temperature

6 Typical characteristics

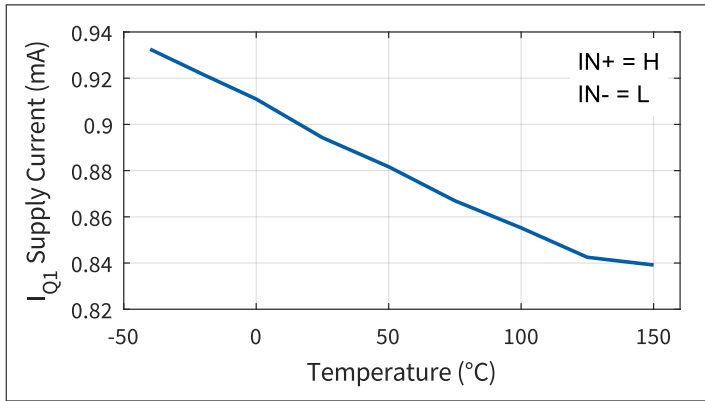


Figure 13 I_{Q1} supply current vs. temperature

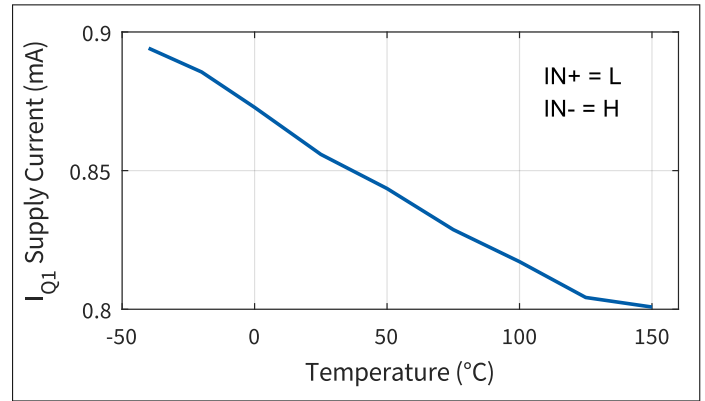


Figure 14 I_{Q1} supply current vs. temperature

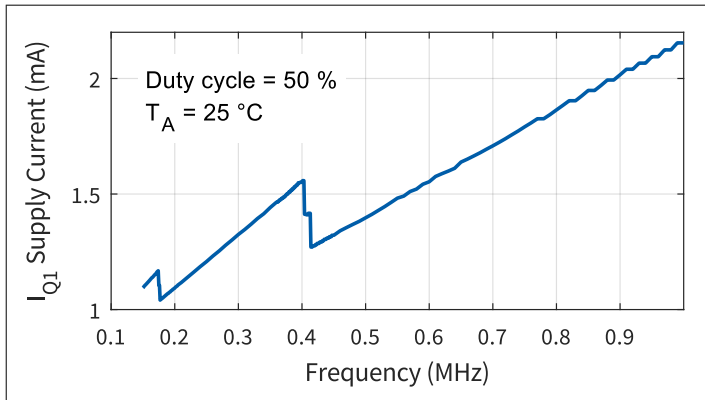


Figure 15 I_{Q1} supply current vs. input frequency

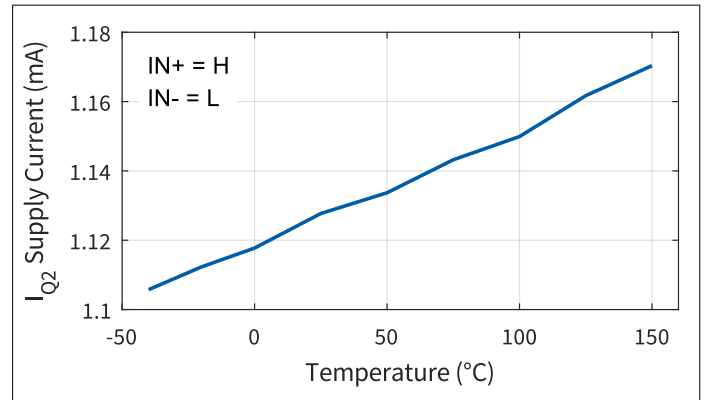


Figure 16 I_{Q2} supply current vs. temperature

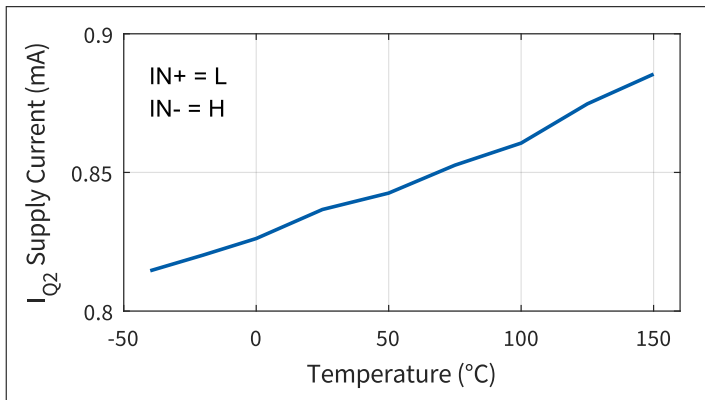


Figure 17 I_{Q2} supply current vs. temperature

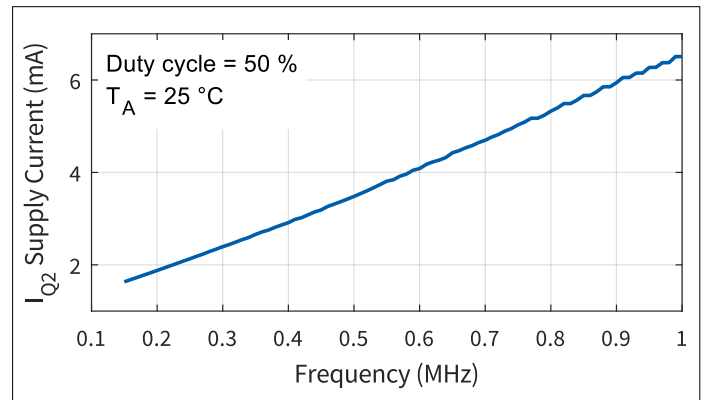


Figure 18 I_{Q2} supply current vs. input frequency

6 Typical characteristics

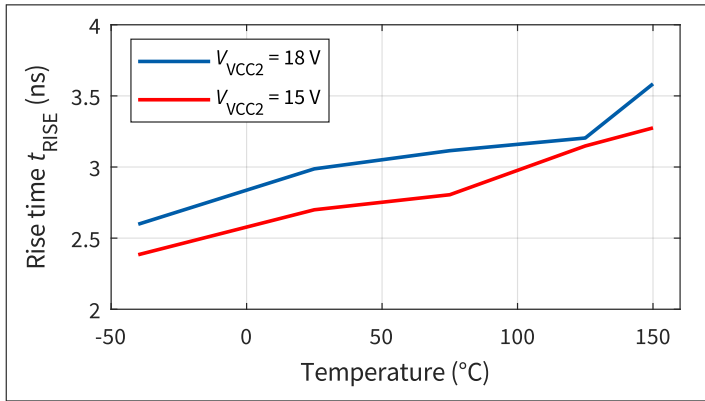


Figure 19 Rise time t_{RISE} vs. temperature

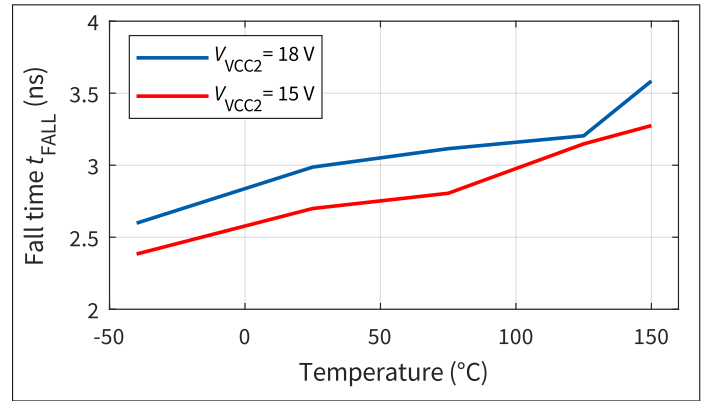


Figure 20 Fall time t_{FALL} vs. temperature

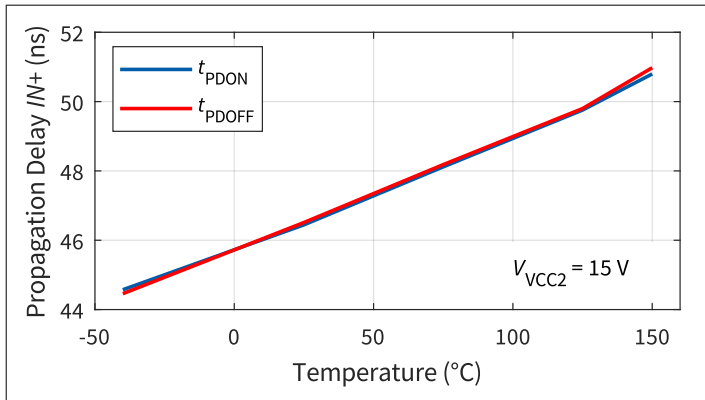


Figure 21 Propagation delay for $IN+$ vs. temperature ($V_{VCC2} = 15 V$)

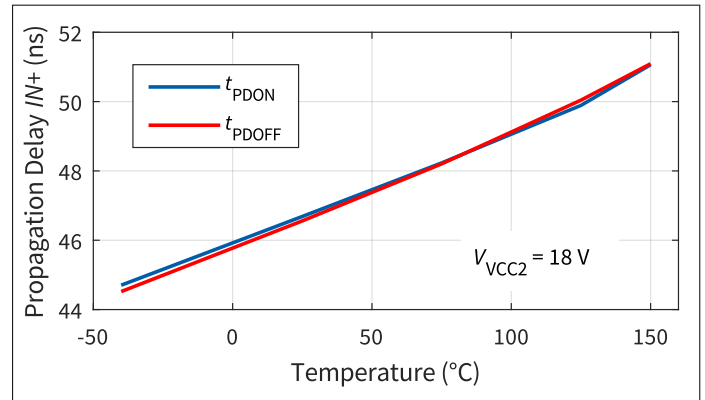


Figure 22 Propagation delay for $IN+$ vs. temperature ($V_{VCC2} = 18 V$)

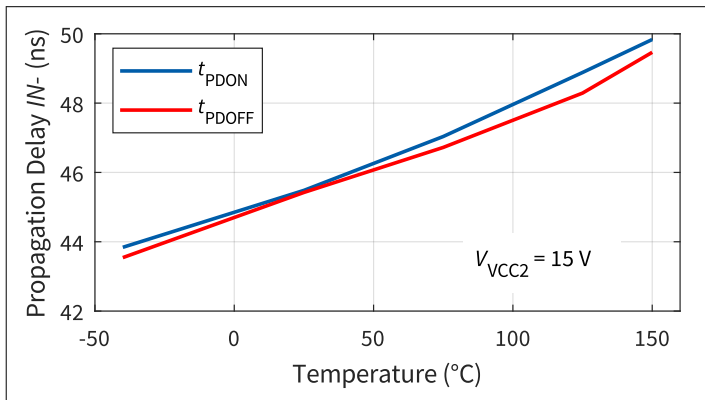


Figure 23 Propagation delay for $IN-$ vs. temperature ($V_{VCC2} = 15 V$)

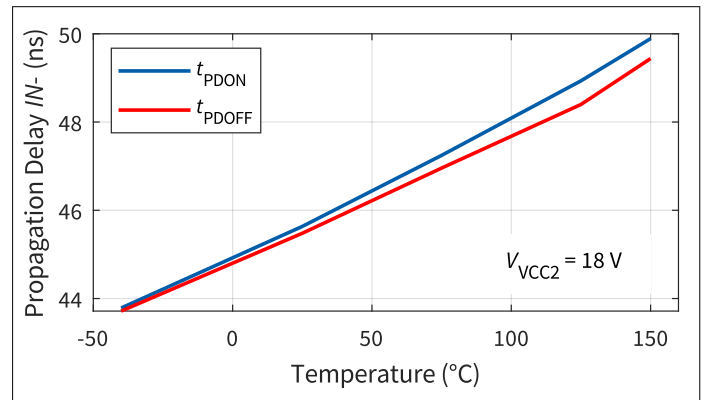


Figure 24 Propagation delay for $IN-$ vs. temperature ($V_{VCC2} = 18 V$)

6 Typical characteristics

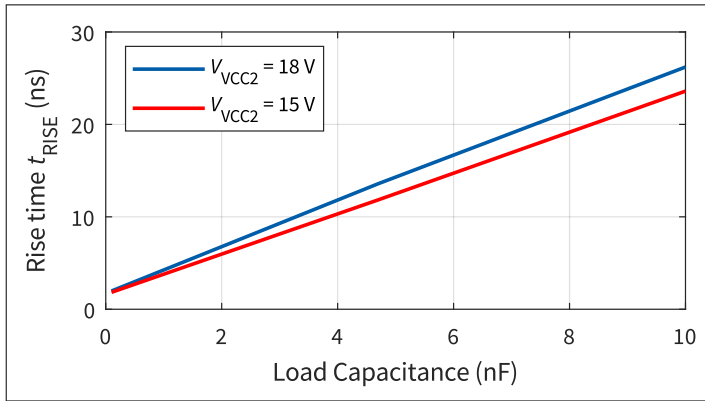


Figure 25 Rise time t_{RISE} vs. load capacitance

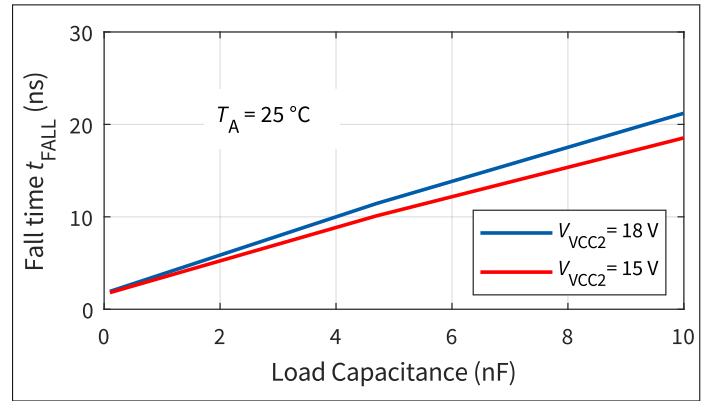


Figure 26 Fall time t_{FALL} vs. load capacitance

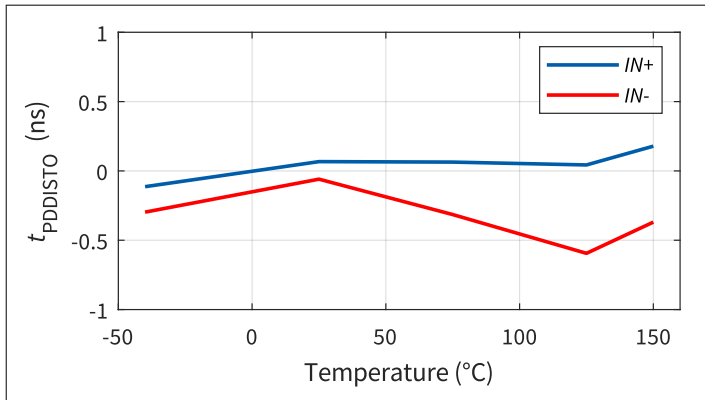


Figure 27 Propagation delay distortion t_{PDISTO} vs. temperature

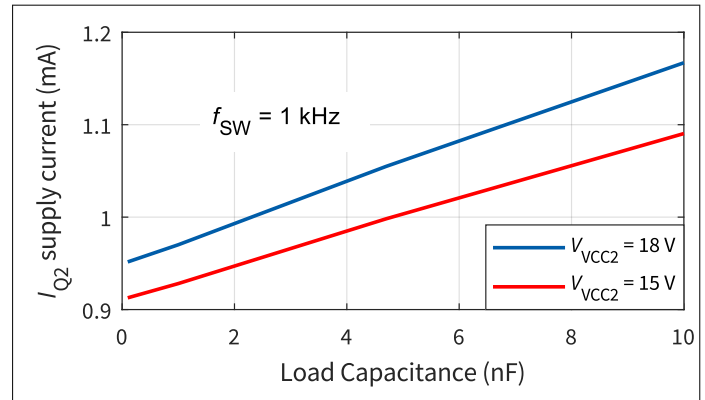


Figure 28 I_{Q2} supply current vs. load capacitance

7 Parameter measurement

7.1 CMTI measurement setup

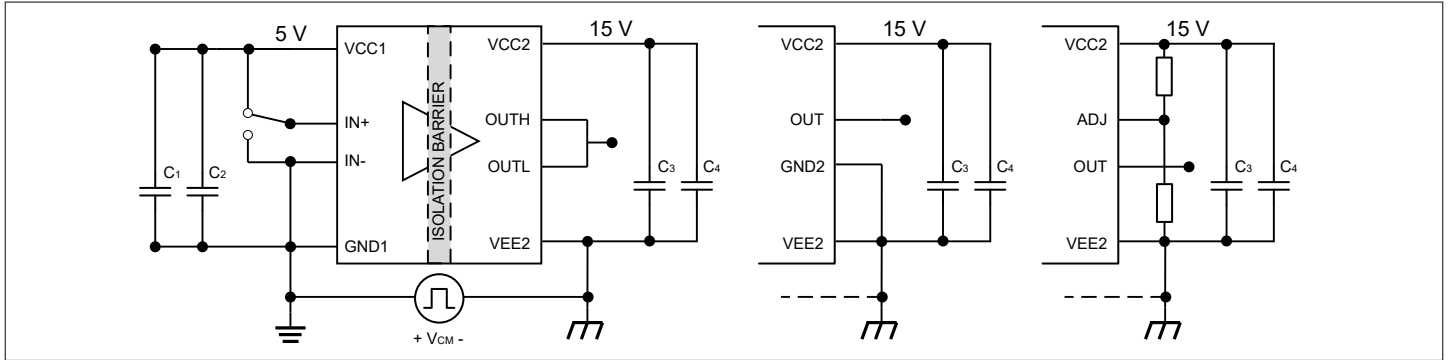


Figure 29 CMTI test circuits for all the variants

Figure 29 shows CMTI test setup for the common mode transient immunity measurements.

7.2 Undervoltage lockout (UVLO)

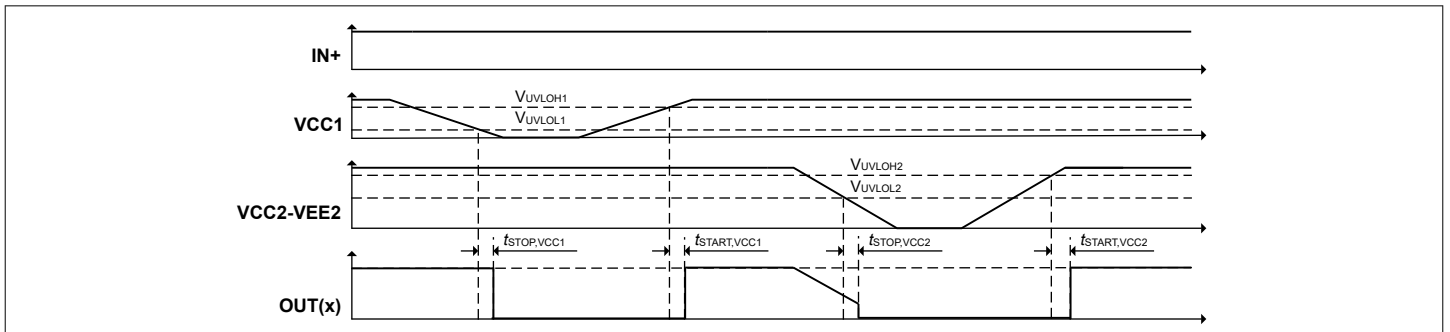


Figure 30 UVLO behavior of variants with separate source and sink pins

To ensure correct switching of IGBT, Si or SiC MOSFET, the device is equipped with an independent undervoltage lockout for both input and output side. Operation starts only after both supply voltage levels have increased beyond the respective V_{UVLOH} levels.

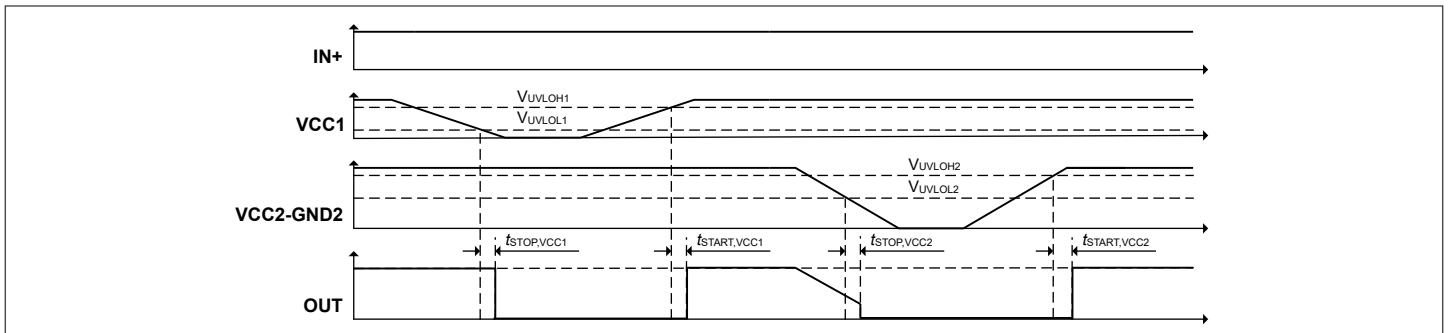


Figure 31 UVLO behavior of variants with GND2 pin

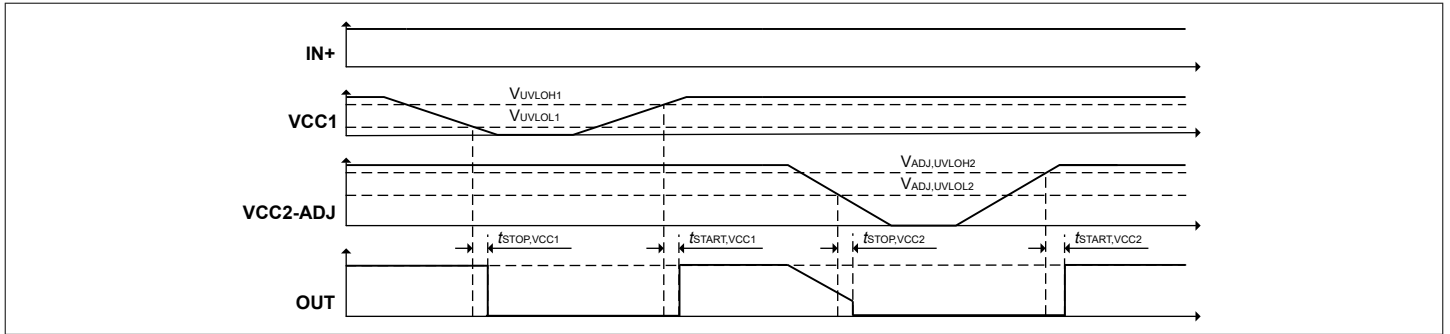


Figure 32 UVLO behavior of variants with ADJ pin

If the power supply voltage, V_{VCC1} , of the input chip drops below V_{UVLOL1} , a turn-off signal is sent to the output chip before power-down. The IGBT, Si or SiC MOSFET is switched off and the signals at $IN+$ and $IN-$ are ignored until V_{VCC1} reaches the power-up voltage, V_{UVLOH1} , again.

If the power supply voltage, V_{VCC2} , of the output chip goes down below V_{UVLOL2} , the IGBT, Si or SiC MOSFET is switched off and signals from the input chip are ignored until V_{VCC2} reaches the power-up voltage, V_{UVLOH2} , again.

7.3 Propagation delay, rise and fall time

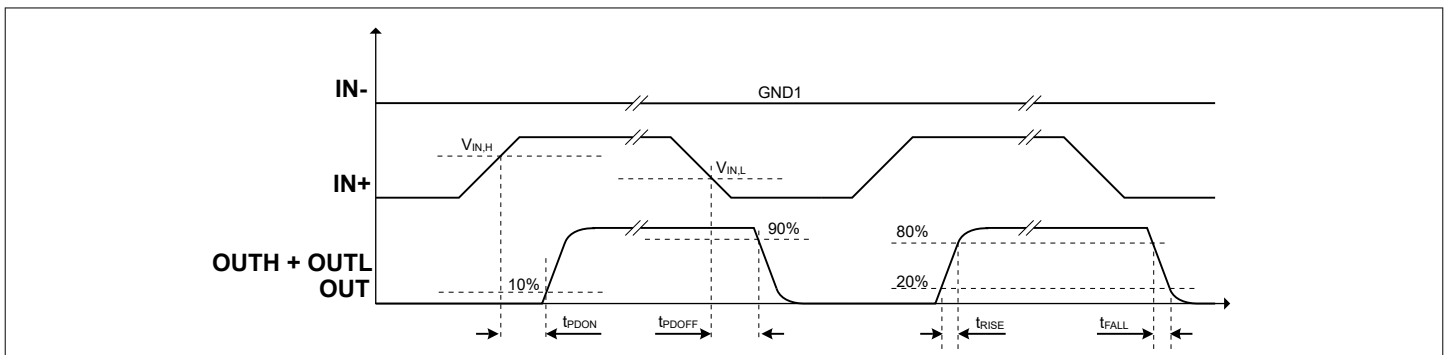


Figure 33 Propagation delay, rise time and fall time using the non-inverting input

Figure 33 and Figure 34 show the propagation delays t_{PDON} and t_{PDOff} for the non-inverting input $IN+$ and the inverting input $IN-$ including the rise time, t_{RISE} , and fall time, t_{FALL} , diagrams.

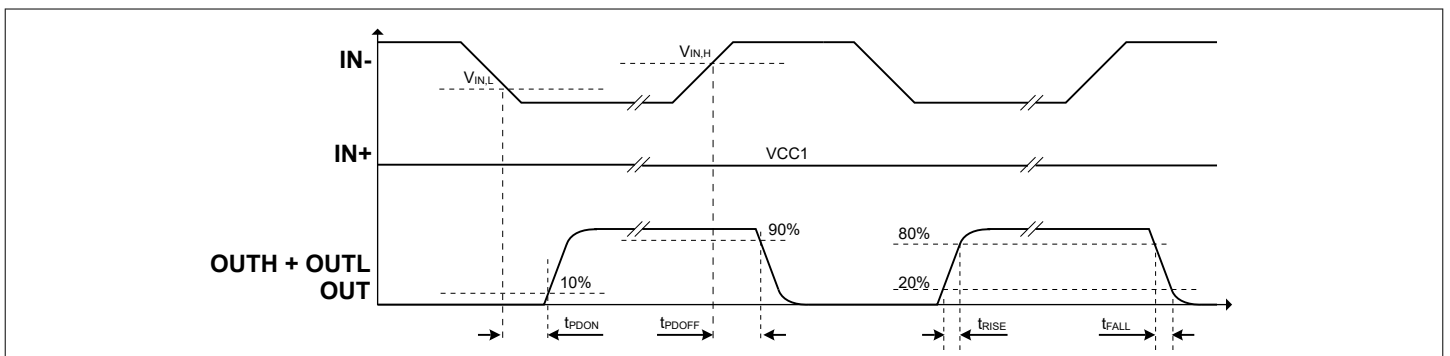


Figure 34 Propagation delay, rise time and fall time using the inverting input

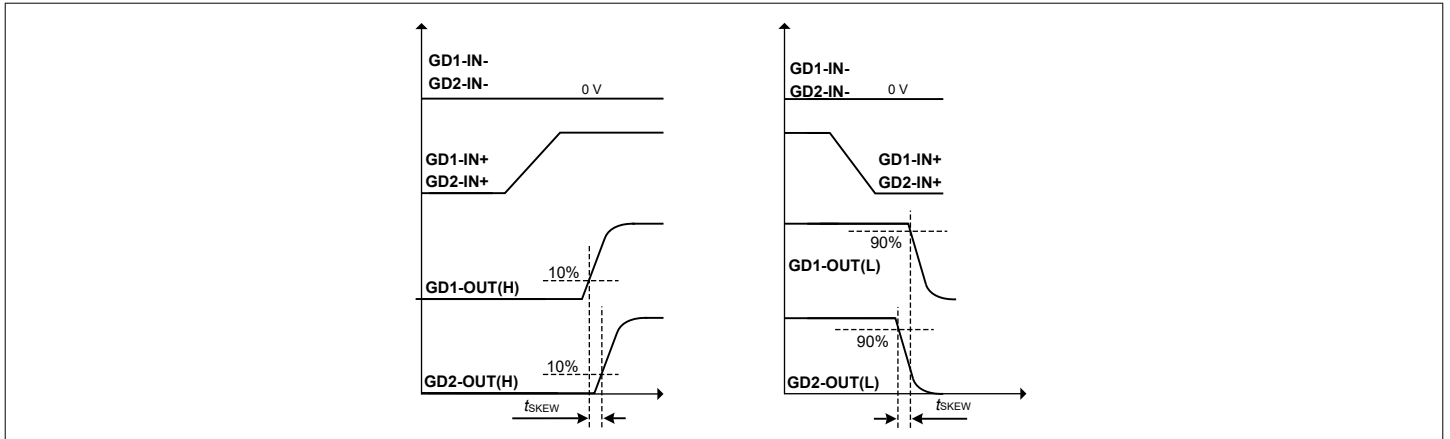


Figure 35 Input to output, part to part skew using non-inverting input

Figure 35 and Figure 36 show the input to output, part to part skew, t_{SKEW} measurement with the non-inverting and inverting inputs. This parameter highlights the part to part variation in propagation delay and is relevant when paralleling gate drivers. The parameter is always assuming the same conditions (temperature and supply voltages) between the parts.

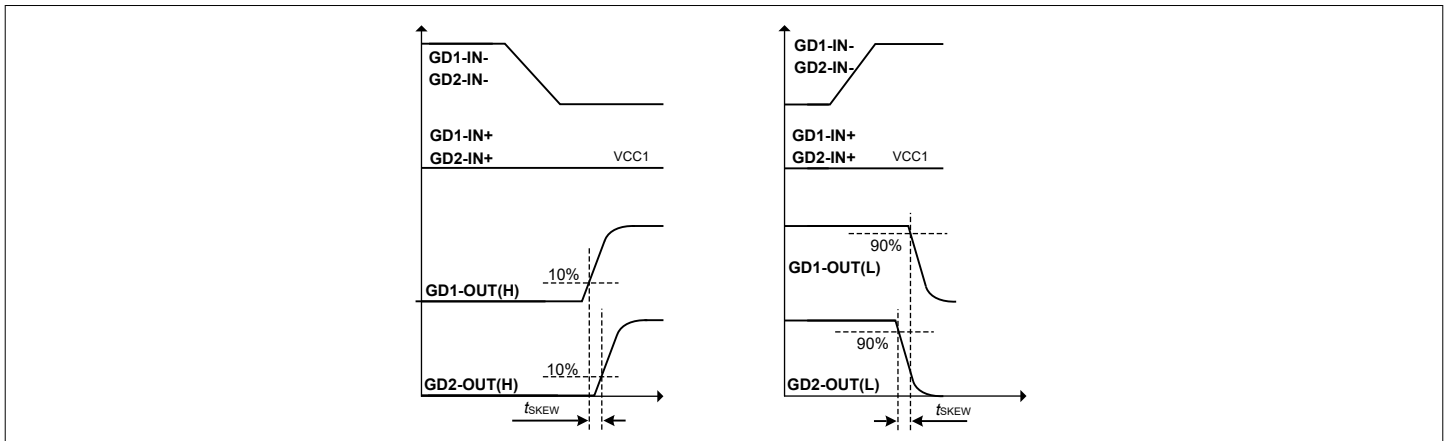


Figure 36 Input to output, part to part skew using the inverting input

Figure 37, Figure 38, Figure 39 and Figure 40 show the skew plus (t_{SKEW+}) using the non-inverting or inverting inputs on the input side under all the possible combinations. The skew plus parameter is valid at the same temperature and supply voltages. The parameter describes the variation between the turn-on and turn-off propagation delays in a half-bridge, under the previously mentioned conditions and defines the minimum dead time required from the gate driver perspective. This is relevant when driving the gate drivers with complimentary pulses, such as in a half-bridge.

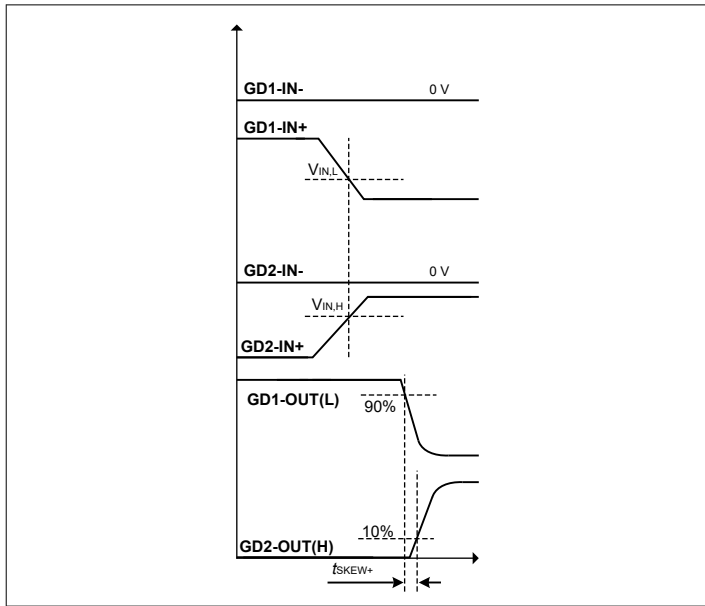


Figure 37 Skew plus using the non-inverting inputs

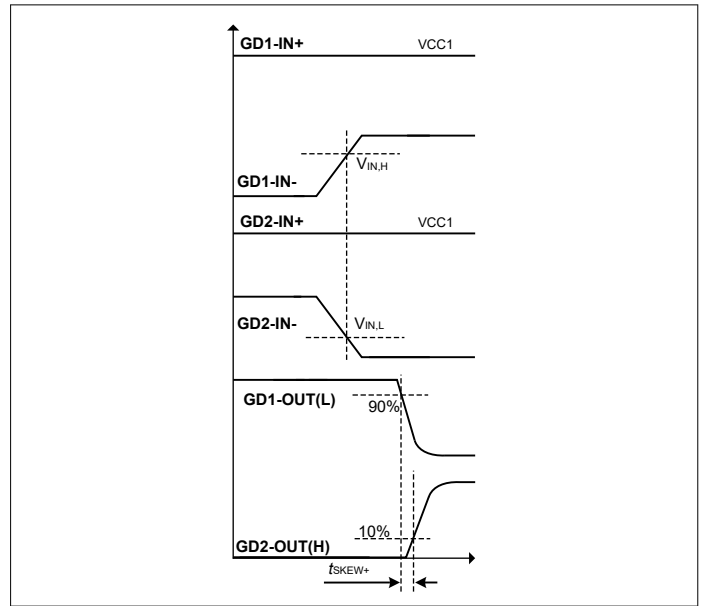


Figure 38 Skew plus using the inverting inputs

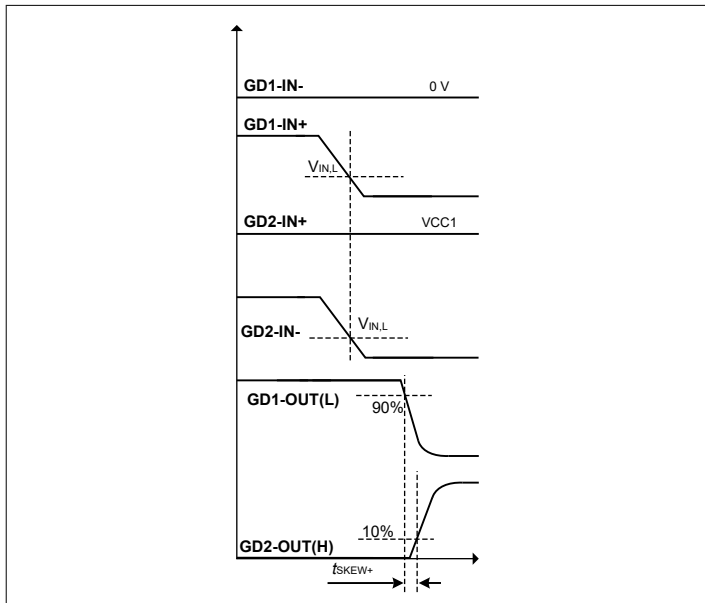


Figure 39 Skew plus using the inverting and non-inverting inputs with falling edges

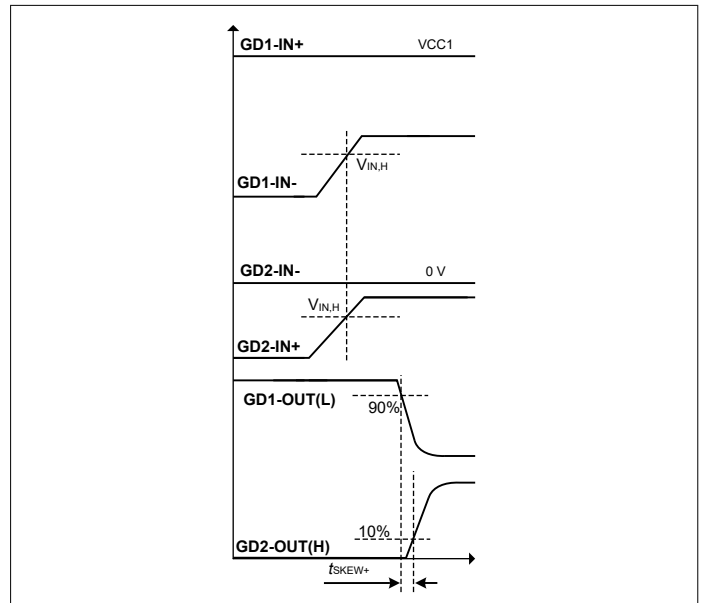


Figure 40 Skew plus using the inverting and non-inverting inputs with rising edges

8 Functional description

8.1 Input features

The input side of the gate driver has two inputs, $IN+$ and $IN-$, for the control signals and two power terminals, $VCC1$ and $GND1$, for the input chip supply.

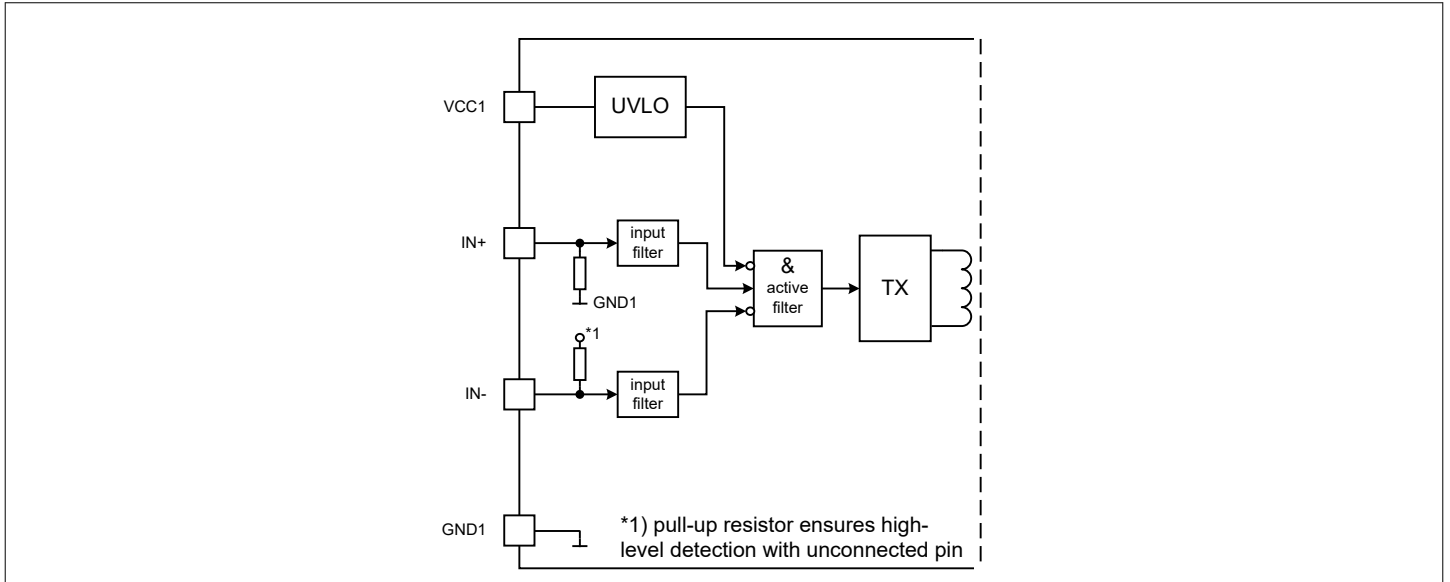


Figure 41 Block diagram of the input section

The gate driver IC input section consists of the following functional blocks:

- Input undervoltage lockout circuit
- Signal filtering
- Pull-up resistor for inverting input
- Pull-down resistor for non-inverting input
- Signal transmission to isolated output section

8.1.1 Input signal filtering (degitch filter)

The input section of the driver IC filters both the input signals to suppress the short pulses triggered by external influences.

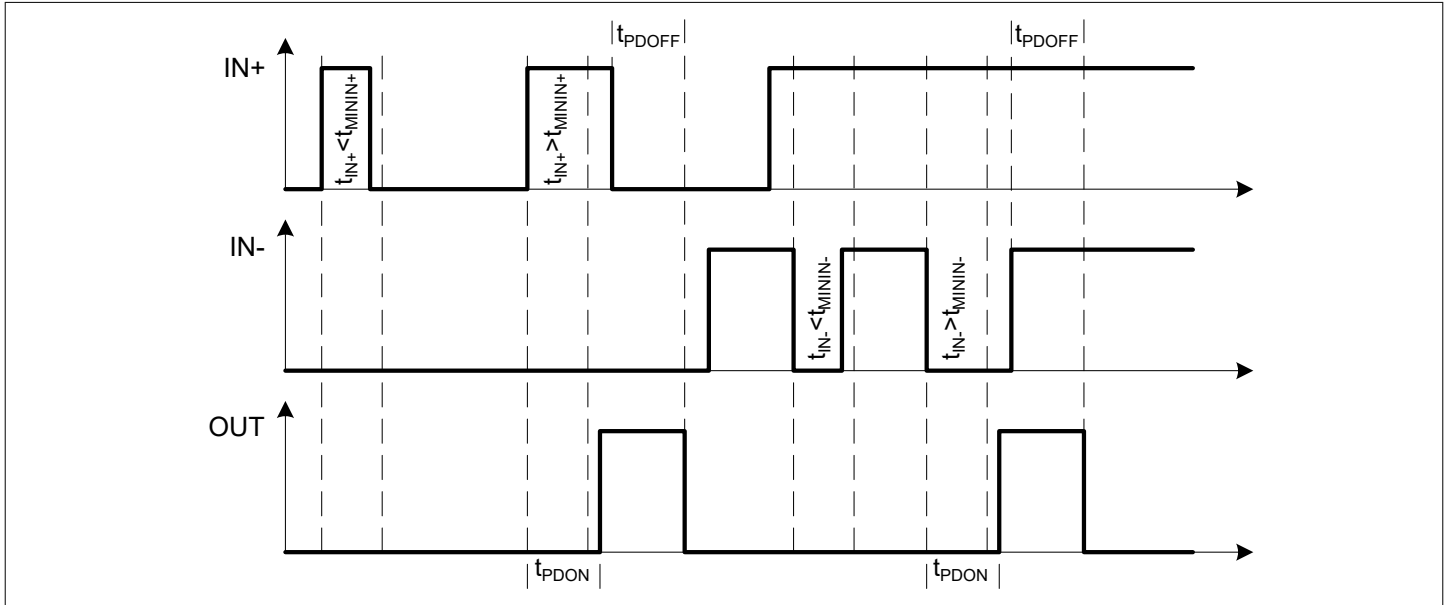


Figure 42 Input pulse suppression and turn-on/turn-off propagation delay

Every pulse at $IN+$ or $IN-$, shorter than the input pulse suppression time, t_{INFLT} , will be filtered and will not be transmitted to the output chip. Longer pulses will be sent to the output with the shown propagation delay, t_{PDON} and t_{PDOFF} . This helps the design and an external RC filter for noise suppression will not be needed in most cases.

8.1.2 Pull-up and pull-down resistors for the input pins

The input pull-up or pull-down resistors ensure an OFF-state in case the corresponding input is not connected. These resistors have a typical value of 75 kΩ. Even with the maximum allowed voltage at the $VCC1$ pin, the input current due to these resistors stays below 1 mA.

The pull-up and pull-down resistors are designed to be connected to an external supply or ground potential to permanently activate the individual driver input.

8.1.3 Input supply and undervoltage lockout (UVLO)

The input supply range has absolute maximum ratings of -0.3 V to 17 V. Static operation beyond the absolute maximum voltage (abs max) damages the internal structures and is, therefore, forbidden.

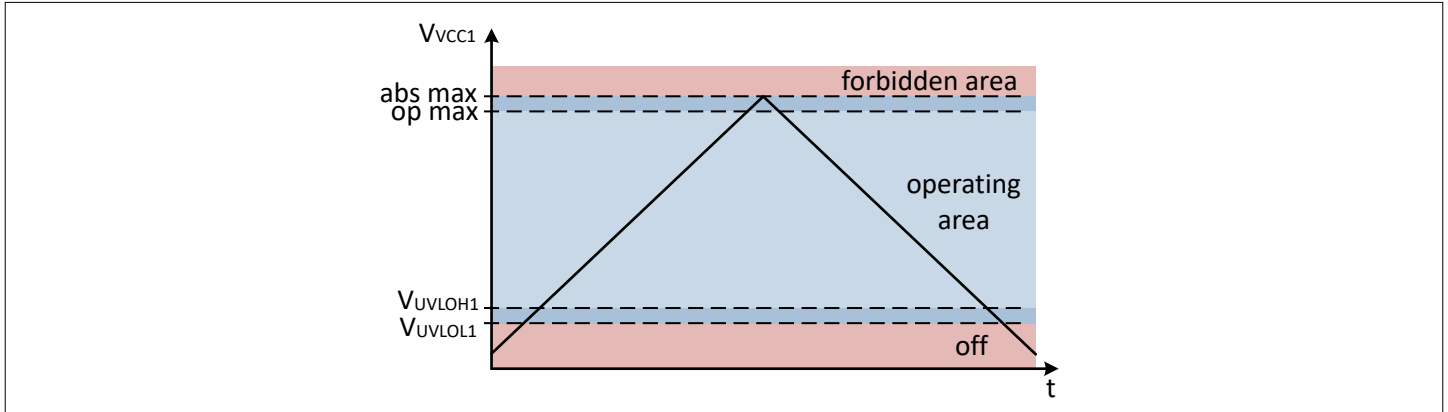


Figure 43 Input supply and UVLO threshold

At a crossing of the turn-on undervoltage lockout threshold, (V_{UVLOH1}), during a positive ramp at V_{CC1} pin, the input section starts to operate. It evaluates the input signals $IN+$ and $IN-$ and transmits their current state to the output section. During V_{VCC1} ramp down and crossing of the turn-off undervoltage lockout threshold, (V_{UVLOL1}), the input section sends a final off signal regardless of the $IN+$ or $IN-$ state. The hysteresis between the thresholds V_{UVLOL1} and V_{UVLOH1} ensures a stable operation when the supply voltage is close to the threshold levels.

Any voltage overshoot above the absolute maximum voltage (abs max) rating can damage the driver circuits. In this area, the current consumption increases dramatically and results in a violation of the maximum allowed input power dissipation. The operating area is defined between the turn-on undervoltage lockout threshold, (V_{UVLOH1}), and the maximum recommended operating voltage.

8.2 Output features

This section describes the output section of the gate drivers. The output features of the gate driver IC include undervoltage lockout for the output supply, shoot-through protection circuitry for the internal output stage and the active shutdown circuitry.

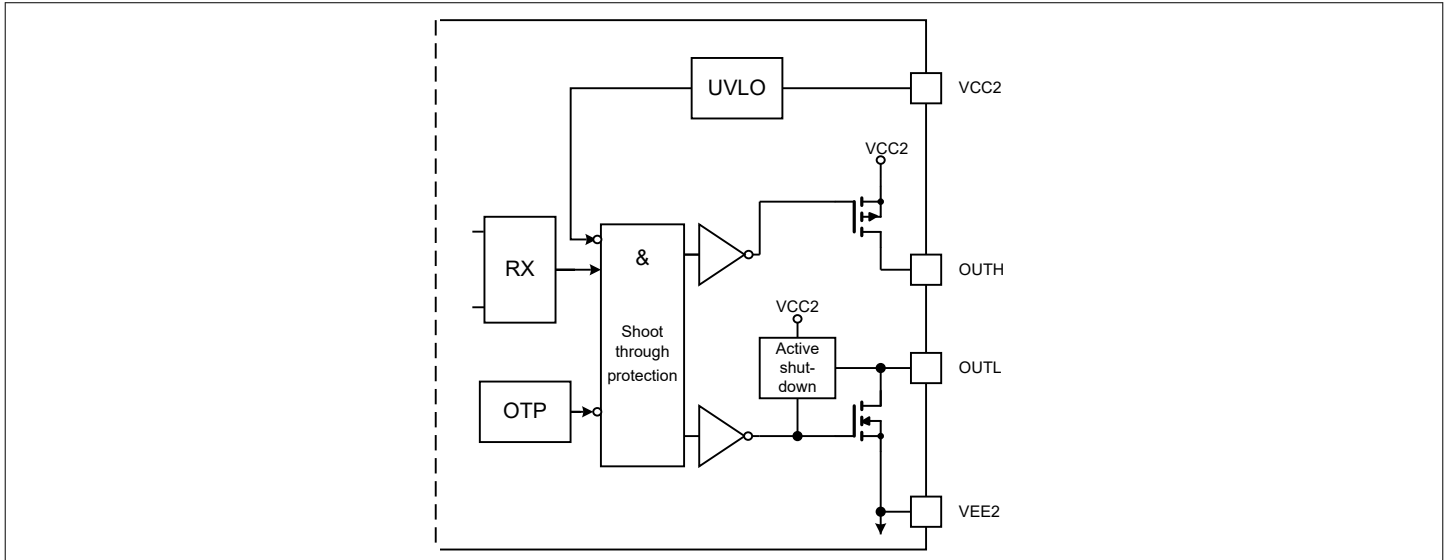


Figure 44 Block diagram of the output section for variants with separate source and sink pins

The output section of the gate driver ICs with separate outputs consists of the following functional blocks:

- Output undervoltage lockout circuit
- Isolated signal receiver from the input section
- Sourcing and sinking output stage
- Active shutdown circuitry
- Overtemperature protection

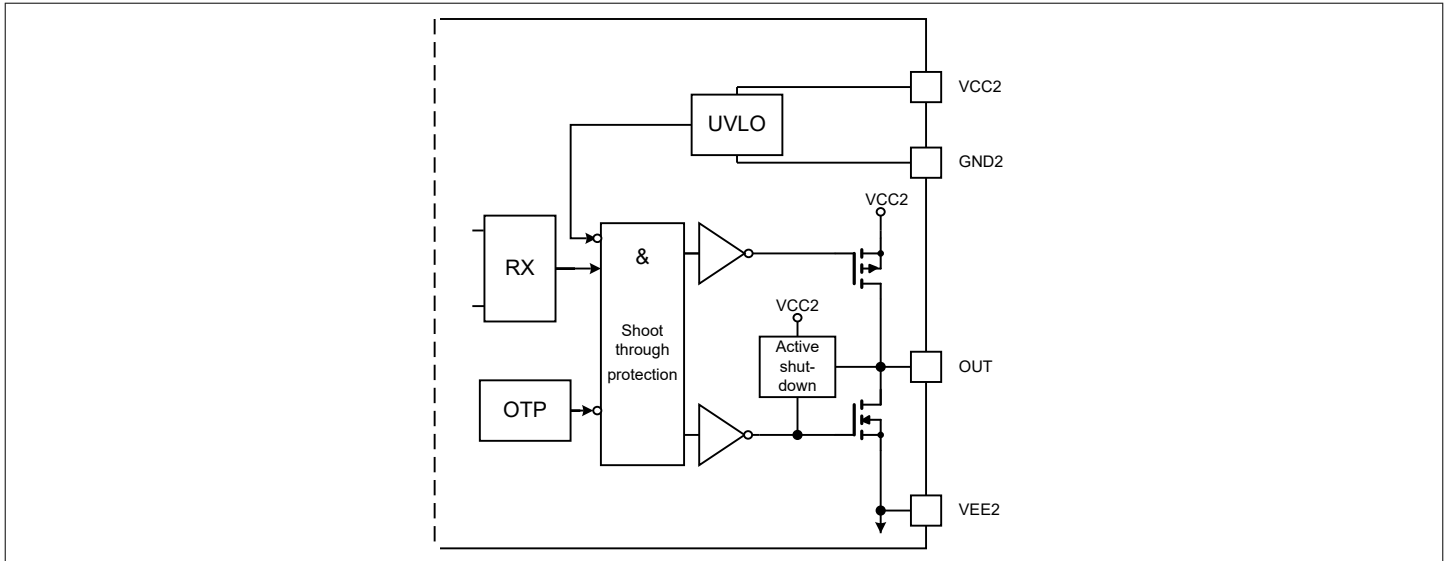


Figure 45 Block diagram of the output section for variants with GND2 pin

The output section of the gate driver ICs with *GND2* pin consists of the following functional blocks:

- Output undervoltage lockout circuit which is referenced to *GND2* pin
- Isolated signal receiver from the input section
- Sourcing and sinking output stage connected together internally
- Active shutdown circuitry
- Overtemperature protection

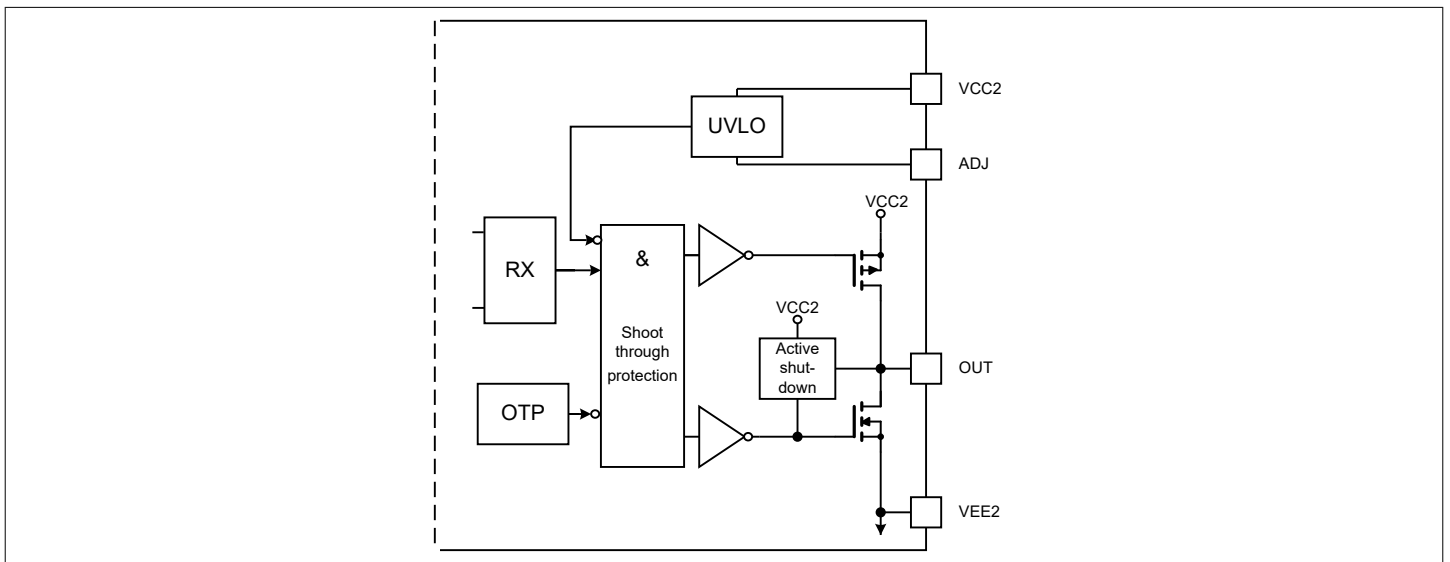


Figure 46 Block diagram of the output section for variants with ADJ pin

The output section of the gate driver ICs with *ADJ* pin consists of the following functional blocks:

- Output undervoltage lockout circuit that allows adjusting the UVLO threshold voltages using the *ADJ* pin
- Isolated signal receiver from the input section
- Sourcing and sinking output stage connected together internally
- Active shutdown circuitry
- Overtemperature protection

8.2.1 Driver outputs and supply

The output driver section uses MOSFETs to provide a rail-to-rail output as shown in Figure 44, Figure 45 and Figure 46. This feature allows a tight control of the gate voltage during ON-state and short circuit to be maintained as long as the driver's supply voltage is stable. Due to the low internal voltage drop, switching behavior of the IGBT, Si or SiC MOSFET is predominantly governed by the gate resistor for as long as the current rating of the gate driver is not exceeded. Furthermore, it reduces the power to be dissipated by the driver as most of the energy is dissipated in the gate resistor.

The current sourcing stage of the gate driver ICs is designed with a PMOS-only MOSFET. The PMOS delivers a strong current, at the beginning of the turn-on process and then sustains a high gate current until the gate reaches V_{CC2} rail voltage, ensuring a fast turn-on of the IGBT, Si or SiC MOSFET. The current sinking stage consists of an NMOS.

8.2.2 Output undervoltage lockout (UVLO)

The output supply range has a positive absolute maximum rating of 35 V for all variants. The gate driver ICs are therefore capable of providing a bipolar gate voltage to a connected power switch.

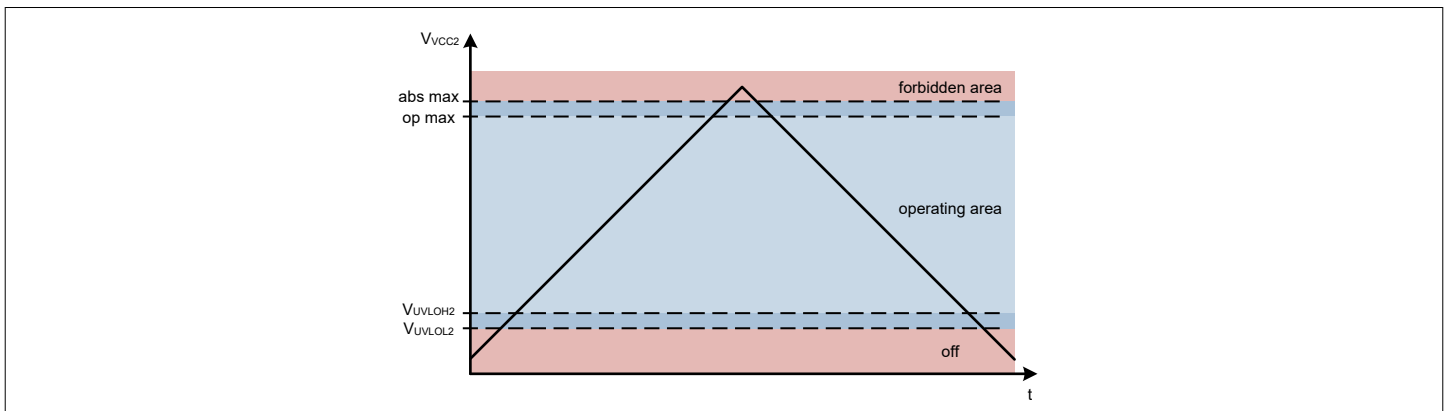


Figure 47 Output supply and UVLO threshold

The UVLO feature protects the power switch by preventing the operation when the output supply voltage, V_{VCC2} , is too low. During the positive ramp of the output supply voltage, V_{VCC2} , once the voltage is higher than the UVLO threshold (V_{UVLOH2}), the output stage starts operating by switching the output pins on and off depending on the signals received from the input side of the gate driver. During V_{VCC2} ramp down, once the voltage is lower than the turn-off UVLO threshold, (V_{UVLOL2}), the output section initiates a turn-off command regardless of the signals received from the input section. The hysteresis between the thresholds V_{UVLOL2} and V_{UVLOH2} ensures a stable operation when the supply voltage is close to the threshold levels.

For the variants with separate outputs, the output supply voltage, V_{VCC2} , is measured against the voltage, V_{VEE2} . Therefore, for these variants, the output UVLO monitors the complete rail-to-rail supply voltage. Alternatively, for the variants with $GND2$ pin, the V_{VCC2} is measured against the ground pin $GND2$. Hence, for these variants, the UVLO monitors only the positive supply voltage when a bipolar supply voltage is used on the output side and the gate driver prevents the OUT pin from turning on when the positive supply voltage is too low. As a result, in applications where bipolar supply voltage is used, the variants with $GND2$ pin offer a more effective UVLO protection to the IGBT, Si or SiC MOSFET.

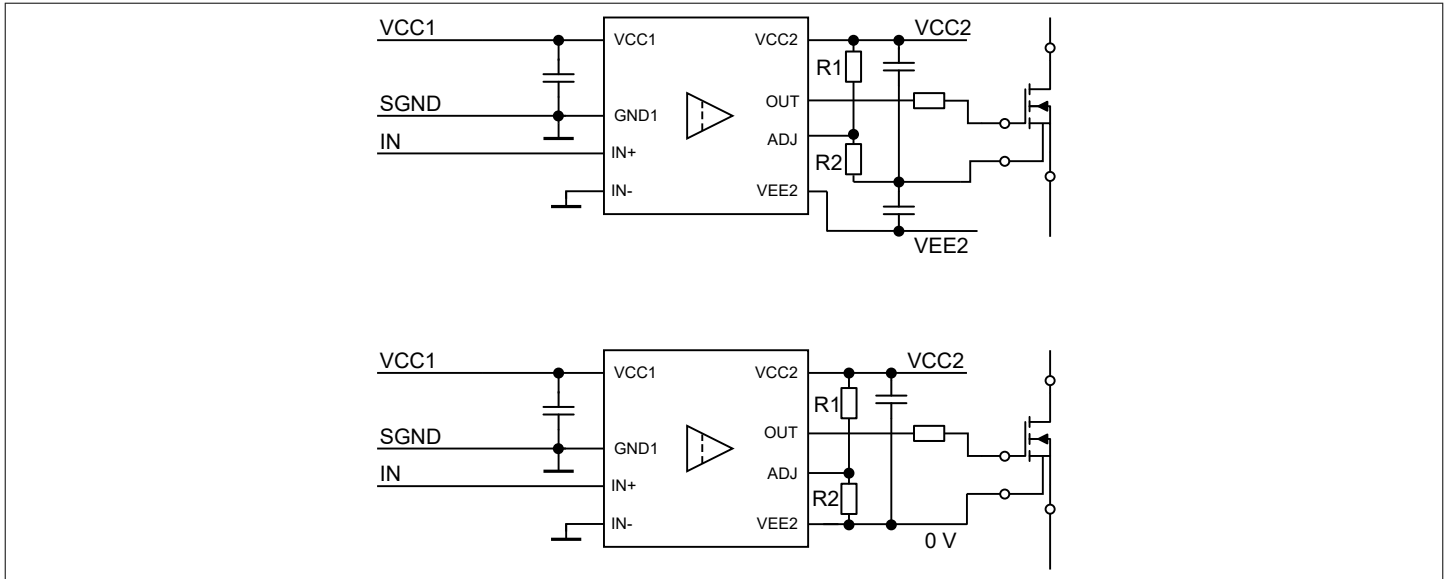


Figure 48 UVLO level adjustment for 1ED3145 with unipolar and bipolar supply voltages

Lastly, the part 1ED3145 allows the adjustment of the voltage, V_{VCC2} , at which the UVLO protection is active. As shown in the [Figure 46](#), the output UVLO block has the ADJ pin that is used for adjusting the UVLO level. The UVLO block of the gate driver monitors the voltage, V_{VCC2} , against the voltage on this ADJ pin. During the positive voltage ramp of the output supply voltage, V_{VCC2} , once the voltage on the ADJ pin exceeds the UVLO threshold, $V_{ADJ,UVLOH2}$, the output stage starts operating by switching the output pin on and off depending on the signals received from the input side of the gate driver. During the ramp down of the supply voltage, V_{VCC2} , once the voltage on the ADJ pin is lower than the turn-off UVLO threshold, $V_{ADJ,UVLOL2}$, the output section initiates a turn-off regardless of the signals received from the input section. The hysteresis between the thresholds $V_{ADJ,UVLOL2}$ and $V_{ADJ,UVLOH2}$ ensures stable operation when the supply voltage is close to the threshold levels.

A resistive voltage divider consisting of the resistors R_1 and R_2 is used to set the voltage on the ADJ pin to the desired level. When a unipolar supply voltage is used, the resistor divider is connected between $VCC2$ and the $VEE2$ pins. In case a bipolar supply is used in the application, the resistor divider is connected between $VCC2$ pin and the virtual ground of the system so that the UVLO block monitors only the positive supply voltage and prevents the operation of the gate driver when the positive supply voltage is too low.

The voltage on the ADJ pin, V_{ADJ} , is set in a way such that when the supply voltage, V_{VCC2} , is higher than the desired level for turn-on, $V_{VCC2,ON}$, the following condition is true :

$$V_{VCC2} - V_{ADJ} > V_{ADJ,UVLOH2} (\text{Max.}) \quad (1)$$

Therefore, the resistance of the resistors R_1 and R_2 can be selected to meet the condition:

$$\frac{R_1}{R_1 + R_2} \times V_{VCC2,ON} > V_{ADJ,UVLOH2} (\text{Max.}) \quad (2)$$

For reliable operation of the gate driver's UVLO function, using a resistance value between 1 k Ω and 10 k Ω for R_1 and to limit the total resistance in the voltage divider to less than 100 k Ω is recommended. In case of a noisy environment, using a resistance close to 1 k Ω for the resistor R_1 is recommended.

Any voltage overshoot above the absolute maximum voltage rating can damage the driver circuits. In this area, the current consumption increases dramatically and therefore results in a violation of the maximum allowed power dissipation. The operating area is defined between the turn-on undervoltage lockout threshold (V_{UVLOH2}) and the maximum recommended operating voltage.

8.2.3 Active shut down

The active shut down function is a protection feature of the driver. It is designed to prevent the free-floating gate of a connected power switch from triggering a turn on.

The active shut down feature ensures a safe IGBT, Si or SiC MOSFET OFF-state in case the output chip is not connected to the power supply or an undervoltage lockout is in effect. The IGBT, Si or SiC MOSFET gate is clamped via the *OUT(L)* pin to *VEE2*.

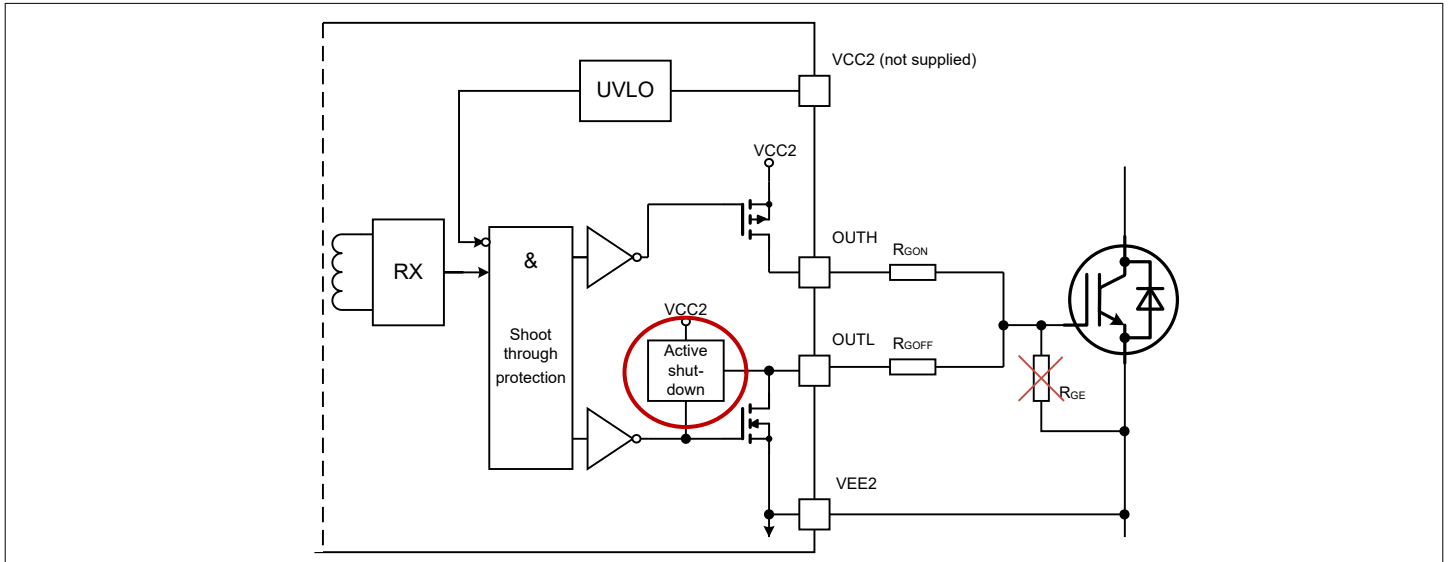


Figure 49 Block diagram showing active shut down for the variants with separate source and sink pins

In case of a missing or collapsing power supply at the *VCC2* pin, the output section of the driver operates in the active shutdown mode. In this case, the driver uses the floating voltage of the connected gate to supply this internal circuit. This solution is much stronger than using an external gate to emitter resistor, R_{GE} . At the same time, in the case of fast dV/dt events on the switch that could generate Miller current which can bias the gate, even when the gate driver is not powered on, the active shutdown circuit will use the voltage to power itself and actively pull the gate low. The active shut down feature functions in a similar manner across all the variants.

8.2.4 Short circuit clamping

During short circuit, the gate voltage of the power transistor tends to rise because of the feedback via the Miller capacitance. In this situation, the IC internally clamps the voltage on the *OUT(H)* pin and limits the voltage to a value slightly higher than the supply voltage, V_{VCC2} . A maximum current of 500 mA may be fed back to the supply through this path for 10 μ s. If higher currents are expected or tighter clamping is desired, external Schottky diodes should be added between the *OUT(H)* and *VCC2* pins.

8.2.5 Overtemperature protection

Overtemperature protection shuts down the output of the gate driver IC and protects the application from destructive failure when the junction temperature of the IC exceeds the threshold temperature, T_{OTPOFF} . However, it is important to note that this protection activation threshold and the release threshold exceed the absolute maximum junction temperature, T_J , of the IC. Therefore, overtemperature protection does not prevent the damage of the gate driver IC, in case the absolute maximum junction temperature is exceeded.

9 Application information

Note: Infineon is providing this information as a courtesy only and without acknowledging any legal obligation. Information in the following application chapters is not part of the Infineon component specification, and Infineon does not warrant its accuracy or completeness. Infineon's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical application

This section describes how the gate drivers can be used in an application.

Figure 50 and Figure 51 show a typical application for gate drivers with separated outputs for current sourcing and sinking. For these variants, individual gate resistors can be used for turning a power switch on and off. By having separate sourcing pin, *OUTH*, and sinking pin, *OUTL*, the bill of materials (BOM) can be optimized, saving a bypass schottky diode for each power switch used.

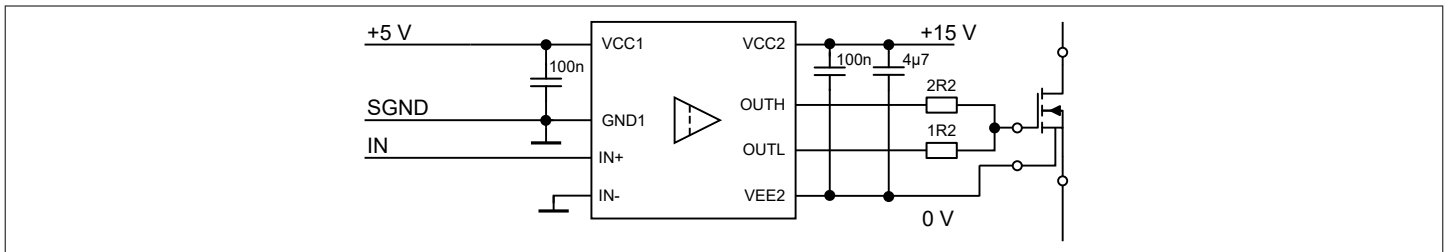


Figure 50 Circuit example for variants with separate source and sink pins using unipolar power supply driving SiC MOSFET

When driving the switch with unipolar power supply voltages, the *VEE2* pin should be connected directly to the source or emitter of the power transistor as shown in Figure 50.

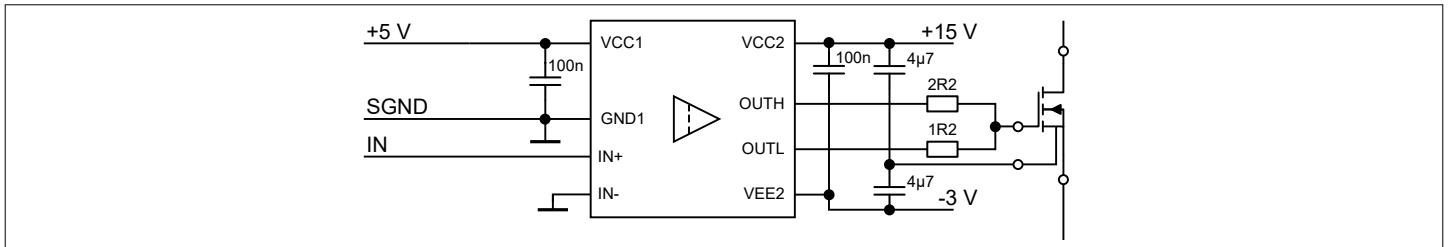


Figure 51 Circuit example for variants with separate source and sink pins bipolar power supply driving SiC MOSFET

When driving the switch with bipolar power supply voltages, a virtual ground should be created between the two capacitors connected to the *VCC2* and *VEE2* pins. This virtual ground should then be connected to the source or emitter of the power transistor as shown in Figure 51.

Figure 52 and Figure 53 depict the typical application circuit for the gate drivers with *GND2* pin. For the variants with *GND2* pin, the sourcing and sinking stages of the output are connected internally and the sourcing and sinking gate currents are provided by the *OUT* pin. In case different gate resistances are required for turning the power switch on and off, a separate bypass diode of schottky type can be used on the sinking path.

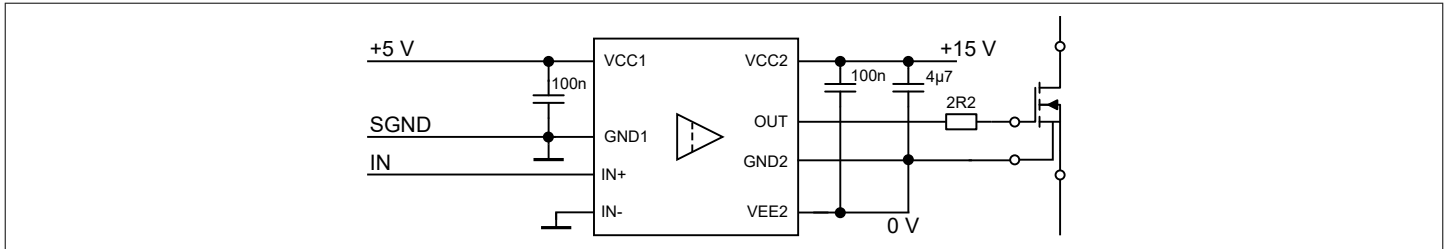


Figure 52 Circuit example for variants with *GND2* pin using unipolar power supply driving SiC MOSFET

When driving the switch with unipolar power supply voltages, the *GND2* pin should be connected directly to the source or emitter of the power transistor as shown in [Figure 52](#). Furthermore, the *VEE2* pin should be connected to the *GND2* pin.

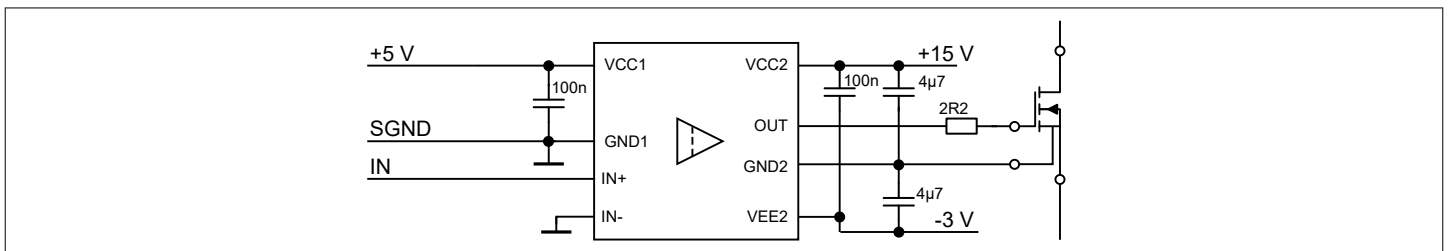


Figure 53 Circuit example for variants with *GND2* pin using bipolar bipolar power supply driving SiC MOSFET

When driving the switch with bipolar power supplies, the *GND2* pin should be connected to the source or emitter of the power transistor as shown in [Figure 53](#).

Finally, the typical application circuit for variants that have output side adjustable UVLO function are shown in [Figure 54](#) and [Figure 55](#).

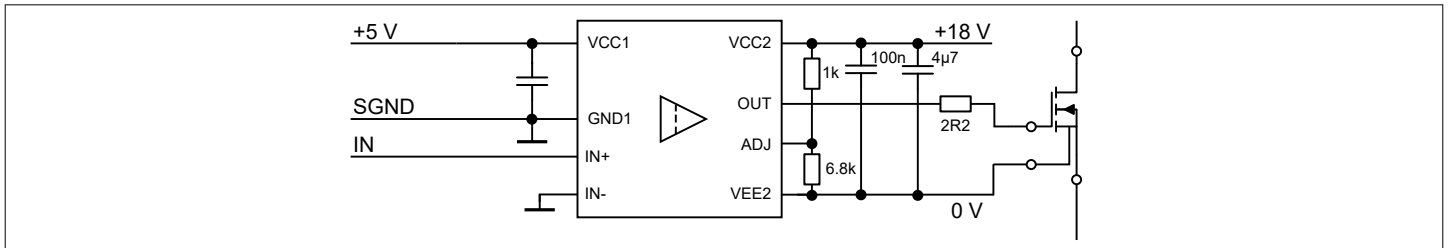


Figure 54 Circuit example for variants with adjustable UVLO using unipolar power supply driving SiC MOSFET

When driving the switch with unipolar power supply voltages, the *VEE2* pin should be connected directly to the source or emitter of the power transistor as shown in [Figure 54](#). The resistor voltage divider connected between *VCC2* and *VEE2* pins is used to adjust the output side UVLO thresholds

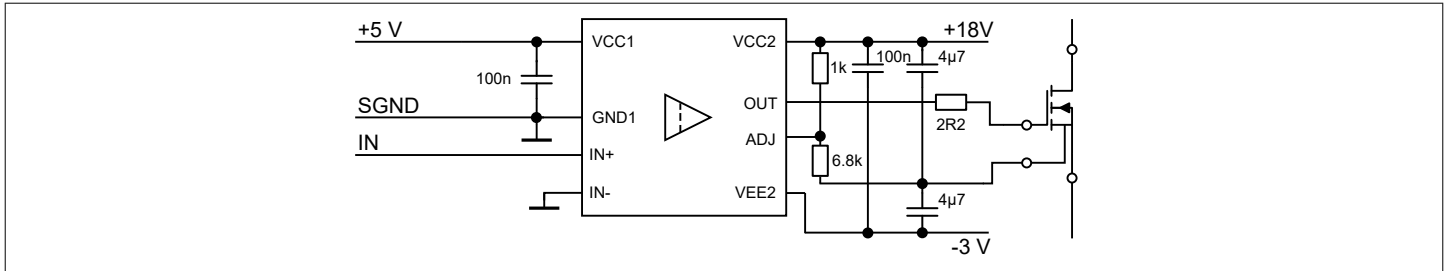


Figure 55 Circuit example for variants with adjustable UVLO using bipolar power supply driving SiC MOSFET

When driving the switch with bipolar power supply voltages, a virtual ground should be created between the two capacitors connected to the *VCC2* and *VEE2* pins as shown in Figure 55. The resistor voltage divider connected between *VCC2* and the virtual ground is used to adjust the output side UVLO thresholds.

9.2 Power supply recommendations

The 1ED314x gate drivers support a wide range of voltages on the input and output side. These devices can operate with unipolar as well as bipolar power supply voltages on the output side for reliable and safe operation in the application.

To ensure that the gate driver operates correctly, it is necessary to place appropriate decoupling capacitors on the power supply pins. On the input side, placing a low ESR, surface mount, multilayer ceramic capacitor of 100 nF between the *VCC1* pin and *GND1* pin is recommended. This capacitor should be placed as close as possible to the pins. The decoupling capacitors on the output side, in addition to decoupling any disturbance on the power supply, also store the energy necessary to deliver the gate currents required for turning on and off the power transistor. Therefore, these capacitors should be dimensioned appropriately to limit the voltage drop during the power transistor turn-on and turn-off process. When using a unipolar power supply, a low ESR, surface mount, multilayer ceramic capacitor of at least 4.7 µF should be placed between the *VCC2* pin and the *VEE2* pin, in close proximity of the pins. In case of bipolar power supply, using at least 4.7 µF ceramic capacitor between *VCC2* and virtual ground (source or emitter potential of power transistor) or, if applicable *GND2* pin is recommended. Similarly, using a 4.7 µF capacitor between *VEE2* pin and virtual ground or *GND2* pin is recommended. Depending on the gate charge of the power transistor and the peak source and sink gate currents, a higher capacitance may be necessary to limit the voltage drop during power transistor turn-on and turn-off. Finally, a 100 nF decoupling capacitor is recommended between *VCC2* and *VEE2* pins to ensure a short path between them to decouple any high frequency noise.

When selecting the capacitors, it is important to consider the capacitance drop of ceramic capacitors with respect to the applied DC voltage.

9.3 Usage of $IN+$ and $IN-$

The inverting, $IN-$, and non-inverting, $IN+$, input pins offer multiple possibilities to connect the PWM input and logic signals for various control and protection uses.

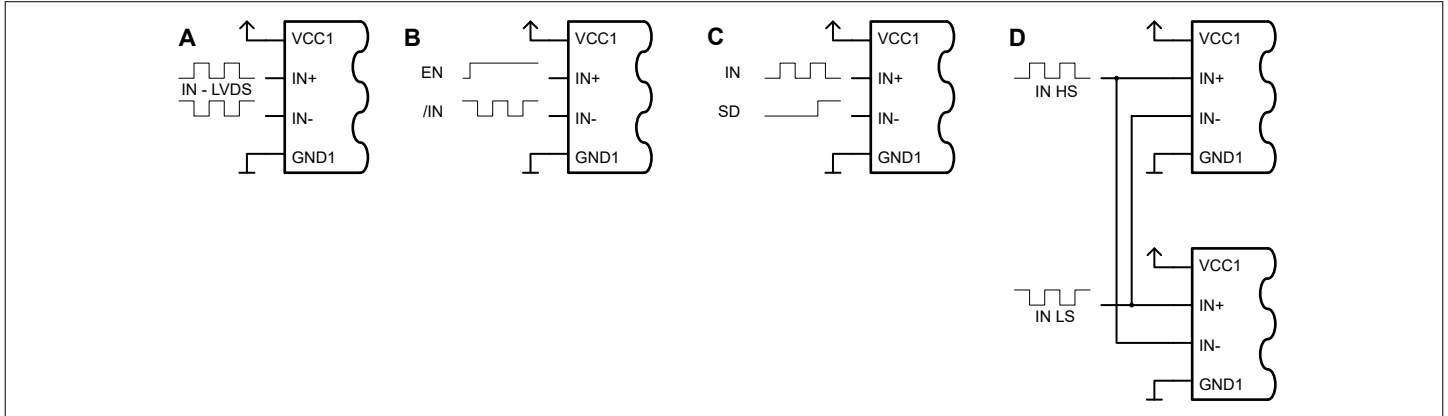


Figure 56 Input $IN+$ and $IN-$ usage

Apart from using both inputs with a differential signal (A) ($VCC1$ and $GND1$ levels), using only one input signal for actual switch control leaves the second input available for functions such as Enable (B), Shutdown (C), or Interlock (D).

A) Differential signal

Applying a logic-level differential signal on both $IN+$ and $IN-$ with the positive level of $VCC1$ pin and the negative level of $GND1$ pin improves common-mode noise rejection. However, it is important to note that the input pins $IN+$ and $IN-$ are not truly differential in nature and the signals on these pins are referenced against the input ground, $GND1$.

B) Enable

Using the $IN+$ pin as enable signal leaves the $IN-$ to control the output PWM with an inverted logic input signal. The enable signal can then be shared between the gate driver ICs of a complete inverter to start operation with a single control signal.

C) Shutdown

Using the $IN-$ pin as shutdown signal leaves the $IN+$ to control the output PWM with a non-inverted logic input signal. The shutdown signal can then be shared between the gate driver ICs of a complete inverter to interrupt operation with a single control signal.

D) Interlock

Interlocking is often used in half-bridge configurations to avoid a shoot-through current from the high-voltage DC bus supply. Connecting the following input signal pins of the top and bottom driver ICs together inhibits the static turn on for both channels at the same time:

- Top gate driver's non-inverting input ($IN+$) with the bottom driver inverting input ($IN-$)
- Bottom gate driver's non-inverting input ($IN+$) with the top driver inverting input ($IN-$)

Dynamic turn-on and turn-off characteristics of gate drivers and power switches can still lead to short-term shoot through. To avoid overlapping turn-on times at the power switches, a proper dead time setting for the PWM generation at the microcontroller is recommended.

9.4 Gate resistor selection

The gate resistor is a key component in the gate drive circuit. The gate resistor limits the source and the sink current of the gate driver thereby exercising control over the switching speed of the associated power transistor during both turn-on and turn-off operations. As such, the careful selection of an appropriate gate resistor represents a vital consideration in the design process. Some important considerations for selection of the gate resistance are:

- Optimize the switching losses
- Limit the overshoots and oscillations of the drain source voltage or the collector emitter voltage of the power transistor during turn-off
- Limit the overshoot and oscillations of the drain current or collector current during turn-on
- Damp the oscillations of the gate source or gate emitter voltage caused by parasitic inductances and capacitances in the gate loop

As a starting point in the gate driver selection, the gate resistor used in the datasheet of the power transistor for the characterization of turn-on and turn-off losses can be used. The power supply conditions are rarely the same as the power supply conditions used in power transistor datasheets. Therefore, an adaptation of the power transistor datasheet values is required to obtain a starting point to optimize of the final gate resistor. The method proposed here uses the same peak gate current value for both the actual application and the power transistor datasheet.

The peak gate current as per power transistor datasheet equals to:

$$I_{G, pk} = \frac{\Delta V_{GS, datasheet}}{R_{G, datasheet} + R_{G, int}} = \frac{\Delta V_{GS, application}}{R_{G, application} + R_{G, int}} \quad (3)$$

with $\Delta V_{GS} = V_{VCC2} - V_{VEE2}$

Solving this equation for $R_{G, application}$ leads to:

$$R_{G, application} = \frac{\Delta V_{GS, application}}{I_{G, pk}} - R_{G, int} \quad (4)$$

This method results in a starting point for the gate resistor selection. Further evaluations, such as EMI measurements, are required for the final dimensioning of the gate resistors as they have to be adjusted to work with the circuitry inductance, margins and allowed dV/dt transients.

While dimensioning the components for gate resistances, it is necessary to consider the average power dissipation in these resistors due to the switching of the power transistor, as explained in [Chapter 9.5.2](#), as well as the pulse power capability of the component.

9.5 Power dissipation estimation

9.5.1 Gate driver

The gate driver's input side losses are dominated by the quiescent losses, which are calculated as:

$$P_{Q1} = V_{VCC1} \cdot I_{Q1} \quad (5)$$

The gate driver's output side losses consist of the quiescent current losses, P_{Q2} , at nominal switching frequency and no load, the sourcing losses, P_{source} , and the sinking losses, P_{sink} :

$$P_{OUT} = P_{Q2} + P_{source} + P_{sink} \quad (6)$$

The quiescent losses on the output side, P_{Q2} , can be calculated as:

$$P_{Q2} = (V_{VCC2} - V_{VEE2}) \cdot I_{Q2} \quad (7)$$

The turn-on, P_{source} , and turn-off, P_{sink} , losses can be estimated using the inner gate driver resistance, $R_{DSON,H}$ or $R_{DSON,L}$, the external gate resistor, $R_{G,ext}$, and, if applicable, the internal gate resistance of the power transistor, $R_{G,int}$, the application related gate charge, Q_G , the total gate driving voltage, $V_{VCC2} - V_{VEE2}$, and switching frequency, f_{sw} :

$$P_{source} = \frac{1}{2} Q_G \cdot f_{sw} \cdot (V_{VCC2} - V_{VEE2}) \cdot \frac{R_{DSON,H}}{R_{DSON,H} + R_{G,ext,ON} + R_{G,int}} \quad (8)$$

$$P_{sink} = \frac{1}{2} Q_G \cdot f_{sw} \cdot (V_{VCC2} - V_{VEE2}) \cdot \frac{R_{DSON,L}}{R_{DSON,L} + R_{G,ext,OFF} + R_{G,int}}$$

Additionally, external components that surround the gate driver can heat up the IC. The mere calculation of losses and the theoretical junction temperature alone are not sufficient for a proven gate driver circuit design. A verification through measurement is required to avoid unexpected effects in the application. It is possible to identify the hotspots, for example, by using an infrared camera.

9.5.2 External gate resistor

The losses in the gate resistor for turn-on, $R_{G,ext,ON}$ and the gate resistor for turn-off, $R_{G,ext,OFF}$ can be estimated using the same resistive voltage divider formed by the resistances in the source and the sink path of the gate current as:

$$P_{source,ext} = \frac{1}{2} Q_G \cdot f_{sw} \cdot (V_{VCC2} - V_{VEE2}) \cdot \frac{R_{G,ext,ON}}{R_{DSON,H} + R_{G,ext,ON} + R_{G,int}} \quad (9)$$

$$P_{sink,ext} = \frac{1}{2} Q_G \cdot f_{sw} \cdot (V_{VCC2} - V_{VEE2}) \cdot \frac{R_{G,ext,OFF}}{R_{DSON,L} + R_{G,ext,OFF} + R_{G,int}}$$

9.6 Output UVLO level adjustment

As described in [Chapter 8.2.2](#), the output side UVLO can be set to a desired level for enhanced system reliability, especially when using SiC MOSFETs. An example of UVLO setting is shown in [Figure 57](#). In this example, a bipolar power supply is used where V_{VCC2} is 18 V and V_{VEE2} is -3 V referred to the Kelvin source potential.

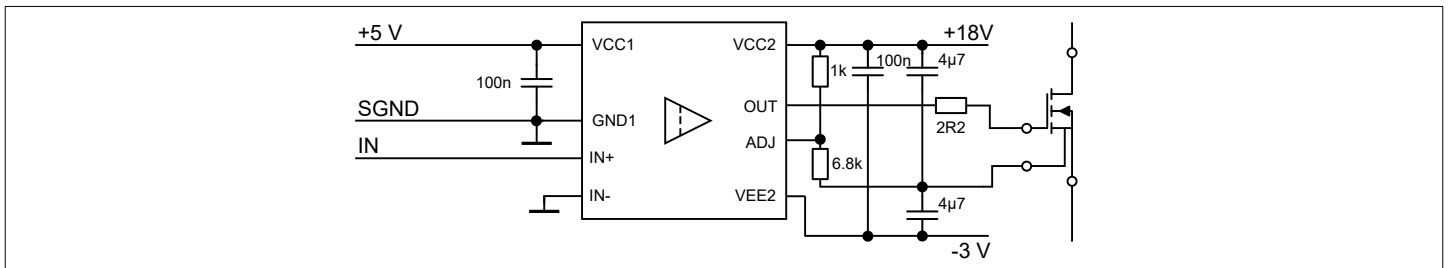


Figure 57 Example of UVLO level adjustment for 1ED3145

To set the UVLO such that the gate driver is ready for operation when V_{VCC2} exceeds 16.2 V:

$$\frac{R_1}{R_1 + R_2} \times V_{VCC2, ON} > V_{ADJ, UVLOH2} (\text{Max.}) \quad (10)$$

$$\frac{R_1}{R_1 + R_2} \times 16.2 \text{ V} > 2.07 \text{ V} \quad (11)$$

Selecting a value of 1 kΩ for R_1 results in 6.8 kΩ for the resistor R_2

9.7 Layout guideline

Having a well-designed PCB layout is crucial to achieve optimal performance of the gate driver. Subsequently, it ensures that the entire power electronic converter operates at its best. Creating a well-designed PCB layout requires a certain level of attention and consideration to specific key factors. The key points that should be considered while designing the PCB layout using 1ED314x gate drivers are:

- The low-ESR, low-ESL type decoupling capacitor on the input side must be placed close to the $VCC1$ and $GND1$ pins and connected to the pins such that the decoupling loop is as short as possible. Similarly, the decoupling capacitors on the output side should be placed close to the $VCC2$ and $VEE2$ pins and connected to the pins with a short connection
- It is crucial to minimize the physical area of the gate current loop that carries the current for charging and discharging the gate of the power transistor. The gate loop contains traces with high dv/dt and di/dt and having a short loop minimizes the noise caused by the turning on and off of the gates of the power transistor. Furthermore, a short loop also minimizes the stray inductance of the gate loop and improves the switching performance. To accomplish a short gate loop, the gate driver should be positioned near the power transistor and the decoupling capacitors that store the energy for high peak currents should be located in close proximity to the gate driver
- To reduce the stray inductance of the gate loop even further, wide traces can be used for the traces in the gate loop. Furthermore, the forward path and the return path of the currents can be routed parallel to each other on the same PCB layer or overlapping each other on adjacent PCB layers to achieve the least amount of stray inductance
- In the case of a unipolar power supply, the $VEE2$ pin of the gate driver should be connected to the Kelvin source/emitter pin of the power transistor, if available. Similarly, in the case of a bipolar power supply, the virtual ground between the decoupling capacitors or the $GND2$ pin should be connected to the Kelvin source/emitter pin of the power transistor. If the Kelvin pin is not available, then the connection to the source/emitter should be as short as possible to avoid the high current from the power transistor flowing in the gate loop
- The area below the body of the gate driver package should be kept free of any traces to ensure the integrity of the safety isolation between the input and output side
- It is recommended that the input signals of the gate driver connected to the $IN+$ and $IN-$ pins be kept away from any noisy traces. Although the 1ED314x gate drivers come with an integrated input filter that can filter high frequency noise on the input signal, an external RC filter with a small time constant can be placed close to these pins for enhanced filtering. Additionally, a ground plane below the input signal traces is recommended for shielding the signals from noise
- For the variant with adjustable UVLO, 1ED3145, care must be taken while designing the layout of the output side UVLO circuit. Traces of the UVLO circuit and resistors used for setting the UVLO must be placed away from any high dV/dt and di/dt generated by the switching of the power transistor. Additionally, it is also crucial to ensure there is no noise, caused by the high dV/dt and di/dt of the gate loop, coupling in to the UVLO circuit
- The gate driver IC experiences power dissipation during system operation as explained in [Chapter 9.5.1](#). This heat generated in the device is dissipated mostly via the PCB. Maximizing the copper area connected to the $GND1$ and $VEE2$ pins is recommended for effectively dissipating the heat from the gate driver on to the PCB

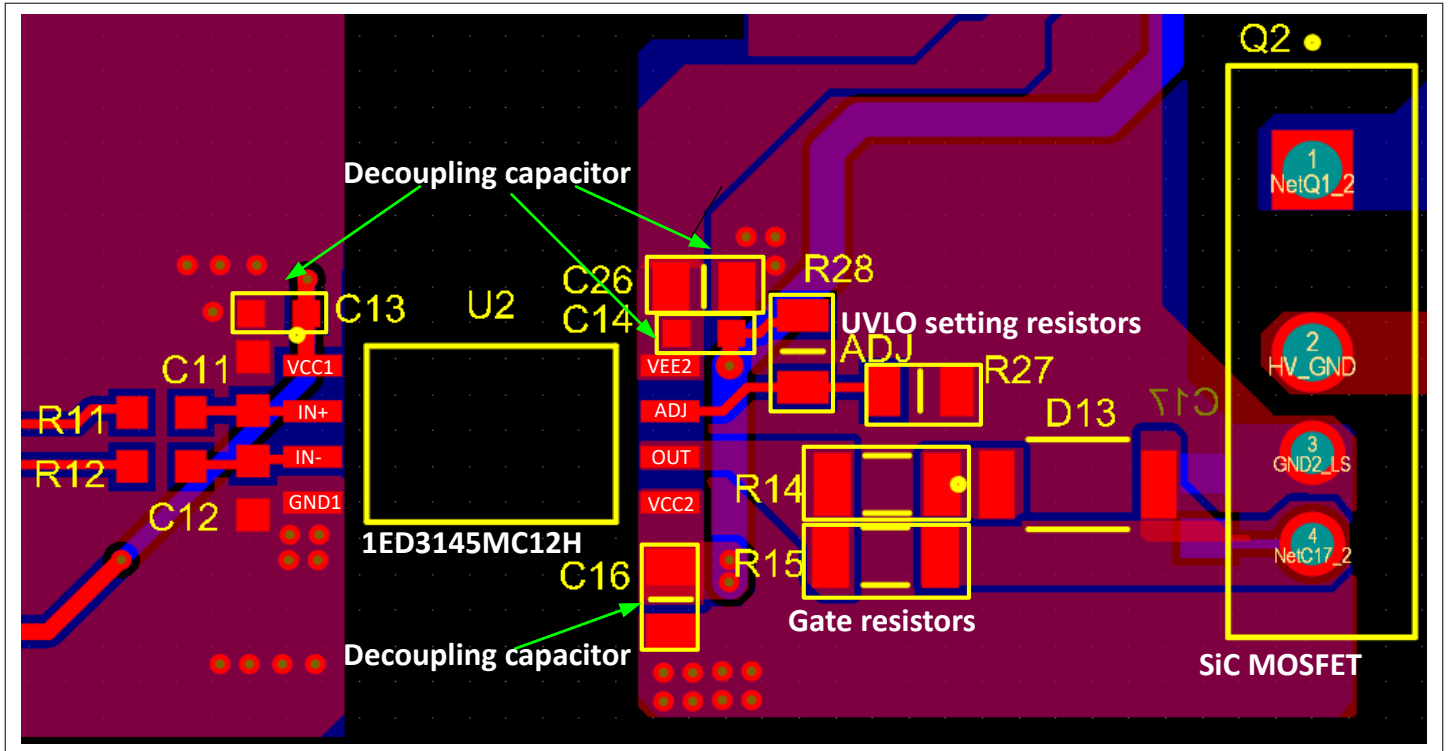


Figure 60 Sample PCB layout for variants with adjustable UVLO

10 Related products

Note: Please consider the gate driver IC power dissipation and insulation requirements for the selected power switch and operating condition.

Product group	Product name	Description
TRENCHSTOP™ IGBT Discrete	IKWH40N65WR6	650 V, 40 A IGBT with anti-parallel diode in TO-247-3-HCC
	IHW30N160R5	1600 V, 30 A IGBT Discrete with anti-parallel diode in TO-247
	IKW15N120CS7	1200 V IGBT7 S7, 15 A IGBT with anti-parallel diode in TO247
	IKQ75N120CS7	1200 V IGBT7 S7, 75 A IGBT with anti-parallel diode in TO247-3
CoolSiC™ SiC MOSFET Discrete	IMBF170R1K0M1	1700 V, 1000 mΩ SiC MOSFET in TO-263-7 with extended creepage
	IMZA120R040M1H	1200 V, 40 mΩ SiC MOSFET in TO247-4 package
	IMZA120R014M1H	1200 V, 14 mΩ SiC MOSFET in TO247-4 package
	IMBG120R030M1H	1200 V, 30 mΩ SiC MOSFET in TO-263-7 package
	IMYH200R012M1H	2000 V, 12 mΩ SiC MOSFET in TO-247-PLUS with high creepage and clearance
CoolSiC™ SiC MOSFET Module	FS33MR12W1M1H_B11	EasyPACK™ 1B 1200 V, 33 mΩ sixpack module
	FF17MR12W1M1H_B11	EasyDUAL™ 1B 1200 V, 17 mΩ half-bridge module
	FF4MR12W2M1H_B11	EasyDUAL™ 2B 1200 V, 4 mΩ half-bridge module
	F4-17MR12W1M1H_B11	EasyPACK™ 1B 1200 V, 17 mΩ fourpack module
TRENCHSTOP™ IGBT Modules	F4-100R17N3E4	EconoPACK™ 3 1700 V, 100 A fourpack IGBT module
	F4-200R17N3E4	EconoPACK™ 3 1700 V, 200 A fourpack IGBT module
	FP10R12W1T7_B11	EasyPIM™ 1B 1200 V, 10 A three phase input rectifier PIM IGBT module
	FS100R12W2T7_B11	EasyPACK™ 2B 1200 V, 100 A sixpack IGBT module
	FP150R12KT4_B11	EconoPIM™ 3 1200V three-phase PIM IGBT module
	FS200R12KT4R_B11	EconoPACK™ 3 1200 V, 200 A sixpack IGBT module

11 Package dimensions

11 Package dimensions

PG-DSO-8 (150 mil)

This package has a moisture sensitivity level MSL=3.

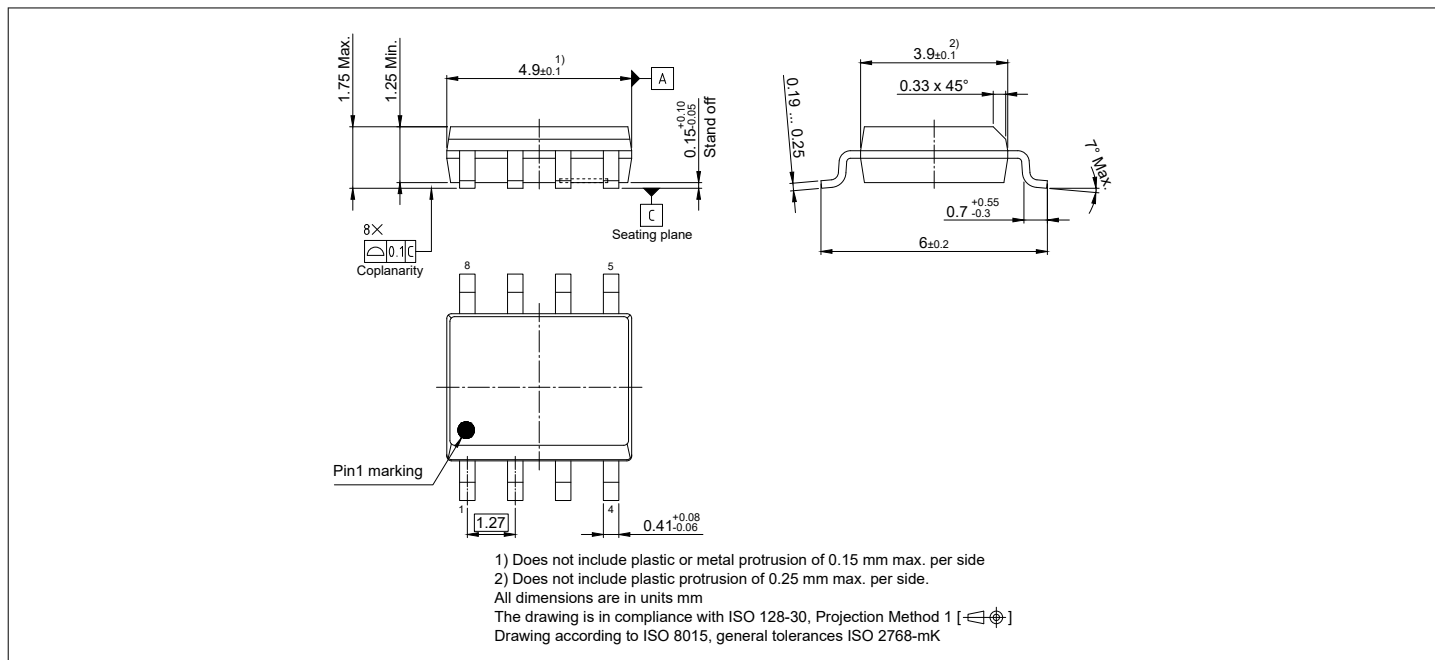


Figure 61 PG-DSO-8 (150 mil) (Plastic dual small outline package, 150 mil)

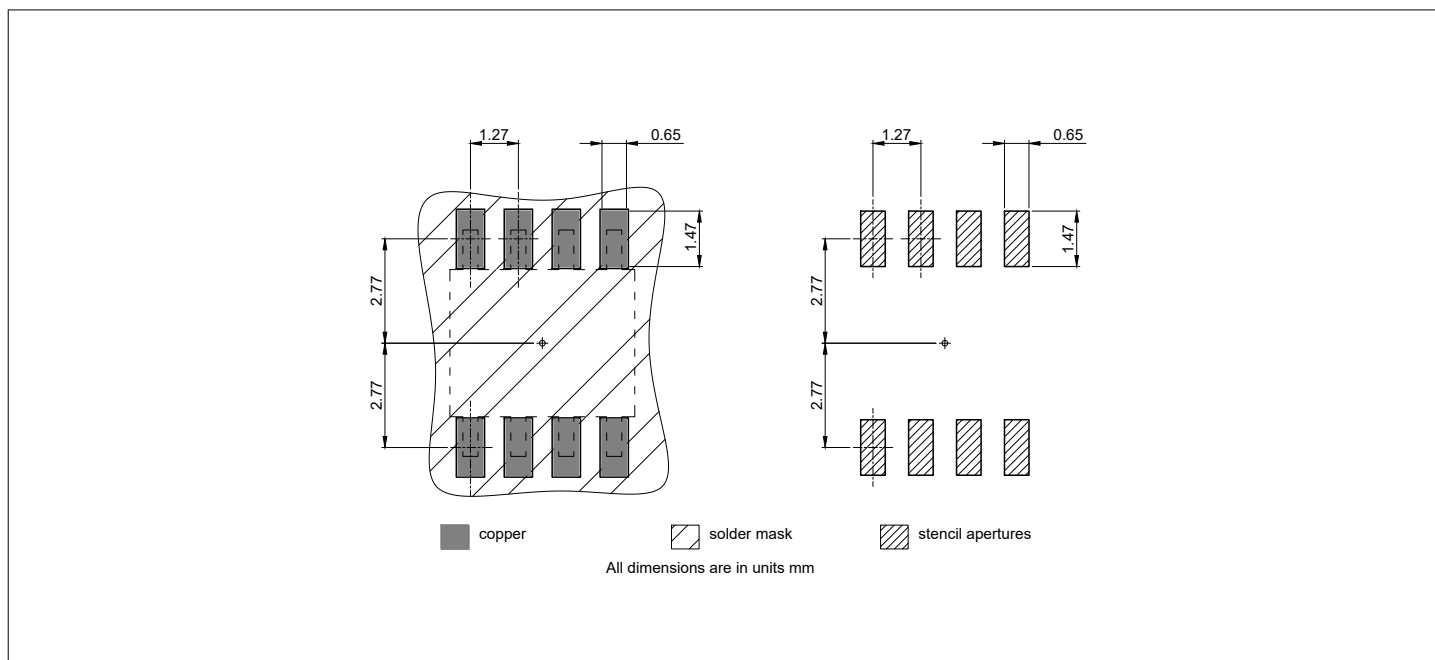


Figure 62 PG-DSO-8 (150 mil) recommended footprint

11 Package dimensions

PG-LDSO-8 (300 mil)

This package has a moisture sensitivity level MSL=2.

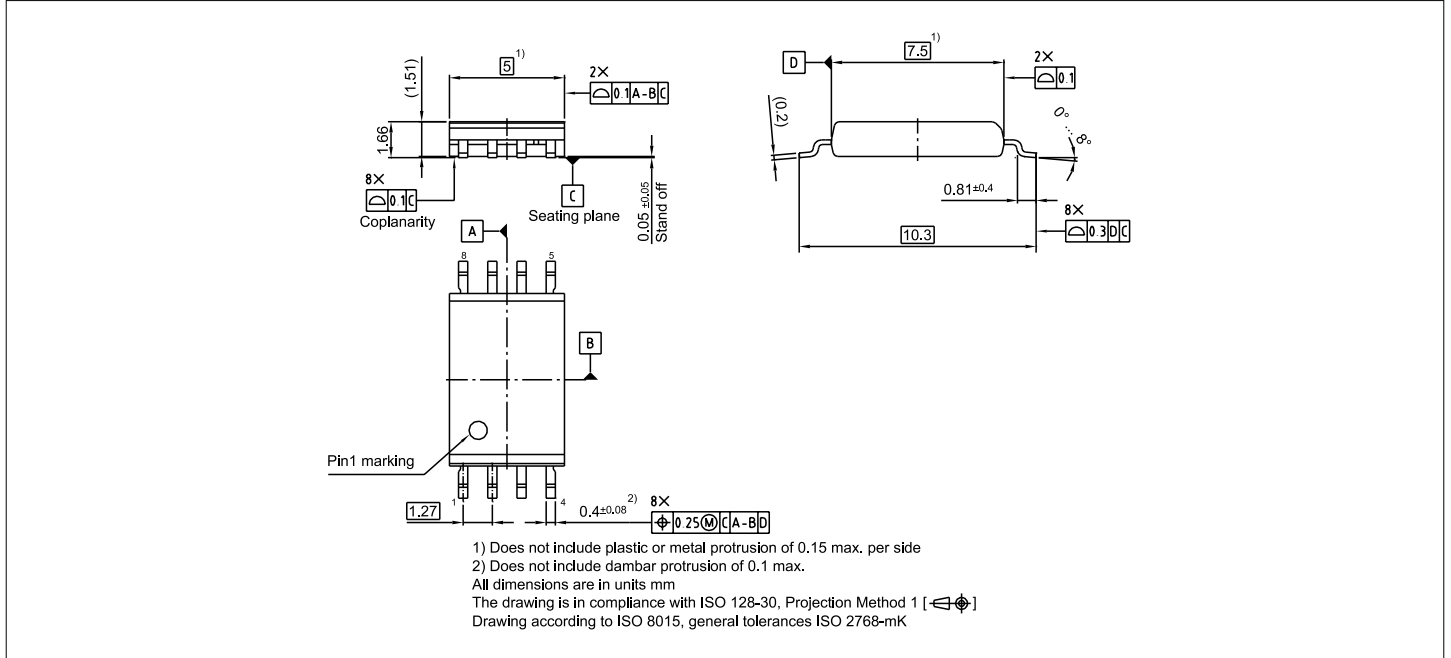


Figure 63 PG-LDSO-8 (300 mil) (Plastic dual small outline package, 300 mil)

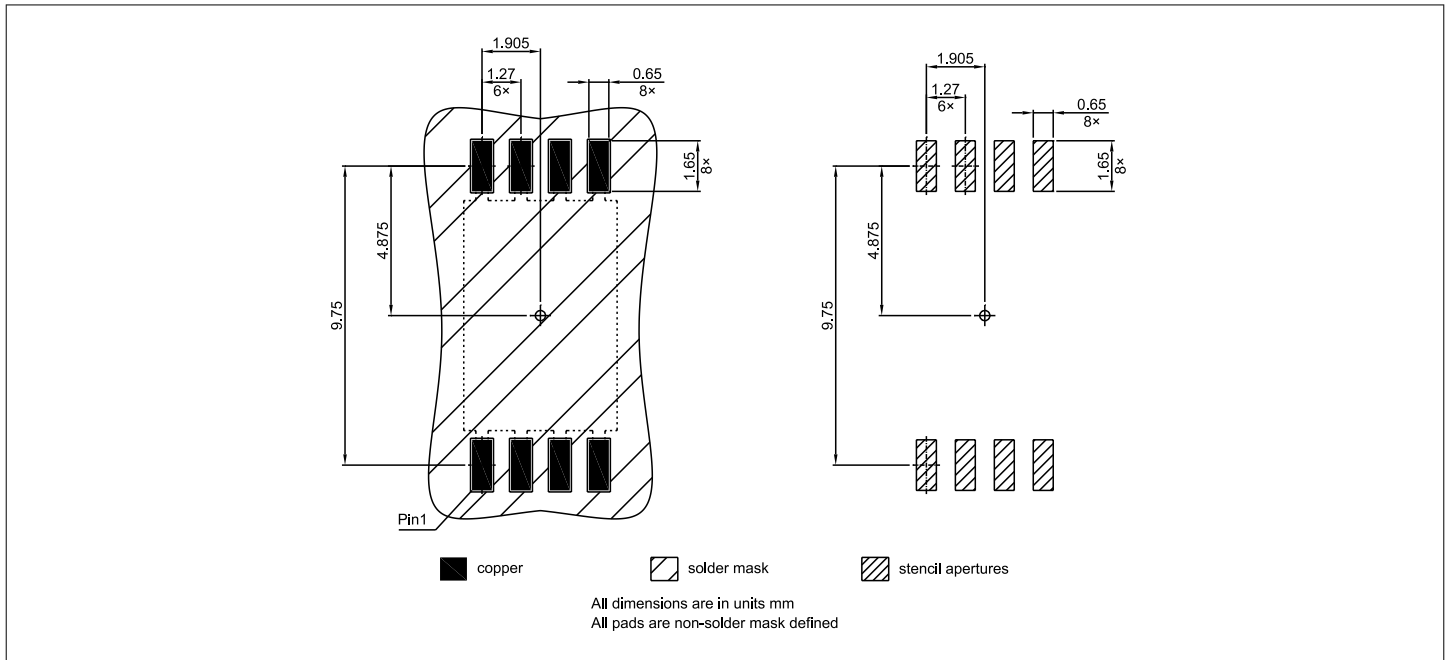


Figure 64 PG-LDSO-8 (300 mil) recommended footprint

11 Package dimensions

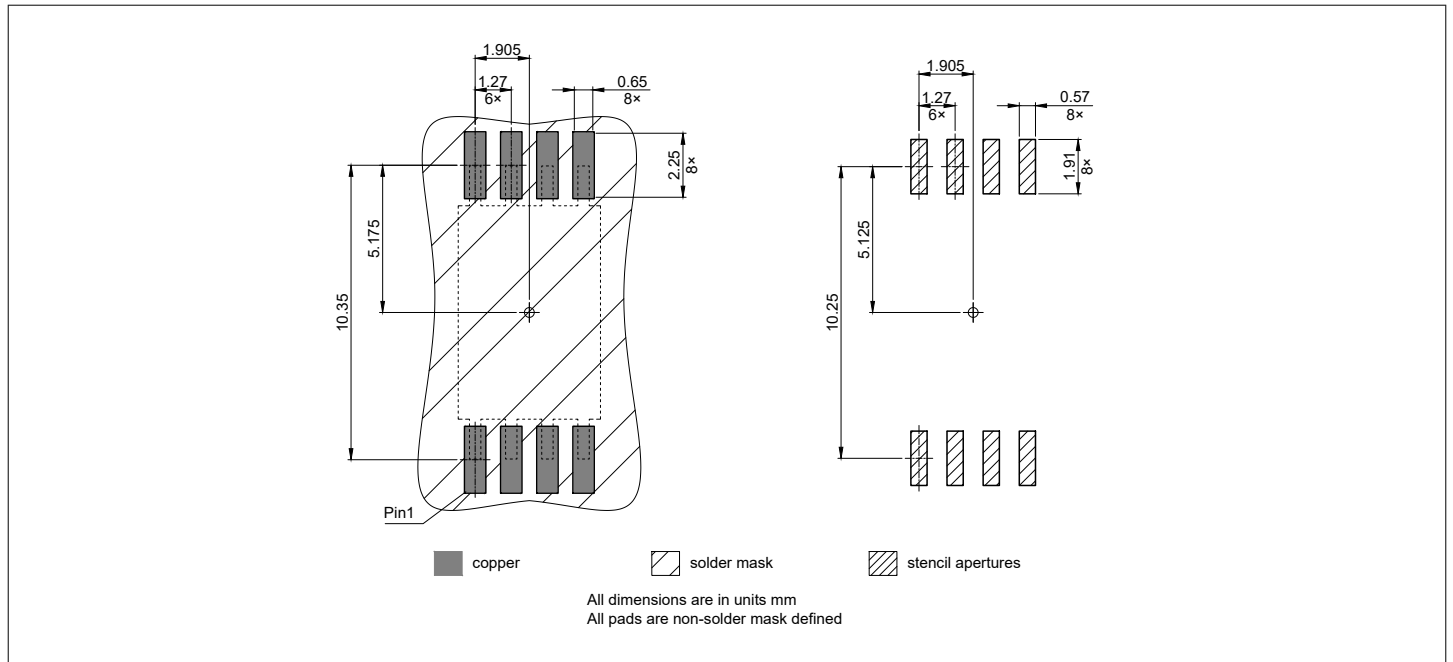


Figure 65 PG-LDSO-8 (300 mil) alternative footprint

Revision history

Document version	Date of release	Description of changes
v2.20	2026-02-25	<ul style="list-style-type: none">Updated IEC 60747-17 certificate informationAdded moisture sensitivity level for PG-DSO-8 (150 mil) and PG-LDSO-8 (300 mil) packageAdded alternative footprint for PG-LDSO-8 (300 mil) package
v2.10	2025-10-10	<ul style="list-style-type: none">Added the overvoltage category to insulation characteristics table for PG-DSO-8 (150 mil) packageUpdated the maximum working isolation voltage for PG-LDSO-8 (300 mil) package
v2.0	2024-10-04	<ul style="list-style-type: none">Initial release of 1ED314xMC12H products
v1.20	2024-10-01	<ul style="list-style-type: none">Updated the values of the parameters, t_{PDON}, t_{PDOFF}, t_{INFLT} and $t_{IN,min}$
v1.11	2023-07-26	<ul style="list-style-type: none">Removed duplicate parameters from dynamic characteristics and active shut down
v1.10	2023-06-26	<ul style="list-style-type: none">Increased CTI value to 600
v1.0	2023-01-15	<ul style="list-style-type: none">Initial release of 1ED314xMU12F products

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