33 W USB power delivery charger using ICE5QSBG

REF_5QSBG_33W1

About this document

Scope and purpose

This document shows a reference board design for a 33 W USB power delivery (PD) charger using the latest Infineon 5th generation quasi-resonant (QR) controller **ICE5QSBG**. The charger is designed with a universal input with a USB type-C output connector to charge USB PD-enabled devices such as smartphones and tablets with multi-output configuration.

Highlights of the 33 W USB PD charger:

- Supports USB PD 3.0 programmable power supply (PPS) up to 33 W continuous output power in a universal input voltage range
- High average efficiency and low standby power to meet the European Union's Code of Conduct (CoC) Version 5 Tier 2 single-voltage external AC-DC power supply basic-voltage/low-voltage requirements
- Comprehensive protection feature, QR controller **ICE5QSBG** in DSO-8 package and a highly intergrated USB type-C port controller with synchronous rectifier (SR) function from Cypress PAG1S for secondary side
- Narrow-lead **700 V CoolMOS™ P7** in **TO-220** package and high-frequency switching OptiMOS™ in **SuperSO8** package

Intended audience

This document is intended for power supply design or application engineers, etc. who want to design USB PD chargers that are efficient under light and heavy load conditions, reliable and easy to design.

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1 System introduction

It's now possible to charge laptops, tablets, smartphones, smartwatches and other wearable and portable gadgets that have rechargeable batteries using a single universal charger solution. Most chargers have fast-charging capabilities, detecting whether the connected device can accept fast-charging, and then configuring their output to the right charging profile. Standards such as USB PD, quickcharge (QC) and supercharge are among the proprietary technologies that enable the fast-charging feature. Charging cables and connectors should be able to support increased output power without compromising safety, for example by resisting overheating. Lightning and USB type-C ports are the most used for these types of applications. Although charging power is increased, the form factor should remain small for portability.

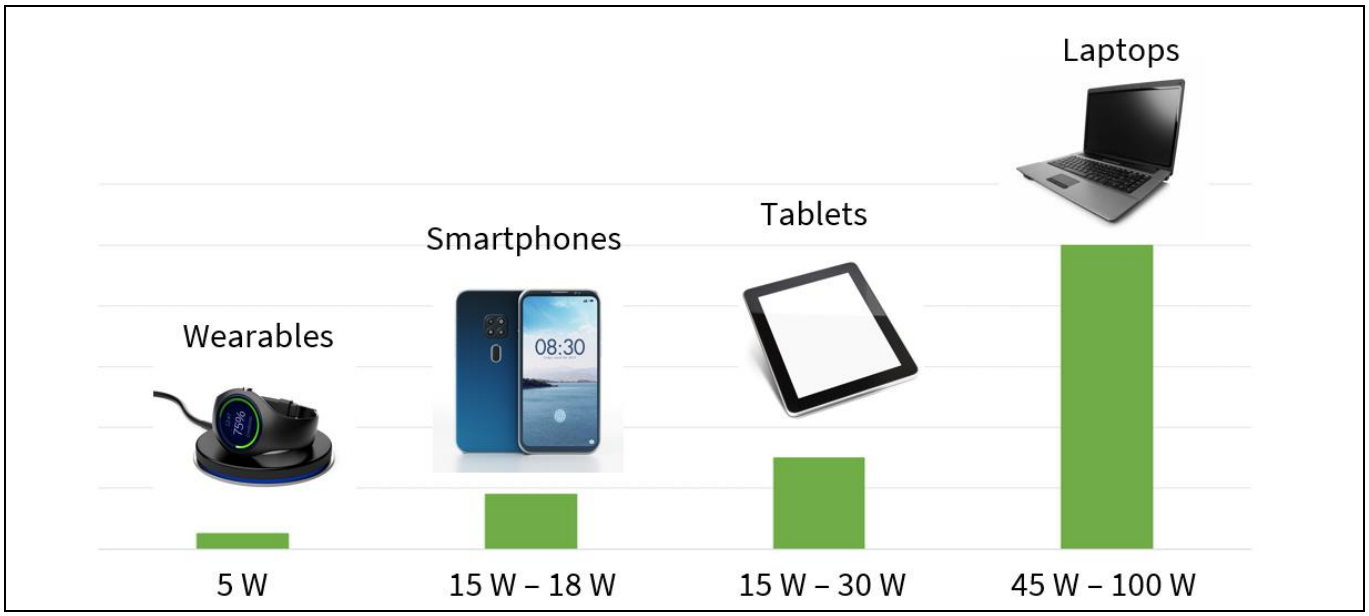


Figure 1 Charging requirements for portable devices

1.1 Fast-charging technologies

There are various fast-charging standard protocols in the market. The most commonly used protocols are QC and USB PD.

QC 4.0+ and USB PD are intercompatible, which means a USB PD charger should support fast-charging a QC 4.0+ device, and a QC 4.0+ charger should support fast-charging a USB PD device.

QC 4.0+ and USB PD are variable-output voltages up to 20 V. With the USB PD 3.0 PPS, which is also compatible and supports QC 4.0+, the output allows small steps in voltage (as low as 20 mV incremental steps) and current (as low as 50 mA incremental steps).

As for the connector ports, the previous version of QC (2.0 and 3.0) can be delivered through USB type-A. QC 4.0+ and USB PD use USB type-C, which can deliver up to 100 W power.

USB PD implements a power rule, recommending four voltage levels at 5 V, 9 V, 15 V and 20 V. Sources supplying more than 15 W offer voltages of 5 V and 9 V, those supplying more than 27 W offer 5 V, 9 V and 15 V, and those supplying more than 45 W offer 5 V, 9 V, 15 V and 20 V. The maximum 100 W power supply is achieved with 20 V and up to 5 A, which requires a higher end cable to support such current, although all of the other voltage modes cap out at 3 A, depending on the required power.

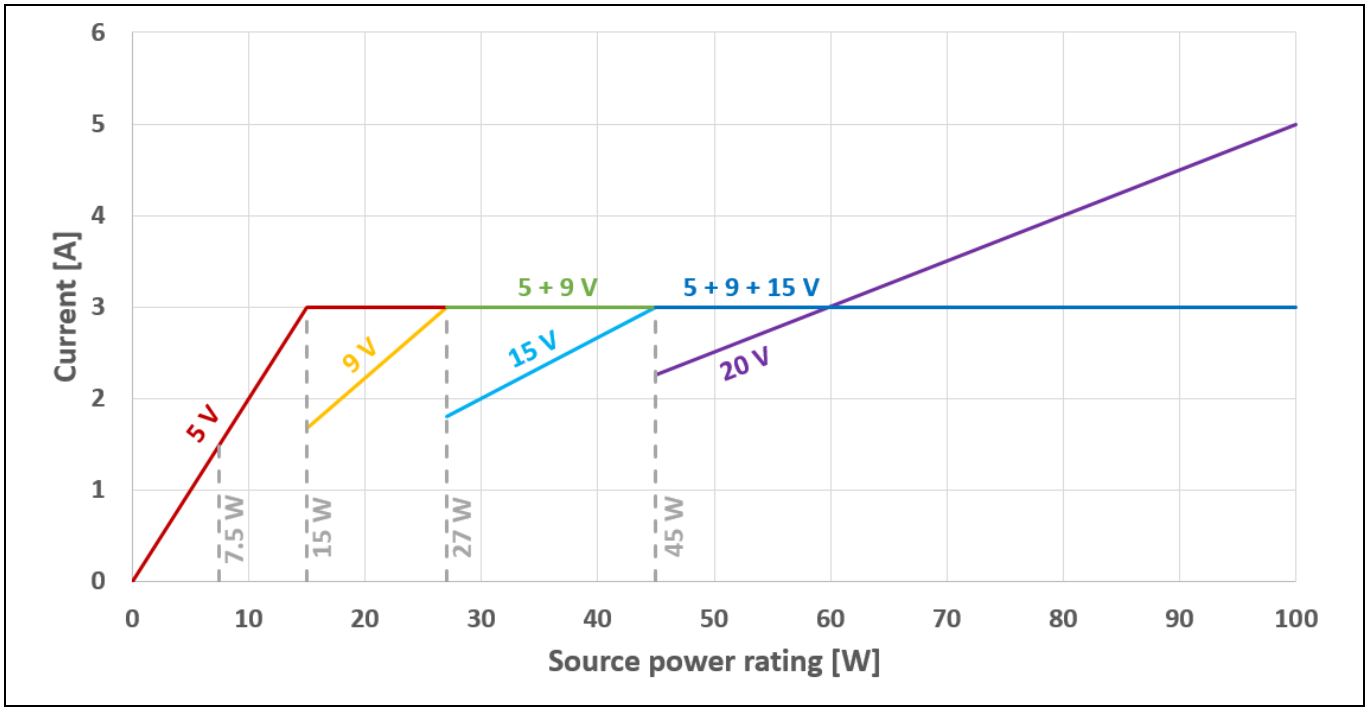


Figure 2 Output current against output power under different output voltages

1.2 High average efficiency and low standby power

In this reference design, **ICE5QSBG** was primarily chosen due to its digital frequency reduction switching scheme and active burst mode (ABM). Compared with a traditional QR flyback, the controller reduces its switching frequency by switching to the next valley (e.g., from first valley to eighth valley for low-line and third valley to tenth valley for high-line), thereby minimizing switching losses. Further reduction in load will trigger the controller to operate in ABM for a more efficient operation.

PAG1S is an integrated SR controller and charging port controller. PAG1S is designed to fit into a traditional primary-controlled flyback system with secondary-side sensing and regulation. PAG1S is targeted toward mobile power adapters, and it fits well into high-efficiency AC-DC flyback designs for USB PD, Qualcomm QC and other standard charging protocols. PAG1S also supports USB PD PPS mode.

In addition, the low switching losses introduced by the latest 700 V CoolMOS™ P7 **IPAN70R600P7S** in **TO-220** narrow-lead package and high-frequency switching OptiMOS™ **BSC070N10NS5** in **SuperSO8** package enable the charger to meet the highest efficiency standards and support high power density.

2 Reference board design

This document provides complete design details including specifications, schematics, bill of materials (BOM), PCB layout, and transformer design and construction information. Performance results pertaining to line/load regulation, efficiency, transient load, thermal conditions, conducted EMI scans and so on are also included.

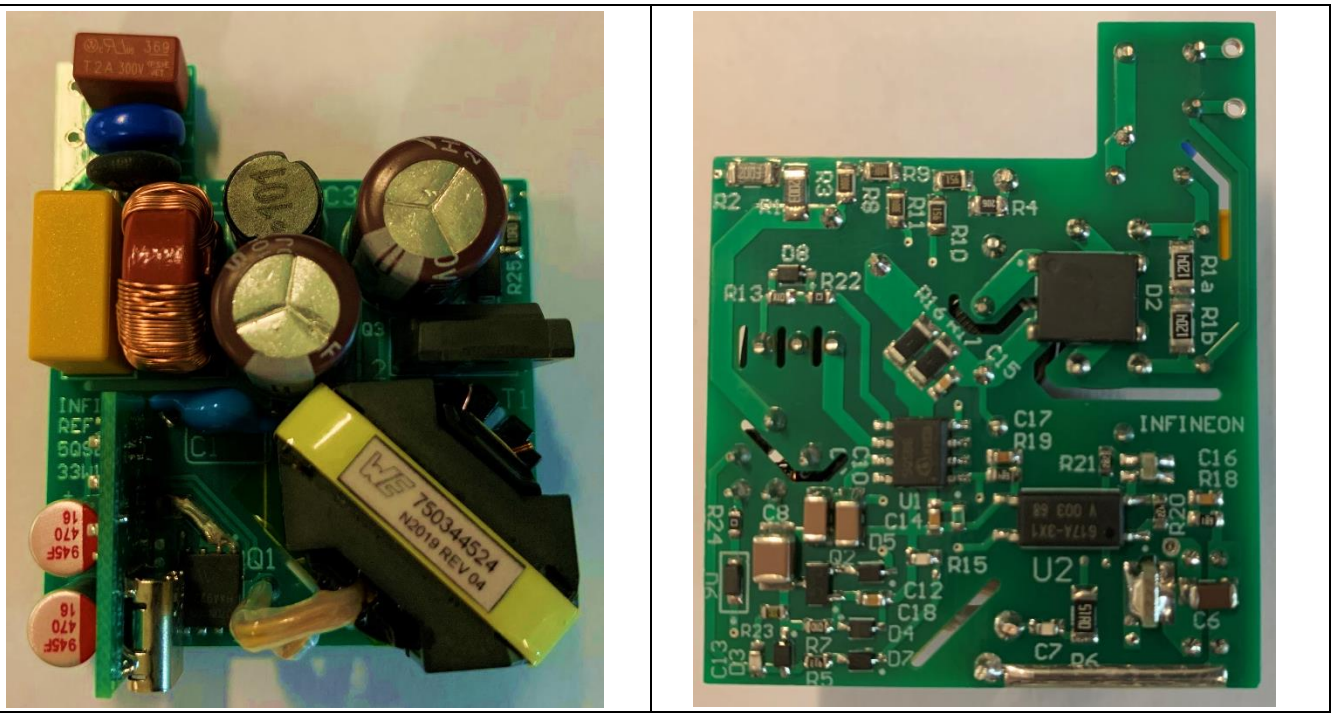


Figure 3 PCB

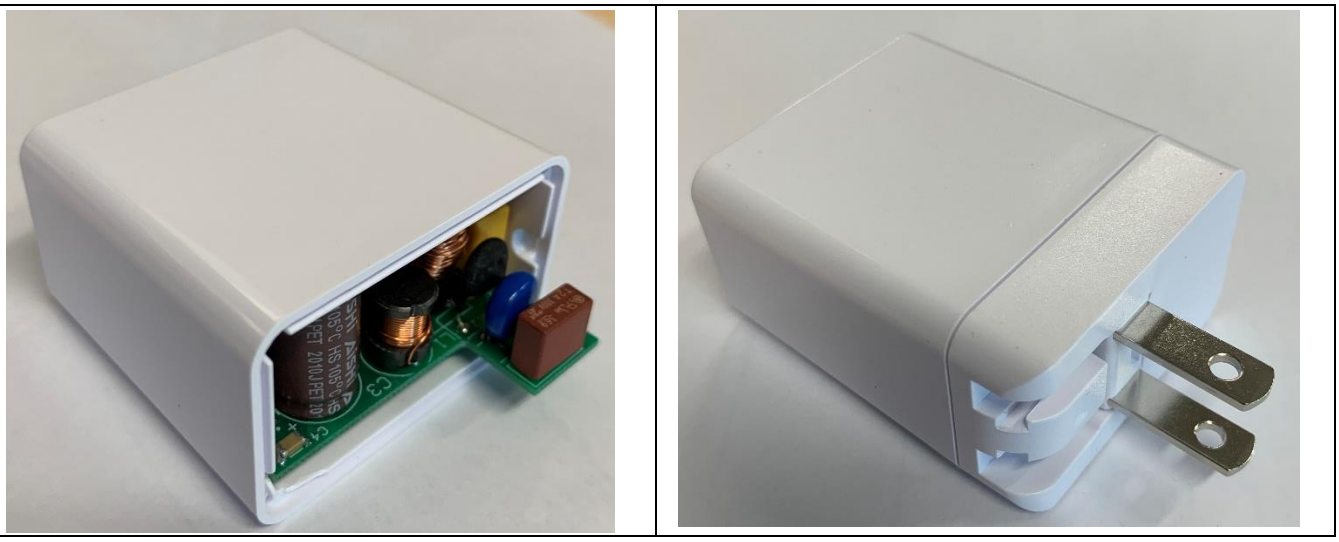


Figure 4 PCBA fitted in a case size of 54 x 45 x 28 mm (L x W x T), with foldable prongs

3 Power supply specifications

The table below represents the minimum acceptance performance of the design at 25°C ambient temperature. Actual results are listed in the measurements section.

Table 1 Specifications of REF_5QSBG_33W1

Description		Symbol	Min.	Typ.		Max.	Units	Comments
Input								
Voltage		V_{IN}	90	–		264	V AC	2-wire (no PE)
Frequency		f_{LINE}	47	50/60		63	Hz	
Standby power		P_{stby}	–	–		75	mW	230 V AC
Output Voltage and current	PD 3.0 mode		–	5/3	9/3	–	V/A	PPS: 3.3 to 5.9 V, 0 to 3 A
	PPS mode		3.3/3	–	–	11/3		PPS: 3.3 to 11 V, 0 to 3 A
	QC 2.0 mode		–	5/3	9/3	12/2.25		
Efficiency		η_{avg}	CoC Tier 2				%	
Output voltage accuracy			Less than ±5% (PD mode)				%	
Constant current accuracy			Less than ±150 (PPS mode)				mA	
Overcurrent protection (OCP)			Less than 130% of rated current				A	Latch-up
Overvoltage protection (OVP)			Less than 120% of V_{bus_set}				V	Latch-up
Undervoltage protection (UVP)			More than 70% of V_{bus_set}				V	Latch-up
Dynamic load		V_{dy}	Less than ±10% of V_{bus_set}				V	100 Hz, 0.4 A/µs
Ripple and noise voltage		V_{pk-pk}	Less than 3% of V_{bus_set} (20 MHz bandwidth)				mV	With 10 µF E-cap and 0.1 µF MLCC
Start-up time		t_{start_up}	–	–		500	ms	5 V output
Hold-up time		t_{hold_up}	10	–		–	ms	115 V AC, 27 W
Environmental								
Conducted EMI				6			dB	Margin, CISPR 22 class B
Surge immunity								
Differential mode (DM)				±1			kV	EN 61000-4-5
Ambient temperature		T_{amb}	-20	–		50	°C	Free convection, sea level
PCBA form factor			40 × 40 × 18				mm^3	L × W × H

4 Circuit diagram

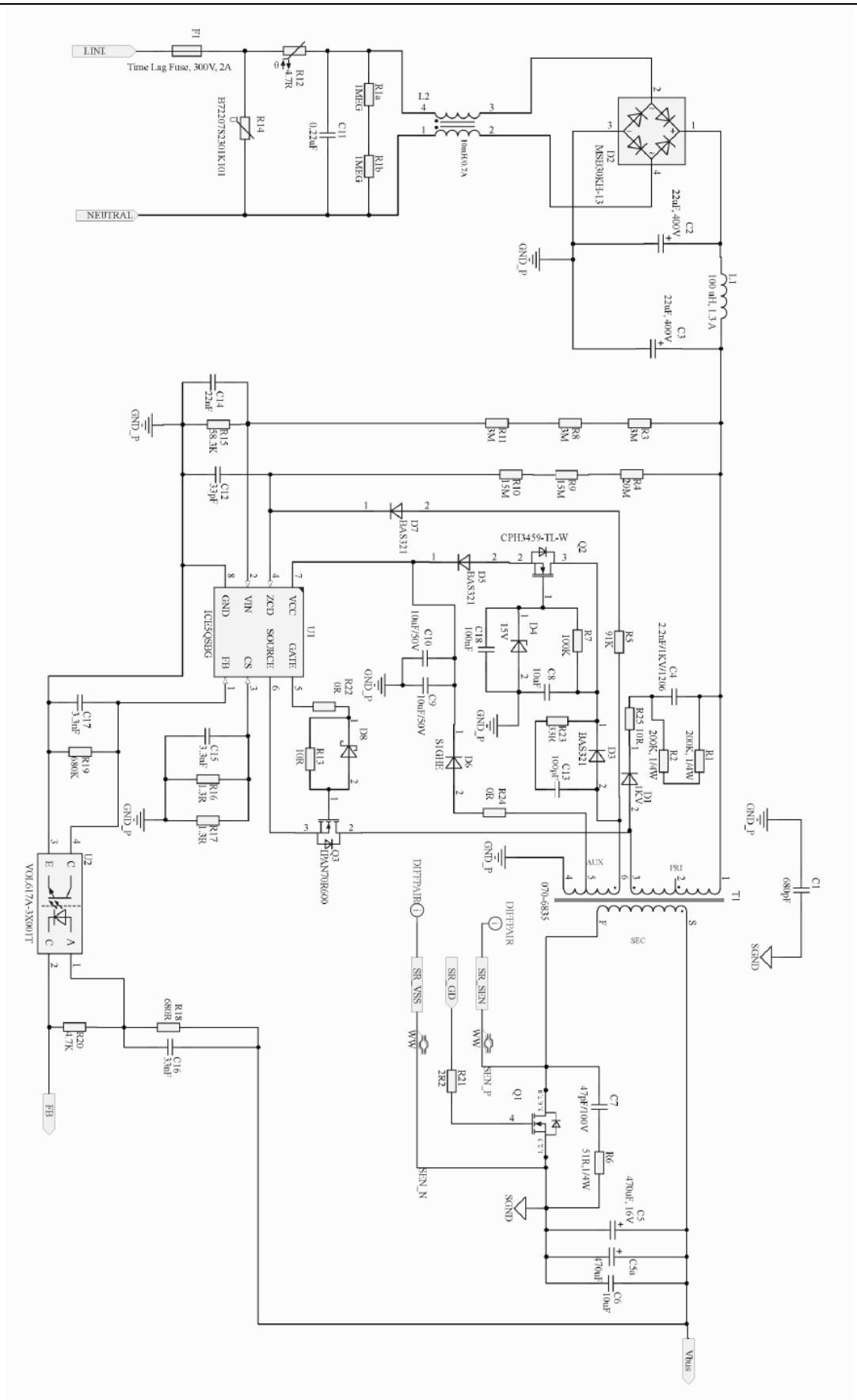


Figure 5 Schematic diagram of REF_5QSBG_33W1_M

Circuit diagram

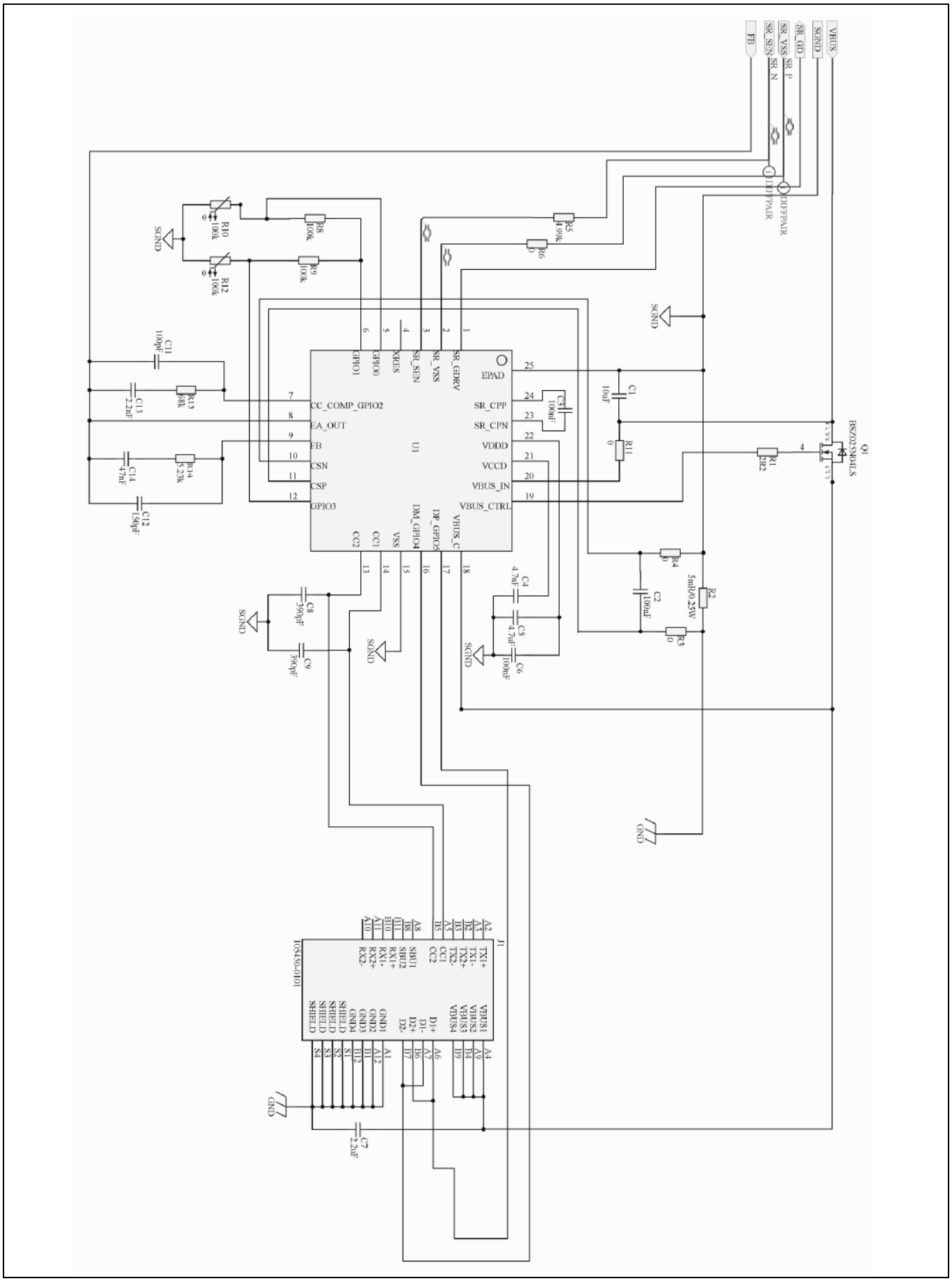


Figure 6 Schematic diagram of REF_5QSBG_33W1_D

5 Circuit description

In this section, the reference design circuit for the USB PD charger will be briefly described by the different functional blocks. For details of the design procedure and component selection for the flyback circuitry, please refer to the IC design guide [4] and calculation tool [5].

5.1 EMI filtering and line rectification

The input of the USB PD charger is taken from the AC power grid, which is in the range of 90 V AC ~ 264 V AC. The fuse F1 is directly connected to the input line to protect the system in case of excess current entering the system circuit due to any fault. Following is the thermistor R12, which is connected in series with F1 to reduce the inrush current, then the varistor R14, which is connected across the input to absorb excess energy during line surge transient. CM choke L2 together with π filter C2, L1 and C3 are filters to attenuate the DM and CM conducted EMI noise. The bridge rectifier D2 rectifies the AC input into DC voltage, filtered by the bulk capacitors C2 and C3.

5.2 Flyback converter power stage

The flyback converter power stage consists of transformer T1, a primary HV MOSFET Q3, secondary SR MOSFET Q1 and secondary output capacitors C5 and C5a.

When the HV MOSFET turns on, energy is stored in the transformer. When it turns off, the stored energy is discharged to the output capacitors and into the output load.

Secondary winding is sandwiched between two layers of primary winding to reduce leakage inductance. This improves efficiency and reduces voltage spikes.

For output rectification, the SR MOSFET is used to improve efficiency. Capacitors C5 and C5a store the energy needed during output load jumps, and help ensure low ESR.

5.3 Clamper circuit

A clamper network consisting of D1, C4, R1, R2 and R25 is used to reduce the switching voltage spikes across the drain pin of the HV MOSFET, which are generated from the leakage inductance of the transformer T1. This is a dissipative circuit, therefore R1, R2 and C4 need to be fine-tuned depending on the voltage derating factor and efficiency requirements.

5.4 Control of flyback converter through 5th generation QR controller ICE5QSBG

The **ICE5QSBG** controller is an eight-pin device in a DSO-8 package. It has been integrated with all necessary features and protections needed for a QR flyback controller.

5.4.1 Fast self-start-up and sustaining of V_{CC}

The IC uses a cascode structure to fast-charge the V_{CC} capacitor. Pull-up resistors R4, R9 and R10 connected to the multifunction zero crossing detection (ZCD) pin (pin 4) is used to initiate the start-up phase. At first, 0.2 mA is used to charge the V_{CC} capacitor from 0 V to 1.1 V. This is a protection which reduces the power dissipation of the power MOSFET during V_{CC} short-to-GND condition. Thereafter, a much higher charging current of 3.2 mA will charge the V_{CC} capacitor until the V_{CC_ON} is reached.

After start-up, the IC V_{CC} supply is sustained by the auxiliary winding of transformer T1, which needs to support the V_{CC} to be above undervoltage lockout (UVLO) voltage (10 V typ.) through two rectifier circuits.

5.4.2 QR switching with valley sensing

ICE5QSBG is a QR flyback controller which turns the HV MOSFET on at the lowest valley point of the drain voltage to minimize the switching losses. The IC senses the valley point through the ZCD pin (pin 4), which monitors auxiliary winding voltage through R5, D7 and C12 together with the internal resistor R_{ZCD}. When the ZCD voltage drops below 100 mV (typ.), the HV MOSFET switches on.

The IC employs digital frequency reduction to avoid the inherent increasing switching frequency of QR operation during load reduction. With **ICE5QSBG**, the HV MOSFET switches on from first to eighth valley for low-line or third to tenth valley for high-line.

5.4.3 Current sensing (CS)

The **ICE5QSBG** is a CM controller. The peak current is controlled cycle-by-cycle through the CS resistors R16 and R17 in the CS pin (pin 3). Transformer saturation can be avoided through peak current control (PCL), making the system better protected and more reliable.

5.4.4 Feedback (FB) and compensation network

V_{OUT} is sensed by PAG1S together with PD protocol integrated to switch between 3 V and 12 V output.

The FB pin of **ICE5QSBG** is a multifunction pin which is used to select the entry/exit burst power level through the resistor at the FB pin (R44) and also the burst-on/burst-off sense input during ABM.

5.4.5 System robustness and reliability through protection features

Protection is one of the major factors in determining whether the system is safe and robust – therefore sufficient protection is necessary. **ICE5QSBG** provides comprehensive protection to ensure the system is operating safely. This includes brown-in/brown-out, V_{IN} overvoltage (OV), V_{OUT} OV, V_{CC} OV and undervoltage (UV), open-loop/overload, overtemperature and V_{CC} short-to-GND. When those faults are found, the system will enter into protection mode. Once the fault is removed, the system resumes normal operation. A list of protections and failure conditions is shown in the table below.

PAG1S also supports configurable output OVP/UVP, and output overcurrent/short-circuit protection.

Table 2 Protection functions of ICE5QSBG

Protection function	Failure condition (typical values)	Protection mode
V_{CC} OV	V_{VCC} more than 25.5 V	Odd-skip auto restart
V_{CC} UV	V_{VCC} less than 10 V	Auto restart
V_{OUT} OV	V_{ZCD} more than 2 V for 10 consecutive pulses	Non-switch auto restart
V_{IN} OV	V_{VIN} more than 2.9 V	Non-switch auto restart
Brown-in/brown-out	V_{VIN_BI} less than 0.66 V/ V_{VIN_BO} less than 0.40 V	Non-switch auto restart
Open-loop/overload	V_{FB} more than 2.75 V and lasts for 30 ms	Odd-skip auto restart
Overtemperature	T_J more than 140°C (40°C hysteresis)	Non-switch auto restart
V_{CC} short-to-GND (V_{VCC} = 0 V, start-up = 50 MΩ and V_{DRAIN} = 90 V)	V_{VCC} less than 1.1 V, $I_{VCC_Charge1}$ ≈ -0.2 mA	Cannot start-up

5.5 Synchronous rectification

PAG1S is an integrated SR controller and charging port controller, which is good to drive an N-channel power MOSFET in a secondary output rectifier circuit. The MOSFET gate is switched on and off to bypass its body diode during the conduction period to minimize power dissipation, remaining off during the blocking period. The drain-to-source voltage is accurately sensed to determine the direction and magnitude of the current, allowing the PAG1S to turn the MOSFET on and off at close to zero current.

5.6 Output voltage configuration

The device connected on the output terminal communicates with the protocol IC to set the output voltage of the USB PD charger. The output connector is a USB type-C to support higher PD.

5.7 PCB design tips

For a good PCB design layout, there are several points to note.

- The switching power loop needs to be as small as possible (see **Figure 7**). There are two power loops in the reference design: one on the primary side and one on the secondary side. The primary-side loop starts from the bulk capacitor (C2/C3) positive terminal, primary transformer winding, primary MOSFET Q3, QR controller, CS resistors and back to the C4 negative terminal. The secondary-side loop starts at the secondary transformer winding, output capacitor C5/C5a, SR MOSFET Q1 and T1.

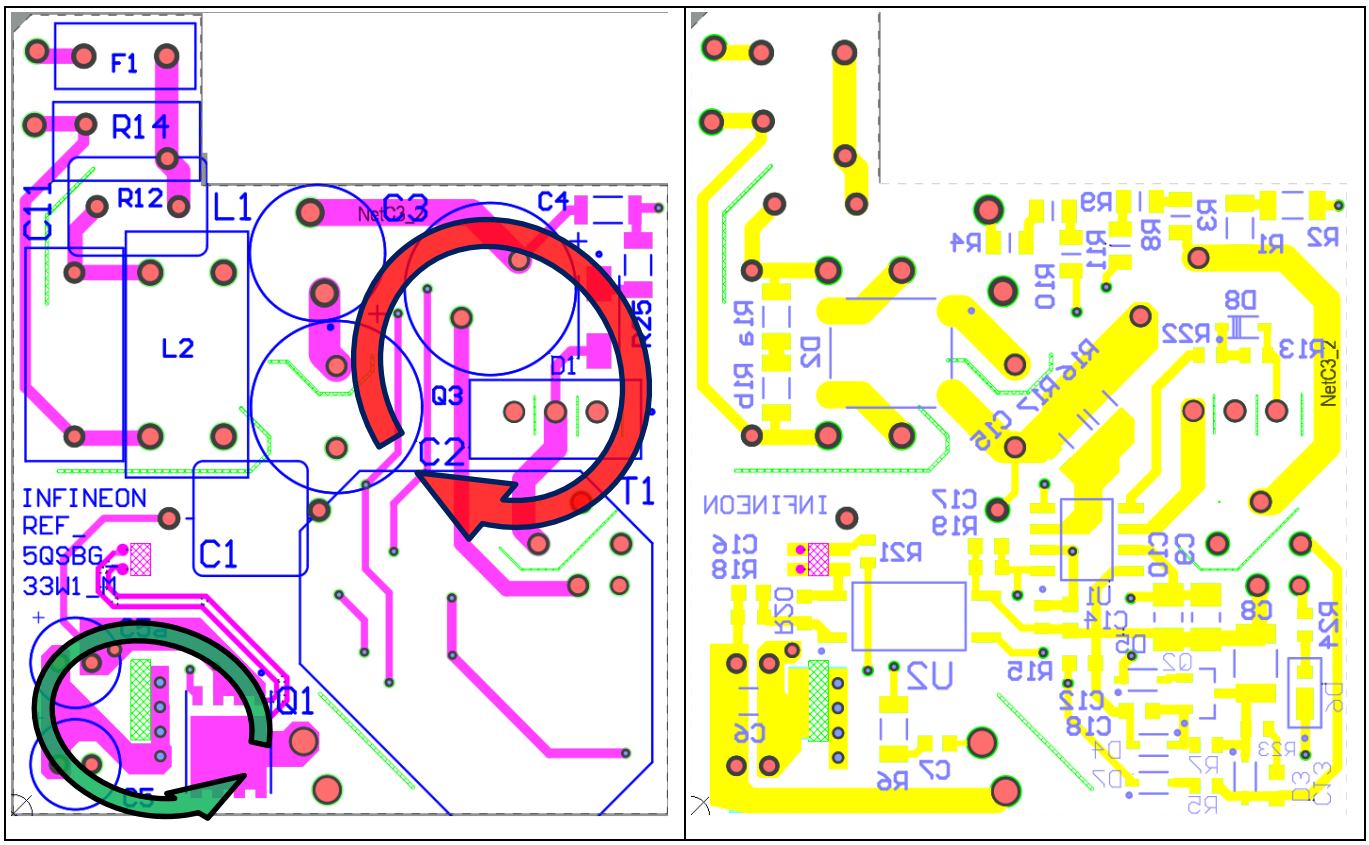


Figure 7 PCB layout tips

- Star-ground connection should be used to reduce HF noise coupling that can affect functional operation. The ground of the small-signal components, e.g., R15, C12, C17, R19, C14, and the emitter of the optocoupler (pin 3 of OPTO1) should connect directly to the IC ground (pin 8 of U1).
- Separating the HV components, e.g., the clamper circuit and the LV components, can reduce the spark-over chance of the high energy surge during ESD or a lightning surge test.
- Make the PCB copper pour on the DRAIN pin of the MOSFETs cover as wide an area as possible to act as a heatsink.

5.8 EMI reduction tips

EMI compliance is always a challenge for the power supply designer. There are several critical points to consider in order to achieve satisfactory EMI performance.

- A proper transformer design can significantly reduce EMI. Low leakage inductance can incur a low switching spike and HF noise. Interlaced winding is the most common technique to reduce leakage inductance. Winding shield, core shield and whole transformer shield are also among the techniques used to reduce EMI.
- Input CMC and X-capacitor greatly reduce EMI, but are costly and impractical, especially for low-power applications.
- Short-switching power-loop design in the PCB (as described in section 5.7) can reduce radiated EMI due to the antenna effect.
- The Y-capacitor CY1 dampens the HF noise generated between the primary and secondary, reducing the EMI noise.
- A secondary SR MOSFET snubber circuit (R6 and C7) can reduce HF noise.
- Ferrite beads can reduce HF noise especially on critical nodes such as the DRAIN pin of MOSFETs and clamper diodes. There is no ferrite bead used in this design, as this can reduce the efficiency due to additional losses, especially on MOSFETs.

6 PCB layout

6.1 Main board

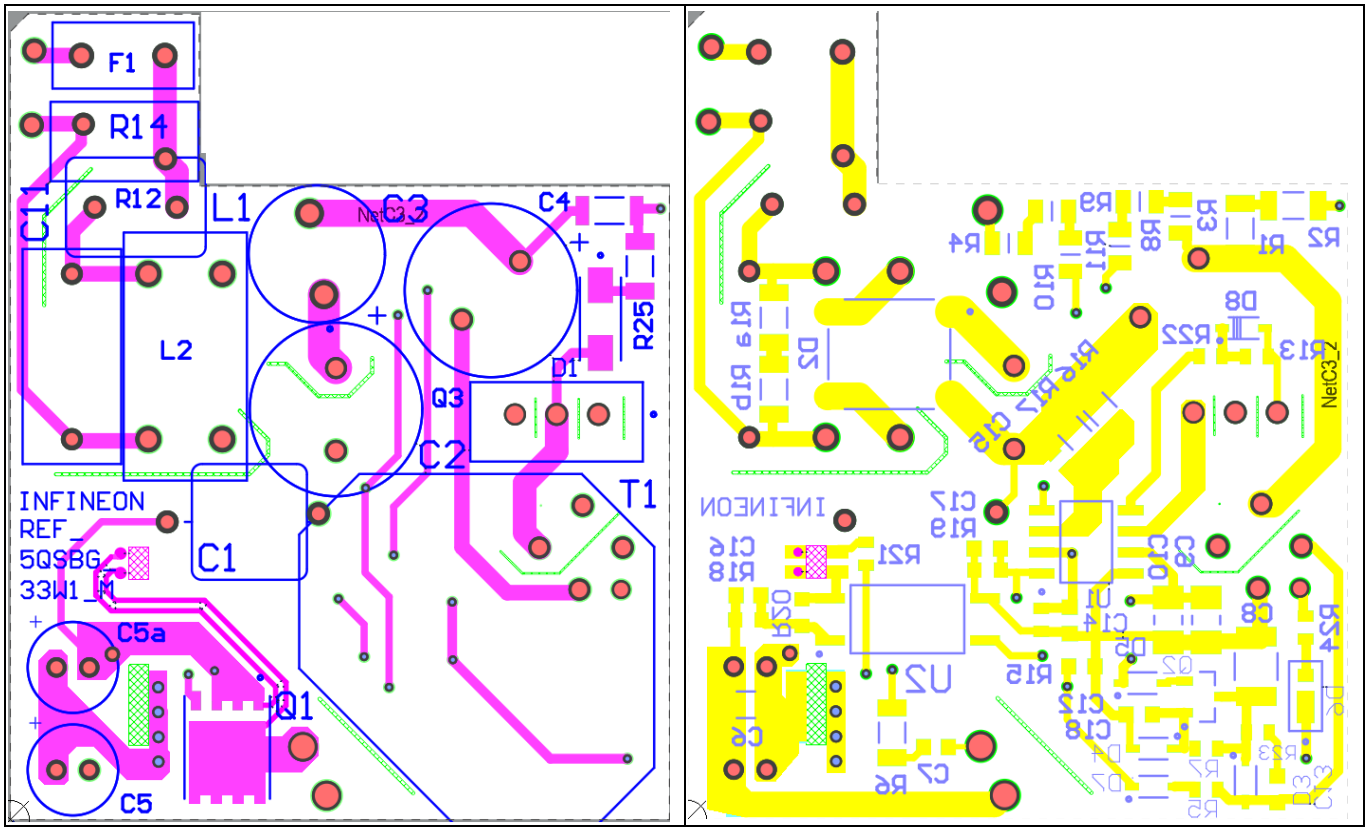


Figure 8 Main board top side (left) and bottom side (right) copper and component legend

6.2 Daughter board

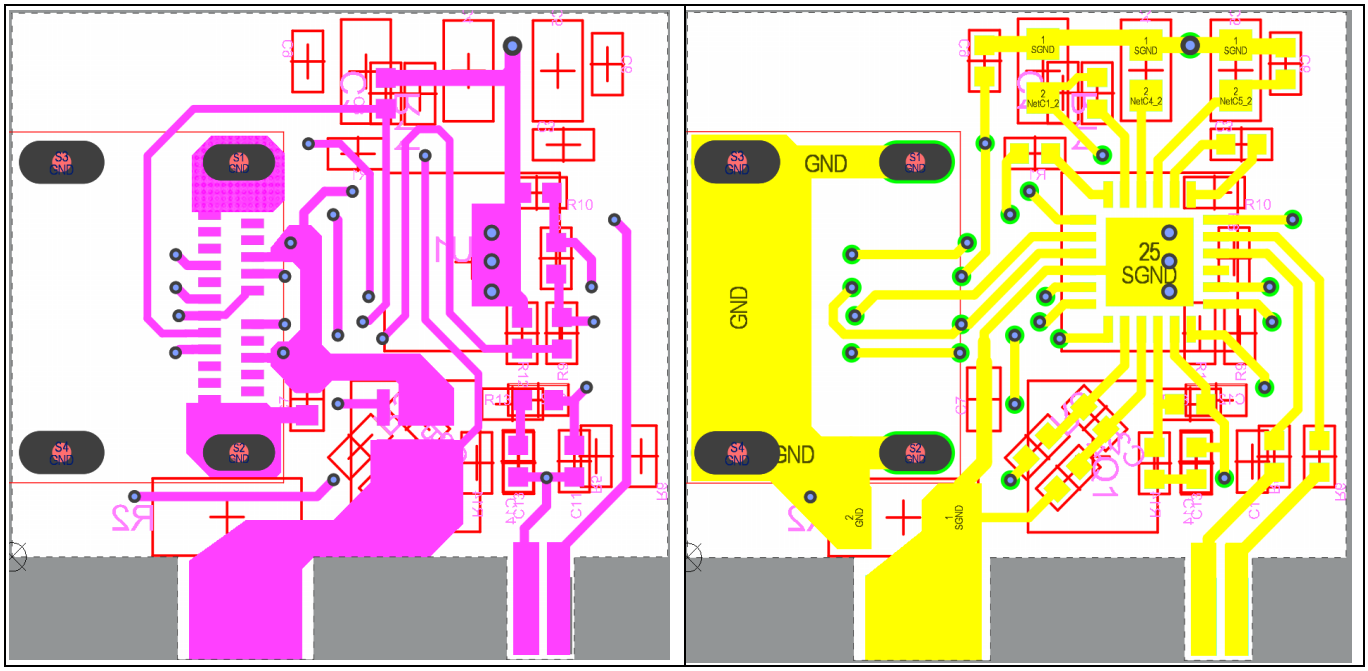


Figure 9 Daughter board top side (left) and bottom side (right) copper and component legend

7 Bill of materials (BOM)

Table 3 BOM

No.	Designator	Description	Part number	Manufacturer	Qty
1	C1	Safety capacitors 250 V AC 680 pF	DE1B3RA681KN4AN01F	Murata	1
2	C2, C3	Aluminum electrolytic capacitors 22 µF 400 V 20%	EHS2GM220G16OT	AiSHi	2
3	C4	MLCC – SMD/SMT 1206 2200 pF 1000 V X7R 10%	GRM31BR73A222KW01	Murata	1
4	C5, C5a	Aluminum polymer capacitors 470 µF 16 V 20%	SPF1CM471B11O00RAXXX	AiSHi	2
5	C6	MLCC – SMD/SMT 10.0 µF 16.0 V	C1206C106J4RAC	Kemet	1
6	C7	MLCC – SMD/SMT 100 V 47 pF 0603 C0G 5%			1
7	C8	MLCC – SMD/SMT 1210 100 V 4.7 µF X7S 10%	CGA6M3X7S2A475K200AE	TDK Corporation	1
8	C9, C10	MLCC – SMD/SMT 1206 50 V 4.7 µF X7R 10%	C3216X7R1H106K160AE	TDK Corporation	2
9	C11	Safety capacitors 0.22 µF 310 V 20% X2	MKP224K310VAC	KYET	1
10	C12	MLCC – SMD/SMT 0603 50 V 33 pF 10%			1
11	C13	MLCC – SMD/SMT 0603 100 V 100 pF 10%			1
12	C14	MLCC – SMD/SMT 0603 50 V 22 nF 10%			1
13	C15	MLCC – SMD/SMT 0603 50 V 3.3 nF 10%			1
14	C16	MLCC – SMD/SMT 0603 50 V 33 nF 10%			1
15	C17	MLCC – SMD/SMT 0603 50 V 4.7 nF 10%			1
16	C18	MLCC – SMD/SMT 50 V 0.1 µF X7R 0603 10%			1
17	D1	Standard recovery diode 1 kV 1 A, single	S1M	ON Semiconductor	1
18	D2	Bridge rectifier single phase 1 kV 3 A SMD	MSB30M-13	Diodes	1
19	D3, D5, D7, D8	Diode 200 V 250 MA SOD-323	BAS321	Nexperia	4
20	D6	Standard diode 400 V 1 A SMD SOD-323HE	S1GHE	ON Semiconductor	1
21	D4	Zener single diode 15 V SOD-323	BZX384-C15,115	Nexperia	1
22	F1	Time-lag fuse 300 V 2 A	36912000000	Littelfuse	1
23	L1	Radial leaded wire-wound inductor WE-TI size 8095 100 µH 1.3 A	7447720101	Würth Elektronik	1
24	L2	WE-CMB CM power line choke type XS 10 mH 0.7 A 250 V	744821110	Würth Elektronik	1
25	Q1	MOSFET N-channel 100 V 80 A TDSON-8	BSC070N10NS5	Infineon	1

26	Q2	MOSFET N-channel 200 V 500 mA 2.8 Ω SOT-23	CPH3459-TL-W	ON Semiconductor	1
27	Q3	MOSFET N-channel 700 V 8.5 A TO220-FP	IPAN70R600P7S	Infineon	1
28	R1, R2	Thick-film resistors – SMD 1206 200 kΩ 1%			2
29	R1a, R1b	Thick-film resistors – SMD 1206 1.2 MΩ 5%			2
30	R3, R8, R11	Thick-film resistors – SMD 0805 3 MΩ 5%			3
31	R9, R10	Thick-film resistors – SMD 0805 15 MΩ 5%			2
32	R4	Thick-film resistors – SMD 0805 20 MΩ 5%			1
33	R5	Thick-film resistors – SMD 0603 91 kΩ 1%			1
34	R6	Thick-film resistors – SMD 1206 51 Ω 1%			1
35	R7	Thick-film resistors – SMD 0603 100 kΩ 1%			1
36	R12	NTC 4.7 Ω -20% to +20% radial leaded	B57153S0479M000	TDK Corporation	1
37	R13	Thick-film resistors – SMD 0603 91 Ω 1%			1
38	R14	SIOV metal oxide varistor	B72207S2301K101	Epcos	1
39	R15	Thin-film resistors – SMD 0603 58.3 KΩ 1%			1
40	R16, R17	Thick-film resistors – SMD 1R3 1% 0.25 W 1206			1
41	R18	Thin-film resistors – SMD 0603 680 Ω 1%			1
42	R19	Thin-film resistors – SMD 0603 680 KΩ 1%			1
43	R20	Thin-film resistors – SMD 0603 4700 Ω 1%			1
44	R21	Thick-film resistors – SMD 1/10 W 2.2 Ω 1%			1
45	R23	Thin-film resistors – SMD 0603 33 Ω 1%			1
46	R22, R24	Thick-film resistors – SMD 0 R 0.1 W 0603			2
47	R25	Thick-film resistors – SMD 1206 10 Ω 1%			1
48	T1	Transformer THT vertical RM-style bobbins RM8		Würth Elektronik	1
49	U1	QR PWM controller	ICE5QSBG	Infineon	1
50	U2	Optocoupler	VOL617A-3X001T	Vishay	1

Table 4 Daughter board list

No.	Designator	Description	Part number	Manufacturer	Qty
1	C1	MLCC – SMD/SMT 0603 16 V DC 10 µF X5R 10%			1
2	C2, C3, C6	MLCC – SMD/SMT 16 V 0.1 µF X7R 0402 10%			3
3	C4, C5	MLCC – SMD/SMT 0603 25 V DC 4.7 µF X5R 10%			2
4	C7	MLCC – SMD/SMT 0402 25 V DC 2.2 µF 10% X5R			1
5	C8, C9	MLCC – SMD/SMT 390 pF 50 V C0G 5% 0402			2
6	C11	MLCC – SMD/SMT 100 pF 50 V C0G 5% 0402			1
7	C12	MLCC – SMD/SMT 150 pF 50 V C0G 5% 0402			1
8	C13	MLCC – SMD/SMT 0402 25 V DC 2.2 nF 10% X5R			1
9	C14	MLCC – SMD/SMT 0402 25 V DC 47 nF 10% X5R			1
10	J1	USB connectors USB type-C recep. R/A top-mounted	105450-0101	Molex	1
11	Q1	OptiMOS™ power – N-channel 40 A 40 V 2 mΩ	BSZ025N04LS	Infineon	1
12	R1	Thick-film resistors – SMD 0402 2.2 Ω 5%			1
13	R2	Resistors – SMD 1/4 W 0.005 Ω 1%		Vishay	1
14	R3, R4, R6, R11	Thick-film resistors – SMD 0402 0 Ω			4
15	R5	Thick-film resistors – SMD 0402 4.99 kΩ 1%			1
16	R8, R9	Thick-film resistors – SMD 100 kΩ 1% 1/16 W			2
17	R10, R12	Thermistors 0402 100 kΩ 1% NTC			2
18	R13	Thin-film resistors – SMD 68 kΩ 1% 0402			1
19	R14	Thick-film resistors – SMD 1/16 W 5.23 kΩ 1%			1
20	U1	USB PD power adapter SR controller	CYPD3184A1-24LQXQ	Cypress	1

8 Transformer specification

Core: RM8, TP4A

Bobbin: 10-terminal EXT, THT, vertical

Primary inductance: L_P = 400 µH (±10 percent), measured between pin 1 and pin 3

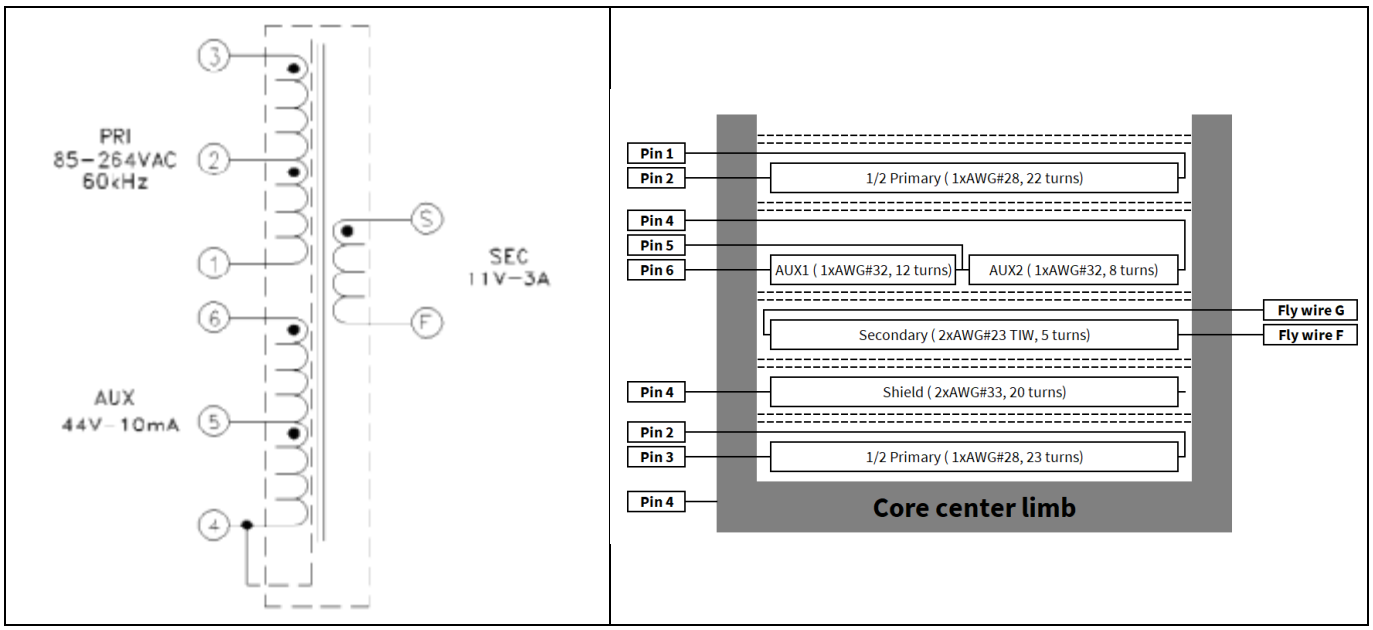


Figure 10 Transformer structure

9 Measurement data and graphs

All measurements are tested at 25°C room temperature and taken at the PCB end. ArteZ USB PD tester is used to configure the output voltage. Standby power is measured by a Yokogawa power meter WT210 with integrated testing of one minute.

Table 5 Standby power measurements

Input (V AC/Hz)	Loading	P_{IN} (mW)	Criteria	Remark
115 V AC/60 Hz	0% load	35	Less than 75 mW	No USB sink attached
230 V AC/50 Hz	0% load	53	Less than 75 mW	

Table 6 3.3 V output electrical measurements

Input (V AC/Hz)	Loading	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)
90 V AC/ 60 Hz	10% load	1.178	3.300	0.2981	0.98	83.51%	
	25% load	2.869	3.296	0.7498	2.47	86.13%	86.89%
	50% load	5.644	3.290	1.4950	4.92	87.15%	
	75% load	8.461	3.283	2.2465	7.38	87.17%	
	100% load	11.270	3.277	2.9956	9.82	87.10%	
115 V AC/ 60 Hz	10% load	1.148	3.300	0.2943	0.97	84.57%	
	25% load	2.829	3.296	0.7453	2.46	86.84%	87.56%
	50% load	5.568	3.290	1.4950	4.92	88.34%	
	75% load	8.383	3.283	2.2465	7.38	87.98%	
	100% load	11.270	3.277	2.9956	9.82	87.10%	
230 V AC/ 50 Hz	10% load	1.230	3.300	0.2994	0.99	80.33%	
	25% load	2.906	3.296	0.7453	2.46	84.52%	86.25%
	50% load	5.650	3.290	1.4950	4.92	87.06%	
	75% load	8.516	3.283	2.2500	7.39	86.74%	
	100% load	11.278	3.277	2.9827	9.77	86.67%	
264 V AC/ 50 Hz	10% load	1.250	3.300	0.2994	0.99	79.04%	
	25% load	2.990	3.296	0.7453	2.46	82.16%	85.20%
	50% load	5.702	3.290	1.4950	4.92	86.26%	
	75% load	8.595	3.283	2.2500	7.39	85.94%	
	100% load	11.310	3.277	2.9827	9.77	86.42%	

Table 7 5 V output electrical measurements

Input (V AC/Hz)	Loading	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)
90 V AC/ 60 Hz	10% load	1.720	5.096	0.2944	1.50	87.22%	
	25% load	4.316	5.092	0.7456	3.80	87.97%	88.43%
	50% load	8.562	5.086	1.4950	7.60	88.81%	
	75% load	12.876	5.080	2.2465	11.41	88.63%	
	100% load	17.210	5.073	2.9956	15.20	88.30%	
115 V AC/ 60 Hz	10% load	1.726	5.096	0.2944	1.50	86.94%	
	25% load	4.335	5.092	0.7456	3.80	87.58%	88.78%
	50% load	8.520	5.086	1.4950	7.60	89.24%	
	75% load	12.790	5.080	2.2465	11.41	89.23%	
	100% load	17.056	5.072	2.9956	15.19	89.08%	
230 V AC/ 50 Hz	10% load	1.812	5.096	0.2944	1.50	82.80%	
	25% load	4.547	5.092	0.7456	3.80	83.50%	87.14%
	50% load	8.655	5.086	1.4950	7.60	87.85%	
	75% load	12.910	5.080	2.2465	11.41	88.40%	
	100% load	17.105	5.072	2.9956	15.19	88.83%	
264 V AC/ 50 Hz	10% load	1.844	5.096	0.2944	1.50	81.36%	
	25% load	4.520	5.092	0.7456	3.80	84.00%	86.68%
	50% load	8.747	5.086	1.4950	7.60	86.93%	
	75% load	13.001	5.080	2.2465	11.41	87.78%	
	100% load	17.263	5.072	2.9956	15.19	88.01%	

Table 8 9 V output electrical measurements

Input (V AC/Hz)	Loading	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)
90 V AC/ 60 Hz	10% load	3.078	9.054	0.2943	2.66	86.57%	
	25% load	7.605	9.050	0.7457	6.75	88.74%	88.75%
	50% load	15.209	9.043	1.4956	13.52	88.93%	
	75% load	22.846	9.037	2.2465	20.30	88.86%	
	100% load	30.580	9.030	2.9956	27.05	88.46%	
115 V AC/ 60 Hz	10% load	3.070	9.054	0.2943	2.66	86.79%	
	25% load	7.577	9.050	0.7457	6.75	89.07%	89.70%
	50% load	15.032	9.043	1.4950	13.52	89.94%	
	75% load	22.555	9.037	2.2465	20.30	90.01%	
	100% load	30.127	9.030	2.9956	27.05	89.79%	
230 V AC/ 50 Hz	10% load	3.180	9.054	0.2943	2.66	83.79%	
	25% load	7.770	9.050	0.7457	6.75	86.85%	89.33%

Measurement data and graphs

Input (V AC/Hz)	Loading	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)
	50% load	15.053	9.043	1.4956	13.52	89.85%	
	75% load	22.500	9.037	2.2465	20.30	90.23%	
	100% load	29.932	9.030	2.9956	27.05	90.37%	
264 V AC/ 50 Hz	10% load	3.220	9.054	0.2943	2.66	82.75%	
	25% load	7.877	9.050	0.7457	6.75	85.68%	88.75%
	50% load	15.144	9.043	1.4956	13.52	89.31%	
	75% load	22.580	9.037	2.2465	20.30	89.91%	
	100% load	30.020	9.030	2.9956	27.05	90.11%	

Table 9 11 V output electrical measurements

Input (V AC/Hz)	Loading	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)
90 V AC/ 60 Hz	10% load	3.794	10.960	0.2950	3.23	85.21%	
	25% load	9.204	10.960	0.7456	8.17	88.79%	88.78%
	50% load	18.344	10.950	1.4950	16.37	89.24%	
	75% load	27.600	10.940	2.2465	24.58	89.05%	
	100% load	37.212	10.940	2.9953	32.77	88.06%	
115 V AC/ 60 Hz	10% load	3.791	10.960	0.2950	3.23	85.29%	
	25% load	9.163	10.960	0.7456	8.17	89.18%	89.82%
	50% load	18.169	10.950	1.4953	16.37	90.12%	
	75% load	27.289	10.940	2.2465	24.58	90.06%	
	100% load	36.444	10.940	2.9956	32.77	89.92%	
230 V AC/ 50 Hz	10% load	3.869	10.960	0.2945	3.23	83.43%	
	25% load	9.336	10.960	0.7456	8.17	87.53%	89.47%
	50% load	18.304	10.950	1.4953	16.37	89.46%	
	75% load	27.252	10.940	2.2465	24.58	90.18%	
	100% load	36.120	10.940	2.9956	32.77	90.73%	
264 V AC/ 50 Hz	10% load	3.950	10.960	0.2950	3.23	81.84%	
	25% load	9.452	10.960	0.7456	8.17	86.45%	88.88%
	50% load	18.394	10.950	1.4950	16.37	89.00%	
	75% load	27.438	10.944	2.2465	24.59	89.60%	
	100% load	36.234	10.940	2.9956	32.77	90.45%	

Table 10 12 V output electrical measurements

Input (V AC/Hz)	Loading	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)	Average efficiency (%)
90 V AC/ 60 Hz	10% load	3.050	12.063	0.2128	2.57	84.16%	
	25% load	7.700	12.060	0.5606	6.76	87.80%	88.69%
	50% load	15.108	12.054	1.1146	13.44	88.93%	
	75% load	22.679	12.050	1.6768	20.21	89.09%	
	100% load	30.419	12.044	2.2465	27.06	88.95%	
115 V AC/ 60 Hz	10% load	3.098	12.063	0.2128	2.57	82.86%	
	25% load	7.684	12.060	0.5606	6.76	87.99%	89.46%
	50% load	14.982	12.054	1.1146	13.44	89.68%	
	75% load	22.447	12.050	1.6768	20.21	90.01%	
	100% load	30.010	12.044	2.2465	27.06	90.16%	
230 V AC/ 50 Hz	10% load	3.154	12.063	0.2128	2.57	81.40%	
	25% load	7.880	12.060	0.5606	6.76	85.80%	88.97%
	50% load	15.025	12.054	1.1146	13.44	89.42%	
	75% load	22.386	12.050	1.6768	20.21	90.26%	
	100% load	29.927	12.044	2.2465	27.06	90.41%	
264 V AC/ 50 Hz	10% load	3.180	12.063	0.2128	2.57	80.72%	
	25% load	7.970	12.060	0.5606	6.76	84.83%	88.19%
	50% load	15.188	12.054	1.1146	13.44	88.46%	
	75% load	22.600	12.050	1.6768	20.21	89.40%	
	100% load	30.040	12.044	2.2465	27.06	90.07%	

Table 11 Efficiency summary

Parameter	Test condition	Criteria	Test result	
		Minimum	115 V AC/60 Hz	230 V AC/50 Hz
CoC Version 5 Tier 2 four-point average efficiency (average of 25%, 50%, 75%, 100% load)	V_{OUT} = 3.3 V DC, I_{OUT} = 3 A	78.19%	87.56%	86.25%
	V_{OUT} = 5 V DC, I_{OUT} = 3 A	81.76%	88.78%	87.14%
	V_{OUT} = 9 V DC, I_{OUT} = 3 A	87.30%	89.70%	89.33%
	V_{OUT} = 11 V DC, I_{OUT} = 3 A	88.03%	89.82%	89.47%
	V_{OUT} = 12 V DC, I_{OUT} = 2.25 A	87.30%	89.46%	88.97%
CoC Version 5 Tier 2 10% load efficiency	V_{OUT} = 3.3 V DC, I_{OUT} = 0.3 A	68.98%	84.57%	80.33%
	V_{OUT} = 5 V DC, I_{OUT} = 0.3 A	72.48%	86.94%	82.80%
	V_{OUT} = 9 V DC, I_{OUT} = 0.3 A	77.30%	86.79%	83.79%
	V_{OUT} = 11 V DC, I_{OUT} = 0.3 A	78.03%	85.29%	83.43%
	V_{OUT} = 12 V DC, I_{OUT} = 0.225 A	77.30%	82.86 %	80.72%

9.1 Efficiency curves

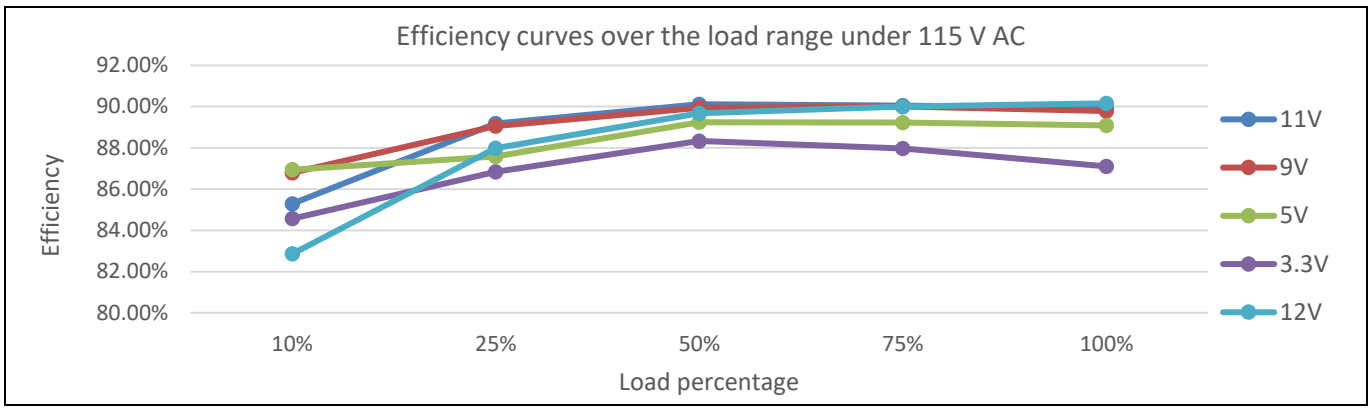


Figure 11 Efficiency curves over the load range under 115 V AC

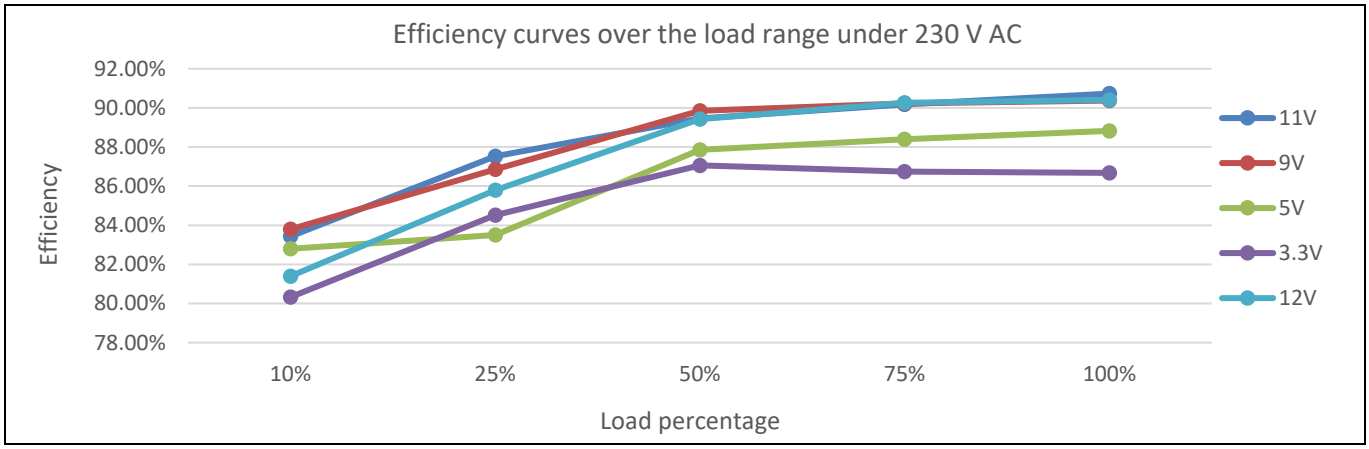


Figure 12 Efficiency curves over the load range under 230 V AC

9.2 Line and load regulation

The steady-state output regulation is verified under various loadings and different input voltages, which passes ±5 percent specification.

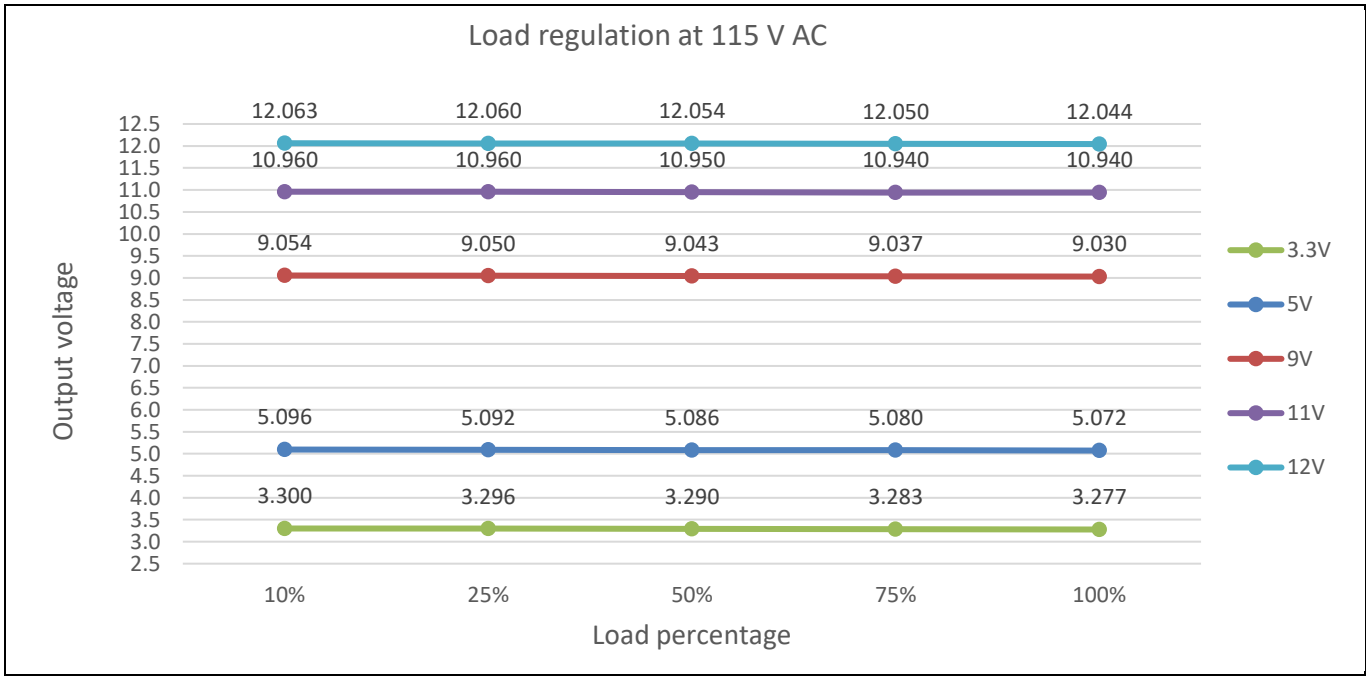


Figure 13 Load regulation at 115 V AC line input voltage

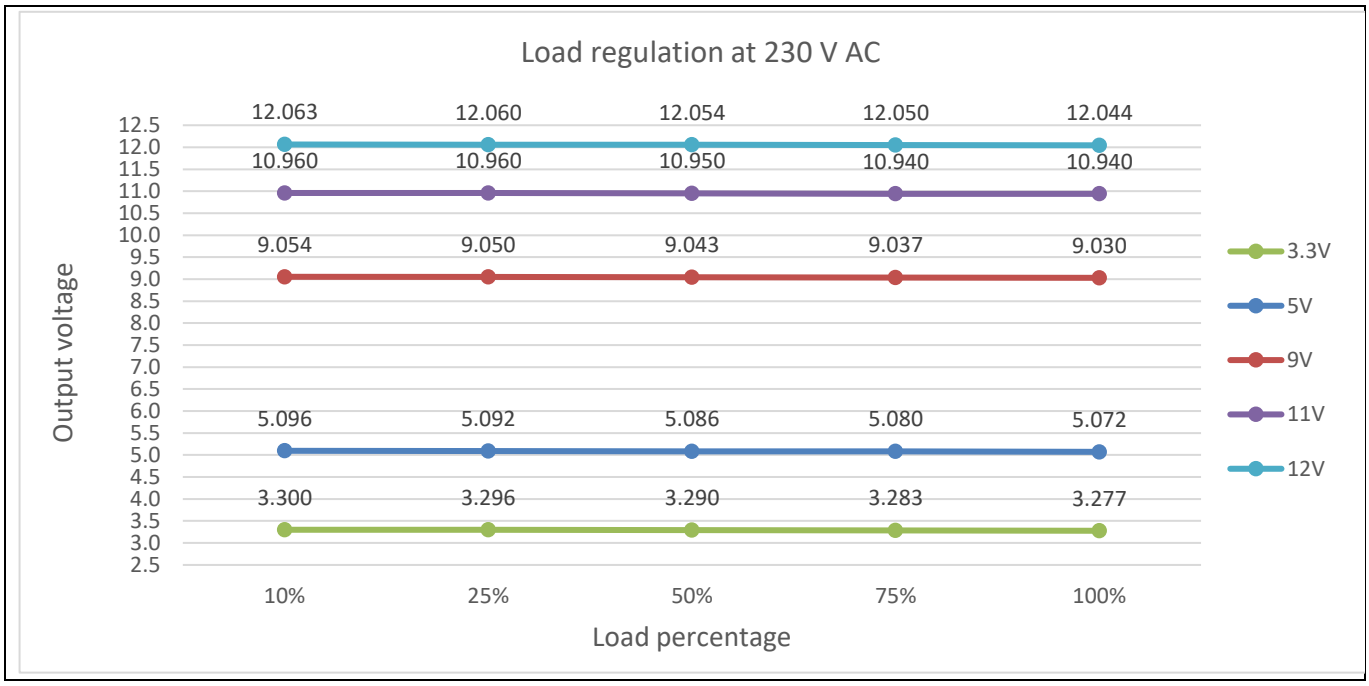


Figure 14 Load regulation at 230 V AC line input voltage

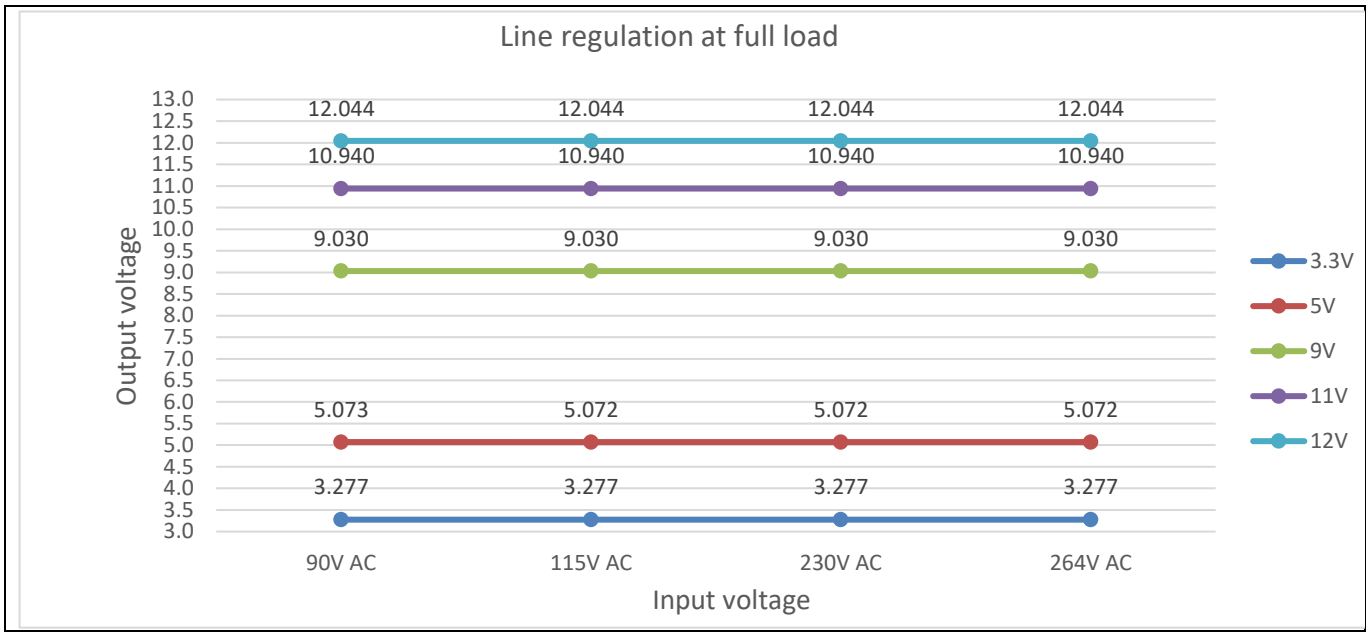


Figure 15 Line regulation at 100 percent load

9.3 PPS compatible mode

Constant current (CC) mode current limitation function is tested by E-load under CR mode; set device under test (DUT) to PPS mode and then increase current (by reducing R) to verify CC-CV curve.

Table 12 PPS mode constant current

Mode	V_{OUT} (V)	V_{IN_AC} (V/Hz)	I_{OUT_CC} (A)	Requirement (A)
PPS	3.3	90/60	3.021	2.85 ~ 3.15 (less than ±150 mA of rated output current)
		264/50	3.022	
	5.9	90/60	3.022	
		264/50	3.021	
	11	90/60	3.022	
		264/50	3.021	

9.4 Surge immunity (EN 61000-4-5)

The reference board was subjected to a surge immunity test (±1 kV DM) according to EN 61000-4-5. It was tested at 11 V full load (33 W) using resistive load (3.6 Ω) at an input voltage of 230 V AC. Output GND was connected to PE during testing. A test failure was defined as a non-recoverable and/or system auto restart.

Table 13 System surge immunity test results

Description	Test	Level		Number of strikes				Test result
				0°	90°	180°	270°	
230 V AC, 33 W ($3.6\ \Omega\ R_{LOAD}$)	DM	+1 kV	L → N	3	3	3	3	Pass
		-1 kV	L → N	3	3	3	3	Pass

9.5 Conducted emissions (EN 55022 class B)

The conducted EMI (CEMI) was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The reference board was tested at 11 V full load using resistive load at an input voltage of 115 V AC and 230 V AC with more than 6 dB margin.

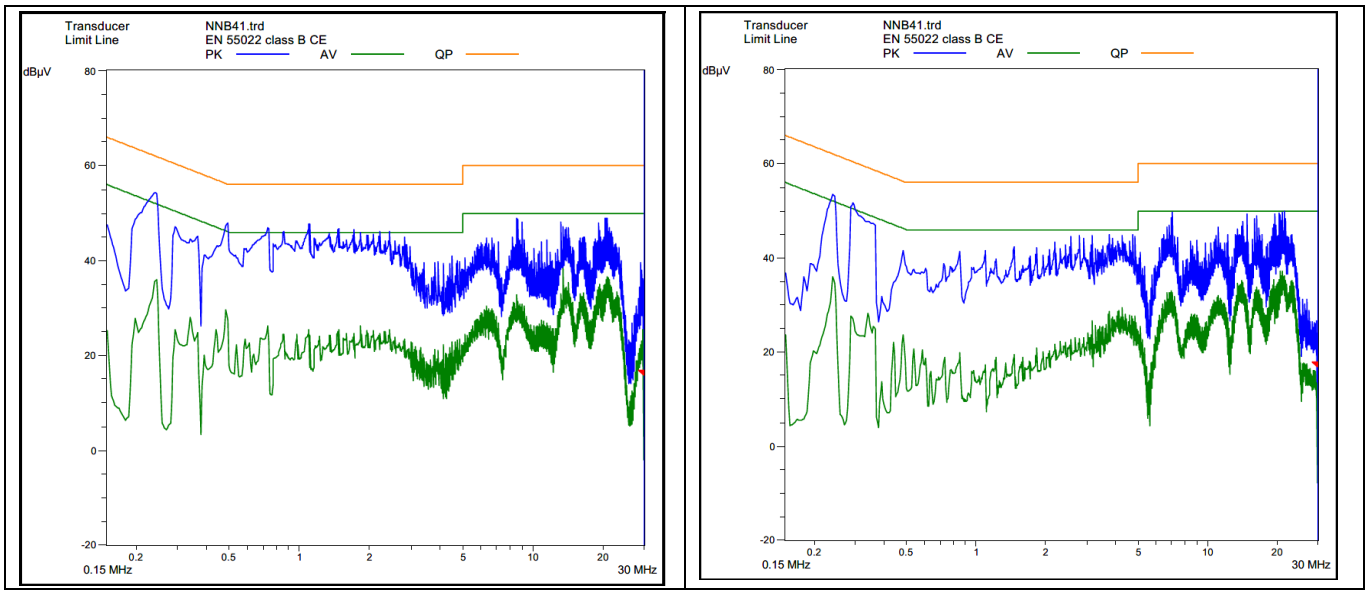


Figure 16 Conducted emissions on line (left) and neutral (right) at 115 V AC and full load

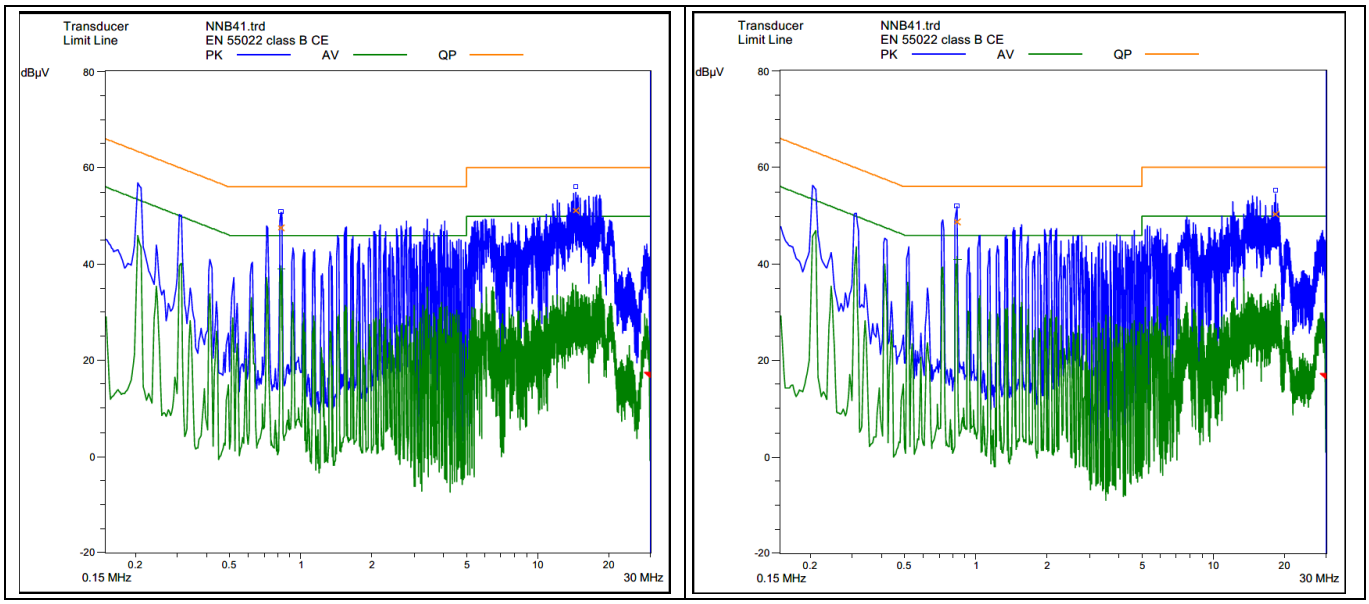


Figure 17 Conducted emissions on line (left) and neutral (right) at 230 V AC and full load

9.6 Thermal measurements

Thermal measurements were taken using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C, after one hour running at full load, 33 W. The component temperatures were taken in an open-frame setup.

Table 14 11 V output thermal measurements on components (open-frame)

No.	Components	Temperature at 90 V AC (°C)	Temperature at 264 V AC (°C)
1	Q1 (SR MOSFET)	83.6	81.9
2	T1 (transformer)	78.4	76.2
3	U1 (ICE5QSBG)	85.2	64.8
4	Q3 (primary MOSFET)	83.6	78.9
5	D2 (diode bridge)	95.5	64.9

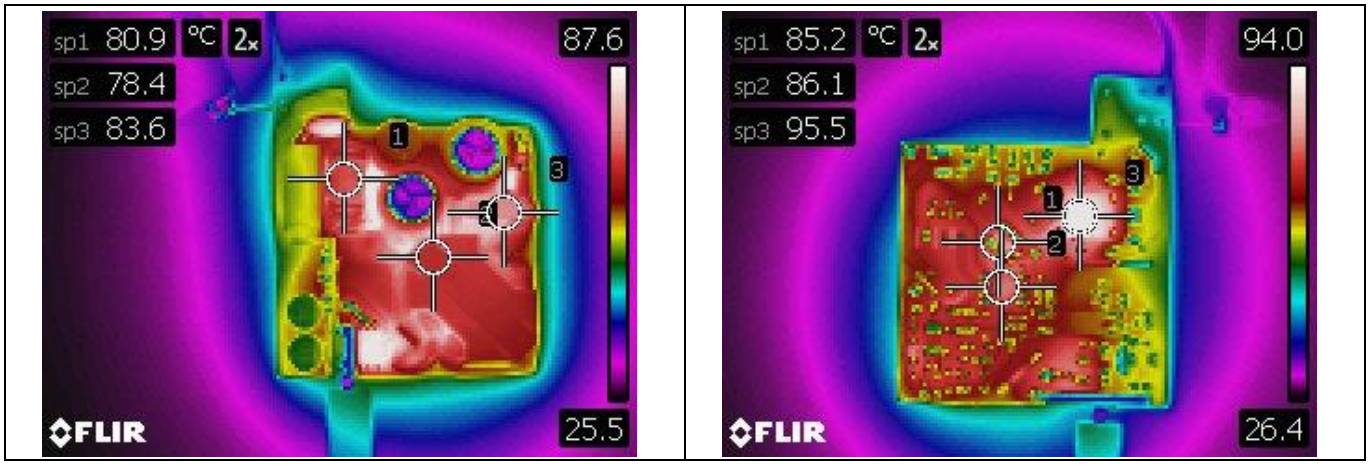


Figure 18 Top layer (left) and bottom layer (right) thermal image at 90 V AC input voltage

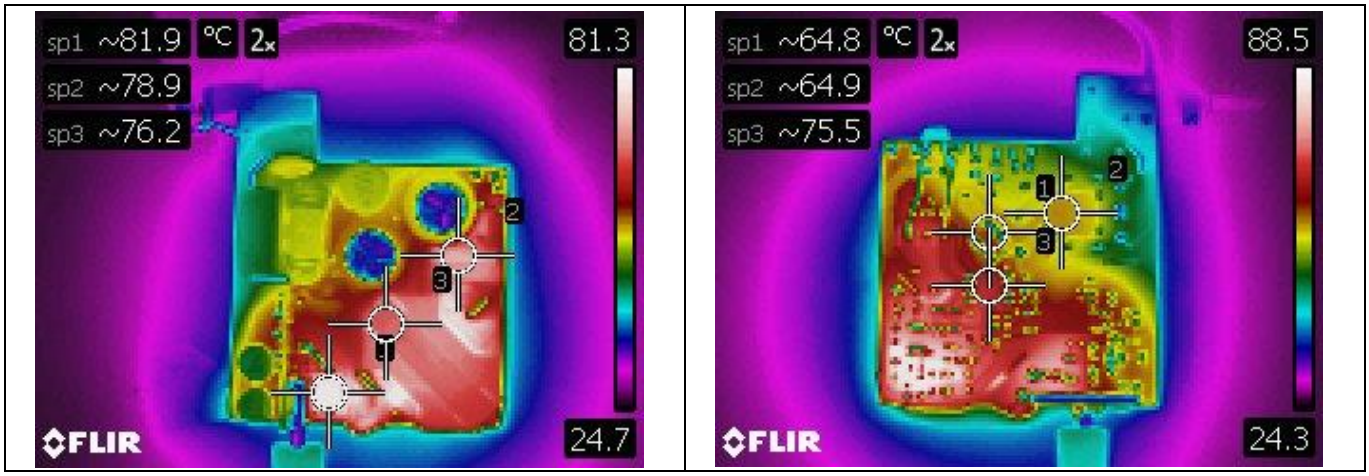


Figure 19 Top layer (left) and bottom layer (right) thermal image at 264 V AC input voltage

10 Waveform and oscilloscope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy WaveRunner 40xi oscilloscope.

10.1 Start-up time (5 V output)

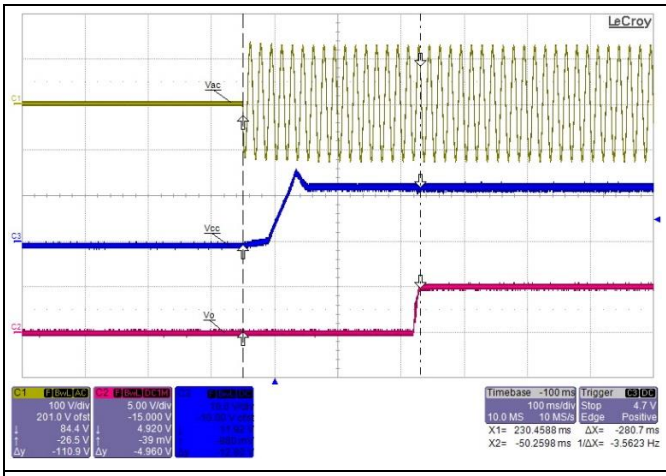
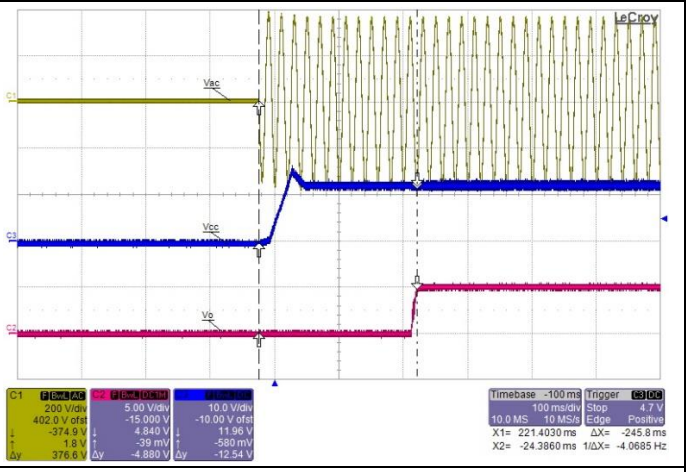
	
C1 (yellow) : AC-line voltage C2 (red) : Output voltage C3 (blue) : V_{CC} voltage	C1 (yellow) : AC-line voltage C2 (red) : Output voltage C3 (blue) : V_{CC} voltage
90 V AC start-up time at full load: 280 ms	264 V AC start-up time at full load: 245 ms

Figure 20 Start-up time

10.2 Primary MOSFET drain and CS voltage at full load (11 V output)

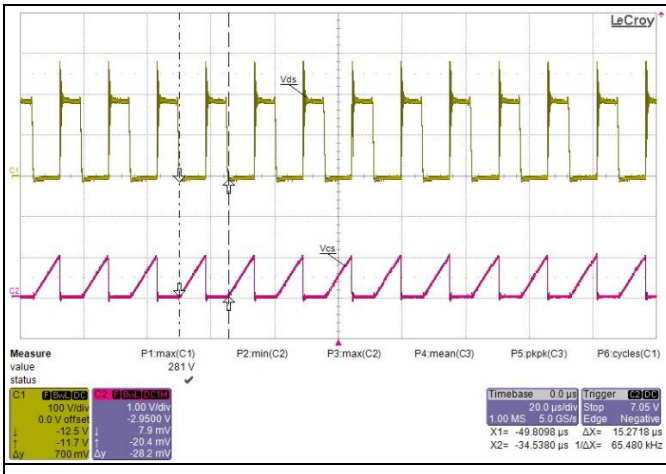
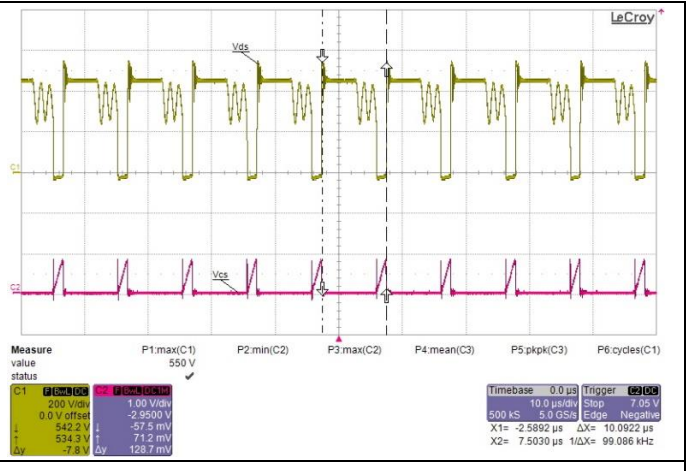
	
C1 (yellow) : Primary MOSFET drain voltage C2 (red) : CS voltage	C1 (yellow) : Primary MOSFET drain voltage C2 (red) : CS voltage
90 V AC maximum primary MOSFET drain voltage at full load is ~281 V; switching frequency at 65 kHz; MOSFET switch-on at first valley	264 V AC maximum primary MOSFET drain voltage at full load is ~550 V; switching frequency at 100 kHz; MOSFET switch-on at third valley

Figure 21 Primary MOSFET drain and CS voltage

10.3 SR MOSFET drain-to-source voltage at full load (11 V output)

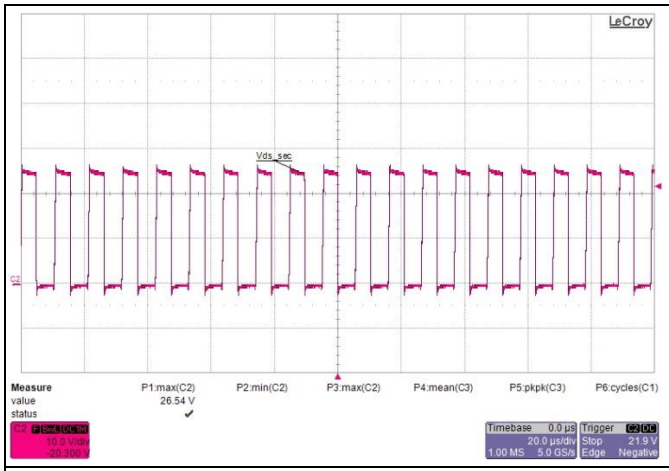
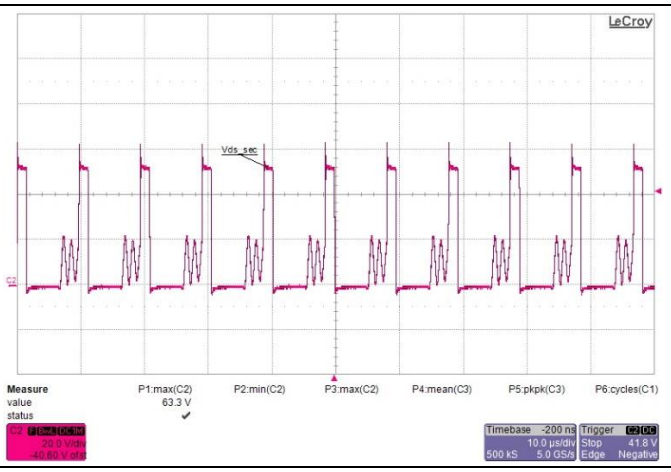
	
C2 (red) : SR MOSFET drain-to-source voltage	C2 (red) : SR MOSFET drain-to-source voltage
90 V AC maximum SR MOSFET drain-to-source voltage at full load is ~27 V	264 V AC maximum SR MOSFET drain-to-source voltage at full load is ~64 V

Figure 22 SR MOSFET drain-to-source voltage

10.4 Output ripple voltage

Output ripple is measured at the PCB end with no load or full load. Probe terminals are decoupled with a 10 µF electrolytic capacitor and a 0.1 µF ceramic capacitor. Oscilloscope bandwidth is limited to 20 MHz.

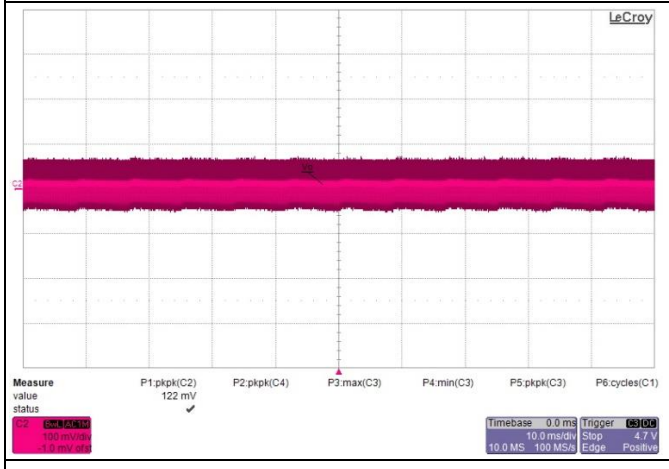
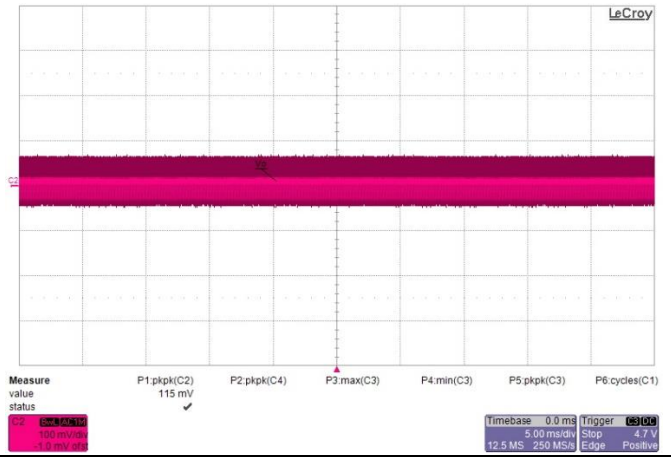
3.3 V/3 A	
	
C2 (red) : Output voltage	C2 (red) : Output voltage
90 V AC 3.3 V output voltage $V_{ripple_pk_pk}$ is ~122 mV	264 V AC 3.3 V output voltage $V_{ripple_pk_pk}$ is ~115 mV

Figure 23 3.3 V output ripple voltage

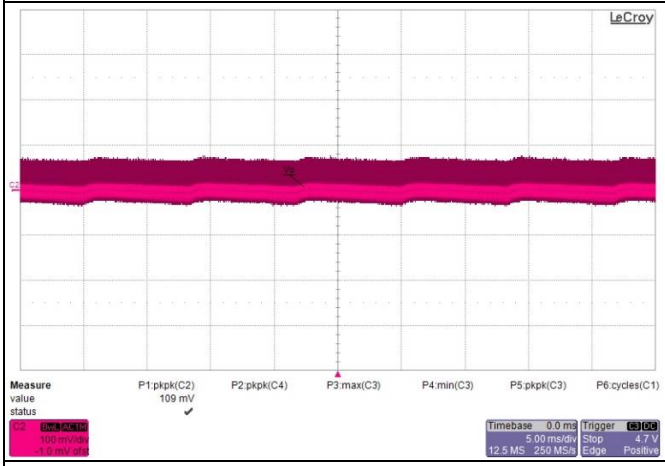
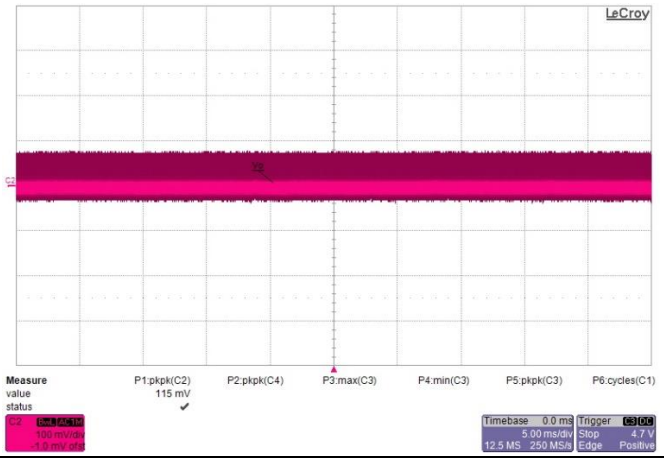
5 V/3 A	
	
C2 (red) : Output voltage	C2 (red) : Output voltage
90 V AC 5 V output voltage $V_{ripple_pk_pk}$ is ~109 mV	264 V AC 5 V output voltage $V_{ripple_pk_pk}$ is ~115 mV

Figure 24 5 V output ripple voltage

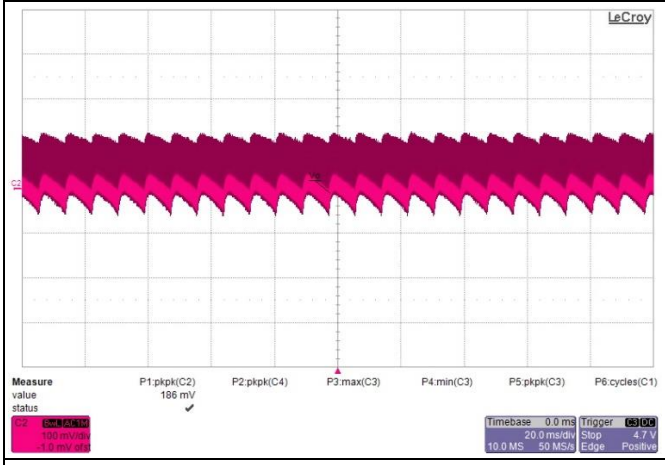
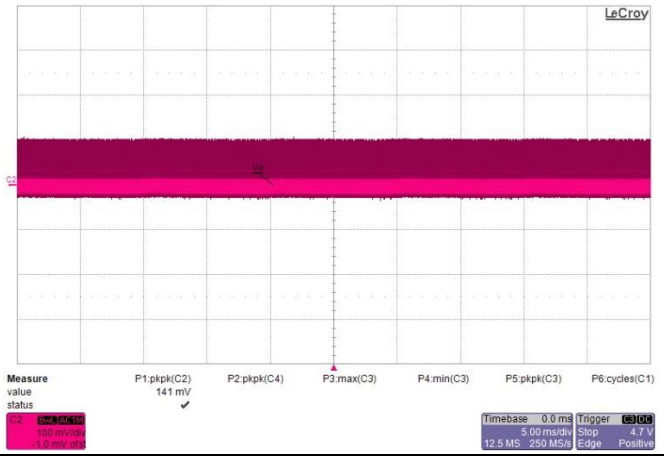
9 V/3 A	
	
C2 (red) : Output voltage	C2 (red) : Output voltage
90 V AC 9 V output voltage $V_{ripple_pk_pk}$ is ~186 mV	264 V AC 9 V output voltage $V_{ripple_pk_pk}$ is ~141 mV

Figure 25 9 V output ripple voltage

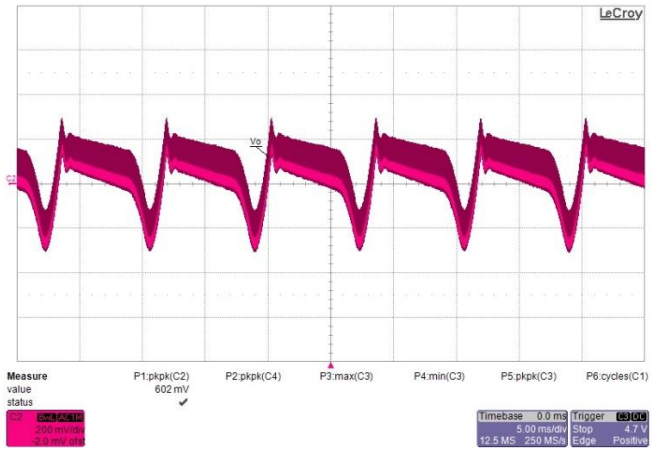
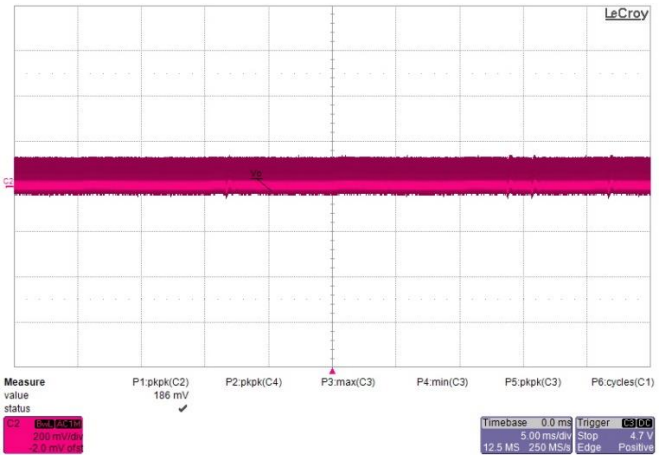
11 V/3 A	
	
C2 (red) : Output voltage	C2 (red) : Output voltage
90 V AC 11 V output voltage $V_{ripple_pk_pk}$ is ~602 mV	264 V AC 11 V output voltage $V_{ripple_pk_pk}$ is ~186 mV
Note: To improve ripple at 90 V AC, reduce output power or increase bulk capacitance.	

Figure 26 11 V output ripple voltage

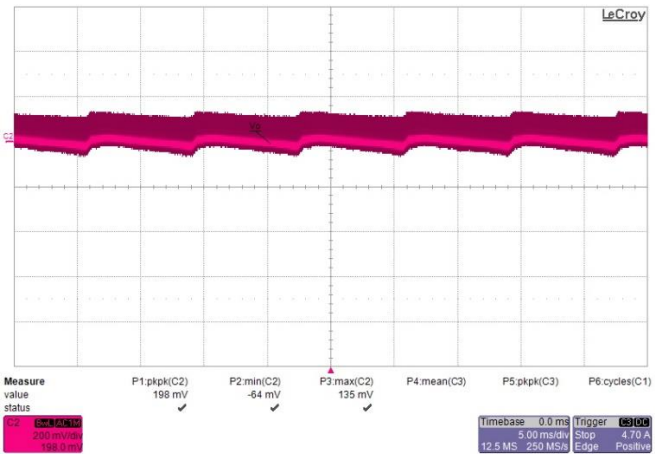
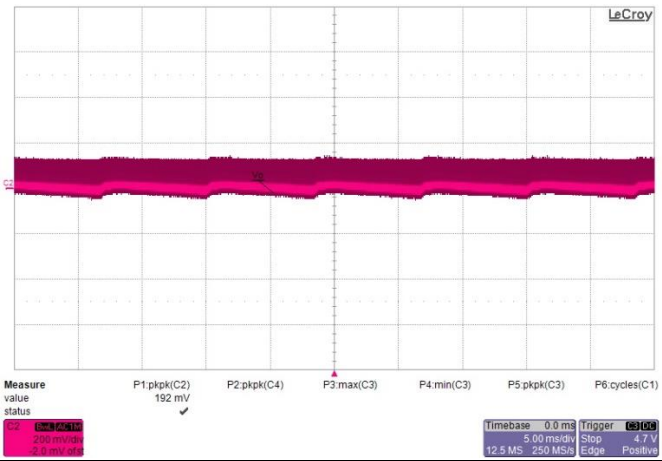
11 V/2.45 A (27 W with input 90 V AC)	11 V/3 A (33 W with input 115 V AC)
	
C2 (red) : Output voltage	C2 (red) : Output voltage
90 V AC 11 V output voltage $V_{ripple_pk_pk}$ is ~198 mV	115 V AC 11 V output voltage $V_{ripple_pk_pk}$ is ~192 mV

Figure 27 11 V output ripple voltage with 27 W load at 90 V AC and with 33 W load at input 115 V AC

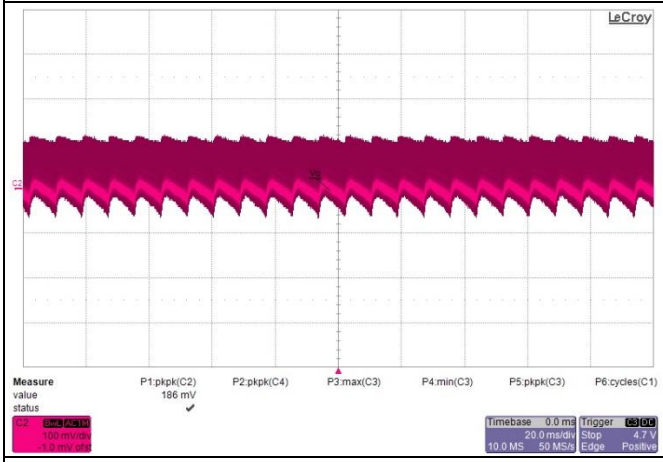
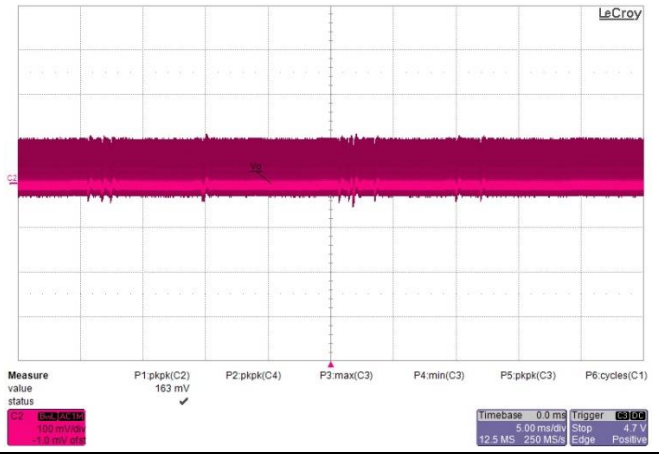
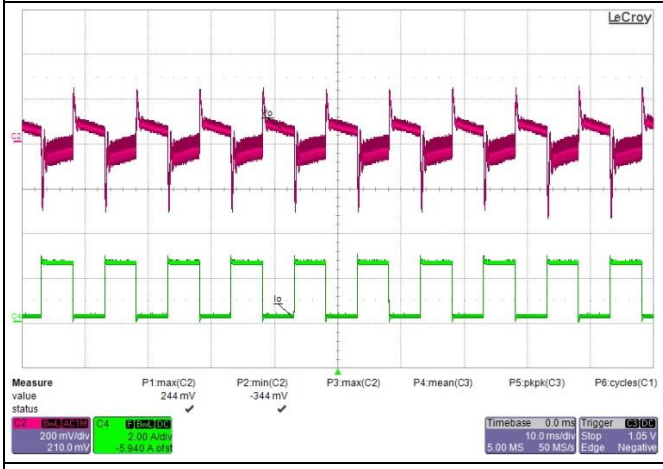
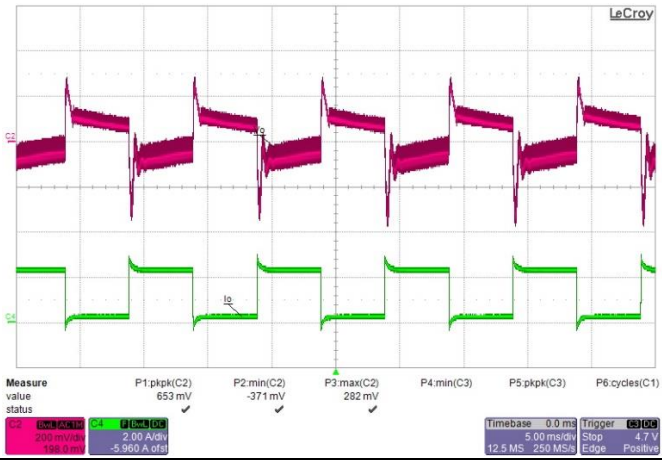
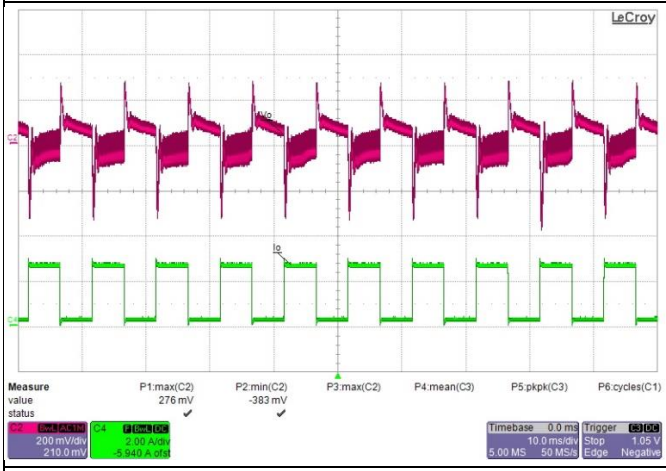
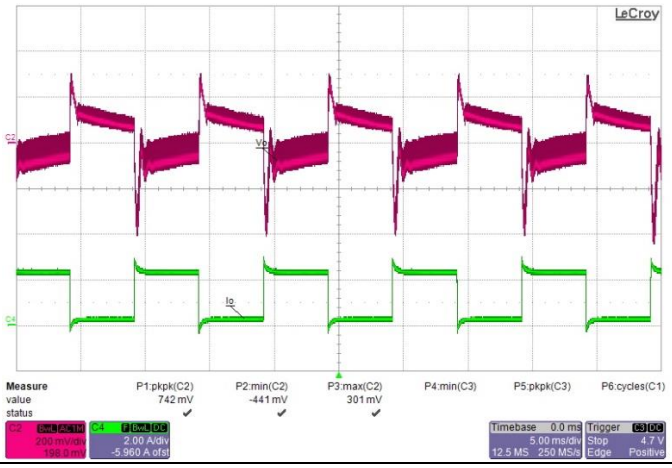
12 V/2.25 A	
	
C2 (red) : Output voltage	C2 (red) : Output voltage
90 V AC 12 V output voltage $V_{ripple_pk_pk}$ is ~186 mV	264 V AC 12 V output voltage $V_{ripple_pk_pk}$ is ~163 mV

Figure 28 12 V output ripple voltage

10.5 Dynamic load (fixed PDO)

<table>
<tr><td colspan="2">5 V (PD 3.0)</td></tr>
<tr><td>
</td><td>
</td></tr>
<tr><td>C2 (red) : Output voltage
C4 (green) : Output current</td><td>C2 (red) : Output voltage
C4(green) : Output current</td></tr>
<tr><td>90 V AC 5 V output voltage $V_{ripple_pk_pk}$ is ~ 588 mV</td><td>264 V AC 5 V output voltage $V_{ripple_pk_pk}$ is ~653 mV</td></tr>
<tr><td colspan="2">Requirement: 4.5 V less than V_{OUT} less than 5.5 V</td></tr>
<tr><td colspan="2">9 V (PD 3.0)</td></tr>
<tr><td>
</td><td>
</td></tr>
<tr><td>C2 (red) : Output voltage
C4 (green) : Output current</td><td>C2 (red) : Output voltage
C4 (green) : Output current</td></tr>
<tr><td>90 V AC 9 V output voltage $V_{ripple_pk_pk}$ is ~659 mV</td><td>264 V AC 9 V output voltage $V_{ripple_pk_pk}$ is ~742 mV</td></tr>
<tr><td colspan="2">Requirement: 8.1 V less than V_{OUT} less than 9.9 V</td></tr>
<tr><td colspan="2">12 V (QC 2.0)</td></tr>
</table>

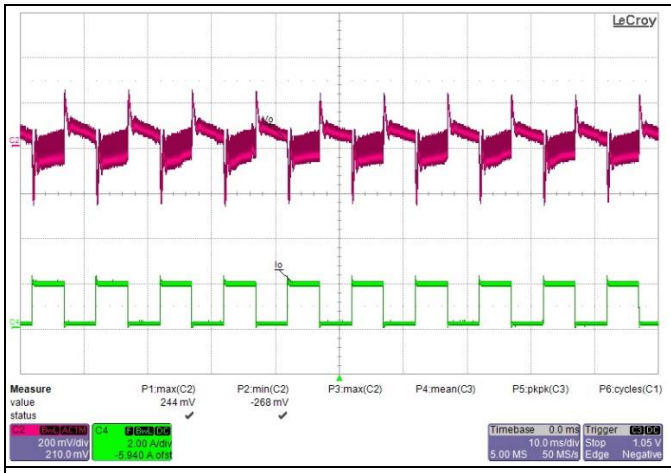
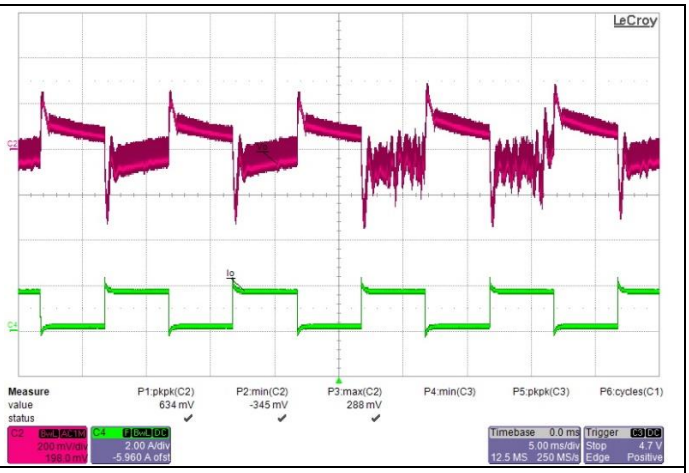
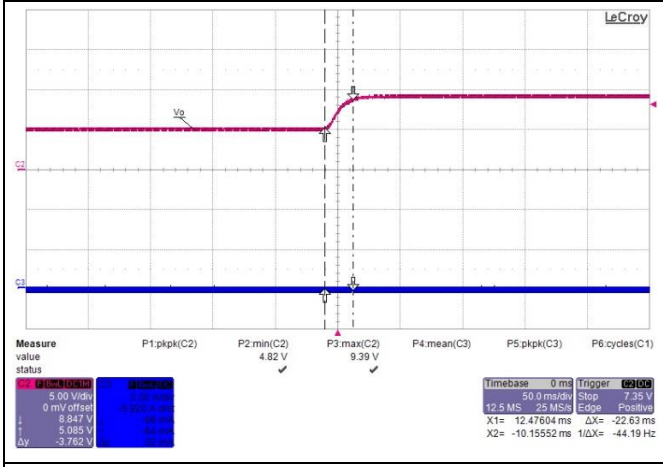
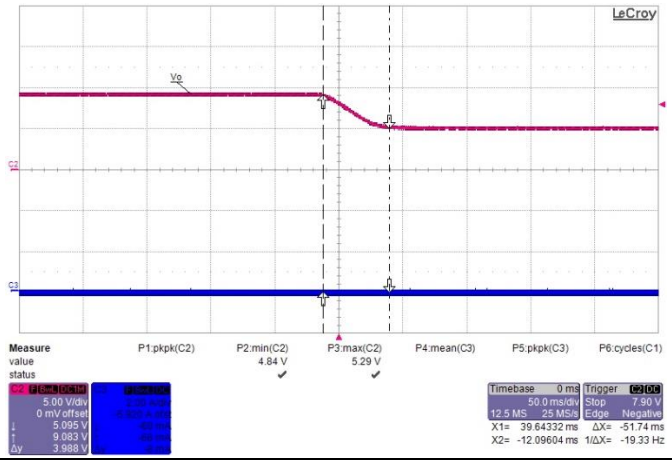
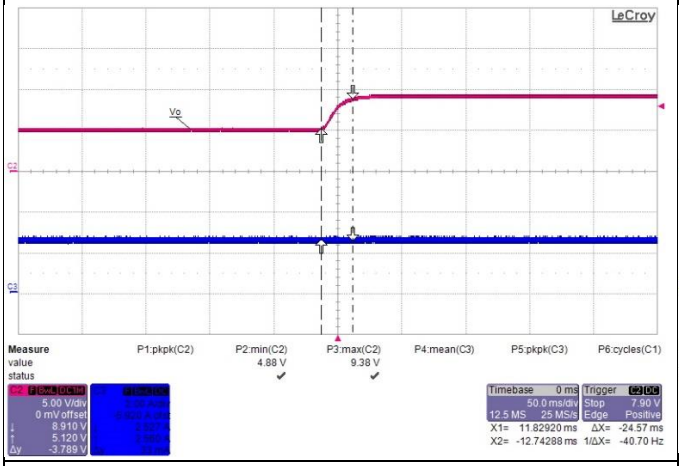
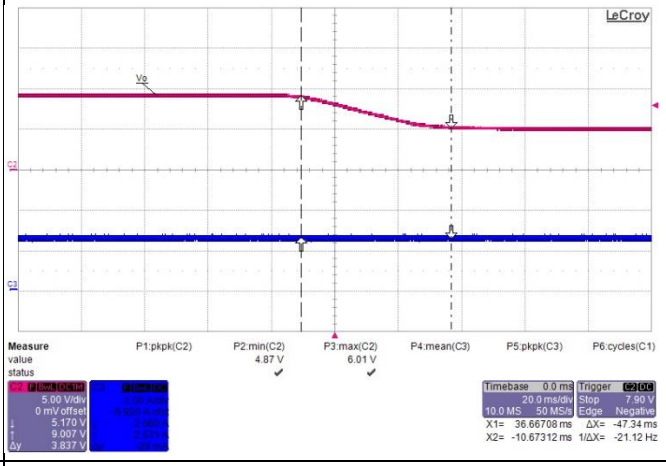
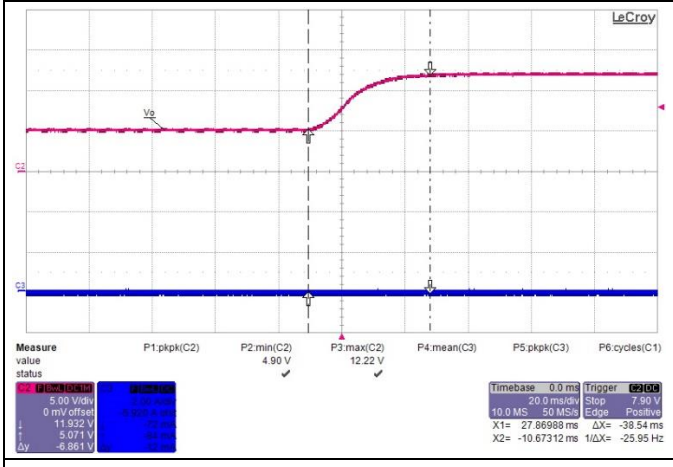
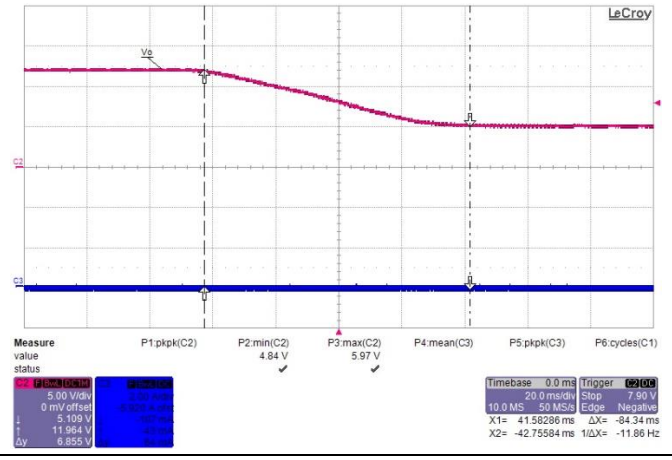
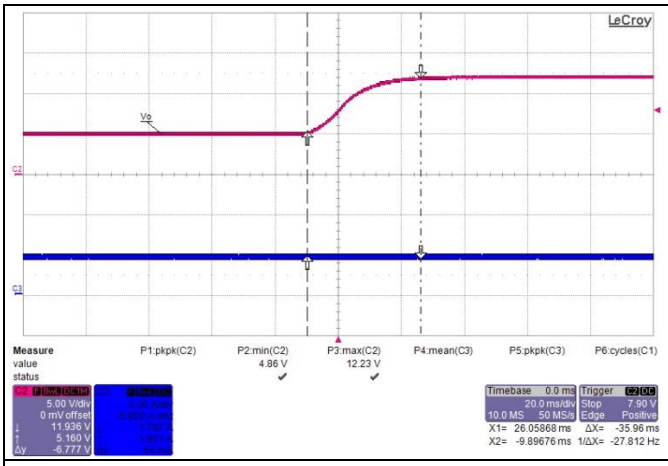
	
C2 (red) : Output voltage C4 (green) : Output current	C2 (red) : Output voltage C4 (green) : Output current
90 V AC 12 V output voltage $V_{ripple_pk_pk}$ is ~512 mV	264 V AC 12 V output voltage $V_{ripple_pk_pk}$ is ~634 mV
Requirement: 10.8 V less than V_{OUT} less than 13.2 V	

Figure 29 Load-transient response with output load change from 10 percent to 100 percent at 0.4 A/µs slew rate, 100 Hz. Probe terminals are connected on the PCB end and decoupled with a 1 µF electrolytic capacitor and a 0.1 µF ceramic capacitor. Oscilloscope is bandwidth filter limited to 20 MHz.

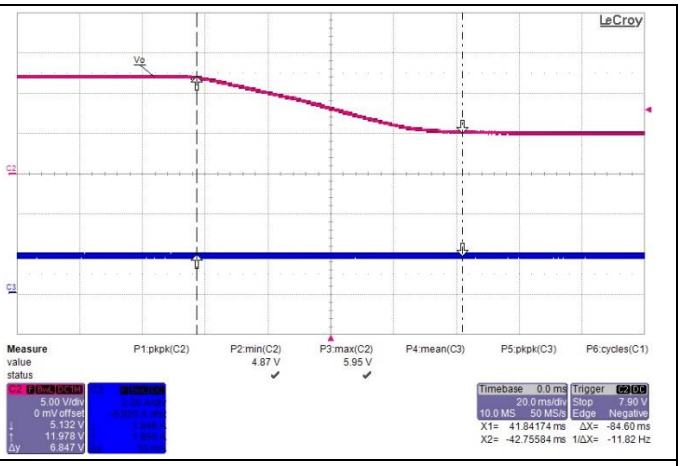
10.6 Output voltage transition (fixed PDO)

Input voltage: 115 V AC/60 Hz
Output current: No load and full load
Requirement: Less than 200 mS
5 V ↔ 9 V

<table>
<tr><td></td><td></td></tr>
<tr><td>Transition time without load: 22.63 ms</td><td>Transition time without load: 51.74 ms</td></tr>
<tr><td></td><td></td></tr>
<tr><td>Transition time with full load: 24.57 ms</td><td>Transition time with full load: 47.34 ms</td></tr>
<tr><td colspan="2">5 V ↔ 12 V</td></tr>
<tr><td></td><td></td></tr>
<tr><td>Transition time without load: 38.54 ms</td><td>Transition time without load: 84.34 ms</td></tr>
</table>

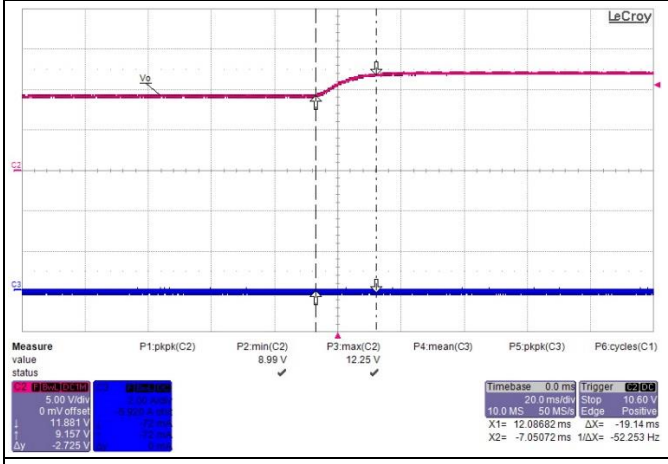


Transition time with full load: 35.96 ms

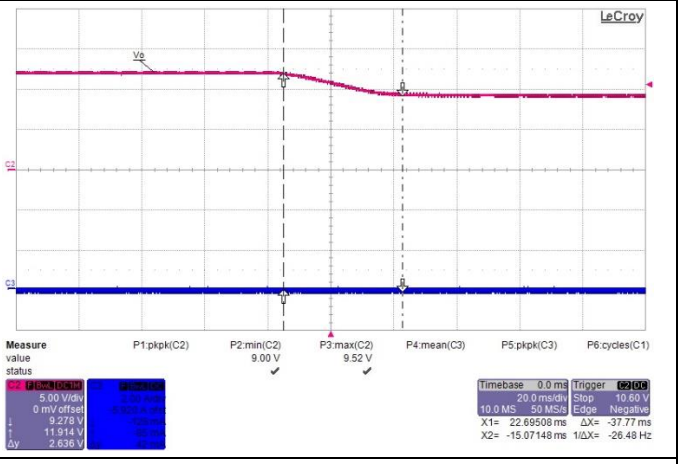


Transition time with full load: 84.6 ms

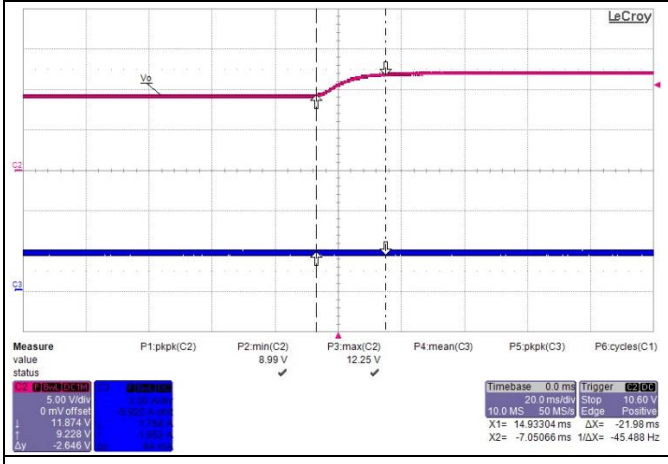
9 V ↔ 12 V



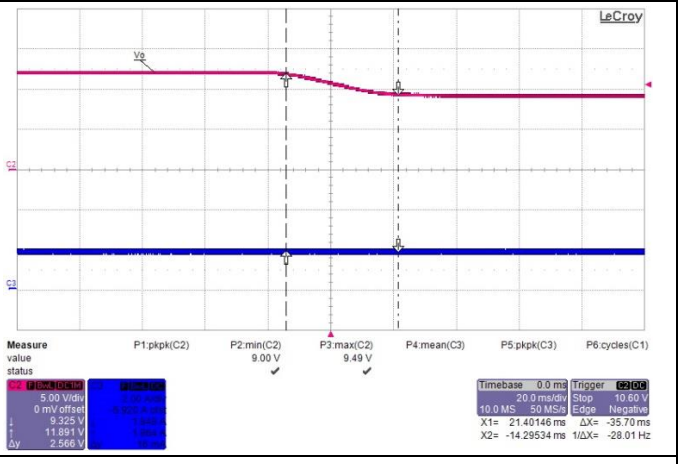
Transition time without load: 19.14 ms



Transition time without load: 37.77 ms



Transition time with full load: 21.98 ms



Transition time with full load: 35.7 ms

Figure 30 Output voltage transition

10.7 Entering ABM (5 V output)

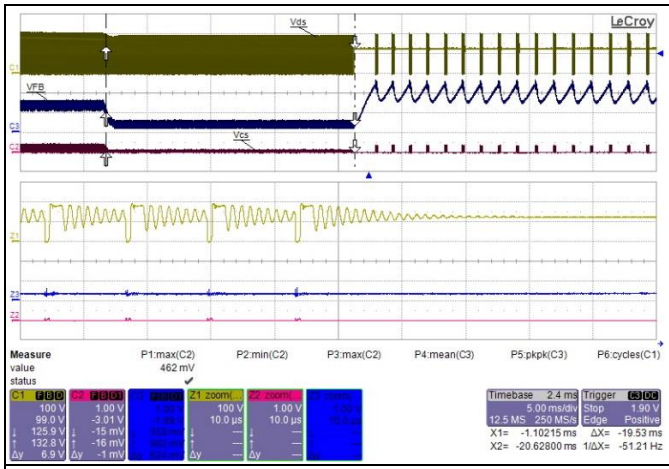
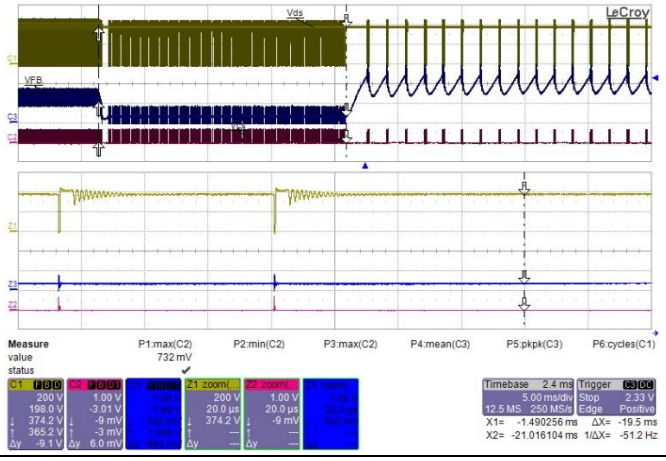
	
C1 (yellow) : Primary MOSFET drain voltage C2 (purple) : CS voltage C3 (blue) : FB pin voltage	C1 (yellow) : Primary MOSFET drain voltage C2 (purple) : CS voltage C3 (blue) : FB pin voltage
90 V AC 1 A to 0.1 A load. Enter ABM at FB pin voltage less than 1.05 V (V_{FB_EBL2}) and eighth valley for ~20 ms (t_{FB_BEB})	264 V AC 1 A to 0.1 A load. Enter ABM at FB pin voltage less than 1.05 V (V_{FB_EBL2}) and tenth valley for ~20 ms (t_{FB_BEB})

Figure 31 Entering ABM; output at 1 A to 100 mA load

10.8 During ABM (5 V output)

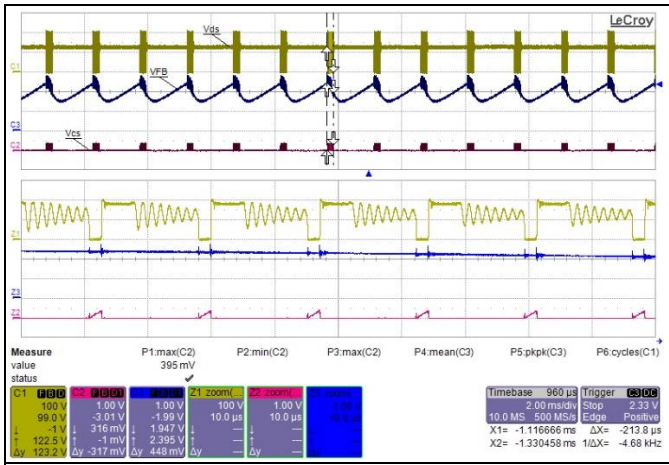
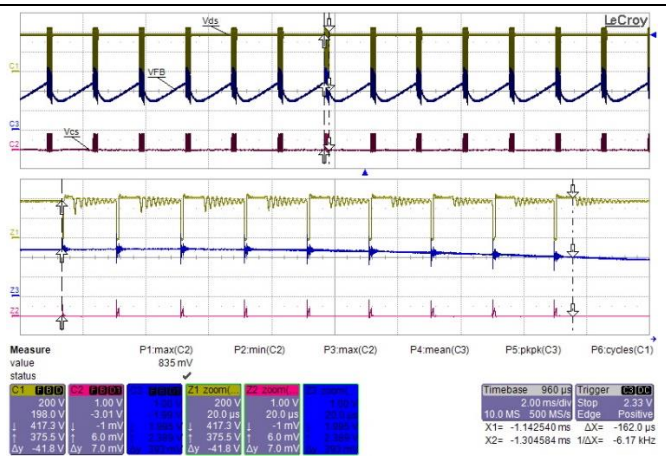
	
C1 (yellow) : Primary MOSFET drain voltage C2 (purple) : CS voltage C3 (blue) : FB pin voltage	C1 (yellow) : Primary MOSFET drain voltage C2 (purple) : CS voltage C3 (blue) : FB pin voltage
90 V AC at 100 mA load. Burst-on at FB voltage 2.4 V (V_{FB_BOn}) and burst-off at 2 V (V_{FB_BOff}). CS voltage at 0.35 V (V_{CS_BL2}). Switch-on at eighth valley.	264 V AC at 100 mA load. Burst-on at FB voltage 2.4 V (V_{FB_BOn}) and burst-off at 2 V (V_{FB_BOff}). CS voltage at 0.35 V (V_{CS_BL2}). Switch-on at tenth valley.

Figure 32 During ABM; output at 100 mA load

10.9 Leaving ABM (5 V output)

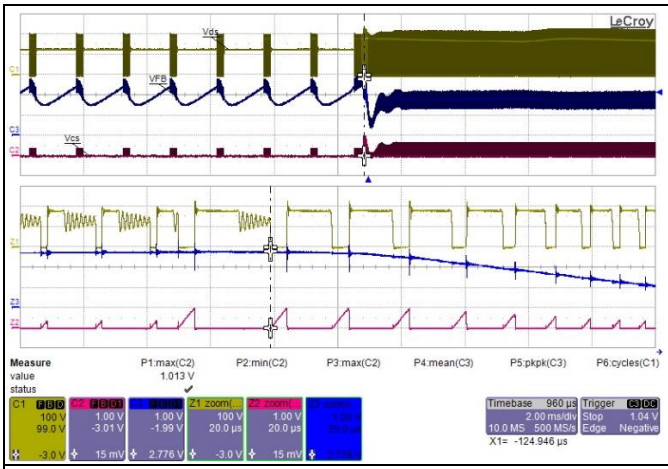
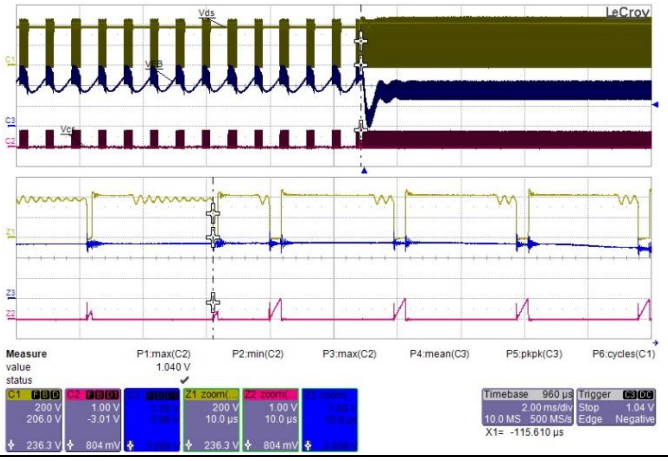
	
C1 (yellow) : Primary MOSFET drain voltage C2 (purple) : CS voltage C3 (blue) : FB pin voltage	C1 (yellow) : Primary MOSFET drain voltage C2 (purple) : CS voltage C3 (blue) : FB pin voltage
90 V AC at 100 mA load to 1 A load. Leave ABM at FB voltage greater than 2.75 V (V_{FB_LB}) and gate turn-on after detecting valley.	264 V AC at 100 mA load to 1 A load. Leave ABM at FB voltage greater than 2.75 V (V_{FB_LB}) and gate turn-on after detecting valley.

Figure 33 Leaving ABM; output at 10 mA load to 1 A load

10.10 Output OVP (fixed PDO)

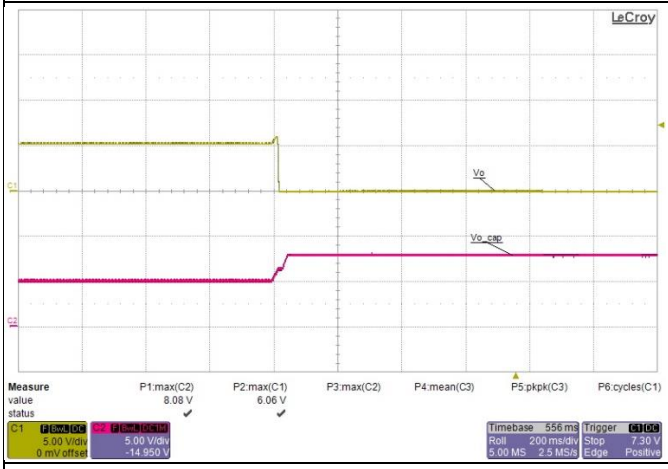
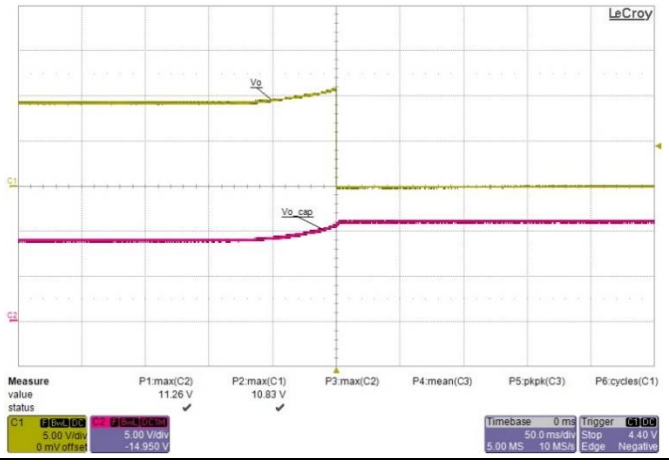
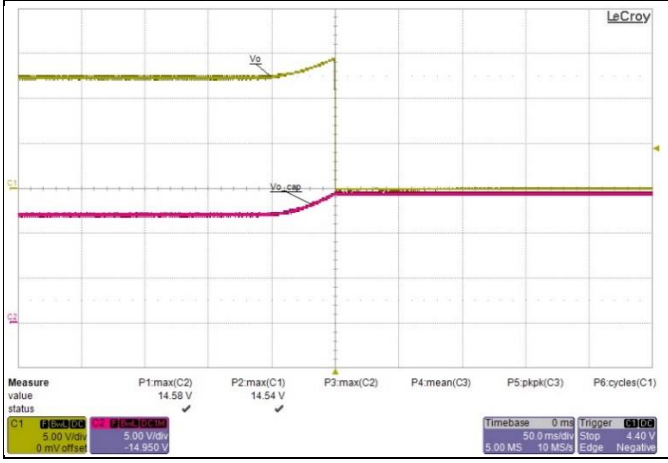
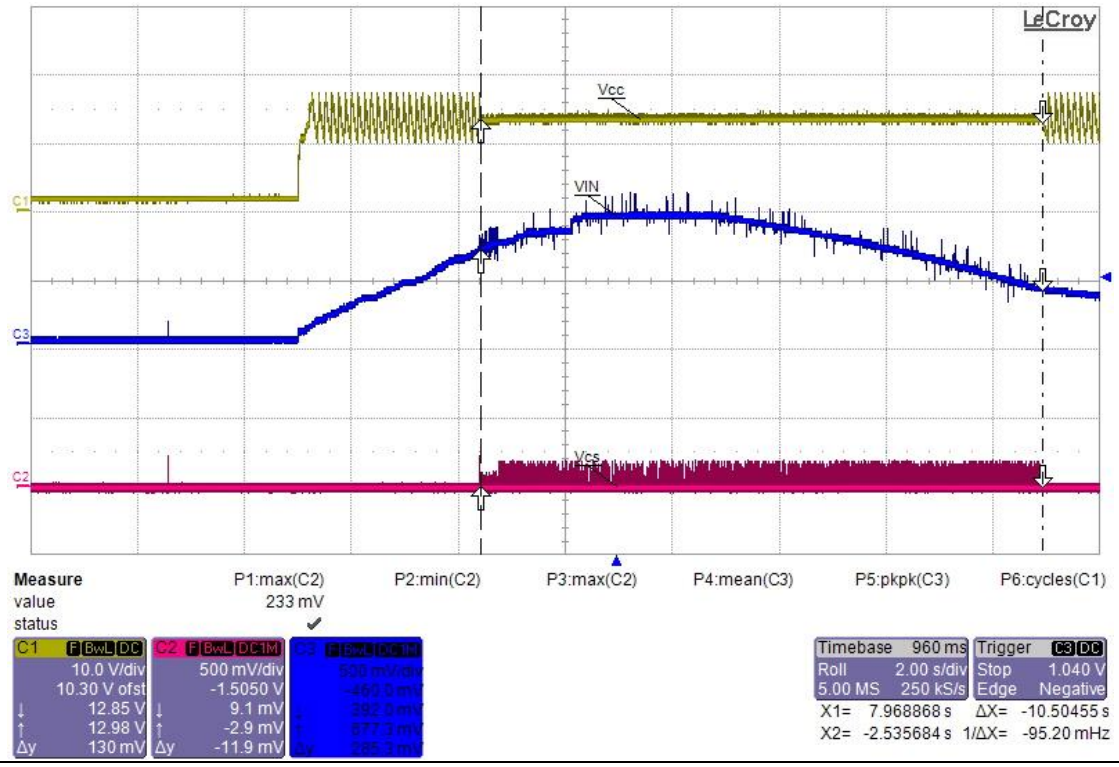
5 V OVP Test	9 V OVP Test
	
C1 (yellow) : Output voltage C2 (purple) : C5 voltage (output capacitor) Apply DC voltage 8 V DC on V_{c5} output capacitor; OVP_voltage = 6.06 V	C1 (yellow) : Output voltage C2 (purple) : C5 voltage (output capacitor) Apply DC voltage 11 V DC on V_{c5} output capacitor; OVP_voltage = 10.83 V
12 V OVP test	
	C1 (yellow) : Output voltage C2 (purple) : C5 voltage (output capacitor) Apply DC voltage 15 V DC on V_{c5} output capacitor; OVP_voltage = 14.54 V

Figure 34 Output OVP at no load

10.11 Brown-in/-out protection



C1 (yellow) : Primary MOSFET drain voltage
C2 (purple) : CS voltage
C3 (blue) : VIN pin voltage

1. Gradually increase input voltage at no load. Brown-in at V_{VIN} voltage greater than 0.66 V (V_{VIN_BI}).
2. Gradually decrease input voltage at no load. Trigger brown-out protection at V_{VIN} voltage less than 0.40 V (V_{VIN_BO}).

Non-switch auto restart mode.

Figure 35 Brown-in/-out protection at no load. Brown-in at ~80 V AC and brown-out at ~48 V AC. The expected line OVP is at ~350 V AC.

10.12 Overcurrent protection (fixed PDO)

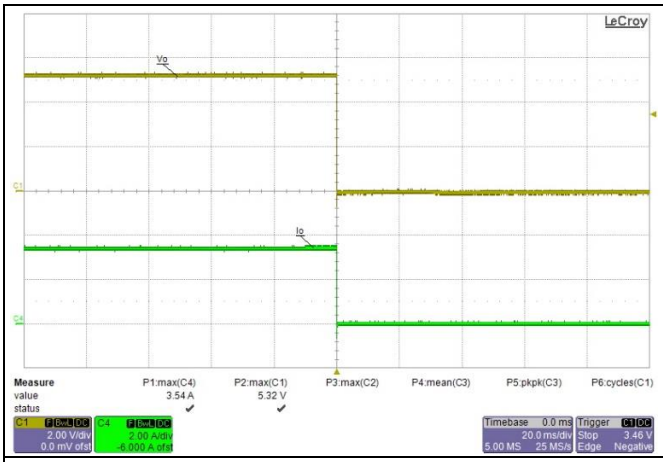
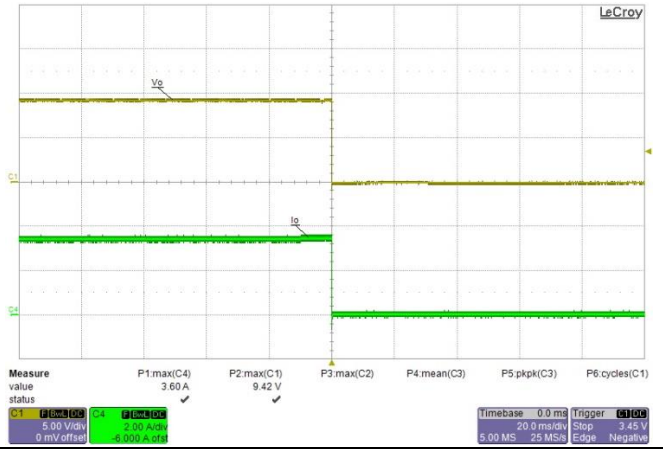
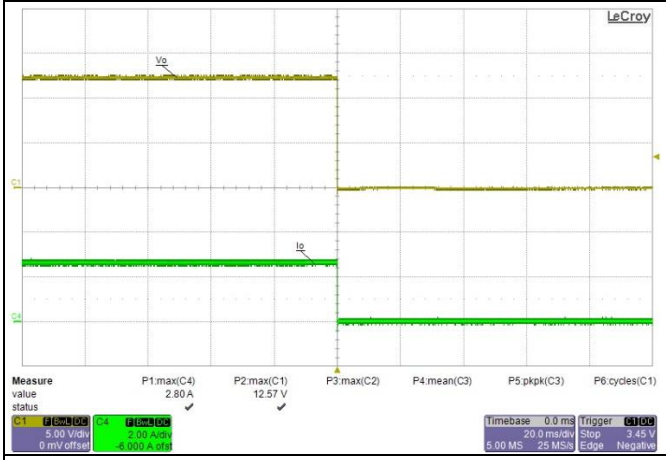
	
C1 (yellow) : Output voltage C4 (green) : Output current	C1 (yellow) : Output voltage C4 (green) : Output current
5 V output voltage, OCP_current = 3.54 A	9 V output voltage, OCP_current = 3.60 A
	
C1 (yellow) : Output voltage C4 (green) : Output current	
12 V output voltage, OCP_current = 2.80 A	

Figure 36 Overcurrent protection

10.13 Hold-up time (9 V/3 A)

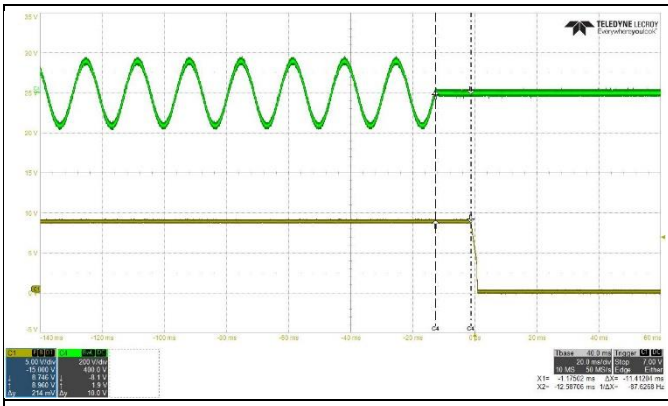
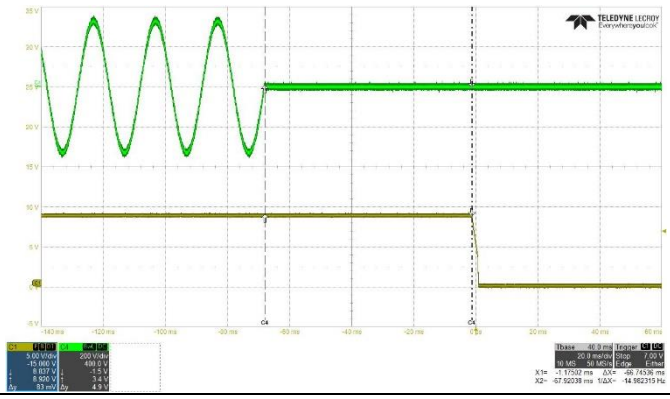
	
C1 (yellow) : Output voltage C4 (green) : AC-line voltage	C1 (yellow) : Output voltage C4 (green) : AC-line voltage
115 V AC full load hold-up time is 11.4 ms	230 V AC full load hold-up time is 67 ms

Figure 37 Hold-up time at full load

11 Appendix A: Transformer design and spreadsheet

Design procedure for QR flyback converter using Q5 CoolSET™ 5QRxxxxAx (Version 1.1)

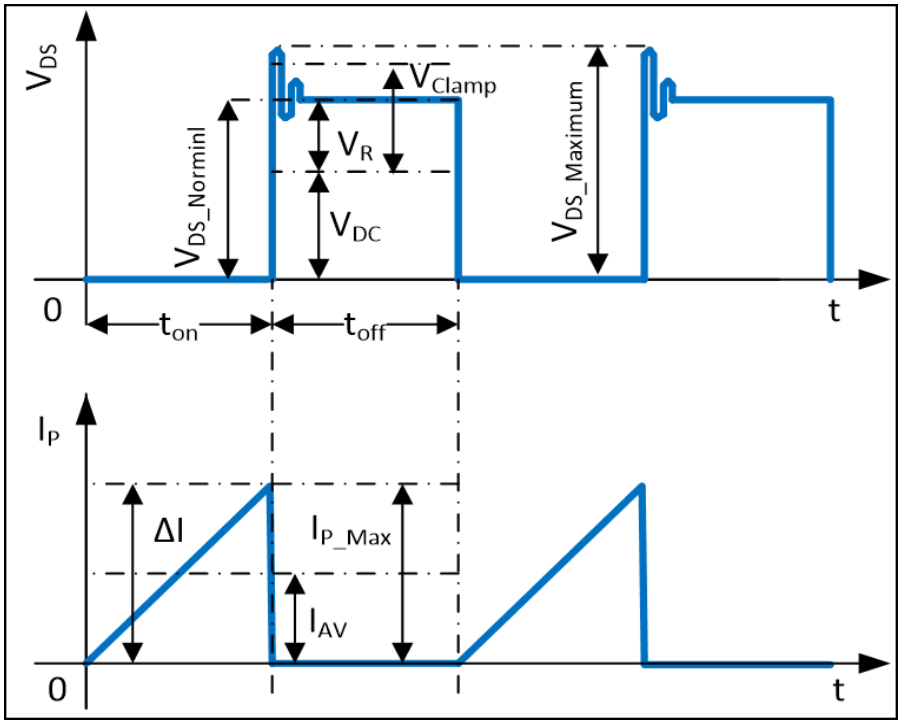
Project	**33 W USB PD charger using ICE5QSBG**
Application	**90 ~ 264 V AC, 11 V/3 A single-output single FB**
Controller	**ICE5QSBG**
Date	
Version	**1.0**

Enter design variables in yellow colored cells

Read design results in green colored cells

Equation numbers are according to the application note

			Unit	Value
Input	**Minimum AC input voltage**	**$V_{AC\ Min}$**	[V]	**90**
Input	**Maximum AC input voltage**	**$V_{AC\ Max}$**	[V]	**264**
Input	**Line frequency**	**f_{AC}**	[Hz]	**60**
Input	**Bus capacitor (C13) DC ripple voltage**	**$V_{DC\ Ripple}$**	[V]	**48**
Input	**Output voltage 1**	**V_{Out1}**	[V]	**11**
Input	**Output current 1**	**I_{Out1}**	[A]	**3.00**
Input	**Forward voltage of output diode (D21)**	**$V_{F\ Out1}$**	[V]	**0.1**
Input	**Output ripple voltage**	**$V_{Out\ Ripple}$**	[V]	**0.24**
Input	**Maximum output power for start-up, transient response and over-load protection**	**$P_{Out\ Max}$**	[W]	**33**
Result	**Nominal output power**	**$P_{Out\ Nor}$**	[W]	33.00
Input	**Minimum output power**	**$P_{Out\ Min}$**	[W]	**3**
Input	**Efficiency**	**η**		**0.88**
Result	**Drain-to-source capacitance of MOSFET (including $Co_{(er)}$ of MOSFET)**	**C_{DS}+$Co_{(er)}$**	[pF]	10.00



Input	**Reflection voltage**	**V_R**	[V]	**99.9**
Input	**V_{CC} voltage**	**V_{Vcc}**	[V]	**18**
Input	**Forward voltage of V_{CC} diode (D12)**	**$V_{F\ Vcc}$**	[V]	**0.6**
Result	**Fifth-generation QR flyback PWM controller**	**CoolSET™ -Q5**		**ICE5QSBG**
Input	**Low-line min. switching frequency**	**f_S**	[Hz]	**62000**
Input	**Targeted max. drain-to-source voltage**	**$V_{DS\ Max}$**	[V]	**700**
Input	**Max. ambient temperature**	**T_a**	[°C]	**50**
Diode bridge (BR1)				
Result	**Eq 1**	$P_{In\ Max}$	[W]	37.5
Result	**Eq 2**	$I_{AC\ RMS}$	[A]	0.694
Result	**Eq 3**	$V_{DC\ Max\ Pk}$	[V]	373.35
Result	**Eq 4**	$V_{DC\ Min\ Pk}$	[V]	127.28
Result	**Eq 10**	$V_{DC\ Min}$	[V]	77.83
Result	**Eq 6**	T_D	[ms]	5.95
Result	**Eq 7**	W_{In}	[Ws]	0.22
Result	**Eq 11**	D_{Max}		0.5621
Input capacitor (C13)				
Result	**Eq 8**	C_{In} (C13)	[µF]	45.01
Input	**Select input capacitor**	**C_{In} (C13)**	[µF]	**44**
Transformer (TR1)				
Result	**Eq 12**	L_P	[H]	4.015E-04
Result	**Eq 13**	I_{AV}	[A]	0.86
Result	**Eq 14**	ΔI	[A]	1.758
Result	**Eq 15**	$I_{P\ Max}$	[A]	1.74
Result	**Eq 16**	I_{Valley}	[A]	0.0
Result	**Eq 17**	$I_{P\ RMS}$	[A]	0.75
Select core type				
Input	**Select core type**			**10**
		Core type		**RM8**
		Core material		**TP4A**
	Maximum flux density	B_{Max}	[T]	**0.35**
	Effective magnetic cross-section	A_e	[mm²]	**52**
	Bobbin width	BW	[mm]	**9.14**
	Winding cross-section	A_N	[mm²]	**31.35**
	Average length of turn	l_N	[mm]	**44.6**
Winding calculation				
Result	**Eq 18**	N_P	Turns	38.29
Input	**Choose number of primary turns**	**N_P**	Turns	**45**
Result	**Eq 19**	N_{S1}	Turns	5.00
Input	**Choose number of secondary turns**	**N_{S1}**	Turns	**5**
Result	**Eq 20**	N_{Vcc}	Turns	8.38
5Input	**Choose number of auxiliary turns**	**N_{Vcc}**	Turns	**20**
Result	**Auxiliary supply voltage (Eq 21)**	V_{Vcc}	[V]	**43.80**
Post calculation				
Result	**Eq 23**	V_R	[V]	**99.9**
Result	**Eq 24**	D_{Max}		**0.56**
Result	**Eq 25**	D_{Max}'		**0.44**
Result	**Eq 26**	B_{Max}	[T]	**0.298**

Appendix A: Transformer design and spreadsheet

CS resistor (R14)

Input	**CS threshold value from datasheet**	**V_{csth}**	[V]	**1**
Result	**Eq 21**	R_{Sense}	[Ω]	0.58
Result	**Eq 22**	P_{SR}	[W]	**0.32**
Input	**PWM-OP gain from datasheet**	**A_V**		**2.05**
Result	**Eq 94**	Z_{PWM}	[V/A]	**1.2**

Transformer winding design

Input	**Margin according to safety standard**	**M**	[mm]	**0**
Input	**Copper space factor**	**f_{Cu}**		**0.4**

Primary

Input	**Insulation thickness**	**INS**	[mm]	**0.01**
Result	**Eq 32**	A_p (area of primary wire)	[mm^2]	0.14
Result	**Eq 36**	d (diameter of primary wire)	[mm]	0.42
Result	**Eq 35**	AWG		26
Input	**Selected wire size**	**AWG**		**27**
Input	**Number of parallel wires**	**np**		**1**
Result	**Eq 37**	D (diameter of primary wire)	[mm]	0.36
Result	**Eq 38**	(Effective copper area of primary)	[mm^2]	0.1034
Result	**Eq 39**	Sp (primary current density)	[A/mm^2]	7.22
Result	**Eq 30**	BW_e (effective bobbin width)	[mm]	9.1
Result	**Eq 40**	Od_p (diameter of primary wire including insulation)	[mm]	0.38
Result	**Eq 41**	NL_P (max. primary turns/layer)	Turns/layer	23
Result	**Eq 42**	Ln_P (primary layers)	Layers	2

Secondary

Input	**Insulation thickness**	**INS**	[mm]	**0.02**
Result	**Eq 33**	A_S (area of secondary wire)	[mm^2]	1.13
Result	**Eq 36**	d (diameter of secondary wire)	[mm]	1.20
Result	**Eq 35**	AWG		17
Input	**Selected wire size**	**AWG**		**22**
Input	**Number of parallel wires**	**np**		**2**
Result	**Eq 37**	dia (diameter of secondary wire)	[mm]	0.65
Result	**Eq 38**	(Effective copper area of secondary)	[mm^2]	0.6564
Result	**Eq 39**	S_S (secondary current density)	[A/mm^2]	9.04
Result	**Eq 30**	BW_E (effective bobbin width)	[mm]	9.1
Result	**Eq 40**	Od_S (diameter of secondary wire including insulation)	[mm]	0.69
Result	**Eq 41**	NL_S (max. secondary turns/layer)	Turns/layer	6
Result	**Eq 42**	Ln_S (secondary layers)	Layers	1

Leakage Inductance

Input		**Leakage inductance in % of L_P**	[%]	**1**
Result	**Eq 45**	L_{LK}	[H]	4.01E-06

RCD clamper circuit (D11,R11 and C15)

Result	**Eq 44**	V_{Clamp}	[V]	226.75
Result	**Eq 46**	C_{clamp} (C15)	[nF]	0.2
Input	**Selected C_{clamp} capacitor value**	**C_{clamp} (C15)**	[nF]	**1**
Result	**Eq 47**	R_{clamp} (R11)	[kΩ]	257.9
Input	**Selected R_{clamp} value**	**R_{clamp} (R11)**	[kΩ]	**440**

Output and V_{CC} diode (D21, D22 and D12)

Result	**Eq 27**	K_{L1} (load factor)		1.00

Appendix A: Transformer design and spreadsheet

Result	**Eq 43a**	$V_{RDiode1}$ (for output MOSFET)	[V]	52.48
Result	**Eq 28**	$I_{S\,Max1}$	[A]	15.62
Result	**Eq 29**	$I_{S\,RMS1}$	[A]	5.93
Result	**Eq 43b**	V_{RDiode} (for V_{CC} diode)	[V]	183.93

Output capacitor (C22 and C23)

Input	**Max. voltage overshoot at output capacitor (C22, C23)**	**ΔV_{Out}**	[V]	**0.5**
Input	**Number of clock periods**	**n_{cp}**		**10**
Result	**Eq 49**	I_{Ripple}	[A]	5.11
Result	**Eq 50**	C_{Out}	[µF]	968

Soft-start time

Input	**Chosen soft-start time from datasheet**	**$t_{softstart}$**	[ms]	**12**

V_{CC} capacitor (C16) and start-up time

Input	**Chosen $I_{VCC,Charge3}$ from datasheet**	**$I_{VCC,Charge3}$**	[mA]	**3**
Input	**Chosen V_{VCChys} from datasheet**	**V_{VCChys}**	[V]	**6**
Result	**Eq 56A**	C_{VCC}	[µF]	6.00
Input	**Select V_{CC} capacitor**	**C_{Vcc} (C16)**	[µF]	**20**
Input	**Select $V_{VCC,STG}$ from datasheet**	**$V_{VCC,STG}$**	[V]	**1.1**
Input	**Select $I_{VCC,Charge1}$ from datasheet**	**$I_{VCC,Charge1}$**	[mA]	**0.2**
Input	**Select $V_{VCC,ON}$ from datasheet**	**$V_{VCC,ON}$**	[V]	**16**
Result	**Eq 56B**	$t_{StartUp}$	[ms]	216.67

Calculation of losses

Input diode bridge

Result	**Eq 57 (Vf = 1.1 V)**	P_{DIN}	[W]	1.53

Transformer copper losses

Result	**Eq 58**	R_{PCu}	[mΩ]	333.74
Result	**Eq 58**	R_{SCu}	[mΩ]	5.84
Result	**Eq 59**	P_{PCu}	[mW]	186.13
Result	**Eq 60**	P_{SCu}	[mW]	205.64
Result	**Eq 61**	P_{Cu}	[W]	0.3918

Output SR

Result	**Eq 62 ($R_{DS(on)}$ = 9 mΩ)**	$P_{Out\,SR}$	[W]	0.05

RCD clamper circuit

Result	**Eq 63**	$P_{Clamper}$	[W]	0.54

MOSFET

Input	**$R_{DS(on)}$ from datasheet**	**R_{DSON} @ T_A=125°C**	[Ω]	**1.03**
Input	**$Co_{(er)}$ from datasheet**	**Co(er)**	[pF]	**17**
Input	**External drain-to-source capacitance of MOSFET**	**C_{DS}**	[pF]	**0**

MOSFET losses at V_{ACmin} + P_{max}

Result	**Eq 65**	P_{SON}	[W]	0.000256704
Result	**Eq 66**	P_{cond}	[W]	0.5744
Result	**Eq 67**	MOSFET losses	[W]	0.5747

MOSFET losses at V_{ACmax} + P_{max}

Result	**Eq 68**	P_{SON}	[W]	0.0512
Result	**Eq 69**	P_{cond}	[W]	0.1557
Result	**Eq 70**	MOSFET losses	[W]	0.2069

Temperature calculation

Input	**Enter MOSFET losses**	**MOSFET losses**	[W]	0. .5747
Input	**Enter thermal resistance junction – ambient**	**Rth**	[°K/W]	80
Result	**Eq 74**	ΔT	[°K]	46

Result	**Eq 75**	T_{jmax}	°C	96
Controller				
Result	$I_{VCC,Normal}$xV_{VCC}	Controller losses	[W]	0.0258
Choke losses and thermistor loss				
Result	$I_{AC,RMS}$xR_{DCR}	P_{Choke}	[W]	0.6389
Result	$I_{AC,RMS}$xR_{NTC}	P_{NTC}	[W]	0.1069
Sum of losses				
Result	**Eq 77**	P_{Losses}	[W]	3.85
Efficiency after losses				
Result	**Eq 78**	η_L		0.8855
ZCD and output OVP calculation				
Input	**Designed V_{OUT_OVP}**	V_{OUT_OVP}	[V]	**15**
Input	**$V_{ZC_OVP_MIN}$ from datasheet**	$V_{ZC_OVP_MIN}$	[V]	**1.9**
Input	**R_{ZCD_MIN} from datasheet**	R_{ZCD}	[kΩ]	**3**
Result	**Eq 103**	R_{ZC} (R15)	[kΩ]	92.37
Input	**Selected value of R15**	**R_{ZC} (R15)**	[kΩ]	**91**
Input	**f_{OSC2} by measurement**	f_{OSC2}	[kHz]	**820**
Result	**Eq 104**	C_{ZC} (C19)	[pF]	118
Input	**Selected value of C_{ZC}(C19)**	C_{ZC} (C19)	[pF]	33
Line OVP is the first priority and its associated brown-out, brown-in and line selection				
Input		**R_{I1} (R18)**	[Ω]	**9,000,000**
Input		Line over voltage (V_{OVP_AC})	[V_{AC}]	**320**
Input		**$V_{DC\ Ripple}$**	[V]	**48**
Result	**Eq 105A**	R_{I2} (R19)	[Ω]	58,045
Input	**Selected value of R19 (R_{I2})**	**R_{I2} (R19)**	[Ω]	**58,300**
Result	**Eq 106**	Brown-in voltage ($V_{Brownin_AC}$)	[V AC]	73
Result	**Eq 107**	Brown-out voltage for full load which considers V DC_{RIPPLE} ($V_{Brownout_AC}$)	[V AC]	78
Result	**Eq 107**	Brown-out voltage for light load which neglects V DC_{RIPPLE} ($V_{Brownout_AC}$)	[V AC]	44
Result	**Eq 108**	Line selection threshold with V DC_{RIPPLE} (V_{VIN} = 1.52 V)	[V AC]	201
Result	**Eq 108**	Line selection threshold without V DC_{RIPPLE} (V_{VIN} = 1.52 V)	[V AC]	167
Brown-out is the first priority and its associated line OVP and line selection				
Input		**R_{I1} (R18)**	[Ω]	**9,000,000**
Input		Brown-in voltage (V_{OVP_AC})	[V AC]	**73**
Input		**V DC_{RIPPLE}**	[V]	**48**
Result	**Eq 105B**	R_{I2} (R19)	[Ω]	57,907
Input	**Selected value of R19 (R_{I2})**	**R_{I2} (R19)**	[Ω]	**58,300**
Result	**Eq 107**	Brown-out voltage for full load which considers V DC_{RIPPLE} ($V_{Brownout_AC}$)	[V AC]	78
Result	**Eq 107**	Brown-out voltage for light load which neglects V DC_{RIPPLE} ($V_{Brownout_AC}$)	[V AC]	44
Result	**Eq 114**	Line over voltage (V_{OVP_AC})	[V AC]	319
Result	**Eq 108**	Line selection threshold with V DC_{RIPPLE} (V_{VIN} = 1.52 V)	[V AC]	201
Result	**Eq 108**	Line selection threshold without V DC_{RIPPLE} (V_{VIN} = 1.52 V)	[V AC]	167

12 References

[1] ICE5QSBG datasheet, Infineon Technologies AG

[2] PAG1S – CYPAS111 datasheet, Cypress Semiconductor Corporation

[3] IPAN70R600P7S datasheet, Infineon Technologies AG

[4] AN-201609_PL83_026 – 5th Generation QR Design Guide

[5] Calculation Tool Quasi Resonant CoolSET™ Generation 5

Revision history

Document version	Date of release	Description of changes
V 1.0	2020-09-07	First release

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