Power rail Reference Design for Versal™ AI Edge/Prime series Gen 2

About this document

Scope and purpose

This document provides reference design to power Versal™ AI Edge/Prime series Gen 2 FPGA family. This can be taken as a reference for designing power solution for other devices of AI Edge/Prime series Gen2.

Intended audience

This document is intended for hardware designers working on design with Versal™ AI Edge/Prime Gen 2 FPGA family.

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1 Introduction

Infineon's integrated POL voltage regulators deliver benchmark efficiency and dramatically reduce the system size. Target applications for integrated point-of-load regulator include servers, storage, routers and switches, telecom base stations, and embedded computing. Solutions with and without digital interfaces are available in single-output and multi-rail formats.

Reference design for Versal™ AI Edge Series and Prime Series Gen 2 devices series uses different Infineon's integrated POLs with COT architecture. COT control offers quick response to load and input voltage changes, making it suitable for load transients. COT control reduces the number of external components and simplify the design compared to other control methods.

TDA38806 and TDA38725A used in this reference design uses a fast Constant On-Time (COT) control scheme. TDA38806 gives an analog power rail, whereas TDA38725A gives digital power rail.

The TDA38806 is a 6 A fully integrated and highly efficient DC - DC Buck regulator. It uses a fast Constant On-Time (COT) control scheme, which simplifies the design efforts and achieves fast control response during the transients while maintaining excellent line and load regulation. It can operate over a wide range of input voltage (2.7 V to 16 V) using an external bias supply.

The TDA38725A OptiMOS™ IPOL is an easy-to-use, fully integrated and highly efficient synchronous buck regulator with PMBus interface supporting up to 25 A. The device uses Infineon's FAST Constant On-time engine for superior transient response. It is easily configured using Infineon's XDP™ Designer GUI and the configuration can be stored in the on-chip memory. It has a wide input voltage range of 3V to 17V. it supports output voltages from 0.25V to 5V.

0.8V/92A is the core power rail in this reference design. This is achieved with a combination of a multiphase controller (XDPE19283) and three power stages (TDA21590). XDPE19283 is a multiphase controller, which controls three TDA21590 (power stages). The TDA21590 is an integrated power stage contains a low quiescent current synchronous buck gate-driver IC which is co-packed with control and synchronous MOSFETs along with an active diode structure that achieves low VDS like a Schottky with very little reverse recovery charge. Three power stages are used to support output current requirement.

LDO (TLS835B2ELV) is used to produce 1.5V/0.2A rail. The OPTIREG™ linear TLS835B2ELV is a linear voltage regulator with high performance, very low dropout linear voltage and very low quiescent current. With an input voltage range of 3 V to 40 V and very low quiescent current of only 20 µA.

The main power source for this system is typically 12V (8V-16V Vin). This power source is fed to J100. This power source is used to power and enable 5V_AUX, 3V3_AUX, 1.8V/4.3A and 3.3V/3.8A rails. This power source is used to power 0.8V/92A, 1.5V/6A, 0.92A/5A, 1.5V/0.2A and 1.2V/5A. Detailed power rails and sequence is seen in the power-tree diagram in Figure 1. 6-layer PCB (DB703 REV1 board) with all power rails highlighted is shown in Figure 12.

Introduction

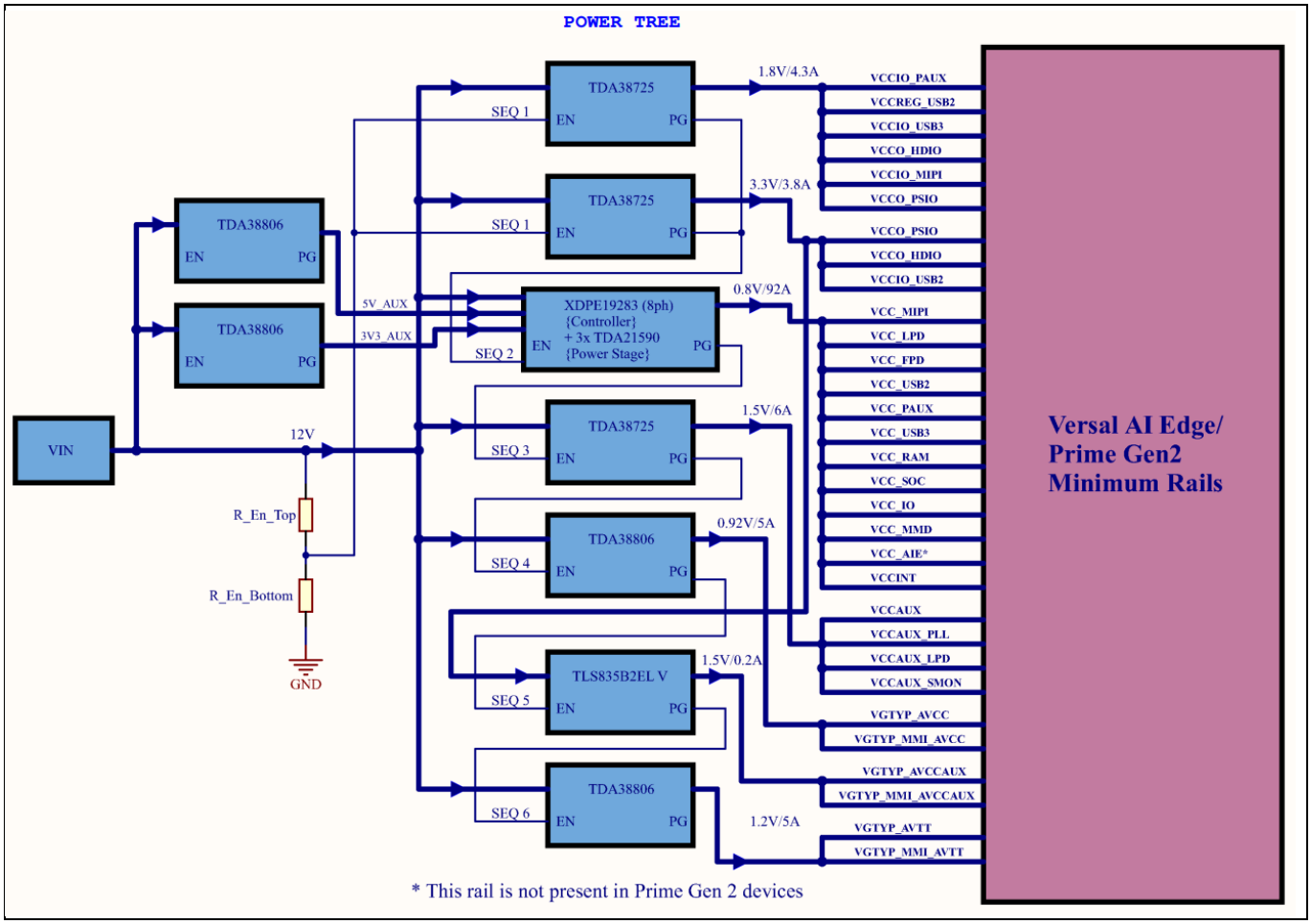


Figure 1 Power-tree with sequence of Versal™ AI Edge Series and Prime Series Gen 2 devices reference design

2 Design Parameters

Table 1 show the power rails specifications including voltages and tolerances, load currents, and sequence order for each rail. This reference design has been designed to meet Versal™ AI Edge Series and Prime Series Gen 2 devices power delivery specifications.

Table 1 Power rail description.

Sequence	Rail Group	Combined Rails	Nominal voltage (V)	DC Tolerance	AC Transient Margin	Step Load (%)	Load current (A)	IFX device
2	0V8 (digital)	VCC_MIPI, VCC_LPD, VCC_FPD, VCC_USB2, VCC_PAUX, VCC_USB3, VCC_RAM, VCC_SOC, VCC_IO, VCC_MMD, VCC_AIE*, VCCINT	0.8	±1%	±17mV	33	92	XDPE19283 (multiphase controller) + TDA21590 (3 power stages)
3	1V5 (digital)	VCCAUX, VCCAUX_PLL, VCCAUX_LPD, VCCAUX_SMON	1.5	±1%	±2%	100	6	TDA38725A
4	0V92 (analog)	VGTYP_AVCC**, VGTYP_MMI_AVCC**	0.92	±1%	±2%	70	5	TDA38806
5	1V5 (analog)	VGTYP_AVCCAUX**, VGTYP_MMI_AVCCAUX**	1.5	±1%	±2%	70	0.2	TDA38806
6	1V2 (analog)	VGTYP_AVTT**, VGTYP_MMI_AVTT**	1.5	±1%	±2%	70	5	TDA38806
1	1V8 (digital)	VCCIO_PAUX, VCCREG_USB2, VCCIO_USB3, VCCO_HDIO, VCCIO_MIPI, VCCO_PSIO	1.8	±1%	±2%	100	4.3	TDA38725A
1	3V3 (digital)	VCCO_PSIO, VCCO_HDIO, VCCIO_USB2	3.3	±1%	+2/-4%	100	3.8	TDA38725A
Assumes high toggle/clock rate, ~80% utilization - Customer designs will vary Assume current slew rate of 200A/us for VCCINT and VCC_AIE. All others 10A/us * Not present on Prime Series Gen2 devices ** AC noise limit of <10mVpp from 10 kHz to 80 MHz								

Figure 1 shows the power-tree and sequence of reference design for Versal™ AI Edge Series and Prime Series Gen 2 devices.

3 Schematic of each power rail

3.1 Auxiliary power supplies rails

3.1.1 3V3_AUX

Figure 2 shows schematic of 3V3_AUX. This is a 3.3V power supply using TDA38806. For layout guidance, see the corresponding device data sheet and EVM user guide.

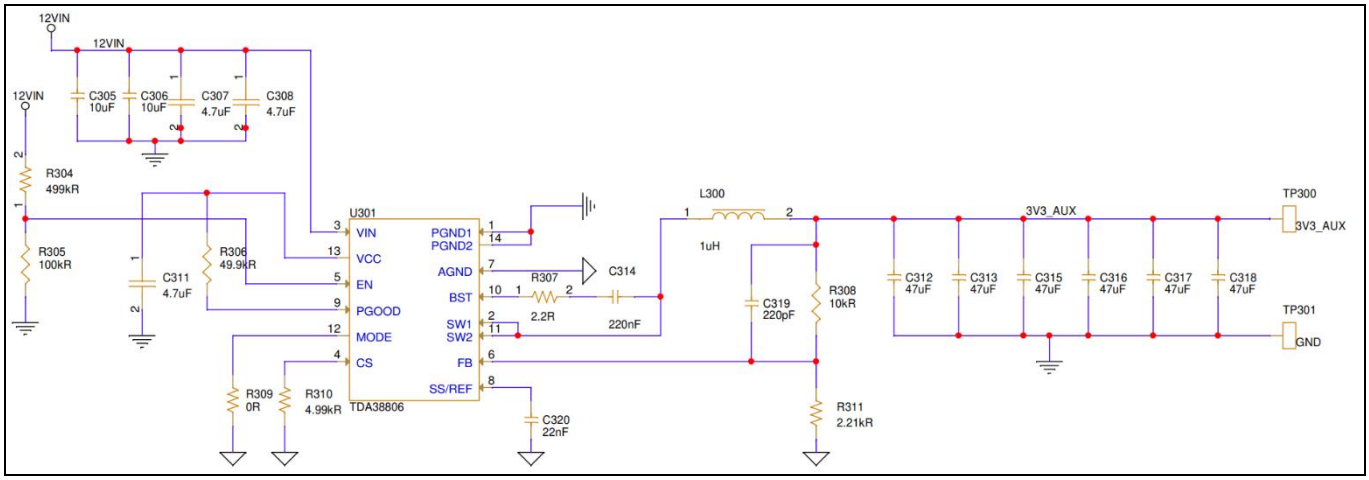


Figure 2 3V3_AUX rail using TDA38806

3.1.2 5V_AUX

Figure 3 shows schematic of 5V_AUX. This is a 5V power supply using TDA38806. For layout guidance, see the corresponding device data sheet and EVM user guide.

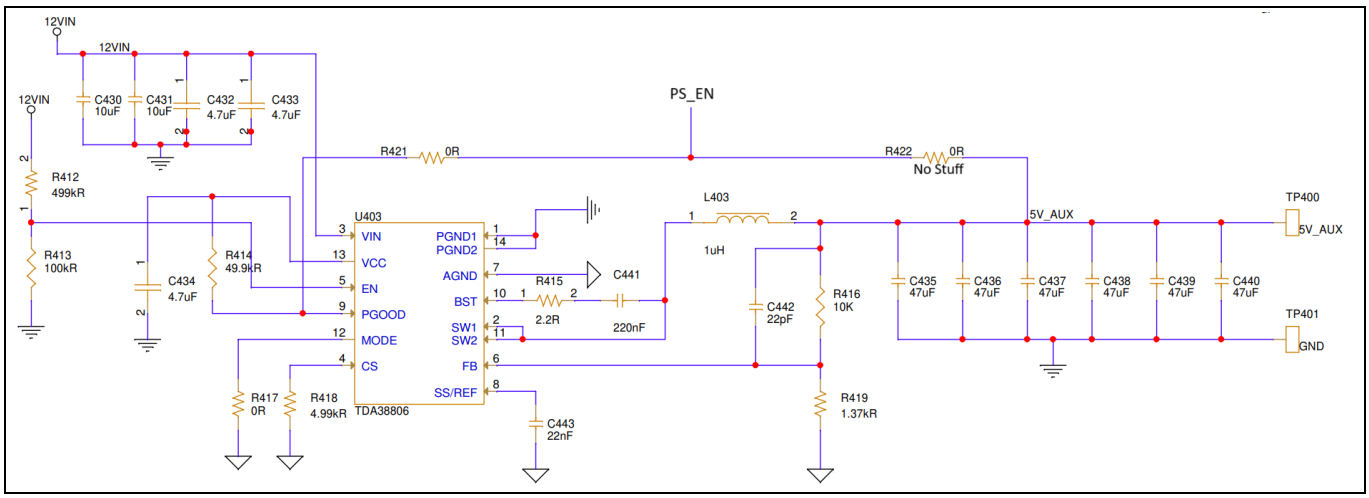


Figure 3 5V_AUX rail using TDA38806

3.2 1.8V/4.3A rail

Figure 4 shows schematic of 1.8V/4.3A rail. This is a 1.8V power supply using TDA38725A. For layout guidance, see the corresponding device data sheet and EVM user guide.

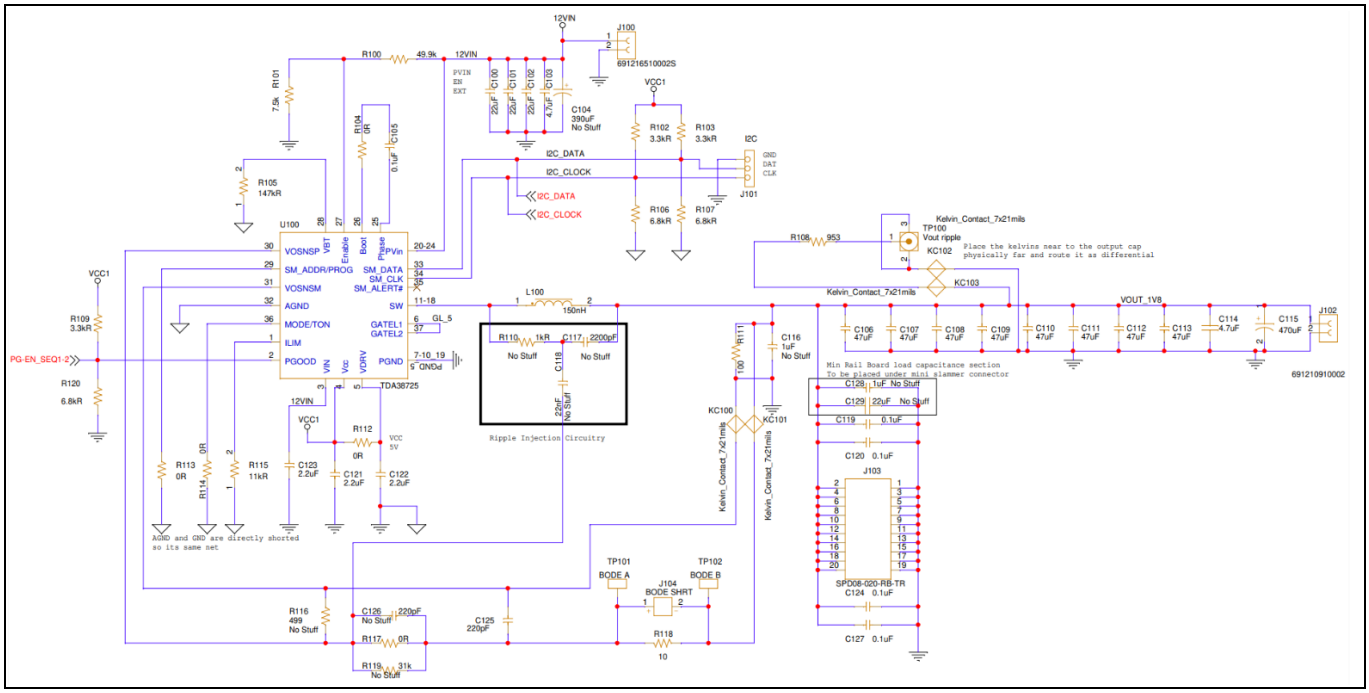


Figure 4 1.8V/4.3A rail using TDA38725A

3.3 3.3V/3.8A rail

Figure 5 shows schematic of 3.3V/3.8A rail. This is a 3.3V power supply using TDA38725A. For layout guidance, see the corresponding device data sheet and EVM user guide.

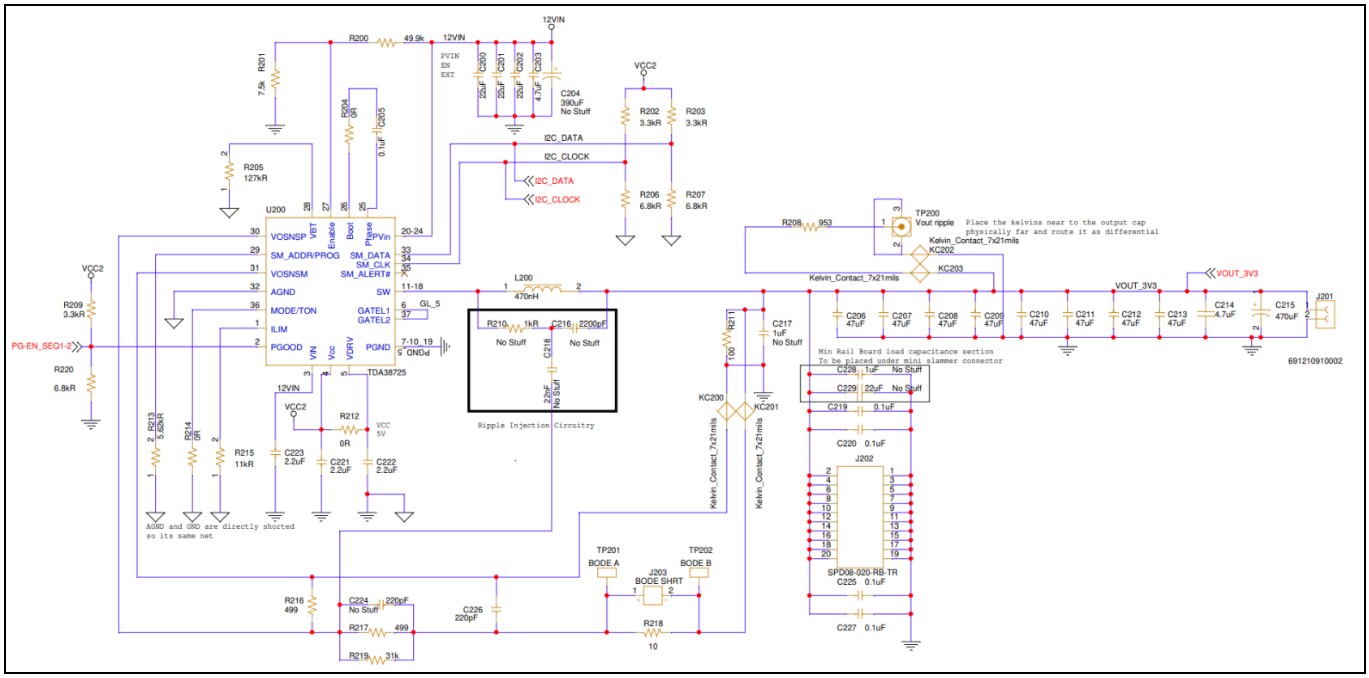


Figure 5 3.3V/3.8A rail using TDA38725A

3.4 0.8V/92A rail

Figure 6 and Figure 7 shows schematic of 0.8V/92A rail. For layout guidance, see the corresponding device data sheet and EVM user guide.

This is the core rail, using a multiphase controller (XPDE19283) and three number of power stages (TDA21590).

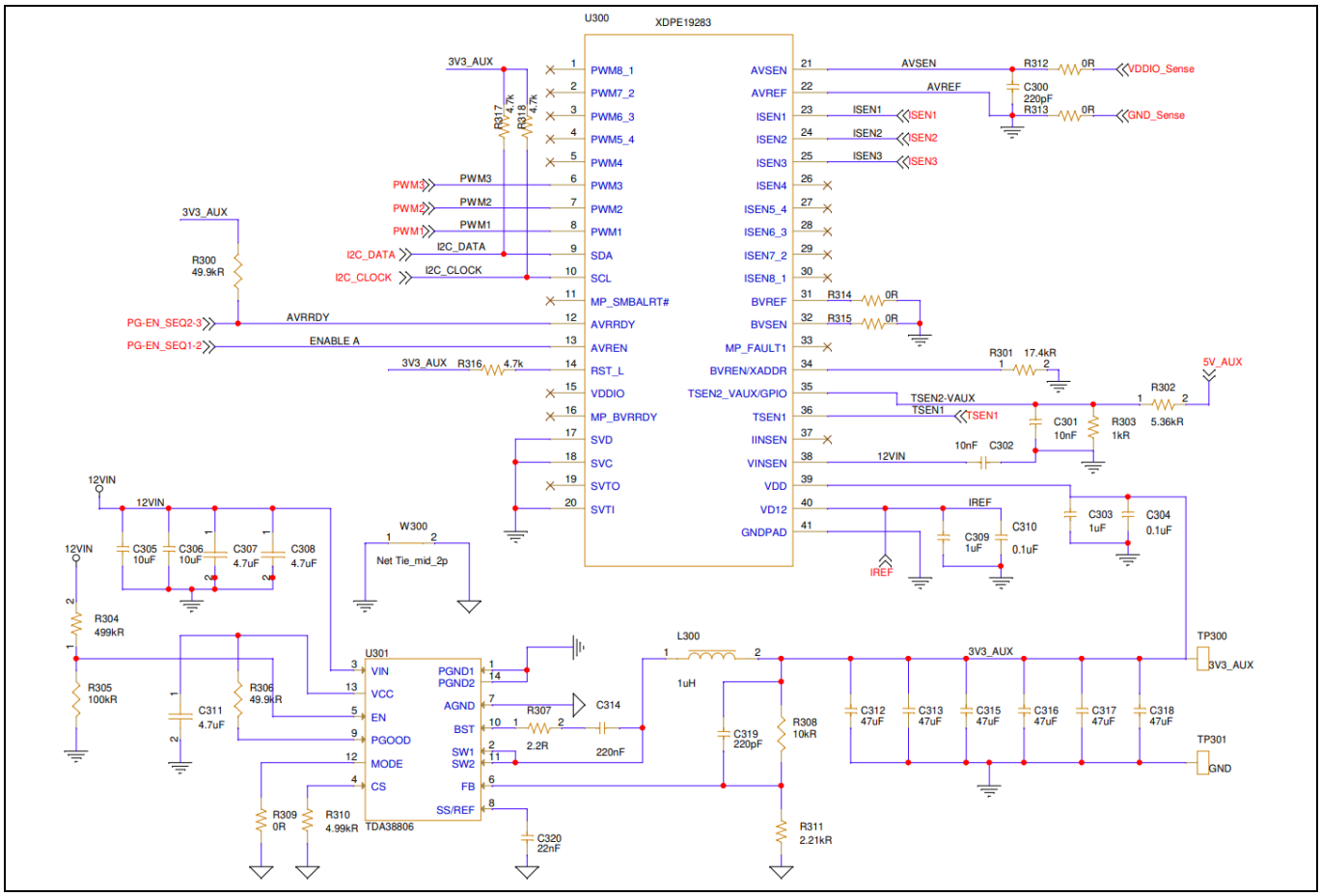


Figure 6 XDPE19283 as a controller to control three TDA21590(power stages)

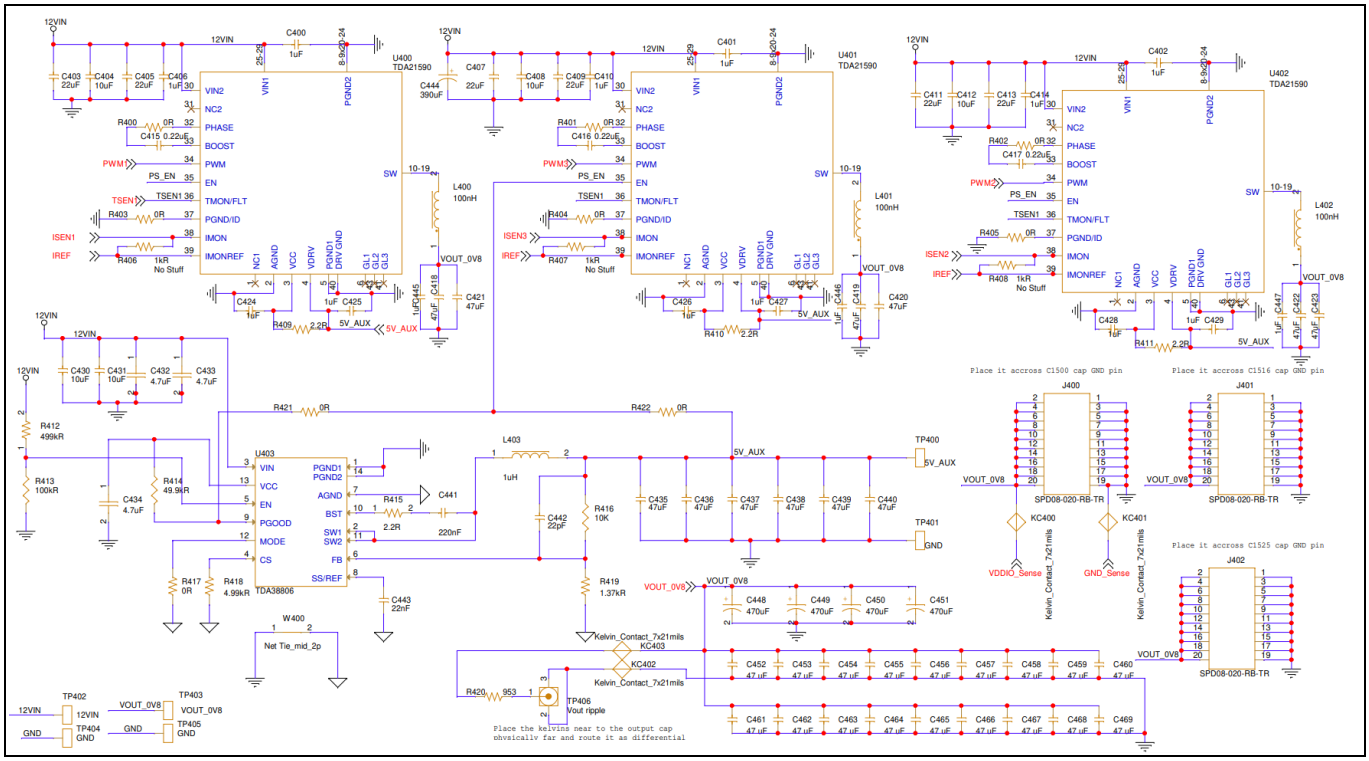


Figure 7 Three TDA21590 which forms 0.8V/92A rail

3.5 1.5V/6A rail

Figure 8 shows schematic of 1.5V/6A rail. This is a 1.5V power supply using TDA38725A. For layout guidance, see the corresponding device data sheet and EVM user guide.

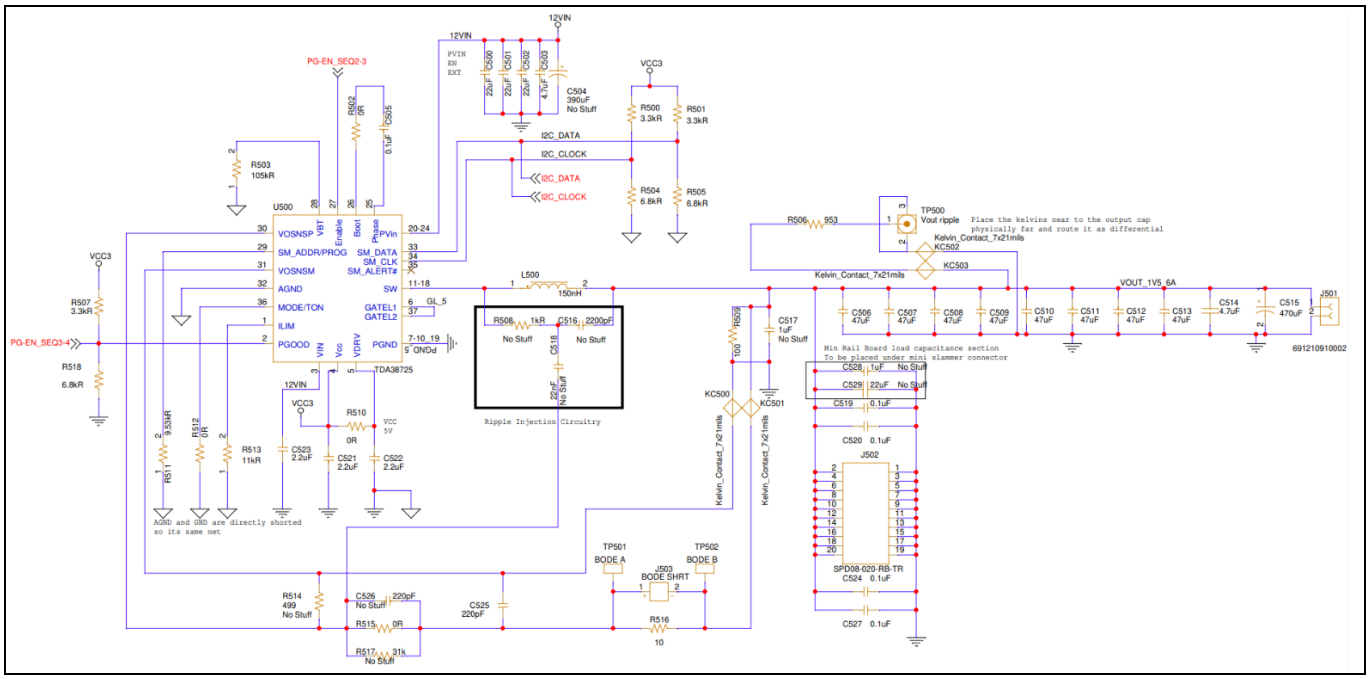


Figure 8 1.5V/6A rail using TDA38725A

3.6 0.92V/5A rail

Figure 9 shows schematic of 0.92V/5A rail. This is a 0.92V power supply using TDA38806. For layout guidance, see the corresponding device data sheet and EVM user guide.

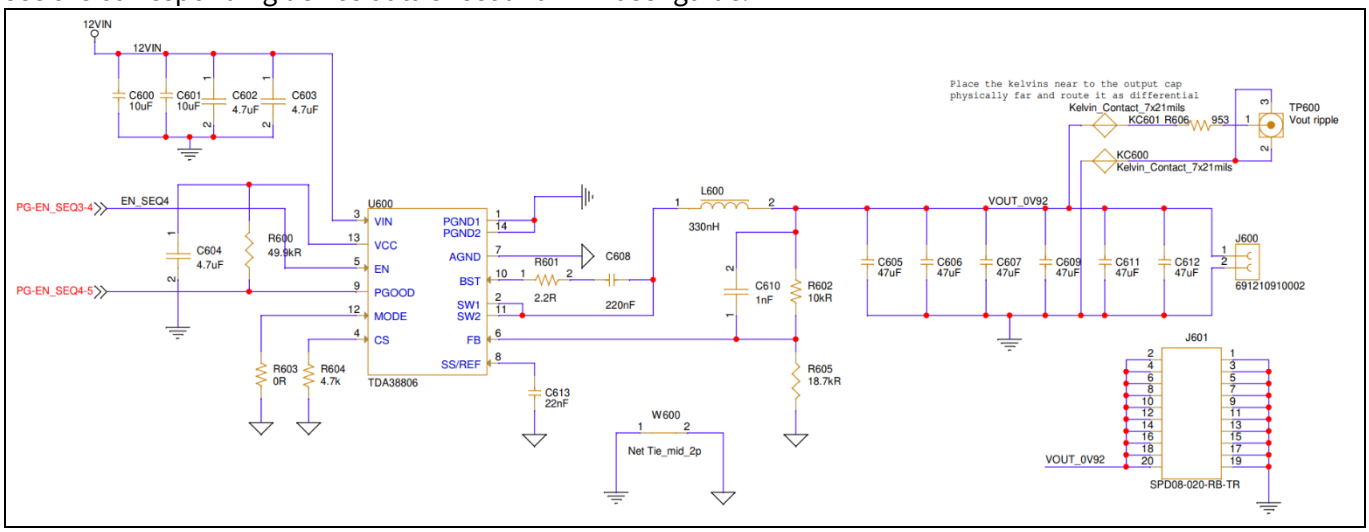


Figure 9 0.92V/5A rail using TDA38806

3.7 1.5V/0.2A rail

Figure 10 shows schematic of 1.5V/0.2A rail. This is a 1.5V power supply using TLS835B2EL V(LDO). For layout guidance, see the corresponding device data sheet and EVM user guide.

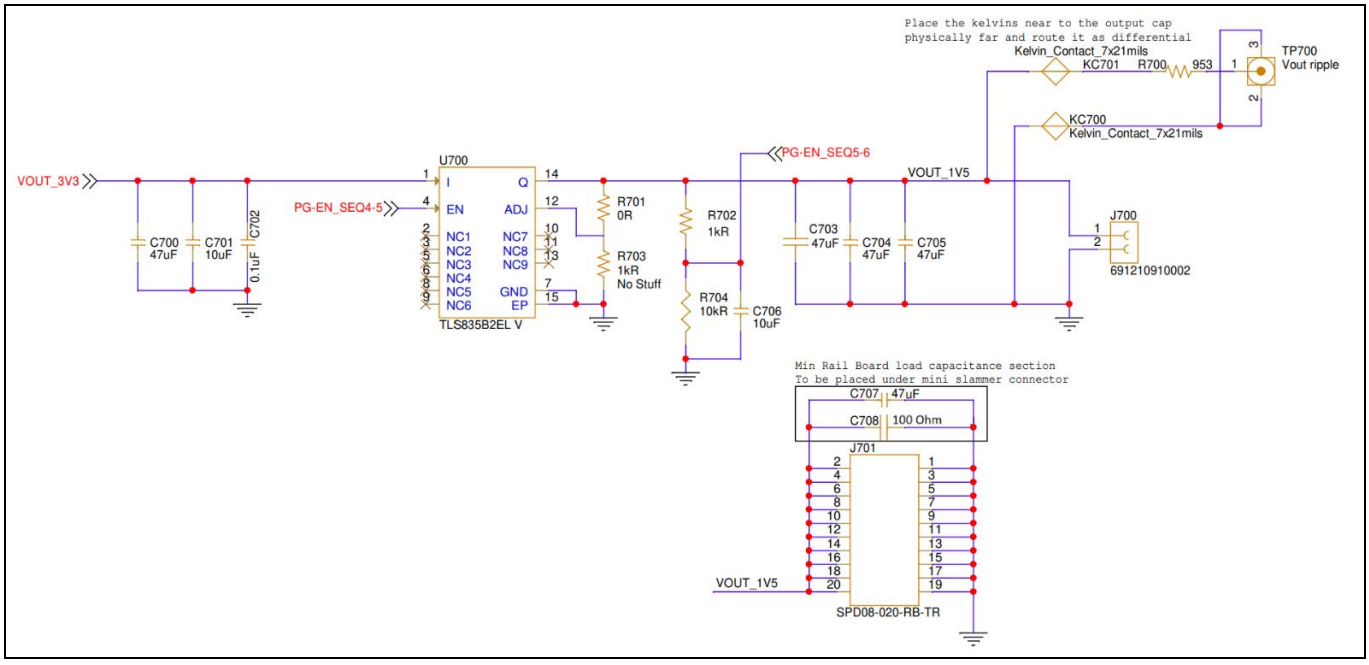


Figure 10 1.5V/0.2A rail using TLS835B2EL

3.8 1.2V/5A rail

Figure 11 shows schematic of 1.2V/5A rail. This is a 1.2V power supply using TDA38806. For layout guidance, see the corresponding device data sheet and EVM user guide.

Schematic of each power rail

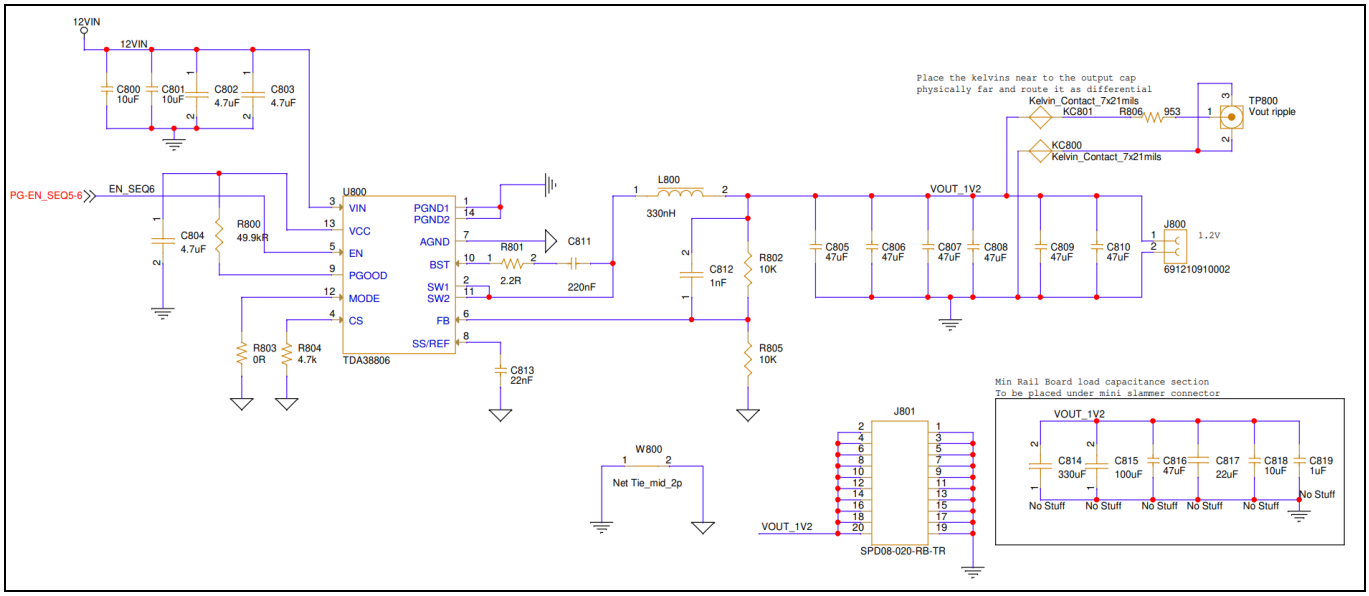


Figure 11 1.2V/5A rail using TDA38806

4 Board information

AMD VERSAL™ AI CORE PDRD MIN RAIL DB703 REV1 board is shown in Figure 12.

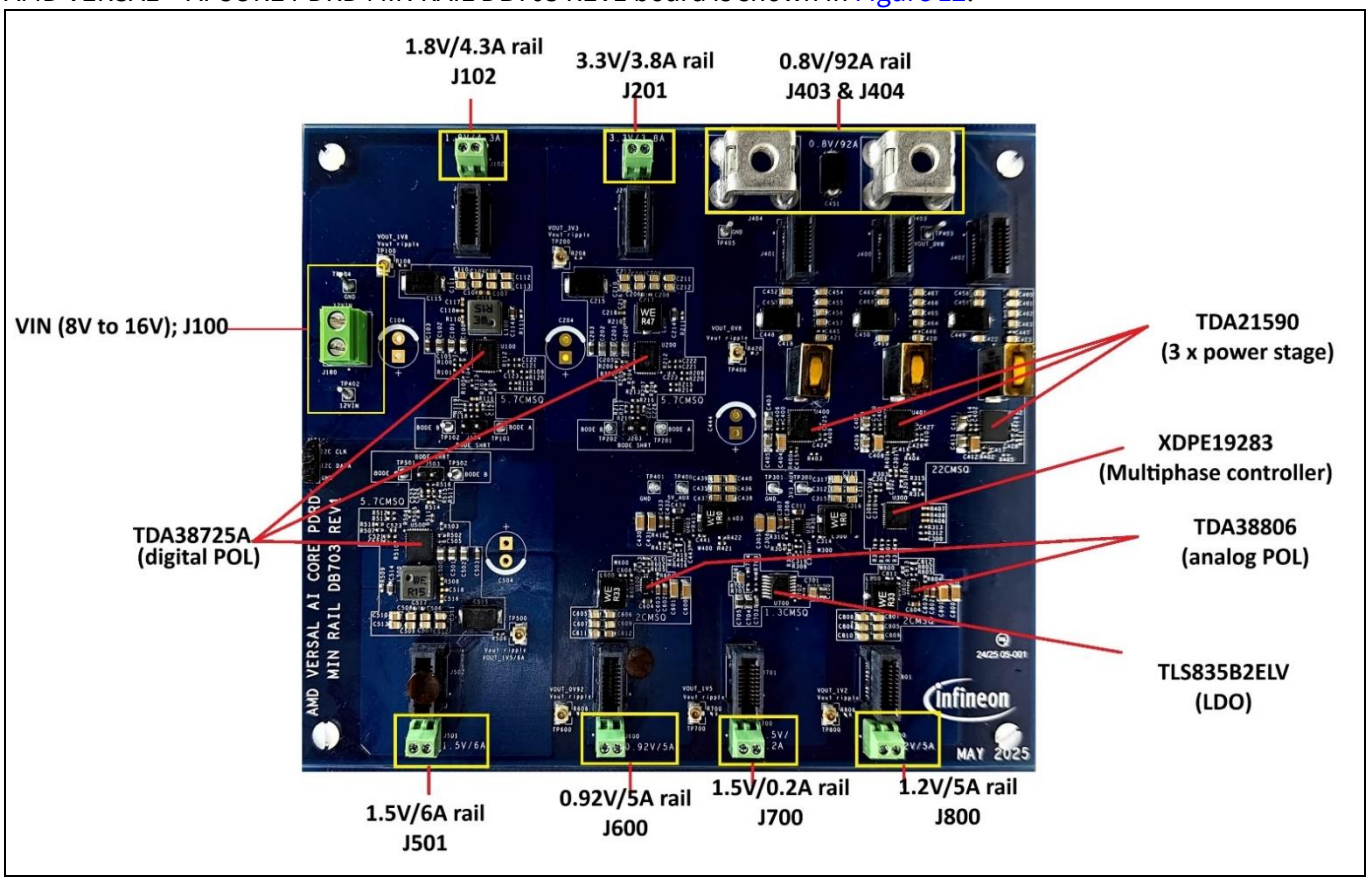


Figure 12 AMD VERSAL™ AI CORE PDRD MIN RAIL DB703 REV1 board

5 Inductor selection

The chosen power inductor value must satisfy the buck converter input and output specifications. The lower the inductor value, the smaller the size, thereby resulting in a high peak current.

5.1.1 Power inductor value – buck mode

The basic inductor current and voltage relation are $V_L = L\frac{dI_L}{dt}$. In a buck converter, the change in inductor current during the switch S1 on-time is equal to the change in current during the switch S1 off-time. The change in the inductor current (I_L) during the switch S1 on time is $\frac{\Delta I_L}{DT_{sw}}$.

$$L_{buck} = \frac{(V_{IN_max} - V_{OUT}) \times D_{Buck}}{\Delta I_L \times f_{sw}}$$

$\Delta I_{L,}$ can be fraction (0.2 to 0.6) of the $I_{part_capacity}$ to meet best transient performance

Where,

V_{IN_max} = Maximum input voltage

$I_{part_capacity}$ = maximum current rating of the part

5.1.2 Inductor selection

Inductor selected for this board are shown in Table 2.

Table 2 Selected inductors

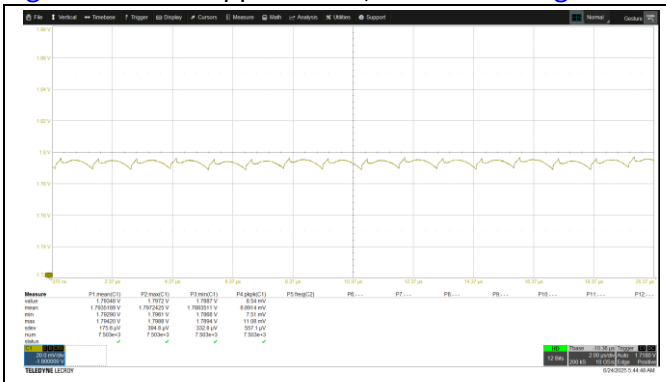
Reference designator	Description	Manufacture Part number
L100, L500	WE-XHMI SMT POWER INDUCTOR 6030;	744393440015
L200	FIXED IND 470NH 15A 2.75MOHM SMD	744316047
L300, L403	FIXED IND 1UH 11.5A 4.75MOHM SMD	744316100
L400, L401, L402	FIXED IND 100NH 37A 0.000125OHM	74431012007
L600, L800	FIXED IND 330NH 18.5A 1.75 MOHM	744316033

Self-resonating frequency of all the chosen inductors are high, which will help in reducing the switching noise at the output voltage. For example, 744393440015 has a self-resonating frequency of 191 MHz.

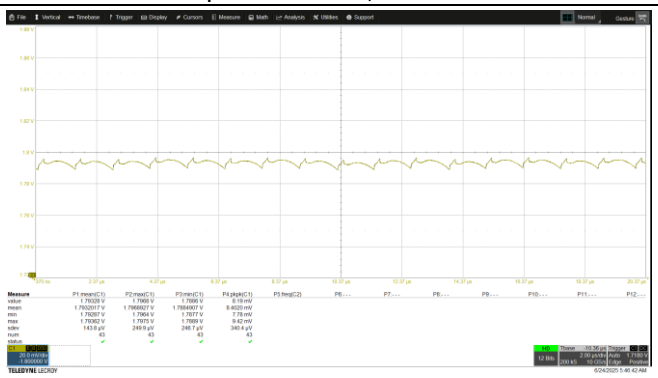
6 Test results

6.1 1.8V/4.3A rail

Figure 13 shows ripple of 1.8V/4.3A rail and Figure 14 shows transient response of 1.8V/4.3A rail.

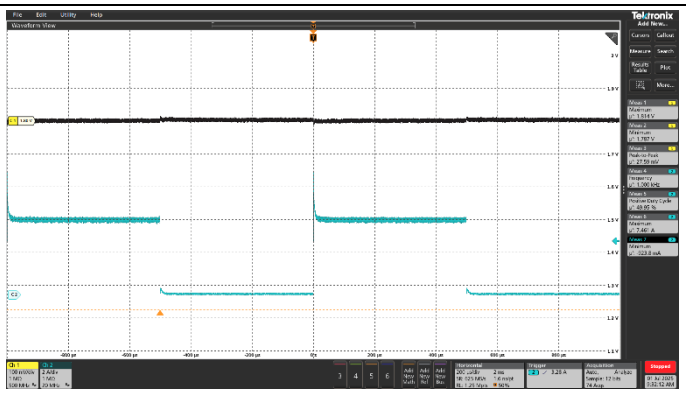


8.8mV pk-pk ripple - No load



8.5mV pk-pk ripple - Full load

Figure 13 Ripple at no-load and full load of 1.8V/4.3A rail; CH1=VOUT



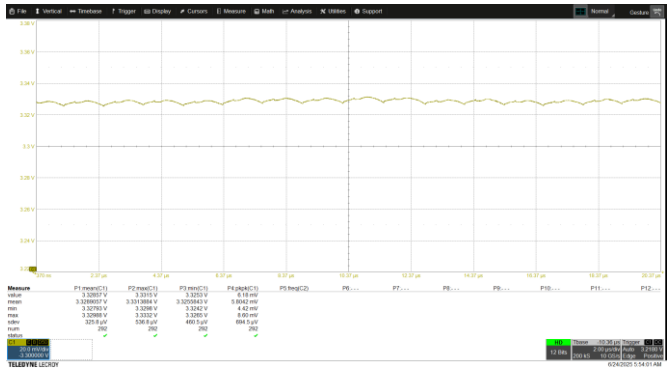
CH1: VOUT; CH2: IOUT

Overshoot =14mV and Undershoot = 13mV

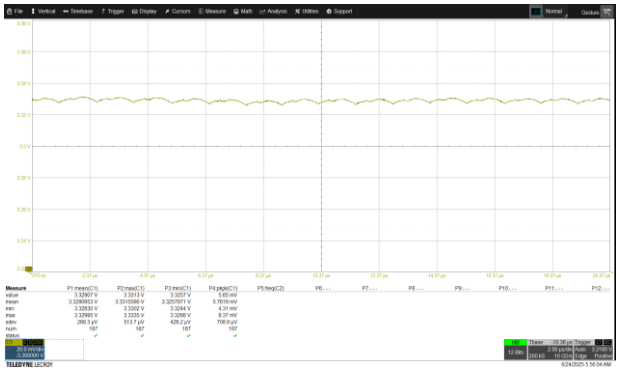
Figure 14 Load transient on 1.8V/4.3A rail from 0A to 4.3A at a slew rate of 10A/µS

6.2 3.3V/3.8A rail

Figure 15 shows ripple of 3.3V/3.8A rail and Figure 16 shows transient response of 3.3V/3.8A rail.

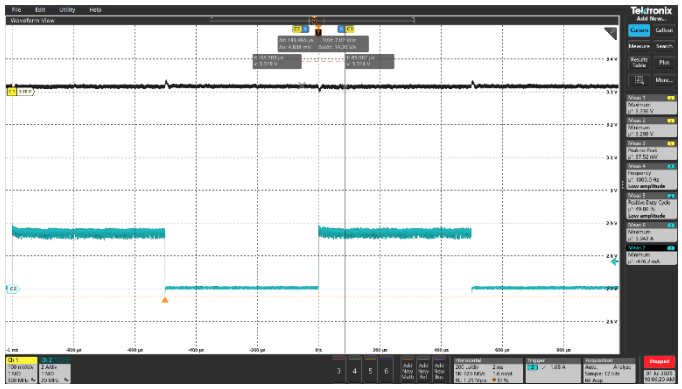


5.8mV pk-pk ripple - No load



5.7mV pk-pk ripple - Full load

Figure 15 Ripple at no-load and full load of 3.3V/3.8A rail



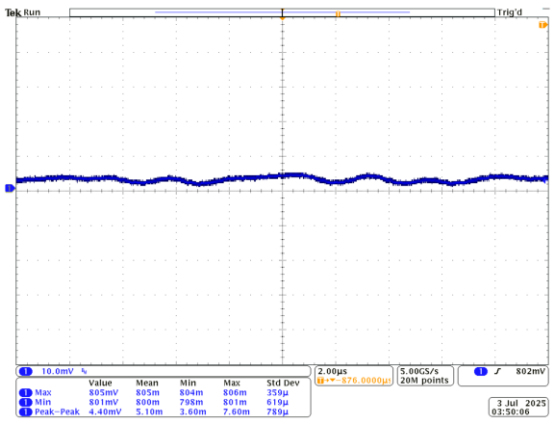
CH1: VOUT; CH2: IOUT

Overshoot = 36mV and Undershoot = 2mV

Figure 16 Load transient on 3.3V/3.8A rail from 0A to 3.8A at a slew rate of 10A/µS

6.3 0.8V/92A rail

Figure 17 shows ripple of 0.8V/92A rail and Figure 18 shows transient response of 0.8V/92A rail.



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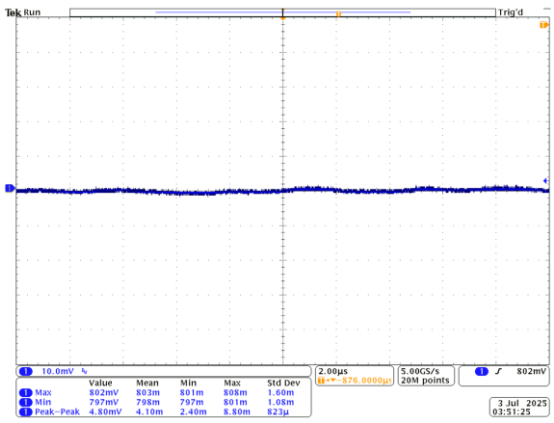
4.4mV pk-pk ripple - No load



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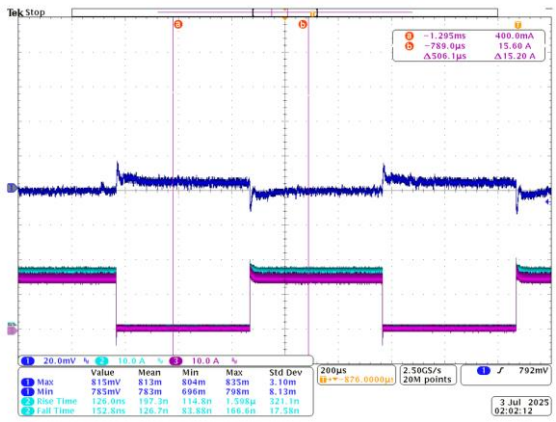
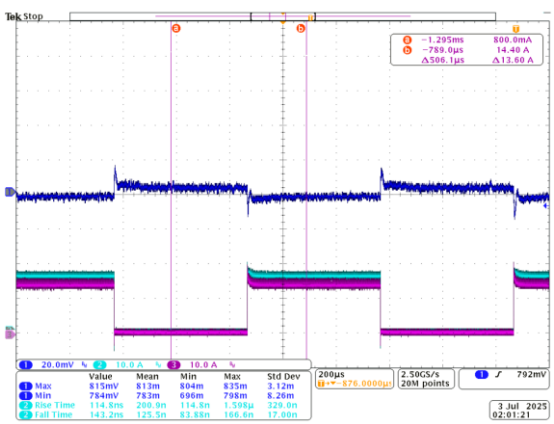
4.8mV pk-pk ripple - Full load

Figure 17 Ripple at no-load and full load of 0.8V/92A rail



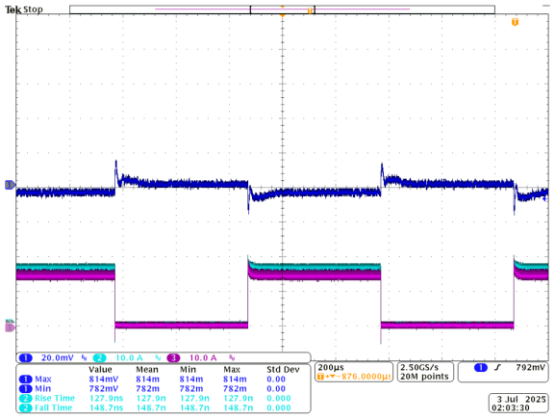
CH1: VOUT; CH2: IOUT1; CH3: IOUT2

Overshoot = 15mV and Undershoot = 15mV



CH1: VOUT; CH2: IOUT1; CH3: IOUT2

Overshoot = 15mV and Undershoot = 16mV



CH1: VOUT; CH2: IOUT1; CH3=IOUT2

Overshoot = 14mV and Undershoot = 18mV

Figure 18 Load transient on 0.8V/92A rail from no-load to 30A, 20A to 50A and 60A to 90A at a slew rate of 200A/µS

Load transient of 30A is realized using two mini-slammer, each mini-slammer sharing a load of 15A each as shown in Figure 18.

6.4 1.5V/6A rail

Figure 19 shows ripple measured on 1.5V/6A rail. Figure 20 shows transient response of 1.5V/6A rail.

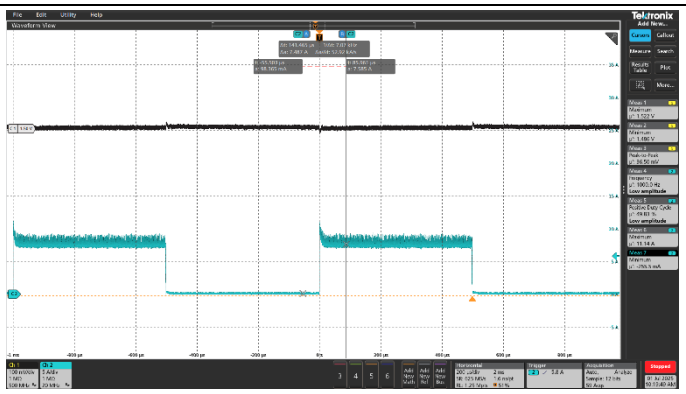


8.7mV pk-pk ripple - No load



8.7mV pk-pk ripple - Full load

Figure 19 Ripple at no-load and full load of 1.5V/6A rail



CH1: VOUT; CH2: IOUT

Overshoot = 22mV and Undershoot = 14mV

Figure 20 Load transient on 1.5V/6A rail from 0A to 6A at a slew rate of 10A/µS

6.5 0.92V/5A rail

Figure 21 shows ripple measurement of 0.92V/5A rail and Figure 22 shows transient response on 0.92V/5A rail.

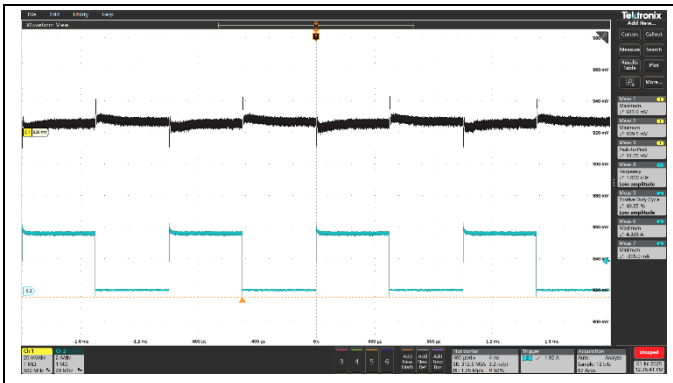


2.9mV pk-pk ripple - No load



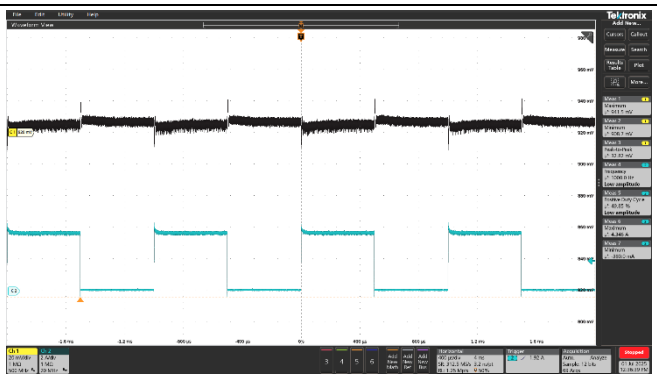
2.9mV pk-pk ripple - Full load

Figure 21 Ripple at no-load and full load of 0.92V/5A rail



CH1: VOUT; CH2: IOUT

Overshoot = 9.5mV and Undershoot = 14.6mV



CH1: VOUT; CH2: IOUT

Overshoot = 8.7mV and Undershoot = 21.5mV

Figure 22 Load transient on 0.92V/5A rail from 0A to 3.5A at a slew rate of 10A/µS and 1.5A to 5A at a slew rate of 10A/µS

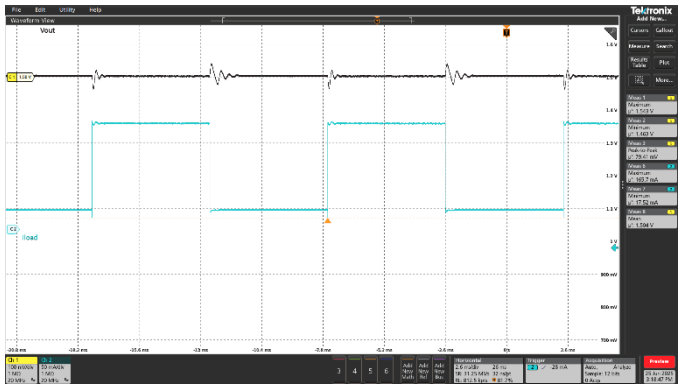
6.6 1.5V/0.2A rail

Figure 23 shows ripple of 1.5V/0.2A rail and Figure 24 shows transient response of 1.5V/0.2A rail.



0.9mV pk-pk ripple – Full load

Figure 23 Ripple at no-load and full load of 1.5V/0.2A rail



CH1: VOUT; CH2: IOUT

Overshoot = 43mV and Undershoot = 37mV

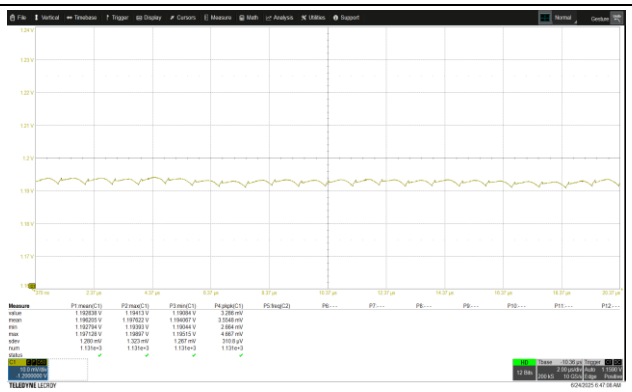
Figure 24 Load transient on 1.5V/0.2A rail from 0A to 1A with a load current of 30mA

6.7 1.2V/5A rail

Figure 25 shows ripple measured on 1.2V/5A rail at no-load and full load. Figure 26 shows transient response of 1.2V/5A rail.

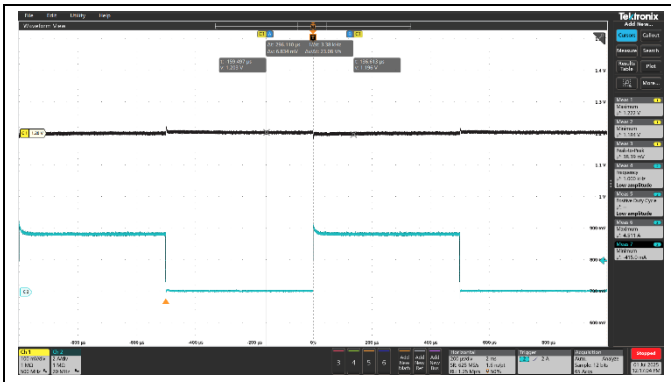


3.6mV pk-pk ripple - No load



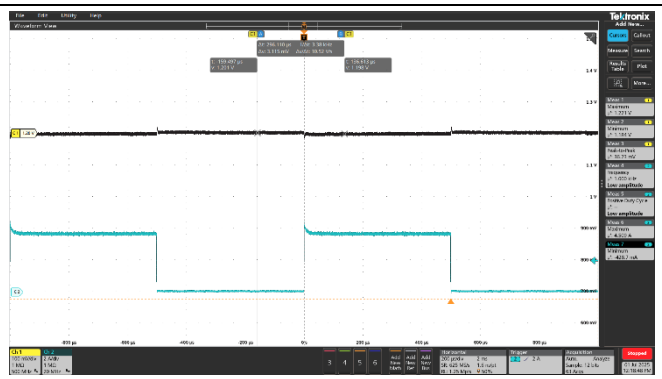
3.5mV pk-pk ripple - Full load

Figure 25 Ripple measured at no-load and full load on 1.2V/5A rail



CH1: VOUT; CH2: IOUT

Overshoot = 22mV and Undershoot = 16mV



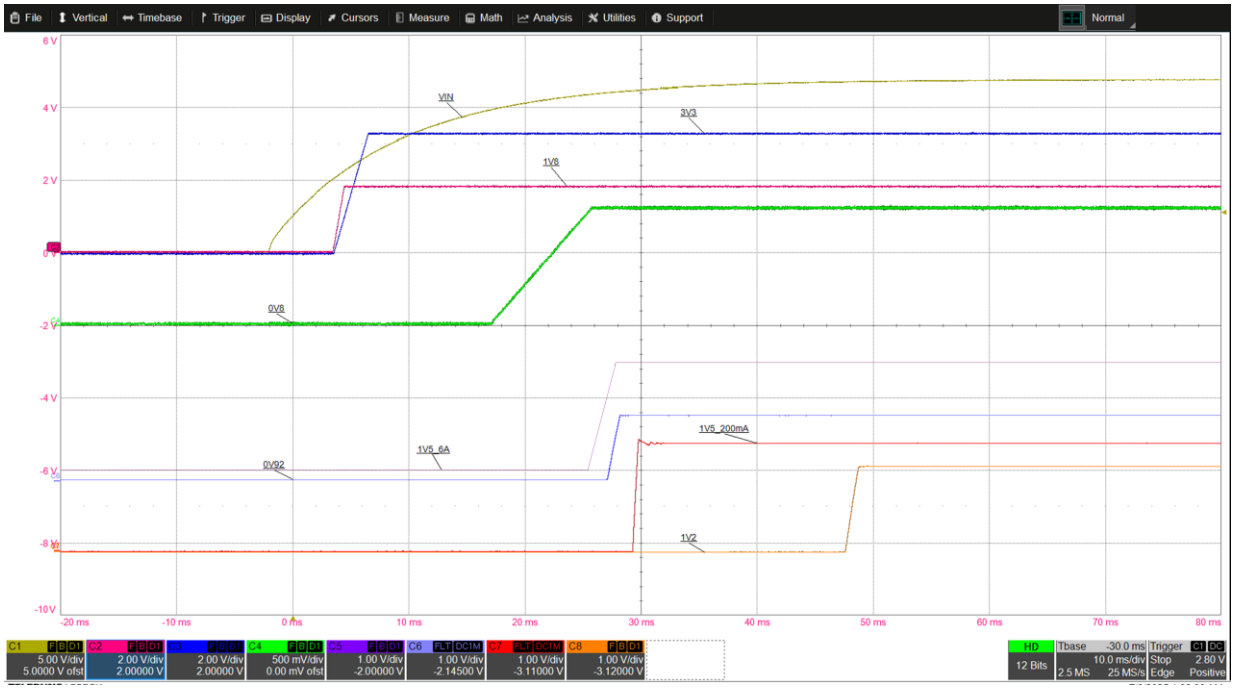
CH1: VOUT; CH2: IOUT

Overshoot = 21mV and Undershoot = 16mV

Figure 26 Transient response of 1.2V/5A rail from 0A to 3.5A at a slew rate of 10A/µS and 1.5A to 5A at a slew rate of 10A/µS

6.8 Sequence of the power rails

Figure 27 shows the sequence in which the power rails shall be tuned ON.



CH1: VIN; CH2:1.8V rail; CH3:3.3V rail; CH4:0.8V rail.
CH5:1.5V/6A rail; CH6:0.92V rail; CH7:1.5V rail; CH8: 1.2V rail

Figure 27 Sequence of which the power rails are turned ON

References

Datasheets

[1] TDA38806 – 6 A synchronous Buck regulator.

[2] TDA38725A OptiMOS iPOL - 40/25A Single-voltage Synchronous Buck Regulator with PMBusUSB

[3] XDPE19283D - Digital Multi-phase Controller; 8-phase Dual Loop Voltage Regulator

[4] TDA21590 - High Efficiency OptiMOS™ 90A Integrated internal Current Sense Power Stage

Guides

[5] TDA38806 P1V8 user guide

[6] User manual for TDA38725A evaluation board

Revision history

Document revision	Date	Description of changes
01	2025-07-02	Initial release
02	2026-05-05	Changes made in Header, corrected Versal™ AI Edge Series and Prime Series Gen 2 devices in Minimum Rails

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