Power rail Reference Design for Versal™ AI Edge/Prime Series Gen 2 - SOC Board (DB704 rev1)

About this document

Scope and purpose

This document provides a reference design for power rails for Versal™ AI Edge/Prime SOC board. This can be taken as a reference for designing power tree for other devices of AI Edge/Prime series Gen2.

Intended audience

This document is intended for hardware designers working on design with Versal™ AI Edge/ Prime Gen 2 FPGA family.

Table of contents

About this document **1**
Table of contents **2**
1 Introduction **3**
2 Design Parameters **5**
3 Schematic of each power rail **7**
3.1 5V_AUX, 3V3_AUX, 1V8/3A, 3V3/3A and 1V5/0.1A rails 7
3.2 1.2V/2A rail 7
3.3 0.92V/2A rail 8
3.4 0.92V/3A rail 8
3.5 1.2V/3A rail 8
3.6 1.5V/6A rail, 3.3V/0.6A rail, 1.8V/1.3A rail, 1.5V/3A rail, and 1.5V/0.1A rail 9
3.7 0.8V/30A rail 10
3.8 0.8V/60A rail and 0.8V/37A rail 10
4 Board information **12**
5 Inductor selection **13**
5.1.1 Power inductor value – buck mode 13
5.1.2 Inductor selection 13
6 Test results **14**
6.1 1.2V/2A rail 14
6.2 0.92V/2A rail 14
6.3 0.92V/3A rail 15
6.4 1.2V/3A rail 15
6.5 1.8V/1.3A rail 16
6.6 1.5V/3A rail 17
6.7 1.5V/6A rail 17
6.8 3.3V/0.6A rail 18
6.9 0.8V/30A rail 19
6.10 1.5V/0.1A rail 20
6.11 0.8V/60A rail 20
6.12 1.5V/0.1A rail 21
6.13 0.8V/37A rail 21
6.14 3.3V/3A rail 22
6.15 1.8V/3A rail 23
6.16 Sequence of the power rails 24
References **25**
Revision history **26**
Disclaimer **27**

1 Introduction

Infineon's integrated POL voltage regulators deliver benchmark efficiency and dramatically reduce the system size. Target applications for integrated point-of-load regulator include servers, storage, routers and switches, telecom base stations, and embedded computing. Solutions with and without digital interfaces are available in single-output and multi-rail formats.

Reference design for Versal™ AI core PDRD-SOC uses different Infineon's integrated POLs with COT architecture. COT control offers quick response to load and input voltage changes, making it suitable for load transients. COT control reduces the number of external components and simplify the design compared to other control methods.

TDA38806 and TDA38740 used in this reference design uses a fast Constant On-Time (COT) control scheme. Analog power rail from TDA38806, whereas digital power rail from TDA38740.

The IRPS5401 is a complete power management unit delivering up to 5 output voltages to processors, FPGA's and other multi-rail power systems. Allows combining outputs and/or the use of an external IR MOSFET™ Power Stage to increase output current to as high as 50A. The IRPS5401 switching regulators utilize fixed frequency emulated current mode control, and thus no external compensation is required.

The TDA38806 is a 6 A fully integrated and highly efficient DC - DC Buck regulator. It uses a fast Constant On-Time (COT) control scheme, which simplifies the design efforts and achieves fast control response during the transients while maintaining excellent line and load regulation. It can operate over a wide range of input voltage (2.7 V to 16 V) using an external bias supply.

The TDA38740 OptiMOS™ IPOL is an easy-to-use, fully integrated and highly efficient synchronous buck regulator with PMBus interface supporting up to 40 A. The device uses Infineon's FAST Constant On-time engine for superior transient response. It is easily configured using Infineon's XDP™ Designer GUI and the configuration can be stored in the on-chip memory. It has a wide input voltage range of 3V to 17V. it supports output voltages from 0.25V to 5V.

0.8V/60A and 0.8V/37A is the core power rail in this reference design. This is achieved with a combination of a multiphase controller (XDPE19283) and three power stages (TDA21590). XDPE19283 is a multiphase controller, which controls three TDA21590 (power stages). The TDA21590 is an integrated power stage contains a low quiescent current synchronous buck gate-driver IC which is co-packed with control and synchronous MOSFETs along with an active diode structure that achieves low VDS like a Schottky with very little reverse recovery charge. Three power stages are used to support output current requirement and transient response.

The main power source for this system is typically 12V (8V-16V Vin). This power source is fed to J100. This power source is used to power and enable 5V_AUX, 3V3_AUX, 1.8V/1.3A and 3.3V/0.6A rails. This power source is used to power 0.8V/30A, 1.5V/6A, 0.92A/2A, 1.5V/0.1A, 1.2V/2A, 1.5V/3A, 1.8V/3A, 3.3V/3A, 0.8V/37A, 0.92V/3A, 1.5V/0.1A, 1.2V/3A and 0.8V/60A. Detailed power rails and sequence is seen in the power-tree diagram in Figure 1. 6-layer PCB (DB704 REV1 board) with all power rails highlighted is shown in Figure 10.

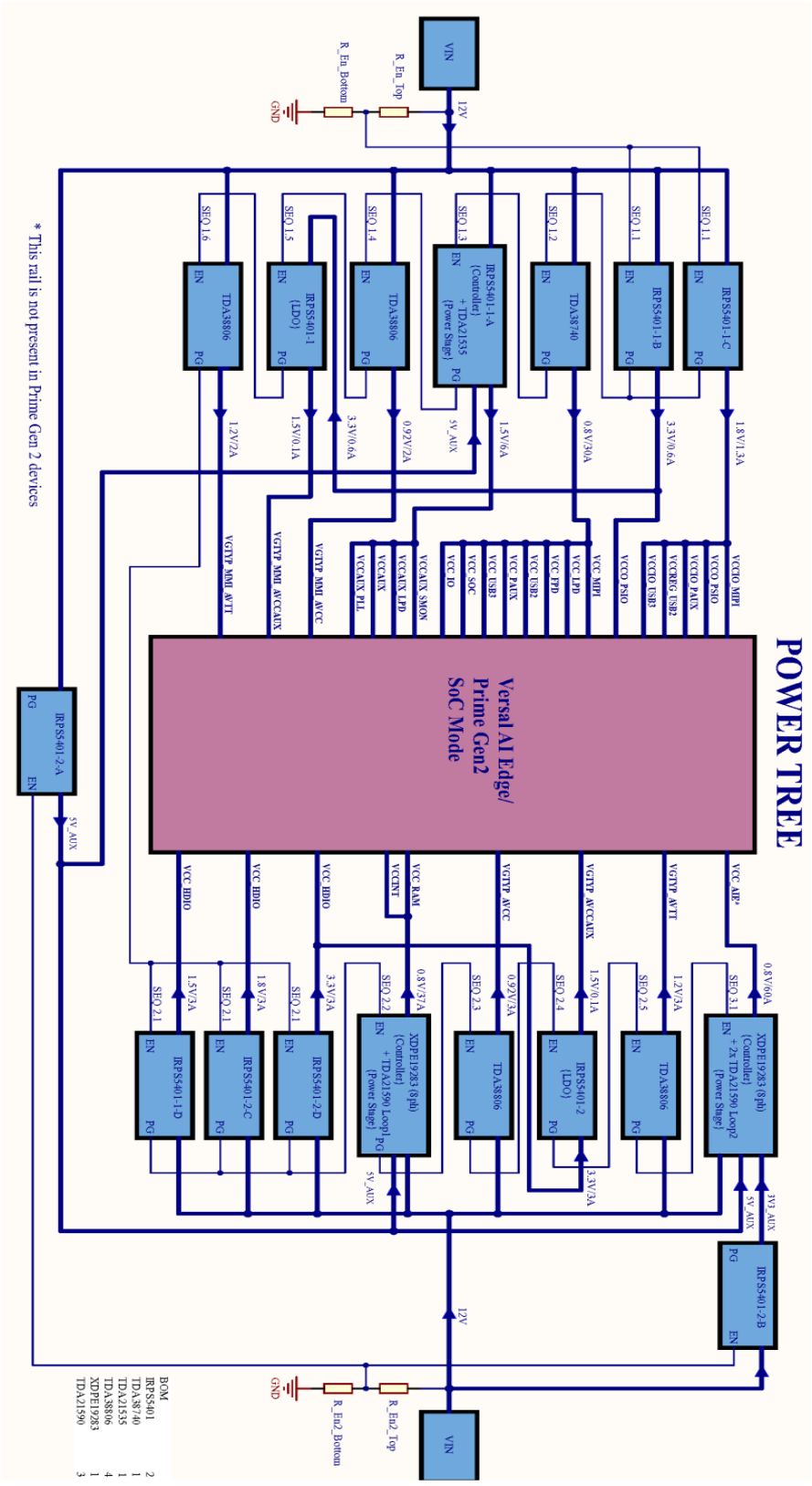


Figure 1 Power-tree with sequence of VERSAL™ AI Edge/ Prime Gen2 SoC Mode

2 Design Parameters

Table 1 show the power rails specifications including voltages and tolerances, load currents, and sequence order for each rail. This reference design has been designed to meet AMD Versal™ AI Edge Series and Prime Series Gen 2 devices in SOC Mode power delivery specifications.

Table 1 Power rail description.

Sequence	Rail Group	Combined Rails	Nominal voltage (V)	DC Tolerance	AC Transient Margin	Step Load (%)	Load current (A)	IFX device
1.2	0V8 (digital)	VCC_MIPI, VCC_LPD, VCC_FPD, VCC_USB2, VCC_PAUX, VCC_USB3, VCC_RAM, VCC_SOC, VCC_IO	0.8	±1%	±2%	33	30	TDA38740
1.3	1V5 (digital)	VCCAUX, VCCAUX_PLL, VCCAUX_LPD, VCCAUX_SMON	1.5	±1%	±2%	100	6	IRPS5401-1-A (controller) + TDA21535 (power stages)
1.4	0V92 (analog)	VGTYP_MMI_AVCC**	0.92	±1%	±2%	70	2	TDA38806
1.5	1V5 (analog)	VGTYP_MMI_AVCCAUX**	1.5	±1%	±2%	70	0.1	IRPS5401-1-A
1.6	1V2 (analog)	VGTYP_MMI_AVTT**	1.2	±1%	±2%	70	2	TDA38806
1.1	1V8 (digital)	VCCIO_PAUX, VCCREG_USB2, VCCIO_USB3, VCCIO_MIPI, VCCO_PSIO	1.8	±1%	±2%	100	1.3	IRPS5401-1-C
1.1	3V3 (digital)	VCCO_PSIO	3.3	±1%	+2/-4%	100	0.6	IRPS5401-1-B
2.2	0V8 (digital)	VCC_RAM, VCCINT	0.8	±1%	±17mV	33	37	XDPE19283 (8ph) (controller) + TDA21590 (power stage)
2.1	1V5 (digital)	VCCO_HDIO	1.5	±1%	±2%	100	3	IRPS5401-1-D
2.3	0V92 (Analog)	VGTYP_AVCC**	0.92	±1%	±2%	70	3	TDA38806
2.4	1V5 (Analog)	VGTYP_AVCCAUX**	1.5	±1%	±2%	70	0.1	IRPS5401-2
2.5	1V2 (Analog)	VGTYP_AVTT**	1.2	±1%	±2%	70	3	TDA38806
2.1	1V8 (Digital)	VCCO_HDIO	1.8	±1%	±2%	100	3	IRPS5401-2-C
2.1	3V3 (Digital)	VCCO_HDIO	3.3	±1%	±2/-4%	100	3	IRPS5401-2-D

Design Parameters

Sequence	Rail Group	Combined Rails	Nominal voltage (V)	DC Tolerance	AC Transient Margin	Step Load (%)	Load current (A)	IFX device
3.1	0V8_AIE (Digital)	VCC_AIE	0.8	±1%	±17mV	33	60	XDPE19283 (multiphase controller) + TDA21590 (2 power stage)
Assumes high toggle/clock rate, ~80% utilization - Customer designs will vary Assume the current slew rate of 200A/us for VCCINT and VCC_AIE. All others 10A/us * Not present on Prime Gen2 devices ** AC noise limit of <10mVpp from 10 kHz to 80 MHz								

Figure 1 shows the power-tree and sequence of reference design for Versal™ AI Edge Series and Prime Series Gen 2 devices in SOC Mode rail consolidation.

3 Schematic of each power rail

3.1 5V_AUX, 3V3_AUX, 1V8/3A, 3V3/3A and 1V5/0.1A rails

Figure 2 shows schematics of 5V_AUX, 3V3_AUX, VOUT_1V8_3A, VOUT_3V3_3A and VOUT_1V5_0A1, these are achieved using IRPS5401. For layout guidance, see the corresponding device data sheet and EVM user guide.

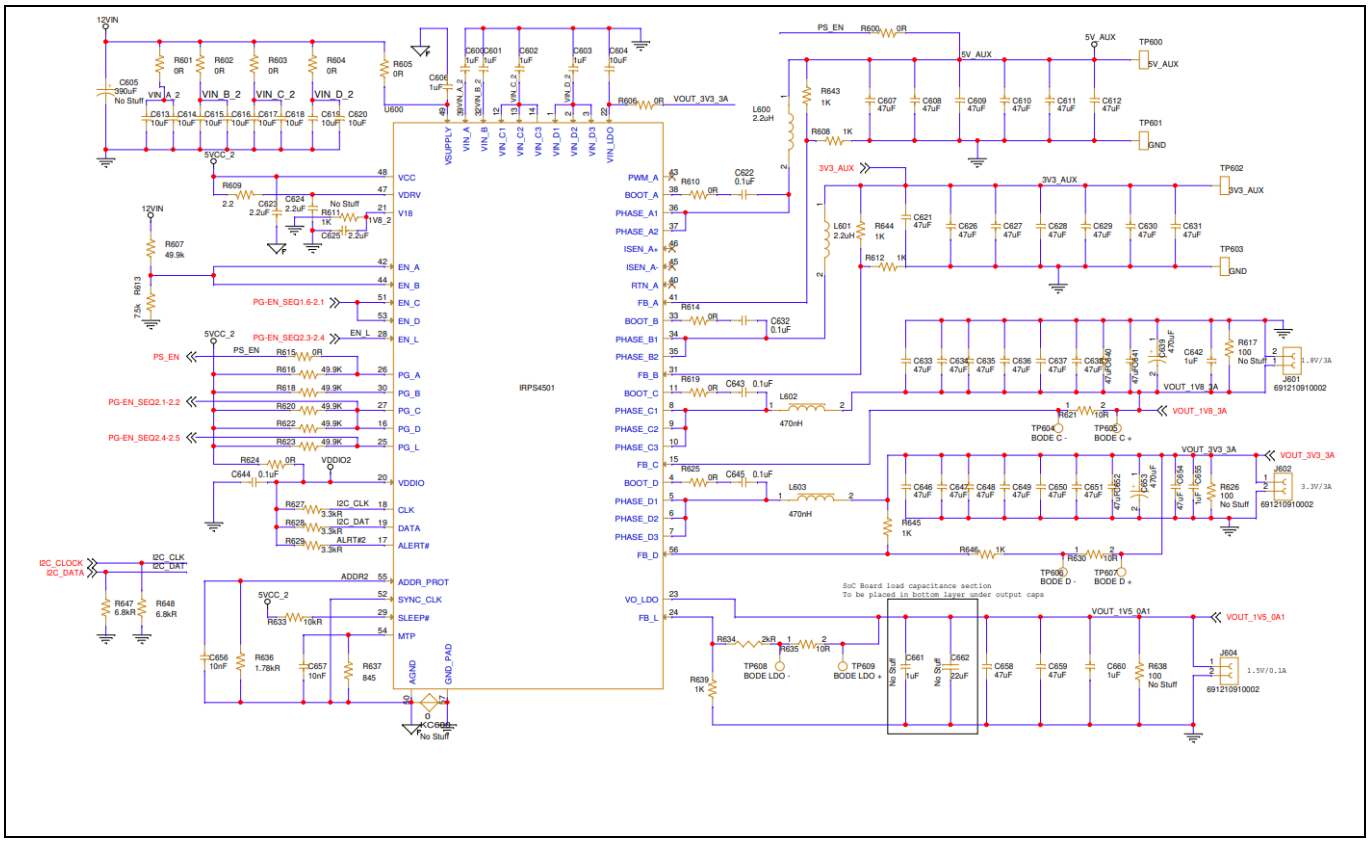


Figure 2 5V_AUX, 3V3_AUX, 1V8/3A, 3V3/3A and 1V5/0.1A rails using IRPS5401

3.2 1.2V/2A rail

Figure 3 shows the schematics of 1.2V/2A rail. This is a 1.2V power supply using TDA38806. For layout guidance, see the corresponding device data sheet and EVM user guide.

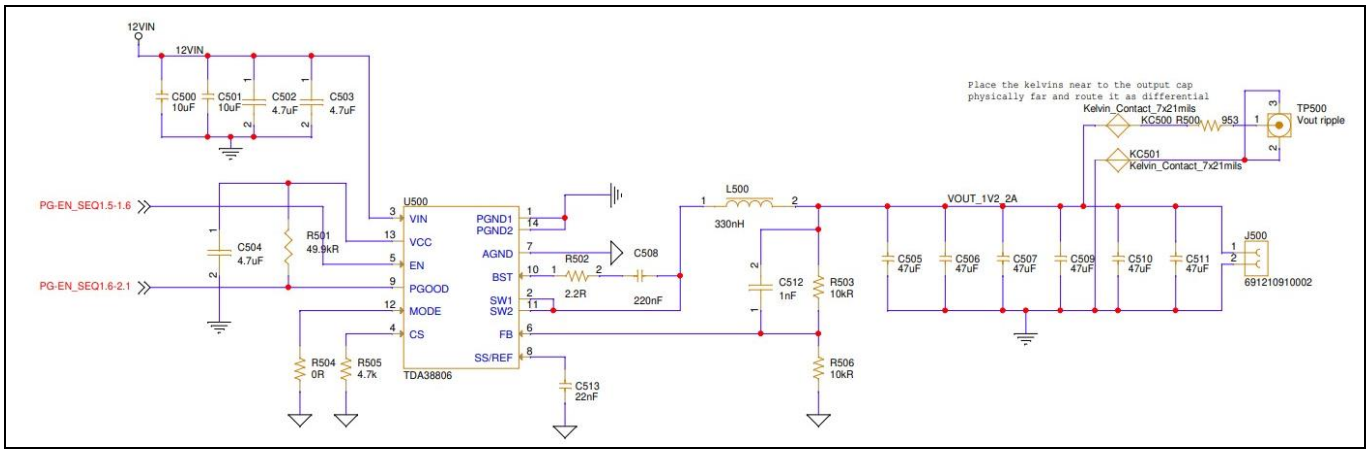


Figure 3 1.2V/2A rail using TDA38806

3.3 0.92V/2A rail

Figure 4 shows a schematic of 0.92V/2A rail. This is a 0.92V power supply using TDA38806. For layout guidance, see the corresponding device data sheet and EVM user guide.

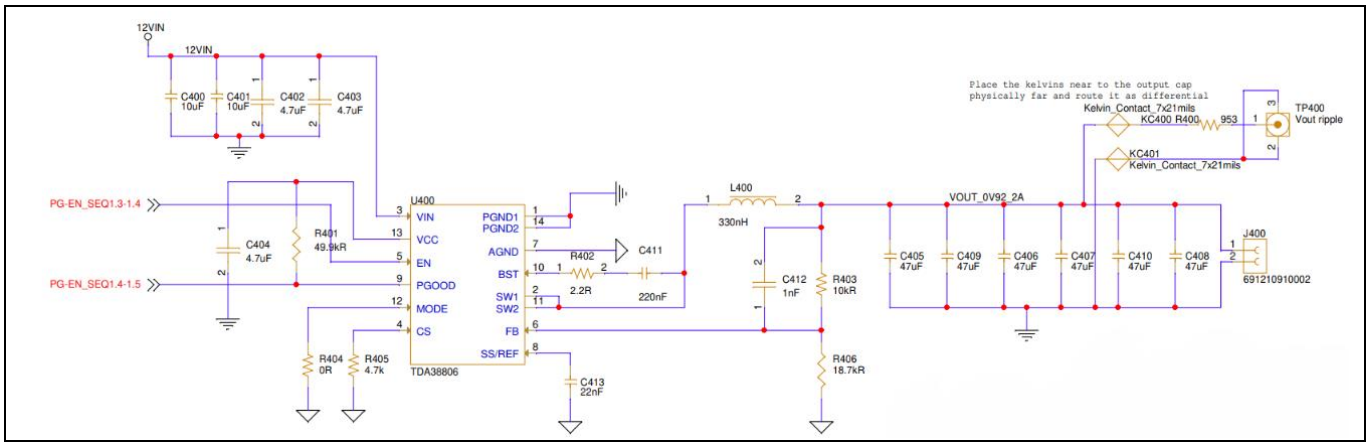


Figure 4 0.92V/2A rail using TDA38806

3.4 0.92V/3A rail

Figure 5 shows a schematic of 0.92V/3A rail. This is a 0.92V power supply using TDA38806. For layout guidance, see the corresponding device data sheet and EVM user guide.

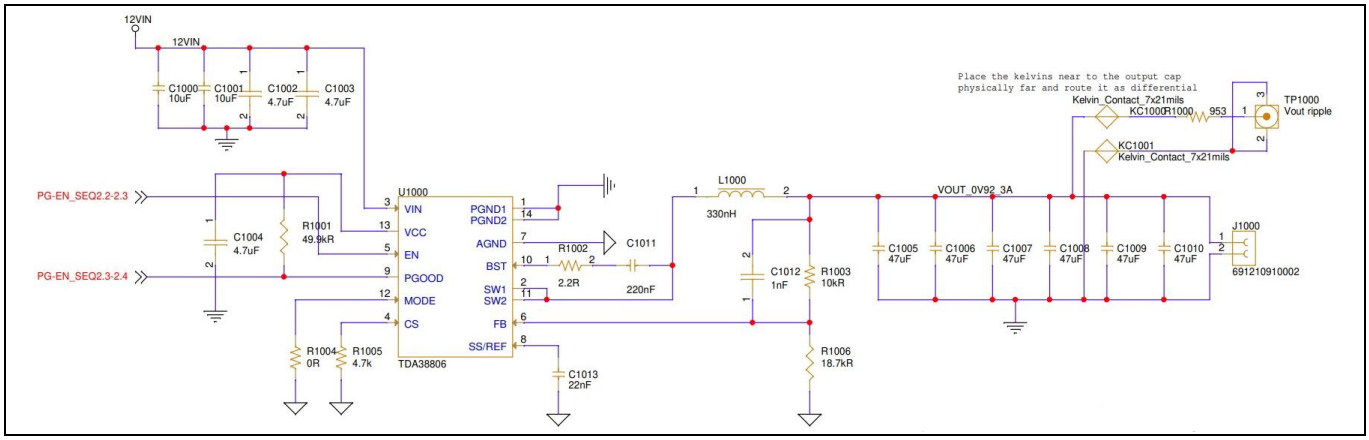


Figure 5 0.92V/3A rail using TDA38806

3.5 1.2V/3A rail

Figure 6 shows the schematic of 1.2V/3A rail. This is a 1.2V power supply using TDA38806. For layout guidance, see the corresponding device data sheet and EVM user guide.

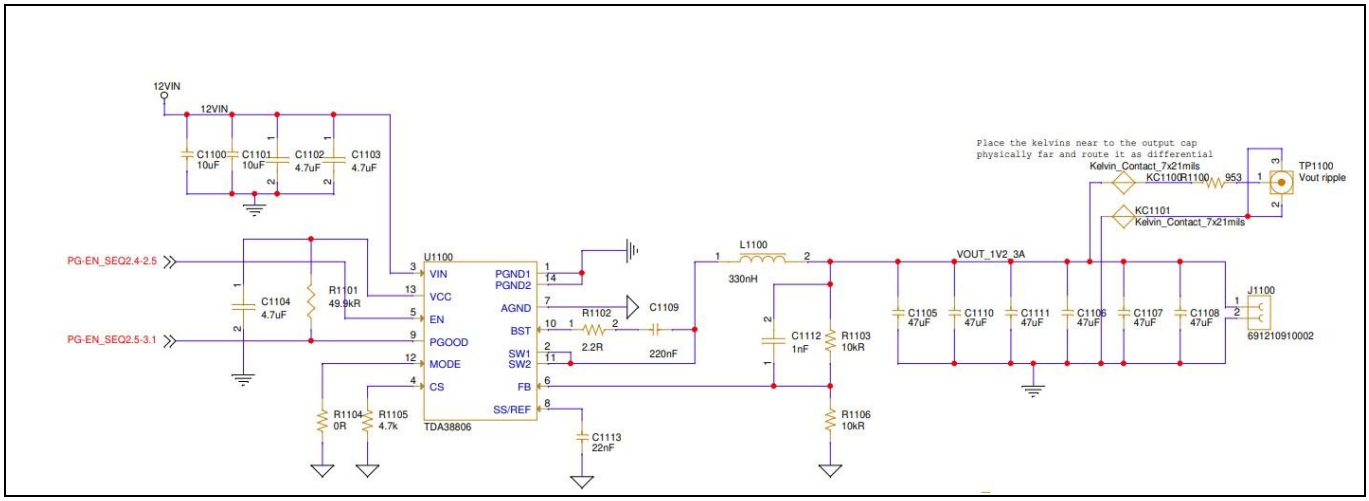
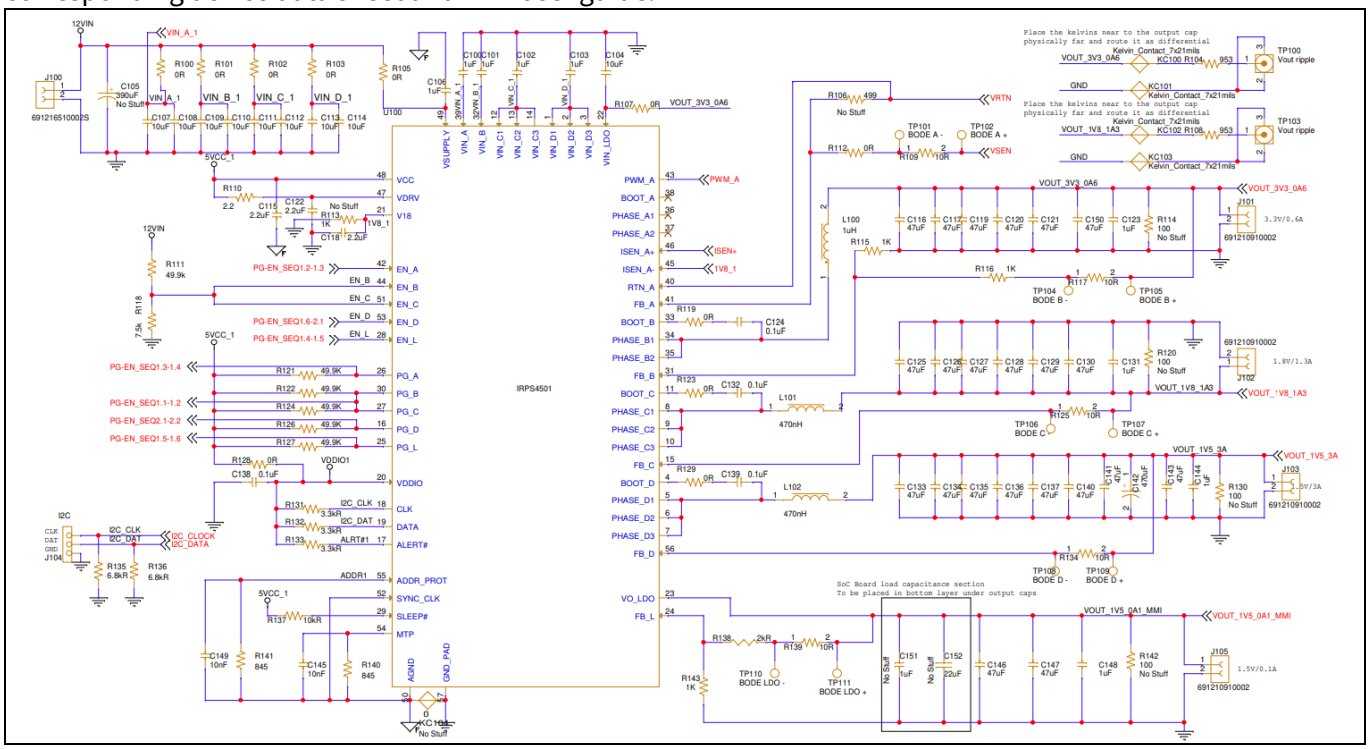


Figure 6 1.2V/3A rail using TDA38806

3.6 1.5V/6A rail, 3.3V/0.6A rail, 1.8V/1.3A rail, 1.5V/3A rail, and 1.5V/0.1A rail

Figure 7 shows the schematic of 1.5V/6A rail, 3.3V/0.6A rail, 1.8V/1.3A rail, 1.5V/3A rail, 1.5V/0.1A rail. These 3.3V, 1.8V, 1.5V and 1.5V power supply using IRPS5401. 1.5V/6A rail is from TDA21535. For layout guidance, see the corresponding device data sheet and EVM user guide.



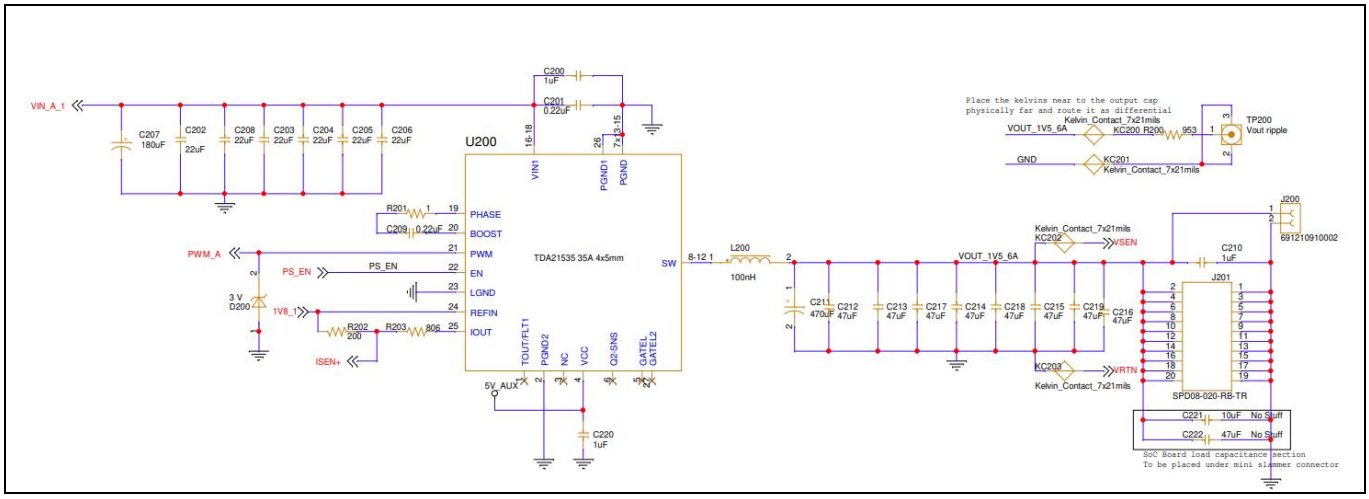


Figure 7 1.5V/6A rail, 3.3V/0.6A rail, 1.8V/1.3A rail, and 1.5V/0.1A rail using IRPS5401 and TDA21535

3.7 0.8V/30A rail

Figure 8 shows schematic of 0.8V/30A rail. This is a 0.8V power supply using TDA38740. For layout guidance, see the corresponding device data sheet and EVM user guide.

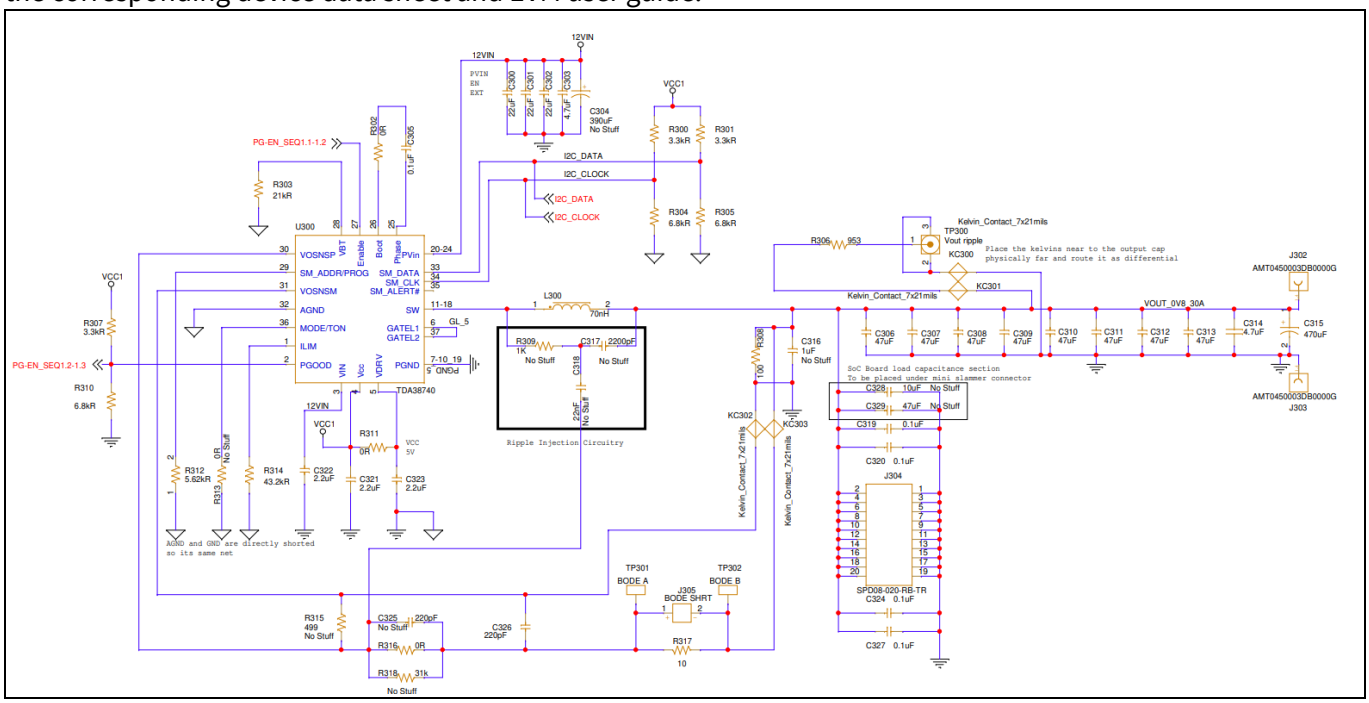


Figure 8 0.8V/30A rail using TDA38740

3.8 0.8V/60A rail and 0.8V/37A rail

Figure 9 shows a schematic of 0.8V/60A rail and 0.8V/37A. These are 0.8V power supply using TDA21590 and XDPE19283. Two phases are used for 0.8V/60A rail. For layout guidance, see the corresponding device data sheet and EVM user guide.

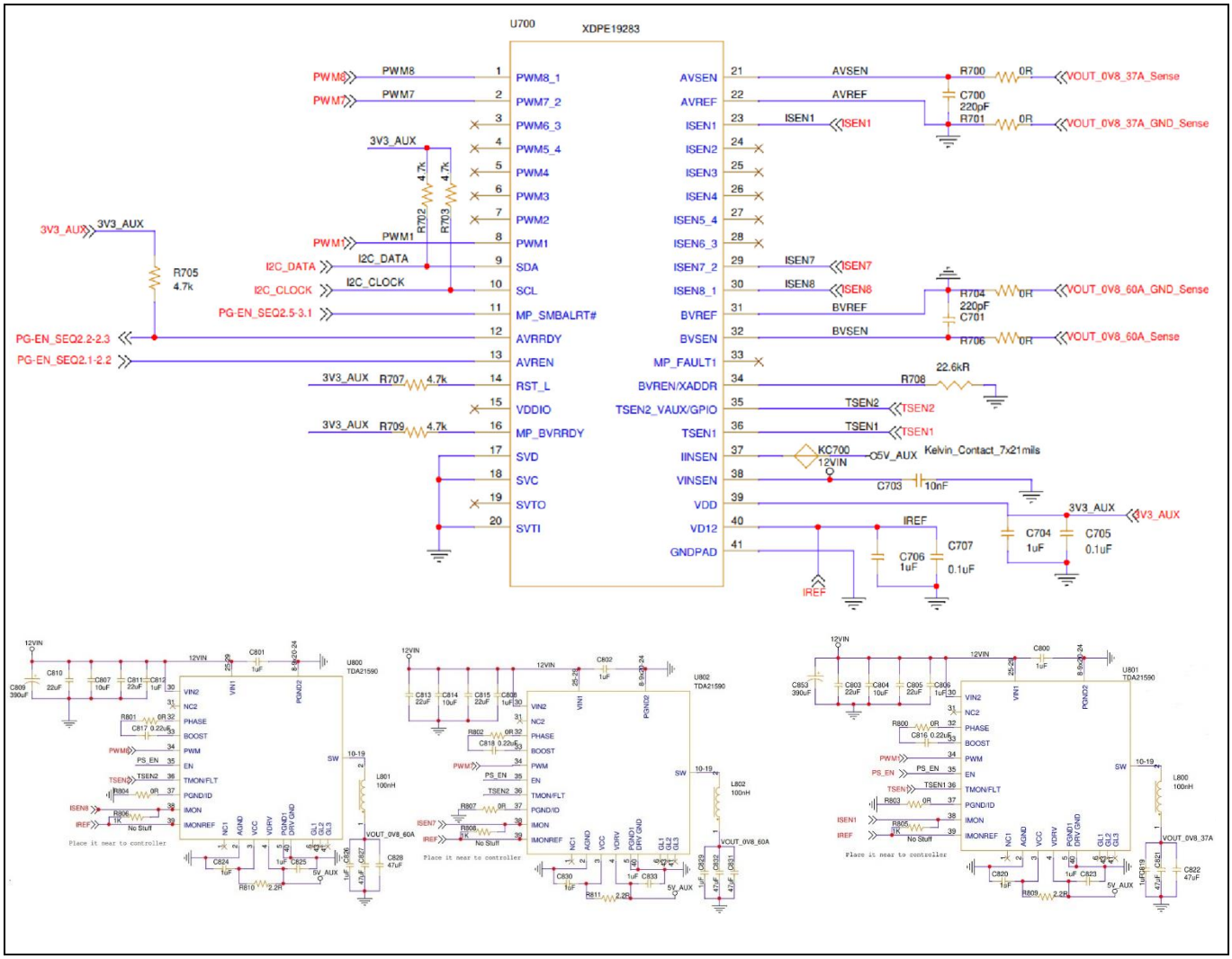


Figure 9 0.8V/60A rail and 0.8V/37A rail using TDA21590

4 Board information

AMD Versal™ AI Edge Series and Prime Series Gen 2 devices in SOC Mode rail consolidation board is shown in Figure 10.

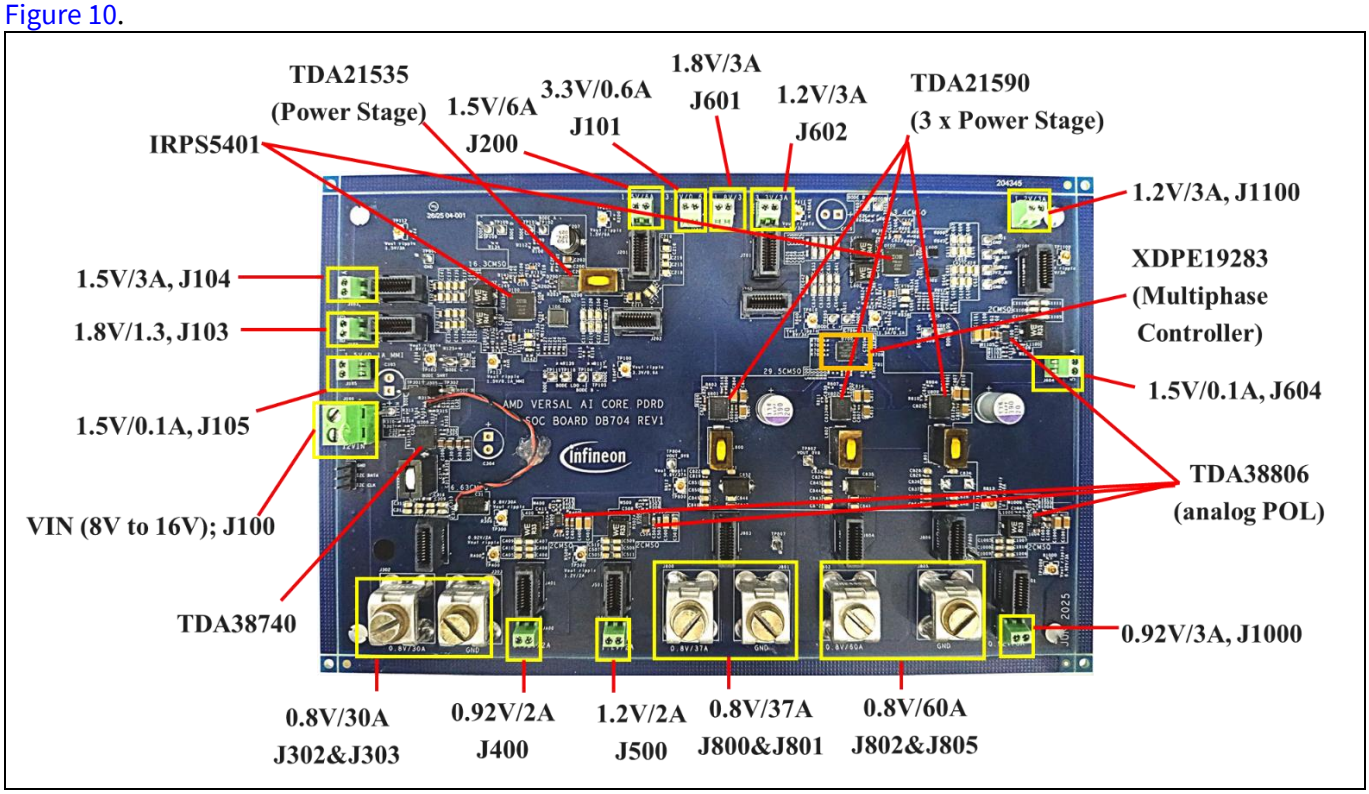


Figure 10 AMD Versal™ AI Edge Series and Prime Series Gen 2 devices in SOC Mode rail consolidation board

5 Inductor selection

The chosen power inductor value must satisfy the buck converter input and output specifications. The lower the inductor value, the smaller the size, thereby resulting in a high peak current.

5.1.1 Power inductor value – buck mode

The basic inductor current and voltage relation are $V_L = L\frac{dI_L}{dt}$. In a buck converter, the change in inductor current during the switch S1 on-time is equal to the change in current during the switch S1 off-time. The change in the inductor current (I_L) during the switch S1 on time is $\frac{\Delta I_L}{DT_{sw}}$.

$$L_{buck} = \frac{(V_{IN_max} - V_{OUT}) \times D_{Buck}}{\Delta I_L \times f_{sw}}$$

$\Delta I_{L,}$ can be fraction (0.2 to 0.6) of the $I_{part_capacity}$ to meet best transient performance

Where,

V_{IN_max} = Maximum input voltage

$I_{part_capacity}$ = maximum current rating of the part

5.1.2 Inductor selection

Inductor selected for this board are shown in Table 2.

Table 2 Selected inductors

Reference designator	Description	Manufacture Part number
L100	FIXED IND 1UH 4.47A 23 MOHM SMD	74406042010
L101,L102,L602,L603	FIXED IND 470NH 15A 2.75MOHM SMD	744316047
L200,L800,L801,L802	FIXED IND 100NH 37A 0.000125OHM	74431012010
L300	FIXED IND 70NH 37A 0.000125OHM	74431012007
L400,L500,L1000,L1100	FIXED IND 330NH 18.5A 1.75 MOHM	744316033
L600,L601	POWER INDUCTOR SMD 2.2 H; 4.0 A;	74479325207222

Self-resonating frequency of all the chosen inductors is high, which will help in reducing the switching noise at the output voltage. For example, 74431012010 has a self-resonating frequency of 80 MHz.

6 Test results

6.1 1.2V/2A rail

Figure 11 shows a ripple of 2V/2A rail and Figure 12 shows transient response of 1.2V/2A rail.

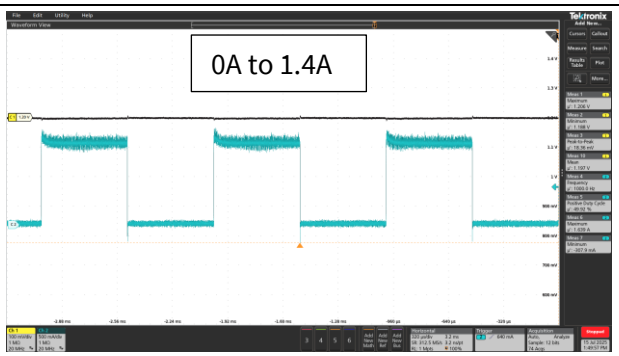


4.464mV pk-pk ripple - No load

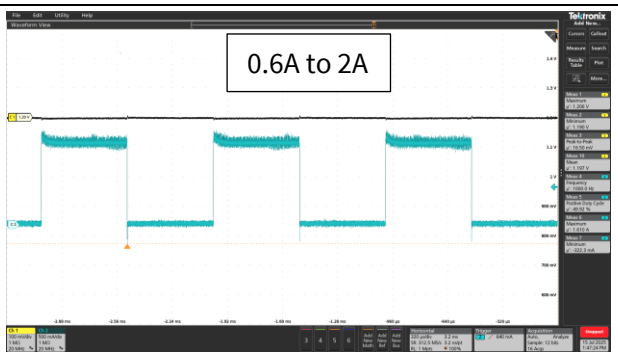


4.370mV pk-pk ripple - Full load

Figure 11 Ripple at no-load and full load of 1.2V/2A rail



CH1: VOUT; CH2: IOUT
Overshoot =6mV and Undershoot = 10mV



CH1: VOUT; CH2: IOUT
Overshoot =6mV and Undershoot = 12mV

Figure 12 Load transient on 1.2V/2A rail from 0 to 0.6A and 1.4 to 2A at a slew rate of 10A/µS

6.2 0.92V/2A rail

Figure 13 shows a ripple of 0.92V/2A rail and Figure 14 shows a transient response of 0.92V/2rail.

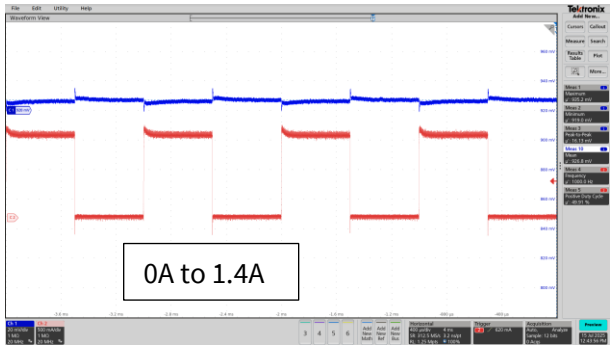


4.558mV pk-pk ripple - No load

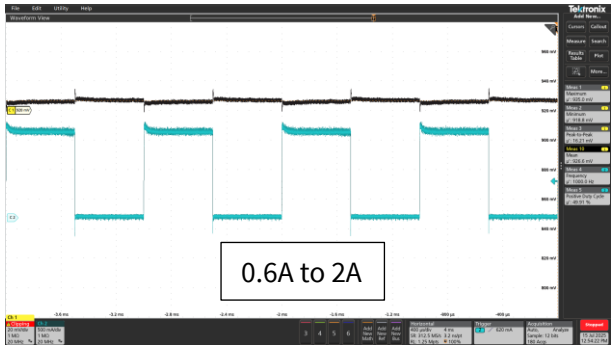


4.978mV pk-pk ripple - Full load

Figure 13 Ripple at no-load and full load of 0.92V/2A rail



CH1: VOUT; CH2: IOUT
Overshoot = 15mV and Undershoot = 1mV



CH1: VOUT; CH2: IOUT
Overshoot = 15mV and Undershoot = 2mV

Figure 14 Load transient on 0.92V/2A rail from 0 to 1.4A and 0.6 to 2A at a slew rate of 10A/µS

6.3 0.92V/3A rail

Figure 15 shows a ripple of 0.92V/3A rail and Figure 16 shows a transient response of 0.92V/3A rail.

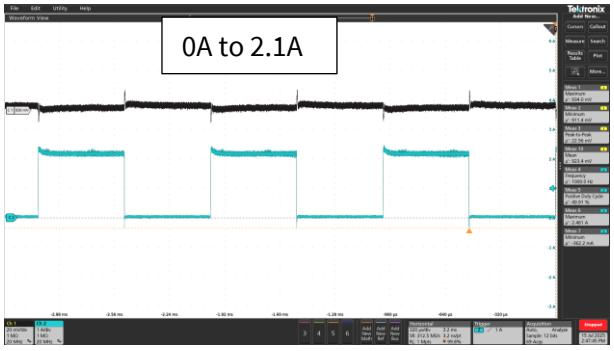


3.198mV pk-pk ripple - No load

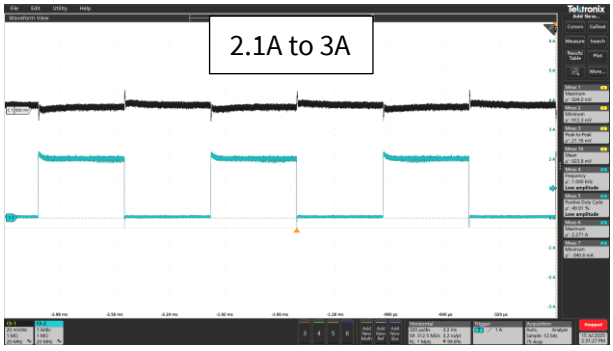


3.871mV pk-pk ripple - Full load

Figure 15 Ripple at no-load and full load of 0.92V/3A rail



CH1: VOUT; CH2: IOUT
Overshoot = 11mV and Undershoot = 11mV

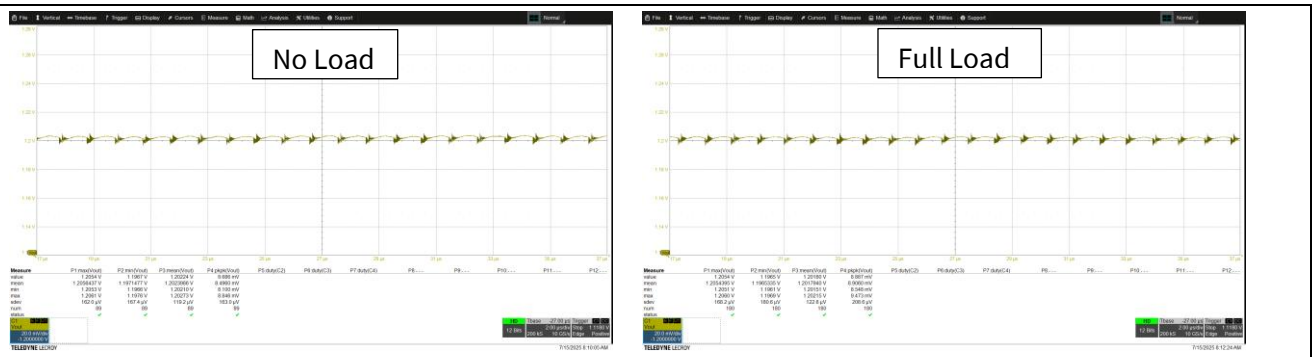


CH1: VOUT; CH2: IOUT
Overshoot = 11mV and Undershoot = 12mV

Figure 16 Load transient on 0.92V/3A rail from 0 to 2.1A and 0.9 to 3A at a slew rate of 10A/µS

6.4 1.2V/3A rail

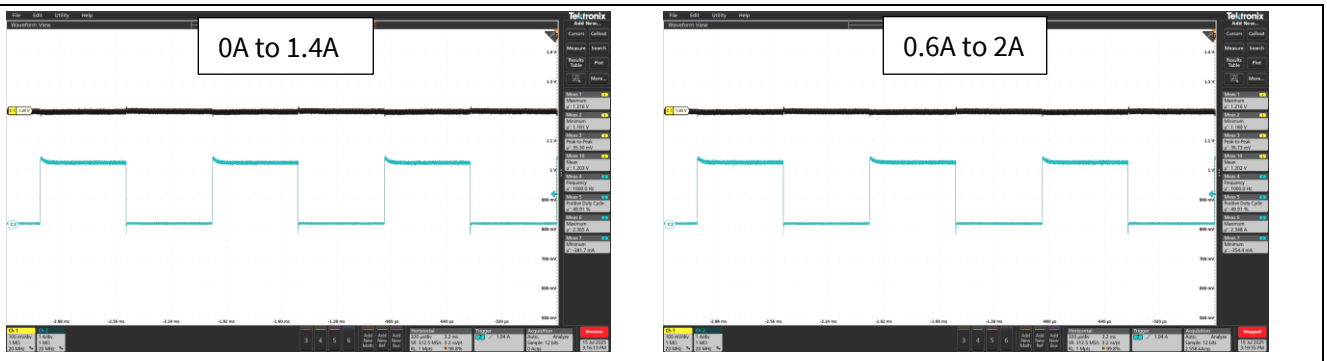
Figure 17 shows ripple measured on 1.2V/3A rail. Figure 18 shows transient response of 1.2V/3A rail.



8.686mV pk-pk ripple - No load

8.887mV pk-pk ripple - Full load

Figure 17 Ripple at no-load and full load of 1.2V/3A rail



CH1: VOUT; CH2: IOUT

Overshoot = 16mV and Undershoot = 21mV

CH1: VOUT; CH2: IOUT

Overshoot = 16mV and Undershoot = 20mV

Figure 18 Load transient on 1.2V/3A rail from 0 to 2.1A and 0.9 to 3A at a slew rate of 10A/µS

6.5 1.8V/1.3A rail

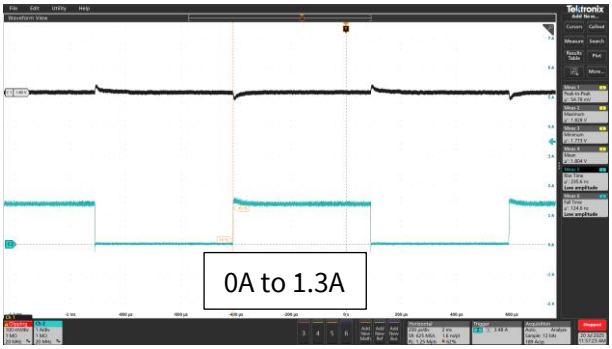
Figure 19 shows ripple measurement of 1.8V/1.3A rail and Figure 20 shows transient response on 1.8V/1.3A rail.



5.21mV pk-pk ripple - No load

4.57mV pk-pk ripple - Full load

Figure 19 Ripple at no-load and full load of 1.8V/1.3A rail



CH1: VOUT; CH2: IOUT

Overshoot = 28mV and Undershoot = 27mV

Figure 20 Load transient on 1.8V/1.3A rail from 0A to 1.3A at a slew rate of 10A/µS

6.6 1.5V/3A rail

Figure 21 shows a ripple of 1.5V/3A rail and Figure 22 shows a transient response of 1.5V/3A rail.

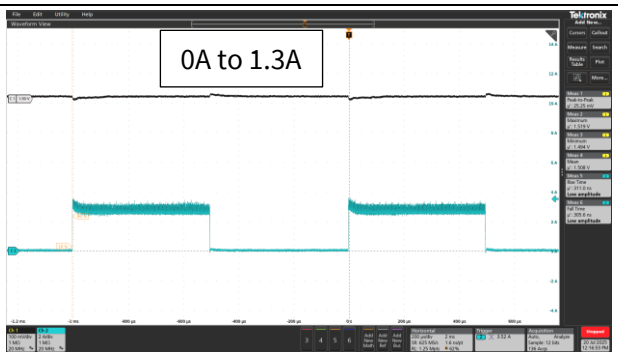


5.132mV pk-pk ripple – No load



5.490mV pk-pk ripple – Full load

Figure 21 Ripple at no-load and full load of 1.5V/3A rail



CH1: VOUT; CH2: IOUT

Overshoot = 19mV and Undershoot = 6mV

Figure 22 Load transient on 1.5V/3A rail from 0A to 3A at a slew rate of 10A/µS

6.7 1.5V/6A rail

Figure 23 shows ripple measured on 1.5V/6A rail at no-load and full load. Figure 24 shows transient response of 1.5V/6A rail.

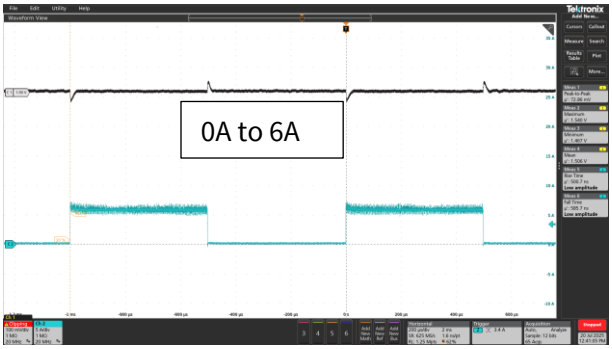


6.757mV pk-pk ripple - No load



8.550mV pk-pk ripple - Full load

Figure 23 Ripple measured at no-load and full load on 1.5V/6A rail



CH1: VOUT; CH2: IOUT

Overshoot = 40mV and Undershoot = 33mV

Figure 24 Transient response of 1.5V/6A rail for a slew rate of 10A/µS

6.8 3.3V/0.6A rail

Figure 25 shows ripple of 1.5V/3A rail and Figure 26 shows a transient response of 1.5V/3A rail.

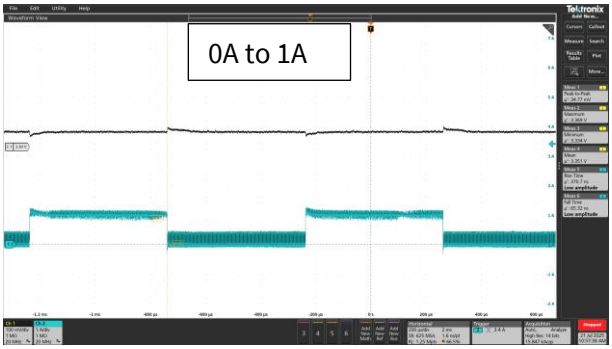


5.122mV pk-pk ripple – No load



5.298mV pk-pk ripple – Full load

Figure 25 Ripple at no-load and full load of 3.3V/0.6A rail



CH1: VOUT; CH2: IOUT

Overshoot = 69mV and Undershoot = 34mV

Figure 26 Load transient on 3.3V/0.6A rail at a slew rate of 10A/µS

6.9 0.8V/30A rail

Figure 27 shows ripple of 0.8V/30A rail and Figure 28 shows a transient response of 0.8V/30A rail.



11.81mV pk-pk ripple – No load



12.12mV pk-pk ripple – Full load

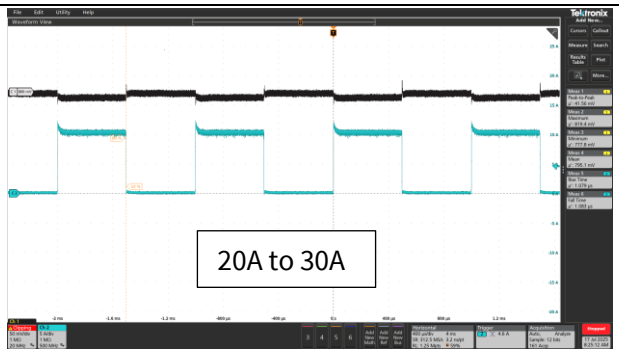
Figure 27 Ripple at no-load and full load of 0.8V/30A rail



Overshoot = 23mV and Undershoot = 19.4mV



Overshoot = 22.5mV and Undershoot = 20.5mV



Overshoot = 19.4mV and Undershoot = 4.9mV

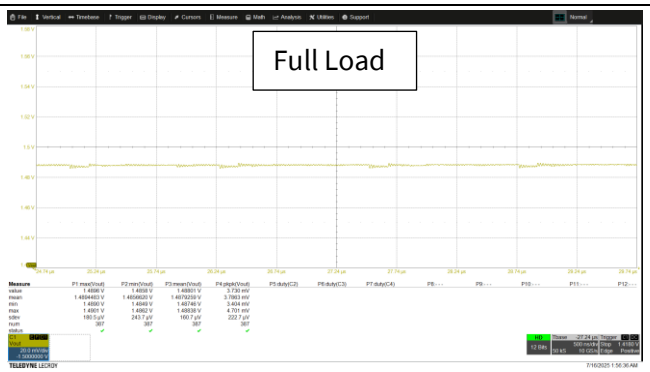
CH1: VOUT; CH2: IOUT

Figure 28 Load transient on 0.8V/30A rail from 0A to 10A, 10A to 20A and 20A to 30A at a slew rate of 10A/µS

6.10 1.5V/0.1A rail

Figure 29 shows a ripple of 1.5V/0.1A rail.





4.017mV pk-pk ripple – No load

3.730mV pk-pk ripple – Full load

Figure 29 Ripple at no-load and full load of 1.5V/0.1A rail

6.11 0.8V/60A rail

Figure 30 shows a ripple of 0.8V/60A rail and Figure 31 shows a transient response of 0.8V/60A rail.

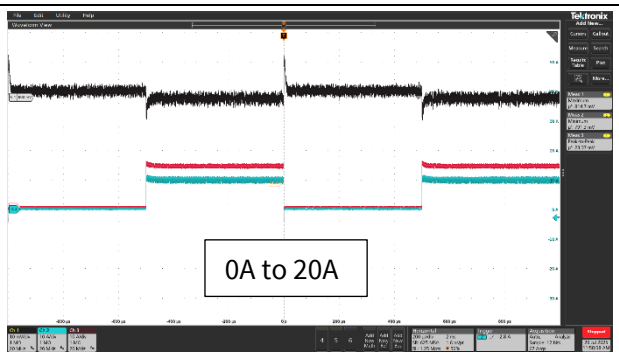




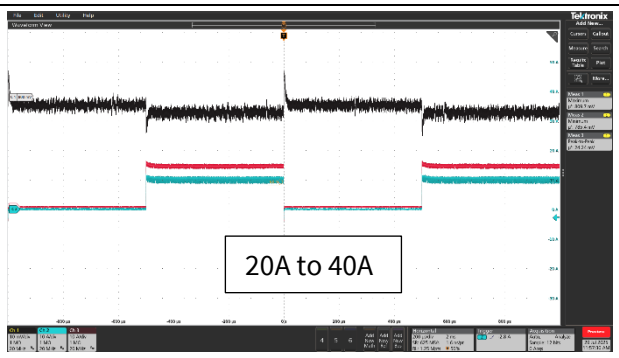
6.377mV pk-pk ripple – No load

7.029mV pk-pk ripple – Full load

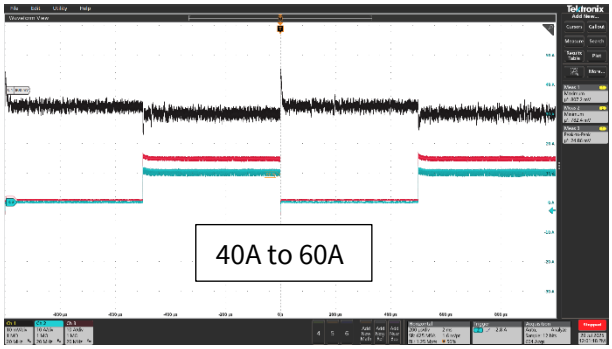
Figure 30 Ripple at no-load and full load of 0.8V/60A rail



Overshoot = 14mV and Undershoot = 9mV



Overshoot = 9mV and Undershoot = 15mV



Overshoot = 7mV and Undershoot = 17mV

CH1: VOUT; CH2: IOUT1; CH3: IOUT2

Figure 31 Load transient on 0.8V/60A rail from 0A to 20A, 20A to 40A and 40A to 60A at a slew rate of 10A/µS

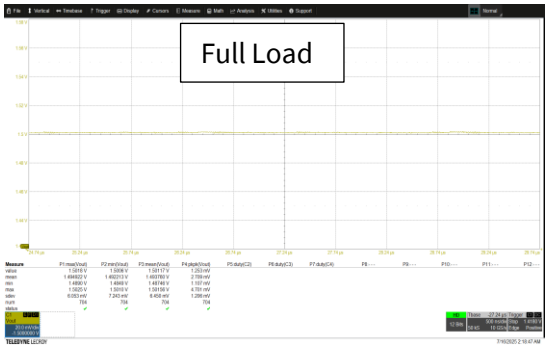
Load transient of 20A is realized using two mini-slammer, each mini-slammer sharing a load of 10A each as shown in Figure 16.

6.12 1.5V/0.1A rail

Figure 32 shows a ripple of 1.5V/0.1 rail.



1.213mV pk-pk ripple – No load

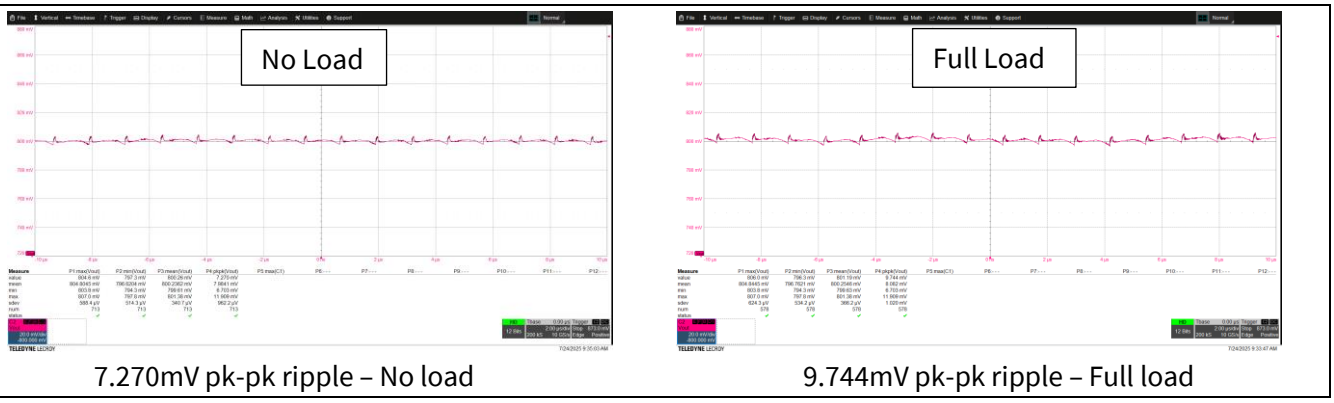


1.253mV pk-pk ripple – Full load

Figure 32 Ripple at no-load and full load of 1.5V/0.1A rail

6.13 0.8V/37A rail

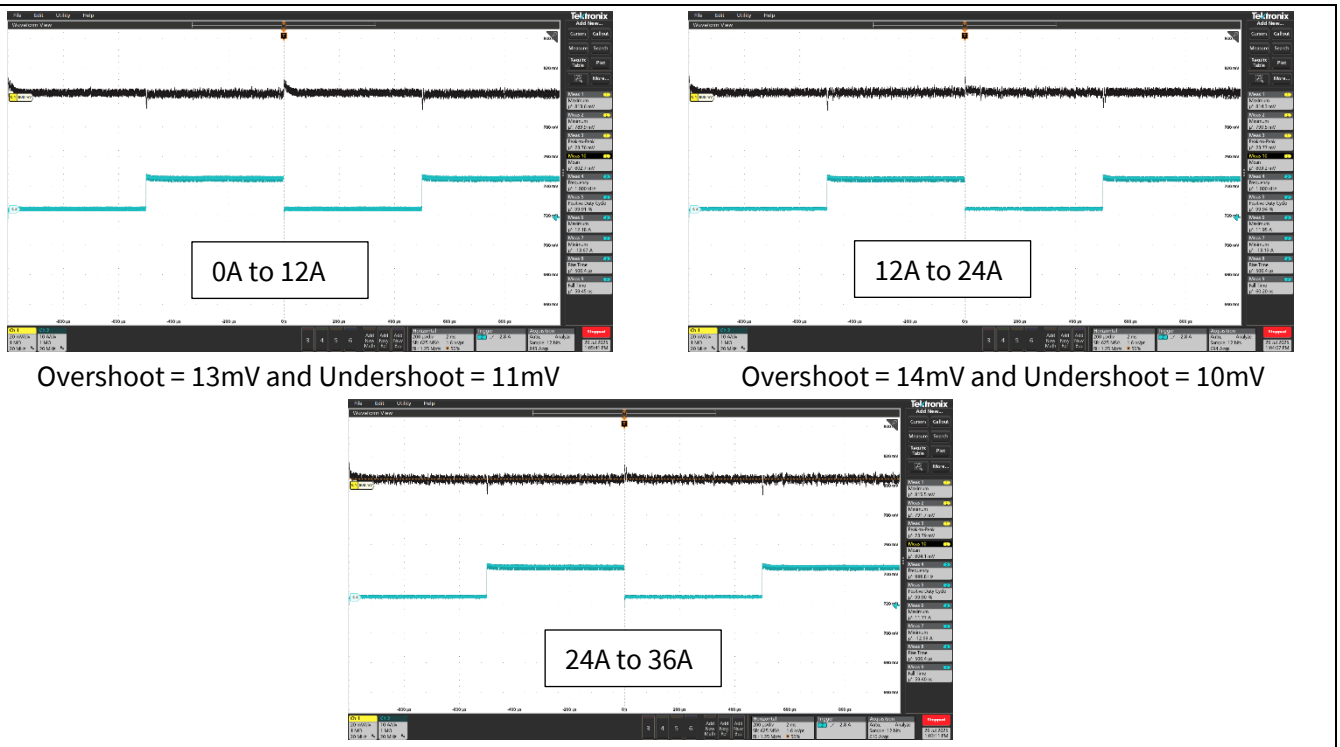
Figure 33 shows a ripple of 0.8V/37A rail and Figure 34 shows a transient response of 1.5V/3A rail.



7.270mV pk-pk ripple – No load

9.744mV pk-pk ripple – Full load

Figure 33 Ripple at no-load and full load of 0.8V/37A rail



Overshoot = 13mV and Undershoot = 11mV

Overshoot = 14mV and Undershoot = 10mV

Overshoot = 15mV and Undershoot = 9mV

CH1: VOUT; CH2: IOUT

Figure 34 Load transient on 0.8V/37A rail from 0A to 12A, 12 to 24A and 24 to 37A at a slew rate of 10A/µS

6.14 3.3V/3A rail

Figure 35 shows a ripple of 3.3V/3A rail and Figure 36 shows a transient response of 3.3V/3A rail.

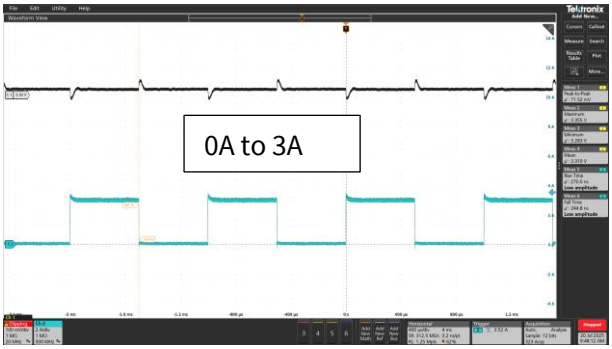


7.267mV pk-pk ripple – No load



7.609mV pk-pk ripple – Full load

Figure 35 Ripple at no-load and full load of 3.3V/3A rail



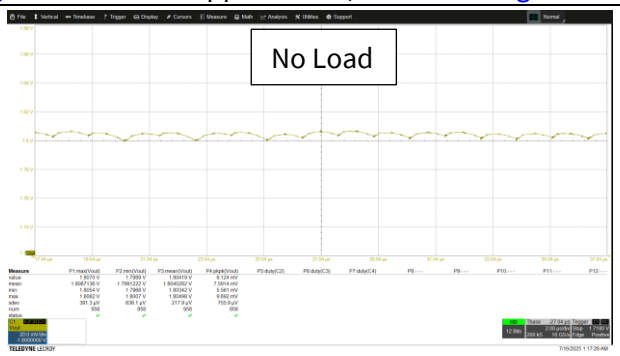
CH1: VOUT; CH2: IOUT

Overshoot = 55mV and Undershoot = 37mV

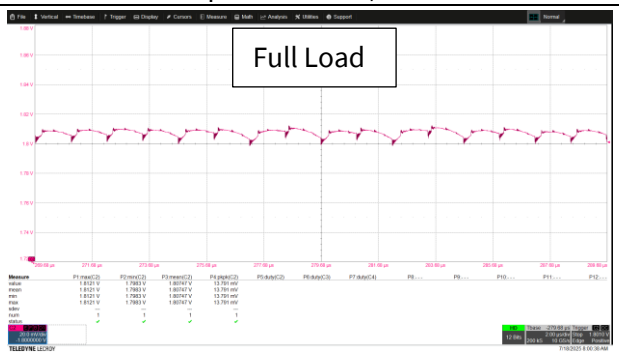
Figure 36 Load transient on 3.3V/3A rail from 0A to 3A at a slew rate of 10A/µS

6.15 1.8V/3A rail

Figure 37 shows a ripple of 1.8V/3A rail and Figure 38 shows a transient response of 1.8V/3A rail.



8.124mV pk-pk ripple – No load



13.791mV pk-pk ripple – Full load

Figure 37 Ripple at no-load and full load of 1.8V/3A rail

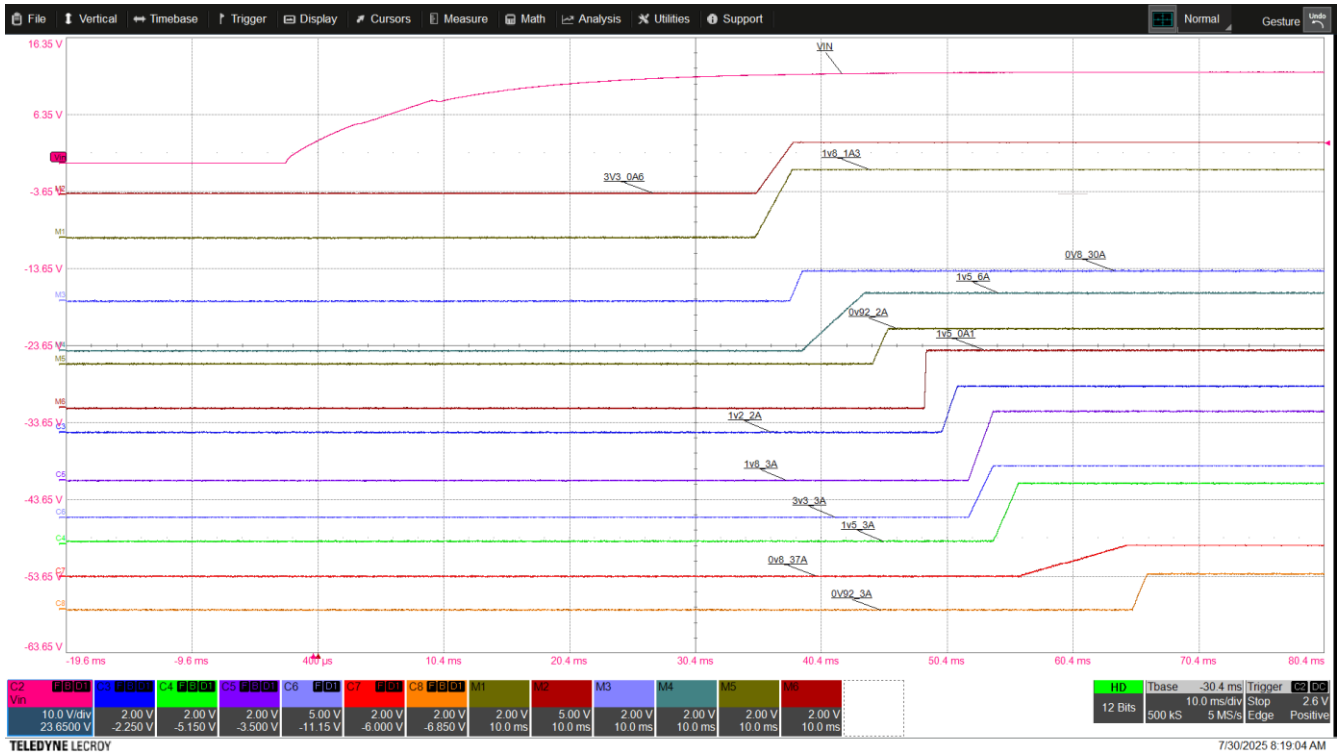


CH1: VOUT; CH2: IOUT
Overshoot = 22mV and Undershoot = 22mV

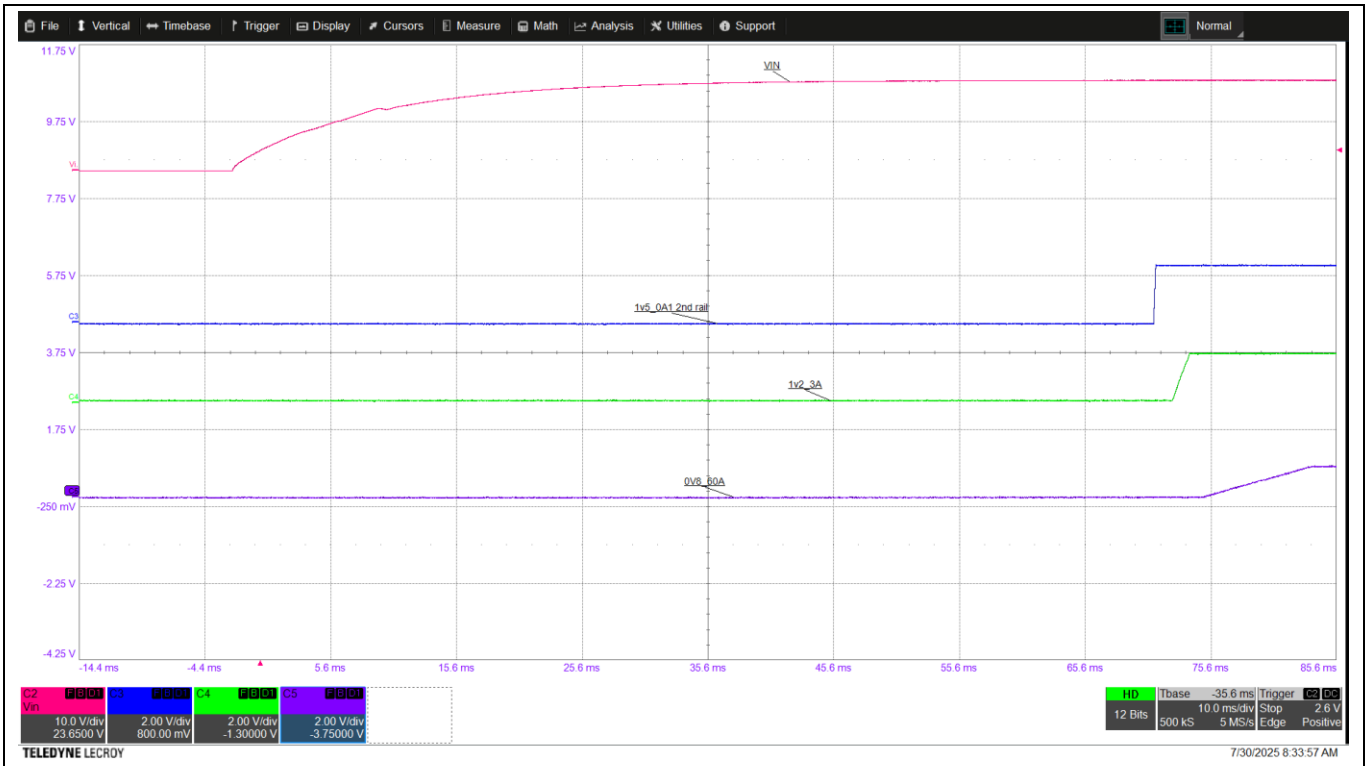
Figure 38 Load transient on 1.8V/3A rail from 0A to 3A at a slew rate of 10A/µS

6.16 Sequence of the power rails

Figure 39 shows the sequence in which the power rails shall be tuned ON.



CH2: VIN; M1:1.8V/1.3A rail; M2:3.3V/0.6A rail; M3:0.8V/30A rail.
M4:1.5V/6A rail; M5:0.92V/2A rail; M6:1.5V/0.1 rail; CH3: 1.2V/2A rail; CH4: 1.5V/3A rail; CH5:1.8V/3A rail.
CH6:3.3V/3A rail; CH7:0.8V/37A rail; CH8:0.92V/3A rail.



CH2: VIN; CH3: 1.5V/0.1A 2nd rail; CH4: 1.2V/3A rail; CH5:0.8V/60A rail.

Figure 39 Sequence of which the power rails are turned ON

References

Datasheets

[1] TDA38806 – 6 A synchronous Buck regulator.

[2] TDA38740 - OptiMOS iPOL - 40/25A Single-voltage Synchronous Buck Regulator with PMBusUSB

[3] IRPS5401- Flexible Power Management including 5 integrated outputs 4A, 4A, 2A and 2A Switching Regulators

[4] TDA21590- 90A synchronous buck regulator IC

[5] XDPE19283D - Digital Multi-phase Controller; 8-phase Dual Loop Voltage Regulator

[6] TDA21590 - High Efficiency OptiMOS™ 90A Integrated internal Current Sense Power Stage

Guides

[7] TDA38806 P1V8 user guide

[8] User manual for TDA38740 evaluation board

[9] IRPS5401 programming guide

Revision history

Document revision	Date	Description of changes
01	2025-07-30	Initial release
02	2026-05-06	Changes made in Header, corrected Versal™ AI Edge Series and Prime Series Gen 2 devices in SOC Mode rail consolidation, Hyperlinks.

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