System Simulation & Design Creation Tool (Transformer, BOM and IC Parameters)

Single-Stage PFC Flyback Dimmable Constant-Current Controller

XDPL8105
XDP™ digital power

About this document

Scope and purpose

This document is a guide to using the Infineon XDPL8105 system simulation and design creation tool. It enables users to generate transformer, bill of materials (BOM) and IC parameter designs based on the system simulation/calculation output.

The Infineon XDPL8105 is a digital controller for high-performance single-stage flyback converter, targeting LED lighting applications.

Intended audience

This document is intended for anyone wishing to evaluate the performance of the Infineon XDPL8105 for their own application tests or to use it as a base/reference for a new Infineon XDPL8105-based development.

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1 Key features

1.1 System simulation/calculation

Single-stage PFC Flyback is the most cost-effective topology for lighting applications which have low output power and require isolation. However, system optimization of such a topology is not so straightforward as it mostly requires trade-off with other performance factors. For instance, increasing output capacitance will reduce output current ripple but the trade-off could be a longer startup time at low dimming. Therefore, the system simulation and calculation with this tool is intended to help XDPL8105 customers when creating a board design with overall-balanced performance profiles which fit best to their requirements.

Below is a list of system simulation and calculation outputs generated by the tool:

- Normalized primary average current curve simulation for iTHD optimization (see example in **Figure 1**)
- Controller operating mode validation during non-dimmed operation
- Minimum and maximum on-times during non-dimmed operation
- Minimum and maximum switching frequencies during non-dimmed operation
- Maximum primary peak current, primary rms current, secondary rms current calculations
- Output current estimation at minimum dimming
- Maximum output current ripple estimation
- Maximum startup time estimation
- Maximum MOSFET drain voltage and output diode reverse voltage estimation
- Transformer conduction loss, core loss estimation at minimum and maximum input voltages
- Minimum and maximum value selection for passive components (capacitors & resistors)
- Maximum power loss estimation of selected values of XDPL8105 CS pin resistor, ZCD pin resistors and bleeder resistor.

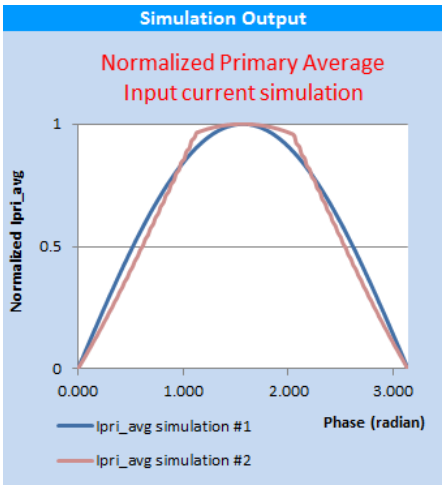


Figure 1 Example of normalized primary average current curve simulation (for iTHD optimization)

Note: iTHD refers to input current harmonics distortion.

1.2 System design creation

A full system design with XDPL8105 can be achieved easily with this tool as it is highly interactive, providing design tips and detecting any errors or warnings based on user inputs in each step. Upon completion of the 3 main design steps in the tool without any error, the transformer drawing, bill of materials (BOM) and IC parameters are automatically generated.

1.2.1 Auto-generated transformer drawing

Below is a list of transformer drawing outputs generated by the tool:

- Wire size and type of each winding
- Parallel wires used in each layer of winding
- Number of turns and layers for each winding
- Winding layers sequencing based on “sandwich-winding” construction

An example of an auto-generated transformer drawing is shown in **Figure 2**.

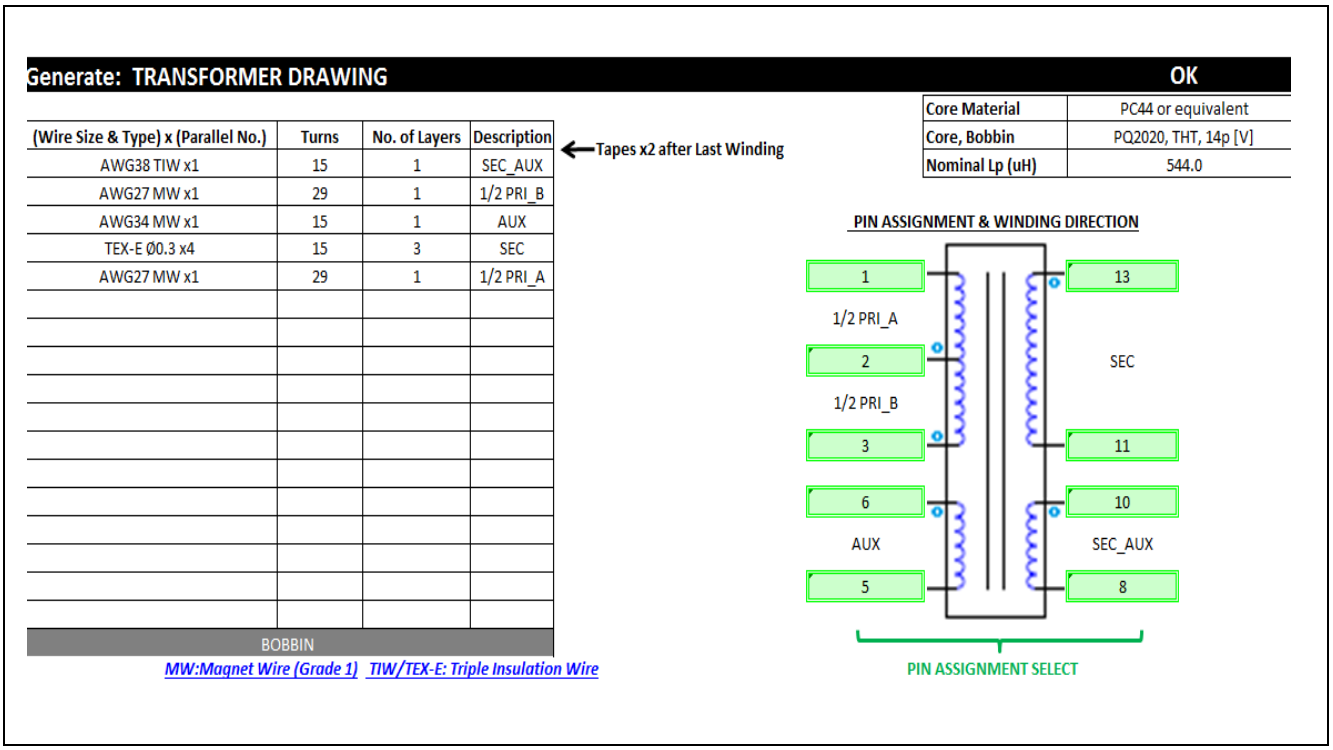


Figure 2 Example of auto-generated transformer drawing

1.2.2 Auto-generated BOM and IC parameters

The XDPL8105 is a high-performance digital controller which allows custom parameterization by designers or end users. For instance, the XDPL8105 allows changes to non-dimmed output current settings on the same board with no change in hardware. There are a total of 73 IC parameters which can be configured using a GUI called .dpVision.

Based on the design inputs of each step, the tool will recommend the minimum and maximum values of parameters and components dimensioning in order to guide users in the selection of appropriate values. After completing the final step with no error detected, BOM and IC parameters will be automatically generated – as shown in **Figure 3**.

Auto-generated BOM

Auto-Generated BOM

Note: Based on sheet "SCH" schematic of 40W Ref Design. EMI Line Filter & Bridge not included in this BOM

Schematic Section	Symbol	Value	Rating	Supplier	Part Number/Package
FB_PRI	T1	Lp: 0.544mH; Np: 58; Ns: 15; Naux: 15; Nsec_aux: 15		WURTH	Core, Bobbin: PQ2020, THT, 14p [V]
	IC3	XDPL8105	-	INFINEON	XDPL8105 (DSO-8)
	Q1	IPD80R1K0CE	800V	INFINEON	DPAK
	D3	≥1A	≥800V	DIODES	RS3MB-13-F(SMB)
	D20, D21	1A	600V	FAIRCHILD	ES1J (SMA)
	C3	6800pF	> 378V	ANY	Film cap
	C4	0.22uF	> 498V	ANY	Film cap
	C5	100pF	50V, COG	ANY	SMD Package: 0603
	R2	20kohm	1%	ANY	SMD Package: 0603
	R4+R5+R6	66kohm	1%	ANY	SMD Package:1206 (3 pcs, in series)
	R7+R8	174.8kohm	≤5%	ANY	Power rating: >0.67W
	R10	56.2kohm	1%	ANY	SMD Package: 1206
	R11	2kohm	1%	ANY	SMD Package: 0603
	R14	0.22ohm	1%	ANY	Power rating: >0.12W
	R16	10ohm	1%	ANY	SMD Package: 0805
AUX VCC SUPPLY	Q2	NPN Transistor	Vceo >60V	ANY	Power rating: >0.72W
	D4	≥0.25A	>242V	ANY	BAV103 (SOD-80C)
	D12	0.25A	≥30V	ANY	BAV102 (SOD-80C)
	ZD1	Zener 15V	≤5%	ANY	SOD-323 or similar
	C6	4.7uF	>60V	ANY	Electrolytic Cap
	C8	15uF	≥25V	ANY	E-Cap or SMD1206
	C38	0.1uF	≥25V	ANY	SMD Package: 0603
	R17	47kohm	1%	ANY	SMD Package: 1206
	R18	4.7ohm	1%	ANY	SMD Package: 1206
DIMMING *Secondary 0-10V dimming with CDM10V*	IC30	Schmitt trig. IC	invert out	TI	SN74LVCG14DBVR
	IC100	CDM10V adapter	-	INFINEON	CDM10V adapter board
	PC1	Optocoupler	>4kV, UL	VISHAY	VO617A-2
	Q100	NPN Transistor	Vceo >57	ANY	SOT-89 or larger
	ZD30	Vz=5.1V at 1mA	≤2.5%	ANY	SOD323 or similar
	D100	0.25A	>242V	ANY	BAV103 (SOD-80C)
	D105	Schottky	low leakage	ANY	MMBD301LT1G(SOT23)
	ZD100	Zener 15V	≤5%	ANY	SOD-323 or similar
	C33	0.68uF	16V	ANY	SMD Package: 0603
	C34	4.7uF	25V	ANY	SMD Package: ≥0805
	C35, C36	0.1uF	≥25V	ANY	SMD Package: 0603
	C102	2.2uF	>60V	ANY	Electrolytic Cap
	C103	10uF	25V	ANY	SMD Package: 1206
	R19	620kohm	1%	ANY	SMD Package: 0603
	R31	2.2kohm	1%	ANY	SMD Package: 0603
	R32	36kohm	1%	ANY	SMD Package: 0603
	R33	5.1kohm	1%	ANY	SMD Package: 0603
	R34	47kohm	1%	ANY	SMD Package: 0603
	R36	18kohm	1%	ANY	SMD Package: 0603
	R37	2.2kohm	1%	ANY	SMD Package: 0805
	R100	4.7ohm	1%	ANY	SMD Package: 1206
	R101	47kohm	1%	ANY	SMD Package: 1206
FB_SEC	D6	> 8.1A	> 237V	ONSEMI	MBRB40250TG
	C7	0.1uF	≥70V	ANY	SMD Package: ≥0805
	C12//C13	940uF	63V	ANY	Electrolytic Cap
	C99	OPEN	-	-	-
	R99	OPEN	-	-	-
OUTPUT BLEEDER *Active (Auto-Discharge Circuit)*	Q3, Q4	2N7002	60V	INFINEON	2N7002 (SOT-23)
	D7	Dual Diode	> 237V	INFNEON	BAT240A (SOT-23)
	D8, D9	OPEN	-	-	-
	ZD4, ZD5	Zener 12V	≤5%	ANY	SOD-323 or similar
	C10	1000pF	> 296V	ANY	Discrete or SMD 1206
	C11	0.1uF	≥25V	ANY	SMD Package: 0603
	R26//R29 //R30	1.3kohm	1%	ANY	Power rating > 1W
	R27, R28	1Mohm	1%	ANY	SMD Package: 0805
	R9	OPEN	-	-	-
Y-CAP	C9	2200pF	≥277Vac	ANY	Safety Ceramic Cap
DEBUG/PROGRAMMING	C31	470p	≥25V, COG	ANY	SMD Package: 0603
	J4	3 pins	-	ANY	3 pins (Vcc, Uart, Gnd)
SAFETY & LINE SURGE *(Fuse is mandatory for your safety!)*	F1	UL safety fuse	>0.98A	ANY	-
	MOV1	surge absorber	UL Safety	ANY	Radial, Disc Type
	D1, D2	surge absorber	>216.3V	ANY	Case Style: 1.5KE
	D10	ESD Diode 12V	low leakage	ANY	-
JUMPERS	R1,R50,R51	0ohm	-	ANY	SMD Package: 0603

Auto-generated IC Parameters

Auto-Generated IC Parameters
for XDPL8105 csv version: Rev1

Hardware configuration		
I_out_set	880.0	mA
N_p	58	turns
N_s	15	turns
N_a	15	turns
L_p	0.5440	mH
R_CS	0.220	ohm
V_OCP1	0.49 ~ 0.51	V
R_ZCD_1	56.2	kohm
R_ZCD_2	2.00	kohm
VCC_SUPPLY	Wide	
C_VCC	15	uF
V_out_cap rating	63	V
R_HV	66	kohm
I_GD_pk	49	mA
Protections		
t_auto_restart	1.0	s
t_auto_restart_fast	0.4	s
Reaction_OVP_Vout	Auto-Restart	
Speed_OVP_Vout	Slow	
V_outOV	48.4	V
EN_UVP_Vout	Enabled	
t_start_max	10.0	ms
EN_Iout_max_avg	Enabled	
EN_Iout_max_peak	Enabled	
I_out_max_peak	1980	mA
Speed_OCP_Iout	Slow	
EN_UVP_In	Enabled	
EN_OVP_In	Enabled	
V_inOV	329.0	V
V_in_start_max	329.0	V
V_in_start_min	72.0	V
V_inUV	62.0	V
Reaction_VCCP	Latch-Mode	
Debug_Mode	Disabled	
Temperature guard		
T_critical	119	°C
EN_ITP	Enabled	
T_hot	110	°C
I_out_red	220	mA
t_step	10	s
Startup & shutdown		
t_ss	0.50	ms
V_out_dim_min	11.9	V
V_out_start	9.5	V
V_start_OCP1	V_OCP1	V
Control_loop_init	DCM	
f_DCM_init	12	kHz
N_ABM_init	100	
Control loop		
PI_KP_QRM	550	
PI_KI_QRM	8	
PI_KI_DCM	17000	
PI_KI_DCM	200	
PI_KP_ABM	64	
PI_KI_ABM	32	
Dimming		
EN_DIM	Enabled	
V_DIM_min	0.2	V
I_out_dim_min	88.0	mA
C_DIM	Quadratic	
EN_DIM_TO_OFF	Disabled	
V_DIM_off	0.18	V
V_DIM_on	0.19	V
EN_SQW	Disabled	
Multimode		
f_sw_max	180.80	kHz
t_on_max	11.3	us
t_on_min	1.1	us
t_min_demag	3.0	us
f_sw_min_DCM	12.0	kHz
EN_ABM	Disabled	
Power Factor Correction		
C_EMI	0.1000	uF
Fine tuning		
t_ZCDPD	410	ns
t_PDC	200	ns
T_coupling	1.020	
R_in	11.90	ohm
N_DCM_mod_gain	8	
a_DIM	0.000	mV/K

PLEASE FINE TUNE BASED ON APP. NOTE

Figure 3 Example of auto-generated BOM and IC parameters

2 Overview

This section provides general information about the tool.

2.1 Software and version

- Software name: Microsoft Excel
- Software version: 2010 or later
- Excel file format: *.xlsm (macro-enabled Excel sheet)

2.2 Worksheets

There are 3 worksheets in this Excel tool by default.

- The “SCH” worksheet shows a schematic of the auto-generated BOM
- The “Wire” worksheet shows wire table used in the calculation of the auto-generated transformer drawing
- The “Simulation & Design” worksheet is the tool itself with which users can enter design inputs and where the simulation output/system design will be generated

Note: “SCH” and “Wire” worksheets are for reference only. The workbook structure is protected by password.

2.3 Cell protection and legend

The “Simulation & Design” worksheet is protected by password. Users can only enter or modify values in the design input cell, which is light-green-coloured, as shown in **Figure 4**.

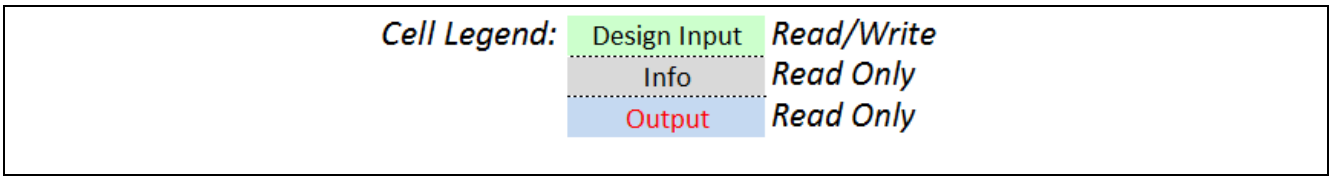


Figure 4 Cell legend of “Simulation & Design” worksheet

2.4 Cell comments

Comments are available to provide explanations or give guidance on every design input and calculation output. For an example, refer to **Figure 5**.

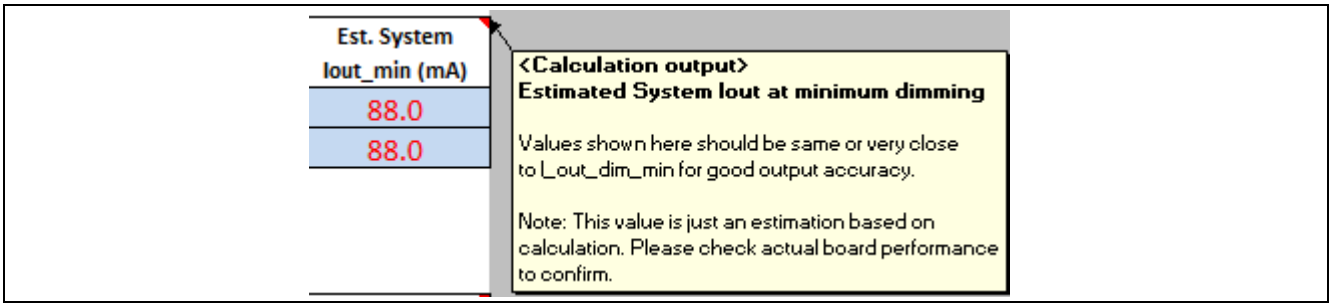


Figure 5 Example of a cell comment explanation

2.5 Expand/collapse button and status bar

Each design step and generated output can be expanded or collapsed according to the user's preference. The expand/collapse button is available on the left side (See **Figure 6**).

Also, the status of each step will be shown in the status bar on the right side (See **Figure 6**):

- "OK" means that no error or warning has been found.
- "WARNING" means that a warning, but no error has been found. The user should pay attention to the warnings.
- "ERROR" means an inappropriate design input has been found. The user should adjust the design input.

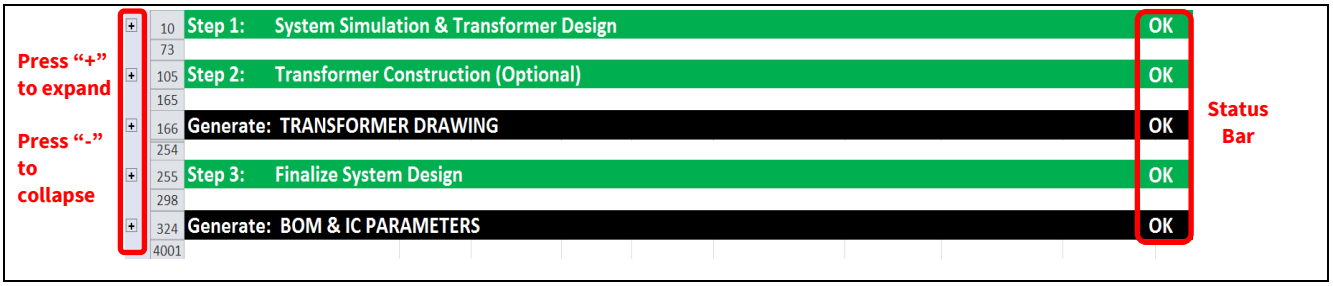


Figure 6 Expand/collapse button and status bar

2.6 Other important notes

- The Excel macro must be enabled to use the tool when opened and must be saved in *.xlsm format.
- The Excel zoom level setting should be set to a minimum of 90% for proper content display.
- The user can click the "Optimize View" shortcut button for the best view settings (zoom level: 110%, full screen, formula bar disabled). To exit full-screen mode, press the "ESC" key.
- Press the "Enter" key on the design input cell whenever its value is modified. This will ensure that the output results are updated with the calculation based on the new modified value. Depending on the CPU resources, the output results update could take up to 3 seconds.

3 User guide

This section provides a detailed guide on each of the 3 main design steps given below:

- Step 1: System simulation and transformer design
- Step 2: Transformer construction
- Step 3: System design finalization

3.1 STEP 1 – System simulation and transformer design

In this step, the system design outlined below is based on the simulation/calculation output:

- Transformer design (primary inductance, turns ratios of all windings)
- Maximum switching frequency parameter setting
- Output and input OVP-related parameters setting
- Minimum dimming level-related parameters setting
- Input and output capacitor values
- HV pin series resistor value
- Vcc supply source selection
- Voltage regulator circuit design (if necessary)
- Vcc capacitor value
- Secondary 0-10V dimming circuit design (if necessary)
- MOSFET and output diode voltage rating

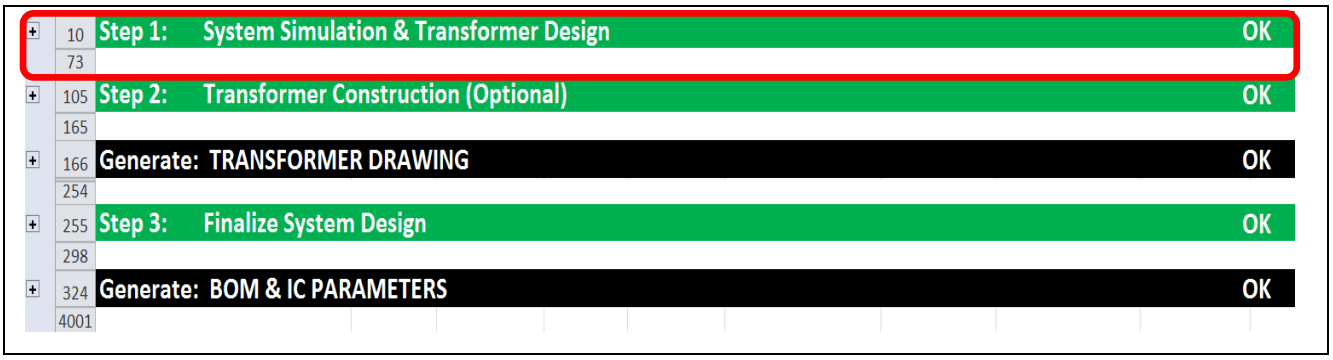


Figure 7 STEP 1 – System simulation and transformer design

3.1.1 Project specification input

The first half of the step 1 main design input (as circled in red in **Figure 8**) is related to project specification, so is straightforward to fill in.

- **Vin**: AC input voltage range
- **Vo**: Output load voltage range (LED forward voltage range) at non-dimming
- ***I_out_set* setting**: Non-dimmed Iout setting by IC parameterization
- ***V_outOV* setting**: Output OVP level setting by IC parameterization (based on typ. value)
- **Efficiency**: System efficiency estimation
- **Iout Dimming?**: Output dimming (No / Primary side Dimming / Secondary 0-10V dimming)
- ***EN_OVP_In* setting**: Input OVP enabled/disabled setting by IC parameterization

- ***V_inOV* setting**: Input OVP level setting by IC parameterization (based on typ. value)

If necessary, please refer to the cell comments or to the “Tips and Interactive Info” section for guidance and details.

Step 1: System Simulation & Transformer Design

Main Design Input

	min	typ	max	Tips & Interactive Info
Vin (Vrms)	90	230	277	AC input voltage (normal operation)
Vo (V)	18.0	31.5	45.0	Non-Dimming LED output voltage range
V_outOV setting(V)	46.0	48.4	55.6	Autoset to Vo_max/0.93; tolerance: -5%, +15%
I_out_set setting (A)		0.88		Output current at non-dimming condition
Efficiency (%)		90%		Est. Efficiency (Vin_min, Pout_max)
Iout Dimming?	Yes (Secondary side 0-10V dimming)			Iout Dimming option (see comment for details)
EN_OVP_In setting	Enabled			Input OVP (Enabled/Disabled?)
V_inOV setting (V)	306.0	329	352.0	Range: 297.9 ~ 396.2; Tolerance:+/-7%
Np/Ns Selection		3.870		Higher for better iTHD. Tips: Use 3.82 ~ 4.58
L_p (uH)		544.0		Higher for lower dim current. Tips: Use 512 ~ 768
Cin, Input capacitor (uF)		0.220		Tips: <40W: 0.15uF; 40 ~ 60W: 0.22uF
MOSFET Co(tr) (pF)		69.0		Tips: See comment for list of MOSFET Co(tr) values
f_sw_max setting (kHz)		180.80		Tips: ≤180.8kHz(if Tj≤125°C), ≤136.4kHz(if Tj >125°C)
N_DCM_MOD_GAIN setting		8		Tips: See comment. Modulation(Max:4, Min:32, Off:0)
t_on_min setting (us)		1.1		Tips: see comment. Range: 1~2.5
Normalized Ipri_avg simulation #1	Perfect Sine			Select checkpoint for iTHD optimization, if needed.
Normalized Ipri_avg simulation #2	Vin_typ, Vo_max			(Perfect Sine is just for reference purpose.)

ENTER DESIGN INPUT

Figure 8 Project specification (Step 1 Main design input)

3.1.2 Transformer electrical spec. input

Np/Ns selection refers to the turn ratio of primary main winding turns to secondary main winding turns. Based on quasi-resonant (QR) constant on-time operation, higher Np/Ns values give lower iTHD. However, please take note that MOSFET drain voltage will increase with higher Np/Ns values and it should not exceed the MOSFET drain voltage rating.

L_p is the primary main winding inductance of the transformer. Too high a value could force the system to enter CCM protection mode, while too low a value could cause non QR valley switching or discontinuous conduction mode (DCM) at non-dimming level and high output current at min-dimming level.

Tips are available in the “Tips and Interactive Info” section to help users to find the right Np/Ns and *L_p* values by dynamically calculating a recommended value range based on project specification input (as shown in the red-highlighted text in **Figure 9**). It is recommended (but not mandatory) to follow the tips given there.

Step 1: System Simulation & Transformer Design

Main Design Input

	min	typ	max	Tips & Interactive Info
Vin (Vrms)	90	230	277	AC input voltage (normal operation)
Vo (V)	18.0	31.5	45.0	Non-Dimming LED output voltage range
V_outOV setting(V)	46.0	48.4	55.6	Autoset to Vo_max/0.93; tolerance: -5%, +15%
I_out_set setting (A)		0.88		Output current at non-dimming condition
Efficiency (%)		90%		Est. Efficiency (Vin_min, Pout_max)
Iout Dimming?	Yes (Secondary side 0-10V dimming)			Iout Dimming option (see comment for details)
EN_OVP_In setting	Enabled			Input OVP (Enabled/Disabled?)
V_inOV setting (V)	306.0	329	352.0	Range: 297.9 ~ 396.2; Tolerance:+/-7%
Np/Ns Selection		3.870		Higher for better iTHD. Tips: Use 3.82 ~ 4.58
L_p (uH)		544.0		Higher for lower dim current. Tips: Use 512 ~ 768
Cin, Input capacitor (uF)		0.220		Tips: <40W: 0.15uF; 40 ~ 60W: 0.22uF
MOSFET Co(tr) (pF)		69.0		Tips: See comment for list of MOSFET Co(tr) values
f_sw_max setting (kHz)		180.80		Tips: ≤180.8kHz(if Tj≤125°C), ≤136.4kHz(if Tj >125°C)
N_DCM_MOD_GAIN setting		8		Tips: See comment. Modulation(Max:4, Min:32, Off:0)
t_on_min setting (us)		1.1		Tips: see comment. Range: 1~2.5
Normalized Ipri_avg simulation #1	Perfect Sine			Select checkpoint for iTHD optimization, if needed. (Perfect Sine is just for reference purpose.)
Normalized Ipri_avg simulation #2	Vin_typ, Vo_max			

ENTER DESIGN INPUT

Figure 9 Transformer electrical spec (Step 1 Main design input)

The XDPL8105 flyback transformer ***L_p*** and **Np/Ns selection** have to consider many factors relating to performance, such as the power factor, optimized iTHD (**Section 3.1.5**), optimum switching frequency range (**Section 3.1.6**), minimum dimming current (**Section 3.1.7**) and voltage rating of the MOSFET/output diode (**Section 3.1.11**). By referring to the system simulation/calculation output of these performance factors in this step, the user can find the optimized values for these 2 design inputs.

Of course, it is important to take note that whatever design is finalized in step 1 can only be valid provided the transformer inductance and all numbers of winding turns can fit in the transformer construction with the desired core/bobbin size (decided by the board form factor) and acceptable losses (conduction and core loss). Such transformer construction checks can be carried out easily with step 2 afterwards.

3.1.3 Input capacitor and MOSFET parasitic capacitor values input

Cin, input capacitor refers to the DC capacitor placed after the bridge rectifier. Higher Cin values give better EMI but worse power factors, and vice versa. However, please take note that different values here could have a slight impact on the minimum dimming level.

MOSFET Co(tr) refers to the MOSFET time-related effective output capacitance. It is mainly used to estimate the LC resonant period for more precise QR switching frequency estimation. As a start, please refer to the cell comment for a list of Co(tr) values based on Infineon MOSFETs.

Tips are available in the “Tips and Interactive Info” section to help the user to get the rough values of these inputs (as shown in the red-highlighted text in **Figure 10**)

Step 1: System Simulation & Transformer Design

Main Design Input

	min	typ	max	Tips & Interactive Info
Vin (Vrms)	90	230	277	AC input voltage (normal operation)
Vo (V)	18.0	31.5	45.0	Non-Dimming LED output voltage range
V_outOV setting(V)	46.0	48.4	55.6	Autoset to Vo_max/0.93; tolerance: -5%, +15%
I_out_set setting (A)		0.88		Output current at non-dimming condition
Efficiency (%)		90%		Est. Efficiency (Vin_min, Pout_max)
Iout Dimming?	Yes (Secondary side 0-10V dimming)			Iout Dimming option (see comment for details)
EN_OVP_In setting	Enabled			Input OVP (Enabled/Disabled?)
V_inOV setting (V)	306.0	329	352.0	Range: 297.9 ~ 396.2; Tolerance:+/-7%
Np/Ns Selection		3.870		Higher for better iTHD. Tips: Use 3.82 ~ 4.58
L_p (uH)		544.0		Higher for lower dim current. Tips: Use 512 ~ 768
Cin, Input capacitor (uF)		0.220		Tips: <40W: 0.15uF; 40 ~ 60W: 0.22uF
MOSFET Co(tr) (pF)		69.0		Tips: See comment for list of MOSFET Co(tr) values
f_sw_max setting (kHz)		180.80		Tips: ≤180.8kHz(if Tj≤125°C), ≤136.4kHz(if Tj >125°C)
N_DCM_MOD_GAIN setting		8		Tips: See comment. Modulation(Max:4, Min:32, Off:0)
t_on_min setting (us)		1.1		Tips: see comment. Range: 1~2.5
Normalized Ipri_avg simulation #1	Perfect Sine			Select checkpoint for iTHD optimization, if needed.
Normalized Ipri_avg simulation #2	Vin_typ, Vo_max			(Perfect Sine is just for reference purpose.)

ENTER DESIGN INPUT

Figure 10 Input capacitor and MOSFET parasitic capacitor values input (Step 1 Main design input)

3.1.4 IC timing parameters input

***f_sw_max* setting** refers to the controller maximum switching frequency parameterization. As shown in the tips (see red highlighted text in **Figure 11**), the maximum configurable value is limited according to the maximum operating junction temperature.

The lower *f_sw_max* setting could give better iTHD in most cases, particularly during high input voltage, because the system will shift more of its operating point over the AC input half-sine wave period from quasi-resonant (QR) valley switching to non QR valley switching. For more details, please refer to **Section 3.1.5** or **Figure 13**.

***N_DCM_MOD_GAIN* setting** refers to the modulation gain of the maximum allowable switching frequency over a half sine wave period. Its main purpose is to improve light quality when dimming with DCM switching. Furthermore, it also helps to improve the iTHD in most cases. User can adjust the modulation gain as following:

- Select “4” for maximum modulation gain
- Select “8” for high modulation gain
- Select “16” for medium modulation gain
- Select “32” for minimum modulation gain
- Select “0” for no modulation

Note: “0” setting option is only available if Iout dimming is set to “No” in step 1 main design input.

The lower *N_DCM_MOD_GAIN* setting (except value “0”) could give better iTHD in most cases, particularly during high input voltage, because the system will shift more of its operating point over the AC input half-sine wave period from quasi-resonant (QR) valley switching to non QR valley switching. For more details, please refer to **Section 3.1.5** or **Figure 14**.

***t_on_min* setting** refers to the XDPL8105 controller minimum on-time. Please use lower value to achieve a lower dimming level. However, if it is set too low, please beware that it could result to current steps while dimming. The setting range is shown in the tips (see red highlighted text in **Figure 11**).

Step 1: System Simulation & Transformer Design

Main Design Input

	min	typ	max	Tips & Interactive Info
Vin (Vrms)	90	230	277	AC input voltage (normal operation)
Vo (V)	18.0	31.5	45.0	Non-Dimming LED output voltage range
V_outOV setting(V)	46.0	48.4	55.6	Autoset to Vo_max/0.93; tolerance: -5%, +15%
I_out_set setting (A)		0.88		Output current at non-dimming condition
Efficiency (%)		90%		Est. Efficiency (Vin_min, Pout_max)
Iout Dimming?	Yes (Secondary side 0-10V dimming)			Iout Dimming option (see comment for details)
EN_OVP_In setting	Enabled			Input OVP (Enabled/Disabled?)
V_inOV setting (V)	306.0	329	352.0	Range: 297.9 ~ 396.2; Tolerance:+/-7%
Np/Ns Selection		3.870		Higher for better iTHD. Tips: Use 3.82 ~ 4.58
L_p (uH)		544.0		Higher for lower dim current. Tips: Use 512 ~ 768
Cin, Input capacitor (uF)		0.220		Tips: <40W: 0.15uF; 40 ~ 60W: 0.22uF
MOSFET Co(tr) (pF)		69.0		Tips: See comment for list of MOSFET Co(tr) values
f_sw_max setting (kHz)		180.80		Tips: ≤180.8kHz(if Tj≤125°C), ≤136.4kHz(if Tj >125°C)
N_DCM_MOD_GAIN setting		8		Tips: See comment. Modulation(Max:4, Min:32, Off:0
t_on_min setting (us)		1.1		Tips: see comment. Range: 1~2.5
Normalized Ipri_avg simulation #1	Perfect Sine			Select checkpoint for iTHD optimization, if needed.
Normalized Ipri_avg simulation #2	Vin_typ, Vo_max			(Perfect Sine is just for reference purpose.)

ENTER DESIGN INPUT

Figure 11 IC timing parameters input (Step 1 Main design input)

3.1.5 Simulation output: Primary average input current curve

For low iTHD, the primary average input current curve should be as close as possible to the shape of a positive half-sine waveform. Based on the step 1 main design input, this tool will simulate the normalized primary average input current curve across a AC input half-sine wave period for iTHD optimization. The simulation output is shown in the blue area on the right side of **Figure 12**.

The input and output voltage (Vin, Vo) conditions of the current curve simulation are based on checkpoint #1 and #2 in the main design input of step 1, as shown in the red circled box in **Figure 12**. Users can select any of the following for each simulation checkpoint (based on a non-dimming condition):

- Perfect Sine
- Vin_min, Vo_max
- Vin_min, Vo_min
- Vin_typ, Vo_max
- Vin_typ, Vo_typ
- Vin_typ, Vo_min
- Vin_max, Vo_max
- Vin_max, Vo_typ
- Vin_max, Vo_min

A practical use case example for users would be to choose either of the following options:

- Simultaneously simulate 2 current curves with different Vin, Vout conditions **OR**
- Simulate 1 current curve while having the other checkpoint set as “Perfect Sine” for reference/comparison.

In the example shown in **Figure 12** below, the user is comparing the primary average input current curve at "Vin_typ, Vo_max" (typical input voltage, maximum output voltage) with the "Perfect Sine" reference.

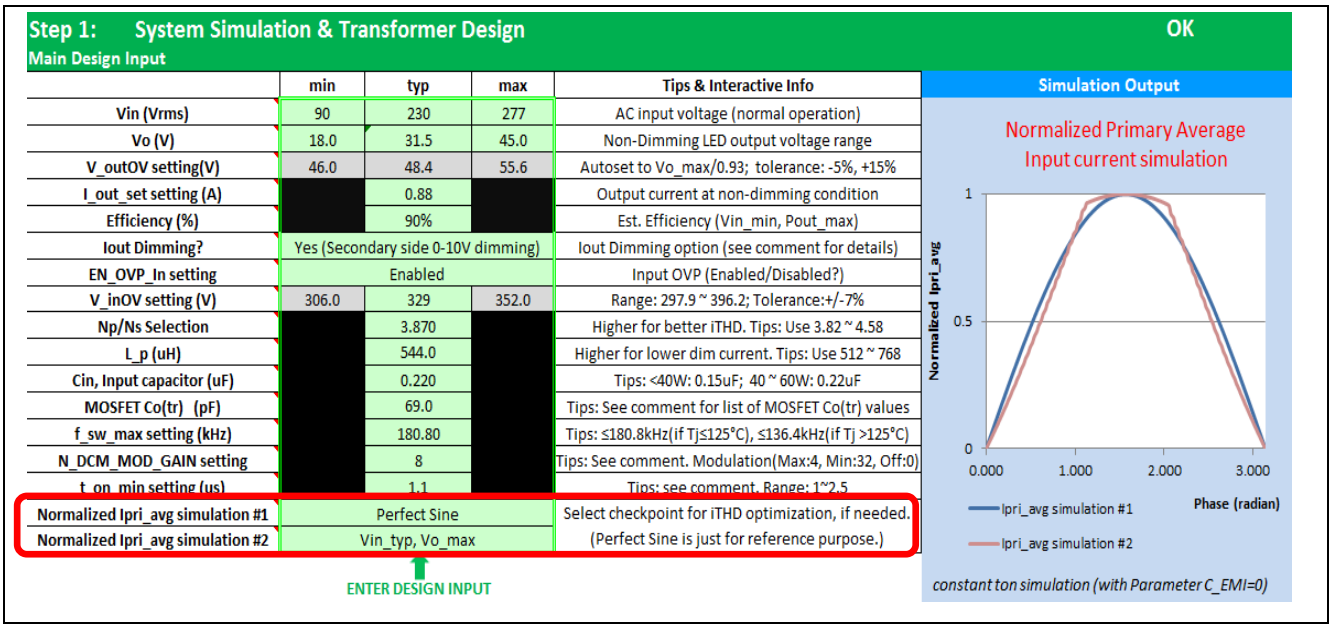


Figure 12 Normalized primary average current curve simulation checkpoint (for iTHD optimization)

It is possible to improve iTHD especially at high input voltages with the XDPL8105 by reducing the ***f_sw_max* setting** or ***N_DCM_MOD_GAIN* setting** as this will increase the non QR valley switching operating area across the AC input half-sine wave period (see the example in **Figure 13** & **Figure 14**).

However, please take note that there could be an impact on the efficiency especially at high input voltage as well if the non QR valley switching operating area increases too much, due to the higher switching loss.

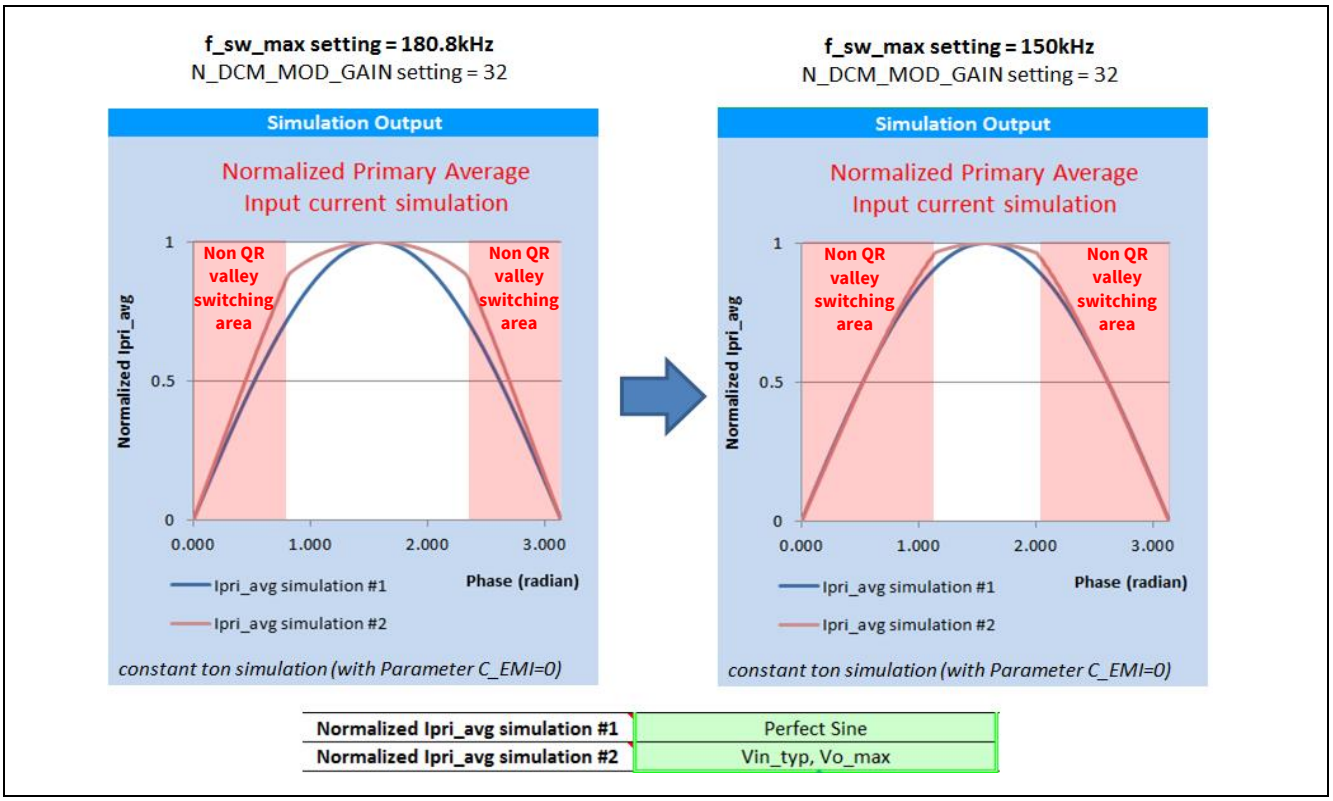


Figure 13 iTHD improvement by *f_sw_max* setting reduction

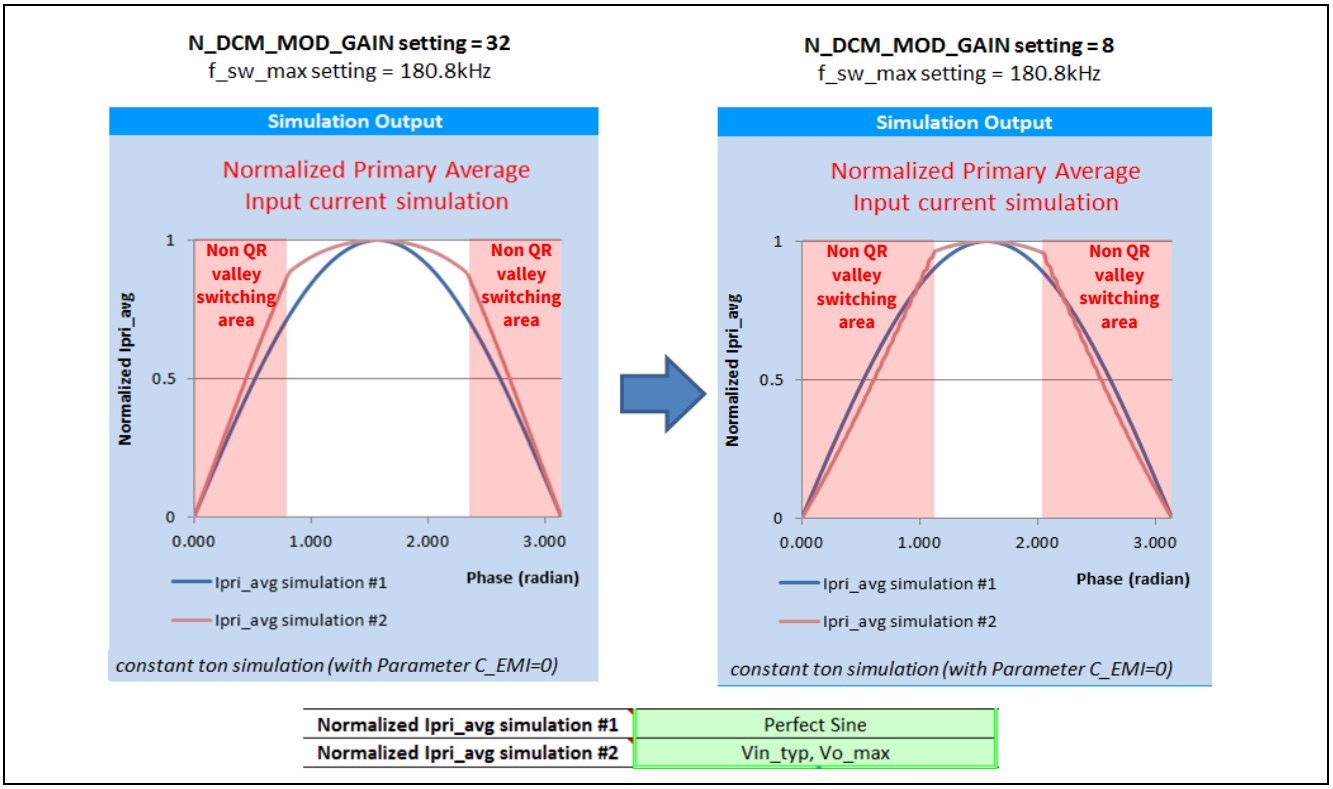


Figure 14 iTHD improvement by *N_DCM_MOD_GAIN* setting reduction

3.1.6 Non-dimming system switching behavior estimation

In step 1 section I, there will be a simulation/calculation of the system switching behavior with non-dimming at the peak of the input voltage sine wave (as shown in **Figure 15**).

Simulation/Calculation Output

I. Non-dimmming System switching behaviour at peak of input voltage sine wave

Vin (Vrms)	Vo (V)	Iout (A)	ton / (ton + tdemag)	t-valley1 (us)	Switching	Ipri_pk (A)	ton (us)	fsw (kHz)
90	18.0	0.88	0.35	0.61	QR	1.436	6.14	55.68
90	45.0	0.88	0.58	0.61	QR	2.311	9.88	56.47
230	18.0	0.88	0.18	0.61	QR	1.149	1.92	86.91
230	31.5	0.88	0.27	0.61	QR	1.427	2.39	106.79
230	45.0	0.88	0.35	0.61	QR	1.694	2.83	114.51
277	18.0	0.88	0.15	0.61	QR	1.127	1.56	91.14
277	31.5	0.88	0.24	0.61	QR	1.414	1.96	112.54
277	45.0	0.88	0.31	0.61	QR	1.711	2.38	120.03

Figure 15 Non-dimming system switching behavior (Step 1 Simulation/calculation output I)

t-valley1 refers to the timing between the end of demagnetization and the first QR valley. It is just a rough estimation based on the half-resonant period of ***L_pri*** & **MOSFET Co(tr)**. In **Section 3.1.3**, the suggestion is to enter a MOSFET Co(tr) value based on the MOSFET datasheet – but keep in mind that other parasitics are not yet considered, which could affect the accuracy of this calculation output.

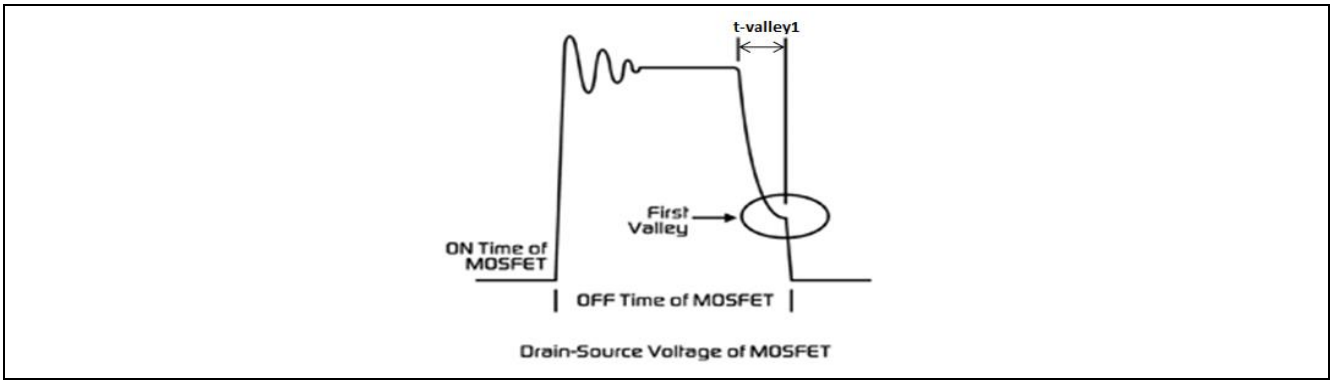


Figure 16 Example of t-valley1 timing in MOSFET drain voltage waveform

Switching refers to the switching characteristics and controller operation. There are 4 possible outputs here:

- QR: On-time controlled QR operating mode with valley switching (OK)
- *f_sw_max*: On-time controlled operating mode with *f_sw_max* & non QR valley switching (OK)
- ERROR: Invalid calculation as the system enters period-controlled DCM (NOT GOOD)
- CCM: Continuous conduction mode protection (NOT GOOD)

Ipri_pk refers to the primary peak current. If the tool detects that the Ipri_pk value (at Vin_min, Vo_max) is not the maximum of all conditions, an error will be shown.

ton refers to the MOSFET on-time. If ton < *t_on_min*, **Switching** will show “ERROR” because it means the controller enters the period-controlled DCM too early, which should not happen in non-dimming conditions.

fsw refers to the switching frequency. If fsw < 20 kHz, **Switching** will show “CCM”, which is not supported by the controller and the CCM protection will be triggered. If fsw = *f_sw_max*, **Switching** will show “f_sw_max”, which means the on-time controlled operating mode is with non QR valley switching due to *f_sw_max* limitation across the entire AC input half sine-wave period.

3.1.7 Vcc supply source selection and minimum output current estimation

In step 1 section II, the user has to select a **Vcc supply source** for the design and check the estimated minimum output current based on the related IC parameter settings (see red-circled boxes in **Figure 17**).

There are 2 possible choices, as shown below.

- External: The Vcc supply is not from the flyback AUX winding (e.g. external standby power circuit)
- Flyback AUX: The Vcc supply source is from the flyback AUX winding

If **Vcc supply source** = “Flyback AUX”, the minimum output current estimation can be lower than compared to **Vcc supply source** = “External” due to energy being drawn from the transformer via the AUX winding for the Vcc supply.

As shown in **Figure 17**, there are other design inputs that can be adjusted if needed. These design inputs are placed in this section because they mainly affect the output current at minimum dimming.

***EN_ABM* setting** refers to an IC parameterization input that enables or disables the active burst mode (ABM). If disabled, the controller will only operate in quasi-resonant (QR) mode and discontinuous conduction mode (DCM).

***f_sw_min_DCM* setting** refers to an IC parameterization input that sets the minimum DCM switching frequency. The configurable range is 3 ~ 20 kHz. Lower minimum output current can be achieved with lower f_sw_min_DCM setting but please beware of audible noise if configured to be less than 18 kHz.

ΔV of Vo_min @ min dim is a design input that defines the change percentage of **Vo_min** at minimum dimming input. The selectable value is 0%, -5%, -10%, … ,-25%. This input is needed because Vo_min (step 1 main design input) is defined for a non-dimmed condition; therefore the LED voltage at minimum dimming should be lower than Vo_min by a certain percentage. For instance, if Vo_min = 18 V and ΔV of Vo_min @ min dim is -10%, it means the voltage of a minimum number of LEDs is approx. 16.2 V at the ***I_out_dim_min*** **setting.**

I_out_dim_min **setting** refers to an IC parameterization input that sets the controller target output current at minimum dimming. The configuration range here is from 10 mA to I_out_set setting. It is highly recommended not to set this value too low to have reasonable output accuracy and startup time (see **Est. Worst Case Startup Time** calculation in **Section 3.1.8**).

Est. System Iout_min refers to the simulation output of the estimated system output current at the minimum dimming level. This value should be same or close to the ***I_out_dim_min*** **setting** for good output accuracy. If Iout Dimming is set to "No" in step 1 main design input, Est. System Iout_min will show "No Dimming".

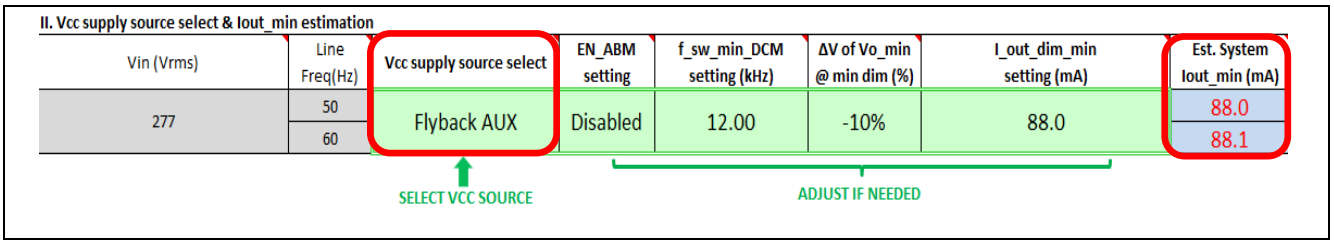


Figure 17 Vcc supply source select and minimum output current estimation (Step 1 Simulation/calculation output II)

3.1.8 Maximum output ripple, worst case startup time estimation

In step 1 section III, the user has to choose the optimum **output capacitor selection** based on the simulation results of maximum output ripple and worst case startup time estimation (see red-circled boxes in **Figure 18**).

As shown in **Figure 18**, there are also other design inputs that can be adjusted if needed. These design inputs are placed in this section because they mainly affect either the output ripple or the startup time.

Output Cap tolerance is the design input that defines the tolerance specification of the **output capacitor selection**. Based on this tolerance value, the minimum and maximum output capacitance will be used for estimating the maximum output ripple and worst case startup time, respectively.

NLED in series @ Vo_min is the design input which specifies the number of LEDs at **Vo_min**. For example, based on Vo_min = 18 V, the user can select either 6 or 7 from the dropdown box.

Dynamic resistance for each series LED @ ***I_out_set*** is the design input that specifies the dynamic resistance of a single LED at *I_out_set* setting which can be calculated from the I-V curve in the LED datasheet. The multiplication of this value with **NLED in series @ Vo_min** will be used to simulate **Est. Max Iout ripple**.

ΔV of Vo_max @ min dim is the design input that defines the percentage change of Vo_max at minimum dimming. The selectable value is 0%, -5%, -10%, … , -25%. This input is needed because Vo_max (step 1 main design input) is defined for the non-dimmed condition; therefore the LED voltage at minimum dimming should be lower than Vo_max by a certain percentage. For instance, if Vo_max = 45 V and the selected value is -10%, the voltage of the maximum number of LEDs is approx. 40.5 V at ***I_out_dim_min*** **setting**. The selected value here should be the same as **ΔV of Vo_min @ min dim** else there will be a warning.

R_HV **setting** refers to the design input of the resistor value connected in series with the XDPL8105 HV pin and it is also an IC parameterization value. This value only has an effect on the startup time but not on the output

ripple. The configurable range is dependent on the main design input. If the user inputs an out-of-range value, an error will pop up along with the configurable range.

Est. Max Iout Ripple is the simulation output that estimates the maximum output current peak-to-peak ripple percentage and it is likely at the Vo_min, *I_out_set* condition.

Est. Worst Case startup is the simulation output that estimates the worst case startup time (from AC input being applied to first light, regardless of light percentage) and is likely at the Vin_min, Vo_max, Iout_min condition (for non-dimming designs, it is based on ***I_out_set* setting** instead).

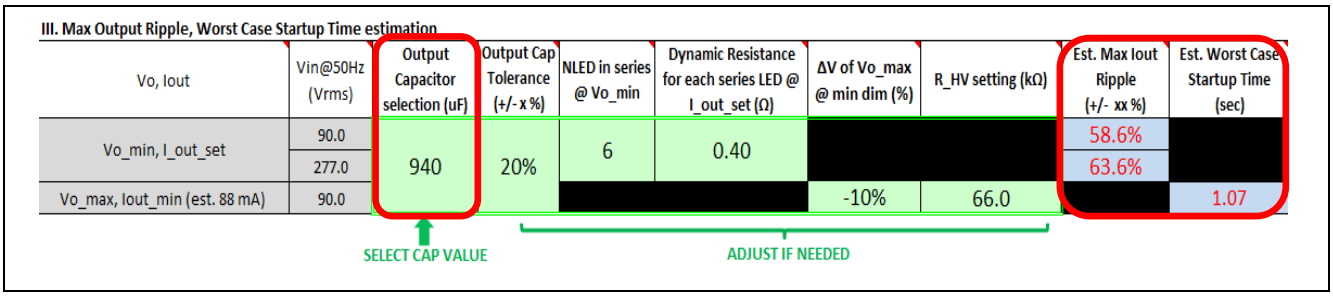


Figure 18 Max output ripple, worst startup time estimation (Step 1 Simulation/calculation output III)

3.1.9 Primary aux turns ratio and Vcc circuit design calculation

In Step 1 section IV, the user has to decide on the **Vcc cap** value and primary auxiliary winding turns ratio, **Na/Ns selection** based on the calculation output of **min Vcc cap**, **min Na/Ns** and **max Na/Ns** (see red-circled boxes in **Figure 19**).

Please take note that changing **Vcc cap** value would have an effect on the **Est. Worst Case Startup Time** in **Section 3.1.8**.

For the Vcc circuit design, the tool will also check and output whether **Pri Aux winding Vcc regulator needed** applies in the design based on the step 1 main design input and selected Vcc supply source in section II.

If Pri Aux winding Vcc regulator needed is “Yes”, the tool will calculate the **Vcc reg. min input cap** value as well.

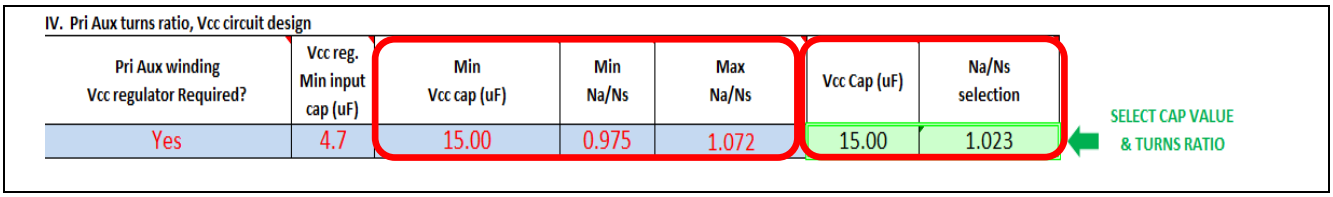


Figure 19 Primary aux turns ratio and Vcc circuit design (Step 1 Simulation/calculation output IV)

3.1.10 Secondary aux turns ratio and IEC60929-compliant 0-10 V circuit design (with CDM10V)

In step 1 section V, the user has to decide on the secondary auxiliary winding turns ratio, **Nsec_aux/Ns selection** based on the calculation output of **Min Nsec_aux/Ns** and **Max Nsec_aux/Ns** (see red-circled boxes in **Figure 20**).

CDM10V is a fully integrated 0-10V dimming interface IC from Infineon which transmits secondary side analog voltage based signals from 0-10V dimmer to primary side, by driving an external opto-coupler with a 5mA current based PWM signal. The secondary auxiliary winding is necessary to supply the operating voltage of CDM10V. For more details about CDM10V, please visit Infineon website: http://www.infineon.com/cdm10v

Therefore, please note that this section is only necessary if the Iout dimming option selected in step 1 main design input is “Secondary side 0-10 V Dimming”.

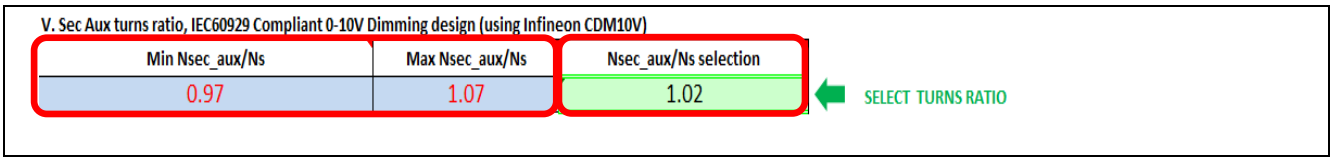


Figure 20 Secondary aux turns ratio, IEC60929-compliant 0-10 V dimming design (Step 1 Simulation/ calculation output V)

3.1.11 MOSFET Vds_max, output diode Vr_max estimation

Similar to any flyback transformer design, the maximum MOSFET drain voltage, **MOSFET Vds_max** and maximum output diode reverse voltage, **Output diode Vr_max** have to be calculated. Therefore, in step 1 section VI, the user has to check if these calculation outputs are ok for the component selection (see red-circled box in **Figure 21**).

The calculation will be based on 2 kinds of conditions, as shown below:

- Vin_max, V_outOV_Max (Output over-voltage protection at maximum input voltage)
- V_inOV_max, V_out_max (Input over-voltage protection at maximum output voltage)

Note: If input over-voltage protection, EN_OVP_In setting is “disabled”, calculating condition V_inOV_max above will be replaced by Vin_max instead.

For output over-voltage protection condition, if Vds_max is 800~900 V, there will be a warning; if it exceeds 900 V, there will be an error. For input over-voltage protection condition, if Vds_max exceeds either 800 V or 900 V, there will only be a warning.

As shown in **Figure 21**, there are other design inputs that can be adjusted if needed. These design inputs are placed in this section because they mainly affect the MOSFET Vds_max and output diode Vr_max.

MOSFET Vds_spike refers to the spike voltage (due to leakage inductance) on the MOSFET. As a rule of thumb, it should be at least 45% of **Vin_max**. For example, If Vin_max = 300Vac, the minimum value will be 135 V.

Output Diode Vr_spike refers to the spike voltage on the output diode. As a rule of thumb, it should be at least 40% of (**Vreflect_sec** + **V_outOV_max**). Vreflect_sec is the secondary winding reflection voltage when flyback MOSFET is switched on. V_outOV_max refers to maximum output over-voltage level.

If the **MOSFET Vds_max** is too high, the user can either reduce **Np/Ns selection** (Step 1 main design input) or **MOSFET Vds_spike,** but there is a risk of exceeding Vds_max in the actual board test if MOSFET Vds_spike is set too low.

If the **Output Diode Vr_max** is too high, the user can either increase **Np/Ns selection** (Step 1 main design input) or reduce **Output Diode Vr_spike,** but there is a risk of exceeding Vr_max in the actual board test if Output Diode Vr_spike is set too low.

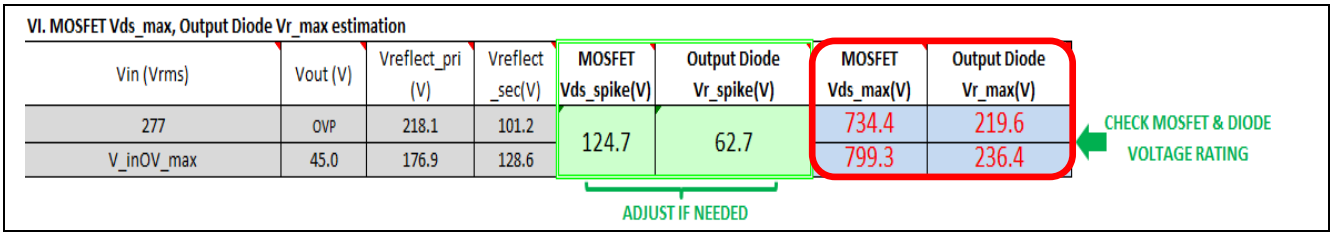


Figure 21 MOSFET Vds_max and output diode Vr_max (Step 1 Simulation/calculation output VI)

3.2 STEP 2 – Transformer construction (optional)

In step 2, the user can construct the transformer with suitable wires, core and bobbin for the board design. Upon completion without error in both step 1 and step 2, the transformer drawing is auto-generated.

However, step 2 is optional and can be skipped if not needed, which means that the user can still possibly proceed to complete step 3 for BOM and IC parameters generation despite an error/warning in step 2.

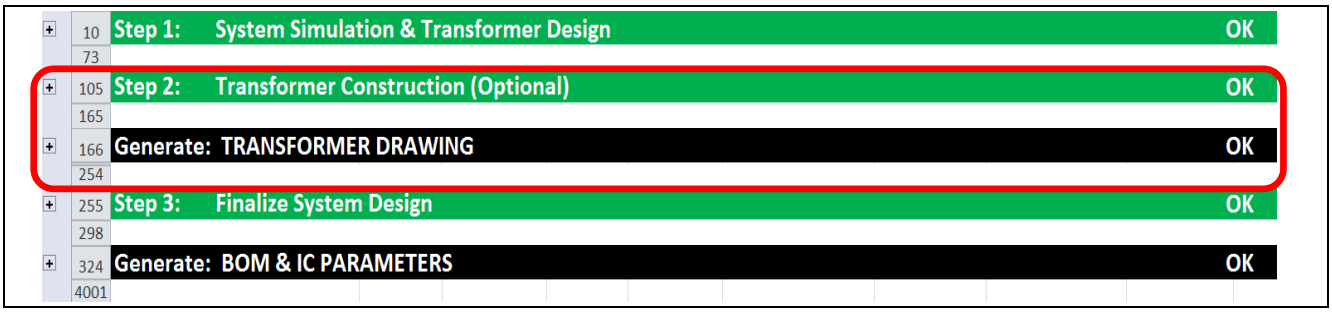


Figure 22 STEP 2 – Transformer construction (optional)

3.2.1 Core and bobbin selection input

Based on the **Bobbin Isolation Type** (Functional/Reinforced) and **Bobbin Mounting Type** (THT/SMD) design input by the user, the **Core Bobbin Selection** dropdown box will be updated and a list of suitable cores and bobbins will be shown (see **Figure 23**). THT and SMD refer to through-hole and surface mount, respectively.

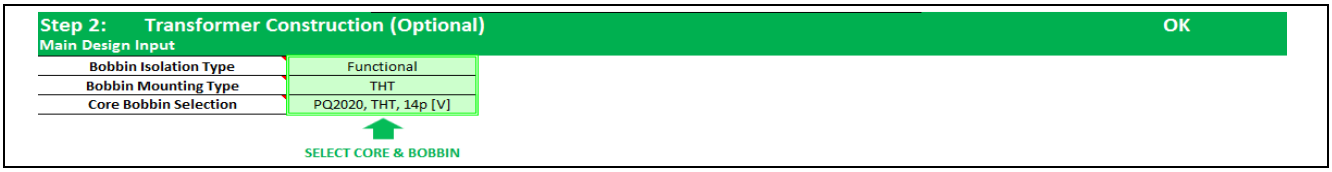


Figure 23 Core and bobbin selection (Step 2 Main design input)

Users can check the core and bobbin properties of the selection**,** as circled in red in **Figure 24.**

- Bobbin height, width, length
- Bobbin window, depth, perimeter
- Core effective cross sectional area, Ae and core volume
- Primary margin tape

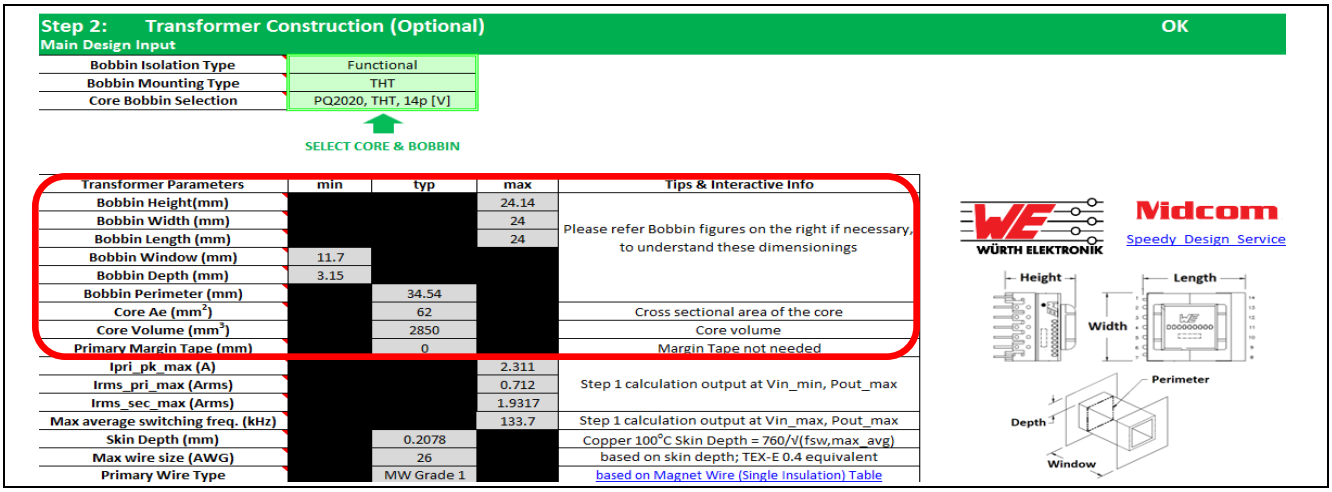


Figure 24 Selected core and bobbin properties display

Alternatively, users can define the core and bobbin properties by selecting “Others” in **Core Bobbin Selection** if the desired part is not in the list. A small table will appear on the right (circled in red in **Figure 25**), which allows the user to enter self-defined property values. There will be errors beside the table at first but once the table is filled up, these errors will disappear (as shown in **Figure 26**).

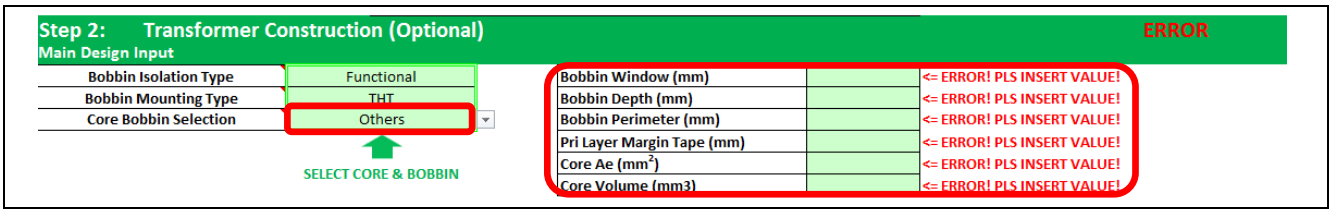


Figure 25 Self-defined core and bobbin properties by selecting “Others”

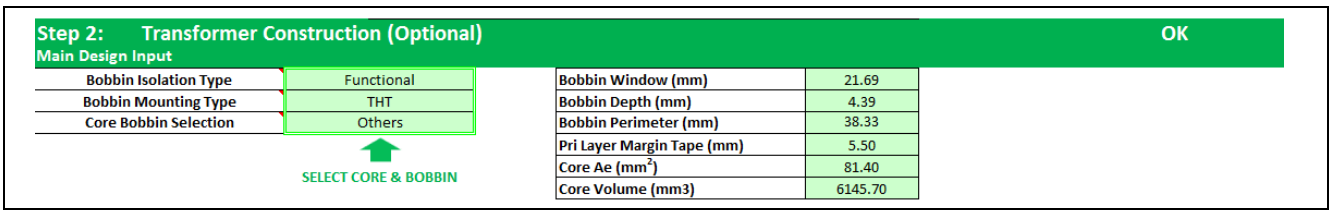


Figure 26 Example of inserting values of self-defined core and bobbin properties

Note: The user is not required to enter the bobbin height, width and length if “Others” is selected because these dimensions will only affect the board form factor but not the transformer winding construction itself.

3.2.2 Transformer electrical spec. (read-only information)

Apart from primary inductance and all turn ratios, the following step 1 calculation output will be passed to the step 2 design input (as circled in red box of **Figure 27**) for transformer construction calculation:

- **Ipri_pk_max**: Maximum primary peak current (Vin_min, Pout_max)
- **Irms_pri_max**: Maximum primary rms current (Vin_min, Pout_max)
- **Irms_sec_max**: Maximum secondary rms current (Vin_min, Pout_max)
- **Max average switching freq**: Maximum average switching frequency (Vin_max, Pout_max)

Users cannot modify these values because they are read-only information in step 2. Therefore, it is very important to complete step 1 with no errors before proceeding to step 2.

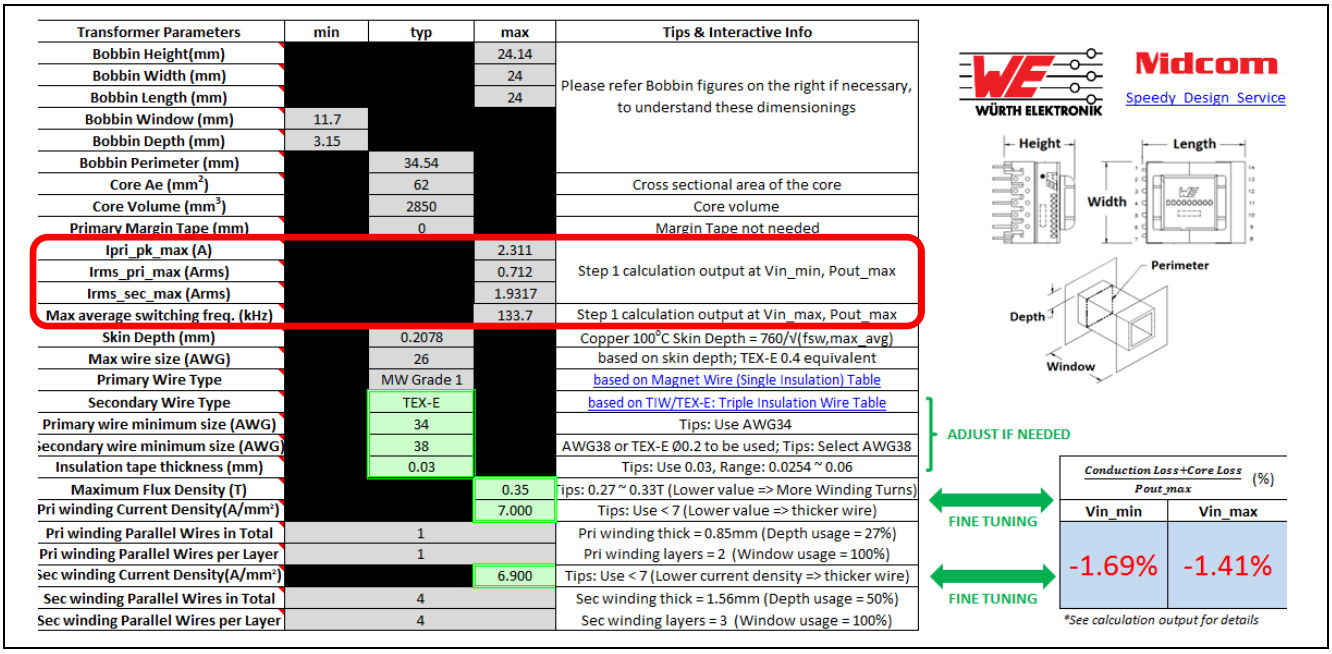


Figure 27 Transformer electrical spec. (read-only information in Step 2)

3.2.3 Skin depth and max wire size (read-only information)

AC electric current flows mainly at the "skin" of the conductor, between the outer surface and a level called the skin depth. Based on the average maximum switching frequency (at Vin_max, Pout_max condition), the skin depth will be calculated based on copper material at 100 °C.

This tool will then select the maximum wire size (AWG) based on the calculated skin depth. This is to avoid selecting wires with a high skin effect. This max wire size (AWG) is applied to the primary wire and TIW-type secondary wire while the max wire size for the TEX-E type secondary wire will also be shown in the “Tips & Interactive Info”. Please refer to **Section 3.2.4** for details about the wire type.

The skin depth and max wire size information is shown in the red box in **Figure 28**.

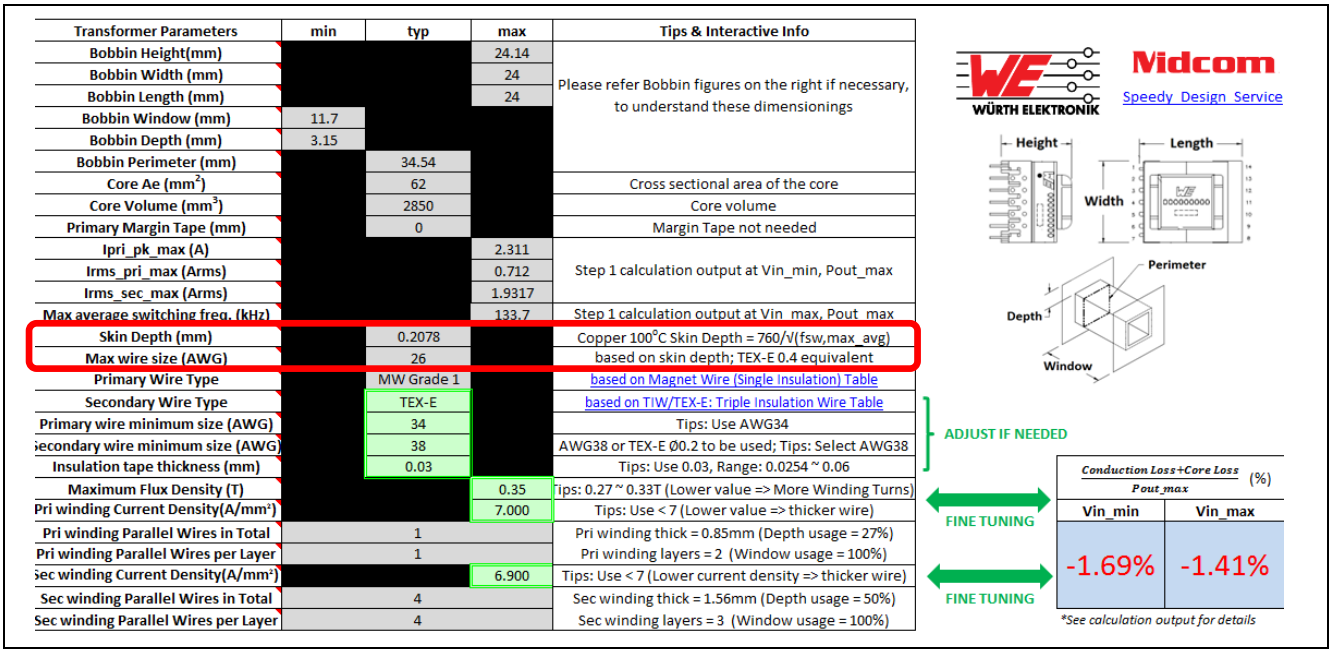


Figure 28 Skin depth and maximum wire size (read-only information of Step 2)

3.2.4 Wire type, minimum wire size and insulation tape thickness input

The **Primary wire type** is fixed as “MW Grade 1”, which means a magnet wire single insulation wire. 2 types of triple insulation wire can be selected for **Secondary wire types:**

- TIW (more common wire type, but the wire diameter is generally larger than TEX-E)
- TEX-E (preferred wire type if available because the wire diameter is generally smaller than TIW)

There is generally a limitation on using overly thin wire in transformer manufacturing. Therefore, the **Primary Wire minimum size** and **Secondary Wire minimum size** have to be specified. Users are recommended to follow the tips suggesting AWG34 for primary wire and AWG38 for secondary wire (as shown in **Figure 29**) or else it is also possible to select other wire size, according to their transformer supplier requirement.

Insulation tape is typically applied after each winding layer so it is necessary to specify the **insulation tape thickness.** Please follow the recommended value of 0.03 mm. Otherwise, the user can also specify the desired value within the range of 0.0254 ~ 0.06mm.

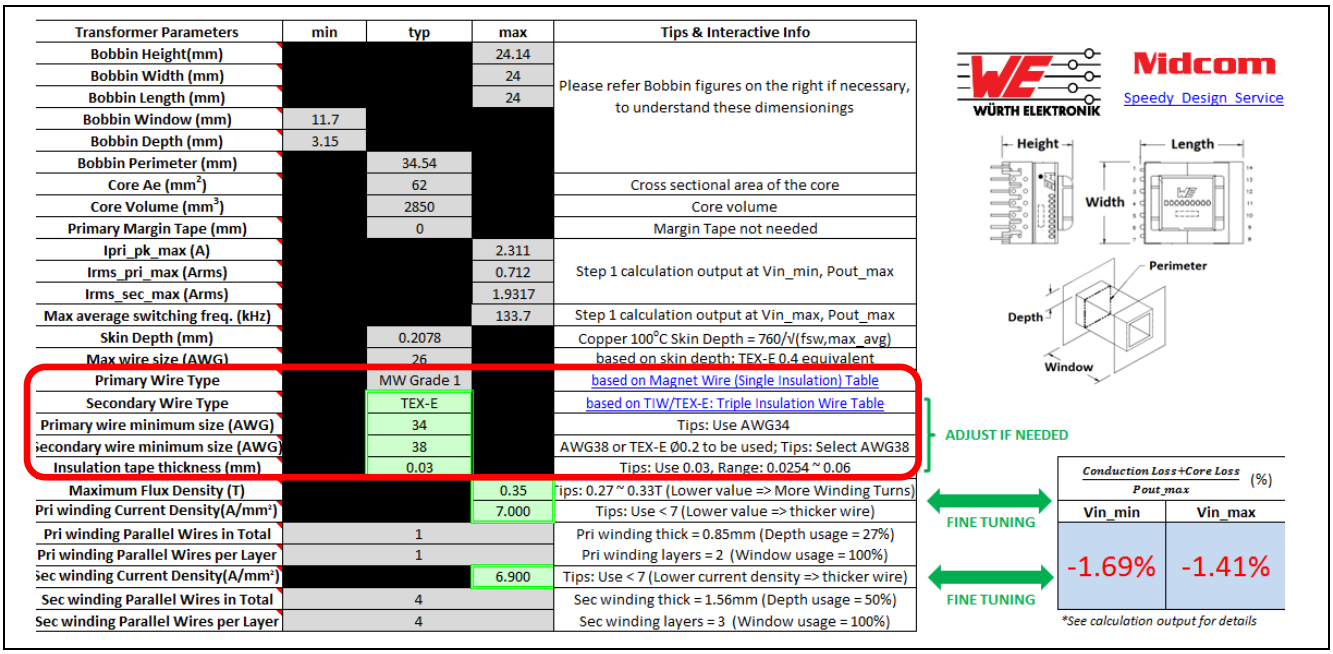


Figure 29 Wire type, min. wire size and tape thickness (Step 2 Main design input)

3.2.5 Maximum flux density and current density input (fine-tuning)

Maximum Flux Density input is required to calculate the number of turns needed for each winding. More winding turns are needed if the **Maximum Flux Density** input is lower, and vice-versa. The recommended value will be between 0.27 ~ 0.33 teslas. Maximum value is 0.35 teslas. These design inputs are shown in the red box in **Figure 30**.

Based on the **Pri Winding Current Density** and **Sec Winding Current Density** input, this tool will find the best combination of the following outputs from the wire tables (as shown in the “Wire” worksheet) that fits the calculated numbers of turns of each winding with the minimum bobbin depth usage.

- Wire Size
- Parallel Wire Number (total)
- Parallel Wire Number (for each layer)

*Note: This wire information is shown in the red box in **Figure 30**.*

In general, the depth usage or winding thickness will be higher if the current density input is lower and vice versa. As a rule of thumb, it is recommended to select a value ≤ 7 A/mm^2. To start, the user can set the following as an initial check to see if the selected core/bobbin could possibly fit the Step 1 transformer design.

- Maximum flux density = 0.35 teslas
- Both primary winding current density and secondary winding current density = 7 A/mm^2

If an error shows that the build is too thick, the user should consider selecting a larger core/bobbin or reduce **L_p** in step 1.

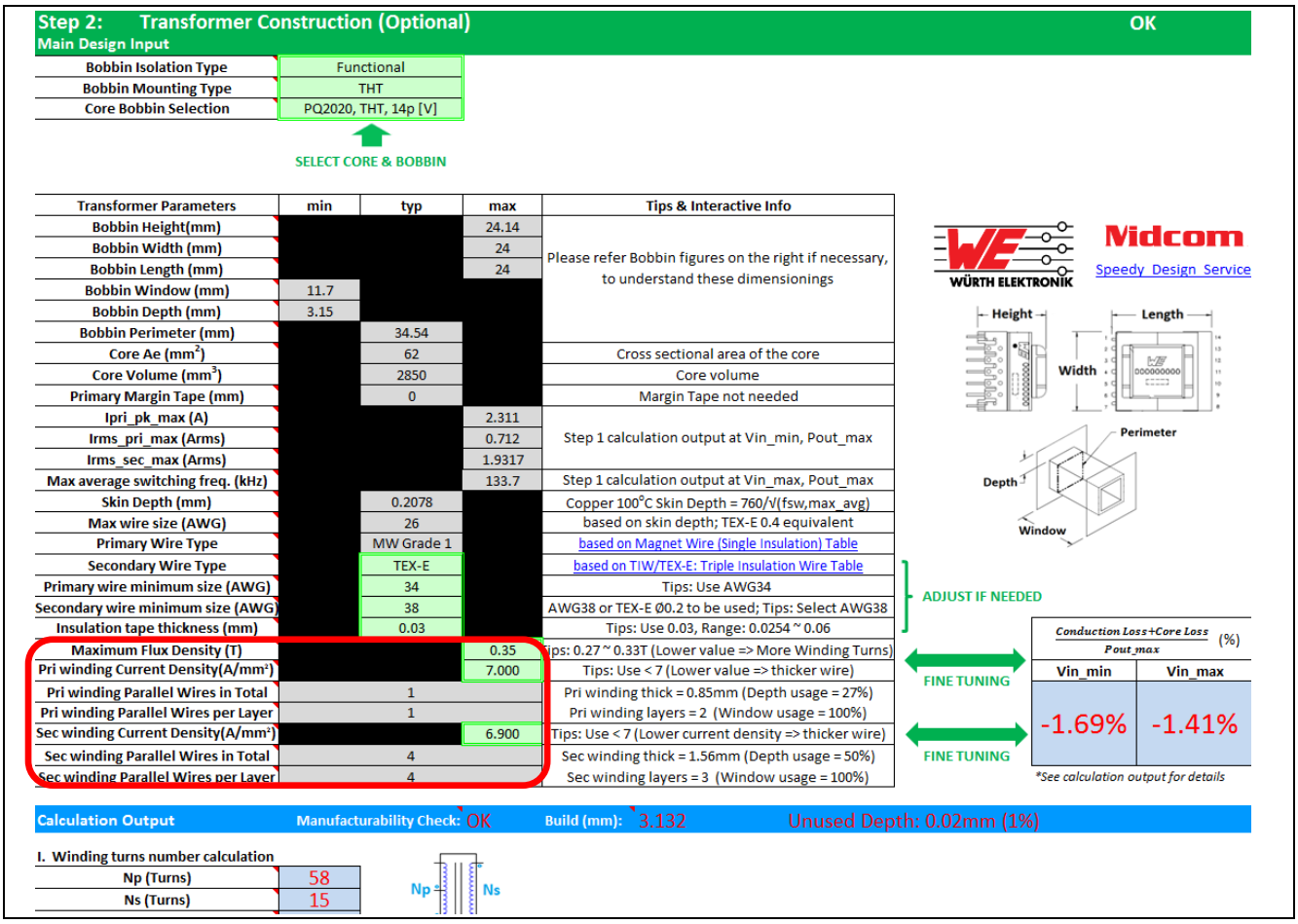


Figure 30 Maximum flux density and current density input (Step 2 Main design input)

If the initial check is ok, the user can fine-tune these 3 design inputs to further optimize the transformer design based on the following guide information generated by the tool (See red-circled parts a, b, c and d in **Figure 31**)

- Bobbin Depth and Window Usage Percentage

For each primary and secondary winding, the bobbin depth and window usage percentage will be calculated (see red-circled part a in **Figure 31**). It is suggested to maximize window usage (best case up to 100%).

- Manufacturability Check

Based on the total wire and tape layers of each winding with corresponding wire and tape thickness, the total build thickness is calculated. If it is less than the bobbin depth, the manufacturability check shows “OK”, else “NG” (see red-circled part b in **Figure 31**). Please note that this manufacturability check is just based on theoretical calculation, so it is important to confirm the manufacturability in actual production environment with the transformer supplier based on the auto-generated transformer drawing (see **section 3.2.9)**

- Build Information

If the manufacturability check is “OK”, the unused depth (in mm and percentage of bobbin depth) will be shown (see red-circled part c in **Figure 31**). If the manufacturability check is “NG”, for example, if the build thickness is 5 mm but the bobbin depth is 4 mm, the build information will show “ERROR! Build too thick(120% of Bobbin Depth used)”. For an optimized transformer design, the unused bobbin depth should not be too high.

- Conduction and Core Loss Percentage

The flux density and current density input fine-tuning should minimize the conduction and core losses of part d in **Figure 31**. This calculation does not include losses from other main components like the MOSFET and diode.

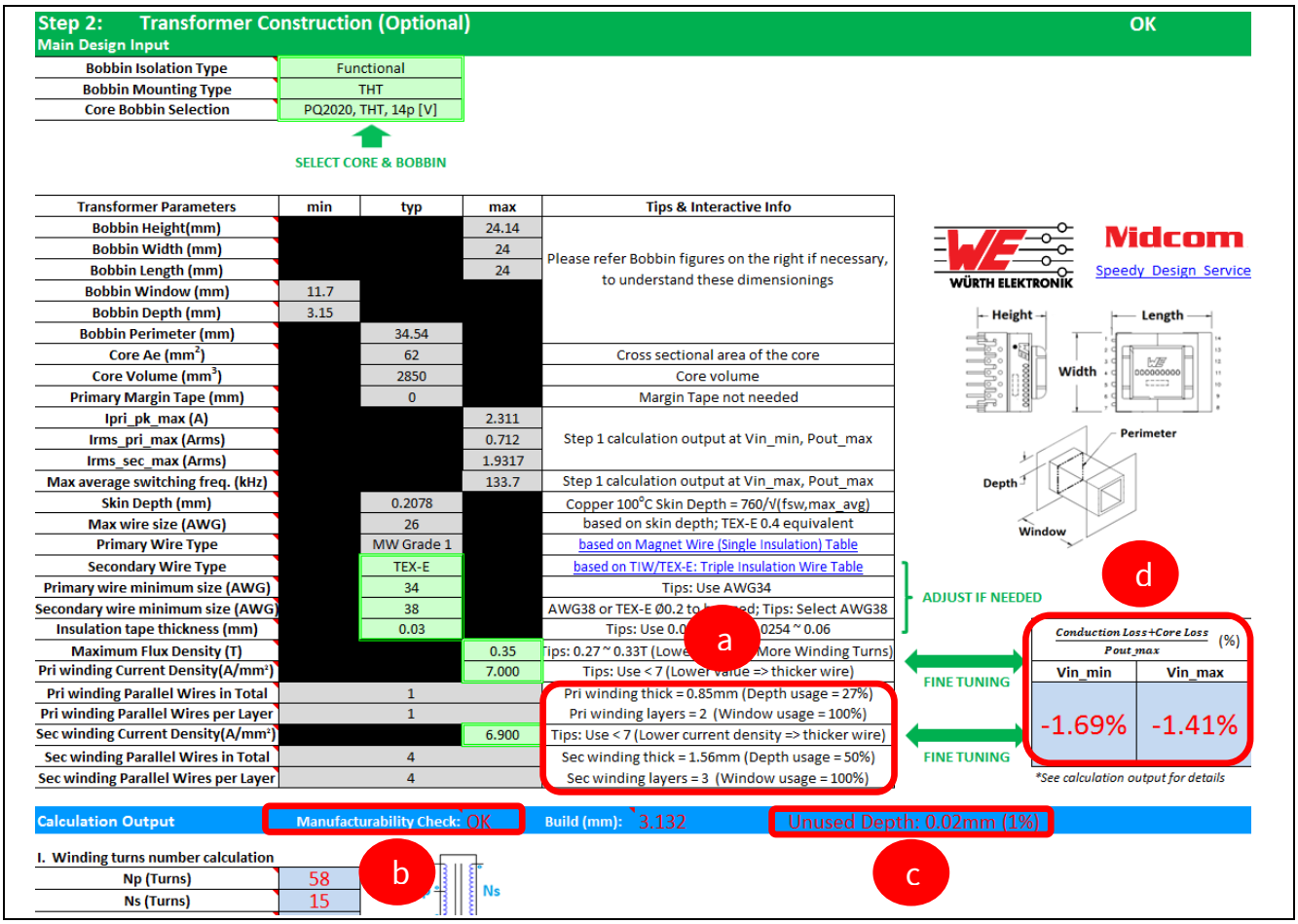


Figure 31 Guide information for fine-tuning of maximum flux density and current density

3.2.6 Calculation output for number of winding turns

In step 2 section I (see **Figure 32**), the number of winding turns for **Np** is calculated using the equation below:

$$Np = \frac{L_p * Ipri_pk_max}{Ae * Bmax}$$

Where

L_p: Primary inductance

Ipri_pk_max: Maximum primary peak current

Bmax: Maximum flux density

Ae: Effective core area

The absolute number of winding turns for **Ns**, **Na** and **Nsec_aux** will then be calculated based on the **Np/Ns**, **Na/Ns** and **Nsec_aux/Ns selection** from step 1.

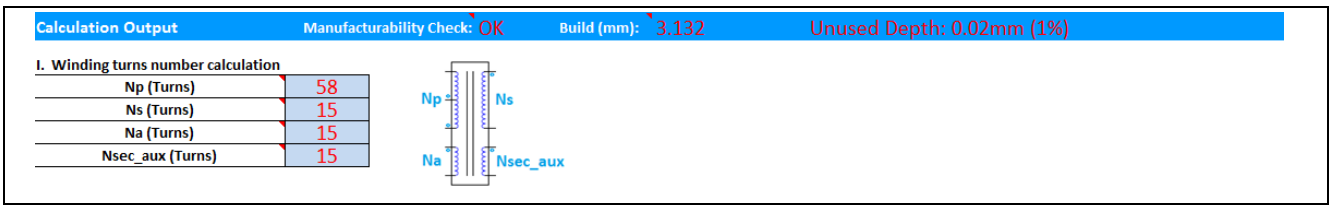


Figure 32 Calculation of number of winding turns (Step 2 Calculation output I)

3.2.7 Winding turns ratio check and comparison

Despite using the step 1 design input turns ratio to calculate the absolute number of winding turns for **Ns**, **Na** and **Nsec_aux** in the calculation output section I, the ratios of turns (based on the step 2 transformer construction) might vary due to limited ratio combinations. Therefore, the ratios of winding turns can be checked and compared in calculation output section II, as shown in **Figure 33**.

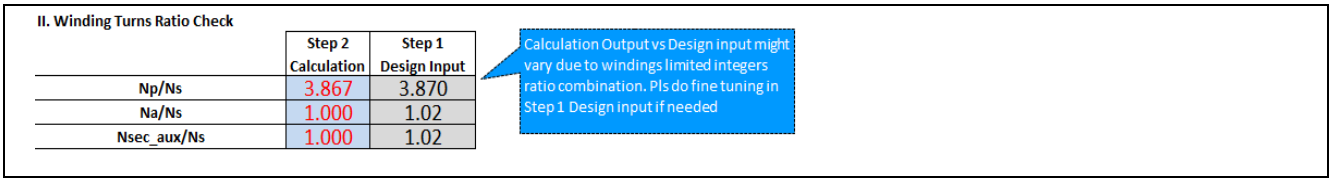


Figure 33 Check and compare ratio of winding turns (Step 2 Calculation output II)

3.2.8 Estimated transformer losses

The transformer losses are calculated for the following two conditions:

- Vin_min, Pout_max (calculation output section III in **Figure 34**)
- Vin_max, Pout_max (calculation output section IV in **Figure 34**)

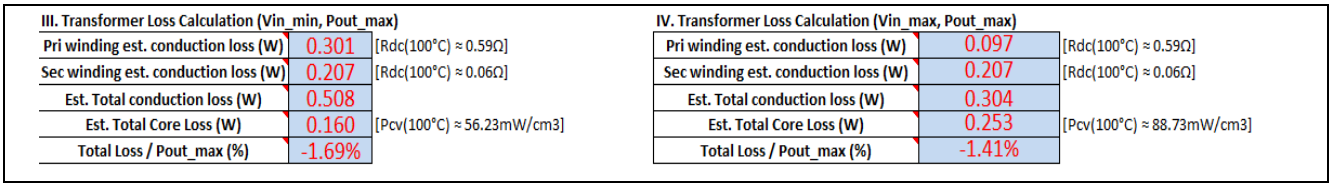


Figure 34 Estimated transformer losses (Step 2 Calculation output sections III & IV)

The following calculated outputs are generated for each section or condition.

- Primary winding estimated conduction loss

$= I_pri_rms^2 \times Rdc_pri(100°C)$ [unit: W]

$$Rdc_pri(100°C) = \frac{\rho_{copper(100°C)} \times l_{pri}}{N_{total(pri)} \times A_{wire(pri)}}$$ [unit: Ω]

where:

$\rho_{copper(100°C)} = 2.22 \times 10^{-8}$ [unit: Ωm]

$l_{pri} = Np \times \{bobbin\ perimeter + (bobbin\ depth \times 4)\}$ [unit: m]

$N_{total(pri)} = number\ of\ primary\ parallel\ wires\ in\ total$

$A_{wire(pri)} = conductor\ cross\ section\ area\ of\ each\ primary\ parallel\ wire$ [unit: m²]

Secondary winding estimated conduction loss

$= I_sec_rms^2 \times Rdc_sec(100°C)$ [unit: W]

$Rdc_sec(100°C) = \frac{\rho_{copper(100°C)} \times l_{sec}}{N_{total(sec)} \times A_{wire(sec)}}$ [unit: Ω]

Where:

$\rho_{copper(100°C)} = 2.22 \times 10^{-8}$ [unit: Ωm]

$l_{sec} = Ns \times \{bobbin\ perimeter + (bobbin\ depth \times 4)\}$ [unit: m]

$N_{total(sec)} = number\ of\ secondary\ parallel\ wires\ in\ total$

$A_{wire(sec)} = conductor\ cross\ section\ area\ of\ each\ secondary\ parallel\ wire$ [unit: m²]

Estimated total conduction loss

$= I_pri_rms^2 \times Rdc_pri(100°C) + I_sec_rms^2 \times Rdc_sec(100°C)$ [unit: W]

Estimated total core loss

$= Pcv_{100°C,PC44} \times core\ volume$ [unit: W]

$$Pcv_{100°C,PC44} = \frac{1}{\pi} \times \int_{\theta=0}^{\pi} 6.674 \times 10^{-7} \times f_{sw}(\theta)^{1.412} \times B(\theta)^{2.567}\ d\theta$$

where:

$f_{sw}(\theta) = switching\ frequency\ of\ AC\ input\ sine\ phase\ angle$

$B(\theta) = flux\ density\ of\ AC\ input\ sine\ phase\ angle$

Total loss percentage over Pout_max

$= \frac{\text{Est. conduction loss+core loss}}{\text{Pout_max}} \times 100\%$

3.2.9 Auto-generated transformer drawing

If no error is found in both steps 1 and 2, a transformer drawing will be generated, as shown in **Figure 35**. Please note that it is still necessary for the user to input the transformer pin assignment (see the light-green cells in **Figure 35**) based on the board schematic and PCB layout design to finalize the transformer drawing.

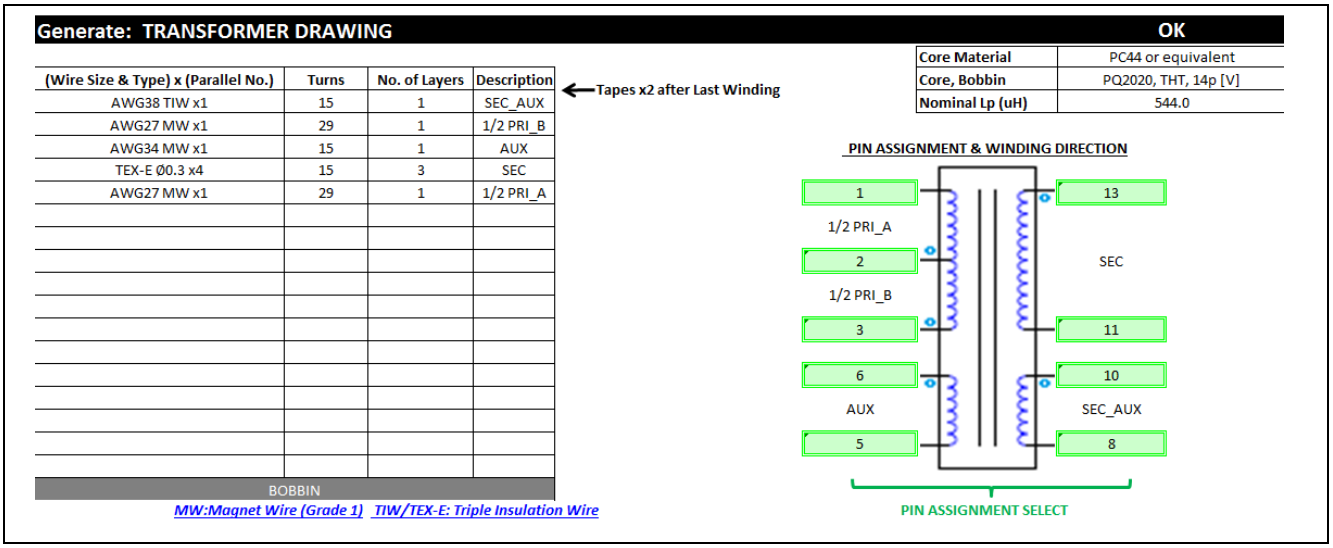


Figure 35 Generated transformer drawing (end of Step 2)

3.3 STEP 3 – Finalize system design

In this last step, the user has to finalize the system design as outlined below:

- CS shunt resistor selection and maximum power loss estimation
- ZCD series and shunt resistor selection and maximum power loss estimation
- Primary RCD snubber design
- Output bleeder (active/passive) design

Upon completion of steps 1 and 3 without error, the BOM and IC parameters are auto-generated, as shown in **Figure 36**.

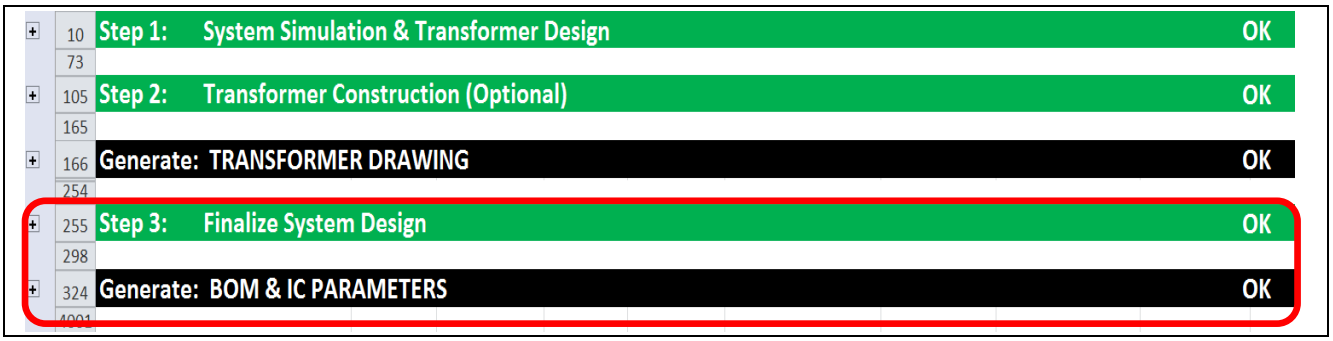


Figure 36 STEP 3 – Finalize system design

3.3.1 CS resistor preference input

The **CS Resistor Preference** allows users to select either one of the options shown below:

- Higher output accuracy

This selection allows higher resolution of the primary peak current measurement but higher power dissipation with a higher resistance value.

- Lower power dissipation

This selection allows lower power dissipation but lower resolution of the primary peak current measurement with a lower resistance value.

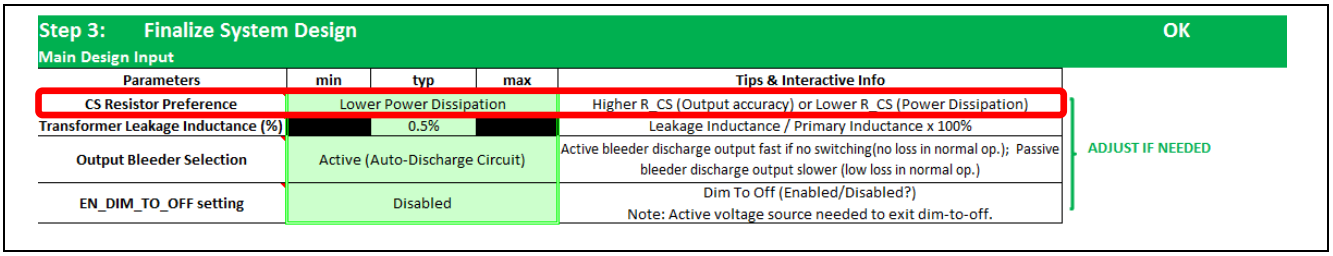


Figure 37 CS resistor preference (Step 3 Main design input)

3.3.2 Transformer leakage inductance percentage input

The **Transformer Leakage Inductance** (in percentage) over primary inductance needs to be input by the user for RCD snubber design calculation (see **Section 3.3.7**). The typical value of a good design could be around 0.5 to 1%. The user can select a value of 0.5%, 1.0%, 1.5%, 2.0%, 2.5% or 3.0%.

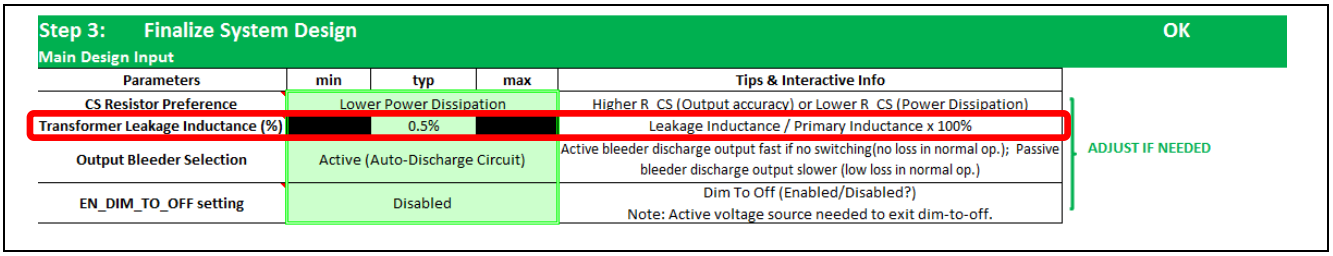


Figure 38 Transformer leakage inductance percentage (Step 3 Main design input)

3.3.3 Output bleeder selection input

Selection of an output bleeder is mandatory for flyback primary side control to ensure the output will not be over-charged under no-load condition (e.g. LED not connected). There are two options available:

- Active (auto-discharge circuit)

An output will only be discharged by the bleeder resistor when transformer switching is stopped (e.g. during AC-off or dim-to-off). The component count is higher but there is no drop in efficiency and fast discharge occurs with low bleeder resistances.

- Passive (dummy resistor)

An output will be always discharged by a dummy resistor connected in parallel with output LEDs. The component count is the lowest but there is a slight drop in efficiency and slow discharge with high bleeder resistances.

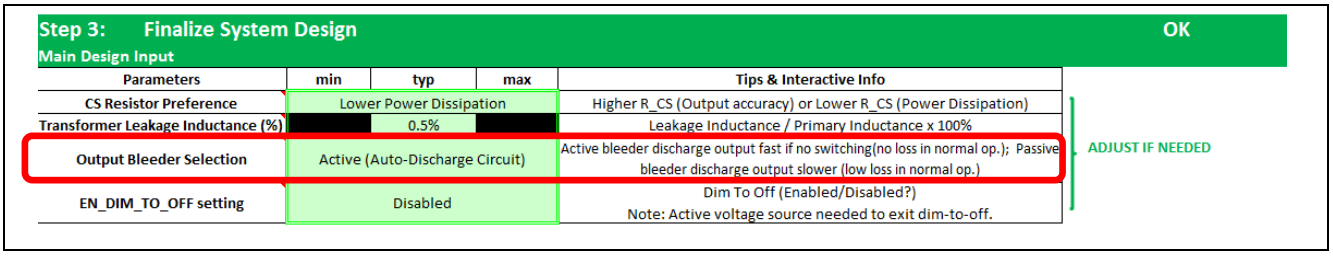


Figure 39 Output bleeder selection (Step 3 Main design input)

3.3.4 Dim-to-off setting input

The XDPL8105 allows dim-to-off operation but it requires an active voltage source to exit from dim-to-off.

The **EN_DIM_TO_OFF setting** allows users to enable/disable such operations but it is strongly recommended to enable it only when the application design is for primary side dimming and an external Vcc supply. Therefore, step 3 will show a warning if this setting is enabled but the step 1 design inputs (**Iout Dimming** and **Vcc supply source**) do not meet these two requirements.

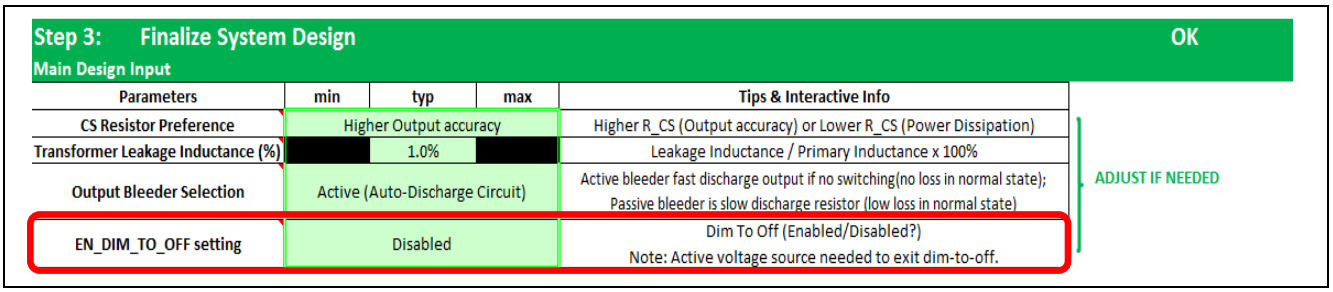


Figure 40 Dim-to-off setting (Step 3 Main design input)

3.3.5 CS pin-related design calculation

In step 3 section I, the user has to decide on an ***R_CS* Selection** or CS shunt resistor selection (see red-circled part in **Figure 41**).The selection value should be between the calculation ouputs for **Min *R_CS*** and **Max *R_CS*.**

The **Min *R_CS*** and **Max *R_CS*** are calculated based on the maximum of **Ipri_pk** (from Step 1 calculation output section I) and **CS Resistor Preference** (from Step 3 main design input) based on the following equations:

If **CS Resistor Preference** is set to “higher output accuracy”,

$$Min\ R_CS = \frac{0.98}{I_pri_pk_max} \qquad Max\ R_CS = \frac{1.08}{I_pri_pk_max} \qquad \text{[unit: Ω]}$$

If **CS Resistor Preference** is set to “lower power dissipation”,

$$Min\ R_CS = \frac{0.49}{I_pri_pk_max} \qquad Max\ R_CS = \frac{0.54}{I_pri_pk_max} \qquad \text{[unit: Ω]}$$

R_CS Selection Max Power Loss refers to the maximum power loss calculation based on the *R_CS* Selection input by the user. The equation is as shown below:

$$P_{loss,\max(R_{CS})} = I_pri_rms^2 \times R_CS\ Selection \qquad \text{[unit: W]}$$

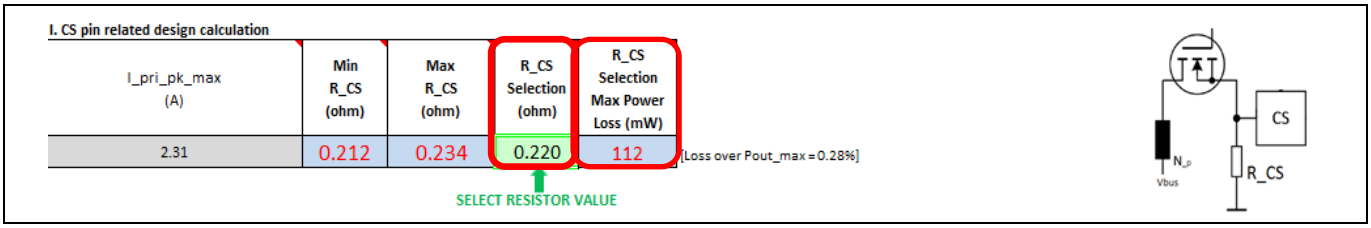


Figure 41 CS pin-related design calculation (Step 3 Calculation output I)

3.3.6 ZCD pin-related design calculation

In step 3 section II, the user has to decide on the *R_ZCD_1* selection and *R_ZCD_2* selection (see the red-circled part in **Figure 42**).

R_ZCD_1* Selection** should be between the calculation outputs for **Min *R_ZCD_1 and **Max *R_ZCD_1***, which are based on the equations below:

$$Min\ R_ZCD_1 = \frac{(Vin_\max \times 107\%)\times\sqrt{2}\times\frac{Na}{Np}-0.22}{3} \quad \text{[unit: kΩ]}$$

$$Max\ R_ZCD_1 = \frac{(Vin_\max \times 107\%)\times\sqrt{2}\times\frac{Na}{Np}-0.15}{1.9} \quad \text{[unit: kΩ]}$$

Note: The highest value for Max R_ZCD_1 is 100 kΩ. If input OVP is enabled, Vin_max in the equations will be replaced by V_inOV typical value.

R_ZCD_2* Selection** should be between the calculation outputs for **Min *R_ZCD_2 and **Max *R_ZCD_2***, which are based on the equations below:

$$Min\ R_ZCD_2 = \frac{R_ZCD_1\ Selection}{(V_outOV_\max \times \frac{Na}{Ns} \div 1.9) - 1} \quad \text{[unit: kΩ]}$$

$$Max\ R_ZCD_2 = \frac{R_ZCD_1\ Selection}{(V_outOV_\max \times \frac{Na}{Ns} \div 2.3) - 1} \quad \text{[unit: kΩ]}$$

***R_ZCD_1* Selection Max Power Loss** refers to the maximum power loss calculation based on the ***R_ZCD_1* Selection** input by the user.

II. ZCD pin related design calculation

Min R_ZCD_1 (kohm)	Max R_ZCD_1 (kohm)	Min R_ZCD_2 (kohm)	Max R_ZCD_2 (kohm)	R_ZCD_1 Selection (kohm)	R_ZCD_2 Selection (kohm)	R_ZCD_1 Selection Max Power Loss (mW)	
43.9	69.2	1.94	2.36	56.2	2.00	54	[Loss over Pout_max = 0.14%]

SELECT RESISTOR VALUE

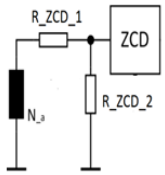


Figure 42 ZCD pin-related design calculation (Step 3 Calculation output II)

3.3.7 Primary RCD snubber design calculation

In step 3 section III, the user has to decide on the **Csn Selection** for the primary RCD snubber (see red-circled part in **Figure 43**). The primary RCD snubber is to clamp the MOSFET spike voltage, caused by the transformer leakage inductance. Generally, higher Csn values will result in lower Rsn values needed in the RCD snubber design. Please choose a standard capacitor value for **Csn Selection** within the range of 2200 ~ 47000 pF.

L_p_lk is calculated by multiplying the ***L_p*** and **Transformer leakage inductance** percentage inputs.

MOSFET Vds_spike is read-only and refers to the MOSFET drain voltage spike based on the step 1 section VI input.

Recommended Initial Rsn for the primary RCD snubber is calculated based on the equation below:

$$Rsn = \frac{t_{discharge}}{\boldsymbol{Csn\ Selection} \cdot \ln\left(\frac{\Delta V_{Csn} - Vds_spike}{Vds_spike}\right)}$$

where:

$$t_{discharge} = \frac{1}{f_{sw(Vin_max,Pout_max)}} - \frac{\pi}{2} \cdot \sqrt{L_p_lk \cdot Csn}$$

$$\Delta V_{Csn} = Vds_max - \sqrt{Vds_max^2 - \frac{L_p_lk \cdot I_{pri_pk(Vin_max,Pout_max)}{}^2}{Csn}}$$

$$Vds_max = Vin_\max \cdot \sqrt{2} + \frac{Np}{Ns} \cdot Vout_\max + Vds_spike$$

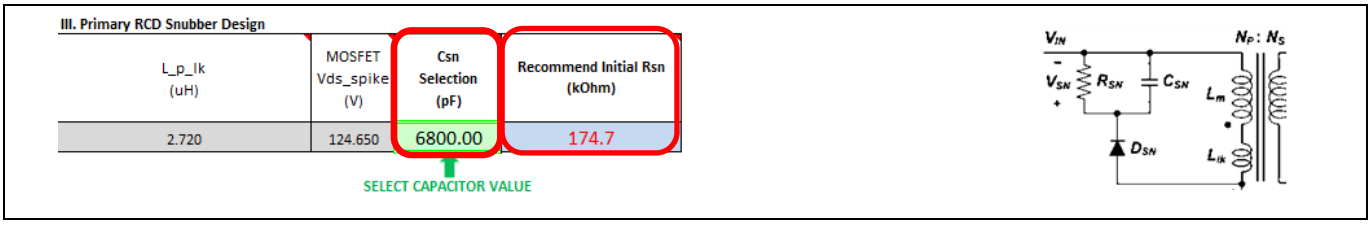


Figure 43 Primary RCD snubber design calculation (Step 3 Calculation output III)

3.3.8 Output bleeder design calculation

Based on the **output bleeder selection** in the step 3 main design input, the user has to make a **bleeder resistor selection**.

As shown in **Figure 44**, there are also design inputs that can be adjusted if needed. These design inputs are placed in this section because they mainly affect the output bleeder design calculation.

- ***Reaction_OVP_Vout* setting:**

  IC parameterization to set the reaction of the output over-voltage protection (selectable value is “Auto-Restart” or “Latch”)

- ***t_auto_restart* setting:**

  IC parameterization to set the auto restart time for all protections with reaction = "Auto-Restart" and speed of reaction = "Slow" (selectable value is ***t_auto_restart_fast*** ~ 10 sec)

- ***t_auto_restart_fast* setting:**

  IC parameterization to set the auto restart time for all protections with reaction = "Auto-Restart" and speed of reaction = "Fast” (selectable value is 0.2 ~ 10 sec)

- ***Speed_OVP_Vout* setting:**

  IC parameterization to set the speed of reaction for the output over-voltage protection (selectable value is “Slow” or “Fast”)

The calculation output below will then be generated:

- Vout OVP auto-restart time:

  Output over-voltage protection auto-restart time based on the IC parameterization above.

- Max Bleeder Resistance:

  Maximum bleeder resistance calculation output. **Bleeder resistor Selection** should not exceed this value.

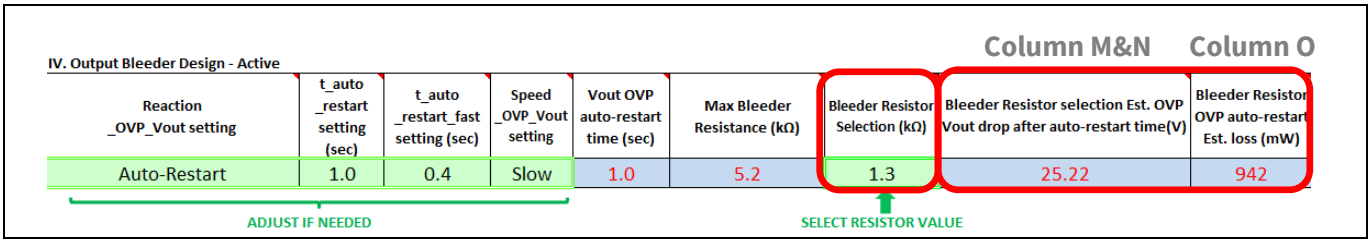


Figure 44 Output bleeder design calculation (Step 3 Calculation output V)

In the column M&N calculation output (see **Figure 44**), the tool will then calculate the estimated output voltage drop with the selected bleeder resistor value over a period of time dependent on the ***Reaction_OVP_Vout* setting**, as shown in **Table 1**.

Table 1 Calculation output of column M&N based on conditions

Reaction_OVP_Vout setting	Calculation output (column M&N)
Auto-restart	Bleeder Resistor Selection Est. OVP Vout drop after auto-restart time
Latch mode	Bleeder Resistor Selection Est. OVP Vout drop after 3-sec. discharge

In the column O calculation output (See **Figure 44**), the estimated loss of the bleeder resistor selection is calculated based on the ***Reaction_OVP_Vout* setting** and the highest loss condition, as shown in **Table 2**.

Table 2 Calculation output for column O based on conditions

<table>
<tr><td rowspan="2">*Reaction_OVP_Vout* setting</td><td colspan="2">Est. Loss of Bleeder Resistor Selection</td><td rowspan="2">Calculation Output (Column O)</td></tr>
<tr><td>OVP auto-restart</td><td>Normal Operation</td></tr>
<tr><td rowspan="2">Auto-restart</td><td>Higher</td><td>Lower</td><td>Bleeder Resistor OVP auto-restart Est. Loss</td></tr>
<tr><td>Lower</td><td>Higher</td><td rowspan="2">Bleeder Resistor Normal Operation Est. Loss</td></tr>
<tr><td>Latch mode</td><td>Not applicable</td><td>Any value</td></tr>
</table>

3.3.9 Auto-generated BOM & IC parameters

If the user has completed step 2 with the desired core and bobbin without errors, please **select generate option for T1** as “AUTO GENERATE BASED ON STEP 2” (see **Figure 45**).

Otherwise, please select “MANUAL KEY IN” which requires the user to enter **Np** manually (see **Figure 46**).

Note: T1 refers to the reference designator of flyback transformer

ERROR CHECK here will detect if there are any errors in each of the steps. If detected, it will show in which step the error is located and the user should resolve the error or errors accordingly (as shown in **Figure 45** with “NO ERROR FOUND”). This is to ensure that the generated BOM and IC parameters are correct.

WARNING CHECK here will detect if there are any warnings in each of the steps. If detected, it will show in which step the warning is located. It is recommended to resolve the warnings (as shown in **Figure 45** with "NO WARNING FOUND") but this is not mandatory. The BOM and IC parameters can still be generated with warnings.

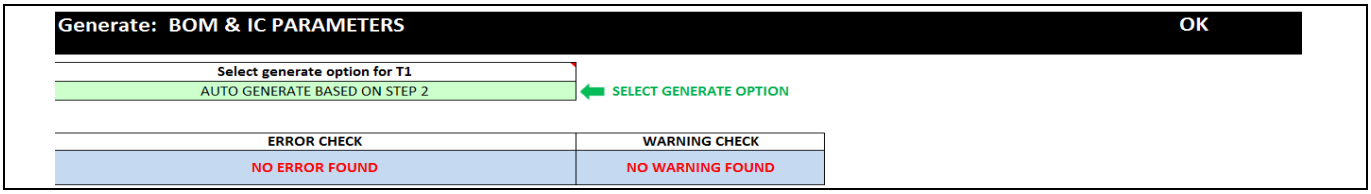


Figure 45 Flyback transformer, T1 parameter-generating option ("AUTO GENERATE BASED ON STEP 2")

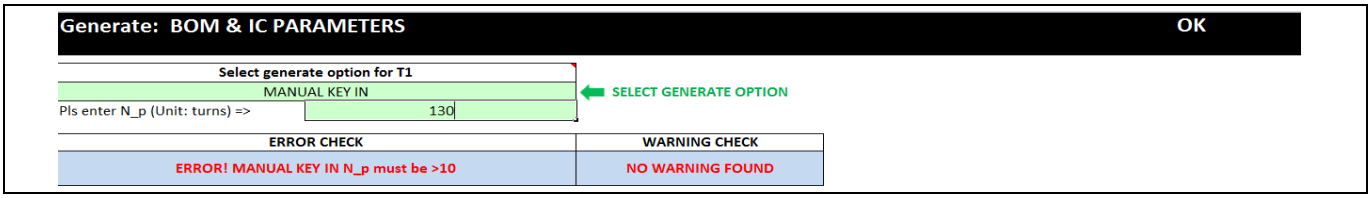


Figure 46 Flyback transformer, T1 parameter-generating option ("MANUAL KEY IN")

Figure 47 shows an example of the generated BOM and IC parameters.

The BOM reference designators are based on the schematic of XDPL8105 Reference Design with CDM10V. For easy reference, the schematic is available in the "SCH" worksheet of the excel tool.

Please note that the primary snubber resistance value shown in the green-highlighted cell for R7 + R8 in the BOM in **Figure 47** is only for an initial design and requires fine-tuning based on the actual MOSFET drain voltage measurement against its maximum rating.

By opening the XDPL8105 parameterization file (*.csv) with the GUI called .dpVision, user can enter the generated IC parameters from the excel tool and burn these parameters into the IC, using the .dp Interface Board Gen 2.

Please note that there are a few IC parameters which could not be calculated but require fine-tuning at system level. These parameters are as shown in the green-highlighted cell in the IC parameters table in **Figure 47**. Please refer to the "XDPL8105 40W Reference Design with CDM10V Application Note" for the fine-tuning guide.

Also, there are some application related IC parameters below which are each generated with an initial default value, instead of dynamically adapted based on the input or output from the design steps before. If necessary, user can adjust each of these following parameter values later in .dpVision according to the application needs.

- Output current dimming curve, *C_DIM*
- Gate driver peak source current, *I_GD_pk*
- Enable output under-voltage protection, *EN_UVP_Vout*
- Enable maximum average output current protection, *EN_Iout_max_avg*
- Enable maximum peak output current protection, *EN_Iout_max_avg*
- Auto restart speed for output current protection, *Speed_OCP_Iout*
- Enable input under-voltage protection, *EN_UVP_In*
- Enable adaptive temperature protection, *EN_ITP*
- Adaptive temperature protection derating time for output current, *t_step*
- Time per soft start step, *t_ss*
- Initial number of pulses in ABM, *N_ABM_init* (if *EN_ABM* is enabled and control loop init is selected as "ABM")
- Control loop parameters, *PI_KP_xxx* and *PI_KI_xxx*

- DIM/UART voltage threshold for minimum output current, *V_DIM_min*
- DIM/UART voltage threshold for dim-to-off and dim-to-on, *V_DIM_off* and *V_DIM_on*
- Power factor enhancement gain parameter, *C_EMI*

Auto-generated BOM

Auto-Generated BOM

Note: Based on sheet "SCH" schematic of 40W Ref Design. EMI Line Filter & Bridge not included in this BOM

Schematic Section	Symbol	Value	Rating	Supplier	Part Number/Package
FB_PRI	T1	Lp: 0.544mH; Np: 58; Ns: 15; Naux: 15; Nsec_aux: 15		WURTH	Core, Bobbin: PQ2020, THT, 14p [V]
	IC3	XDPL8105	-	INFINEON	XDPL8105 (DSO-8)
	Q1	IPD80R1K0CE	800V	INFINEON	DPAK
	D3	≥1A	≥800V	DIODES	RS3MB-13-F(SMB)
	D20, D21	1A	600V	FAIRCHILD	ES1J (SMA)
	C3	6800pF	> 378V	ANY	Film cap
	C4	0.22uF	> 498V	ANY	Film cap
	C5	100pF	50V, COG	ANY	SMD Package: 0603
	R2	20kohm	1%	ANY	SMD Package: 0603
	R4+R5+R6	66kohm	1%	ANY	SMD Package:1206 (3 pcs, in series)
	R7+R8	174.8kohm	≤5%	ANY	Power rating: >0.67W
	R10	56.2kohm	1%	ANY	SMD Package: 1206
	R11	2kohm	1%	ANY	SMD Package: 0603
	R14	0.22ohm	1%	ANY	Power rating: >0.12W
	R16	10ohm	1%	ANY	SMD Package: 0805
AUX VCC SUPPLY	Q2	NPN Transistor	Vceo >60V	ANY	Power rating: >0.72W
	D4	≥0.25A	>242V	ANY	BAV103 (SOD-80C)
	D12	0.25A	≥30V	ANY	BAV102 (SOD-80C)
	ZD1	Zener 15V	≤5%	ANY	SOD-323 or similar
	C6	4.7uF	>60V	ANY	Electrolytic Cap
	C8	15uF	≥25V	ANY	E-Cap or SMD1206
	C38	0.1uF	≥25V	ANY	SMD Package: 0603
	R17	47kohm	1%	ANY	SMD Package: 1206
	R18	4.7ohm	1%	ANY	SMD Package: 1206
DIMMING *Secondary 0-10V dimming with CDM10V*	IC30	Schmitt trig. IC	invert out	TI	SN74LVCG14DBVR
	IC100	CDM10V adapter	-	INFINEON	CDM10V adapter board
	PC1	Optocoupler	>4kV, UL	VISHAY	VO617A-2
	Q100	NPN Transistor	Vceo >57	ANY	SOT-89 or larger
	ZD30	Vz=5.1V at 1mA	≤2.5%	ANY	SOD323 or similar
	D100	0.25A	>242V	ANY	BAV103 (SOD-80C)
	D105	Schottky	low leakage	ANY	MMBD301LT1G(SOT23)
	ZD100	Zener 15V	≤5%	ANY	SOD-323 or similar
	C33	0.68uF	16V	ANY	SMD Package: 0603
	C34	4.7uF	25V	ANY	SMD Package: ≥0805
	C35, C36	0.1uF	≥25V	ANY	SMD Package: 0603
	C102	2.2uF	>60V	ANY	Electrolytic Cap
	C103	10uF	25V	ANY	SMD Package: 1206
	R19	620kohm	1%	ANY	SMD Package: 0603
	R31	2.2kohm	1%	ANY	SMD Package: 0603
	R32	36kohm	1%	ANY	SMD Package: 0603
	R33	5.1kohm	1%	ANY	SMD Package: 0603
	R34	47kohm	1%	ANY	SMD Package: 0603
	R36	18kohm	1%	ANY	SMD Package: 0603
	R37	2.2kohm	1%	ANY	SMD Package: 0805
	R100	4.7ohm	1%	ANY	SMD Package: 1206
	R101	47kohm	1%	ANY	SMD Package: 1206
FB_SEC	D6	> 8.1A	> 237V	ONSEMI	MBRB40250TG
	C7	0.1uF	≥70V	ANY	SMD Package: ≥0805
	C12//C13	940uF	63V	ANY	Electrolytic Cap
	C99	OPEN	-	-	-
	R99	OPEN	-	-	-
OUTPUT BLEEDER *Active (Auto-Discharge Circuit)*	Q3, Q4	2N7002	60V	INFINEON	2N7002 (SOT-23)
	D7	Dual Diode	> 237V	INFNEON	BAT240A (SOT-23)
	D8, D9	OPEN	-	-	-
	ZD4, ZD5	Zener 12V	≤5%	ANY	SOD-323 or similar
	C10	1000pF	> 296V	ANY	Discrete or SMD 1206
	C11	0.1uF	≥25V	ANY	SMD Package: 0603
	R26//R29 //R30	1.3kohm	1%	ANY	Power rating > 1W
	R27, R28	1Mohm	1%	ANY	SMD Package: 0805
	R9	OPEN	-	-	-
Y-CAP	C9	2200pF	≥277Vac	ANY	Safety Ceramic Cap
DEBUG/PROGRAMMING	C31	470p	≥25V, COG	ANY	SMD Package: 0603
	J4	3 pins	-	ANY	3 pins (Vcc, Uart, Gnd)
SAFETY & LINE SURGE *(Fuse is mandatory for your safety!)*	F1	UL safety fuse	>0.98A	ANY	-
	MOV1	surge absorber	UL Safety	ANY	Radial, Disc Type
	D1, D2	surge absorber	>216.3V	ANY	Case Style: 1.5KE
	D10	ESD Diode 12V	low leakage	ANY	-
JUMPERS	R1,R50,R51	0ohm	-	ANY	SMD Package: 0603

Auto-generated IC Parameters

Auto-Generated IC Parameters

for XDPL8105 csv version: Rev1

Hardware configuration		
I_out_set	880.0	mA
N_p	58	turns
N_s	15	turns
N_a	15	turns
L_p	0.5440	mH
R_CS	0.220	ohm
V_OCP1	0.49 ~ 0.51	V
R_ZCD_1	56.2	kohm
R_ZCD_2	2.00	kohm
VCC_SUPPLY	Wide	
C_VCC	15	uF
V_out_cap rating	63	V
R_HV	66	kohm
I_GD_pk	49	mA
Protections		
t_auto_restart	1.0	s
t_auto_restart_fast	0.4	s
Reaction_OVP_Vout	Auto-Restart	
Speed_OVP_Vout	Slow	
V_outOV	48.4	V
EN_UVP_Vout	Enabled	
t_start_max	10.0	ms
EN_Iout_max_avg	Enabled	
EN_Iout_max_peak	Enabled	
I_out_max_peak	1980	mA
Speed_OCP_Iout	Slow	
EN_UVP_In	Enabled	
EN_OVP_In	Enabled	
V_inOV	329.0	V
V_in_start_max	329.0	V
V_in_start_min	72.0	V
V_inUV	62.0	V
Reaction_VCCP	Latch-Mode	
Debug_Mode	Disabled	
Temperature guard		
T_critical	119	°C
EN_ITP	Enabled	
T_hot	110	°C
I_out_red	220	mA
t_step	10	s
Startup & shutdown		
t_ss	0.50	ms
V_out_dim_min	11.9	V
V_out_start	9.5	V
V_start_OCP1	V_OCP1	V
Control_loop_init	DCM	
f_DCM_init	12	kHz
N_ABM_init	100	
Control loop		
PI_KP_QRM	550	
PI_KI_QRM	8	
PI_KI_DCM	17000	
PI_KI_DCM	200	
PI_KP_ABM	64	
PI_KI_ABM	32	
Dimming		
EN_DIM	Enabled	
V_DIM_min	0.2	V
I_out_dim_min	88.0	mA
C_DIM	Quadratic	
EN_DIM_TO_OFF	Disabled	
V_DIM_off	0.18	V
V_DIM_on	0.19	V
EN_SQW	Disabled	
Multimode		
f_sw_max	180.80	kHz
t_on_max	11.3	us
t_on_min	1.1	us
t_min_demag	3.0	us
f_sw_min_DCM	12.0	kHz
EN_ABM	Disabled	
Power Factor Correction		
C_EMI	0.1000	uF
Fine tuning		
t_ZCDPD	410	ns
t_PDC	200	ns
T_coupling	1.020	
R_in	11.90	ohm
N_DCM_mod_gain	8	
a_DIM	0.000	mV/K

PLEASE FINE TUNE BASED ON APP. NOTE

Figure 47 Auto-generated BOM and IC parameters (end of Step 3)

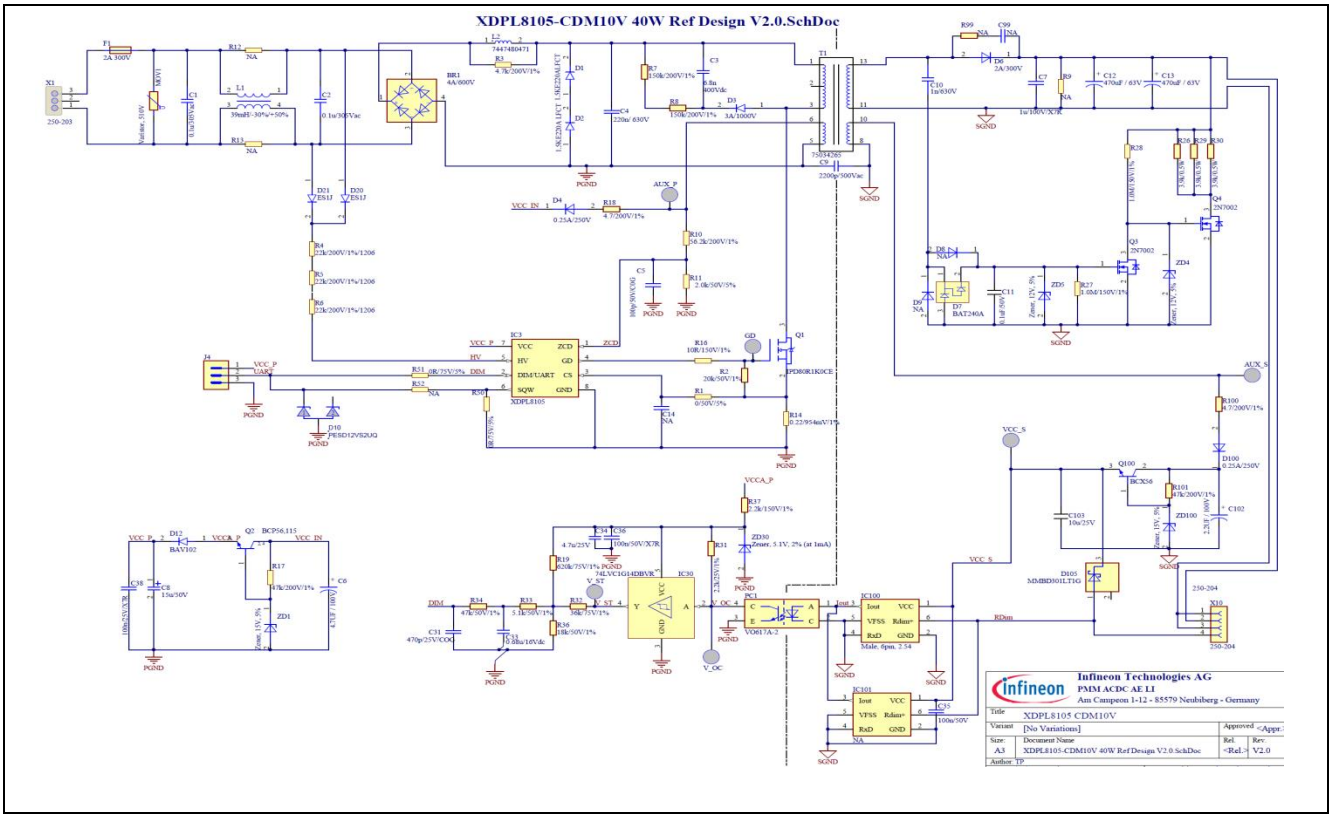


Figure 48 Schematic for the auto-generated BOM (Refer "SCH" Worksheet in the excel tool)

Revision History

Major changes since the last revision

Page or Reference	Description of change

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