

XDPS2221E System Design Guide
- Design tool V1.0.0

Dr. Jing Hu

Overview

- Introduction
  - Application schematic with CoolMOS™ and CoolGaN™
  - XDPS2221E operating principle of PFC and HFB
  - Design flow

- System design guide
  - Excel design tool
  - System level
    - Input and output specification
    - Design assumption
    - R_{HV}
    - MFIO functionality and parameters
  - PFC stage
    - Main components, ZCDCS circuit, PFCVS divider
    - Bus voltage setting via $k_{VcrVbusT}$ and its impact
  - Hybrid flyback (HFB) stage
    - Main components, ZCD circuit, CS circuit, PFCVS divider, VCC supply circuit
    - Construction of the transformer

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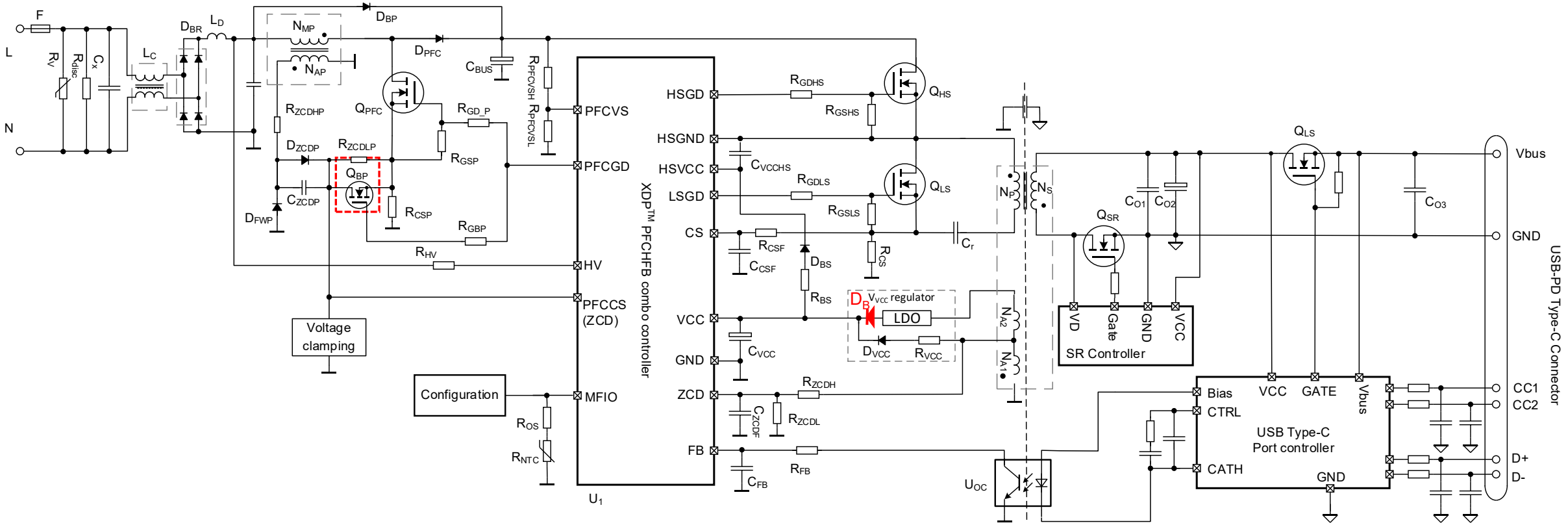
Introduction
- Application with CoolMOS™ switches



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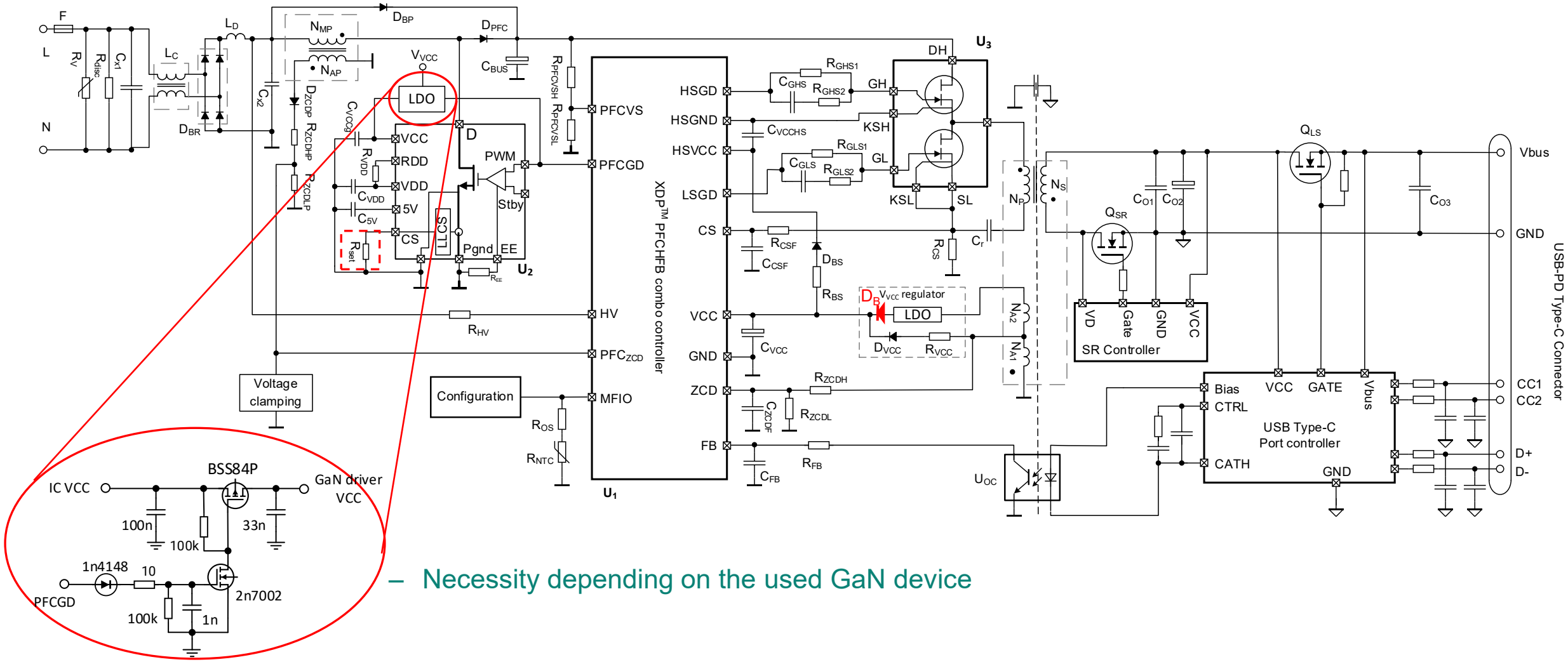
Introduction
- Application with CoolGaN™ switches



– Necessity depending on the used GaN device

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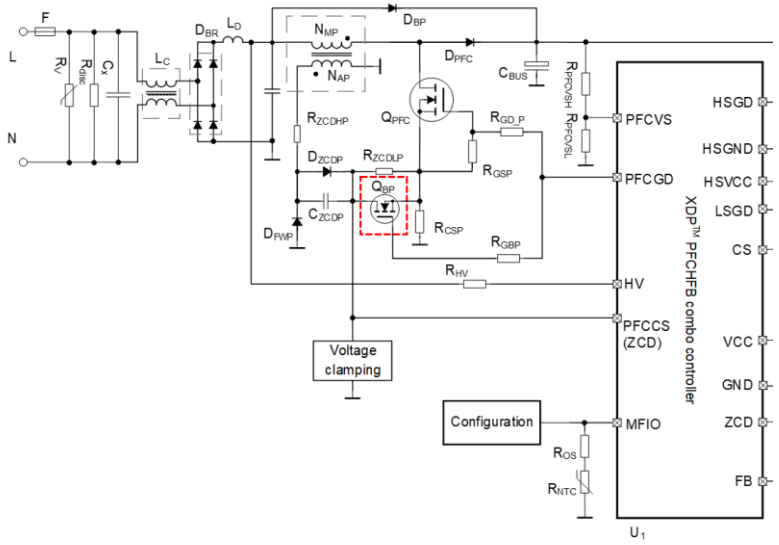
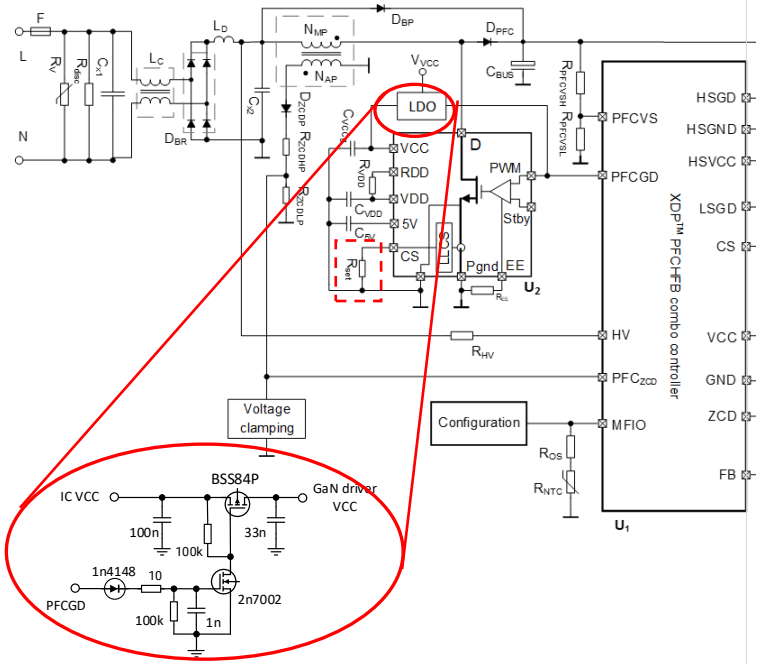
Introduction
- PFC operating principle

– Typical application circuit
  – PFC switch **without** OCP

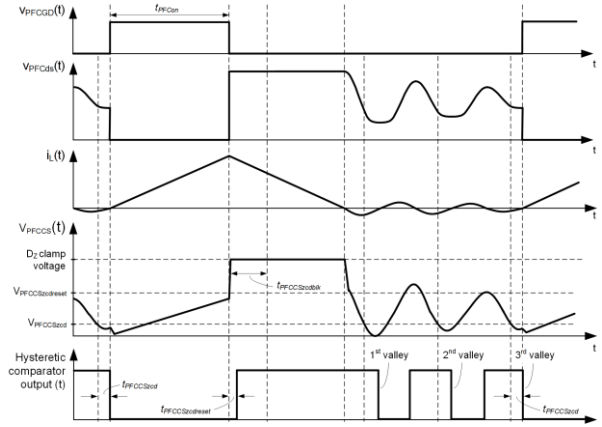


– PFC switch **with** OCP

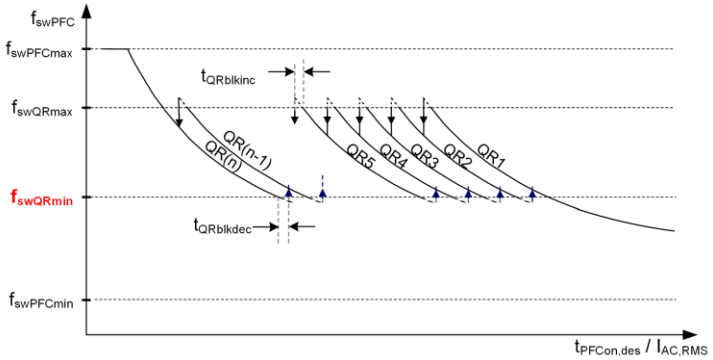


– Lossless current sensing inside the PFC switch

– QRM valley switching boost converter
  – Valley 1 to **N_PFC_valley_max**



  – Switching frequency limitation



XDPS2221E supporting CCM protection with both types of the PFC switches

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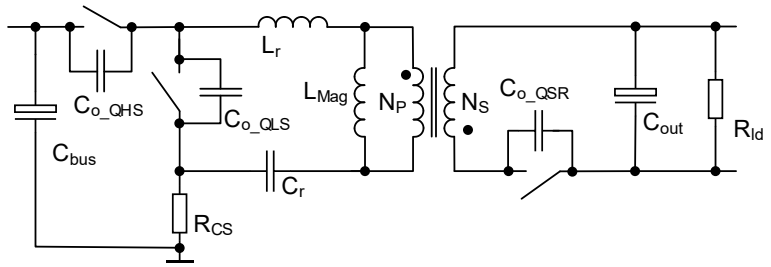
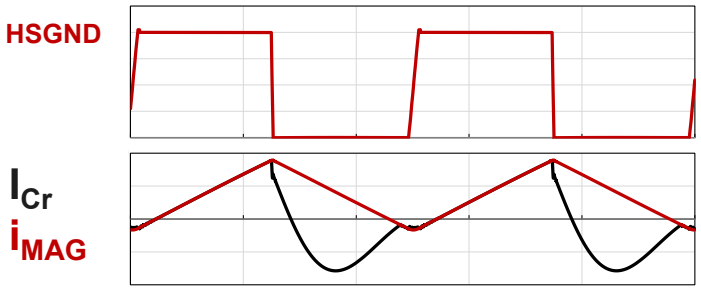
Introduction
- HFB operating principle

– **Circuit**

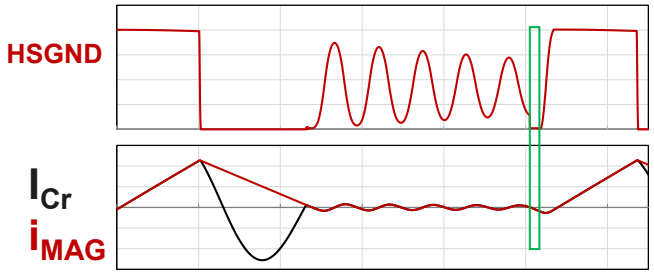


– **Operating principle**
  – Peak current control with fast response
  – Valley switching with ZVS operation for good efficiency
  – Linear increasing primary current during HS on-time and resonant current during LS on-time LS on-time

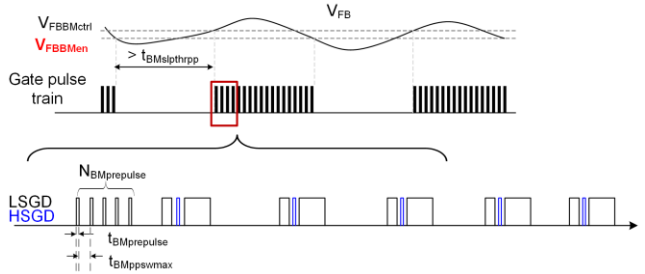
– **Non-burst operation**
  – Continuous Resonant Mode (**CRM**) at high load condition



  – Zero Voltage – Resonant Voltage Switching (**ZV-RVS**) at low and lighter load condition, with ZVS pulse for ZV turn-on of the HS switch



– **Burst mode operation**
  – Burst on- and off-phase based on the HFB V_{FB}



  – PFC operation depends on
    – Bus target voltage
    – Actual bus voltage
    – AC input voltage
    – Output power

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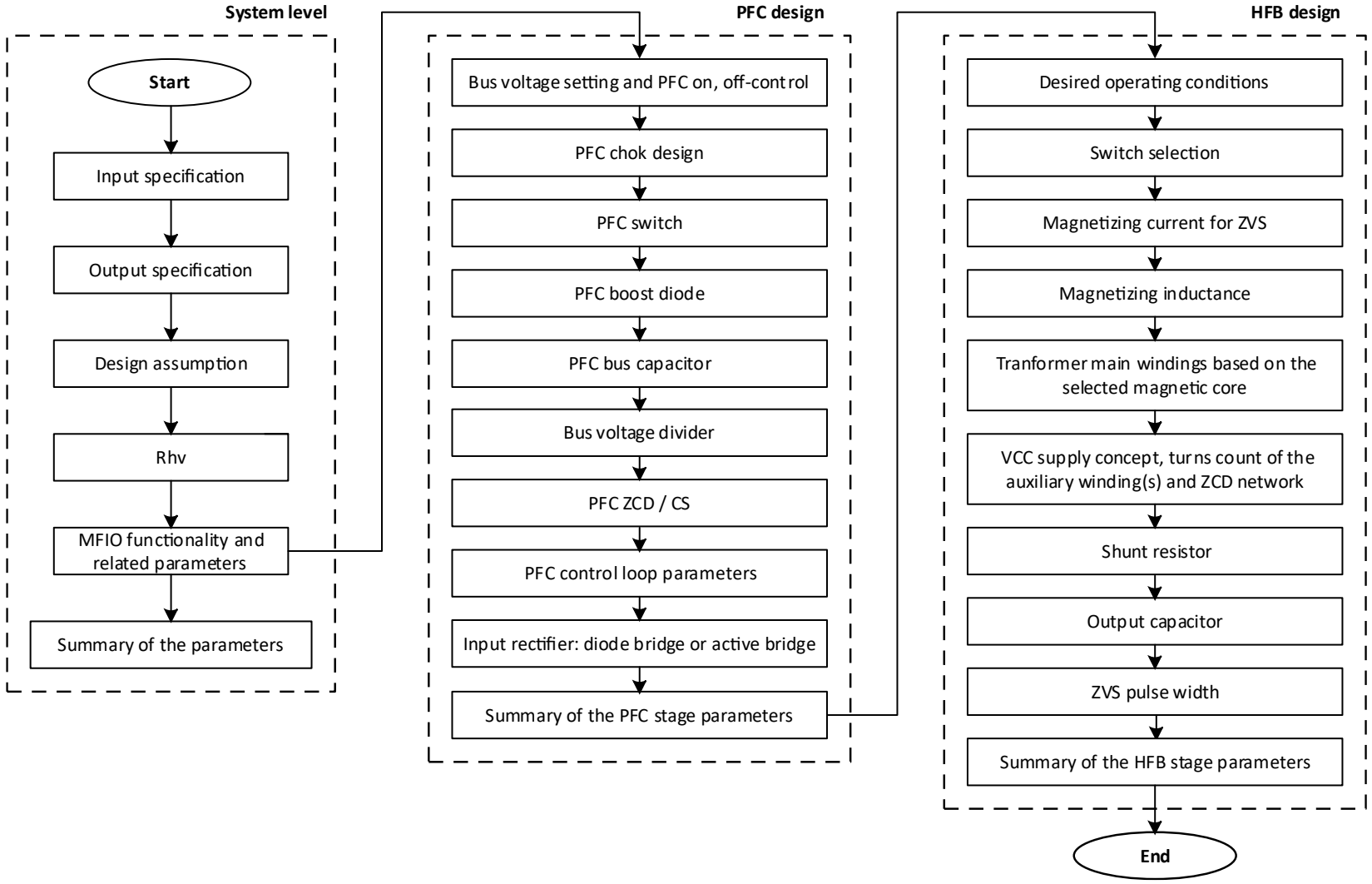
Design flow



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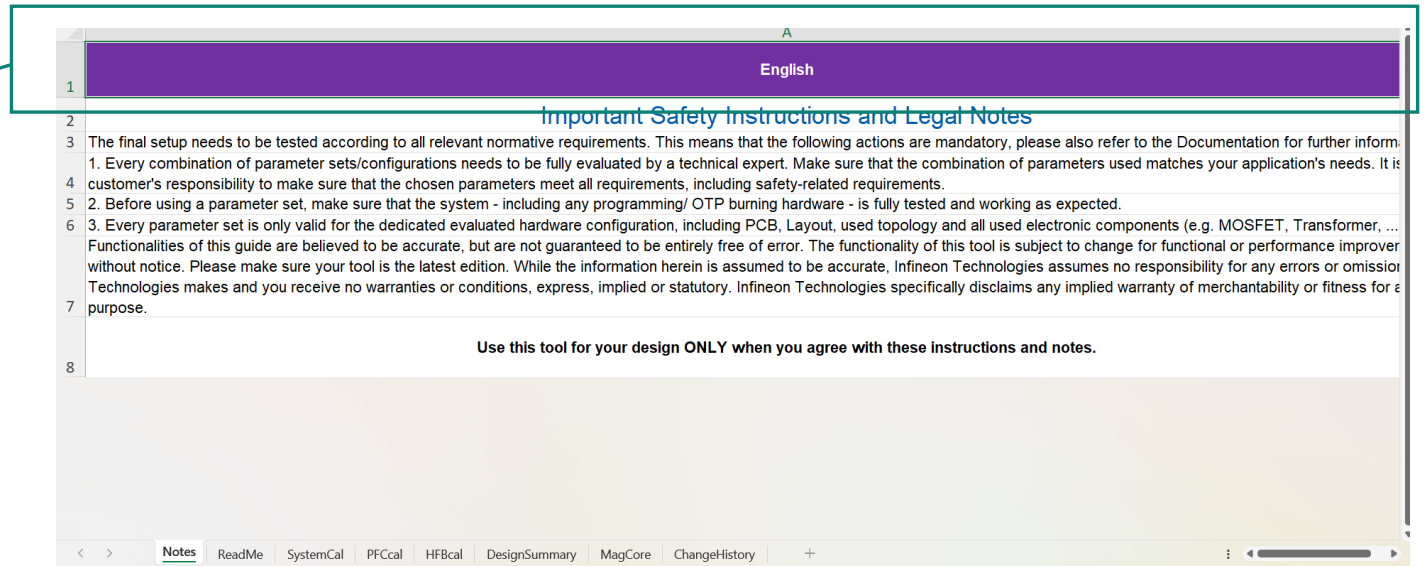
Excel design tool
- Overview

- Microsoft Excel version **2013** or later required
- Design workbook structure
- Sheet overview and color index
- Design steps
- GUI supported language
  - English and Chinese
  - Selectable per A1 on the page Notes



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Excel design tool
- Structure

Important notes

How to use the design sheet

Ferrite core parameters

Notes | ReadMe | SystemCal | PFCcal | HFBcal | DesignSummary | MagCore | ChangeHistory

Main calculation

		Design #	Design1			
	Design steps	Parameter	Value typ.	Value min.	Value max.	Unit
1	Input specification					
	AC input minimum	VacMin	90			V
	AC input low line	VacLL	115			V
	AC input high line	VacHL	230			V

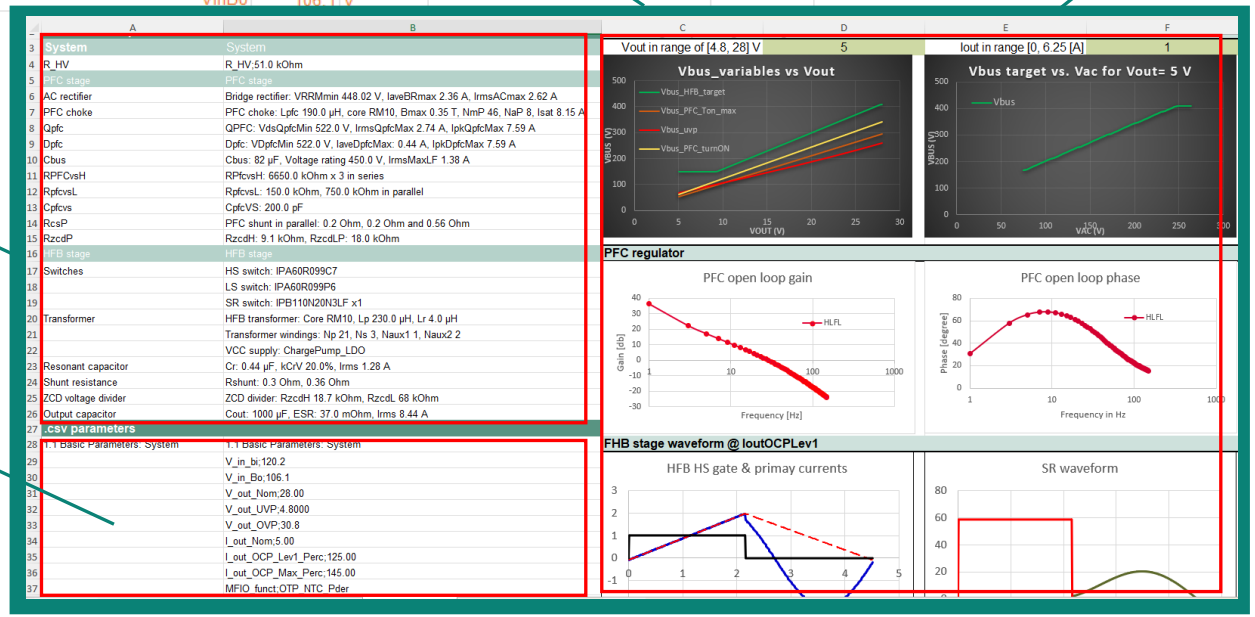
Assistant calculation, design recommendation and information

ADC_VS_RRANGE	2.751 V	ADC_MFIO2_RANGE	2.428 V
ADC_Vzcd_RANGE_THR_MAX	2.75 V	DAC_RANGE	0.437 V
ADC_MFIO2_RANGE_THR_MAX	2.33 V		
VinBi	120.2 V		
VinBo	106.1 V		

Illustration curves

Components

Parameters



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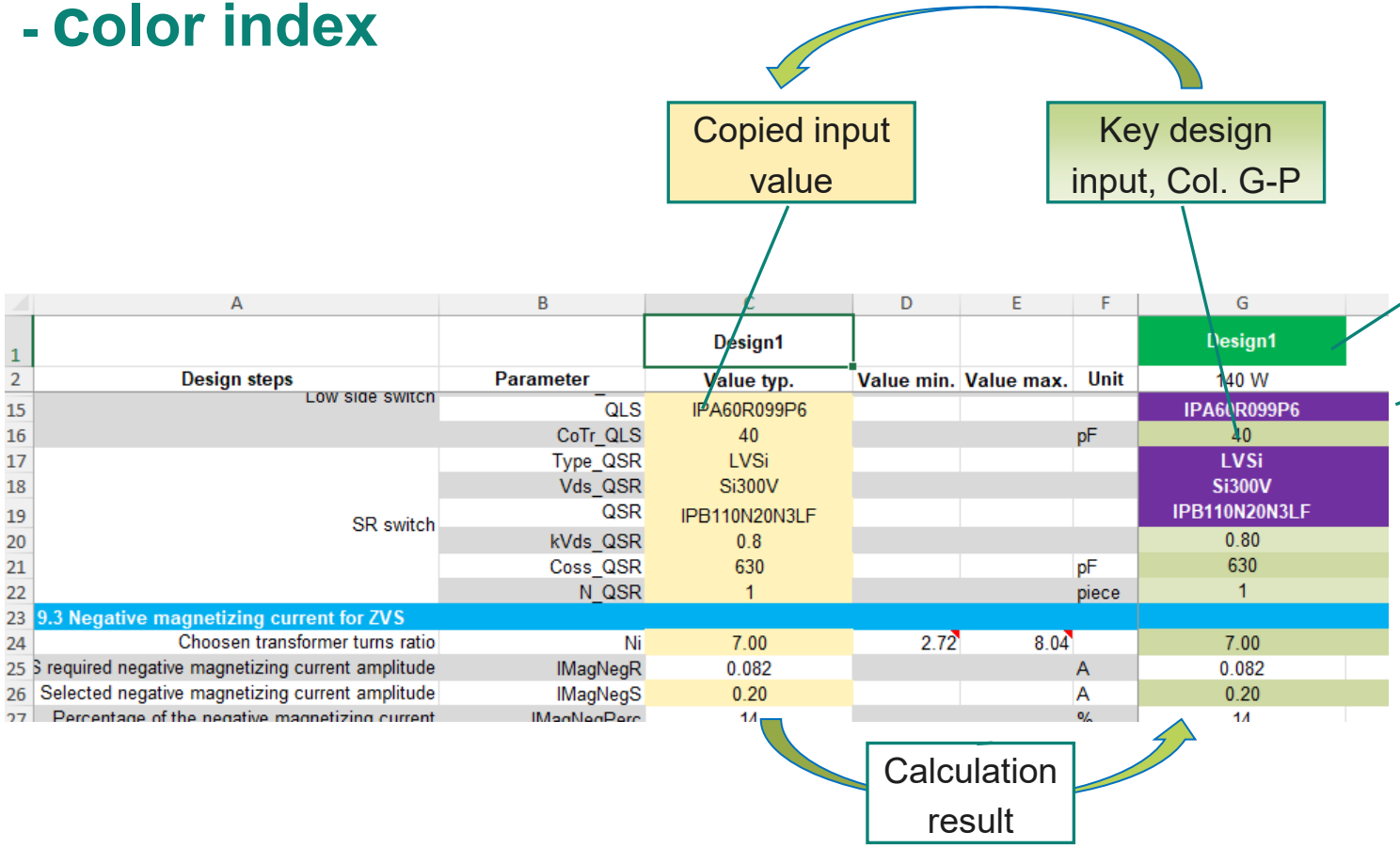
Excel design tool
- Color index



	A	B	C	D	E	F	G
1			Design1				Design1
2	Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	140 W
15	Low side switch	QLS	IPA60R099P6				IPA60R099P6
16		CoTr_QLS	40			pF	40
17		Type_QSR	LVSi				LVSi
18		Vds_QSR	Si300V				Si300V
19	SR switch	QSR	IPB110N20N3LF				IPB110N20N3LF
20		kVds_QSR	0.8				0.80
21		Coss_QSR	630			pF	630
22		N_QSR	1			piece	1
23	9.3 Negative magnetizing current for ZVS						
24	Choosen transformer turns ratio	Ni	7.00	2.72	8.04		7.00
25	S required negative magnetizing current amplitude	IMagNegR	0.082			A	0.082
26	Selected negative magnetizing current amplitude	IMagNegS	0.20			A	0.20
27	Percentage of the negative magnetizing current	IMagNegPerc	14			%	14

csv parameter info | Assistant calculation | Modifiable recommendation | DS info

Q	R	S	T	U	V
Assistant information					
PoutFL	140.00	W	PinVacHLFL	148.15	W
PinVacMaxloutOcp1	183.25	W	PinVacLLFL	152.17	W
PoutOcp1	175.00	W	IbusOcp1	0.44	A
PinVacBoloutOcp1	194.44	W	IrmsVacBoloutOCp1	2.62	A
Rhv	51.0	kOhm	VVCConMax	22	V
			IHVMinAvg	1	mA
			IHVmax	9.6	mA
ACT_EN	OTP_NTC	OTP_NTC_	VoutTog		

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Excel design tool
- Design sheets and steps

- Sheet SystemCal
  - Select the specific design at the cell C1
  - Selected design valid through the sheets SystemCal, PFCcal and HFBcal, and highlighted on the first row
  - System level design
- Sheet PFCcal
  - PFC stage design
- Sheet HFBcal
  - HFB stage design
- Sheet MagCore
  - Ferrite core information
  - Extendable for customized core, the values in column B to D are mandatory
- Sheet DesignSummary
  - Hardware components in cells B3:B26, which can be copied to a text editor and saved for other purpose;
  - csv parameters in cells B28:B72, which can be copied to a text editor, saved and imported by dp vision 2.1.3.3 or later version
- Design steps on the same page
  - Top-down, otherwise any missing input may cause Excel calculation error, such as divided by zero.

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System level design guide
- Overview

- Input and output specification
  - AC input
    - Voltage range and frequency
  - HFB output
    - Output voltage level(s)
    - Output current levels
- Design assumption
  - System efficiency
  - HFB efficiency
  - Power factor
- Design
  - R_{hv}
  - MFIO functionality and the related parameter

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System level design guide
- Input and output specification

- Design specification
  - AC input
    - Voltage range and frequency
    - HFB input brown-in and –out voltage calculated based on the peak value of V_{acBi} and V_{acBo}

      i.e.: $V_{inBi} = \sqrt{2} * V_{acBi}$

VinBi	120.208	V
VinBo	106.066	V

  - HFB output
    - Output voltage level(s)
    - Output current levels
    - Min and max limit coming from
      - Physical meaning, i.e.: $V_{outOVPmin}$
      - csv file setting, i.e.: $I_{outOCPLev1Perc}$ or $I_{outOCPMaxPerc}$
    - Further calculation
      - VoutVzcdRatio $VoutVzcdRatio = \frac{V_{outOVP}}{V_{zcdOVP2}}$
      - Nominal output power $P_{outNom} = I_{outNom} * V_{outNom}$

Design steps	Design # Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
1 Input specification						
AC input minimum	VacMin	90			V	90
AC input low line	VacLL	115			V	115
AC input high line	VacHL	230			V	230
AC input maximum	VacMax	264			V	264
AC brown-in level	VacBi	85			V	85
AC brown-out level	VacBo	75		85	V	75
Line frequency minimum	facMin	47			Hz	47
2 HFB output specification						
Nominal output voltage maximum	VoutNom	28.00	0		V	28.00
Output under voltage level	VoutUVP	3.50			V	3.50
Output over voltage level	VoutOVP	30.80	28		V	30.80
Nominal output current	IoutNom	5.00	0.001		A	5.00
Output lower overcurrent protection threshold	IoutOCPLev1Perc	125	100	145	%	125.0
Output maximum overcurrent protection threshold	IoutOCPMaxPerc	145	125	200	%	145.0

VoutVzcdRatio	11.200	
PoutNom	140	W

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System level design guide
- Design assumption

- Design assumption
  - System efficiency
  - HFB efficiency
  - Power factor

Design steps	Design # Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
3 Design assumption						
Power factor at low line and nominal load	PF	0.99				0.99
System efficiency at max line and nominal load	EtaSysVacMax	95.5%				95.5%
System efficiency at high line and nominal load	EtaSysVacHL	94.5%				94.5%
System efficiency at low line and nominal load	EtaSysVacLL	92.0%				92.0%
System efficiency at VacBo and IoutOCPLev1	EtaSysVacBo	90.0%				90.0%
HFB efficiency at the nominal condition	EtaHFB	98.0%				98.0%

- Further calculation
  - Output power at full load

    $P_{outFL} = I_{outNom} * V_{OutNom}$
  - Output power at $I_{outOCPLev1}$

    $P_{outOcpL1} = I_{outNom} * \frac{I_{outOCPLev1Perc}}{100} * V_{outNom}$
  - Input power at different conditions, such as
    - At AC **l**ow **l**ine and **f**ull **l**oad

      $P_{inVacLLFL} = \frac{P_{outFLNom}}{Eta_{SysVacLL}}$
    - At V_{acMax} and $I_{outOcpL1}$

      $P_{inVacMaxOCP1} = \frac{P_{outOcpL1}}{Eta_{SysVacMax}}$

PoutFL	140.00	W	PinVacHLFL	148.15	W
PinVacMaxIoutOcpL1	183.25	W	PinVacLLFL	152.17	W
PoutOcpL1	175.00	W	IbusOcpL1	0.44	A
PinVacLLOcpL1	190.22	W	PinVacBoFL	155.56	W
PinVacBoOcpL1	194.44	W	IrmsVacBoIoutOcpL1	2.62	A

    - Bus output current at V_{acBo} and $I_{outOCPLev1}$

      $I_{busOCP1} = \frac{P_{outOcpL1}}{Eta_{HFB} * V_{busDsgn}}$ $V_{busDsgn}$ the initial value for the HBF design
    - Input AC rms current at V_{acBo} and $I_{outOCPLev1}$

      $I_{rmsVacBoIoutOCP1} = \frac{P_{outOcpL1}}{Eta_{sysVacBo} * V_{acBo} * PF}$

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System level design guide
- R_{hv}

- Functionality of the resistor at the HV pin R_{hv}
  - VCC capacitor initial charge-up
  - Limiting the maximum current flowing into the HV pin
  - Reducing the thermal stress of the start-up cell

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
4 Rhv					kOhm	
	Rhv1	27.0			kOhm	27
	Rhv2	24.0	49.8	52.5	kOhm	24
	Rhv3	0.0			kOhm	

- Limits of the R_{hv}
  - Minimum value
    - For limiting current at maximum line voltage

$$R_{hvMin} = \frac{\sqrt{2} * V_{acMax}}{I_{hvMax}}$$ with I_{hvMax} at 9.6 mA

  - Maximum value
    - Offering enough charging current for the VCC capacitor

$$R_{hvMax} = MIN\left\{10^5, \frac{V_{acMinRecAvg} - V_{vccOnMax}}{I_{hvMinAvg}} * \left[1 - \frac{2}{\pi} * \sin^{-1}\left(\frac{V_{vccOnMax}}{V_{acMinPk}}\right)\right]\right\}$$

with $I_{hvMinAvg}$ at 1 mA and $V_{acMinRecAvg}$ of 0.9*V_{acMin}

Design_guide_lighting_ICs_XDPL8219_XDP_digital_power-ApplicationNotes-v01_00-EN.pdf

- To be considered
  - Two or three resistors in series
  - Voltage rating of the resistors
  - Recommended to be connected after the AC bridge rectifier
  - One small capacitor, i.e. 100 pF, at the HV pin to reduce the voltage stress at the pin at lightning surge

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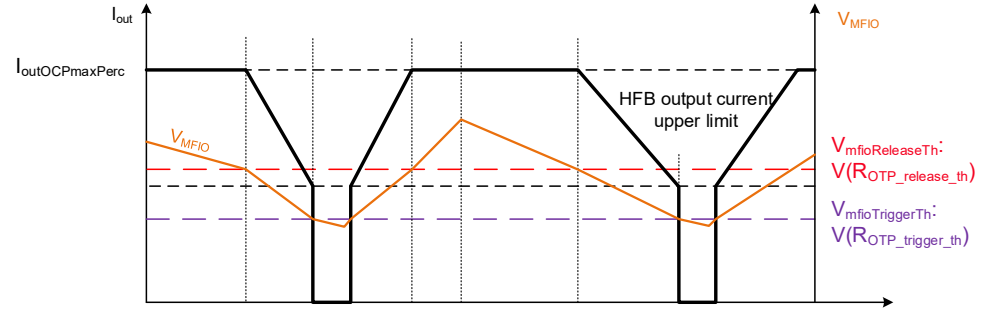
System level design guide
- MFIO pin functionality

- Multi-functionality integrated with this pin
  - ACT_EN
    - Toggling depending on IC state of **burst sleep or not**
    - Use case: to control the active bridge
  - OTP_NTC
    - Using **external NTC** for overtemperature protection
  - OTP_NTC_Pder
    - Using **external NTC** for overtemperature protection and temperature dependent **power foldback**
  - Vout_Tog
    - Toggling depending on **output voltage level**
- Pin internal setting and related parameters
  - Some internal setting depending on the selected functionality
  - Only the configured functionality active

Design steps	Design # Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
5 MFIO function						
	MFIO_funct	ACT_EN				ACT_EN

Power foldback during OTP restart



	Remark	MFIO _func			
Options		ACT_EN	OTP_NTC	VoutTog	OTP_NTC_Pder
Inner supply		VDDP	VREF	VDDP	VREF
Vout	Vout below V_out_MFIO_goL			Low	
	Vout above V_out_MFIO_goH			PU=2.25K	
Operation	Not BM sleep	High	PU=11K		PU=11K
	BM sleep	High-Z	High-Z	High-Z (Case A) PU=2.25K (Case B)	High-Z
OCP	Iset OCP Max	Enabled	Enabled	Enabled	Power foldback
	Iset OCP Lev1	Enabled	Enabled	Enabled	Disabled
Parameters			$R_{MFIO_OTPtrig}$	$V_{out_MFIOgoL}$	$R_{MFIO_OTPtrig}$
			R_{MFIO_OTPrel}	$V_{out_MFIOgoH}$	R_{MFIO_OTPrel}
			$N_{OTPevMax}$		$N_{OTPevMax}$

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PFC design guide
- Overview

- PFC design following the rules for conventional valley-switching (or quasi-resonant mode - QRM) PFC

- Bus voltage setting and PFC on-, off-control

- PFC stage components
  - Choke design L_{PFC}
  - Switch Q_{PFC} and boost diode D_{PFC}
  - Bus capacitor C_{bus}
  - Bus voltage divider R_{PFCvsH}, R_{PFCvsL}
  - PFCZCDCS network
    - PFC switch with current limitation
    - PFC switching without current limitation

- AC rectifier
  - Voltage and current rating

- Control loop and parameters

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PFC design guide
- Bus voltage setting and PFC on-, off-control

- Defining the bus capacitor voltage rating
- Bus voltage divider ratio calculated
  - $k_{PFCvs} = {}^{V_{busCapRvMin}}/_{V_{VpfcvsOVP2Typ}}$ while its min and max calculated by
    - $k_{PFCvsMin} = {}^{V_{busCapRvMin}}/_{V_{VpfcvsOVP2Max}}$
    - $k_{PFCvsMax} = {}^{V_{busCapRvMin}}/_{V_{VpfcvsOVP2Min}}$
- Min and max of the bus OVP levels calculated based on the set V_{busOVP}
  - $V_{busOVPMin} = V_{busOVP} * V_{PFCVSovp2Min}/V_{PFCVSovp2Typ}$
  - $V_{busOVPMax} = V_{busOVP} * V_{PFCVSovp2Max}/V_{PFCVSovp2Typ}$
- $V_{busTargetMax}$ limited up to V_{busOVP}
- Min and max for the $V_{busTargetMin}$
  - $V_{busTargetMinMin} = 1.1 * V_{inBo}$
  - $V_{busTargetMinMax} = V_{busTargetMax} - V_{busTargetVoffset}$

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
6 Bus voltage setting and PFC on-, off-control						
Bus capacitor voltage rating	VbusCapRvMin	450.00	410.7		V	450.00
Divider ratio (RvsH+RvsL)/RvsL	kPFCvs	160.71	155.17	166.67		160.71
Bus OVP level	VbusOvp	435.00	419.46	450.54	V	435.00
Target bus voltage maximum	VbusTargetMax	410.00	392.02	435	V	410.00
Target bus voltage minimum	VbusTargetMin	150.00	117	390	V	150.00
Additional PFC stage control	P_PFC_enable	60.0			W	60.0
	P_PFC_disable	45.0		60	W	45.0
	V_bus_PFCstop	430.0	410.0	435.0	V	430.0
	V_bus_PFCresume	410.0	150.0	430.0	V	410.0

VPFCVSovp2Max	2.9	V	VPFCVSovp2Min	2.7	V
VPFCVSovp2Typ	2.8	V			

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PFC design guide
- Bus voltage setting and PFC on-, off-control (cnt‘)

- The real bus voltage
  - Required bus voltage from the **HFB** stage determined by $k_{VcrVbusT}$

kVcrVbusT	**1.75**	**2**
VbusTargetHFB	min(1.75*Vcr + Vbus_target_V_offset; Vbus_target_max)	min(2 *Vcr + Vbus_target_V_offset; Vbus_target_max)
VbusPFCon	1.75 *Vcr	1.75 *Vcr
VbusPFCtonMax	min(1.25*Vcr, Vbus_max_PFC_Ton_max)	min(1.5 *Vcr, Vbus_max_PFC_Ton_max)
kVcrVbusT	**2.25**	**2.5**
VbusTargetHFB	min(2.25 *Vcr + Vbus_target_V_offset; Vbus_target_max)	min(2.5 *Vcr + Vbus_target_V_offset; Vbus_target_max)
VbusPFCon	2 *Vcr	2 *Vcr
VbusPFCtonMax	min(1.75 *Vcr, Vbus_max_PFC_Ton_max)	min(2 *Vcr, Vbus_max_PFC_Ton_max)

    - Additional influence of $k_{VcrVbusT}$ on bus voltage level
      - To turn on PFC
      - To operate PFC with the maximum on-time
  - Required bus voltage from the **PFC** stage
    - If the PFC stage is enabled
      - $V_{BusTargetPFC} = V_{acPk} + V_{busTargetAcPkOffset}$
  - **Final bus target voltage**
    - $V_{busTarget} = Min\{Max[V_{busTargetMin}, V_{busTargetHFB}, V_{busTargetPFC}], V_{busTargetMax}\}$

- $k_{VcrVbusT}$ determination
  - Lower value resulting in low bus voltage level and beneficial for system efficiency
  - Based on the designed the HFB transformer turns ratio N
  - Bus voltage @ nominal load condition $V_{busDsgn}$ usually limited by the $V_{busTargetMax}$

VbusDsgn	410.0	V

  - The lowest value from [1.75, 2.0, 2,25, 2,5] selected for $k_{VcrVbusT}$, which gives the lowest target bus voltage from the HFB stage based on N and V_{outNom}, but higher than the $V_{busTargetMax}$

		V_bus_target_V_offset		20	V
kVcrVbusT_options	1.75	2	2.25	2.5	
kVcrVbusT	2				
VbusTargetHFB	363	412	461	510	
VbusDsgn	410.0	V			

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PFC design guide
- Bus voltage setting and PFC on-, off-control (cnt‘)

- PFC on-, off-control
  - PFC operation depending on many factors
    - Input AC voltage comparing to the required bus voltage from the HFB stage
    - HFB output power: $P_{PFCenable}$, $P_{PFCdisable}$
  - $P_{PFCenable}$, $P_{PFCdisable}$
    - Estimated average output power based on the output current indirectly via V_{FB} and the output voltage level
    - Pulse load resulting in lower averaged power than the real peak power
    - Practically, it is valid $P_{PFCenable} > P_{PFCdisable}$

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	120 W 3C evaB
6 Bus voltage setting and PFC on-, off-control						
Bus capacitor voltage rating	VbusCapRvMin	450.00	410.7		V	450.00
Divider ratio (RvsH+RvsL)/RvsL	kPFCvs	160.71	155.17	166.67		160.71
Bus OVP level	VbusOvp	435.00	419.46	450.54	V	435.00
Target bus voltage maximum	VbusTargetMax	410.00	392.02	435	V	410.00
Target bus voltage minimum	VbusTargetMin	150.00	117	390	V	150.00
Additional PFC stage control	P_PFC_enable	60.0			W	60.0
	P_PFC_disable	45.0		60	W	45.0
	V_bus_PFCstop	430.0	410.0	435.0	V	430.0
	V_bus_PFCresume	410.0	150.0	430.0	V	410.0

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PFC design guide
- PFC stage components: PFC choke

- Set the minimum of the PFC switching frequency f_{swMin}

Design steps	Design # / Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
7 PFC design						
7.1 Choke design						
PFC switching frequency minimum	fswMin	56.00			kHz	56.00
PFC choke inductance design value	LPfc	180.00		191	µH	180.00
Oscillation period of the PFC Vds	Tosc_P	0.88			µs	0.880
PFC tonMax with impact of valley switching	tPfcOnMax	12.76			µs	12.76
switchign frequency at VacBo peak and IoutOCP1	fswAcBoPkOCP1	56.64			kHz	56.64
Core selected	Core_P	RM10				RM10
Core flux maximum	Bmax_P	0.35			T	0.35
Turns count of the PFC choke main winding	NM_p	46	24.80			46
Turns count of the PFC choke auxiliary winding	NA_P	8	2.28			8
Choke RMS current maximum over AC cycle	IrmsLPFCmax	3.02			A	3.02

LPFCmaxVacBofPFCmin	191	µH	LPFCmaxVacMaxfPFCmin	304	
TonMaxBCM	13.1	µs	tpfcOffAcBoOCP1	5.14	µs
IpkLpfcMaxBCM	7.41	A	IsatLpfcBCM	8.15	A
Ae_PFC	98				
NM_P_Min	45.1				
kvPFCzcd	1.50		VPFCCSzcdresetMax	1.65	V
N_P_max	6.52				

- Required PFC choke inductance
  - Formula for the maximum of the L_{PFC}
    - $L_{PFC} = \frac{V_{ac}^2 * (V_{busDsgn} - \sqrt{2} * V_{ac})}{2 * f_{swMin} * V_{busDsgn} * P_{inVac}}$
  - Load to be considered
    - $I_{outOCPLev1}$, or
    - I_{outNom}
  - Input voltage
    - V_{acBo} or V_{acLL}
    - V_{acMax}
  - Minimum of the combinations
- T_{osc_P}: Period of the PFC oscillation after the Q_{PFC} turn-off
  - $t_{PFConMax}$ with impact of the T_{osc_P}
    - $t_{onMaxBCM} = \frac{2 * P_{inVacBoIoutOCP1}}{V_{acBo}^2 * L_{PFC}}$
    - $t_{pfcOnMax} = t_{onMaxBCM} * \frac{1 + \sqrt{1 + 4 * \left(1 - {}^{\sqrt{2} V_{acBo}}/_{V_{busDsgn}}\right)^{* \, {}^{0.5 * T_{oscP}}/_{T_{onMaxBCM}}}}}{2}$
  - $f_{swAcBoPkOcpL1}$: the realized lowest switching frequency
    - $f_{swACBoPkOCP1} = {}^{1}/_{(t_{pfcOnMax} + t_{pfcOffAcBoOCP1})}$ with
    - $t_{pfcOffAcBoOCP1} = t_{pfcOnMax} * {}^{\sqrt{2} * V_{acBo}}/_{(V_{busDsgn} - \sqrt{2} * V_{acBo})} + {}^{T_{osc_P}}/_{2}$

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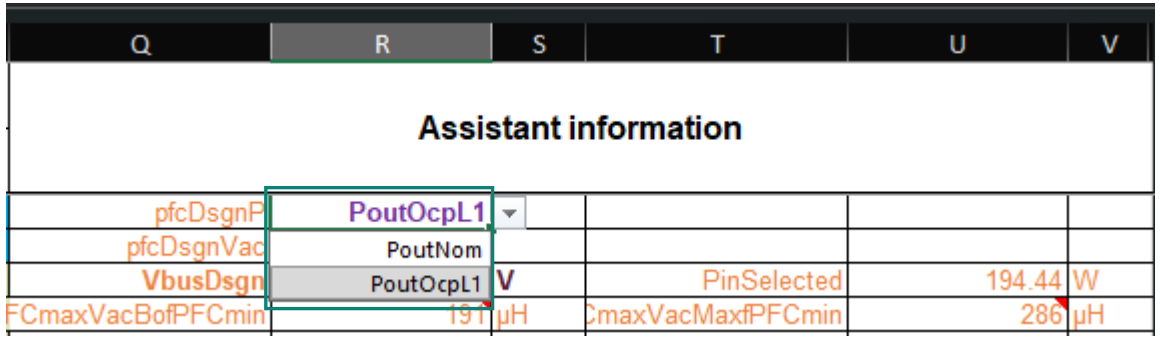
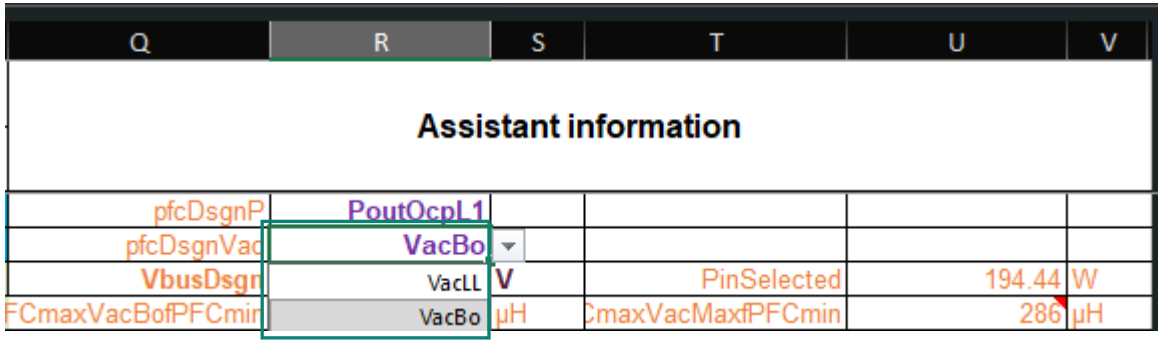
PFC design guide
- PFC stage components: PFC choke

- PFC optimization options
  - Depending on the application, mainly lighting vs. USB PD





- Different requirements from different applications
  - Higher requirement of lighting than USB PD application
    - THD class C in lighting vs. class D in USB PD application
    - THD requirement valid over wider input voltage range
  - High power density of USB PD application
- PFC stage optimized with different criterion
  - pfcDsgnP for the power level
    - P_{outNom}, or
    - $P_{outOcpL1}$
  - pfcDsgnVac for the input voltage level
    - VacBo: sinus input current till input voltage of Vac brown-out level, or
    - VacLL: sinus input current till Vac low line
  - Having impact on the maximum peak current and RMS current for the power devices of the PFC stage and therefore their size and operating temperature over the whole operating range

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PFC design guide
- PFC stage components: PFC choke

- Minimum of the PFC choke main winding turns count N_{M_P} calculated
  - based on the selected
    - PFC core shape Core_p and its A_{e_P}
    - B_{max_P}
  - Limited by $N_{M_{Pmin}} = \frac{L_{PFC} * I_{satLpfc}}{B_{max_P} * A_{e_P}}$ with
    - $I_{satLPFCBCM} = 1.1 * I_{pkLpfcMaxBCM}$ and
    - $I_{pkLpfcMaxBCM} = 2\sqrt{2} * \frac{P_{outOcpL1}}{Eta_{sysVacBo} * V_{acBo} * PF}$
    - Low turns count enabling thicker wire to reduce the DC resistance
- Turns count of the auxiliary winding
  - Minimum of the auxiliary winding turns count
    - Required to ensure proper ZCD at peak of the maximum input voltage
    - defined by
      - $N_{APmin} = {}^{N_{M_P}}/_{N_{pmax}}$ with
      - $N_{Pmax} = \frac{0.95 * V_{busDsgn} - \sqrt{2} * V_{acMax}}{V_{PFCCSzcdResetMax} * k_{vPFCzcd}}$ as the maximum of the PFC choke turns ratio
      - $k_{vPFCzcd}$: a design factor (1.5) to ensure high enough amplitude of the ZCD signal at the peak of the maximum input voltage

Design steps	Design # Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
7 PFC design						
7.1 Choke design						
PFC switching frequency minimum	fswMin	56.00			kHz	56.00
PFC choke inductance design value	LPfc	180.00		191	µH	180.00
Oscillation period of the PFC Vds	Tosc_P	0.88			µs	0.880
PFC tonMax with impact of valley switching	tPfcOnMax	12.76			µs	12.76
switchign frequency at VacBo peak and IoutOCP1	fswAcBoPkOCP1	56.64			kHz	56.64
Core selected	Core_P	RM10				RM10
Core flux maximum	Bmax_P	0.35			T	0.35
Turns count of the PFC choke main winding	NM_p	46	24.80			46
Turns count of the PFC choke auxiliary winding	NA_P	8	2.28			8
Choke RMS current maximum over AC cycle	IrmsLPFCmax	3.02			A	3.02

LPFCmaxVacBofPFCmin	191	µH	axVacMaxfPFCmin	304	
TonMaxBCM	13.1	µs	tpfcOffAcBoOCP1	5.14	µs
IpkLpfcMaxBCM	7.41	A	IsatLpfcBCM	8.15	A
Ae_PFC	98				
NM_P_Min	45.1				
kvPFCzcd	1.20		VPFCCSzcdresetMax	1.65	V
N_P_max	8.16				

Choke rms current maximum $I_{rmsLPFCMax}$

- $I_{rmsLpfcMax} = \frac{2}{\sqrt{3}} * I_{rmsVacBoIoutOcpL1}$ with $I_{rmsVacBoIoutOcpL1}$ as the input AC rms current at
  - V_{acBo}
  - V_{outNom} and I_{out} defined by $I_{outOCPLev1Perc}$

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PFC design guide
- PFC stage components: PFC switch and boost diode

- PFC switch
  - Voltage rating minimum
    - $V_{dsMinQpfc} = 1.2 * V_{busOVP}$
  - Worst case peak current (at peak of V_{acBo}; V_{outNom}, $I_{outOCPLev1}$)
    - $I_{PkMaxQpfc} = I_{pkLpfcMaxBCM} * t_{PFConMax}/t_{onMaxBCM}$
  - Worst case RMS current over AC cycle (V_{acBo}; V_{outNom}, $I_{outOCPLev1}$)
    - $I_{rmsMaxQpfc} = I_{pkMaxQpfc} * \sqrt{\frac{1}{6} - \frac{4}{9\pi} * \frac{\sqrt{2}*V_{acBo}}{V_{busDsgn}}}$
  - Different switch types supported
    - With OCP, or
    - Without OCP

- PFC diode
  - Voltage rating minimum
    - $V_{rrmMinDpfc} = 1.2 * V_{busOVP}$
  - Worst case peak current (at peak of V_{acBo}, V_{outNom}, $I_{outOCPLev1}$)
    - $I_{PkMaxQpfc} = I_{pkLpfcMaxBCM} * t_{PFConMax}/t_{onMaxBCM}$
  - Worst case RMS current over AC cycle (V_{acBo}; V_{outNom}, $I_{outOCPLev1}$)
    - $I_{rmsMaxDpfc} = I_{pkMaxQpfc} * \sqrt{\frac{4}{9\pi} * \frac{\sqrt{2}*V_{acBo}}{V_{busDsgn}}}$

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	120 W 3C evaB
7.2 PFC switch						
Voltage rating minimum	VdsMin_Qpfc	522			V	522
Switch peak current maximum	IpkMax_Qpfc	4.85			A	4.85
Switch rms current maximum over AC cycle	IrmsMax_Qpfc	1.75			A	1.75
Type of the selected PFC switch	Type_Qpfc	With OCP				With OCP
Ratio of Ids/Ics	kI_Qpfc	3520.00				With OCP / Without OCP
OCP threshold	Vtrip	1.90			V	
7.3 PFC boost diode						
Voltage rating minimum	VrrmMin_Dpfc	522			V	522
Peak current maximum	IpkMax_Dpfc	4.85			A	4.85
Average current maximum over AC cycle	IaveMax_Dpfc	0.44			A	0.44
RMS current maximum over AC cycle	IrmsMax_Dpfc	0.93			A	0.93

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PFC design guide
- PFC stage components: Bus capacitor

- Minimum of the required bus capacitance
  - $C_{busMin} = \frac{I_{busOCP1}}{2*\pi*f_{acMin}*V_{busRppl}} * 1.1$
  - Factor of 1.1 introduced considering the capacitance tolerance

- Bus capacitor low frequent rms current
  - $I_{rmsLFCbus} = \sqrt{I_{rmsMaxDpfc}^2 - I_{busOcp1}^2}$

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
7.4 PFC bus capacitor						
Bus voltage ripple at VacBo and Iout Ocp1	VbusRppl	20.00			V	20.00
Bus capacitance selected	Cbus	82	81		uF	82
Low frequent bus RMS current maximum	IrmsLF_Cbus	0.82			A	0.82

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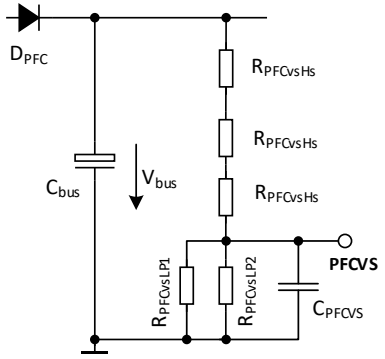
PFC design guide
- PFC stage components: Bus voltage divider

Min = Max ➔
Closest match value

Design steps	Design # / Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
7.5 Bus voltage divider						
1st resistor at lowside	RPfcvsL1_Base	1.5		53,033	kOhm	1.50
	RPfcvsL1_Factor	100k				100k
2nd parallel resistor at lowside, optional	RPfcvsL2_Base	7.5			kOhm	7.50
	RPfcvsL2_Factor	100k				100k
Number of in-series connected same resistors	NRpfcvsH	2				2
Resistance of the single high-side resistor	RPfcvsH_Base	1.05	9,760.00	9,760.00	kOhm	1.05
	RPfcvsH_Factor	10Meg				10Meg
kPFCVS design error	kpfcvs_DE	-5.16%				-5.16%
PFCVS filter capacitance proposal	Cpfcvs			229	pF	200

IPFCVSIkMax	0.2	µA	kIPFCVSDvd	10	
RPFCvsSumMax	53033	kOhm			
RPFCvsL1_Ch	150.00	kOhm			
RPFCvsL2_Ch	750.00	kOhm	RpfcvsLeq	125	kOhm
NRpfcvsHo	2	3	4		
RpfcvsHs_T	10004	kOhm	RPFCvsEq	124.22	kOhm

- Bus voltage divider as shown here



$$k_{PFCvs} = \frac{N_{RpfcvsHs} * R_{PFCvsHs} + R_{PFCvsLeq}}{R_{PFCvsLeq}}$$

  - High-side: $N_{RpfcvsH}$ (2 or 4) resistors of the same value in series
  - Low-side: One resistor, or two in parallel
  - Filter capacitor C_{PFCVS} recommended
- Maximum of the voltage divider resistors
  - $R_{PFCvsSumMax} = N_{RpfcvsH} * R_{PFCvsHs} + R_{PFCvsLeq} = \frac{V_{inBo}}{k_{IpfcvsDvd} * I_{PFCVSIkMax}}$
- Target resistance of each of high-side resistors based on the selected low-side resistor of $R_{PFCvsLP1}$ and $R_{PFCvsLP2}$
  - $R_{PFCvsHs_T} = {(k_{PFCvs}-1) * R_{pfcvsL}}/{N_{RpfcvsH}}$
  - The best match resistance calculated at $R_{PFCvsHs}$ and the design error calculated k_{pfcvs_DE} via $(Target - Result)/Target$
- Recommended filter capacitance
  - $C_{pfcvsMax} = \frac{1}{2\pi * {f_{swMin}}/{10} * R_{PFCvsEq}}$ with $R_{PFCvsEq}$ as the equivalent resistance of the voltage divider and seen at the PFCvs pin

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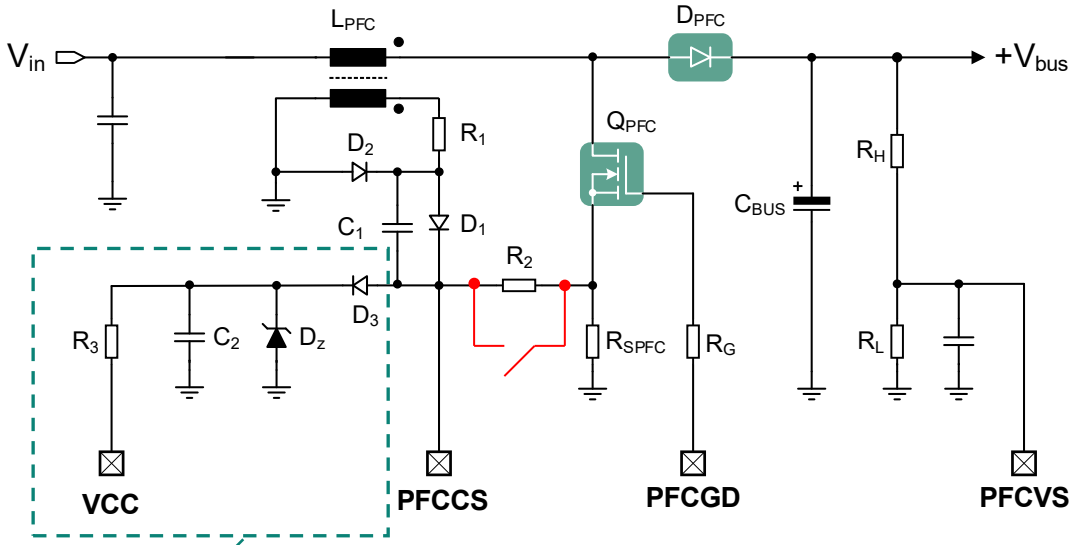
PFC design guide
- PFC stage components: PFCcs + ZCD circuitry

– **Case 1**: PFC switch without OCP

– Current solution



Voltage clamping circuitry

– Design approach
  – Dimension of the voltage clamping circuitry to ensure PFCcs pin voltage below its maximum
  – Select the ratio of $R_2/(R_1+R_2)$ to ensure the amplitude for proper ZCD at the peak of the maximum ac voltage
  – Choose the C1 and R1 for proper ZCD signal amplitude
  – Select the R1 as high as possible to minimize the power losses
  – A by-pass switch (i.e.. 2N7002) mandatory for PFC OCP
    – In parallel to R2 and Controlled by PFC gate
– Cons
  – Losses during PFC switch on-time
    – Free whiling diode D2 and R1
  – Not optimal clamping structure
    – D3, C2, R3, Dz
    – Requiring VCC
      – Causing complexity for PCB layout
      – Additional losses

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PFC design guide
- PFC stage components: ZCD divider

- Minimum of the voltage across the PFC auxiliary winding
  - $V_{auxPMin} = \left(V_{busDsgn} - \frac{V_{busRppl}}{2} - \sqrt{2} * V_{acMax}\right) * {}^{N_{aP}}/_{N_{mP}}$
- Maximum of R_{zcdHP} determined by
  - $R_{zcdHPMax} = {}^{V_{auxPMin}}/_{I_{RzcdHpMin}}$ with $I_{RzcdHpMin}$
    - as the minimum current through the resistor R_{zcdHP}
    - Voltage clamping structure dependent
- Minimum of the $R_{zcdLPMin}$ determined by
  - $R_{zcdLPMin} = \frac{R_{zcdHP}}{{}^{V_auxPMin}/_{(kvpfcZcd * V_PFCCSzcdresetMax)^{-1}}}$
- Minimum voltage at the ZCD pin without voltage clamping
  - $V_{PFCzcdMin} = \frac{R_{zcdL_P}}{R_{zcdH_P} + R_{zcdL_P}} * V_{AuxPMin}$

Design steps	Design # / Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
7.6 PFCZCDCS circuit						
7.6.1 PFC zcd divider						
Highside divider resistor	RzcdH_P_Base	9.1		92.69	kOhm	9.10
	RzcdH_P_Factor	1k				1k
Lowside divider resistor	RzcdL_P_Base	1.8	5.86		kOhm	1.80
	RzcdL_P_Factor	10k				10k
Diode Dzcd blocking voltage rating minimum	VrrmMin_DzcdP	76			V	76
Diode Dzcd current rating manimum	IfMin_DzcdP	48			mA	48

VAuxPMin	4.63	V	IRZCDHpMin	0.5 mA
RZCDHpMax	9.27	kOhm		
RzcdH_P	9.10	kOhm	RzcdLPMin	6.79 kOhm
			RzcdL_P	18.00 kOhm
			VPFCzcdMin	3.08 V

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PFC design guide
- PFC stage components: Current sensing resistor

- **Case 1**: PFC switch without OCP
  - Required current sensing resistance
  - $R_{CSpR} = {}^{V_{PFCCSocp1}}/_{I_{pkMaxQpfc}}$
  - Design error of the shunt resistance R_{CSp_DE} calculated based on the selected shunt resistor R_{CSp1} to R_{CSp3}
- **Case 2**: PFC switch with OCP
  - Over-current level defined by the resistor R_{set}

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	120 W 3C evaB
7.6.2 PFC CS						
Required PFC shunt resistance	RCSpR	0.132			Ohm	0.132
1st shunt resistor	RCSp1	0.24			Ohm	0.24
2nd shunt resistor	RCSp2	0.27			Ohm	0.27
3rd shunt resistor	RCSp3				Ohm	
Shunt resistance design error	RCSp_DE	3.48%				3.48%
Peak power losses maximum	PRCSp	0.402			W	0.402

VPFCCSocp1	0.638	V
RshPFCDsgn	0.085	Ohm

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	120 W 3C evaB
7.6.2 PFC CS						
Required PFC shunt resistance	RCSpR	1,379.985			Ohm	1,379.985
Selected sense resistance	RcsPFC_base	1.37				1.37
	RcsPFC_factor	1k				1k

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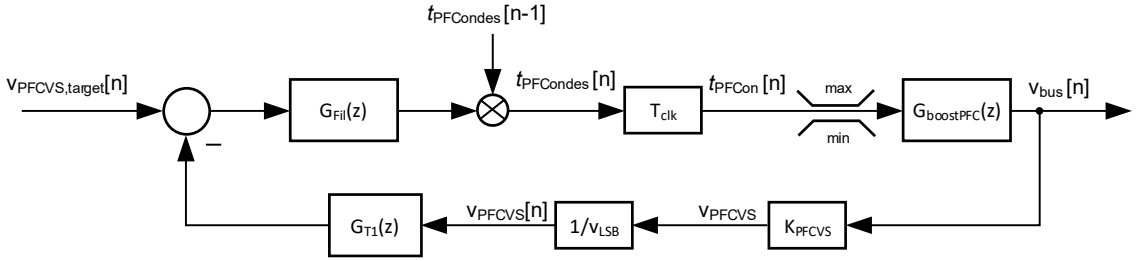
PFC design guide
- PFC regulator

– PFC digital control loop



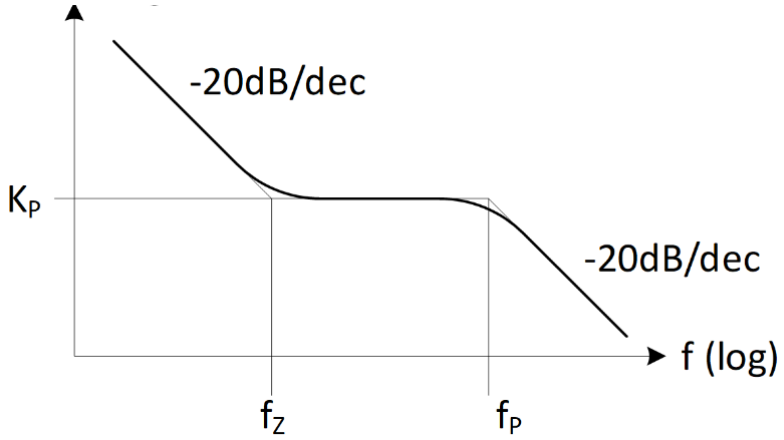
– Open loop gain of the PFC stage with the PIT1 regulator

$$\frac{P_{PFC}}{\bar{V}_{bus}} \cdot \frac{1}{sC_{PFC}} \cdot K_P \cdot \frac{1+\frac{2\pi f_z}{s}}{1+\frac{s}{2\pi f_P}} \quad \text{with}$$

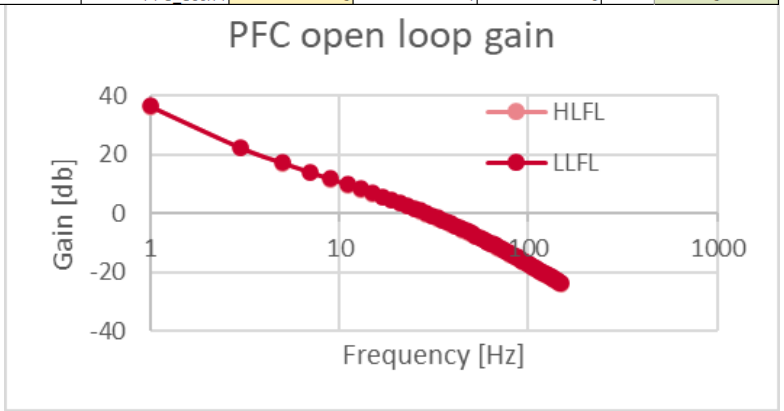
$$f_Z = \frac{\boldsymbol{PFC_{CoefA}}}{256 \cdot 2\pi \cdot 120\mu s \cdot \boldsymbol{PFC_{CoefB}}}$$

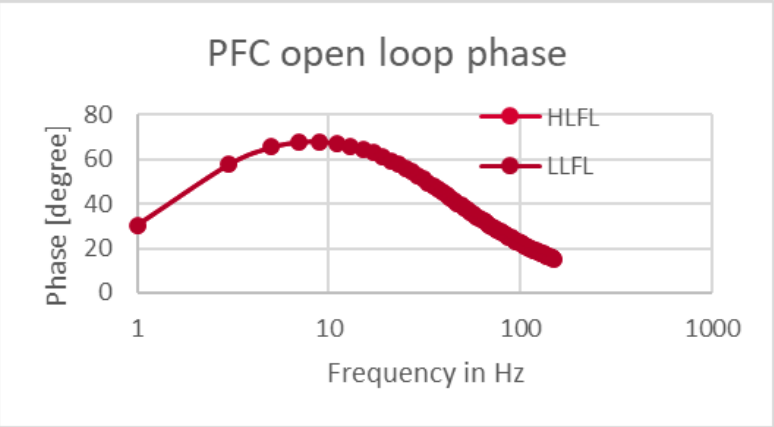
$$f_P = \frac{1}{2\pi \cdot 120\mu s \cdot \left(2^{\boldsymbol{PFC_{CoefT1}}} - 1\right)}$$

$$K_P = \frac{2^{-16} \cdot \boldsymbol{PFC_{CoefB}}}{\frac{2.8333V}{1791} \cdot k_{PFCVS}}$$



Design steps	Design # / Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
7.7 PFC control parameters						
	PFC_CoefA	128	128	2047		128
	PFC_CoefB	256	256	2047		256
	PFC_CoefT1	6	4	6		6





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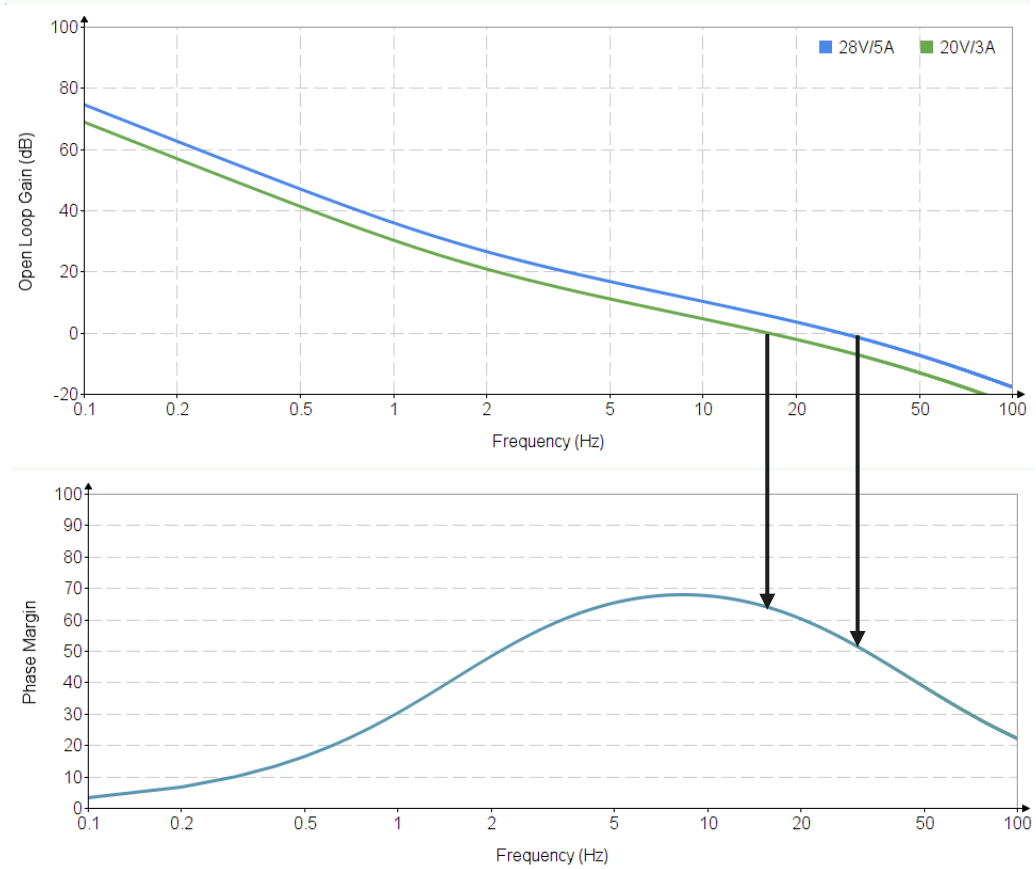
PFC design guide
- PFC regulator (cnt‘)

- Design proposal
  - Set PFC_{CoefT1} f_P to have at least 20dB suppression at the double mains frequency at the full load to reduce the bus voltage ripple
  - Set PFC_{coefB} and PFC_{coefA} to have
    - fz below 5 Hz
    - phase margin is between 45 and 60 degree

- Recommended value range in tracking
  - 128 ≤ **PFC_{CoefB}** ≤ 2047
  - 256 ≤ **PFC_{CoefA}** ≤ 2047
  - 4 ≤ **PFC_{CoefT1}** ≤ 6
    - Parameter value [4, 5, 6, 7] correspond to filter time of [1.86, 3.78, 7.62, 15.30] ms
    - Smaller value for faster V_{bus} responce

- Only load power and bus voltage dependent



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AC rectifier

- Voltage rating minimum
  - $V_{rrmMinDBR} = 1.2 * \sqrt{2} * V_{acMax}$ with 1.2 as safety margin
- RMS current maximum over AC cycle
  - $I_{rmsMaxDBR} = I_{rmsVacBoIoutOCp1}$
- Average current maximum over AC cycle
  - $I_{aveMaxDBR} = \frac{2\sqrt{2}}{\pi} * I_{rmsVacBoIoutOCp1}$

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
8 Input bridge rectifier						
Voltage rating minimum	VrrmMin_DBR	448			V	448
RMS current maximum over AC cycle	IrmsMax_DBR	2.62			A	2.62
Maximum average current	Iavemax_DBR	2.36			A	2.36
Maximum average power losses	Pmax_DBR	4.24			W	4.24

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HFB design
- Overview

- HFB operating process
- Starting point conditions
- Switch selection
- Negative magnetizing current for ZVS
- Transformer
  - Magnetizing inductance and resonant tank
  - Main windings
  - VCC supply and auxiliary winding(s)
- Shunt resistance
- Output capacitance
- Additional csv parameter setting
  - Mode transition voltage
  - ZVS pulse width
- PCB trace resistance for power losses estimation

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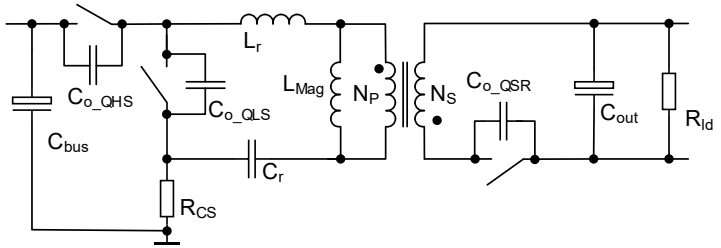
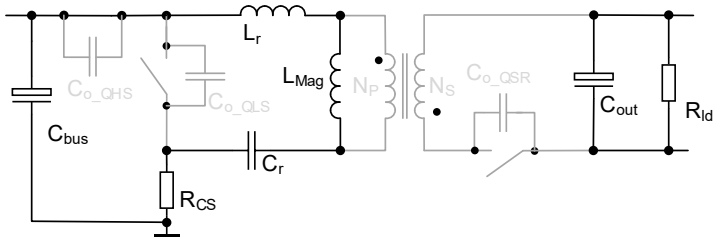
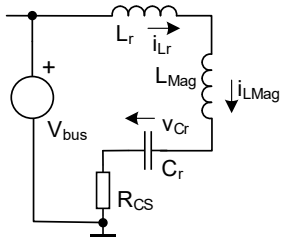
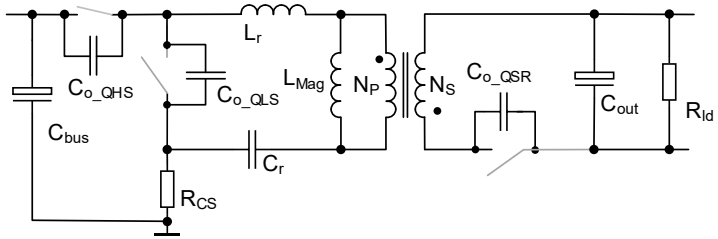
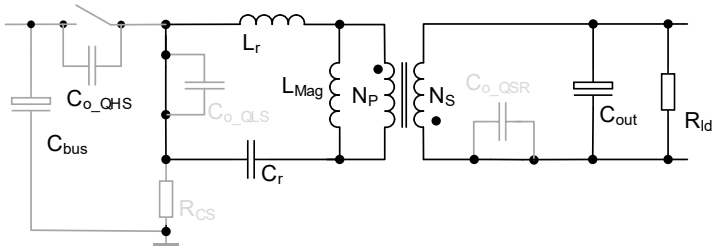
HFB design
- HFB operating process

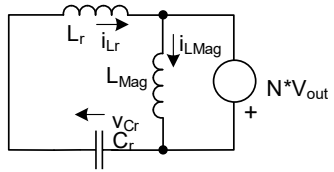


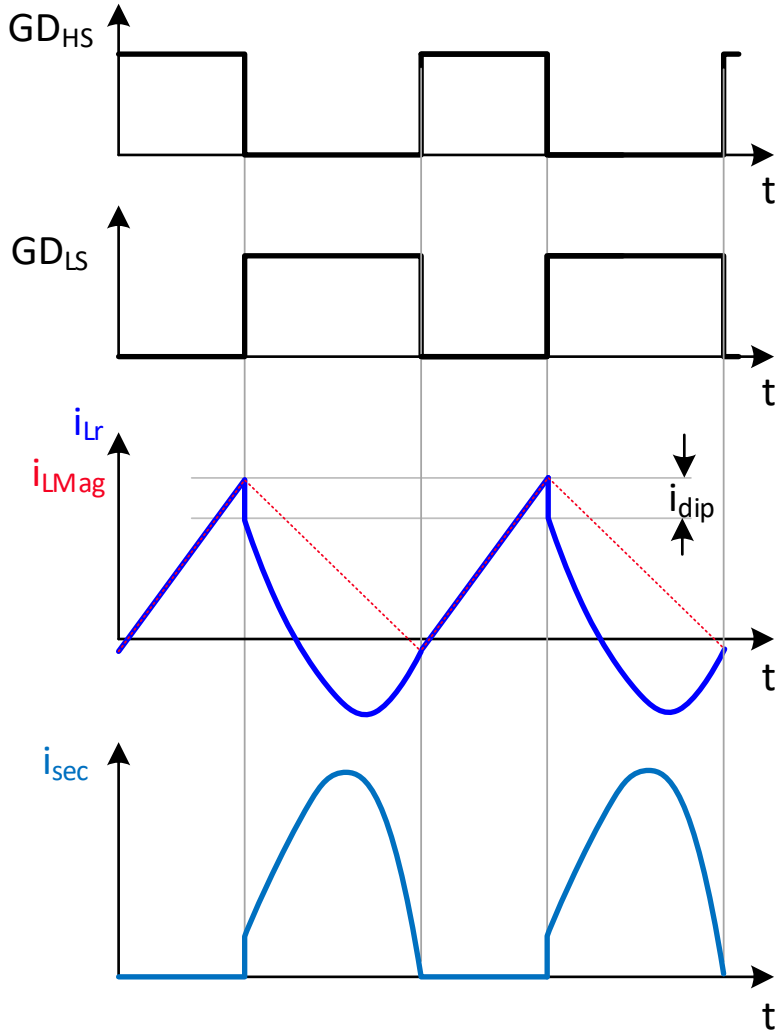












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HFB design
- Starting point conditions

- Design input
  - f_{swD}
    - Desired switching frequency of the HFB at the nominal load
    - Upper limit around 400 kHz
  - D_{max}
    - Maximum duty at $V_{busBoNom}$ and nominal load
    - Selection between 66% or 75%
      - k_tHS_limit configured accordingly in the EDT
      - Higher duty allowing
        - lower value of the bus operating voltage minimum, or
        - possible with smaller bus capacitor
  - $V_{busBoNom}$
    - Bus brown-out (minimum of the bus voltage) at the nominal output voltage
    - Different to the AC brown-out level V_{acBo} or V_{inBo}

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
9 HFB design						
9.1 Design starting point conditions						
Desired switching frequency	fswD	205.0		400	kHz	205.0
Maximum duty at VbusBoNom and nominal load	Dmax	75%				75%
Bus brownout at nominal output voltage	VbusBoNom	300.0	261		V	300.0

TswD	5.00	µs		
			k_tHS_limit	3

  - $V_{busBoNom}$ minimum
    - To be checked after design finished
    - $V_{busUVP} = N \cdot \frac{V_{outNom}}{D_{max}}$
    - $V_{busBoNum} \geq V_{busUVP}$ for proper operation

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HFB design
- Switch selection

- Both GaN and Si MOFET supported
- For the 2nd side rectifier
  - SR FET, or
  - Diode

- Important parameters
  - $C_{o(tr)}$ of the selected Q_{HS} and Q_{LS} switches
  - C_{oss} of the SR device
  - Check the respected DS for the number
  - Impact on
    - Negative magnetizing current setting for ZVS
    - Maximum negative magnetizing current limit

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
9.2 Selection of switches						
9.2.1 High side switch						
Product	QHS	IPD60R600P7				IPD60R600P7
CoTr	CoTr_QHS	30			pF	30
RdsOn	RdsOn_QHS	600			mOhm	600
9.2.2 Low side switch						
Product	QLS	IGLD60R190D1				IGLD60R190D1
CoTr	CoTr_QLS	30			pF	30
RdsOn	RdsOn_QLS	190			mOhm	190
9.2.3 2nd side rectifier						
Type of the 2nd side rectifier	Type_2ndRect	SR				SR
2nd side rectifier device	SecondRect	BSC160N15NS5				BSC160N15NS5
Rated voltage	V2ndRect	150			V	150
Voltage derating factor of the 2nd side rectifier	kVdr_2ndRect	0.8				0.80
Number of the SR switches in parallel	N_QSR	2			piece	2
Coss of the SR switch	Coss_QSR	340			pF	340
RdsOn	RDSonMax_QSR	16			mOhm	16
Qg	Qg_QSR	19			nC	19

- $k_{Vdr_2ndRect}$
  - Voltage derating factor for the SR switch
  - Recommendation: beginning with 0.8

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HFB design
- Negative magnetizing current for ZVS

- ZVS operation requiring enough magnetizing current to swap the voltage at the HFB switching node: to charge and discharge the total equivalent capacitance (C_{oEq}) at the switching node

- Limits of the HFB transformer turns ratio N_i
  - Minimum to limit the drain-source voltage of the SR switch at the maximum bus voltage
  - Maximum to ensure the nominal output voltage at the minimum bus voltage $V_{busBoNom}$ where the HFB running with the maximum HS duty ratio D_{max}

- Required negative magnetizing current $I_{MagNegR}$ at V_{busOVP} as the worst case

- $I_{MagNegPerc}$ calculated based on input $I_{MagNegS}$

Design steps	Design # Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
9.3 Negative magnetizing current for ZVS						
Choosen transformer turns ratio	Ni	7.00	2.32	8.04		7.00
ZVS required negative magnetizing current amplitude	IMagNegR	0.066			A	0.066
Selected negative magnetizing current amplitude	IMagNegS	0.16			A	0.16
Percentage of the negative magnetizing current	IMagNegPerc	11			%	11
Magnetizing current positive peak value at IoutNom	IMagPosNom	1.589			A	1.589
Magnetizing current positive peak value at IoutOCPLev1	IMagPosOcp1	1.946			A	1.946

$$C_{oEq} = C_{oTrQHS} + C_{oTrQLS} + C_{ossQsr}/N_i^2$$

$$N_{Min} = \frac{V_{busOVP}}{V_{dsQsr} * k_{VdsQsr}}$$

			DD_QHS	0.478	
Nmin	5.44		Nmax	8.04	
CoEq	92.9	pF	t_dead_HS_Half	240	ns

$$N_{Max} = \frac{D_{max} * V_{busBoNom}}{V_{outNom}}$$

$$D_{dQHS} = \frac{N_i * V_{outNom}}{V_{busDsgn}}$$

$$I_{MagNegR} = \frac{C_{oEq} * V_{busOVP}}{t_{deadHS_Half}}$$

- $t_{deadHSHalf}$
  - Initial value for the dead time before Q_{HS} turn-on
  - Q_{HS} and Q_{LS} type dependent, and pragmatically
    - Both of GaN devices: 240 ns
    - One or both of Si device 490 ns

$$I_{MagNegPerc} = MIN\left(\frac{I_{MagNegS} * N_i * 100}{2 * I_{outNom}}, I_{MagNegMaxPerc}\right)$$

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HFB design
- Negative magnetizing current for ZVS

- HFB design consideration
  - Steady state operation at $I_{outOCPLev1Perc}$ for the HFB transformer peak current design
  - $I_{outOCPMax}$ to be covered by
    - Proper value of the output capacitance
    - Output voltage range

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
9.3 Negative magnetizing current for ZVS						
Choosen transformer turns ratio	Ni	7.00	2.32	8.04		7.00
ZVS required negative magnetizing current amplitude	IMagNegR	0.066			A	0.066
Selected negative magnetizing current amplitude	IMagNegS	0.16			A	0.16
Percentage of the negative magnetizing current	IMagNegPerc	11			%	11
Magnetizing current positive peak value at IoutNom	IMagPosNom	1.589			A	1.589
Magnetizing current positive peak value at IoutOCPLev1	IMagPosOcp1	1.946			A	1.946

- Magnetizing current for the HFB transformer at $I_{outOCPLev1}$
  - Positive peak $$I_{MagPosOCP1} = \frac{2 * I_{outNom} * {I_{outOCPLev1Perc}}/{100}}{N_i} + I_{MagNegS}$$
  - Peak-peak value $$I_{MagPkPkOCP1} = I_{MagPosOCP1} + I_{MagNegS}$$

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HFB design
- Transformer and resonant tank

- Optimization options
  - Output current at nomial value
    - Recommended for small difference between I_{outNom} and $I_{outOCPLev1}$
  - OCPlev1
- Magnetizing inductance

$$L_{Pcal} = \frac{t_{onQls} * N_i * V_{outNom}}{I_{MagPkPkOCP1}}$$

- Resonant capacitor
  - Two main resonant built-up by
    - L_{Mag} and C_{lump} with C_{lump} as lumped-up capacitance at the
    - L_r and C_{lump} HB switching node
  - Resonant from L_r and C_{lump} defining the dimensioning of C_r
  - Optimal design: i_{Lr} reaching i_{LMag} @ end of t_{onQLS}
  - No simple formula to calculate the proper C_r due to
    - Non-zero starting point
    - Timely changing i_{LMag}
  - Rough calculation: ${}^{T_r}/_2 = 70\sim80\% * t_{onQLS}$ with $T_r = 2 * \pi * \sqrt{L_r * C_r}$
  - Fine tune of C_r on board necessary
  - Calculation with different value of f_r in the spread sheet and best match of f_r for the optimal design shown in the tool

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
9.4 Transformer inductance and resonant tank						
Output power level for HFB optimization	Psel	IoutOCPLev1				IoutOCPLev1
Magnetizing inductance calculated	LpCal	213.19			µH	213.19
Magnetizing inductance choosen	Lp	230			µH	230
Leakage inductance calculated	Lr	4.0			µH	4.0
Resonant capacitance at the nominal condition	CrCal	0.085			µF	0.085
Average voltage across the resonant capacitor	VCrAvg	196.0			V	196.0
Factor of the capacitance at the VCrAvg over at 0 V	kCrV	20%				20.0%
Capacitance at 0 V bias	Cr0V	0.424			µF	0.424
Selected value of the resonant capacitors	Cr	0.440			µF	0.440
Calculated LS on time at the nominal output	tTransNom	2.290			µs	2.290
Percentage of tTRANSnom at 0 V bias	tTransRvs0Vperc	223.6			%	223.6
Equivalent ESR of the resonant capacitor	CrESR	10			mOhm	10

tonD_QHS	2.276 us	tonD_QLS	2.484 us
T_wo_tdeadHS	4.76 us		

$$t_{onDQhs} = \left(T_{swD} - \frac{t_{deadHSHalf}}{1000}\right) * D_{dQhs}$$

$$t_{onDQls} = \left(T_{swD} - \frac{t_{deadHSHalf}}{1000}\right) * \left(1 - D_{dQhs}\right)$$

$$T_{wotdeadHS} = t_{onDQhs} + t_{onDQls}$$

$$C_r = \frac{1}{4 * \pi^2 * f_r^2 * L_r}$$

$$V_{crAvg} = V_{outNom} * N_i$$

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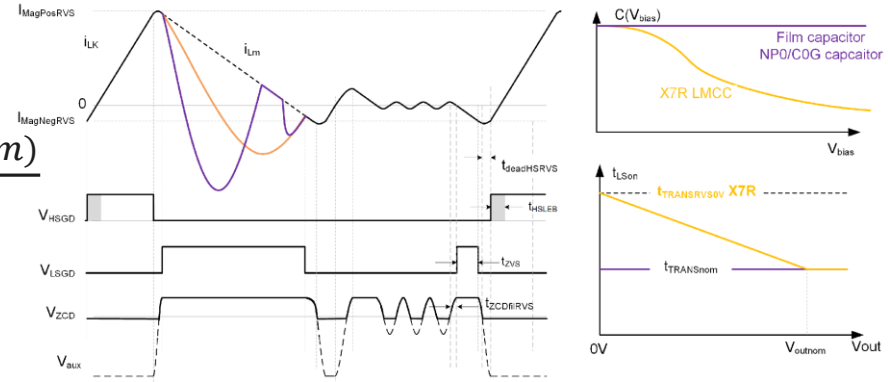
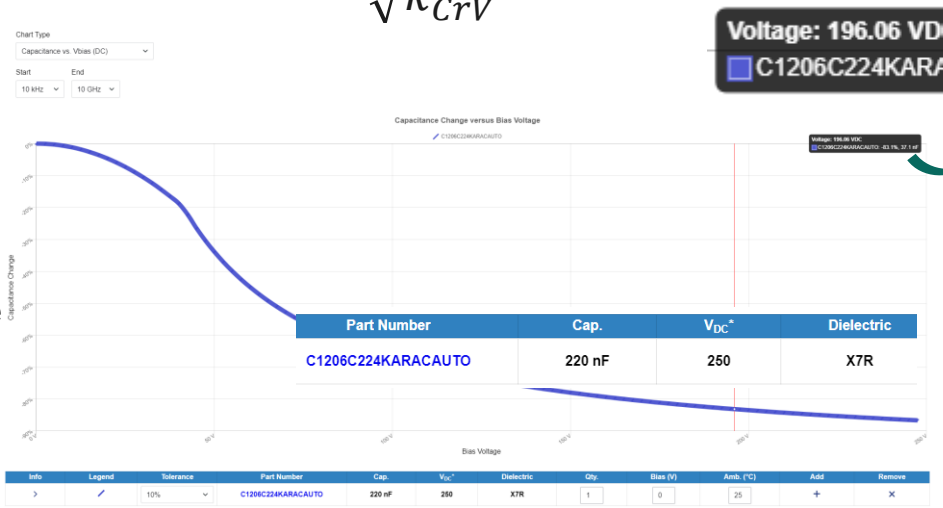
HFB design
- Transformer and resonant tank

- Resonant capacitor (cnt')
  - Different dependence of the capacitance on the DC bias voltage ($k_{CrV} = C(V_{crNom})/C(0V)$) from different types of the capacitor
    - **Film capacitor**: low dependency, $k_{CrV} \approx 1$
      - Pro: lowest audible noise level
      - ➔ Con: relative high price, biggest size/footprint
        Recommended for
        1) application with fixed output voltage
        2) audible noise sensitive application
    - **MLCC NPO/C0G**: low dependency, $k_{CrV} \approx 1$
      - Pro: small size, low audible noise level
      - Con: low capacitance, price, big footprint of required number of the capacitors
    - **MLCC X7R**: high dependency, $k_{CrV} \approx 20\%$ as from the example
      - Pro: smallest size, low price
      - Con: high audible noise
      - ➔ Recommended for
        1) Compact design
        2) Audible noise less-sensitive, but cost sensitive applications

$$k_{CrV} = \frac{C_{(VcrNom)}}{C_{(0V)}}$$



$$t_{TransRvs0Vperc} = \frac{100}{\sqrt{k_{CrV}}}$$



$k_{CrV} \approx 20\%$

(Source: https://ksim3.kemet.com/capacitor-simulation)

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HFB design
- Transformer: main windings

- Main windings
  - Specifying the maximum flux density
  - Select the core for the HFB transformer from the available cores, or insert a customer core info in the MagCore sheet and select that core
  - N_{pMin} calculated with $I_{outOCPMaxperc}$ plus 5% design margin
    - $N_{pMin} = \frac{L_p * \left(I_{MagPosOCP1} * \left(\frac{I_{outOCPMacPerc}}{100} + 0.05 \right) \right)}{B_{max} * A_e}$
    - $N_{sMin} = \frac{N_{pMin}}{N_i}$
- R_{dcPri} and R_{dcSec}
  - Resistance of the transformer primary and secondary winding resistance for the power losses estimation
  - Assumption that the winding AC resistance k_{RacRdc} times of its DS resistance
  - Non-zero value required for the power losses estimation

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
9.5 Transformer main windings						
Maximal core flux	Bmax	0.35			T	0.35
Core selected	Core	RM10				RM10
Selected turns count of the secondary winding	Ns	3	3.00		turns	3
Selected turns count of the primary winding	Np	21	15.98		turns	21
Realized turns ratio of Np:Ns	N	7.00	2.32	8.04		7.00
DC resistance of the transformer primary winding	RdcPri	60.0			mOhm	60.0
DC resistance of the transformer secondary winding	RdcSec	7.0			mOhm	7.0

Ae	98.0	mm^2
NpMin	20.7	
kRacRdc	1.5	

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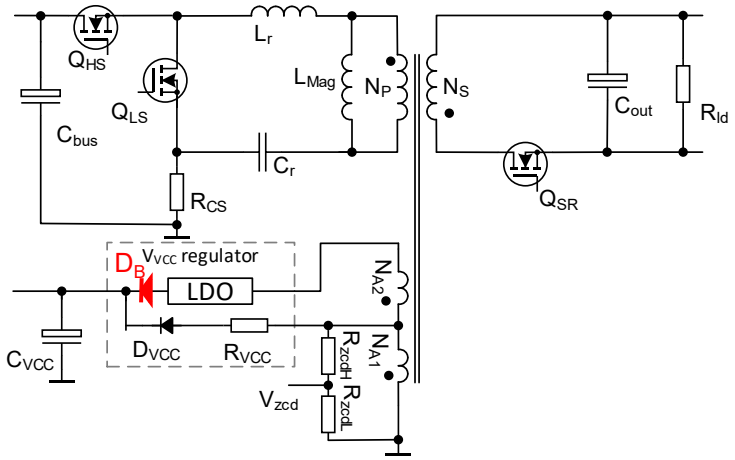
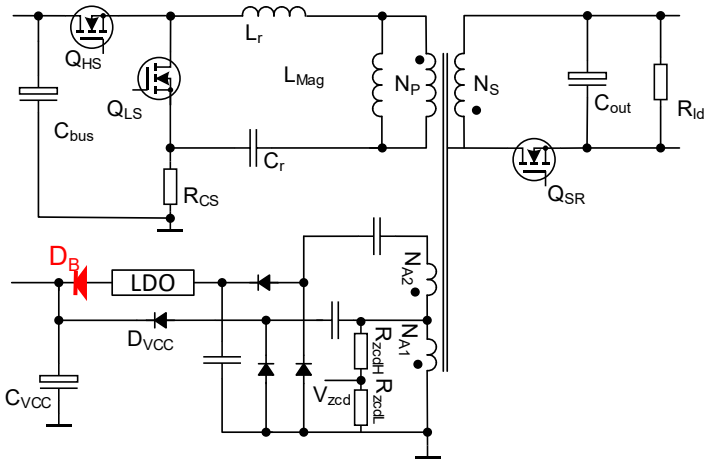
HFB design
- Transformer: VCC supply and auxiliary winding(s)

– Flyback windings + LDO



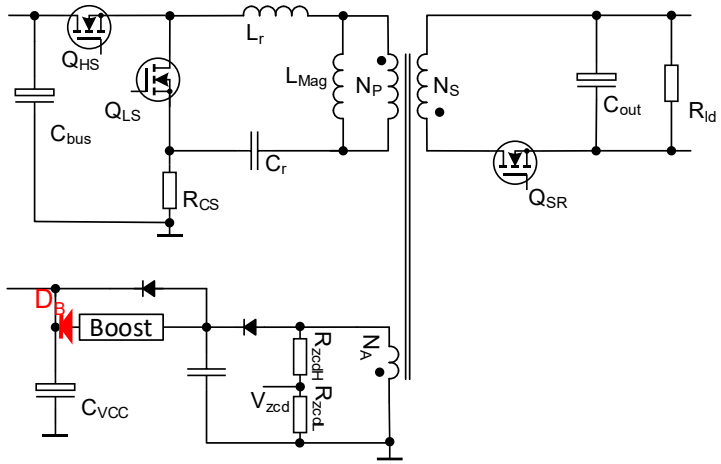
– Auxiliary winding voltage depending on the **output** voltage
– **Two** auxiliary windings
– Step-down LDO, **less efficient**
– Less concern about EMI
– **Cost low**

– Charge-pump + LDO



– Auxiliary winding voltage depending on the **bus** voltage
– **Two** auxiliary windings
– Step-down LDO, **less efficient**
– Less concern about EMI
– **Cost high**
– **Audible noise** with the X7R capacitors due to pulse current

– Flyback winding + boost



– Auxiliary winding voltage depending on the **output** voltage
– **One** auxiliary winding
– Boost converter, **more efficient**
– Concern about EMI
– **Cost middle**

Charge pump + LDO for the case $\frac{V_{outNom}}{V_{outUVP}} > \frac{V_{bucOVP}}{V_{inBo}}$; otherwise, Flyback aux + LDO; Flyback winding + boost for high performance design

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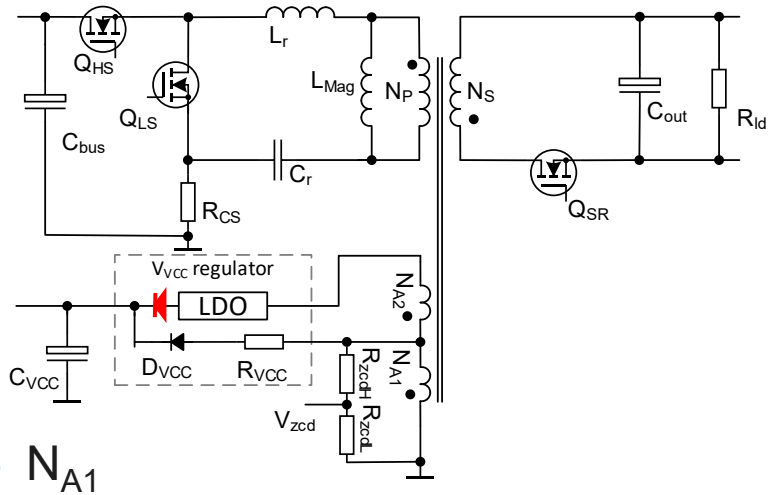
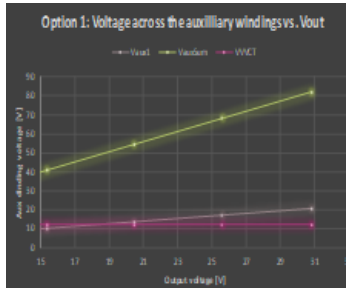
HFB design
- Transformer: VCC supply via flyback windings + LDO





Design steps	Design # / Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
9.6.1 Option 1: flyback auxiliary windings + LDO						
1st auxiliary winding turns count	NA1_FB	2	1.36	2.14	turns	2
2nd auxiliary winding turns count	NA2_FB	9			turns	9
RzcdL	RZCDL_Base_FB	1.50		11	kOhm	1.50
	RZCDL_Factor_FB	10k				10k
RzcdH	RZCDH_Base_FB	9.76	97.60	97.60	kOhm	9.76
	RZCDH_Factor_FB	10k				10k
VoutVzcdRatio design error	VoutVzcdRatio_DE_FB	-0.54%				-0.54%

- N_{A1}
  - Minimum
    - To get the target V_{VCCT} at the nominal output voltage

$$N_{A1Min} = {(V_{VCCT} + V_{fDvcc}) * N_s}/{V_{outNom}}$$

  - Maximum
    - Resulted V_{VCC} touching the $V_{VCConMax}$ at the output OVP

$$N_{A1Max} = {V_{VCConMax} * N_s}/{V_{outOVP}}$$

- N_{A2} to ensure the V_{VCCT} at V_{outUVP}

$$N_{A2} = RoundUp\left(\frac{V_{VCCT*N_s}}{V_{outUVP}} - N_{A1}\right)$$

- R_{zcd} network design
  - The maximum total resistance defined by the required current through the resistor at the lowest output voltage during the HFB operation

$$R_{zcdSumMaxFB} = \frac{(V_{outUVP} * 0.9) * {N_{A1FB}}/{N_s}}{I_{ZCDlkMax} * k_{IzcdDvd}}$$

with the $k_{IzcdDvd}$ of 2.5

  - Maximum of the low-side divider resistor based on the ratio VoutVzcdRatio ($k_{VoutVzcd}$)

$$R_{zcdLFBMaxFB} = {R_{zcdSumMaxFB}}\Big/{\left({N_{A1FB}}/{N_s} * k_{VoutVzcd}\right)}$$

  - Best match for the high-side resistance calculated based on the selected low-side resistance

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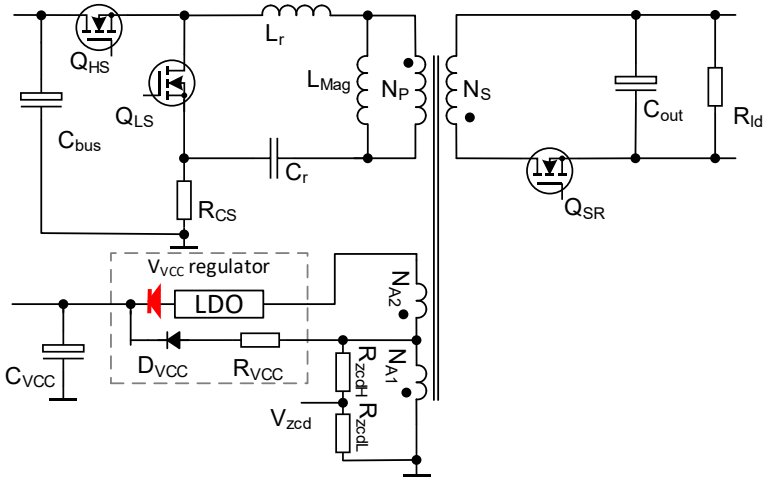
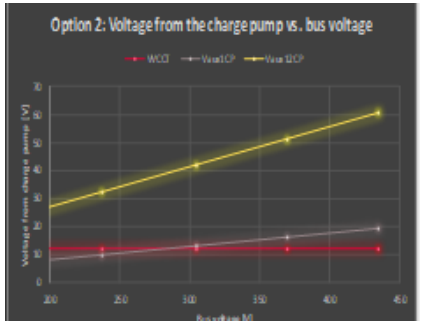
HFB design
- Transformer: Charge-pump + LDO





Design steps	Design # / Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
9.6.2 Option 2: charger pump + LDO						
1st auxiliary winding turns count	NA1_CP	1	1.00	1.13		1
2nd auxiliary winding turns count	NA2_CP	2	1.65			2
RzcdL	RZCDL_Base_CP	6.80		11.25	kOhm	6.80
	RZCDL_Factor_CP	1k				1k
RzcdH	RZCDH_Base_CP	1.87	18.70	18.70	kOhm	1.87
	RZCDH_Factor_CP	10k				10k
VoutVzcdRatio design error	VoutVzcdRatio_DE_C	-0.45%				-0.45%

- N_{A1CP}
  - Maximum at the resulted voltage at V_{auxA1} touching the $V_{VCConMax}$ at V_{busOVP}
  - $N_{A1Max} = \frac{V_{VCConMax}+2*V_{fDVCC}}{V_{busOVP}} * N_p$
- N_{A2CP}
  - To ensure the target V_{VCCT} at V_{inBo}
  - $N_{A2CPMin} = \frac{V_{VCCT}+2*V_{fDVCC}}{V_{inBo}} * N_p - N_{A1CP}$

- R_{zcd} network design
  - Maximum value of R_{ZCDH}+R_{ZCDL} for enough current

$$R_{zcd\mathbf{Sum}MaxCP} = \frac{(V_{outUVP} * 0.9) * {N_{A1CP}}/{N_s}}{I_{ZCDlkMax} * k_{IzcdDvd}}$$

  - Maximum low-side resistance

$$R_{zcd\mathbf{L}CPMaxCP} = \frac{R_{zcdSumMaxCP}}{{N_{A1CP}}/{N_s} * k_{VoutVzcd}}$$

- Best match for the high-side resistance calculated based on the selected low-side resistance

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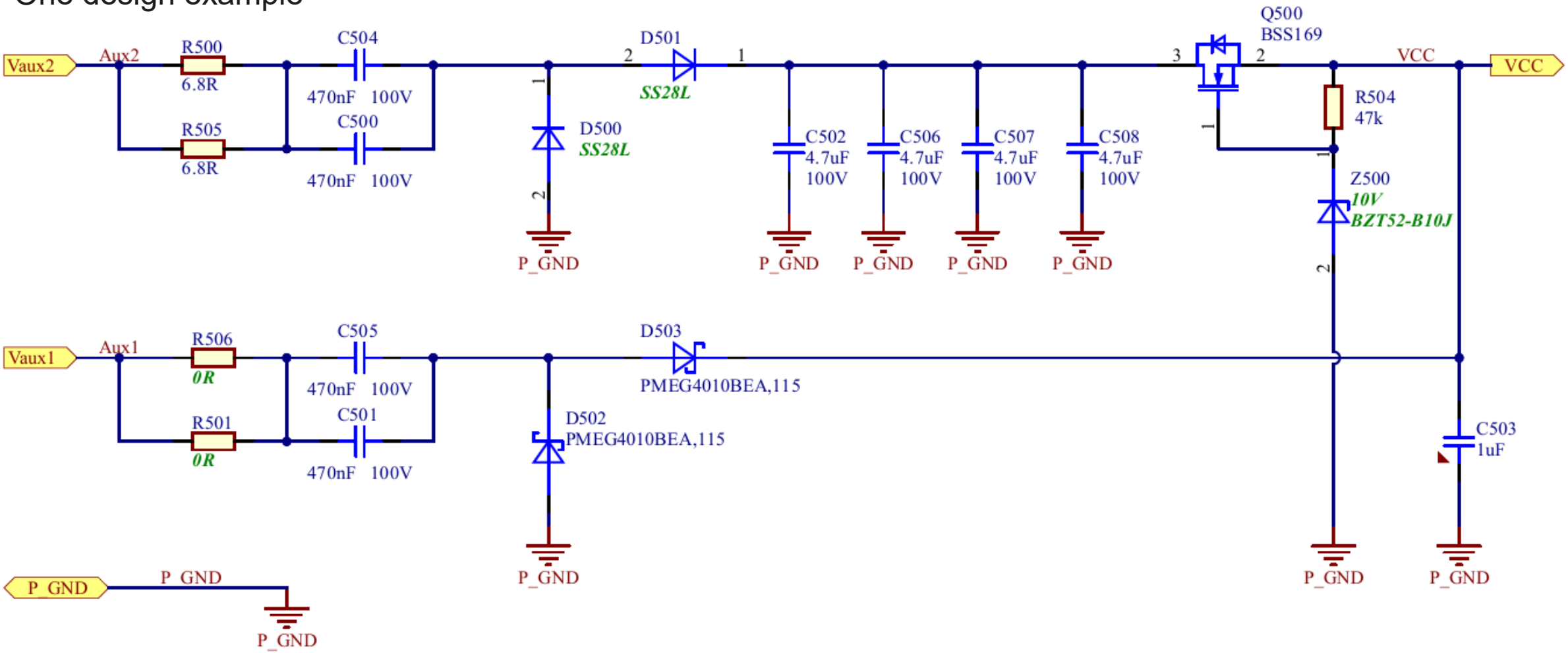
HFB design
- Transformer: Charge-pump + LDO

– One design example



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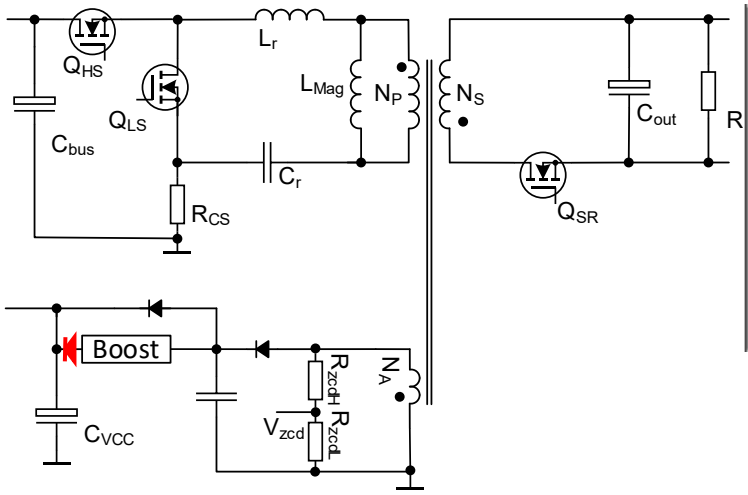
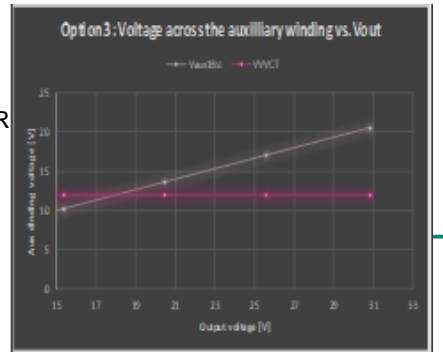
HFB design
- Transformer: VCC supply Flyback winding + boost





Design steps	Design # Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
9.6.3 Option 3: Aux + boost						
Auxiliary winding turns count	NA_Bst	2	1.36	2.14		2
RzcdL	RZCDL_Base_Bst	1.54		11.25	kOhm	1.54
	RZCDL_Factor_Bst	10k				10k
RzcdH	RZCDH_Base_Bst	9.76	97.60	97.60	kOhm	9.76
	RZCDH_Factor_Bst	10k				10k
VoutVzcdRatio design error	VoutVzcdRatio_DE_Bst	1.73%				1.73%

- N_{ABst}
  - Minimum to ensure the target V_{VCCT} at the nominal output voltage
    - $N_{ABstMin} = \frac{V_{VCCT}+V_{fDVCC}}{V_{outNom}} * N_s$
  - Maximum to limit the V_{A1Bst} below the $V_{VCConMax}$ at output OVP level
    - $N_{ABstMax} = \frac{V_{VCConMax}}{V_{outOVP}} * N_s$

- R_{ZCD} network design
  - Maximum value of R_{ZCDH}+R_{ZCDL} for enough current

$$R_{zcdSumMaxBst} = \frac{(V_{outUVP} * 0.9) * {N_{ABst}}/{N_s}}{I_{ZCDlkMax} * k_{IzcdDvd}}$$

  - Maximum low-side resistance

$$R_{zcdLCPMaxBst} = \frac{R_{zcdSumMaxCP}}{{N_{ABst}}/{N_s} * k_{VoutVzcd}}$$

- Best match for the high-side resistance calculated based on the selected low-side resistance

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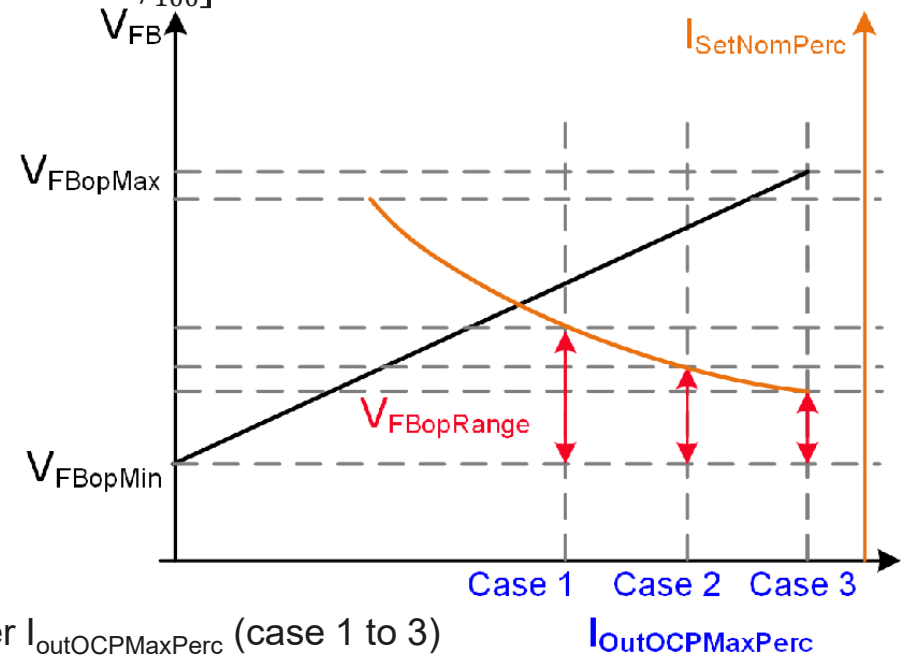
HFB design
- Shunt resistance

Design steps	Design # Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
9.7 Shunt resistor						
Required shunt resistor	RCSR	0.164			Ohm	0.164
1st shunt resistor	RCS1	0.33			Ohm	0.33
2nd shunt resistor	RCS2	0.33			Ohm	0.33
3rd shunt resistor	RCS3				Ohm	
Shunt resistance design error	RCSde	-0.48%				-0.48%
Maximum power losses	PRcsMax	0.82			W	0.82

- Required shunt resistance
  - $R_{csR} = \frac{DAC_Range * {I_{setNomPerc}}/{100}}{2 * {I_{outNom}}/{N_i}}$
  - ${I_{setNomPerc}}/{100} = MIN\left[\frac{ADC_MFIO2_Range_Thr_Max - V_{fbOpMin}}{ADC_MFIO2_Range * {I_outOCPMaxPerc}/{100}}, \frac{1}{{I_{MagNegPerc}}/{100} + {I_{outOCPMaxPerc}}/{100}}\right]$
- The required shunt resistance depending on
  - $I_{outOCPMaxPerc}$
  - $V_{fbOpMin}$

  ➡ Shunt resistance on the board to be updated in case of any change of these parameters
- Power rating calculation
  - $I_{rmsCsMax} = \sqrt{\frac{D_{Max}}{3}} * I_{MagPosPkOCPMax}$ with
    - $I_{MagPosPkOCPMax} = 2 * \frac{I_{outNom} * {I_{outOCPMaxPerc}}/{100}}{N_i} + I_{MagNegNom}$



Higher $I_{outOCPMaxPerc}$ (case 1 to 3) leading to narrower effective V_{FB} operating range!

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HFB design
- Output capacitance

- Minimal capacitance for the allowed voltage drop at load jump
  - $C_{outMin} = \frac{{}^{P_{outNom}}/_{V_{outNom}} * {}^{N_{RspDelay}}/_{f_{swD}}}{V_{outDropLdjmp}}$, with
    - $V_{outDropLdjmp} = V_{outNom} * k_{VoutDropLdjmp}$
    - $N_{RspDelay}$ as the feedback response delay in terms of HFB switching cycles at big load jump, i.e.: from burst to maximum load
- Ripple current rating
  - $I_{rmsCout} = \sqrt{I_{rmsSecNom}^2 - I_{outNom}^2}$, with

$$I_{secSecNom} = \frac{\pi}{2 * \sqrt{2 * (1 - D_{QHS})}} * I_{outNom}$$

Design steps	Design # Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 120 W 3C evaB
9.8 Output capacitor						
Total output capacitor RMS current	Irms_Cout	8.22			A	8.22
Selected output capacitor: current capability of single device	Irms_CoSingle	2800			mA	2800
Selected output capacitor: ESR of single device	ESR_CoSingle	37.0			mOhm	37.0
Selected output capacitors: Required pieces	N_Co	3				3
Total output capacitance	Cout	1000	87		uF	1000
				NRspDelay		10 cycles
				IrmsSecNom		6.09 A

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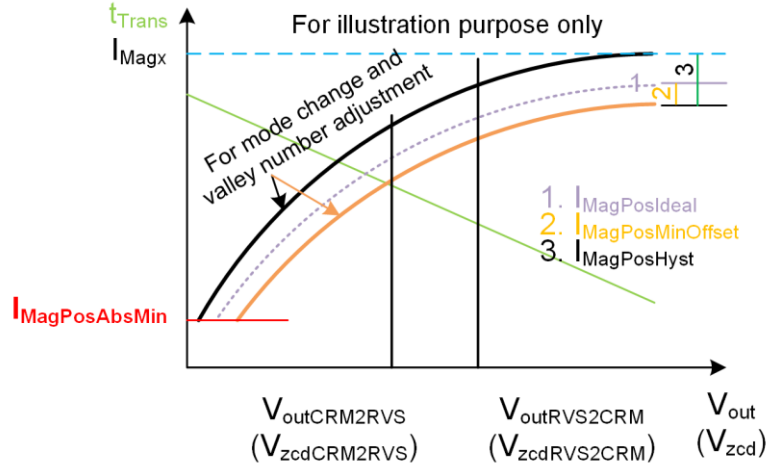
HFB design
- Additional csv parameter setting

- Mode transition
  - CRM vs. ZV-RVS mode
    - CRM at high and medium load
    - ZV-RVS operation at low and light load
  - Voltage thresholds, as defined

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
10.1 mode transition voltage						
Output voltage for CRM to RVS transition	VoutCrm2Rvs	16.0			V	16.0
Output voltage for CRM to RVS transition	VoutRvs2Crm	18.0	16.8		V	18.0

- Two main considerations for the value setting
  - Maximum spike of V_{dsSR}
    - Occurring at the transition from CRM to ZV-RVS at V_{outNom}
    - Beginning with a value for $V_{outCrm2Rvs}$ around 70% of V_{outNom}
    - Select the proper value of $V_{outCrm2Rvs}$ based on V_{dsSR}
    - Set the $V_{outRvs2Crm}$ with good margin to $V_{outCrm2Rvs}$ for stable mode transition
  - Efficiency
    - More efficient at CRM operation at heavy load
    - More efficient at ZV-RVS mode at light load

- Current thresholds
  - Two curved lines for mode transition and valley # change
  - The higher the value of ***$I_{MagPosHystPerc}$***, the higer the output current
    - At mode transition from RVS to CRM
    - Valley number decreasing in RVS mode
  - The higher the value of ***$I_{MagMinOffsetPerc}$***, the lower of the output current at
    - Mode transition from CRM to RVS
    - Valley number increasing in RVS mode



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HFB design
- Additional csv parameter setting

- ZVS pulse width
  - Ensuring ZVS for the Q_{HS} via the ZVS pulse
  - Minimum pulse width higher than the minimum on-time of the SR controller
  - Value t_{ZVSmin} just setting the lower boundary, real t_{ZVS} calculated based on the V_{bus}

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
10.2 ZVS pulse width setting						
Maximum of the SR controller minimal on-time	tonMinSrCtrl	600			ns	600
ZVS pulse width setting	tZVSmin	600	600		ns	600

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HFB design
- PCB trace resistance for power losses estimation

– Additional information for the power losses estimation
– Non-zero value required for the losses estimation

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	120 W 3C evaB
10.3 PCB trace resistance						
Primary high-current PCB trace	RpcbP	20			mOhm	20
Secondary high-current PCB trace	RpcbS	3			mOhm	3

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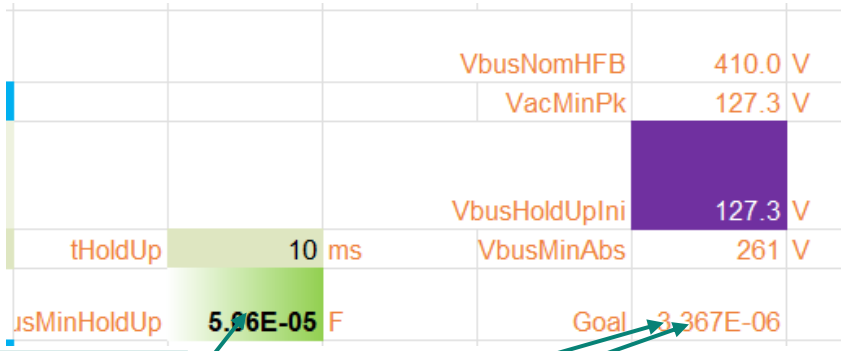
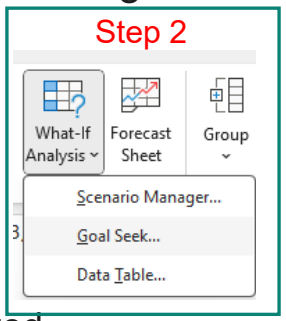
PFC design guide
- Hold-up time and bus capacitance

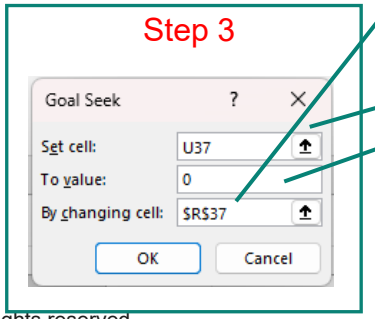
- Some application requesting hold-up time (t_{HoldUP}) ➔ requesting higher bus capacitance
- This requested bus capacitance calculated by

$$C_{busHoldUp} = \frac{2}{V_{busHoldUpIni}^{\ 2} - V_{busMinAbs}^{\ 2}} \cdot \frac{P_{outNom}}{Eta_{HFB}} \cdot \left(\frac{1}{4} \cdot \frac{1}{f_{ac}} + \frac{1}{2} \cdot \frac{1}{f_{ac}} \cdot \frac{ASIN\left(\frac{\sqrt{\frac{2}{C_{busHoldUP}} \cdot t_{HoldUp} \cdot \frac{P_{outNom}}{Eta_{HFB}} + V_{busMinAbs}^{\ 2}}}{V_{busHoldUpIni}} \right)}{\pi} + t_{HoldUp} \right)$$

- No direct solution for the $C_{busMinHoldUp}$ ➔ Goal seek used in the calculation sheet
  - t_{HoldUp} for the hold-up time as input
  - Select the starting point $V_{busHoldUpIni}$ for the hold-up time calculation
    - $V_{acMinPk}$ or $V_{busTargetHFB}$
  - $V_{busMinAbs} = \frac{N \cdot V_{outNom}}{D_{Max}}$ as the absolute minimum bus voltage before bus UVP
  - $C_{busMinHoldUp}$ as input value for the goal seek
    1. Set $C_{BusMinHoldUp}$ (cell R37) to 1
    2. Go to ***Data\What-If analysis\Goal seek***
    3. Set the condition accordingly
    4. Clicking on **OK** button, the $C_{BusMinHoldUp}$ will be calculated







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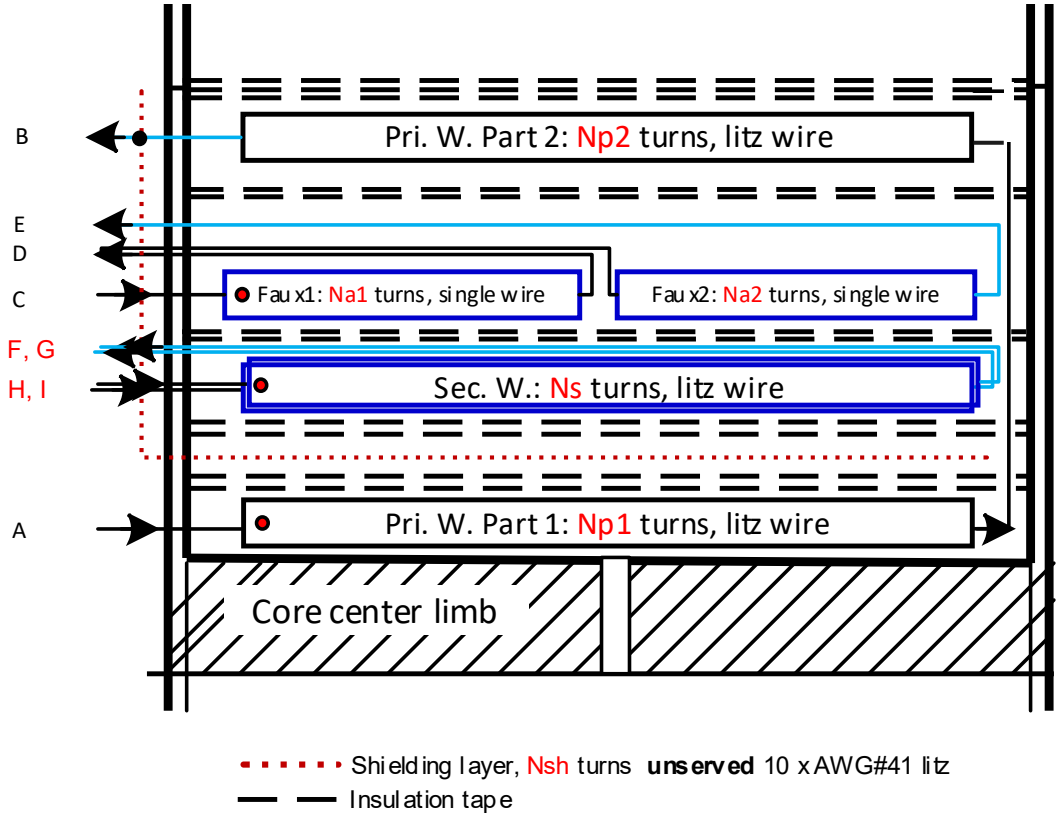
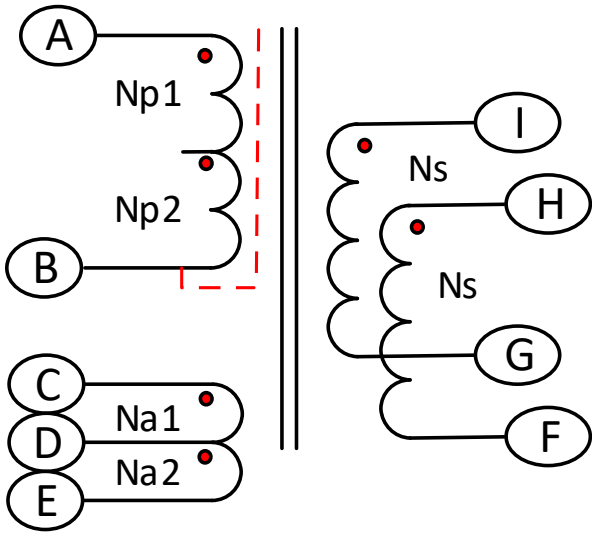
Transformer construction

- Sandwitch structure recommended
- Benefitial of an inner shielding layer on the EMI performance





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Revision history

- V1.0.0
  - Updated according to the design tool V1.0.0
- V0.2.0
  - Updated based on the design tool V0.2.0
- V0.1.0
  - Initial release

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