

XDPS2201E System Design Guide
- Design tool V1.0.0

Dr. J. Hu

Overview

- Introduction
  - Application schematic
  - XDPS2201E operating principle

- Excel design tool
  - XDPS2201E_DesignSheet_V100_RC01.xlsx
  - V1.0.0

- System design guide
  - Design flow
  - System level
    - Input and output specification
    - R_{HV}
    - MFIO functionality and parameters
  - Hybrid flyback (HFB) stage
    - Main components, ZCD circuit, CS circuit, VS divider, VCC supply circuit
    - Construction of the transformer

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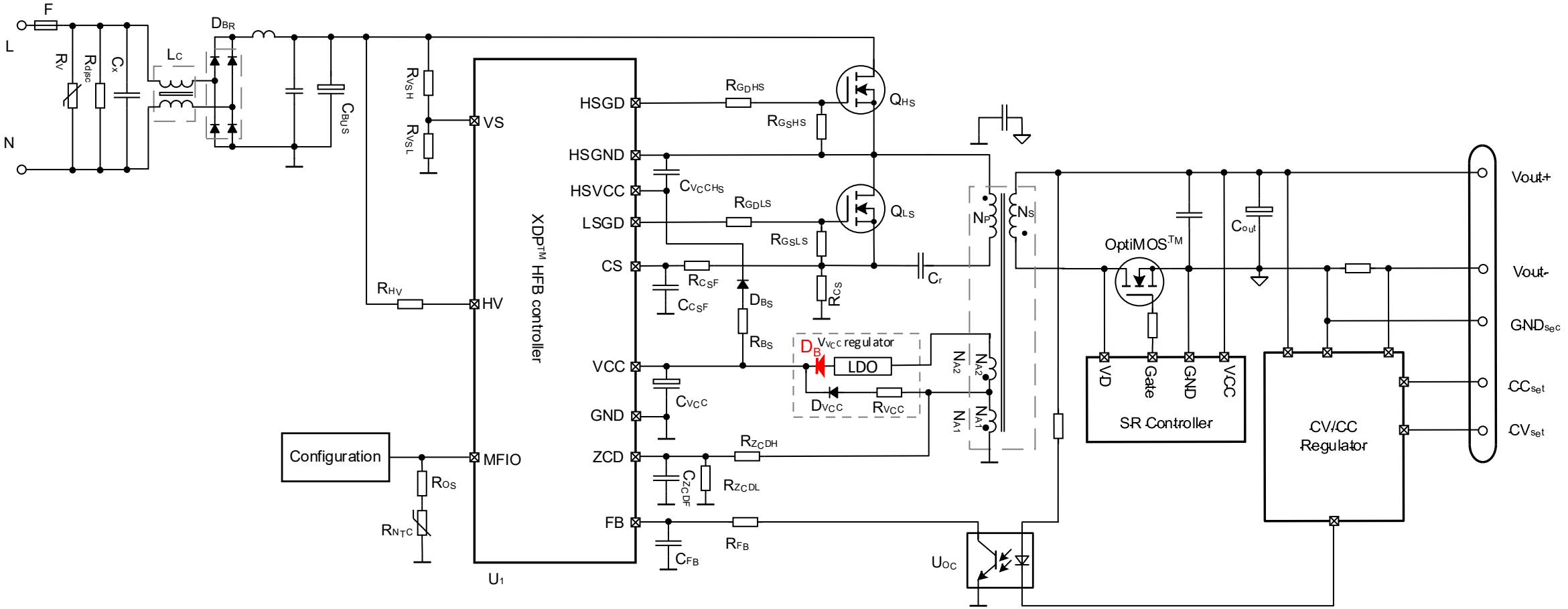
Introduction
- Application with CoolMOS™ switches



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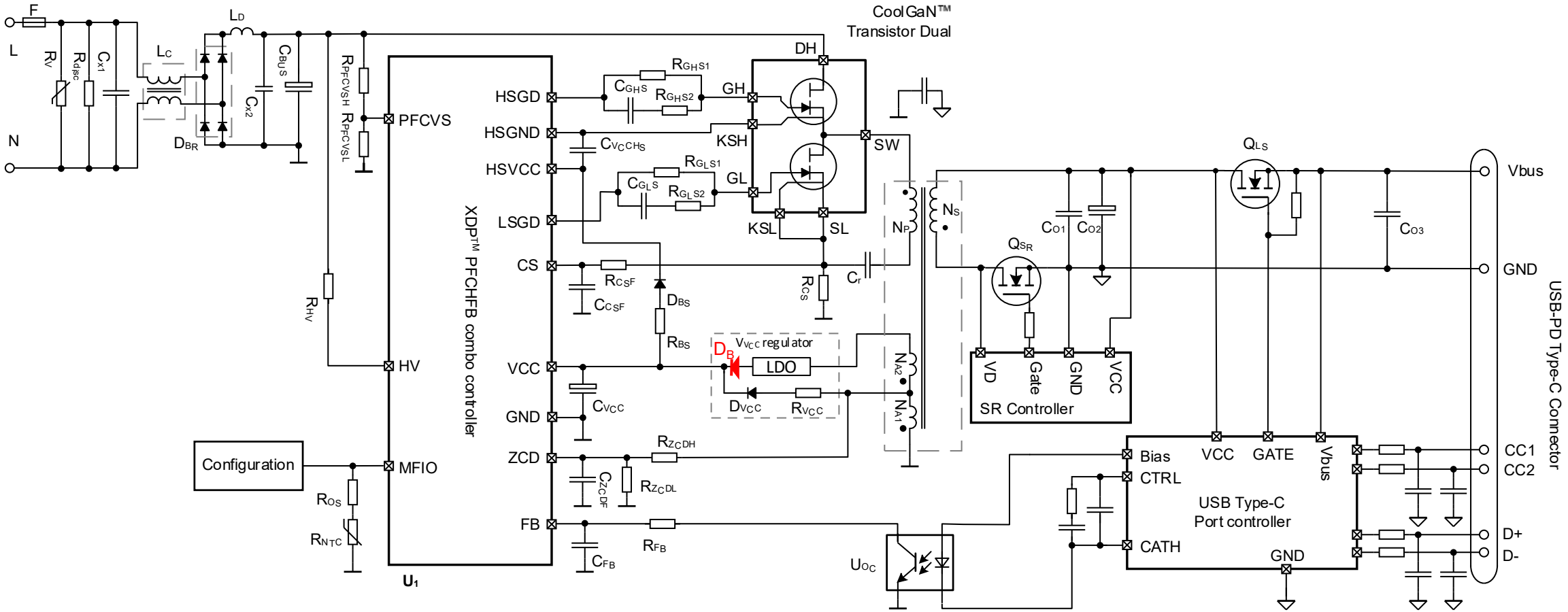
Introduction
- Application with CoolGaN™ Dual switches



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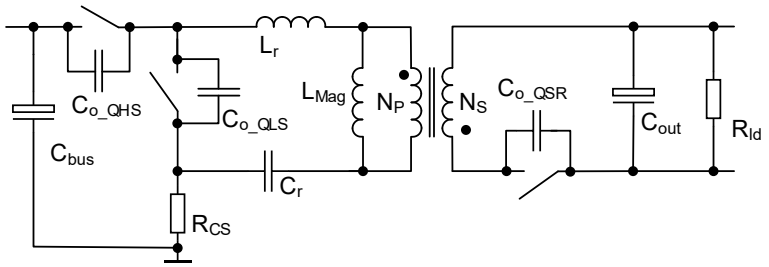
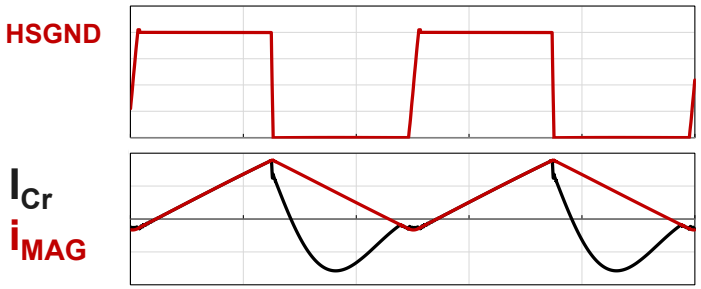
Introduction
- HFB operating principle

– **Circuit**

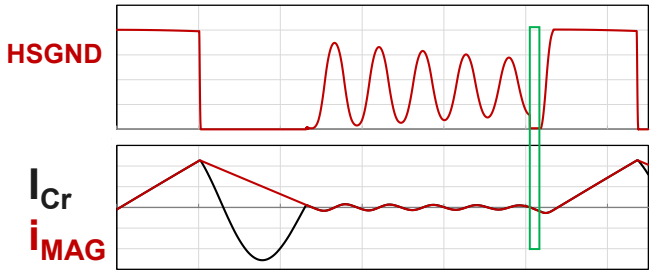


– **Operating principle**
  – Peak current control with fast response
  – Valley switching with ZVS operation for good efficiency
  – Linear increasing primary current during HS on-time and resonant current during LS on-time

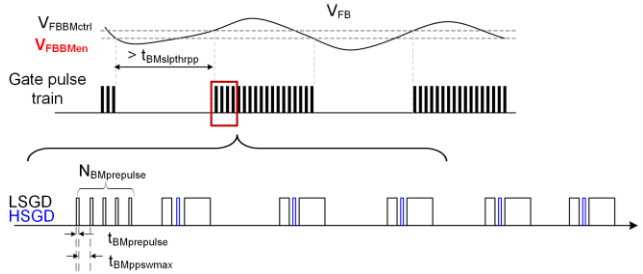
– **Non-burst operation**
  – **CRM**: Continuous Resonant Mode at high load condition



  – **ZV-RVS**: Zero Voltage – Resonant Voltage Switching at low and lighter load condition, with ZVS pulse for ZV turn-on of the HS switch



– **Burst mode operation**
  – Burst on- and off-phase based on the HFB V_{FB}



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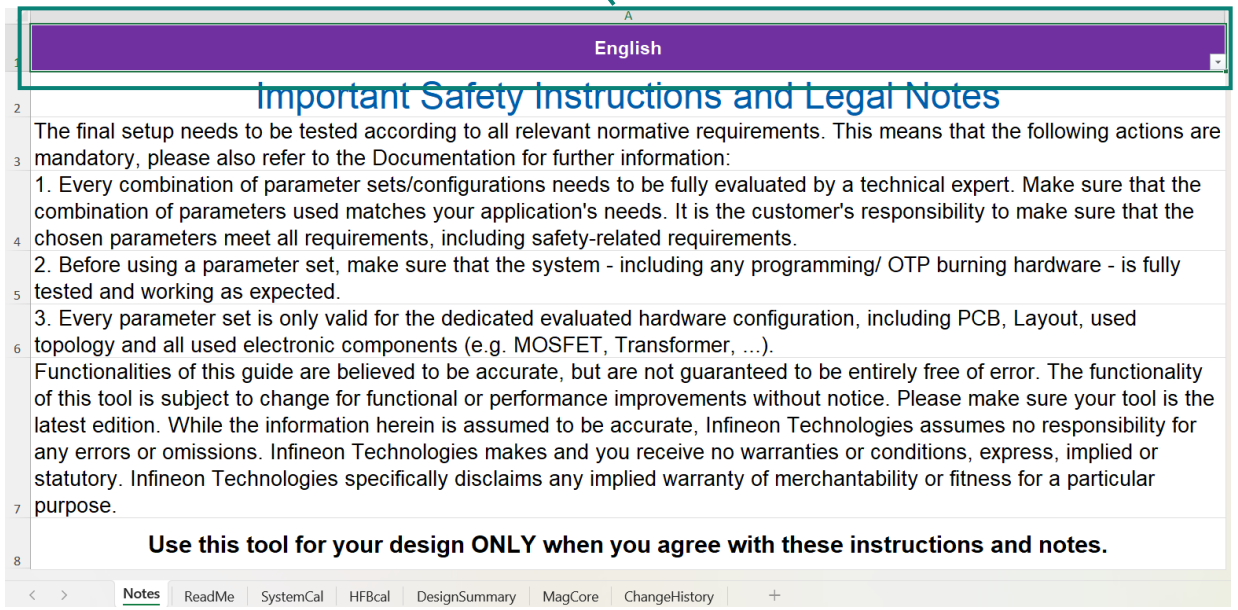
Excel design tool
- Overview

- Design tool reference
  - XDPS2201E_DesignSheet_V100_RC01.xlsx
  - Microsoft Excel version **2013** or later required
- Design workbook structure
- Cell color index
- Design sheets and steps
- Design flow
- System design
- HFB design

- Tool supported language
  - English and Chinese
  - Selectable per A1 on the Sheet Notes



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Excel design tool
- Structure

Important notes

How to use the design sheet

Ferrite core parameters

Notes | ReadMe | SystemCal | HFBcal | DesignSummary | MagCore | ChangeHistory

Main calculation

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	170W BPA
1 Input specification						
Input voltage doubler used	VinDouber	Not used				Not used
AC RMS min	VacMin	180			V	180.0
AC RMS max	VacMax	264			V	264.0
AC frequency	fac	50	47	63	Hz	50.0
Brown-in level	VinBi	260		254.56	V	260.0
Brown-out level	VinBo	240	0	260.00	V	240.0

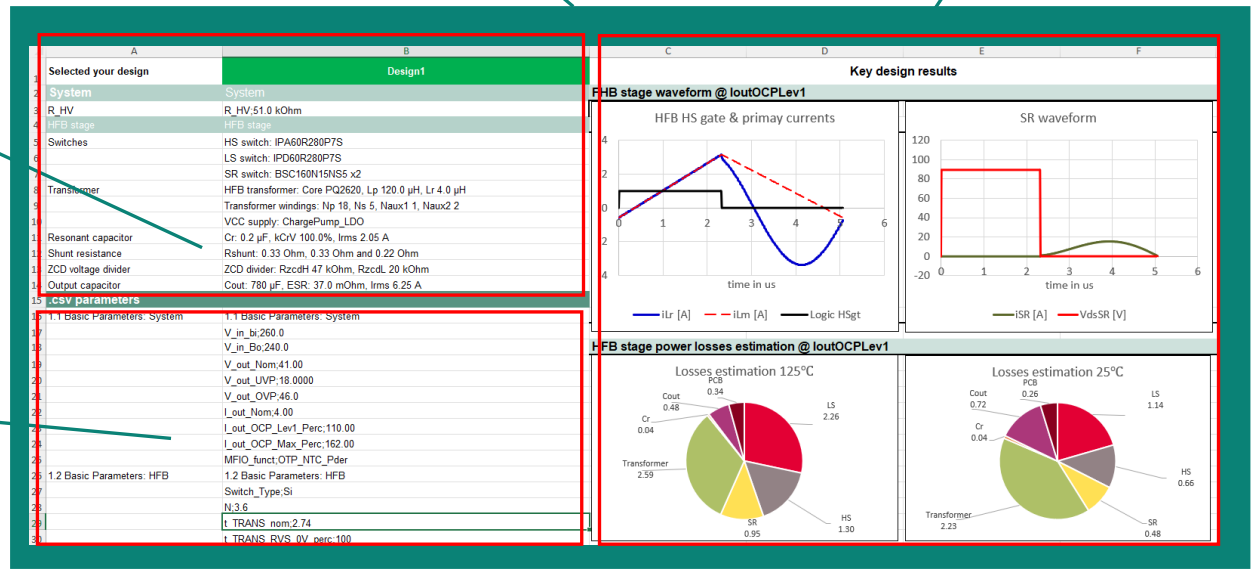
Assistant calculation, design recommendation and information

ADC_MFIO2_RANGE	2.428	V	IAG_neg_max_perc	40	%
DAC_RANGE	0.437	V			
ADC_MFIO2_RANGE_THR_MAX	2.33	V			
ADC_VS_RRANGE	2.751	V	V_FB_OP_min	0.44	V
ADC_Vzcd_RANGE_THR_MAX	2.75	V	P_max_Hlimit_perc	200	%

Design results/estimation

Components

Parameters



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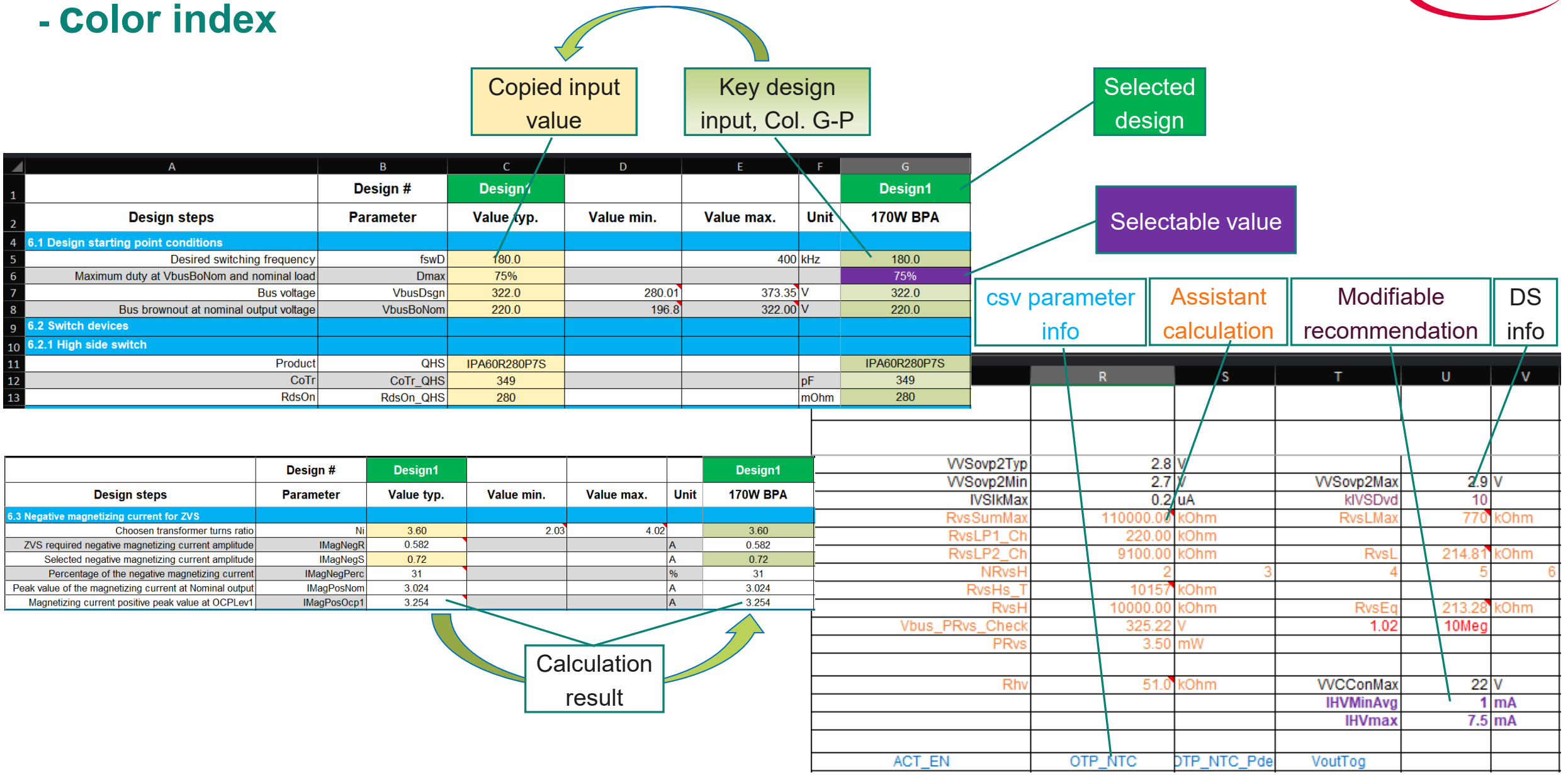
Excel design tool
- Color index



	A	B	C	D	E	F	G
1		Design #	Design1				Design1
2	Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	170W BPA
4	6.1 Design starting point conditions						
5	Desired switching frequency	fswD	180.0		400	kHz	180.0
6	Maximum duty at VbusBoNom and nominal load	Dmax	75%				75%
7	Bus voltage	VbusDsgn	322.0	280.01	373.35	V	322.0
8	Bus brownout at nominal output voltage	VbusBoNom	220.0	196.8	322.00	V	220.0
9	6.2 Switch devices						
10	6.2.1 High side switch						
11	Product	QHS	IPA60R280P7S				IPA60R280P7S
12	CoTr	CoTr_QHS	349			pF	349
13	RdsOn	RdsOn_QHS	280			mOhm	280

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	170W BPA
6.3 Negative magnetizing current for ZVS						
Choosen transformer turns ratio	Ni	3.60	2.03	4.02		3.60
ZVS required negative magnetizing current amplitude	IMagNegR	0.582			A	0.582
Selected negative magnetizing current amplitude	IMagNegS	0.72			A	0.72
Percentage of the negative magnetizing current	IMagNegPerc	31			%	31
Peak value of the magnetizing current at Nominal output	IMagPosNom	3.024			A	3.024
Magnetizing current positive peak value at OCPLev1	IMagPosOcp1	3.254			A	3.254

	R	S	T	U	V
VVSovp2Typ	2.8	V			
VVSovp2Min	2.7	V	VVSovp2Max	2.9	V
IVSIkMax	0.2	uA	kIVSDvd	10	
RvsSumMax	110000.00	kOhm	RvsLMax	770	kOhm
RvsLP1_Ch	220.00	kOhm			
RvsLP2_Ch	9100.00	kOhm	RvsL	214.81	kOhm
NRvsH	2	3	4	5	6
RvsHs_T	10157	kOhm			
RvsH	10000.00	kOhm	RvsEq	213.28	kOhm
Vbus_PRvs_Check	325.22	V	1.02	10Meg	
PRvs	3.50	mW			
Rhv	51.0	kOhm	VVCConMax	22	V
			IHVMinAvg	1	mA
			IHVmax	7.5	mA
ACT_EN	OTP_NTC	OTP_NTC_Pde	VoutTog		

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Excel design tool
- Design sheets and steps

- Sheet systemCal
  - Select the specific design at the cell C1
  - Selected design valid through the sheets SystemCal and HFBcal, and highlighted on the first row
  - System level design
- Sheet HFBcal
  - HFB stage design
- Sheet MagCore
  - Ferrite core information
  - Extendable for customized core, the values in column B to D are mandatory
- Sheet DesignSummary
  - Design results summarized on the page once design done
  - Cells B2 to B14: Hardware components which can be copied to a text editor and saved for hardware design
  - Cells B16 to B45: csv parameters which can be copied to a text editor, saved and imported by dp vision 2.1.3.7 or later version

- Design steps on the same page
  - Top-down, otherwise any missing input may cause Excel calculation error, such as divided by zero

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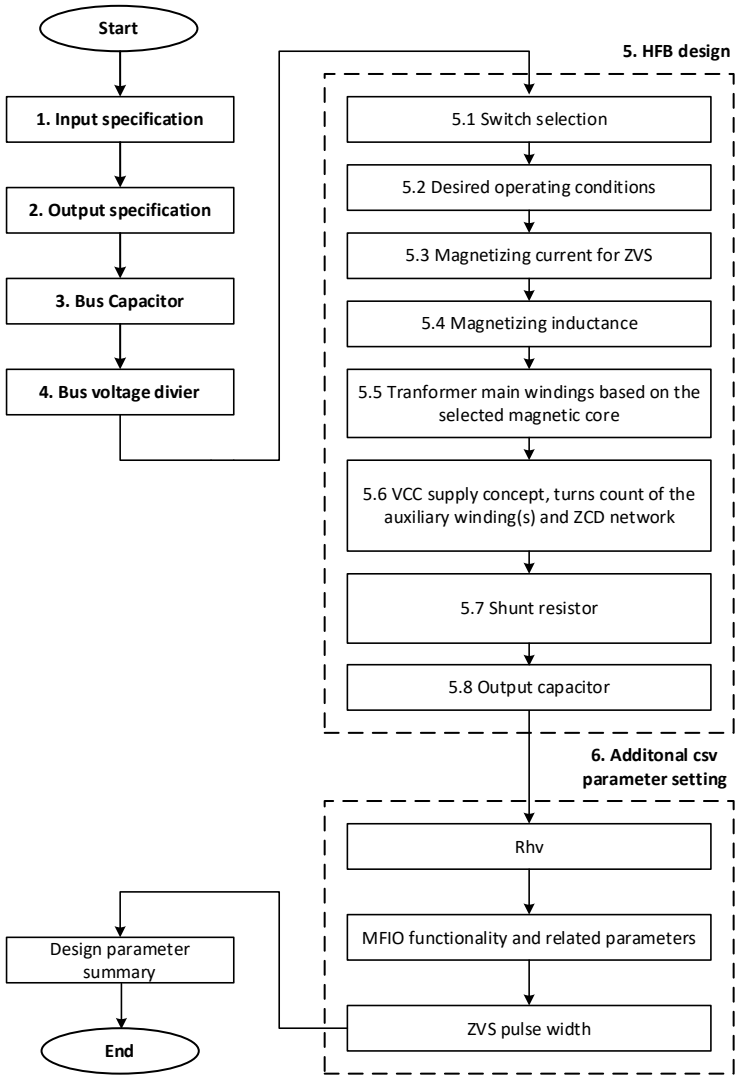
Design flow



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System level
- Overview

1. Input specification
   - AC voltage and frequency, or
   - DC
2. HFB output specification
   - Output voltage level(s)
   - Output current levels
3. Bus capacitor and bus voltage divider
4. R_{hv}
5. MFIO functionality and the related parameter

Design steps	Design # Parameter	Design1 Value typ.
1 Input specification		
Input voltage options	VinOption	VAC
AC RMS min	VacMin	198
AC RMS max	VacMax	264
AC frequency	fac	50
Brown-in level	VinBi	240
Brown-out level	VinBo	220
2 HFB output specification		
Nominal output voltage maximum	VoutNom	41
Output under voltage level	VoutUVP	18
Output over voltage level	VoutOVP	46
Nominal output current	IoutNom	4.15
Output lower overcurrent protection threshold	IoutOCPLev1Perc	110
Output maximum overcurrent protection threshold	IoutOCPMaxPerc	162
HFB efficiency at the nominal condition	EtaHFB	94.0%
3. Bus capacitor and bus voltage divider		
Bus capacitance	CbusC	190
Bus capacitor(s) rated voltage min	CbusRVmin	400
Divider ratio (RvsH+RvsL)/RvsL target	kvs	142.86
realized OVP level	VbusOVP	380
1st resistor at lowside	RvsLP1_Base	2.2
	RvsLP1_Factor	100k
parallel resistor at lowside , optional	RvsLP2_Base	9.1
	RvsLP2_Factor	1Meg
Number of in-series connected highside resistors	NRvsH	3
Resistance of the single highside resistor	RvsH_Base	1
	RvsH_Factor	10Meg
kVS design error	kvsDE	1.54%
VS filter capacitance proposal	Cvs	330
4 Rhv		
	Rhv1	27.0
	Rhv2	24.0
	Rhv3	0.0
5 MFIO function		
	MFIO_funct	OTP_NTC_Pder
	R_MFIO_OTP_trig	1.85
	R_MFIO_OTP_rel	11.75
	N_OTP_ev_max	2

Selected current design

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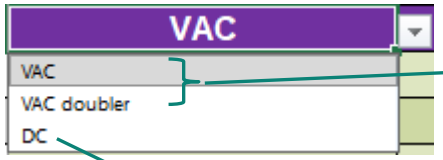
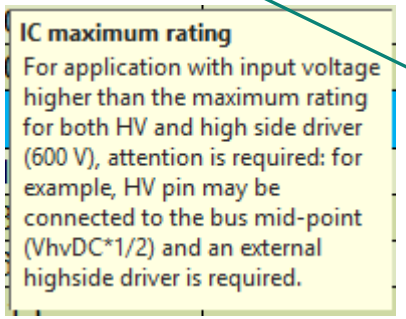
System level
- Input specification

- VinOption



  - Attention required for the DC input higher than 600 V



- V_{acMin}, V_{acMax} as AC input RMS values
- Brown-in and -out setting
  - Brown-in and –out level at the bus capacitor
  - $V_{inBiMax} = \sqrt{2} * V_{acMin}$
  - $V_{inBoMax} = V_{inBi}$

Design steps	Design # Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 170W BPA
1 Input specification						
Input voltage options	VinOption	VAC				VAC
AC RMS min	VacMin	198			V	198.0
AC RMS max	VacMax	264			V	264.0
AC frequency	fac	50	47	63	Hz	50.0
Brown-in level	VinBi	240		280.01	V	240.0
Brown-out level	VinBo	220	196.8	240.00	V	220.0

Design steps	Design # Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 170W BPA	Des
1 Input specification							
Input voltage options	VinOption	DC				DC	
DC voltage min	VDCmin	300			V	300.0	
DC voltage max	VDCmax	1200	300		V	1200.0	
Brown-in level	VinBi	240		1200.00	V	24	
Brown-out level	VinBo	220	196.8	240.00	V	22	
2 HFB output specification							
Nominal output voltage maximum	VoutNom	41	0		V	41	
Output under voltage level	VoutUVP	18			V	18	
Output over voltage level	VoutOVP	46	41		V	46	
Nominal output current	IoutNom	4.15	0.001		A	4	

IC maximum rating
For application with input voltage higher than the maximum rating for both HV and high side driver (600 V), attention is required: for example, HV pin may be connected to the bus mid-point (VhvDC*1/2) and an external highside driver is required.

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System level
- Output specification

- HFB output
  - Output voltage level(s)
  - Output current levels
  - Min and max limit
    - $V_{outOVPMin} = V_{outNom}$
    - $I_{outOCPMaxPercMin} = I_{outOCPLev1Perc}$

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	170W BPA
2 HFB output specification						
Nominal output voltage maximum	VoutNom	41	0		V	41.0
Output under voltage level	VoutUVP	18			V	18.0
Output over voltage level	VoutOVP	46	41		V	46.0
Nominal output current	IoutNom	4.15	0.001		A	4.15
Output lower overcurrent protection threshold	IoutOCPLev1Perc	110	100	162	%	110.0
Output maximum overcurrent protection threshold	IoutOCPMaxPerc	162	110	200	%	162.0
HFB efficiency at the nominal condition	EtaHFB	94.0%				94.0%

- Estimated HFB efficiency EtaHFB

- Additional calculation
  - VoutVzcdRatio

VoutVzcdRatio	16.727
PoutNom	164 W

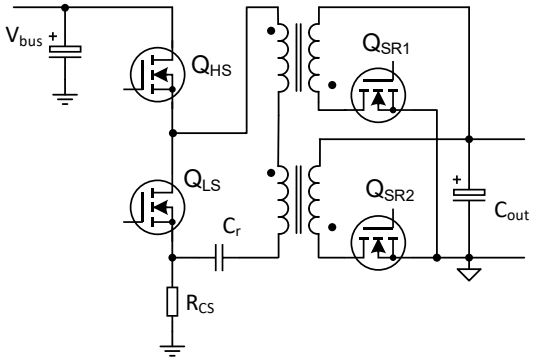
$$k_{VoutVzcd} = \frac{V_{outOVP}}{V_{zcdOVP2}} = \frac{V_{outOVP}}{ADC_Vzcd_Rang_THR_max}$$

  - Output nominal power

$$P_{outNom} = I_{outNom} * V_{outNom}$$

- Proposal for high output current applications

High output current applications
i.e., > 7 A, two-transformer solution is recommended: 1) primary windings (half of the calculated turns Np) in series and secondary windings (same of the calcualted turns Ns) in parallel; 2) core integration + flux cancelling helps to improve efficiency.



- Though more cost than the single-transformer solution, but still lower cost than solution of LLC+buck for applications of wide output voltage

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System level
- Bus capacitor and bus voltage divider

- Bus capacitor
  - Rated voltage minimum CbusVRmin
    - VinOption = VAC
      - $\sqrt{2}V_{acMax}$
    - VinOption = VAC doubler
      - $2\sqrt{2}V_{acMax}$
    - DC input
      - VdcMax
  - Capacitance minimum
    - $C_{busCMin} = \left[\frac{1}{2} + \frac{ASIN\left(\frac{V_{inBo}}{\sqrt{2}*V_{acMin}}\right)}{\pi}\right] * \frac{P_{outNom}}{EtaHFB} * \frac{1}{f_{acMin}} * \frac{1}{2*V_{acMin}^2 - N_{inBo}^2} * 10^6$

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	170W BPA
3. Bus capacitor and bus voltage divider						
Bus capacitance	CbusC	190	75		uF	190
Bus capacitor(s) rated voltage min	CbusRVmin	400	373		V	400.00
Divider ratio (RvsH+RvsL)/RvsL target	kvs	142.86	137.93	148.15		142.86
realized OVP level	VbusOVP	380	366.43	393.57	V	380.00
1st resistor at lowside	RvsLP1_Base	2.2			kOhm	2.20
	RvsLP1_Factor	100k				100k
parallel resistor at lowside , optional	RvsLP2_Base	9.1			kOhm	9.10
	RvsLP2_Factor	1Meg				1Meg
Number of in-series connected highside resistors	NRvsH	3				3.00
Resistance of the single highside resistor	RvsH_Base	1	10200	10200	kOhm	1.00
	RvsH_Factor	10Meg				10Meg
kVS design error	kvsDE	1.54%				1.54%
VS filter capacitance proposal	Cvs	330		373	pF	330

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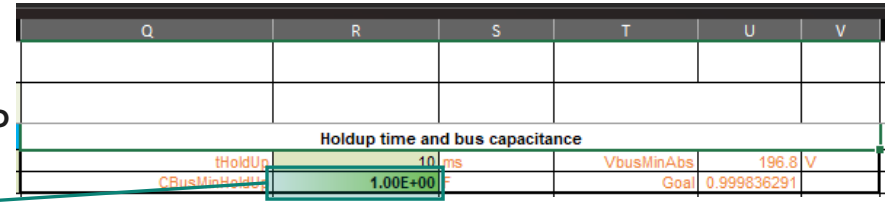
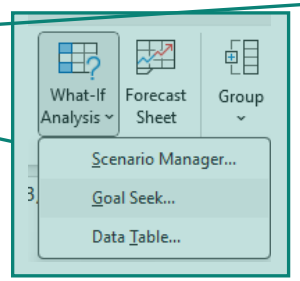
System level
- Bus capacitance and hold-up time

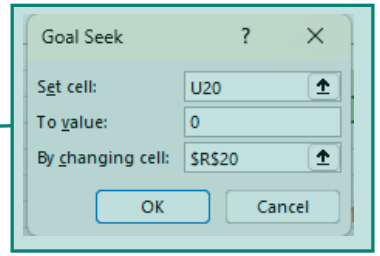
- Some application requesting hold-up time (t_{HoldUP}) ➔ requesting higher bus capacitance
- This requested bus capacitance calculated by

$$C_{busHoldUp} = \frac{2}{V_{acMinPk}{}^2 - V_{busMinAbs}{}^2} \cdot \frac{P_{outNom}}{Eta_{HFB}} \cdot \left(\frac{1}{4} \cdot \frac{1}{f_{ac}} + \frac{1}{2} \cdot \frac{1}{f_{ac}} \cdot \frac{ASIN\left(\frac{\sqrt{\frac{2}{C_{busHoldUP}} \cdot t_{HoldUp} \cdot \frac{P_{outNom}}{Eta_{HFB}} + V_{busMinAbs}{}^2}}{V_{acMinPk}} \right)}{\pi} + t_{HoldUp} \right)$$

- No direct solution for the $C_{busMinHoldUp}$ ➔ Goal seek used in the calculation sheet
  - t_{HoldUp} for the hold-up time as input
  - $V_{busMinAbs} = \frac{N \cdot V_{outNom}}{D_{Max}}$ as the absolute minimum bus voltage before bus UVP
  - $C_{busMinHoldUp}$ as input value for the goal seek
    1. Set $C_{BusMinHoldUp}$ initial value in cell R20), i.e., to 1
    2. Go to ***Data\What-If analysis\Goal seek***
    3. Set the condition accordingly
    4. Clicking on **OK** button, the $C_{BusMinHoldUp}$ will be calculated







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System level
- Bus voltage divider (1/2)

- Bus voltage divider ratio
  - $k_{vs} = {}^{V_{busCapRVmin}}/_{V_{VvsOVP2Typ}}$
  - The min and max calculated by
    - $k_{vsMin} = {}^{V_{busCapRVmin}}/_{V_{VvsOVP2Max}}$
    - $k_{vsMax} = {}^{V_{busCapRVmin}}/_{V_{VvsOVP2Min}}$

V_{vsOVP2}: HW comparator threshold

- Resulted min and max of the bus OVP levels based on the divider ratio k_{vs} and the input $V_{busOVP2Min}$ and $V_{busOVP2Max}$
  - $V_{busOVPMin} = k_{vs} * V_{busOVP2Min}$
  - $V_{busOVPMax} = k_{vs} * V_{busOVP2Max}$

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	170W BPA
3. Bus capacitor and bus voltage divider						
Bus capacitance	CbusC	190	75		uF	190
Bus capacitor(s) rated voltage min	CbusRVmin	400	373		V	400.00
Divider ratio (RvsH+RvsL)/RvsL target	kvs	142.86	137.93	148.15		142.86
realized OVP level	VbusOVP	380	366.43	393.57	V	380.00
1st resistor at lowside	RvsLP1_Base	2.2			kOhm	2.20
	RvsLP1_Factor	100k				100k
parallel resistor at lowside , optional	RvsLP2_Base	9.1			kOhm	9.10
	RvsLP2_Factor	1Meg				1Meg
Number of in-series connected highside resistors	NRvsH	3				3.00
Resistance of the single highside resistor	RvsH_Base	1	10200	10200	kOhm	1.00
	RvsH_Factor	10Meg				10Meg
kVS design error	kvsDE	1.54%				1.54%
VS filter capacitance proposal	Cvs	330		373	pF	330

VVSovp2Typ	2.8	V		
VVSovp2Min	2.7	V	VVSovp2Max	2.9 V

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System level
- Bus voltage divider (2/2)

- Maximum of the total divider resistance calculated based on
  - VS pin leakage current $I_{VSIkMax}$, and
  - Factor of the current through the divider over the leakage current k_{IVSDvd}
  - $R_{vsSumMax} = V_{inBo}/(k_{IVSDvd} * I_{VSIkMax})$
- Maximum of the equivalent resistance of the divider low-side resistor(s)
  - $R_{svLMax} = R_{VSsumMax}/k_{vsDsgn}$
- Desired value of the high-side single resistor calculated based the selected number of the high-side resistors N_{RvsH}
  - $R_{vsHDesired} = (k_{vsDsgn} - 1) * R_{vsL}/N_{RvsH}$
  - The best match resistance calculated as R_{vsH} min and max
  - Design error k_{vs_DE} calculated based on the chosen value of R_{vsH_Base} and R_{vsH_Factor}

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	170W BPA
3. Bus capacitor and bus voltage divider						
Bus capacitance	CbusC	190	75		uF	190
Bus capacitor(s) rated voltage min	CbusRVmin	400	373		V	400.00
Divider ratio (RvsH+RvsL)/RvsL target	kvs	142.86	137.93	148.15		142.86
realized OVP level	VbusOVP	380	366.43	393.57	V	380.00
1st resistor at lowside	RvsLP1_Base	2.2			kOhm	2.20
	RvsLP1_Factor	100k				100k
parallel resistor at lowside , optional	RvsLP2_Base	9.1			kOhm	9.10
	RvsLP2_Factor	1Meg				1Meg
Number of in-series connected highside resistors	NRvsH	3				3.00
Resistance of the single highside resistor	RvsH_Base	1	10200	10200	kOhm	1.00
	RvsH_Factor	10Meg				10Meg
kVS design error	kvsDE	1.54%				1.54%
VS filter capacitance proposal	Cvs	330		373	pF	330

VVSovp2Typ	2.8	V			
VVSovp2Min	2.7	V	VVSovp2Max	2.9	V
IVSIkMax	0.2	uA	kIVSDvd	10	
RvsSumMax	122500.00	kOhm	RvsLMax	857.5	kOhm
RvsLP1_Ch	220.00	kOhm			
RvsLP2_Ch	9100.00	kOhm	RvsL	214.81	kOhm
NRvsH	2	3	4		
RvsHs_T	10157	kOhm			
RvsH	10000.00	kOhm	RvsEq	213.28	kOhm

- R_{vsLP1_Ch} and R_{vsLP2_Ch}
  - Both the base and the factor should be chosen, otherwise it is considered as open (not existing)
- R_{vsL} as the equivalent resistance of the chosen low-side resistors R_{vsLP1_Ch} and R_{vsLP2_Ch}
- A filter capacitance recommended
  - Maximum limit by a corner frequency of 20 kHz

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System level
- R_{hv}

- Functionality of the resistor at the HV pin R_{hv}
  - Delivering the charging current for the VCC capacitor initial charge-up
  - Limiting the maximum current flowing into the HV pin
  - Reducing the thermal stress for the start-up cell
- Limits of the R_{hv}
  - Minimum value
    - Maximum current at maximum line voltage

$$R_{hvMin} = \frac{\sqrt{2} * V_{acMax}}{I_{hvMax}}$$

with I_{hvMax} at 7.5 mA

  - Maximum value
    - Offering enough charging current for the VCC capacitor

$$R_{hvMax} = MIN\left\{10^5, \frac{V_{acMinRecAvg} - V_{vccOnMax}}{I_{hvMinAvg}} * \left[1 - \frac{2}{\pi} * \sin^{-1}\left(\frac{V_{vccOnMax}}{V_{acMinPk}}\right)\right]\right\}$$

with $I_{hvMinAvg}$ at 1 mA and $V_{acMinRecAvg}$ of 0.9*V_{acMin}

- To be considered
  - Two or three resistors in series
  - Voltage rating of the resistors
  - Recommended to be connected after the AC bridge rectifier
  - One small capacitor, i.e. 100 pF, at the HV pin to reduce the voltage stress at the pin at lightning surge

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	170W BPA
Rhv					kOhm	
	Rhv1	27.0	49.8	100.0	kOhm	27
	Rhv2	24.0			kOhm	24
	Rhv3	0.0			kOhm	

Rhv	51.0	kOhm	VVCConMax	22 V
			IHVMinAvg	1 mA
			IHVmax	7.5 mA

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System level
- MFIO pin functionality

- Multi functionality integrated by using the MFIO pin
  - ACT_EN
    - Toggling depending on IC state of **burst sleep or not**
    - User case: to control the active bridge
  - OTP_NTC
    - Using **external NTC** for overtemperature protection
  - OTP_NTC_Pder
    - Using **external NTC** for overtemperature protection and temperature dependent **power foldback**
  - Vout_Tog
    - Toggling depending on **output voltage level**
- Pin internal setting and related parameters
  - Some internal setting depending on the selected functionality
  - Only the configured functionality active

Design steps	Design #	Design1				Design1
	Parameter	Value typ.	Value min.	Value max.	Unit	170W BPA
5 MFIO function						
	MFIO_funct	OTP_NTC_Pder				OTP_NTC_Pder
	R_MFIO_OTP_trig	1.85			kOhm	1.85
	R_MFIO_OTP_rel	11.75	1.85		kOhm	11.75
	N_OTP_ev_max	2				2

MFIO_funct	ACT_EN	ACT_EN

MFIO_funct	OTP_NTC		OTP_NTC
R_MFIO_OTP_trig	1.85	kOhm	1.85
R_MFIO_OTP_rel	11.75	kOhm	11.75
N_OTP_ev_max	2		2

MFIO_funct	VoutTog		VoutTog
V_out_MFIO_goL	16.0	V	16.0
V_out_MFIO_goH	7.0	V	7.0

	Remark	MFIO _func			
Options		ACT_EN	OTP_NTC	VoutTog	OTP_NTC_Pder
Inner supply		VDDP	VREF	VDDP	VREF
Vout	Vout below V_out_MFIO_goL			Low	
	Vout above V_out_MFIO_goH			PU=2.25K	
Operation	Not BM sleep	High	PU=11K		PU=11K
	BM sleep	High-Z	High-Z	High-Z (Case A) PU=2.25K (Case B)	High-Z
OCP	Iset OCP Max	Enabled	Enabled	Enabled	Power foldback
	Iset OCP Lev1	Enabled	Enabled	Enabled	Disabled
Parameters			$R_{MFIO_OTPtrig}$	$V_{out_MFIOgoL}$	$R_{MFIO_OTPtrig}$
			R_{MFIO_OTPrel}	$V_{out_MFIOgoH}$	R_{MFIO_OTPrel}
			$N_{OTPevMax}$		$N_{OTPevMax}$

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HFB design
- Overview

- HFB operating process
- Desired conditions as design starting point
- Switch devices
- Negative magnetizing current for ZVS
- Transformer
  - Magnetizing inductance and resonant tank
  - Main windings
  - VCC supply and auxiliary winding(s)
- Shunt resistance
- Output capacitance
- Additional csv parameter setting
  - Mode transition voltage
  - ZVS pulse width
  - PCB trace resistance for power losses estimation

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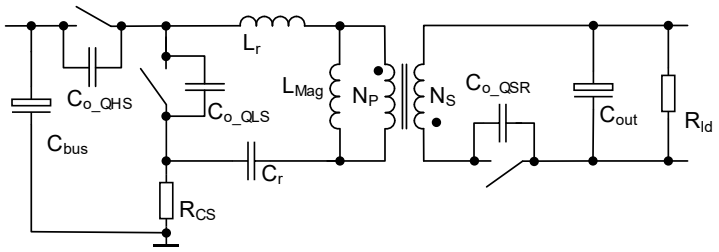
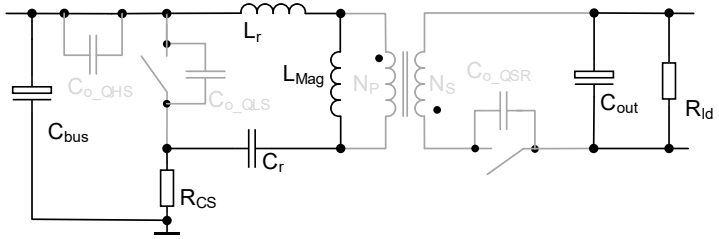
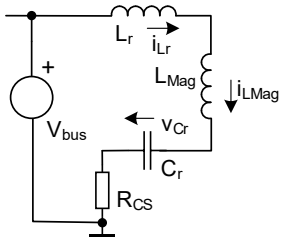
HFB design
- HFB operating process

1

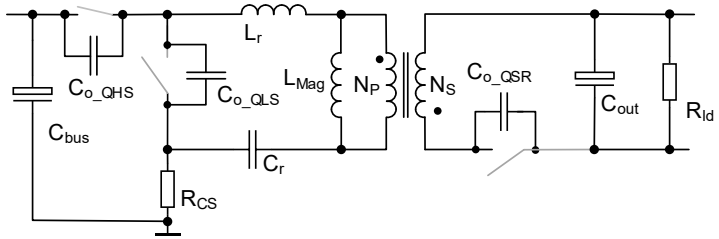


2

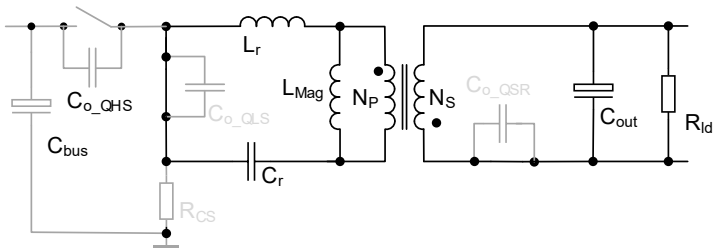


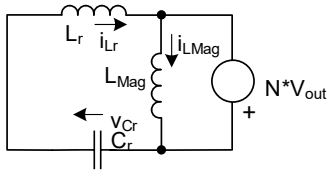


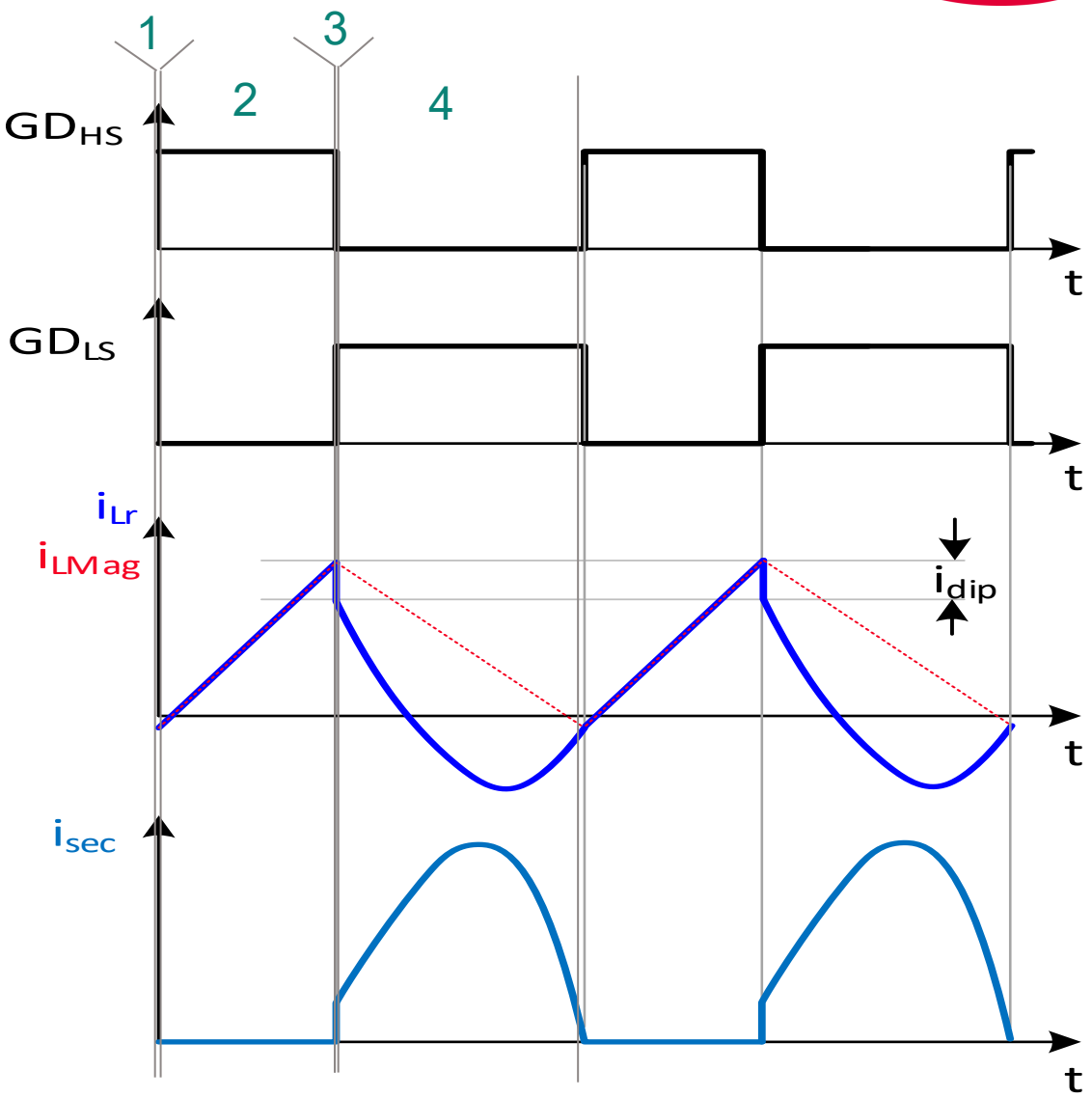
3



4







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HFB design
- Desired conditions as design starting point

- f_{swD}: desired HFB switching frequency at the nominal load and $V_{busDsgn}$
  - Upper limit around 400 kHz
- D_{max}: Maximum duty at $V_{busBoNom}$ and nominal load
  - 66% ➔ k_tHS_limit = 2, or
  - 75% ➔ k_tHS_limit = 3
  - Higher duty allowing low $V_{busBoNom}$ = possible with smaller bus capacitor
  - k_tHS_limit derived for .csv file
- $V_{busDsgn}$: Bus voltage level at the nominal output load
  - Minimum: $SQRT(2) * V_{axMin}$ or V_{DCmin}
  - Maximum: $SQRT(2) * V_{axMax}$ or $VDCm_{ax}$
- $V_{busBoNom}$: Bus voltage brown-out level at the nominal output voltage
  - Maximum: $V_{busDsgn}$

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	170W BPA
6 HFB design						
6.1 Design starting point conditions						
Desired switching frequency	fswD	180.0		400	kHz	180.0
Maximum duty at VbusBoNom and nominal load	Dmax	75%				75%
Bus voltage	VbusDsgn	322.0	280.01	373.35	V	322.0
Bus brownout at nominal output voltage	VbusBoNom	220.0	196.8	322.00	V	220.0
					TswD	5.56 µs
					k_tHS_limit	3

- Additional calculation
  - HFB switching period at the given switching frequency
    - $T_{swD} = 1/f_{swD}$
  - $V_{busBoNom}$ minimum
    - To be checked after design finished
    - $V_{busUVP} = N \cdot \frac{V_{outNom}}{D_{max}}$
    - $V_{busBoNum} \geq V_{busUVP}$ for proper operation

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HFB design
- Switch devices

- Both GaN and Si MOFET supported

- Important parameters
  - Capacitance
    - $C_{o(tr)}$ of the selected Q_{HS} and Q_{LS} switches
    - C_{oss} of the SR device
    - Impact on
      - Negative magnetizing current setting for ZVS
      - Maximum negative magnetizing current limit
  - R_{dson} used for the power losses estimation

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	**170W BPA**
6.2 Switch devices						
6.2.1 High side switch						
Product	QHS	IPA60R280P7S				IPA60R280P7S
CoTr	CoTr_QHS	349			pF	349
RdsOn	RdsOn_QHS	280			mOhm	280
6.2.2 Low side switch						
Product	QLS	IPA60R280P7S				IPA60R280P7S
CoTr	CoTr_QLS	349			pF	349
RdsOn	RdsOn_QLS	280			mOhm	280
6.2.3 2nd side rectifier						
Type of the 2nd side rectifier	Type_2ndRect	SR				SR
SR switch	QSR	BSC160N15NS5				BSC160N15NS5
Rated voltage	Vds_QSR	150			V	150
Voltage derating factor of the 2nd side rectifier	kVdr_2ndRect	0.8				80%
Number of the SR switches in parallel	N_QSR	2			piece	2
Coss of the SR switch	Coss_QSR	340			pF	340
RdsOn	RDSonMax_QSR	16			mOhm	16
Qg	Qg_QSR	19			nC	19

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HFB design
- 2nd side rectifier

- Either SR FET or diode
- $k_{Vds_2ndRect}$
  - Voltage derating factor for the secondary side rectifier
  - Recommendation: beginning with 0.8

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	**170W BPA**
6.2 Switch devices						
6.2.1 High side switch						
Product	QHS	IPA60R280P7S				IPA60R280P7S
CoTr	CoTr_QHS	349			pF	349
RdsOn	RdsOn_QHS	280			mOhm	280
6.2.2 Low side switch						
Product	QLS	IPA60R280P7S				IPA60R280P7S
CoTr	CoTr_QLS	349			pF	349
RdsOn	RdsOn_QLS	280			mOhm	280
6.2.3 2nd side rectifier						
Type of the 2nd side rectifier	Type_2ndRect	SR				SR
SR switch	QSR	BSC160N15NS5				BSC160N15NS5
Rated voltage	Vds_QSR	150			V	150
Voltage derating factor of the 2nd side rectifier	kVdr_2ndRect	0.8				80%
Number of the SR switches in parallel	N_QSR	2			piece	2
Coss of the SR switch	Coss_QSR	340			pF	340
RdsOn	RDSonMax_QSR	16			mOhm	16
Qg	Qg_QSR	19			nC	19

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	**170W BPA**
6.2.3 2nd side rectifier						
Type of the 2nd side rectifier	Type_2ndRect	Diode				Diode
2nd side rectifier device	2ndRect	BSC160N15NS5				BSC160N15NS5
Rated voltage	V2ndRect	150			V	150
Voltage derating factor of the 2nd side rectifier	kVdr_2ndRect	0.8				80%
						2
						340
						16
						19

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HFB design
- Negative magnetizing current for ZVS

- ZVS and magnetizing current
  - ZV turn-on operation requiring enough magnetizing current to charge and discharge the total equivalent capacitance (C_{oEq}) at the switching node = full swap of the HFB switching node voltage
  - Positive magnetizing current for HS ZV turn-on
    - Ensured by the positive peak current which is always high enough
  - Negative magnetizing current for LS ZV turn-on
    - Worst case at V_{busOVP}, $I_{MagNegR}$
    - $I_{MagNegPerc}$ calculated based on input $I_{MagNegS}$
- Boundary of the HFB transformer turns ratio
  - N_i: initial design value
  - Minimum to limit the voltage of the secondary side rectifier at the maximum bus voltage
  - Maximum to ensure the nominal output voltage at the minimum bus voltage $V_{busBoNom}$ where the HFB running with the maximum HS duty ratio D_{max}

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	170W BPA
6.3 Negative magnetizing current for ZVS						
Choosen transformer turns ratio	Ni	3.60	2.03	4.02		3.60
ZVS required negative magnetizing current amplitude	IMagNegR	0.582			A	0.582
Selected negative magnetizing current amplitude	IMagNegS	0.72			A	0.72
Percentage of the negative magnetizing current	IMagNegPerc	31			%	31
Peak value of the magnetizing current at Nominal output	IMagPosNom	3.024			A	3.024
Magnetizing current positive peak value at OCPLev1	IMagPosOcp1	3.254			A	3.254

$$C_{oEq} = C_{oTrQHS} + C_{oTrQLS} + C_{ossQsr}/N_i^2$$

$$D_{dQHS} = \frac{N_i * V_{outNom}}{V_{busDsgn}}$$

			DD_QHS	0.458
Nmin	3.17		Nmax	4.48
CoEq	750.5	pF	t_dead_HS_Half	490 ns

$$N_{iMin} = \frac{V_{busOVP}}{V_{dsQsr} * k_{VdsQsr}}$$

$$N_{iMax} = \frac{D_{max} * V_{inBo}}{V_{outNom}}$$

$$I_{MagNegR} = \frac{C_{oEq} * V_{busOVP}}{t_{deadHS_Half}}$$

High or low Ni?

For the same bus voltage range, higher output voltage requires lower turns ratio.

For the same output voltage range, higher turns ratio leads to lower requirement on the voltage rating, but more losses of the secondary rectifier.

$$I_{MagNegPerc} = MIN\left(\frac{I_{MagNegS} * N_i * 100}{2 * I_{outNom}}, I_{MagNegMaxPerc}\right)$$

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HFB design
- Negative magnetizing current for ZVS

- HFB design consideration
  - $I_{outOCPLev1Perc}$ as steady state operation since the time during is usually long
  - $I_{outOCPMax}$ to be covered by
    - Proper value of the output capacitance, or
    - Higher output voltage range or ripple
- Magnetizing current for the HFB transformer
  - At I_{outNom}
    - Positive peak $I_{MagPosNom} = \frac{2 * I_{outNom}}{N_i} + I_{MagNegS}$
    - Peak-peak value $I_{MagPkPknom} = I_{MagPosNom} + I_{MagNegS}$
  - at $I_{outOCPLev1}$
    - Positive peak $I_{MagPosOCP1} = \frac{2 * I_{outNom} * {I_{outOCPLev1Perc}}/{100}}{N_i} + I_{MagNegS}$
    - Peak-peak value $I_{MagPkPkOCP1} = I_{MagPosOCP1} + I_{MagNegS}$

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	170W BPA
6.3 Negative magnetizing current for ZVS						
Choosen transformer turns ratio	Ni	3.60	2.03	4.02		3.60
ZVS required negative magnetizing current amplitude	IMagNegR	0.582			A	0.582
Selected negative magnetizing current amplitude	IMagNegS	0.72			A	0.72
Percentage of the negative magnetizing current	IMagNegPerc	31			%	31
Peak value of the magnetizing current at Nominal output	IMagPosNom	3.024			A	3.024
Magnetizing current positive peak value at OCPLev1	IMagPosOcp1	3.254			A	3.254

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HFB design
- Transformer inductance and resonant tank

- Magnetizing inductance

$$L_{Pcal} = \frac{t_{onQls} * N_i * V_{outNom}}{I_{MagPkPkOCP1}}$$

  - Optimization options
    - I_{outNom} or
    - $I_{outOCPlev1}$

Optimization options
Transformer can be optimizied based on the nominal power (for smaller transformer) or at the OCPLev1 (for longer OCPLev1 operation).

- Resonant capacitor
  - Two main resonant tanks built-up by
    - HS on-time: L_{Mag} and C_{lump} with C_{lump} as lumped-up capacitance
    - LS on-time: L_r and C_{lump} at the HB switching node
  - Resonant from L_r and C_{lump} defining the dimensioning of C_r
  - Optimal design: i_{Lr} reaching i_{LMag} @ end of t_{onQLS}
  - No simple formula to calculate the proper C_r due to
    - Non-zero starting point
    - Timely changing i_{LMag}
  - Rough calculation: $^{T_r}/_2 = 70\% * t_{onQLSDsgn}$ with $T_r = 2 * \pi * \sqrt{L_r * C_r}$
  - Calculation done in the spread sheet
    - Best match of f_r for the optimal design
    - With information about the resonant current starting point
  - Fine tune on board necessary: C_r, $t_{TransNom}$ and $I_{MagNegNomPerc}$

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	**170W BPA**
6.4 Transformer inductance and resonant tank						
Output power level for HFB optimization	Psel	IoutNom				IoutNom
Magnetizing inductance calculated	LpCal	108.17			µH	108.17
Magnetizing inductance choosen	Lp	120			µH	120
Leakage inductance calculated	Lr	4.0			µH	4.0
Resonant capacitance at the nominal condition	CrCal	0.118			µF	0.118
Average voltage across the resonant capacitor	VCrAvg	147.6			V	147.6
Factor of the capacitance at the VCrAvg over at 0 V	kCrV	100%				100.0%
Capacitance at 0 V bias	Cr0V	0.118			µF	0.118
Selected value of the resonant capacitors	Cr	0.200			µF	0.200
Calculated LS on time at the nominal output	tTransNom	2.744			µs	2.744
Percentage of tTRANSnom at 0 V bias	tTransRvs0Vperc	100.0			%	100.0
Equivalent ESR of the resonant capacitor	CrESR	10			mOhm	10

tonHSDsgn	2.53 us	tLSonDsgn	2.87 us
T_wo_tdeadHS	5.39 us		

$$t_{onDQhsDsgn} = \left(T_{swD} - \frac{t_{deadHSHalf}}{1000}\right) * D_{dQhs}$$

$$t_{onDQlsDsgn} = \left(T_{swD} - \frac{t_{deadHSHalf}}{1000}\right) * \left(1 - D_{dQhs}\right)$$

$$T_{wotdeadHS} = t_{onDQhsDsgn} + t_{onDQlsDsgn}$$

$$C_r = \frac{1}{4 * \pi^2 * f_r^2 * L_r}$$

$$V_{crAvg} = V_{outNom} * N_i$$

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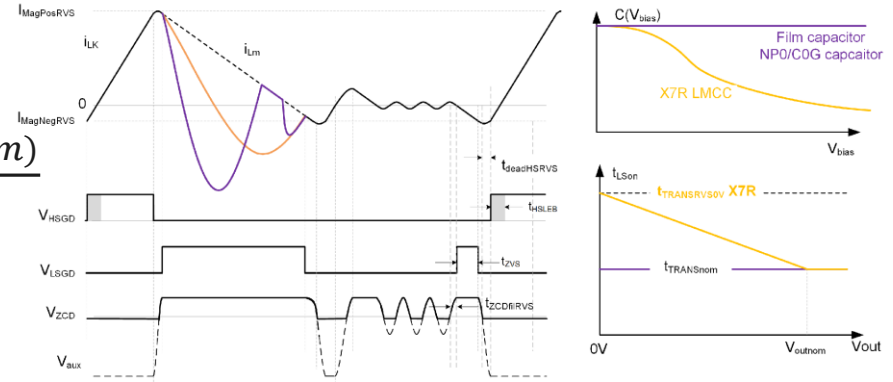
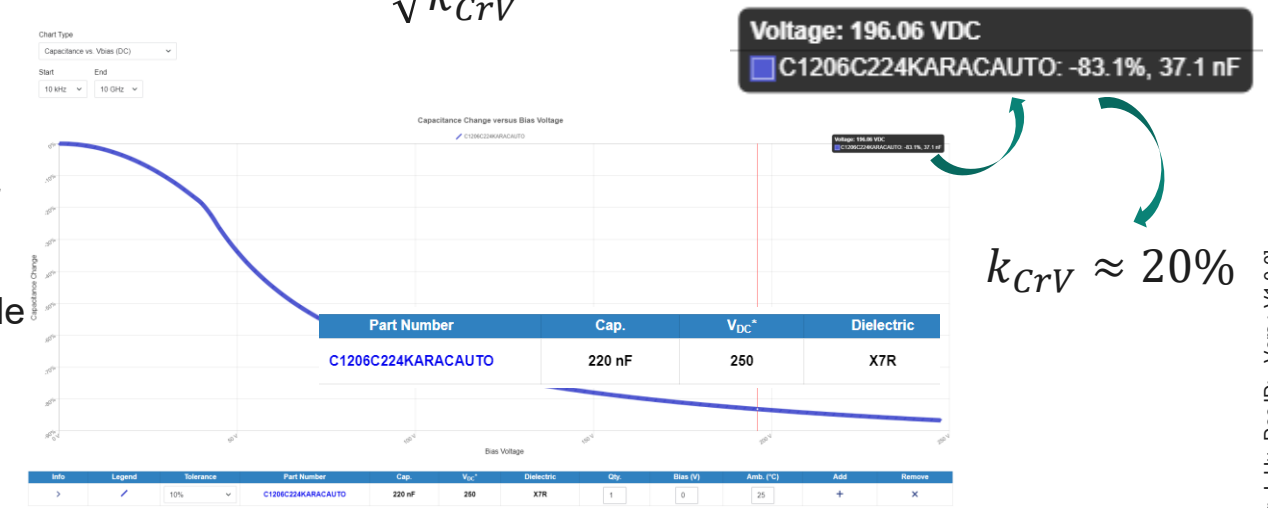
HFB design
- Transformer and resonant tank

- Resonant capacitor (cnt')
  - Different dependence of the capacitance on the DC bias voltage ($k_{CrV} = C(V_{crNom})/C(0V)$) from different types of the capacitor
    - **Film capacitor**: low dependency, $k_{CrV} \approx 1$
      - Pro: lowest audible noise level
      - ➔ Con: relative high price, biggest size/footprint
        Recommended for
        1) application with fixed output voltage
        2) audible noise sensitive application
    - **MLCC NPO/C0G**: low dependency, $k_{CrV} \approx 1$
      - Pro: small size, low audible noise level
      - Con: low capacitance of single device, price, big footprint of required number of the capacitors
    - **MLCC X7R**: high dependency, $k_{CrV} \approx 20\%$ as from the example
      - Pro: smallest size, low price
      - Con: high audible noise
      - ➔ Recommended for
        1) Compact design
        2) Audible noise less-sensitive, but cost sensitive applications

$$k_{CrV} = \frac{C_{(VcrNom)}}{C_{(0V)}}$$



$$t_{TransRvs0Vperc} = \frac{100}{\sqrt{k_{CrV}}}$$



$k_{CrV} \approx 20\%$

(Source: https://ksim3.kemet.com/capacitor-simulation)

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HFB design
- Transformer: main windings

- Main windings
  - Specifying the maximum flux density
  - Select the core for the HFB transformer from the available cores, or insert a customized core info in the MagCore sheet and select that core
  - N_{pMin} calculated with the output OCP maximum plus 5% safety margin

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	170W BPA
6.5 Transformer main windings						
Maximal core flux	Bmax	0.30			T	0.30
Core selected	Core	PQ2620				PQ2620
Selected turns count of the secondary winding	Ns	5	5.00		turns	5
Selected turns count of the primary winding	Np	18	16.69		turns	18
Realized turns ratio of Np:Ns	N	3.60	2.03	4.02		3.60
DC resistance of the transformer primary winding	RdcPri	45.0			mOhm	45.0
DC resistance of the transformer secondary winding	RdcSec	5.0			mOhm	5.0

$$N_{pMin} = \frac{L_p * \left(I_{MagPosNom} * \left(\frac{I_{outOCPMaxPerc}}{100} + \frac{5}{100} \right) \right)}{B_{max} * A_e}$$

$$N_{sMin} = \frac{N_{pMin}}{N_i}$$

Ae	121.0	mm^2	VeThfb	5470.0	mm^3
NpMin	17.96				
kRacRdc	1.5				

- R_{dcPri} and R_{dcSec}: for power losses estimation (optional)
  - Resistance of the transformer primary and secondary winding resistance for the power losses estimation
  - Assumption that the winding AC resistance k_{RacRdc} times of its DS resistance
  - Non-zero value required for the power losses estimation

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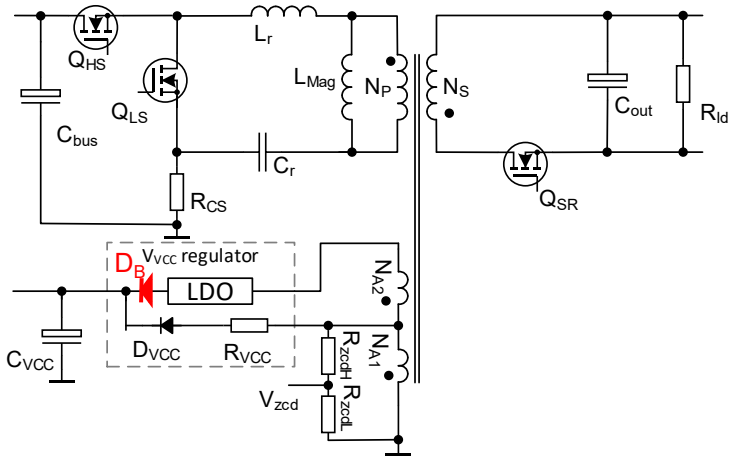
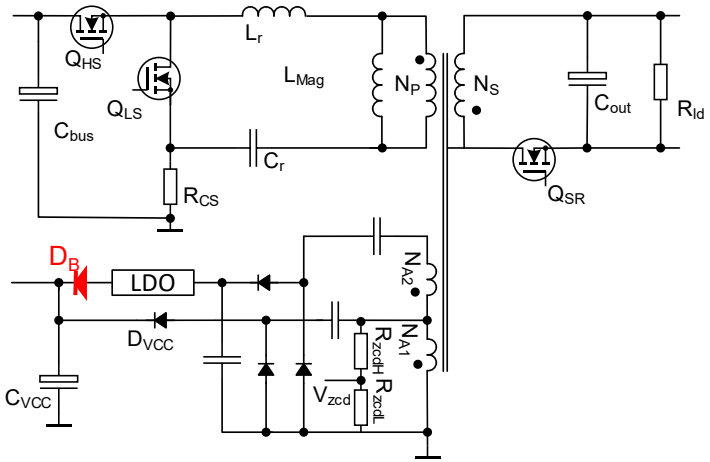
HFB design
- Transformer: VCC supply and auxiliary winding(s)

– Flyback windings + LDO



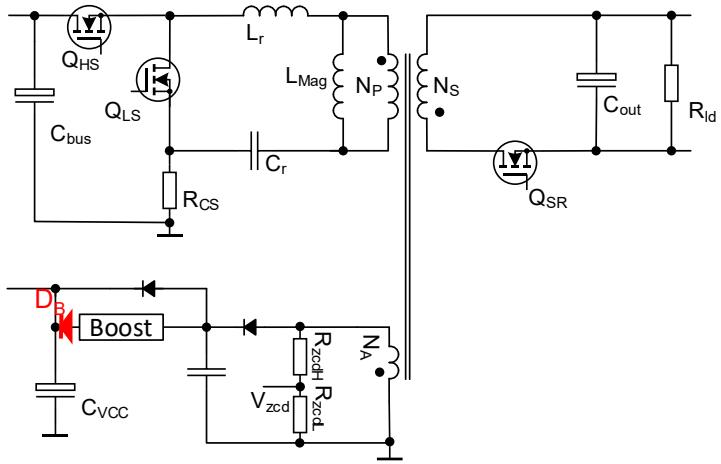
– Auxiliary winding voltage depending on the **output** voltage
– **Two** auxiliary windings for wide output voltage range
– Step-down LDO, **less efficient**
– Less concern about EMI
– **Cost low**

– Charge-pump + LDO



– Auxiliary winding voltage depending on the **bus** voltage
– **Two** auxiliary windings for wide output voltage range
– Step-down LDO, **less efficient**
– Less concern about EMI
– **Cost high**
– **Audible noise** with the X7R capacitors due to pulse current

– Flyback winding + boost



– Auxiliary winding voltage depending on the **output** voltage
– **One** auxiliary winding
– Boost converter, **more efficient**
– Concern about EMI
– **Cost middle**

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HFB design
- Transformer: VCC supply and auxiliary winding(s)

- Criteria for the VCC supply porposal
  - Charge pump + LDO for the case $\frac{V_{outNom}}{V_{outUVP}} > \frac{V_{bucOVP}}{V_{inBo}}$; otherwise, Flyback aux + LDO; or
  - Higher performance design
    - Flyback winding + boost for

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	**170W BPA**
6.6 VCC supply, auxiliary widings and ZCD netwrok						
VCC supply solution proposal		Charge pump + LDO, or Flyback + boost for advanced design				Charge pump + LDO, or Flyback + boost for advanced design
VCC supply solution selected		ChargePump_LDO				ChargePump_LDO
Target VCC voltage fron the auxiliary winding	VVCCT	12.0			V	12.0
Diode forward conduction voltage	Vf_Dvcc	0.7			V	0.7

- Additional parameters
  - V_{VCCT}: VCC voltage target during normal operation
  - V_{f_Dvcc}: forward conduction voltage of the VCC rectifier diode

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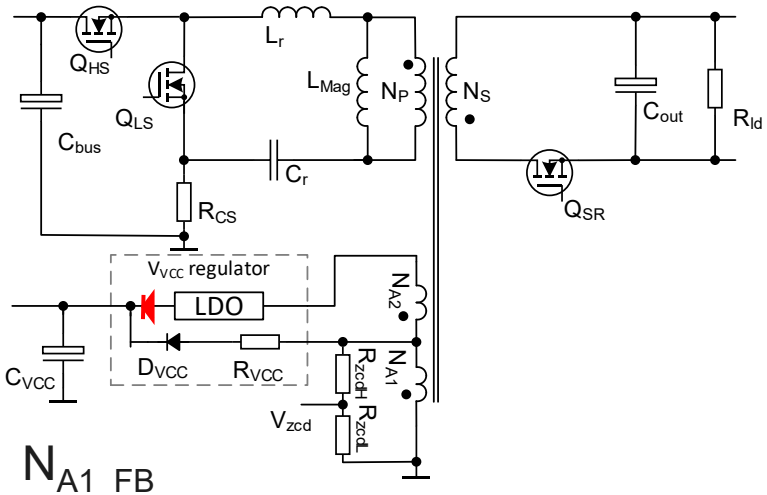
HFB design
- Transformer: VCC supply via flyback windings + LDO



- N_{A1_FB}
  - Minimum
    - To get the target V_{VCCT} at the nominal output voltage

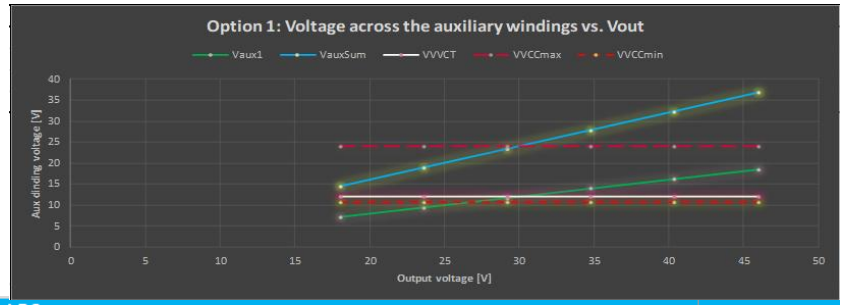
$$N_{A1_FBMin} = {(V_{VCCT} + V_{fDvcc}) * N_s}/{V_{outNom}}$$

  - Maximum
    - Resulted V_{VCC} touching the $V_{VCConMax}$ at the output OVP

$$N_{A1_FBMax} = {V_{VCConMax} * N_s}/{V_{outOVP}}$$

- N_{A2_FB} to ensure the V_{VCCT} at V_{outUVP}

$$N_{A2_FB} = RoundUp\left(\frac{V_{VCCT} * N_s}{V_{outUVP}} - N_{A1}\right)$$



6.6.1 Option 1: flyback auxiliary windings + LDO					
1st auxiliary winding turns count	NA1_FB	2	1.55	2.39 turns	2
2nd auxiliary winding turns count	NA2_FB	2		turns	2
RzcdL	RZCDL_Base_FB	1.50		39	1.50
	RZCDL_Factor_FB	10k		kOhm	10k
RzcdH	RZCDH_Base_FB	8.45	84.50	84.50	8.45
	RZCDH_Factor_FB	10k		kOhm	10k
VoutVzcdRatio design error	VoutVzcdRatio_DE_FB	0.86%			0.86%

- Rzcd network design

RzcdLFB	36.5	kOhm

  - The maximum total resistance defined by the required current through the resistor at the lowest output voltage during the HFB operation

$$R_{zcdSumMaxFB} = \frac{(V_{outUVP} * 0.9) * {N_{A1FB}}/{N_s}}{I_{ZCDlkMax} * k_{IzcdDvd}}$$

kIzcdDvd	2.5	
RzcdSumMax_FB	259	kOhm

  - Maximum of the low-side divider resistor based on the ratio VoutVzcdRatio

$$R_{zcdLFBMaxFB} = {R_{zcdSumMax}}/{\left({N_{A1FB}}/{N_s} * V_{outVzcdRatio}\right)}$$

  - Best match for the high-side resistance calculated based on the selected low-side resistance

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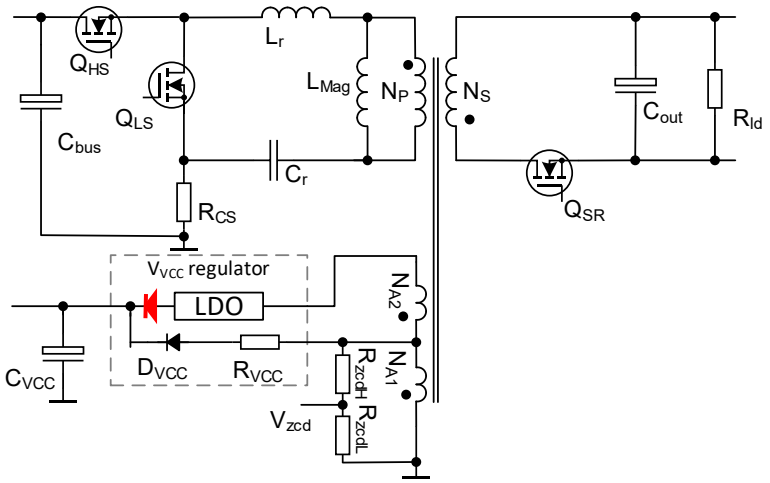
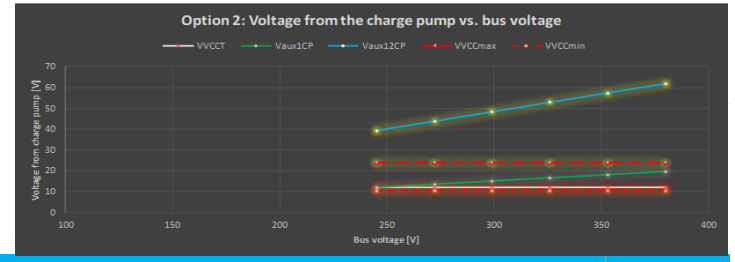
HFB design
- Transformer: Charge-pump + LDO





6.6.2 Option 2: charger pump + LDO					
1st auxiliary winding turns count	NA1_CP	1	1.00	1.11	1
2nd auxiliary winding turns count	NA2_CP	2	-0.02		2
RzcdL	RZCDL_Base_CP	2.00		38.74	2.00
	RZCDL_Factor_CP	10k		kOhm	10k
RzcdH	RZCDH_Base_CP	4.70	47.00	47.00	4.70
	RZCDH_Factor_CP	10k		kOhm	10k
VoutVzcdRatio design error	VoutVzcdRatio_DE_CP	-0.14%			-0.14%

RzcdLCP	20	kOhm	RzcdLMaxCP	39 kOhm

- N_{A1CP}
  - The resulted voltage lower than $V_{VCConMax}$ at the bus OVP
  - $N_{A1Max} = \frac{V_{VCConMax}+2*V_{fDVCC}}{V_{busOVP}} * N_p$
- N_{A2CP}
  - To ensure the target V_{VCCT} at V_{inBo}
  - $N_{A2CPMin} = \frac{V_{VCCT}+2*V_{fDVCC}}{V_{inBo}} * N_p - N_{A1CP}$

- Rzcd network design
  - Maximum value of R_{ZCDH}+R_{ZCDL}

$$R_{zcdSumMaxCP} = \frac{(V_{outUVP} * 0.9) * N_{A1CP}/N_s}{I_{ZCDlkMax} * k_{IzcdDvd}}$$

  - Maximum low-side resistance

$$R_{zcdLCPMaxCP} = \frac{R_{zcdSumMaxCP}}{N_{A1CP}/N_s * V_{outVzcdRatio}}$$

- Best match for the high-side resistance calculated based on the selected low-side resistance

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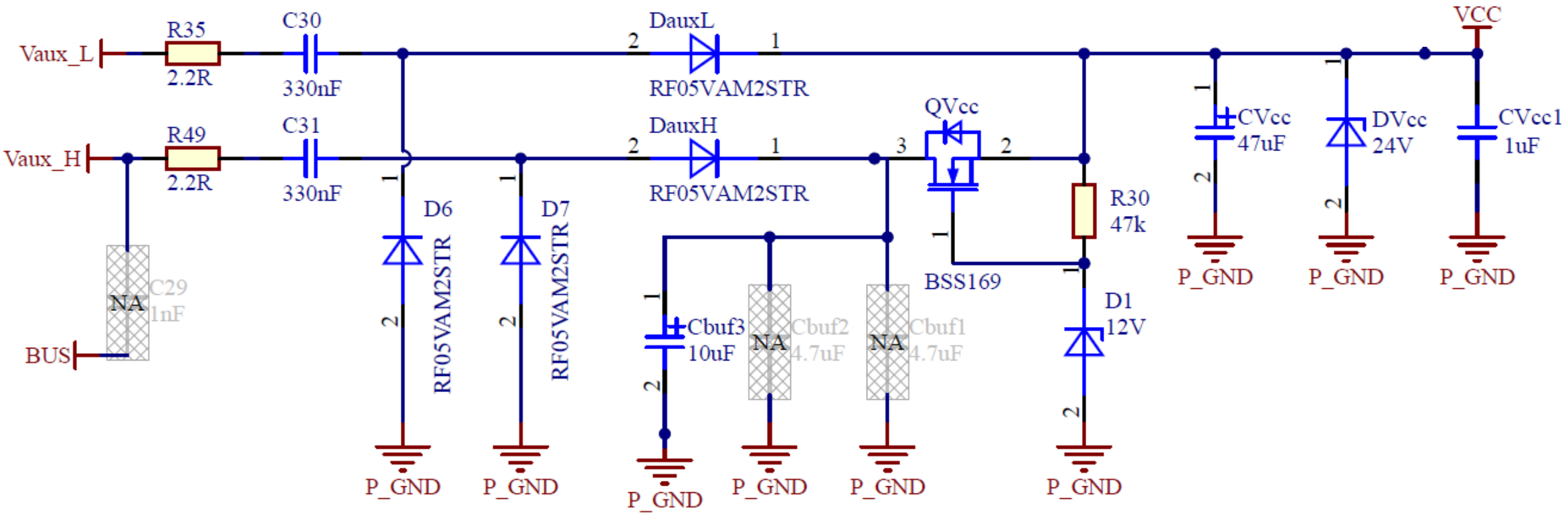
HFB design
- Transformer: Charge-pump + LDO

– One design example from the 170W eva board



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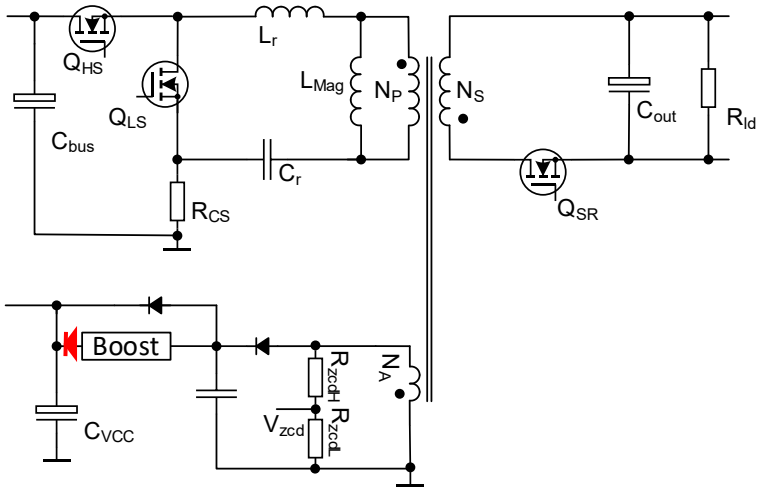
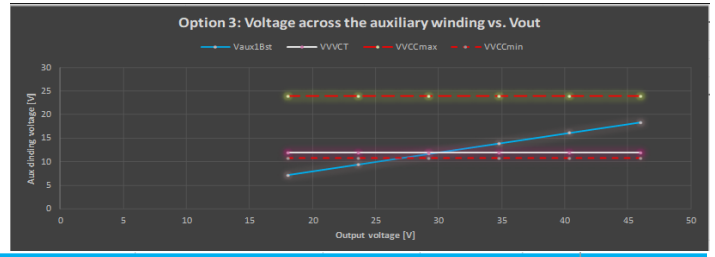
HFB design
- Transformer: VCC supply Flyback winding + boost





6.6.3 Option 3: Aux + boost					
Auxiliary winding turns count	NA_Bst	2	1.55	2.39	2
RzcdL	RZCDL_Base_Bst	1.54		38.74 kOhm	1.54
	RZCDL_Factor_Bst	10k			10k
RzcdH	RZCDH_Base_Bst	8.66	86.60	86.60	8.66
	RZCDH_Factor_Bst	10k		kOhm	10k
VoutVzcdRatio design error	VoutVzcdRatio_DE_Bst	1.01%			1.01%

RzcdLBst	31.6	kOhm	RzcdLMaxBst	39	kOhm

- N_{ABst}
  - Minimum to ensure the target V_{VCCT} at the nominal output voltage
  - $N_{ABstMin} = \frac{V_{VCCT}+V_{fDVCC}}{V_{outNom}} * N_s$
  - Maximum to limit the V_{ABst} below the $V_{VCConMax}$ at output OVP level
  - $N_{ABstMax} = \frac{V_{VCConMax}}{V_{outOVP}} * N_s$

- ZCD network design
  - Maximum value of $R_{ZCDH}+R_{ZCDL}$

$$R_{zcdSumMaxBst} = \frac{(V_{outUVP} * 0.9) * {N_{ABst}}/{N_s}}{I_{ZCDlkMax} * k_{IzcdDvd}}$$

  - Maximum low-side resistance

$$R_{zcdLCPMaxBst} = {R_{zcdSumMaxBst}}\Big/\left({N_{ABst}}/{N_s} * V_{outVzcdRatio}\right)$$

- Best match for the high-side resistance calculated based on the selected low-side resistance

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HFB design
- Shunt resistance

– Required shunt resistance

– $R_{csR} = \frac{DAC_Range * {}^{I_{setNomPerc}}/_{100}}{2 * {}^{I_{outNom}}/_{N_i}}$

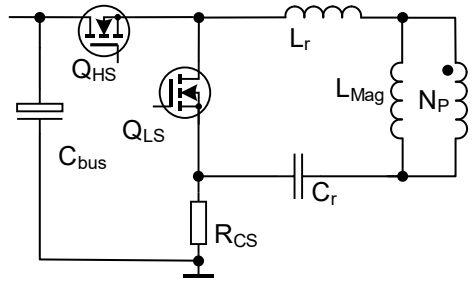
– ${}^{I_{setNomPerc}}/_{100} = MIN\left[\frac{ADC_MFIO2_Range_Thr_Max - V_{fbOpMin}}{ADC_MFIO2_Range * {}^{I_outOCPMaxPerc}/_{100}}, \frac{1}{{}^{I_{MagNegPerc}}/_{100} + {}^{I_{outOCPMaxPerc}}/_{100}}\right]$

Design steps	Design # Parameter	Design1 Value typ.	Value min.	Value max.	Unit	Design1 170W BPA
6.7 Shunt resistor						
Required shunt resistance	RCSR	0.091			Ohm	0.091
1st shunt resistor	RCS1	0.33			Ohm	0.33
2nd shunt resistor	RCS2	0.33			Ohm	0.33
3rd shunt resistor	RCS3	0.20			Ohm	0.20
Shunt resistance design error	RCSde	0.82%				0.82%
Maximum peak power losses	PRcsMax	1.79			W	1.79

IsetNomPerc	48.05	%
RshuntD	0.090	Ohm
MagPosPkOCPMax	4.45	A

– The required shunt resistance depending on
  – $I_{outOCPMaxPerc}$
  – $V_{fbOpMin}$

➡ Shunt resistance on the board to be updated in case of any change of these parameters



– Power rating calculation

– $I_{rmsCsMax} = \sqrt{\frac{D_{Max}}{3}} * I_{MagPosPkOCPMax}$

– $I_{MagPosPkOCPMax} = 2 * \frac{I_{outNom} * {}^{I_{outOCPMaxPerc}}/_{100}}{N_i} + I_{MagNegNom}$

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HFB design
- Output capacitance

- Key requirements on the output capacitor
  - Minimum capacitance for the allowed voltage drop at big load jump
    - $C_{outMin} = \frac{{}^{P_{outNom}}/_{V_{outNom}} * {}^{N_RspDelay}/_{f_{swD}}}{V_{outDropLdjmp}}$, with

      $V_{outDropLdjmp} = V_{outNom} * k_{VoutDropLdjmp}$, and

      Assumed feedback response time of 10 cycles: $NRspDelay = 10$
  - Main criteria: Requirement on the ripple current rating
    - $I_{rmsCout} = \sqrt{I_{rmsSecNom}^2 - I_{outNom}^2}$, with

$$I_{secSecNom} = \frac{\pi}{2 * \sqrt{2 * (1 - D_{QHS})}} * I_{outNom}$$

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	**170W BPA**
6.8 Output capacitor						
Total output capacitor RMS current	Irms_Cout	6.46			A	6.46
Current capability of the single output capacitor	Irms_CoSingle	2800			mA	2800
ESR of the selected output capacitors	ESR_CoSingle	37.0			mOhm	37.0
Required number of the output capacitors	N_Co	3				3
Total output capacitance	Cout	780	56		uF	780

VoutDropLdjmp	2.1	V
NRspDelay	10	cycles
IrmsSecNom	6.09	A

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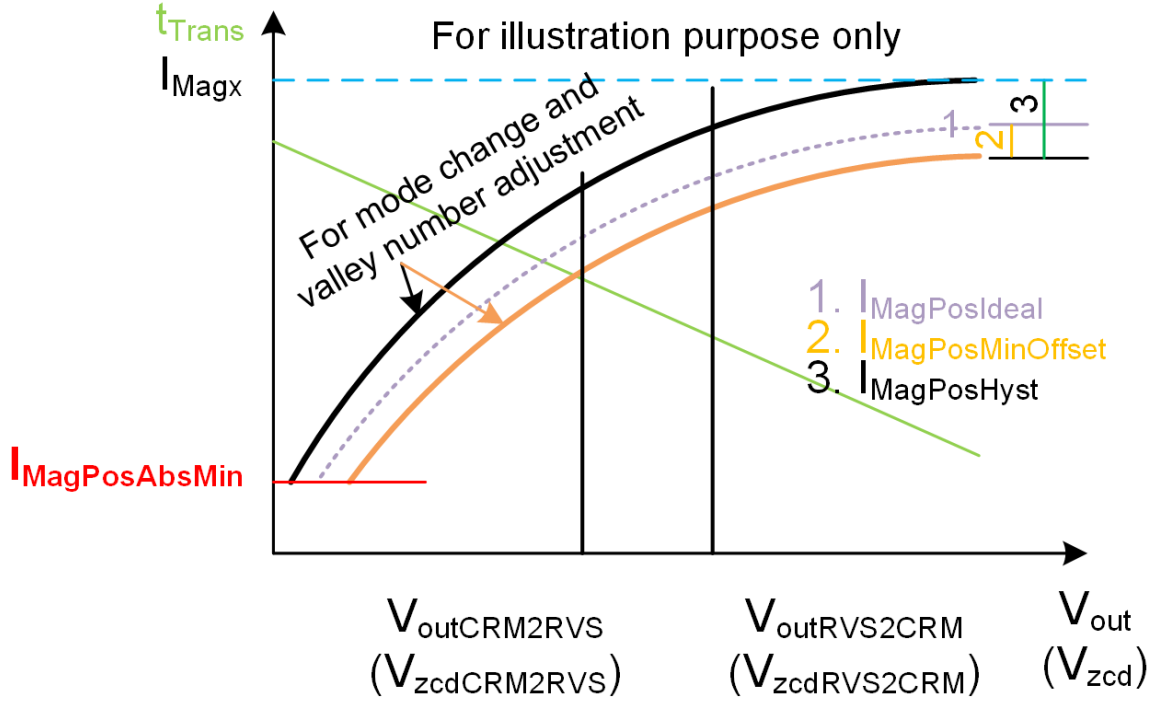
HFB design
- Additional csv parameter setting

- Mode transition
  - CRM vs. ZV-RVS mode
    - CRM at high and medium load
    - ZV-RVS operation at low and light load
  - Voltage thresholds, as defined

- Current thresholds
  - Two curved lines for
    - Mode transition
    - Valley number change
    - Defined by parameter
      - $I_{MAGPosMinOffset}$
      - $I_{MAGPosHyst}$

	Design #	Design1				Design1
Design steps	Parameter	Value typ.	Value min.	Value max.	Unit	170W BPA
7. Additonal csv parameter setting						
7.1 mode transition voltage						
Output voltage for CRM to RVS transition	VoutCrm2Rvs	16.0			V	16.0
Output voltage for CRM to RVS transition	VoutRvs2Crm	18.0	16.8		V	18.0
7.2 ZVS pulse width setting						
Maximum of the SR controller minimal on-time	tonMinSrCtrl	600			ns	600
ZVS pulse width setting	tZVSmin	600	600		ns	600
7.3 PCB trace resistance						
Primary high-current PCB trace	RpcbP	20			mOhm	20
Secondary high-current PCB trace	RpcbS	3			mOhm	3



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HFB design
- Additional csv parameter setting

- ZVS pulse width
  - Ensuring ZVS for the Q_{HS} via the ZVS pulse
  - Minimum pulse width higher than the minimum on-time of the SR controller if it is used

- PCB trace resistance
  - Information required for the power losses estimation
  - Optional

	Design #	Design1				Design1
Design steps	**Parameter**	**Value typ.**	**Value min.**	**Value max.**	**Unit**	**170W BPA**
7. Additonal csv parameter setting						
7.1 mode transition voltage						
Output voltage for CRM to RVS transition	VoutCrm2Rvs	16.0			V	16.0
Output voltage for CRM to RVS transition	VoutRvs2Crm	18.0	16.8		V	18.0
7.2 ZVS pulse width setting						
Maximum of the SR controller minimal on-time	tonMinSrCtrl	600			ns	600
ZVS pulse width setting	tZVSmin	600	600		ns	600
7.3 PCB trace resistance						
Primary high-current PCB trace	RpcbP	20			mOhm	20
Secondary high-current PCB trace	RpcbS	3			mOhm	3

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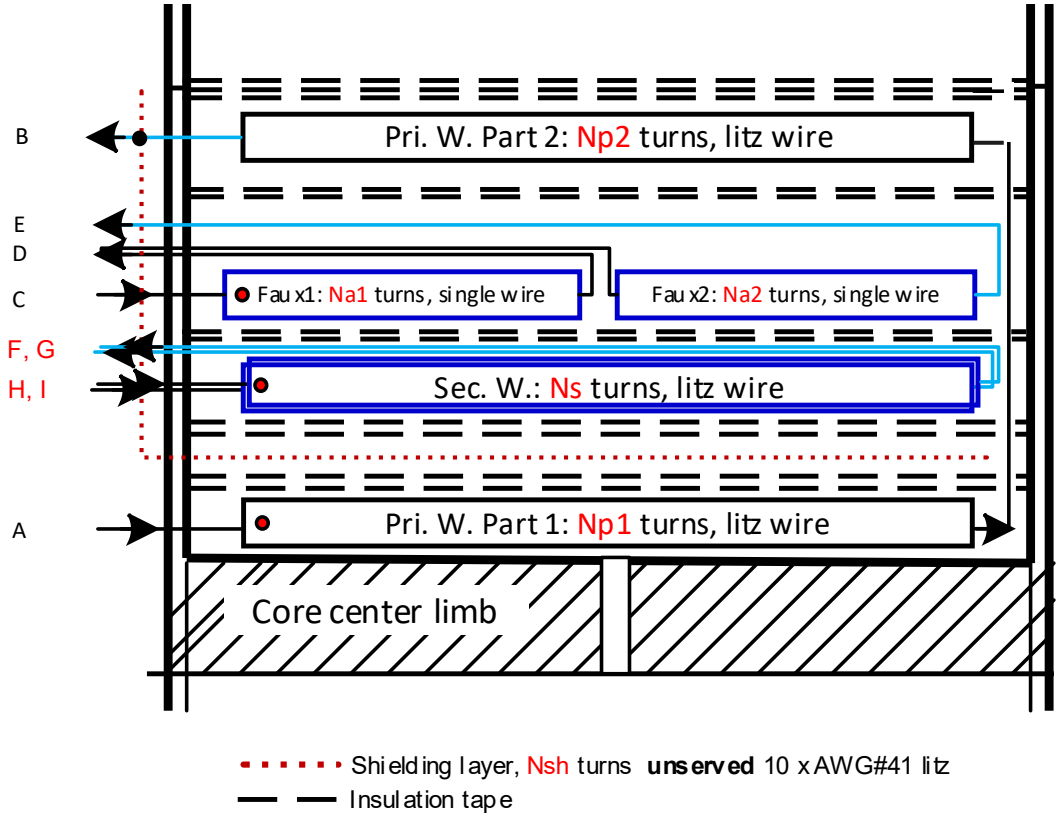
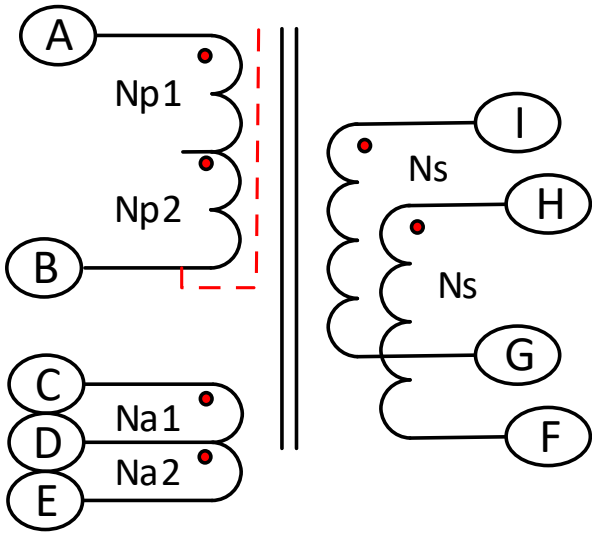
Transformer construction

- Sandwitch structure recommended
- Benefitial of an inner shielding layer on the EMI performance





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Revision history

- V1.0.0
  - Updated according to the design tool V1.0
- V0.2.0
  - Updated based on the design tool V0.2.0
  - Design guide updates
- V0.1.0
  - Initial release

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