XDP™ XDP720-001 PMBus® commands

A user guide to the list of supported PMBus® commands

About this document

Scope and purpose

This document describes all the PMBus® commands supported by the XDP™ XDP720-001 positive input voltage digital eFuse ICs.

Intended audience

This document is intended for XDP™ XDP720-001 users.

Table of contents

Table of contents . . . 2

1 Introduction . . . 5

2 Supported PMBus commands . . . 6

2.1 OPERATION . . . 6
2.2 CLEAR_FAULTS . . . 6
2.3 CAPABILITY . . . 6
2.4 VOUT_OV_WARN_LIMIT . . . 7
2.5 VOUT_UV_WARN_LIMIT . . . 7
2.6 VOUT_UV_FAULT_LIMIT . . . 8
2.7 IOUT_OC_WARN_LIMIT . . . 8
2.8 OT_FAULT_LIMIT . . . 8
2.9 OT_WARN_LIMIT . . . 9
2.10 VIN_OV_FAULT_LIMIT . . . 9
2.11 VIN_OV_WARN_LIMIT . . . 9
2.12 VIN_UV_WARN_LIMIT . . . 10
2.13 VIN_UV_FAULT_LIMIT . . . 10
2.14 PIN_OP_WARN_LIMIT . . . 10
2.15 STATUS_BYTE . . . 11
2.16 STATUS_WORD . . . 12
2.17 STATUS_VOUT . . . 13
2.18 STATUS_IOUT . . . 14
2.19 STATUS_INPUT . . . 14
2.20 STATUS_TEMPERATURE . . . 15
2.21 STATUS_CML . . . 15
2.22 STATUS_OTHER . . . 16
2.23 STATUS_MFR_SPECIFIC . . . 16
2.24 READ_EIN . . . 17
2.25 READ_VIN . . . 18
2.26 READ_VOUT . . . 18
2.27 READ_IOUT . . . 18
2.28 READ_TEMPERATURE_1 . . . 18
2.29 READ_TEMPERATURE_2 . . . 19
2.30 READ_PIN . . . 19
2.31 PMBUS_REVISION . . . 19
2.32 MFR_ID . . . 20
2.33 MFR_MODEL . . . 20
2.34 MFR_REVISION . . . 21
2.35 VIN_OV_FAULT_LIMIT_S . . . 21
2.36 VIN_UV_FAULT_LIMIT_S . . . 22

Table of contents

2.37 PMBUS_CFG . . . 22
2.38 MODE . . . 23
2.39 V_SNS_CFG . . . 23
2.40 I_SNS_CFG1 . . . 25
2.41 I_SNS_CFG2 . . . 26
2.42 UV_TH_TMR . . . 26
2.43 WATCHDOG_TMR . . . 27
2.44 V_TMR . . . 28
2.45 GPO_CFG . . . 29
2.46 IOUT_UC_WARN_LIMIT . . . 30
2.47 ONCHIP_TSD_FAULT_LIMIT . . . 31
2.48 ENABLE_FAULTS . . . 31
2.49 MASK_FAULTS . . . 33
2.50 STATUS_FAULTS . . . 34
2.51 ENABLE_WARNS . . . 36
2.52 MASK_WARNS . . . 37
2.53 STATUS_WARNS . . . 38
2.54 PWRGD_DG_TMR . . . 40
2.55 SOA_TMR . . . 40
2.56 TURN_OFF_CTRL . . . 42
2.57 RETRY . . . 42
2.58 TELEMETRY_EN . . . 44
2.59 TELEMETRY_AVG . . . 45
2.60 WRITE_OTP . . . 46
2.61 STATUS_MEM . . . 47
2.62 RESTART . . . 48
2.63 READ_PIN_EXT . . . 48
2.64 READ_VIN_PEAK . . . 48
2.65 READ_VOUT_PEAK . . . 49
2.66 READ_IOUT_PEAK . . . 49
2.67 READ_PIN_PEAK . . . 49
2.68 READ_TEMP_1_PEAK . . . 50
2.69 READ_VIN_VALLEY . . . 50
2.70 READ_VOUT_VALLEY . . . 51
2.71 READ_IOUT_VALLEY . . . 51
2.72 READ_TEMP_1_VALLEY . . . 51
2.73 STATUS_MODE . . . 52
2.74 CONFIG_ID . . . 53
2.75 READ_EIN_EXT . . . 53

3 Revision history . . . 54

Table of contents

Disclaimer 55

1 Introduction

In tables where register bit fields are defined, the following conventions are used to indicate undefined and unimplemented function. Furthermore, types of bits and bit fields are defined using the abbreviations as shown in the following table.

Table 1 Bit function terminology

Function of bits	Description
Unimplemented, Reserved	Register bit fields named **0** indicate unimplemented functions with the following behavior: • Reading these bit fields returns 0 • These bit fields should be written with 0 if the bit field is defined as r or rh • These bit fields have to be written with 0 if the bit field is defined as rw These bit fields are reserved. The detailed description of these bit fields can be found in the register descriptions.
rw	The bit or bit field can be read and written.
rwh	As rw, but bit or bit field can also be set or reset by hardware.
r	The bit or bit field can only be read (read-only).
w, wX	The bit or bit field can only be written (write-only). A read of this register will always give a default value back that is described in the register documentation.
w0, w1	The bit or bit field can only be written (write-only). A read of this register will always give the value 0 or 1 back.
r0, r1	The bit or bit field can only be read. The read value is 0 or 1.
rh	This bit or bit field can be modified by hardware (read-hardware, typical example: status flags). A read of this bit or bit field give the actual status of this bit or bit field back. Writing to this bit or bit field has no effect on the setting of this bit or bit field.
s	Bits with this attribute are “sticky” in one direction. If their reset value is once overwritten by software, they can be switched again into their reset state only by a reset operation. Software cannot switch this type of bit into its reset state by writing the register. This attribute can be combined to “rws” or “rwhs”.
f	Bits with this attribute are readable only when they are accessed by an instruction fetch. Normal data read operations will return other values.

2 Supported PMBus commands

2.1 OPERATION

This command is used to turn the efuse output on or off in conjunction with the input from the EN, SYNC and FS pins.

OPERATION Address: 001_H

Reset value: 80_H

7	6	5	4	3	2	1	0
ON	**Res**						
rw	r						

Field	Bits	Type	Description
ON	7	rw	**ON bit enables or disables the efuse output.** 0_B efuse output is disabled. 1_B efuse output is enabled.

2.2 CLEAR_FAULTS

This command is used to clear any fault and/or warning bits that have been set. If the fault or warning is still present when the bit is cleared, the fault or warning bit is immediately set again. This command is write only without a data byte.

CLEAR_FAULTS Address: 003_H

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLEAR_FAULTS															
w															

Field	Bits	Type	Description
CLEAR_FAULTS	15:0	w	**Clear any fault or warning bits that have been set.**

2.3 CAPABILITY

This read only command provides a way for the host system to determine some key capabilities of the device.

CAPABILITY Address: 019_H

Reset value: $D0_H$

7	6	5	4	3	2	1	0
PCK_ERR_CHK	**MAX_BUS_SPEED**		**SMBALERT**	**NUMERIC_FORMAT**	**Res**		
rh	rh		rh	rh	r		

Field	Bits	Type	Description
NUMERIC_FORMAT	3	rh	**Specifies the format of the numeric data.** 0_B Numeric data is in direct format. 1_B NA
SMBALERT	4	rh	**Specifies whether or not the device has an SMBALERT# pin and supports SMBus Alert Response protocol.** 0_B NA 1_B Device supports the SMBus Alert Response protocol.
MAX_BUS_SPEED	6:5	rh	**Specifies the maximum speed of the bus.** 00_B NA 01_B NA 10_B Maximum supported bus speed is 1 MHz. 11_B NA
PCK_ERR_CHK	7	rh	**Specifies whether or not the device supports Packet Error Check.** 0_B NA 1_B Packet Error Checking is supported.

2.4 VOUT_OV_WARN_LIMIT

This command sets the value of the output voltage measured at the VOUTS pin that causes an output overvoltage (OOV) warning.

VOUT_OV_WARN_LIMIT Address: 042_H

Reset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				VOUT_OV_WARN_LIMIT											
r				rw											

Field	Bits	Type	Description
VOUT_OV_WARN_LIMIT	11:0	rw	**OOV warning can be programmed from 0 to 22 V, 0 to 44 V or 0 to 88 V (absolute value) depending on the VTLM_RNG settings.**

2.5 VOUT_UV_WARN_LIMIT

This command sets the value of the output voltage measured at the VOUTS pin that causes an output undervoltage (OUV) warning.

VOUT_UV_WARN_LIMIT Address: 043_H

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				VOUT_UV_WARN_LIMIT											
r				rw											

Field	Bits	Type	Description
VOUT_UV_WARN_LIMIT	11:0	rw	**OUV warning can be programmed from 0 to 22 V, 0 to 44 V or 0 to 88 V (absolute value) depending on the VTLM_RNG settings.**

2.6 VOUT_UV_FAULT_LIMIT

This command sets the value of the output voltage measured at the VOUTS pin that causes an output undervoltage (OUV) fault, only in a PRIMARY configured device.

VOUT_UV_FAULT_LIMIT Address: 044_H

Reset value: $05D1_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				VOUT_UV_FAULT_LIMIT											
r				rw											

Field	Bits	Type	Description
VOUT_UV_FAULT_LIMIT	11:0	rw	**OUV fault can be programmed from 0 to 22 V, 0 to 44 V or 0 to 88 V (absolute value) depending on the VTLM_RNG settings.**

2.7 IOUT_OC_WARN_LIMIT

This command sets the current level measured at the IMON pin (via digitized V_IMON) that causes an output overcurrent (OOC) warning.

IOUT_OC_WARN_LIMIT Address: $04A_H$

Reset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				IOUT_OC_WARN_LIMIT											
r				rw											

Field	Bits	Type	Description
IOUT_OC_WARN_LIMIT	11:0	rw	**OOC limit for triggering the warning.**

2.8 OT_FAULT_LIMIT

This command sets the temperature of the internal MOSFET, in degree Celsius, at which the overtemperature (OT) fault is triggered.

OT_FAULT_LIMIT Address: $04F_H$

Reset value: $0C4F_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				OT_FAULT_LIMIT											
r				rw											

Field	Bits	Type	Description
OT_FAULT_LIMIT	11:0	rw	**OT limit for triggering the fault.**

2.9 OT_WARN_LIMIT

This command sets the temperature of the internal MOSFET, in degree Celsius, at which the overtemperature (OT) warning is triggered.

OT_WARN_LIMIT Address: 051_H

Reset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				OT_WARN_LIMIT											
r				rw											

Field	Bits	Type	Description
OT_WARN_LIMIT	11:0	rw	**OT limit for triggering the warning.**

2.10 VIN_OV_FAULT_LIMIT

This command sets the value of the input voltage measured at the VINS pin that causes an input overvoltage (OV) fault, only in a digital comparator based PRIMARY configured device.

VIN_OV_FAULT_LIMIT Address: 055_H

Reset value: $0B45_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				VIN_OV_FAULT_LIMIT											
r				rw											

Field	Bits	Type	Description
VIN_OV_FAULT_LIMIT	11:0	rw	**OV fault can be programmed from 0 to 22 V, 0 to 44 V or 0 to 88 V (absolute value) depending on the VTLM_RNG settings.**

2.11 VIN_OV_WARN_LIMIT

This command sets the value of the input voltage measured at the VINS pin that causes an input overvoltage (OV) warning.

VIN_OV_WARN_LIMIT Address: 057_H

Reset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				VIN_OV_WARN_LIMIT											
r				rw											

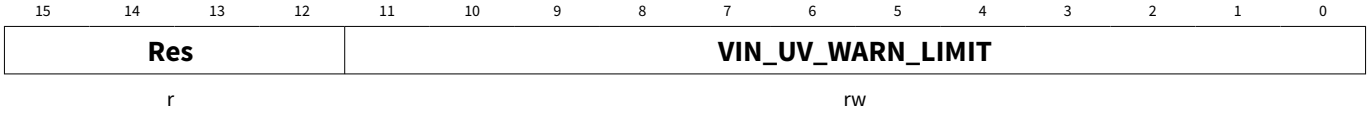
Field	Bits	Type	Description
VIN_OV_WARN_LIMIT	11:0	rw	**OV warning can be programmed from 0 to 22 V, 0 to 44 V or 0 to 88 V (absolute value) depending on the VTLM_RNG settings.**

2.12 VIN_UV_WARN_LIMIT

This command sets the value of the input voltage measured at the VINS pin that causes an input undervoltage (UV) warning.

VIN_UV_WARN_LIMIT Address: 058_H

Reset value: 0000_H



Field	Bits	Type	Description
VIN_UV_WARN_LIMIT	11:0	rw	**UV warning can be programmed from 0 to 22 V, 0 to 44 V or 0 to 88 V (absolute value) depending on the VTLM_RNG settings.**

2.13 VIN_UV_FAULT_LIMIT

This command sets the value of the input voltage measured at the VINS pin that causes an input undervoltage (UV) fault, only in a digital comparator based PRIMARY configured device.

VIN_UV_FAULT_LIMIT Address: 059_H

Reset value: $06D1_H$



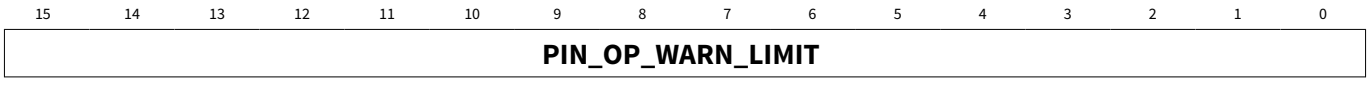
Field	Bits	Type	Description
VIN_UV_FAULT_LIMIT	11:0	rw	**UV fault can be programmed from 0 to 22 V, 0 to 44 V or 0 to 88 V (absolute value) depending on the VTLM_RNG settings.**

2.14 PIN_OP_WARN_LIMIT

This command sets the value of the input power calculated as a product of VIN * IOUT that causes an input overpower (OP) warning.

PIN_OP_WARN_LIMIT Address: $06B_H$

Reset value: $FFFF_H$



Field	Bits	Type	Description
PIN_OP_WARN_LIMIT	15:0	rw	**OP warning can be programmed from 0 to VTLM_RNG * system IMON current**

2.15 STATUS_BYTE

This command returns one byte of information with a summary of the most critical faults.

STATUS_BYTE Address: 078_H

Reset value: 40_H

7	6	5	4	3	2	1	0
Res	**OFF**	**Res**	**IOUT_OC_FAULT**	**VIN_UV_FAULT**	**TEMP**	**CML**	**NONE_OF_THE_ABOVE**
r	rh	r	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
NONE_OF_THE_ABOVE	0	rwh	**This bit indicates if a fault or warning not listed in bits [6:1] has occurred.** 0_B Fault has not ocurred. 1_B Fault has occurred.
CML	1	rwh	**This bit indicates if a communications warning, memory or logic fault has occurred.** 0_B Fault or warning has not occurred. 1_B Fault or warning has occurred.
TEMP	2	rwh	**This bit indicates if a temperature fault or warning has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.
VIN_UV_FAULT	3	rwh	**This bit indicates if an input undervoltage fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.
IOUT_OC_FAULT	4	rwh	**This bit indicates if an output overcurrent fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.
OFF	6	rh	**This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.** 0_B Output is on. 1_B Output is off.

2.16 STATUS_WORD

This command returns two bytes of information with a summary of the device's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status commands. The lower byte of the STATUS_WORD is the same command as the STATUS_BYTE.

STATUS_WORD Address: 079_H

Reset value: 0840_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VOUT	**IOUT_POUT**	**INPUT**	**MFR**	**PG_STATUS**	**Res**	**OTHER**	**Res**		**OFF**	**Res**	**IOUT_OC_FAULT**	**VIN_UV_FAULT**	**TEMP**	**CML**	**NONE_OF_THE_ABOVE**
rwh	rwh	rwh	rwh	rh	r	rwh	r		rh	r	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
NONE_OF_THE_ABOVE	0	rwh	**This bit indicates if a fault or warning not listed in bits [6:1] has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.
CML	1	rwh	**This bit indicates if a communications warning, memory or logic fault has occurred.** 0_B Fault or warning has not occurred. 1_B Fault or warning has occurred.
TEMP	2	rwh	**This bit indicates if a temperature fault or warning has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.
VIN_UV_FAULT	3	rwh	**This bit indicates if an input undervoltage fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occcurred.
IOUT_OC_FAULT	4	rwh	**This bit indicates if an output overcurrent fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.
OFF	6	rh	**This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.** 0_B Output is on. 1_B Output is off.
OTHER	9	rwh	**This bit reflects the status of the STATUS_OTHER command.** 0_B A bit in STATUS_OTHER command is not set. 1_B A bit in STATUS_OTHER command is set.

(table continues...)

(continued)

Field	Bits	Type	Description
PG_STATUS	11	rh	**This bit reflects the status of the internal PWR_GD signal. Note that this bit shows the status of the system power directly, while PWRGD_STATUS in STATUS_MODE command follows the PWRGD pin status with respect to the system power.** 0_B Output voltage is valid. 1_B Output voltage is not valid.
MFR	12	rwh	**This bit indicates if a bit in the STATUS_MFR_SPECIFIC command has been set.** 0_B No bit has been set. 1_B A bit has been set.
INPUT	13	rwh	**This bit indicates if an input voltage, input current, or input power fault or warning has occurred.** 0_B Fault or warning has not occurred. 1_B Fault or warning has occurred.
IOUT_POUT	14	rwh	**This bit indicates if an output current or output power fault or warning has occurred.** 0_B Fault or warning has not occurred. 1_B Fault or warning has occurred.
VOUT	15	rwh	**This bit indicates if an output voltage fault or warning has occurred.** 0_B Fault or warning has not occurred. 1_B Fault or warning has occurred.

2.17 STATUS_VOUT

This command returns one data byte with a summary of the output voltage fault and warnings.

STATUS_VOUT Address: $07A_H$

Reset value: 00_H

7	6	5	4	3	2	1	0
Res	**VOUT_OV_WARN**	**VOUT_UV_WARN**	**VOUT_UV_FAULT**	**Res**			
r	rwh	rwh	rwh	r			

Field	Bits	Type	Description
VOUT_UV_FAULT	4	rwh	**This bit indicates if an output undervoltage fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.
VOUT_UV_WARN	5	rwh	**This bit indicates if an output undervoltage warning has occurred.** 0_B Warning has not occurred. 1_B Warning has occurred.

(table continues...)

(continued)

Field	Bits	Type	Description
VOUT_OV_WARN	6	rwh	**This bit indicates if an output overvoltage warning has occurred.** 0_B Warning has not occurred. 1_B Warning has occurred.

2.18 STATUS_IOUT

This command returns one data byte with a summary of the output current fault and warning status.

STATUS_IOUT Address: $07B_H$

Reset value: 00_H

7	6	5	4	3	2	1	0
IOUT_OC_FAULT	**Res**	**IOUT_OC_WARN**	**Res**				
rwh	r	rwh	r				

Field	Bits	Type	Description
IOUT_OC_WARN	5	rwh	**This bit indicates if an output overcurrent warning has occurred.** 0_B Warning has not occurred. 1_B Warning has occurred.
IOUT_OC_FAULT	7	rwh	**This bit indicates if an output overcurrent fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.

2.19 STATUS_INPUT

This command returns one data byte with a summary of the system input fault and warning status.

STATUS_INPUT Address: $07C_H$

Reset value: 00_H

7	6	5	4	3	2	1	0
VIN_OV_FAULT	**VIN_OV_WARN**	**VIN_UV_WARN**	**VIN_UV_FAULT**	**Res**			**PIN_OP_WARN**
rwh	rwh	rwh	rwh	r			rwh

Field	Bits	Type	Description
PIN_OP_WARN	0	rwh	**This bit indicates if an input over-power warning has occurred.** 0_B Warning has not occurred. 1_B Warning has occurred.
VIN_UV_FAULT	4	rwh	**This bit indicates if an input undervoltage fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.

(table continues...)

(continued)

Field	Bits	Type	Description
VIN_UV_WARN	5	rwh	**This bit indicates if an input undervoltage warning has occurred.** 0_B Warning has not occurred. 1_B Warning has occurred.
VIN_OV_WARN	6	rwh	**This bit indicates if an input overvoltage warning has occurred.** 0_B Warning has not occurred. 1_B Warning has occurred.
VIN_OV_FAULT	7	rwh	**This bit indicates if an input overvoltage fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.

2.20 STATUS_TEMPERATURE

This command returns one data byte with a summary of the internal MOSFET's overtemperature fault and warning status.

STATUS_TEMPERATURE Address: $07D_H$

Reset value: 00_H

7	6	5	4	3	2	1	0
OT_FAULT	**OT_WARN**	**Res**					
rwh	rwh	r					

Field	Bits	Type	Description
OT_WARN	6	rwh	**This bit indicates if an overtemperature warning has occurred.** 0_B Warning has not occurred. 1_B Warning has occurred.
OT_FAULT	7	rwh	**This bit indicates if an overtemperature fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.

2.21 STATUS_CML

This command returns one data byte with a summary of the communication interface fault and warning status.

STATUS_CML Address: $07E_H$

Reset value: 00_H

7	6	5	4	3	2	1	0
INVALID_CMD	**INVALID_DATA**	**PEC_FAIL**	**MEM_FAULT**	**Res**		**OTHER**	**Res**
rwh	rwh	rwh	rwh	r		rwh	r

Field	Bits	Type	Description
OTHER	1	rwh	**This bit indicates if a miscellaneous communications fault has occurred.** 0_B No miscellaneous fault has occurred. 1_B Miscellaneous fault has occurred.
MEM_FAULT	4	rwh	**This bit indicates if an OTP fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.
PEC_FAIL	5	rwh	**This bit indicates Packet Error Check status.** 0_B Packet Error Check has not failed. 1_B Packet Error Check failed.
INVALID_DATA	6	rwh	**This bit indicates if an invalid or unsupported data received.** 0_B Invalid or unsupported data not received. 1_B Invalid or unsupported data received.
INVALID_CMD	7	rwh	**This bit indicates if an invalid or unsupported command received.** 0_B Invalid or unsupported command not received. 1_B Invalid or unsupported command received.

2.22 STATUS_OTHER

This command returns one data byte with SMBALERT# pin status.

STATUS_OTHER Address: $07F_H$
Reset value: 00_H

7	6	5	4	3	2	1	0
Res							**SMBALERT**
r							rwh

Field	Bits	Type	Description
SMBALERT	0	rwh	**This bit indicates if the device is First To Assert SMBALERT# pin status.** 0_B Not the First To Assert SMBALERT# pin. 1_B First To Assert SMBALERT# pin.

2.23 STATUS_MFR_SPECIFIC

This command returns one data byte with a summary of the general device status.

STATUS_MFR_SPECIFIC Address: 080_H
Reset value: 00_H

7	6	5	4	3	2	1	0
Res		**SYNC_FAULT**	**VDS_FAULT**	**STATUS_LATCH_OFF**	**SOC_FAULT**	**WATCHDOG_FAULT**	**FET_HEALTH**
r		rwh	rwh	rh	rwh	rwh	rwh

Field	Bits	Type	Description
FET_HEALTH	0	rwh	**This bit indicates if any MOSFET faults have occured.** 0_B No MOSFET faults occured. 1_B One or more MOSFET faults occured.
WATCHDOG_FAULT	1	rwh	**This bit indicates if a MOSFET start-up watchdog fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.
SOC_FAULT	2	rwh	**This bit indicates if a severe overcurrent (SOC) fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.
STATUS_LATCH_OFF	3	rh	**This bit indicates the device latch-off status.** 0_B Device is not in latch-off state. 1_B Device is in latch-off state.
VDS_FAULT	4	rwh	**This bit indicates if a VDS fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.
SYNC_FAULT	5	rwh	**This bit indicates if a synchronization (SYNC) fault has occurred.** 0_B Fault has not occurred. 1_B Fault has occurred.

2.24 READ_EIN

This command returns the input energy reading in direct format.

READ_EIN

Address: 086_H

Reset value: $0000\ 0000\ 0000_H$

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
SAMPLE_COUNT															
rh															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SAMPLE_COUNT								ROLLOVER_COUNT								ENERGY_COUNT															
rh								rh								rh															

Field	Bits	Type	Description
ENERGY_COUNT	15:0	rh	**Output of an accumulator that continuously sums samples of the instantaneous input power.**
ROLLOVER_COUNT	23:16	rh	**Unsigned integer that will periodically roll over from its maximum positive value to zero.**
SAMPLE_COUNT	47:24	rh	**Unsigned integer that counts the number of samples of the instantaneous input power.**

2.25 READ_VIN

This command returns the input voltage reading measured at the VINS pin in direct format.

READ_VIN Address: 088_H

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**READ_VIN**											
r				rh											

Field	Bits	Type	Description
READ_VIN	11:0	rh	**Input voltage reading.**

2.26 READ_VOUT

This command returns the output voltage reading measured at the VOUTS pin in direct format.

READ_VOUT Address: $08B_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**READ_VOUT**											
r				rh											

Field	Bits	Type	Description
READ_VOUT	11:0	rh	**Output voltage reading.**

2.27 READ_IOUT

This command returns the current reading by measuring the IMON pin voltage, in direct format.

READ_IOUT Address: $08C_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**READ_IOUT**											
r				rh											

Field	Bits	Type	Description
READ_IOUT	11:0	rh	**Current reading.**

2.28 READ_TEMPERATURE_1

This command returns the internal MOSFET temperature reading in direct format.

READ_TEMPERATURE_1 Address: $08D_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**READ_TEMPERATURE_1**											
r				rh											

Field	Bits	Type	Description
READ_TEMPERATURE_1	11:0	rh	**Internal MOSFET temperature reading.**

2.29 READ_TEMPERATURE_2

This command returns the controller's on-chip temperature reading measured by the internal temperature sensor, in direct format.

READ_TEMPERATURE_2

Address: $08E_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**READ_TEMPERATURE_2**											
r				rh											

Field	Bits	Type	Description
READ_TEMPERATURE_2	11:0	rh	**Controller's on-chip temperature reading.**

2.30 READ_PIN

This command returns the input power (PIN = VIN * IOUT) reading in direct format.

READ_PIN

Address: 097_H

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ_PIN															
rh															

Field	Bits	Type	Description
READ_PIN	15:0	rh	**Input power reading.**

2.31 PMBUS_REVISION

This command stores the revision of the PMBus® to which the device is compliant.

PMBUS_REVISION

Address: 098_H

Reset value: 33_H

7	6	5	4	3	2	1	0
PMBUS_P1_REVISION				PMBUS_P2_REVISION			
rh				rh			

Field	Bits	Type	Description
PMBUS_P2_REVISION	3:0	rh	**0x3 indicates part 2 is revision 1.3**
PMBUS_P1_REVISION	7:4	rh	**0x3 indicates part 1 is revision 1.3**

2.32 MFR_ID

This command stores the manufacturer ID according to ISO/IEC 8859-1 [A05].

MFR_ID

Address: 099_H

Reset value: $00\ 4649_H$

23	22	21	20	19	18	17	16
MFR_ID							
rh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MFR_ID															
rh															

Field	Bits	Type	Description
MFR_ID	23:0	rh	**Manufacturer's ID**

2.33 MFR_MODEL

This command contains a string to identify the device model in ASCII.

MFR_MODEL

Address: $09A_H$

Reset values see: Table 2

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
MFR_MODEL																															
r																															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MFR_MODEL																															
r																															

Field	Bits	Type	Description
MFR_MODEL	63:0	r	**Device model identifier string.**

Table 2 Reset values of MFR_MODEL

Reset	Reset value	Note
Reset	0000 3032 3750 4458$_H$	XDP720 device identifier.

2.34 MFR_REVISION

This command is used to read the manufactur's revision number.

MFR_REVISION Address: 09B$_H$
Reset value: 0001$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MFR_REVISION															
rh															

Field	Bits	Type	Description
MFR_REVISION	15:0	rh	**Manufacturer revision (silicon version).**

2.35 VIN_OV_FAULT_LIMIT_S

This command sets the value of the input voltage that causes an input overvoltage (OV) fault along with its hysteresis, only in a digital comparator based SECONDARY configured device.

VIN_OV_FAULT_LIMIT_S Address: 0CD$_H$
Reset value: 3BA2$_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	VIN_OV_HYST_S			VIN_OV_FAULT_LIMIT_S											
r	rw			rw											

Field	Bits	Type	Description
VIN_OV_FAULT_LIMIT_S	11:0	rw	**SECONDARY device's OV fault limit can be programmed from 0 to 22 V, 0 to 44 V or 0 to 88 V (absolute value) depending on VTLM_RNG settings.**
VIN_OV_HYST_S	14:12	rw	**Programmable digital hysteresis for SECONDARY device's OV fault limit at respective VTLM_RNG voltages.** 000$_B$ Typ Hysteresis of 1 V at 88 V VTLM_RNG voltage full scale 001$_B$ Typ Hysteresis of 2 V at 88 V VTLM_RNG voltage full scale 010$_B$ Typ Hysteresis of 3 V at 88 V VTLM_RNG voltage full scale 011$_B$ Typ Hysteresis of 4 V at 88 V VTLM_RNG voltage full scale 100$_B$ Typ Hysteresis of 5 V at 88 V VTLM_RNG voltage full scale 101$_B$ Typ Hysteresis of 6 V at 88 V VTLM_RNG voltage full scale 110$_B$ Typ Hysteresis of 7 V at 88 V VTLM_RNG voltage full scale 111$_B$ Typ Hysteresis of 8 V at 88 V VTLM_RNG voltage full scale

2.36 VIN_UV_FAULT_LIMIT_S

This command sets the value of the input voltage that causes an input undervoltage (UV) fault along with its hysteresis, only in a digital comparator based SECONDARY configured device.

VIN_UV_FAULT_LIMIT_S

Address: $0CE_H$

Reset value: 2674_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIN_UV_HYST_S				**VIN_UV_FAULT_LIMIT_S**											
rw				rw											

Field	Bits	Type	Description
VIN_UV_FAULT_LIMIT_S	11:0	rw	**SECONDARY device's UV fault limit can be programmed from 0 to 22 V, 0 to 44 V or 0 to 88 V (absolute value) depending on VTLM_RNG settings.**
VIN_UV_HYST_S	15:12	rw	**Programmable digital hysteresis for SECONDARY device's UV fault limit at respective VTLM_RNG voltages.** 0_H Typ Hysteresis of 2 V at 88 V VTLM_RNG voltage full scale 1_H Typ Hysteresis of 3 V at 88 V VTLM_RNG voltage full scale 2_H Typ Hysteresis of 4 V at 88 V VTLM_RNG voltage full scale 3_H Typ Hysteresis of 5 V at 88 V VTLM_RNG voltage full scale 4_H Typ Hysteresis of 6 V at 88 V VTLM_RNG voltage full scale 5_H Typ Hysteresis of 7 V at 88 V VTLM_RNG voltage full scale 6_H Typ Hysteresis of 8 V at 88 V VTLM_RNG voltage full scale 7_H Typ Hysteresis of 9 V at 88 V VTLM_RNG voltage full scale 8_H Typ Hysteresis of 9.5 V at 88 V VTLM_RNG voltage full scale 9_H Typ Hysteresis of 10 V at 88 V VTLM_RNG voltage full scale A_H Typ Hysteresis of 10.5 V at 88 V VTLM_RNG voltage full scale B_H Typ Hysteresis of 11 V at 88 V VTLM_RNG voltage full scale C_H Typ Hysteresis of 11.5 V at 88 V VTLM_RNG voltage full scale D_H Typ Hysteresis of 12 V at 88 V VTLM_RNG voltage full scale E_H Typ Hysteresis of 12.5 V at 88 V VTLM_RNG voltage full scale F_H Typ Hysteresis of 13 V at 88 V VTLM_RNG voltage full scale

2.37 PMBUS_CFG

This command configures the PMBus® device address and communication bus speed.

PMBUS_CFG

Address: $0D0_H$

Reset value: 10_H

7	6	5	4	3	2	1	0
PMBUS_SPEED	**PMBUS_BASE_ADDR**			**PMBUS_DEVICE_ADDR**			
rw	rw			rw			

Field	Bits	Type	Description
PMBUS_DEVICE_ADDR	3:0	rw	**LSB part of the PMBus® address [3:0].**
PMBUS_BASE_ADDR	6:4	rw	**MSB part of the PMBus® address [6:4].**
PMBUS_SPEED	7	rw	**Operating PMBus® speed.** 0_B Fast Mode Plus 1_B Standard or Fast Mode

2.38 MODE

This command is used for configuring the comparator modes and quick output discharge function.

MODE Address: $0D1_H$

Reset value: 0183_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res							MODE_P	MODE_S	QOD_EN	Res					
r							rw	rw	rw	r					

Field	Bits	Type	Description
QOD_EN	6	rw	**Enable Quick Output Discharge (QOD).** 0_B QOD Disable 1_B QOD Enable
MODE_S	7	rw	**In a SECONDARY configured device, this bit is used to select between analog and digital comparators for UV & OV faults.** 0_B OV and UV - Analog Comparators Mode (ACM) 1_B OV and UV - Digital Comparators Mode (DCM)
MODE_P	8	rw	**In a PRIMARY configured device, this bit is used to select between analog and digital comparators for UV & OV faults.** 0_B OV and UV - Analog Comparators Mode (ACM) 1_B OV and UV - Digital Comparators Mode (DCM)

2.39 V_SNS_CFG

This command configures the voltage faults and hysteresis levels.

V_SNS_CFG Address: $0D4_H$

Reset value: 0428_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	VDS_FAULT_LIMIT		VIN_OV_HYST			VIN_UV_HYST				OVIN_FAULT_LIMIT		UV_TH_HYST		Res	
r	rw		rw			rw				rw		rw		r	

Field	Bits	Type	Description
UV_TH_HYST	3:2	rw	**Programmable digital hysteresis for UV THROTTLE** 00_B Typ Hysteresis of 0.5 V 01_B Typ Hysteresis of 1 V 10_B Typ Hysteresis of 2 V 11_B Typ Hysteresis of 4 V
OVIN_FAULT_LIMIT	5:4	rw	**OVIN_FAULT_LIMIT bit field sets the value of the input voltage that causes input overvoltage (OVIN) fault.** 00_B 70 V 01_B 75 V 10_B 80 V 11_B 85 V
VIN_UV_HYST	9:6	rw	**Programmable digital hysteresis for UV fault at respective VTLM_RNG voltages, only in a PRIMARY configured device.** 0_H Typ Hysteresis of 2 / 1 / 0.5 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 1_H Typ Hysteresis of 3 / 1.5 / 0.75 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 2_H Typ Hysteresis of 4 / 2 / 1 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 3_H Typ Hysteresis of 5 / 2.5 / 1.25 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 4_H Typ Hysteresis of 6 / 3 / 1.5 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 5_H Typ Hysteresis of 7 / 3.5 / 1.75 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 6_H Typ Hysteresis of 8 / 4 / 2 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 7_H Typ Hysteresis of 9 / 4.5 / 2.25 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 8_H Typ Hysteresis of 9.5 / 4.75 / 2.375 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 9_H Typ Hysteresis of 10 / 5 / 2.5 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V A_H Typ Hysteresis of 10.5 / 5.25 / 2.625 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V B_H Typ Hysteresis of 11 / 5.5 / 2.75 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V C_H Typ Hysteresis of 11.5 / 5.75 / 2.875 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V D_H Typ Hysteresis of 12 / 6 / 3 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V E_H Typ Hysteresis of 12.5 / 6.25 / 3.125 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V F_H Typ Hysteresis of 13 / 6.5 / 3.25 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V

(table continues...)

(continued)

Field	Bits	Type	Description
VIN_OV_HYST	12:10	rw	**Programmable digital hysteresis for OV fault at respective VTLM_RNG voltages, only in a PRIMARY configured device.** 000_B Typ Hysteresis of 1 / 0.5 / 0.25 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 001_B Typ Hysteresis of 2 / 1 / 0.5 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 010_B Typ Hysteresis of 3 / 1.5 / 0.75 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 011_B Typ Hysteresis of 4 / 2 / 1 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 100_B Typ Hysteresis of 5 / 2.5 / 1.25 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 101_B Typ Hysteresis of 6 / 3 / 1.5 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 110_B Typ Hysteresis of 7 / 3.5 / 1.75 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 111_B Typ Hysteresis of 8 / 4 / 2 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V
VDS_FAULT_LIMIT	14:13	rw	**This bit field sets the value of the MOSFET's Vds level that causes a pre-charged output voltage (VDS) fault.** 00_B Typ threshold of 10 / 5 / 2.5 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 01_B Typ threshold of 20 / 10 / 5 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 10_B Typ threshold of 30 / 15 / 7.5 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V 11_B Typ threshold of 35 / 17.5 / 8.75 V at respective VTLM_RNG voltage full scale 88 / 44 / 22 V

2.40 I_SNS_CFG1

This command configures the overcurrent fault limits.

I_SNS_CFG1

Address: $0D5_H$

Reset value: $4D50_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**SYS_OC_LIMIT**								**LOCAL_OC_LIMIT**						
r	rw								r						

Field	Bits	Type	Description
LOCAL_OC_LIMIT	6:0	r	**This bit field configures the local overcurrent limit from 0 A to 69.85 A with 0.55A resolution.**
SYS_OC_LIMIT	14:7	rw	**This bit field configures the system overcurrent limit for the IMON pin voltage.**

2.41 I_SNS_CFG2

This command configures the start-up current limit and severe overcurrent fault limits.

I_SNS_CFG2

Address: $0D6_H$

Reset value: 5942_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	SOC_LIMIT_S						SOC_LIMIT_P						START_ILIM		
r	rw						rw						rw		

Field	Bits	Type	Description
START_ILIM	2:0	rw	**This bit field sets the start-up current limit.** 000_B 100% of max startup current. 001_B 75% of max startup current. 010_B 50% of max startup current. 011_B 25% of max startup current. 100_B 15% of max startup current. 101_B 12,5% of max inrush current. 110_B 9% of max startup current. 111_B 5% of max startup current.
SOC_LIMIT_P	8:3	rw	**In a PRIMARY configured device, this bit field sets the SOC fault limit from 0 A to 138.6 A with 2.2 A resolution step.**
SOC_LIMIT_S	14:9	rw	**In a SECONDARY configured device, this bit field sets the SOC fault limit from 0 A to 138.6 A with 2.2 A resolution step.**

2.42 UV_TH_TMR

This command configures the UV throttle timers.

UV_TH_TMR

Address: $0D7_H$

Reset value: 2828_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UV_TH_DEGLITCH_TMR								UV_TH_RECOVERY_TMR							
rw								rw							

Field	Bits	Type	Description
UV_TH_RECOVERY_TMR	7:0	rw	**Programmable deglitch time for UV throttle rising edge, from 0 ms to 127.5 ms with 0.5 ms resolution step.**
UV_TH_DEGLITCH_TMR	15:8	rw	**Programmable deglitch time for UV throttle falling edge, from 0 ms to 127.5 ms with 0.5 ms resolution step.**

2.43 WATCHDOG_TMR

This command configures the maximum allowed MOSFET start-up time and the enable deglitch time.

WATCHDOG_TMR Address: $0D8_H$

Reset value: 0329_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					**SURGE_REC_WD**			**EN_DG**				**WATCHDOG**			
r					rw			r				rw			

Field	Bits	Type	Description
WATCHDOG	3:0	rw	**This bit field sets an upper limit on how long the device can attempt to turn-on the output without fully enhancing the MOSFET.** 0_H 5 ms 1_H 10 ms 2_H 20 ms 3_H 50 ms 4_H 75 ms 5_H 100 ms 6_H 200 ms 7_H 500 ms 8_H 750 ms 9_H 1000 ms A_H 2000 ms B_H 3000 ms C_H 5000 ms D_H 7500 ms E_H 10000 ms F_H 15000 ms
EN_DG	7:4	r	**This bit field sets the deglitch time from the moment when the EN pin crosses the VEN_UV_UTH until the INIT_SOA_REG phase starts.** 0_H 0 ms 1_H 4 ms 2_H 8 ms 3_H 16 ms 4_H 32 ms 5_H 64 ms 6_H 128 ms 7_H 256 ms 8_H 300 ms 9_H 400 ms A_H 512 ms B_H NA … F_H NA

(table continues...)

(continued)

Field	Bits	Type	Description
SURGE_REC_WD	10:8	rw	**Surge protection watchdog timer.** 000_B Timer set by WATCHDOG_TMR:WATCHDOG bit. 001_B 1 ms 010_B 2 ms 011_B 5 ms 100_B 10 ms 101_B 20 ms 110_B 50 ms 111_B 100 ms

2.44 V_TMR

This command configures the voltage faults timers.

V_TMR Address: $0D9_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				OVIN_TMR			OUV_TMR			OV_TMR			UV_TMR		
r				rw			rw			rw			rw		

Field	Bits	Type	Description
UV_TMR	2:0	rw	**This bit field specifies the amount of operating time in undervoltage conditions before UV fault is triggered.** 000_B 0 ms 001_B 1 ms 010_B 5 ms 011_B 10 ms 100_B 50 ms 101_B 100 ms 110_B 500 ms 111_B 1000 ms
OV_TMR	5:3	rw	**This specifies the amount of operating time in overvoltage conditions before OV fault is triggered.** 000_B 0 ms 001_B 1 ms 010_B 5 ms 011_B 10 ms 100_B 50 ms 101_B 100 ms 110_B 500 ms 111_B 1000 ms

(table continues...)

(continued)

Field	Bits	Type	Description
OUV_TMR	8:6	rw	**This specifies the amount of operating time in output-undervoltage conditions before OUV fault is triggered.** 000_B 0 ms 001_B 1 ms 010_B 5 ms 011_B 10 ms 100_B 50 ms 101_B 100 ms 110_B 500 ms 111_B 1000 ms
OVIN_TMR	11:9	rw	**This specifies the amount of operating time in on-chip input overvoltage conditions before OVIN fault is triggered.** 000_B 0 µs 001_B 10 µs 010_B 20 µs 011_B 50 µs 100_B 100 µs 101_B 200 µs 110_B 500 µs 111_B 1000 µs

2.45 GPO_CFG

This command configures the general purpose pins.

GPO_CFG Address: $0DB_H$

Reset value: 0300_H

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1	0
Res	**SMBALERT**	**Res**	**GPO2_CFG**	**GPO1_CFG**	**GPO0_CFG**	**Res**	**GPO 1_ST**	**GPO 0_ST**
r	rw	r	rw	rw	rw	r	rw	rw

Field	Bits	Type	Description
GPO0_ST	0	rw	**This bit sets the state (high or low) of GPO0 pin when it is configured as GPO. It doesn't have any effect when the pin is configured as FAULT or SMBALERT#.** 0_B Output low. 1_B Output high.
GPO1_ST	1	rw	**This bit sets the state (high or low) of GPO1 pin when it is configured as GPO. It doesn't have any effect when the pin is configured as WARN or LED.** 0_B Output low. 1_B Output high.

(table continues...)

(continued)

Field	Bits	Type	Description
GPO0_CFG	5:4	rw	**This bit field configures GPO0 pin.** 00_B Pin is configured as FAULT#. 01_B Pin reflects GPO0_ST status. 10_B NA. 11_B Pin is configured as SMBALERT#, depending on the GPO_CFG.SMBALERT
GPO1_CFG	7:6	rw	**This bit field configures GPO1 pin.** 00_B Pin is configured as WARN#. 01_B Pin reflects GPO1_ST status. 10_B NA. 11_B NA.
GPO2_CFG	9:8	rw	**This bit field configures GPO2 pin.** 00_B Pin is configured as functional. 01_B Pin is configured as UV THROTTLE. 10_B NA. 11_B Pin is configured as RESTARTN with internal pull-up resistor.
SMBALERT	13:12	rw	**This bit field is used to configure the SMBALERT#.** 00_B SMBALERT# is disabled, open drain. 01_B SMBALERT# is configured only for faults. 10_B SMBALERT# is configured only for warnings. 11_B SMBALERT# is configured for faults and warnings.

2.46 IOUT_UC_WARN_LIMIT

This command sets the current level that causes an output undercurrent (OUC) warning.

IOUT_UC_WARN_LIMIT

Address: $0DC_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**IOUT_UC_WARN_AVG**			**IOUT_UC_WARN_LIMIT**											
r	rw			rw											

Field	Bits	Type	Description
IOUT_UC_WARN_LIMIT	11:0	rw	**This bit field sets the OUC warning limit, refer datasheet for details.**

(table continues...)

(continued)

Field	Bits	Type	Description
IOUT_UC_WARN_AVG	14:12	rw	**This bit field specifies the number of samples to be averaged for OUC warning limit.** 000_B 1 sample. 001_B 2 samples. 010_B 4 samples. 011_B 8 samples. 100_B 16 samples. 101_B 32 samples. 110_B 64 samples. 111_B 128 samples.

2.47 ONCHIP_TSD_FAULT_LIMIT

This command sets the temperature of the device, in degree Celsius, measured by the internal temperature sensor, at which the on-chip thermal shut down (TSD) fault is triggered.

ONCHIP_TSD_FAULT_LIMIT Address: $0DD_H$

Reset value: 02_H

7	6	5	4	3	2	1	0
Res						**ONCHIP_TSD_FAULT_LIMIT**	
r						rw	

Field	Bits	Type	Description
ONCHIP_TSD_FAULT_LIMIT	1:0	rw	**This bit field sets the TSD fault limit.** 00_B 125°C 01_B 135°C 10_B 145°C 11_B NA

2.48 ENABLE_FAULTS

This command is used for enabling or disabling the faults.

ENABLE_FAULTS Address: $0DE_H$

Reset value: $FFDB_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDS	**OT**	**UR**	**UV**	**OV**	**OVIN**	**OUV**	**SYNC**	**WD**	**OC**	**Res**	**SOC**	**TSD**	**Res**	**FET_GD**	**FET_GS**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	r	rw	rw

Field	Bits	Type	Description
FET_GS	0	rw	**This bit enables or disables shorted MOSFET Gate-Source (SGD) fault.** 0_B Fault is disabled. 1_B Fault is enabled.
FET_GD	1	rw	**This bit enables or disables shorted MOSFET Gate-Drain (SGD) fault.** 0_B Fault is disabled. 1_B Fault is enabled.
TSD	3	rw	**This bit enables or disables controller's on-chip Thermal Shut-Down (TSD) fault.** 0_B Fault is disabled. 1_B Fault is enabled.
SOC	4	rw	**This bit enables or disables Sever Over-Current (SOC) fault.** 0_B Fault is disabled. 1_B Fault is enabled.
OC	6	rw	**This bit enables or disables Overcurrent (OC) fault.** 0_B Fault is disabled. 1_B Fault is enabled.
WD	7	rw	**This bit enables or disables unsuccessful MOSFET start-up i.e watchdog (WD) fault.** 0_B Fault is disabled. 1_B Fault is enabled.
SYNC	8	rw	**This bit enables or disables SYNC fault** 0_B Fault is disabled. 1_B Fault is enabled.
OUV	9	rw	**This bit enables or disables Output Under-Voltage (OUV) fault.** 0_B Fault is disabled. 1_B Fault is enabled.
OVIN	10	rw	**This bit enables or disables on-chip Input Over-Voltage (OVIN) fault.** 0_B Fault is disabled. 1_B Fault is enabled.
OV	11	rw	**This bit enables or disables system input Over-Voltage (OV) fault.** 0_B Fault is disabled. 1_B Fault is enabled.
UV	12	rw	**This bit enables or disables system input Under-Voltage (UV) fault.** 0_B Fault is disabled. 1_B Fault is enabled.
UR	13	rw	**This bit enables or disables Unsuccessful Retry (UR) fault.** 0_B Fault is disabled. 1_B Fault is enabled.

(table continues...)

(continued)

Field	Bits	Type	Description
OT	14	rw	**This bit enables or disables MOSFET Over-Temperature (OT) fault.** 0_B Fault is disabled. 1_B Fault is enabled.
VDS	15	rw	**This bit enables or disables Pre-charged output voltage (VDS) fault.** 0_B Fault is disabled. 1_B Fault is enabled.

2.49 MASK_FAULTS

This command determines which faults are reflected on the FAULT# pin.

MASK_FAULTS Address: $0DF_H$

Reset value: $FFDB_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDS	**OT**	**UR**	**UV**	**OV**	**OVIN**	**OUV**	**SYNC**	**WD**	**OC**	**Res**	**SOC**	**TSD**	**Res**	**FET_GD**	**FET_GS**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	r	rw	rw

Field	Bits	Type	Description
FET_GS	0	rw	**This bit masks or unmasks shorted MOSFET Gate-Source (SGD) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.
FET_GD	1	rw	**This bit masks or unmasks shorted MOSFET Gate-Drain (SGD) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.
TSD	3	rw	**This bit masks or unmasks controller's on-chip Thermal Shut-Down (TSD) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.
SOC	4	rw	**This bit masks or unmasks Sever Over-Current (SOC) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.
OC	6	rw	**This bit masks or unmasks Overcurrent (OC) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.
WD	7	rw	**This bit masks or unmasks unsuccessful MOSFET start-up i.e. watchdog (WD) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.

(table continues...)

(continued)

Field	Bits	Type	Description
SYNC	8	rw	**This bit masks or unmasks SYNC fault** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.
OUV	9	rw	**This bit masks or unmasks Output Under-Voltage (OUV) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.
OVIN	10	rw	**This bit masks or unmasks on-chip Input Over-Voltage (OVIN) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.
OV	11	rw	**This bit masks or unmasks system input Over-Voltage (OV) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.
UV	12	rw	**This bit masks or unmasks system input Under-Voltage (UV) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.
UR	13	rw	**This bit masks or unmasks Unsuccessful Retry (U#R) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.
OT	14	rw	**This bit masks or unmasks internal MOSFET's Over-Temperature (OT) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.
VDS	15	rw	**This bit masks or unmasks Pre-charged output voltage (TSD) fault.** 0_B Fault is not reflected on the FAULT# pin. 1_B Fault is reflected on the FAULT# pin.

2.50 STATUS_FAULTS

This command summarizes the status of all faults.

STATUS_FAULTS

Address: $0E0_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VDS	**OT**	**UR**	**UV**	**OV**	**OVIN**	**OUV**	**SYNC**	**WD**	**OC**	**Res**	**SOC**	**TSD**	**Res**	**FET_GD**	**FET_GS**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	r	rwh	rwh

Field	Bits	Type	Description
FET_GS	0	rwh	**This bit specifies the status of shorted MOSFET Gate-Source (SGS) fault.** 0_B Fault is not present. 1_B Fault is present.
FET_GD	1	rwh	**This bit specifies the status of shorted MOSFET Gate-Drain (SGD) fault.** 0_B Fault is not present. 1_B Fault is present.
TSD	3	rwh	**This bit specifies the status of the controller's on-chip Thermal Shut-Down (TSD) fault.** 0_B Fault is not present. 1_B Fault is present.
SOC	4	rwh	**This bit specifies the status of Sever Over-Current (SOC) fault.** 0_B Fault is not present. 1_B Fault is present.
OC	6	rwh	**This bit specifies the status of Overcurrent (OC) fault.** 0_B Fault is not present. 1_B Fault is present.
WD	7	rwh	**This bit specifies the status of unsuccessful MOSFET start-up i.e. watchdog (WD) fault.** 0_B Fault is not present. 1_B Fault is present.
SYNC	8	rwh	**This bit specifies the status of SYNC fault.** 0_B Fault is not present. 1_B Fault is present.
OUV	9	rwh	**This bit specifies the status of Output Under-Voltage (OUV) fault.** 0_B Fault is not present. 1_B Fault is present.
OVIN	10	rwh	**This bit specifies the status of on-chip Input Over-Voltage (OVIN) fault.** 0_B Fault is not present. 1_B Fault is present.
OV	11	rwh	**This bit specifies the status of system input Over-Voltage (OV) fault.** 0_B Fault is not present. 1_B Fault is present.
UV	12	rwh	**This bit specifies the status of system input Under-Voltage (UV) fault.** 0_B Fault is not present. 1_B Fault is present.

(table continues...)

(continued)

Field	Bits	Type	Description
UR	13	rwh	**This bit specifies the status of Unsuccessful Retry (UR) fault.** 0_B Fault is not present. 1_B Fault is present.
OT	14	rwh	**This bit specifies the status of the internal MOSFET's Over-Temperature (UR) fault.** 0_B Fault is not present. 1_B Fault is present.
VDS	15	rwh	**This bit specifies the status of Pre-charged output voltage (VDS) fault.** 0_B Fault is not present. 1_B Fault is present.

2.51 ENABLE_WARNS

This command is used for enabling or disabling the warnings.

ENABLE_WARNS Address: $0E1_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			COMM	OP	UV	OV	OUV	OOV	OOC	OUC	Res	OT	TSD	FET_GS	Res
r			rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	r

Field	Bits	Type	Description
FET_GS	1	rw	**This bit enables or disables MOSFET's Gate-Source Low Voltage (VGSL) warning.** 0_B Warning is disabled. 1_B Warning is enabled.
TSD	2	rw	**This bit enables or disables controller's on-chip Thermal Shut-Down (TSD) warning.** 0_B Warning is disabled. 1_B Warning is enabled.
OT	3	rw	**This bit enables or disables internal MOSFET's Over-Temperature (OT) warning.** 0_B Warning is disabled. 1_B Warning is enabled.
OUC	5	rw	**This bit enables or disables Output Under-Current (OUC) warning.** 0_B Warning is disabled. 1_B Warning is enabled.
OOC	6	rw	**This bit enables or disables Output Over-Current (OOC) warning.** 0_B Warning is disabled. 1_B Warning is enabled.

(table continues...)

(continued)

Field	Bits	Type	Description
OOV	7	rw	**This bit enables or disables Output Over-Voltage (OOV) warning.** 0_B Warning is disabled. 1_B Warning is enabled.
OUV	8	rw	**This bit enables or disables Output Under-Voltage (OUV) warning.** 0_B Warning is disabled. 1_B Warning is enabled.
OV	9	rw	**This bit enables or disables Input Over-Voltage (OV) warning.** 0_B Warning is disabled. 1_B Warning is enabled.
UV	10	rw	**This bit enables or disables Input Under-Voltage (UV) warning.** 0_B Warning is disabled. 1_B Warning is enabled.
OP	11	rw	**This bit enables or disables Input Over-Power (OP) warning.** 0_B Warning is disabled. 1_B Warning is enabled.
COMM	12	rw	**This bit enables or disables PMBus® Interface Communication (COMM) warning.** 0_B Warning is disabled. 1_B Warning is enabled.

2.52 MASK_WARNS

This command determines which warnings are reflected in the WARN pin.

MASK_WARNS Address: $0E2_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			COMM	OP	UV	OV	OUV	OOV	OOC	OUC	Res	OT	TSD	FET_GS	Res
r			rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	r

Field	Bits	Type	Description
FET_GS	1	rw	**This bit masks or unmasks MOSFET's Gate-Source Low Voltage (VGSL) warning.** 0_B Warning is not reflected on the WARN# pin. 1_B Warning is reflected on the WARN# pin.
TSD	2	rw	**This bit masks or unmasks controller's on-chip Thermal Shut-Down (TSD) warning.** 0_B Warning is not reflected on the WARN# pin. 1_B Warning is reflected on the WARN# pin.

(table continues...)

(continued)

Field	Bits	Type	Description
OT	3	rw	**This bit masks or unmasks internal MOSFET's Over-Temperature (OT) warning.** 0_B Warning is not reflected on the WARN# pin. 1_B Warning is reflected on the WARN# pin.
OUC	5	rw	**This bit masks or unmasks Output Under-Current (OUC) warning.** 0_B Warning is not reflected on the WARN# pin. 1_B Warning is reflected on the WARN# pin.
OOC	6	rw	**This bit masks or unmasks Output Over-Current (OOC) warning.** 0_B Warning is not reflected on the WARN# pin. 1_B Warning is reflected on the WARN# pin.
OOV	7	rw	**This bit masks or unmasks Output Over-Voltage (OOV) warning.** 0_B Warning is not reflected on the WARN# pin. 1_B Warning is reflected on the WARN# pin.
OUV	8	rw	**This bit masks or unmasks Output Under-Voltage (OUV) warning.** 0_B Warning is not reflected on the WARN# pin. 1_B Warning is reflected on the WARN# pin.
OV	9	rw	**This bit masks or unmasks Input Over-Voltage (OV) warning.** 0_B Warning is not reflected on the WARN# pin. 1_B Warning is reflected on the WARN# pin.
UV	10	rw	**This bit masks or unmasks Input Under-Voltage (UV) warning.** 0_B Warning is not reflected on the WARN# pin. 1_B Warning is reflected on the WARN# pin.
OP	11	rw	**This bit masks or unmasks Input Over-Power (OP) warning.** 0_B Warning is not reflected on the WARN# pin. 1_B Warning is reflected on the WARN# pin.
COMM	12	rw	**This bit masks or unmasks PMBus® Interface Communication (COMM) warning.** 0_B Warning is not reflected on the WARN# pin. 1_B Warning is reflected on the WARN# pin.

2.53 STATUS_WARNS

This command summarizes the warnings status.

STATUS_WARNS Address: $0E3_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			COMM	OP	UV	OV	OUV	OOV	OOC	OUC	Res	OT	TSD	FET_GS	Res
r			rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh	r

Field	Bits	Type	Description
FET_GS	1	rwh	**This bit specifies the status of MOSFET's Gate-Source Low Voltage (VGSL) warning.** 0_B Warning is not present. 1_B Warning is present.
TSD	2	rwh	**This bit specifies the internal MOSFET's Over-Temperature (OT) warning.** 0_B Warning is not present. 1_B Warning is present.
OT	3	rwh	**This bit specifies the status of the internal MOSFET's Over-Temperature (OT) warning.** 0_B Warning is not present. 1_B Warning is present.
OUC	5	rwh	**This bit specifies the status of Output Under-Current (OUC) warning.** 0_B Warning is not present. 1_B Warning is present.
OOC	6	rwh	**This bit specifies the status of Output Over-Current (OOC) warning.** 0_B Warning is not present. 1_B Warning is present.
OOV	7	rwh	**This bit specifies the status of Output Over-Voltage (OOV) warning.** 0_B Warning is not present. 1_B Warning is present.
OUV	8	rwh	**This bit specifies the status of Output Under-Voltage (OUV) warning.** 0_B Warning is not present. 1_B Warning is present.
OV	9	rwh	**This bit specifies the status of Input Over-Voltage (OV) warning.** 0_B Warning is not present. 1_B Warning is present.
UV	10	rwh	**This bit specifies the status of Input Under-Voltage (UV) warning.** 0_B Warning is not present. 1_B Warning is present.
OP	11	rwh	**This bit specifies the status of Input Over-Power (OP) warning.** 0_B Warning is not present. 1_B Warning is present.
COMM	12	rwh	**This bit specifies the status of PMBus® Interface Communication (COMM) warning.** 0_B Warning is not present. 1_B Warning is present.

2.54 PWRGD_DG_TMR

This command sets the deglitch time after PWRGD signal assertion and deassertion.

PWRGD_DG_TMR

Address: $0E4_H$

Reset value: 50_H

7	6	5	4	3	2	1	0
PWRGD_DG_TMR				PWRGDN_DG_TMR			
rw				rw			

Field	Bits	Type	Description
PWRGDN_DG_TMR	3:0	rw	**This bit field sets the PWRGD signal deassertion deglitch time from 0 ms to 15 ms in 1 ms steps.**
PWRGD_DG_TMR	7:4	rw	**This bit field sets the PWRGD signal assertion deglitch time from 0 ms to 15 ms in 1 ms steps.**

2.55 SOA_TMR

This command is used to configure the current fault timers.

SOA_TMR

Address: $0E5_H$

Reset value: 0143_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					SOC_DG_TMR		LOCAL_OC_TMR	OCD_TMR			SOAD_TMR				
r					rw		rw	rw			rw				

Field	Bits	Type	Description
SOAD_TMR	4:0	rw	**This bit field sets the deglitch time for the detection of system overcurrent limit and local overcurrent limit, depending on the LOCAL_OC_TMR bit.** 00_H 0 ms 01_H 0.5 ms 02_H 1 ms 03_H 2 ms 04_H 4 ms 05_H 6 ms 06_H 8 ms 07_H 10 ms 08_H 15 ms 09_H 20 ms $0A_H$ 25 ms $0B_H$ 30 ms $0C_H$ 40 ms $0D_H$ 50 ms $0E_H$ 75 ms $0F_H$ 100 ms 10_H 125 ms 11_H 150 ms 12_H 175 ms 13_H 200 ms 14_H 250 ms 15_H 300 ms 16_H 350 ms 17_H 400 ms 18_H 500 ms 19_H 600 ms $1A_H$ 700 ms $1B_H$ 800 ms $1C_H$ 900 ms $1D_H$ 1000 ms $1E_H$ 1500 ms $1F_H$ 2000 ms
OCD_TMR	7:5	rw	**This bit filed sets the deglitch time for the detection of local overcurrent limit.** 000_B 50 µs 001_B 100 µs 010_B 200 µs 011_B 300 µs 100_B 400 µs 101_B 500 µs 110_B 7500 µs 111_B 1000 µs

(table continues...)

(continued)

Field	Bits	Type	Description
LOCAL_OC_TMR	8	rw	**This bit selects the deglitch timer for local overcurrent limit.** 0_B SOAD_TMR is the deglitch timer for local overcurrent limit. 1_B OCD_TMR is the deglitch timer for local overcurrent limit.
SOC_DG_TMR	10:9	rw	**This bit filed sets the deglitch time for the detection of severe overcurrent limit.** 00_B 0 ns 01_B 200 ns 10_B 500 ns 11_B 1000 ns

2.56 TURN_OFF_CTRL

This command configures the strength of the regular gate pull-down for non-critical faults (i.e. except OVIN and SOC faults).

TURN_OFF_CTRL Address: $0E6_H$

Reset value: 0006_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res													GATE_SLOW_PD		Res
r													rw		r

Field	Bits	Type	Description
GATE_SLOW_PD	2:1	rw	**This bit field sets the regular gate pull-down strength.** 00_B 250 µA 01_B 500 µA 10_B 750 µA 11_B 1250 µA

2.57 RETRY

This command is used to configure the auto-retry settings, input surge immunity function and the RESTART timer.

RETRY Address: $0E7_H$

Reset value: $080F_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	SRG_PROT_EN	Res		RESTART_TMR			RETRY_COUNTER			RETD_TMR			COOLD_TMR		
r	rw	r		rw			rw			rw			rw		

Field	Bits	Type	Description
COOLD_TMR	2:0	rw	**This bit field sets the cool down period before the next retry attempt.** 000_B 0 s 001_B 1 s 010_B 2 s 011_B 4 s 100_B 8 s 101_B 16 s 110_B 32 s 111_B 64 s
RETD_TMR	5:3	rw	**This bit filed sets the retry OK deglitch time after which the retry counter is reset.** 000_B Disables the reset of the retry counter. 001_B 0.5 s 010_B 1 s 011_B 2 s 100_B 3 s 101_B 4 s 110_B 6 s 111_B 8 s
RETRY_COUNTER	8:6	rw	**This bit field sets the maximum number of allowed retry attempts.** 000_B 0 (latch-off i.e. no retry) 001_B 1 010_B 2 011_B 4 100_B 8 101_B 16 110_B 32 111_B Infinite
RESTART_TMR	11:9	rw	**This bit field sets the wait/idle time after a restart event is triggered.** 000_B 0.58 s 001_B 1.16 s 010_B 2.32 s 011_B 4.64 s 100_B 9.28 s 101_B 18.6 s 110_B 37.1 s 111_B 74.2 s
SRG_PROT_EN	14	rw	**This bit enables or disabled the input surge protection.** 0_B Surge protection is disabled. 1_B Surge protection is enabled.

2.58 TELEMETRY_EN

This command enables or disables each one of the telemetry features.

TELEMETRY_EN

Address: $0E8_H$

Reset value: $7FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ_EIN_EN	READ_VIN_EN	READ_VOUT_EN	READ_IOUT_EN	READ_TEMP_1_EN	READ_TEMP_2_EN	READ_PIN_EN	READ_VIN_PEAK_EN	READ_VOUT_PEAK_EN	READ_IOUT_PEAK_EN	READ_PIN_PEAK_EN	READ_TEMP_1_PEAK_EN	READ_VIN_VALLEY_EN	READ_VOUT_VALLEY_EN	READ_IOUT_VALLEY_EN	READ_TEMP_1_VALLEY_EN
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
READ_TEMP_1_VALLEY_EN	0	rw	**This bit enables or disables the MOSFET temperature valley reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_IOUT_VALLEY_EN	1	rw	**This bit enables or disables the output current valley reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_VOUT_VALLEY_EN	2	rw	**This bit enables or disables the output voltage valley reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_VIN_VALLEY_EN	3	rw	**This bit enables or disables the input voltage valley reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_TEMP_1_PEAK_EN	4	rw	**This bit enables or disables the MOSFET temperature peak reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_PIN_PEAK_EN	5	rw	**This bit enables or disables the input power reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_IOUT_PEAK_EN	6	rw	**This bit enables or disables the output current peak reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_VOUT_PEAK_EN	7	rw	**This bit enables or disables the output voltage peak reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_VIN_PEAK_EN	8	rw	**This bit enables or disables the input voltage peak reading.** 0_B Feature is disabled. 1_B Feature is enabled.

(table continues...)

(continued)

Field	Bits	Type	Description
READ_PIN_EN	9	rw	**This bit enables or disables the input power calculation.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_TEMP_2_EN	10	rw	**This bit enables or disables the controller's on-chip temperature reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_TEMP_1_EN	11	rw	**This bit enables or disables the MOSFET temperature reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_IOUT_EN	12	rw	**This bit enables or disables the output current reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_VOUT_EN	13	rw	**This bit enables or disables the output voltage reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_VIN_EN	14	rw	**This bit enables or disables the input voltage reading.** 0_B Feature is disabled. 1_B Feature is enabled.
READ_EIN_EN	15	rw	**This bit enables or disables the energy calculation.** 0_B Feature is disabled. 1_B Feature is enabled.

2.59 TELEMETRY_AVG

This command configures the number of averaging samples for reporting power, voltage and current telemetry. It is also used to select the analog current reporting (IMON) gain.

TELEMETRY_AVG Address: $0E9_H$

Reset value: 0400_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					**GIMON_SEL**	**P_TELEMETRY_AVG**				**V_TELEMETRY_AVG**			**I_TELEMETRY_AVG**		
r					rw	rw				rw			rw		

Field	Bits	Type	Description
I_TELEMETRY_AVG	2:0	rw	**This bit field sets the current telemetry averaging.** 000_B 1 sample. 001_B 2 samples. 010_B 4 samples. 011_B 8 samples. 100_B 16 samples. 101_B 32 samples. 110_B 64 samples. 111_B 128 samples.
V_TELEMETRY_AVG	5:3	rw	**This bit field sets the voltage telemetry averaging.** 000_B 1 sample. 001_B 2 samples. 010_B 4 samples. 011_B 8 samples. 100_B 16 samples. 101_B 32 samples. 110_B 64 samples. 111_B 128 samples.
P_TELEMETRY_AVG	9:6	rw	**This bit field sets the power telemetry averaging.** 0_H 1 sample. 1_H 2 samples. 2_H 4 samples. 3_H 8 samples. 4_H 16 samples. 5_H 32 samples. 6_H 64 samples. 7_H 128 samples. 8_H 256 samples. 9_H 512 samples. A_H 1024 samples. B_H 2048 samples. C_H 4096 samples. D_H 8192 samples. E_H 16384 samples. F_H 32768 samples.
GIMON_SEL	10	rw	**This bit sets the IMON current gain.** 0_B Output gain 9.1 µA/A. 1_B Output gain 18.2 µA/A.

2.60 WRITE_OTP

This command is used for storing the configuration in the One-Time Programmable (OTP) memory and enabling/disabling the PMBus® WRITE protection feature.

WRITE_OTP Address: $0EA_H$

Reset value: 00_H

7	6	5	4	3	2	1	0
Res				WR_PROTECT	Res		WRITE_OTP
r				rw	r		w

Field	Bits	Type	Description
WRITE_OTP	0	w	**This bit is used for writing the configuration into the OTP section i.e. non-volatile memory.** 0_B No writing to OTP. 1_B Write into OTP.
WR_PROTECT	3	rw	**This bit enables or disables the PMBus® WRITE protection.** 0_B PMBus® WRITE protect is disabled. 1_B PMBus® WRITE protect is enabled.

2.61 STATUS_MEM

This command stores the memory status of the device.

STATUS_MEM Address: $0EB_H$

Reset value: 00_H

7	6	5	4	3	2	1	0
PROG_BLOCK	OTP_FAIL	Res		OTP_USER	Res		
rh	rh	r		rh	r		

Field	Bits	Type	Description
OTP_USER	3	rh	**This bit indicates if the OTP section of the device is programmed or not.** 0_B OTP has not been programmed. 1_B OTP has been programmed.
OTP_FAIL	6	rh	**This bit indicates if the OTP programming or the readout of the OTP has been successful or not.** 0_B OTP programming passed or waiting to be programmed. 1_B OTP programming failed; the device must be discarded.
PROG_BLOCK	7	rh	**This bit indicates if the OTP programming is allowed or if it has been blocked because of input voltage or temperature out of range.** 0_B OTP programming is allowed. 1_B OTP programming is blocked due to input voltage or temperature out of range.

2.62 RESTART

This command is used for triggering a restart event. It results in internal MOSFET turning-off for a pre-configured RESTART time from the RETRY command and then it is automatically turned back on. This is a write only command without a data byte.

RESTART

Address: $0EC_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESTART															
w															

Field	Bits	Type	Description
RESTART	15:0	w	**This command turns-off the internal MOSFET for RETRY:RESTART_TMR, then it is automatically turned back on.**

2.63 READ_PIN_EXT

This command returns the input power of the system as a product of VIN * IOUT in direct format.

READ_PIN_EXT

Address: $0EE_H$

Reset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
READ_PIN_EXT							
rh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ_PIN_EXT															
rh															

Field	Bits	Type	Description
READ_PIN_EXT	23:0	rh	**Input power calculation.**

2.64 READ_VIN_PEAK

This command stores the maximum VIN value in direct format. It is automatically cleared when the data is read.

READ_VIN_PEAK

Address: $0EF_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				READ_VIN_PEAK											
r				rh											

Field	Bits	Type	Description
READ_VIN_PEAK	11:0	rh	**Stores the maximum VIN value.**

2.65 READ_VOUT_PEAK

This command stores the maximum VOUT value in direct format. It is automatically cleared when the data is read.

READ_VOUT_PEAK

Address: $0F0_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				READ_VOUT_PEAK											
r				rh											

Field	Bits	Type	Description
READ_VOUT_PEAK	11:0	rh	**Stores the maximum VOUT value.**

2.66 READ_IOUT_PEAK

This command stores the maximum IOUT value in direct format. It is automatically cleared when the data is read.

READ_IOUT_PEAK

Address: $0F1_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				READ_IOUT_PEAK											
r				rh											

Field	Bits	Type	Description
READ_IOUT_PEAK	11:0	rh	**Stores the maximum IOUT value.**

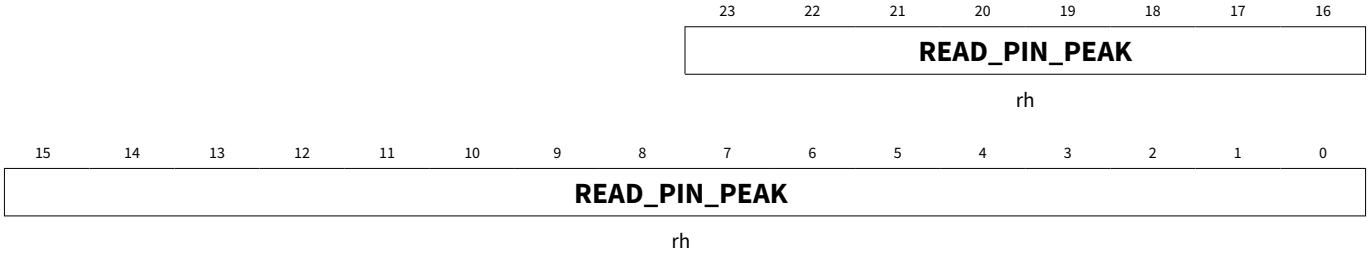
2.67 READ_PIN_PEAK

This command stores the maximum PIN value in direct format. It is automatically cleared when the data is read.

READ_PIN_PEAK

Address: $0F2_H$

Reset value: $00\ 0000_H$



Field	Bits	Type	Description
READ_PIN_PEAK	23:0	rh	**Stores the maximum PIN value.**

2.68 READ_TEMP_1_PEAK

This command stores the internal MOSFET's maximum temperature value in direct format. It is automatically cleared when the data is read.

READ_TEMP_1_PEAK

Address: $0F3_H$

Reset value: 0000_H



Field	Bits	Type	Description
READ_TEMP_1_PEAK	11:0	rh	**Stores the internal MOSFET’s maximum temperature value.**

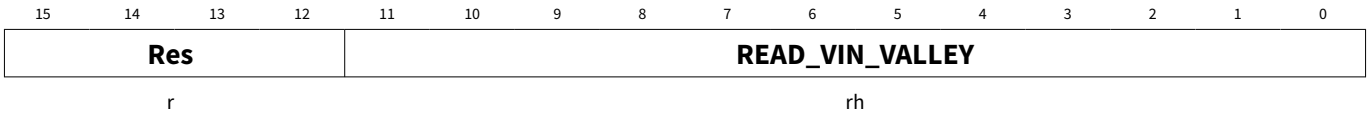
2.69 READ_VIN_VALLEY

This command stores the minimum VIN value in direct format. It is automatically cleared when the data is read.

READ_VIN_VALLEY

Address: $0F4_H$

Reset value: $0FFF_H$



Field	Bits	Type	Description
READ_VIN_VALLEY	11:0	rh	**Stores the minimum VIN value.**

2.70 READ_VOUT_VALLEY

This command stores the minimum VOUT value in direct format. It is automatically cleared when the data is read.

READ_VOUT_VALLEY Address: $0F5_H$

Reset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				READ_VOUT_VALLEY											
r				rh											

Field	Bits	Type	Description
READ_VOUT_VALLEY	11:0	rh	**Stores the minimum VOUT value.**

2.71 READ_IOUT_VALLEY

This command stores the minimum IOUT value in direct format. It is automatically cleared when the data is read.

READ_IOUT_VALLEY Address: $0F6_H$

Reset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				READ_IOUT_VALLEY											
r				rh											

Field	Bits	Type	Description
READ_IOUT_VALLEY	11:0	rh	**Stores the minimum IOUT value.**

2.72 READ_TEMP_1_VALLEY

This command stores the internal MOSFET's minimum temperature value in direct format. It is automatically cleared when the data is read.

READ_TEMP_1_VALLEY Address: $0F7_H$

Reset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				READ_TEMP_1_VALLEY											
r				rh											

Field	Bits	Type	Description
READ_TEMP_1_VALLEY	11:0	rh	**Stores the internal MOSFET's minimum temperature value.**

2.73 STATUS_MODE

This command shows the status of the internal MOSFET's GATE terminal, PWRGD signal and the selected device address.

STATUS_MODE Address: $0F9_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GATE_STATUS		**PWRGD_STATUS**	**Res**			**SELECTED_DEVICE_ADDRESS**				**Res**					
rh		rh	r			rh				r					

Field	Bits	Type	Description
SELECTED_DEVICE_ADDRESS	9:6	rh	**This bit field stores the LSB part of the PMBus® address [3:0].** 0_H 4'b0000 1_H 4'b0001 2_H 4'b0010 3_H 4'b0011 4_H 4'b0100 5_H 4'b0101 6_H 4'b0110 7_H 4'b0111 8_H 4'b1000 9_H 4'b1001 A_H 4'b1010 B_H 4'b1011 C_H 4'b1100 D_H 4'b1101 E_H 4'b1110 F_H Programmed in PMBUS_CFG:PMBUS_DEVICE_ADDR command bit.
PWRGD_STATUS	13	rh	**This bit shows the PWRGD pin status.** 0_B PWRGD pin is deasserted. 1_B PWRGD pin is asserted.
GATE_STATUS	15:14	rh	**This bit field shows the status of the internal MOSFET's GATE terminal.** 00_B GATE pin is low. 01_B GATE pin is high. 10_B GATE pin is in regulation. 11_B NA

2.74 CONFIG_ID

This command provides the user an option to store a unique identification number in order to distinguish among devices with different configuration in the system.

CONFIG_ID

Address: $0FA_H$

Reset value: 00_H



Field	Bits	Type	Description
CONFIG_ID	7:0	rw	**8-bit code for device identification.**

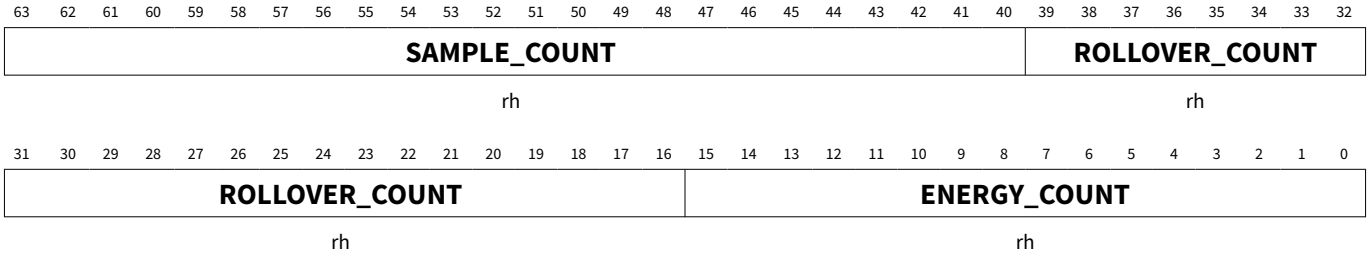
2.75 READ_EIN_EXT

This command returns the input energy reading in direct format.

READ_EIN_EXT

Address: $0FB_H$

Reset value: 0000 0000 0000 0000$_H$



Field	Bits	Type	Description
ENERGY_COUNT	15:0	rh	**Output of an accumulator that continuously sums samples of the instantaneous input power.**
ROLLOVER_COUNT	39:16	rh	**Unsigned integer that will periodically roll over from its maximum positive value to zero.**
SAMPLE_COUNT	63:40	rh	**Unsigned integer that counts the number of samples of the instantaneous input power.**

3 Revision history

Document version	Date of release	Description of changes
1.0	2026-06-02	First release.

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2026-06-02

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2026 Infineon Technologies AG

All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-ajf1775655043928

Important notice

Products which may also include samples and may be comprised of hardware or software or both ("Product(s)") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.

For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability. Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.

If this document is marked as 'Preliminary', 'Target', 'Draft' or 'Proposal', Infineon reserves the right to change all information given in this document at any time without notice. Subject to the development and release of a Product for series supply by Infineon, the technical specifications of the Product are set forth in the relevant datasheet provided by Infineon without such marking.

The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.

Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Products or any consequences of the use thereof can reasonably be expected to result in personal injury.

However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer. Infineon expressly reserves the right to use its content for commercial text and data mining (TDM) according to applicable laws, e.g. Section 44b of the German Copyright Act (UrhG). If the Product includes security features:

Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.

If this document includes or references software:

The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved. Therefore, you may use the software only as provided in the software license agreement accompanying the software.

If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited.

For further information on the Product, technology, delivery terms and conditions, and prices, please contact your nearest Infineon office or visit www.infineon.com.