EVAL_6EDL7141_1KW_36V for battery-powered applications using 6EDL7141 smart gate driver

About this document

Scope and purpose

This document describes the functionalities of the EVAL_6EDL7141_1KW_36V motor drive board for battery-powered brushless DC (BLDC) motor drives; used in applications such as gardening tools up to 1 kW. The evaluation board can support motors with Hall sensors for rotor position sensing, or without Hall sensors.

This solution combines a high-performance three-phase smart driver IC and the motor inverter power stage with two power MOSFETs of BSC012N06NS in parallel for each phase. You can use your own MCU to design the controlling unit by using a daughterboard to connect to the evaluation board using a MADK connector.

Intended audience

This document is intended for design engineers, applications engineers, and students who address the market for gardening tools and other battery-powered motor drive applications, aimed to provide a high-performance system solution as well as to reduce system costs.

Infineon components featured

- OptiMOS™ 5 BSC012N06NS power MOSFET 60 V/1.2 mΩ 5 x 6 package
- MOTIX™ 6EDL7141 smart three-phase half-bridge gate driver

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as under sizing the motor, supplying an incorrect or inadequate DC supply, or excessive ambient temperatures may result in system malfunction.*

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1 Introduction

EVAL_6EDL7141_1KW_36V is a standalone board with MOTIX™ 6EDL7141 smart gate driver from Infineon. MOTIX™ 6EDL7141 integrates buck and linear regulators, charge pumps for both high- and low-side MOSFETs, and current sense amplifiers for three phases. You have the flexibility to select the MCU that is suitable for your system requirements.

1.1 EVAL_6EDL7141_1KW_36V motor drive board

EVAL_6EDL7141_1KW_36V motor driver evaluation board is optimized for 36 V battery-powered application with maximum 1 kW power rating. The current design considers the electrical driving capabilities for BLDC motors without requiring sensors to determine rotor position and speed. This evaluation board (with alternative firmware) also supports operation with Hall sensors. The board is populated with a fuse for inverter overcurrent protection (OCP) and has reverse polarity protection components. You can use your own MCU and motor control algorithm easily. On this board, you can evaluate the MOTIX™ 6EDL7141-based motor drive system using the control capabilities of MCU by means of the implemented control algorithm. The leg overcurrent sensing using MOTIX™ 6EDL7141 gate driver can be configured by the MCU through the SPI interface.

Figure 1 EVAL_6EDL7141_1KW_36V Evaluation Board

Figure 2 shows the key system elements of the EVAL_6EDL7141_1KW_36V board.

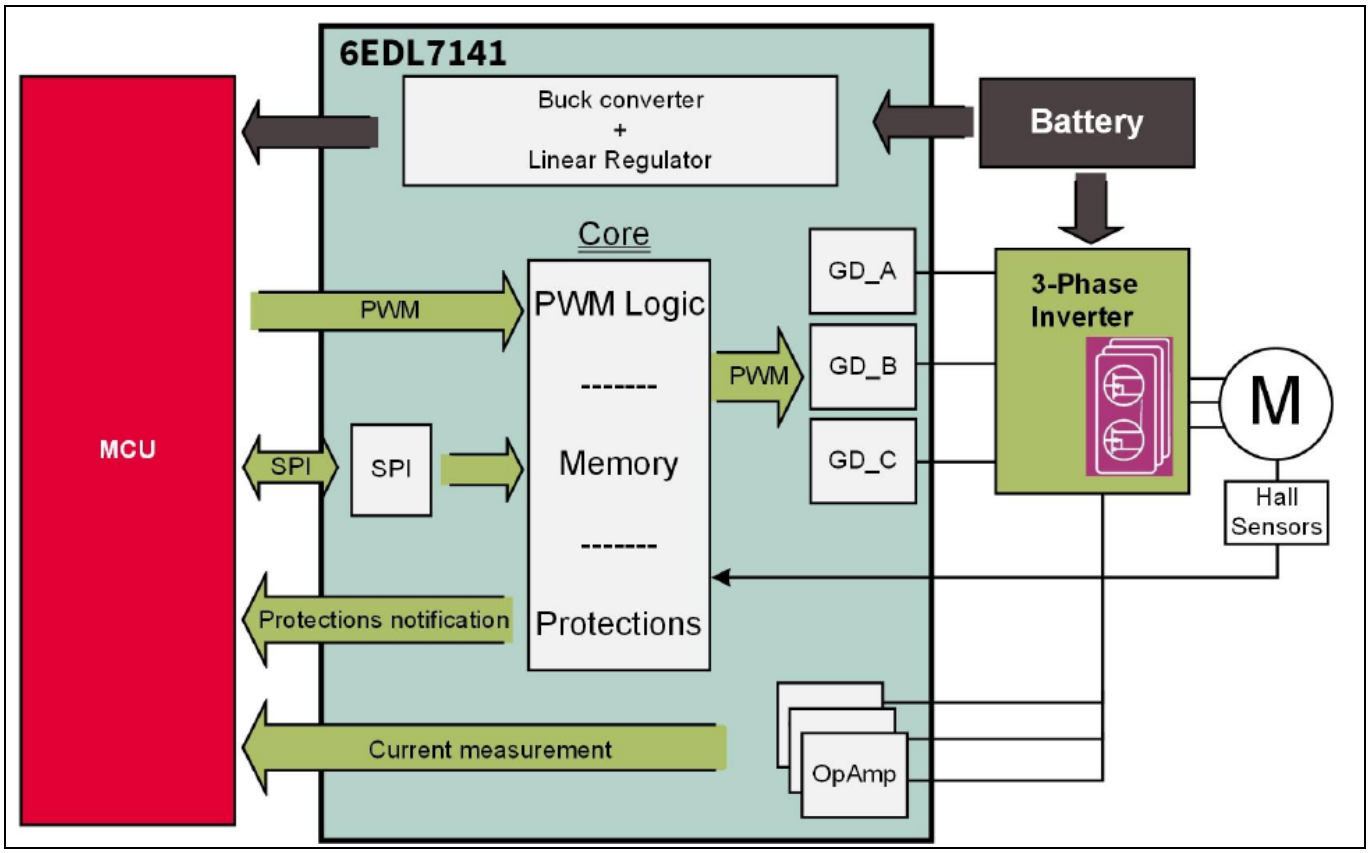

Figure 2 Block diagram

1.2 Board parameters

Table 2 shows the evaluation board parameters.

Table 2 Board parameters

Parameter	Symbol	Conditions	Value	Unit
Input voltage	V_{in}	DC voltage input	36 (typical)	V
Buck output 12 V	+12 V	Maximum 1 A output current	12±5%	V
LDO output 3.3 V	+3.3 V	Maximum 300 mA output current	3.3±5%	V
Phase current sensing resistor	R	Power rating 8 W, 1%, size 3920 inches, three shunts (compatible with single shunt)	1	mΩ
Maximum output power	P_{out}	With supplied heatsink as tested	1000	W
PCB characteristics				
Material	–	1.6 mm thickness, 2 oz. copper each layer, six layers	FR 4	
Dimensions	–	Length x width	4.5 x 3.7	inch

1.3 Specifications

Input and output at normal operation

- DC input voltage 12 V to 40 V, nominal 36 V
- Maximum input current 40 A
- Maximum continuous output power 1 kW

Protection features

- Input fuse
- Overvoltage protection
- Thermal shutdown

Maximum component temperature

In an ambient temperature of 30°C, the maximum allowed component temperatures are as follows:

- Resistors less than 100°C
- Ceramic capacitors, film capacitors, and electrolytic capacitors less than 100°C
- MOSFET transistors and diodes less than 100°C
- ICs less than 100°C

Note: *To operate this board correctly, configure the firmware correctly for the specific motor being driven. This requires motor parameters such as phase-winding inductance and resistance to be integrated in the software design.*

Attention: ***Test the board by qualified engineers and technicians.***

2 Board connections and controls

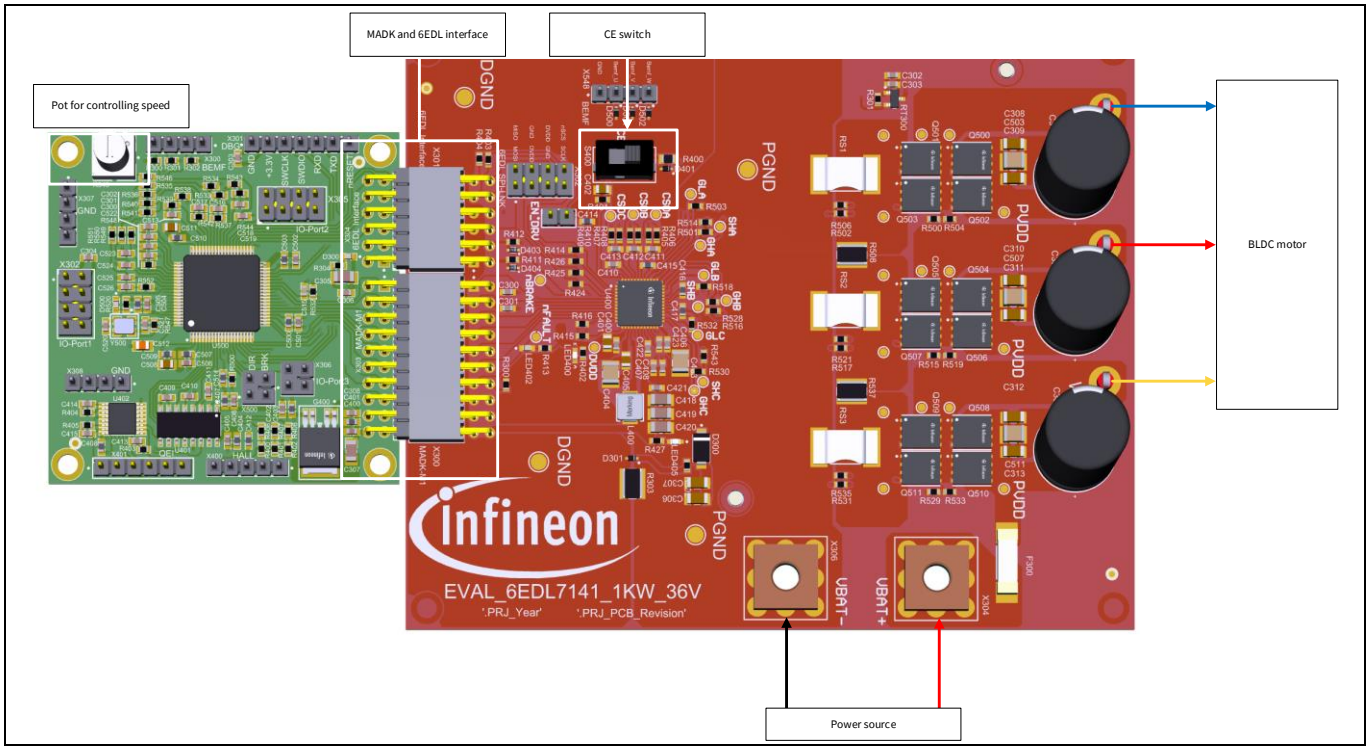

Figure 3 EVAL_6EDL7141_1KW_36V external connections and controls

In this design, the control card (the green board on the left) is for only internal use. You can make your own control board with the suitable microcontroller based on your system design requirements. EVAL_6EDL7141_1KW_36V board reserves standard MADK-M1 connector and 6EDL interface to plug-in the control board. To achieve the full capability of the evaluation board, use a power source with maximum current up to 50 A RMS and a BLDC/PMSM motor with maximum power up to 1.5 kW.

3 Hardware

EVAL_6EDL7141_1KW_36V is a standalone board which integrates the three-phase inverter power stage and the smart three-phase motor control MOTIX™ 6EDL7141 gate driver IC. This enables the development of high-performance battery-powered products using BLDC or PMSM motors. The power stage consists of two OptiMOS™ BSC012N06NS power MOSFETs in parallel for each phase. OptiMOS™ BSC012N06NS power MOSFETs is available in SuperSO8 package with V_{DS} of 60 V and $R_{DS(on),max}$ of 1.2 mΩ. EVAL_6EDL7141_1KW_36V is capable of carrying out 1 kW power output at 36 V.

EVAL_6EDL7141_1KW_36V is only a standalone board without any MCU, you can choose your own MCU in the project to make a suitable system structure to meet your design requirements. Select your preferred controller to adopt in circuitry, it will shorten the firmware developing time as the designers do not need to spend time on a new platform and transfer their motor control algorithms.

EVAL_6EDL7141_1KW_36V has several generic connectors which are convenient to interface with different modules. SPI connectors are compatible with the 6EDL_SPI_LINK board kit. By connecting 6EDL_SPI_LINK kit to this evaluation board, you can set the gate driver's register value directly from the GUI of 6EDL7141 Configurator from MOTIX™ BPA Motor Control Workbench.

If you design your own motor control board to connect to the EVAL_6EDL7141_1KW_36V, this evaluation board also provides a 6EDL Interface that contains the SPI interface signals and some key signals from the 6EDL7141 and the MADK-M1 connector that include the switching signals and the phase current sensing signals.

For the phase current sensing, EVAL_6EDL7141_1KW_36V adopts three 1 mΩ current sense resistors with dimension of 3920 inches which has a power rating of 8 W. The evaluation board reserves the PCB position for changing the existing three shunts to a single shunt as well.

3.1 Three-phase smart gate driver MOTIX™ 6EDL7141

Optimized gate drive pulses to the high- and low-side MOSFETs in each phase are provided by the MOTIX™ 6EDL7141 smart gate driver. Logic-level switching PWM pulses from the MCU are supplied to the EVAL_6EDL7141_1KW_36V via the MADK-M1 connector. The high- and low-side gate drivers allow operation over the full duty cycle range up to 100 percent. The gate drive voltages can be set to different levels, including 7 V, 10 V, 12 V, and 15 V. The benefit of the charge pumps is that voltage levels can be maintained even if the battery voltage drops to a lower level, allowing standard gate-level MOSFET's use.

Control of the drain-source rise and fall times is the most important parameter for optimizing drive systems. It affects critical factors such as switching losses, dead time optimization, and drain voltage ringing that can lead to possible MOSFET avalanching. Correct configuration of the gate drive also helps to minimize EMI emissions.

MOTIX™ 6EDL7141 gate driver can control the slew rate of the driving signal to control the rise and fall slew rates of the drain-to-source voltage by adjusting the gate drive sink and source currents of different time segments during the switch-on and switch-off processes. This permits the designer to eliminate diode resistor networks commonly used in gate drive circuits. In most cases, gate resistors can be removed altogether. Therefore, reducing the total component count and at the same time simplifying and allowing further optimization of the circuit layout.

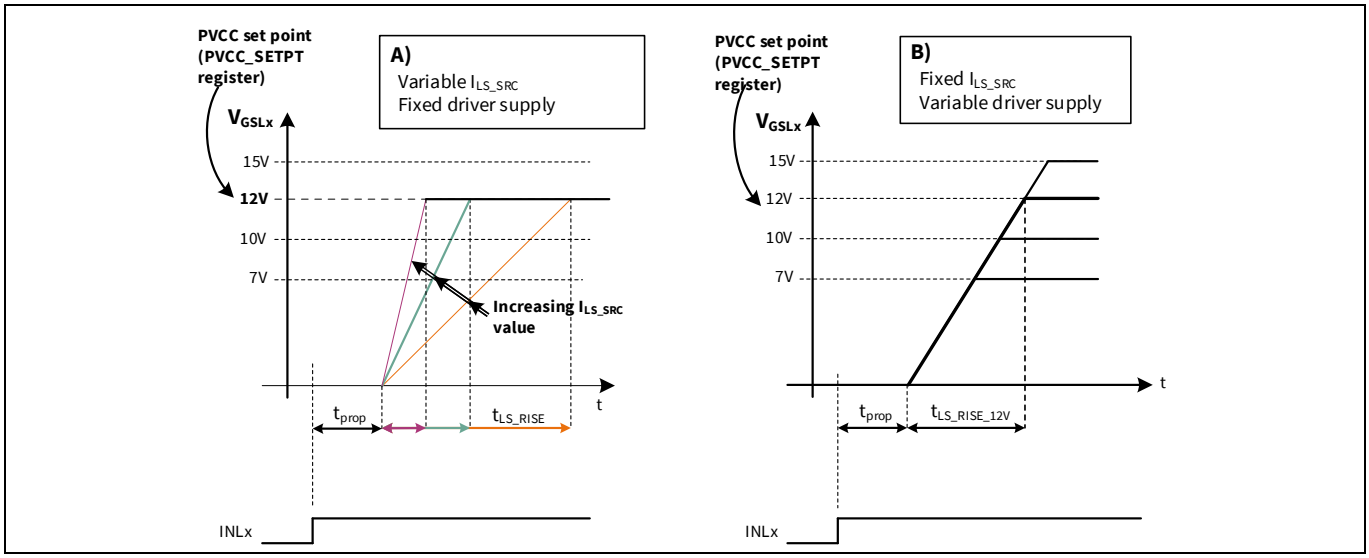

Figure 4 **MOTIX™ 6EDL7141 gate driver slew rate configurability**

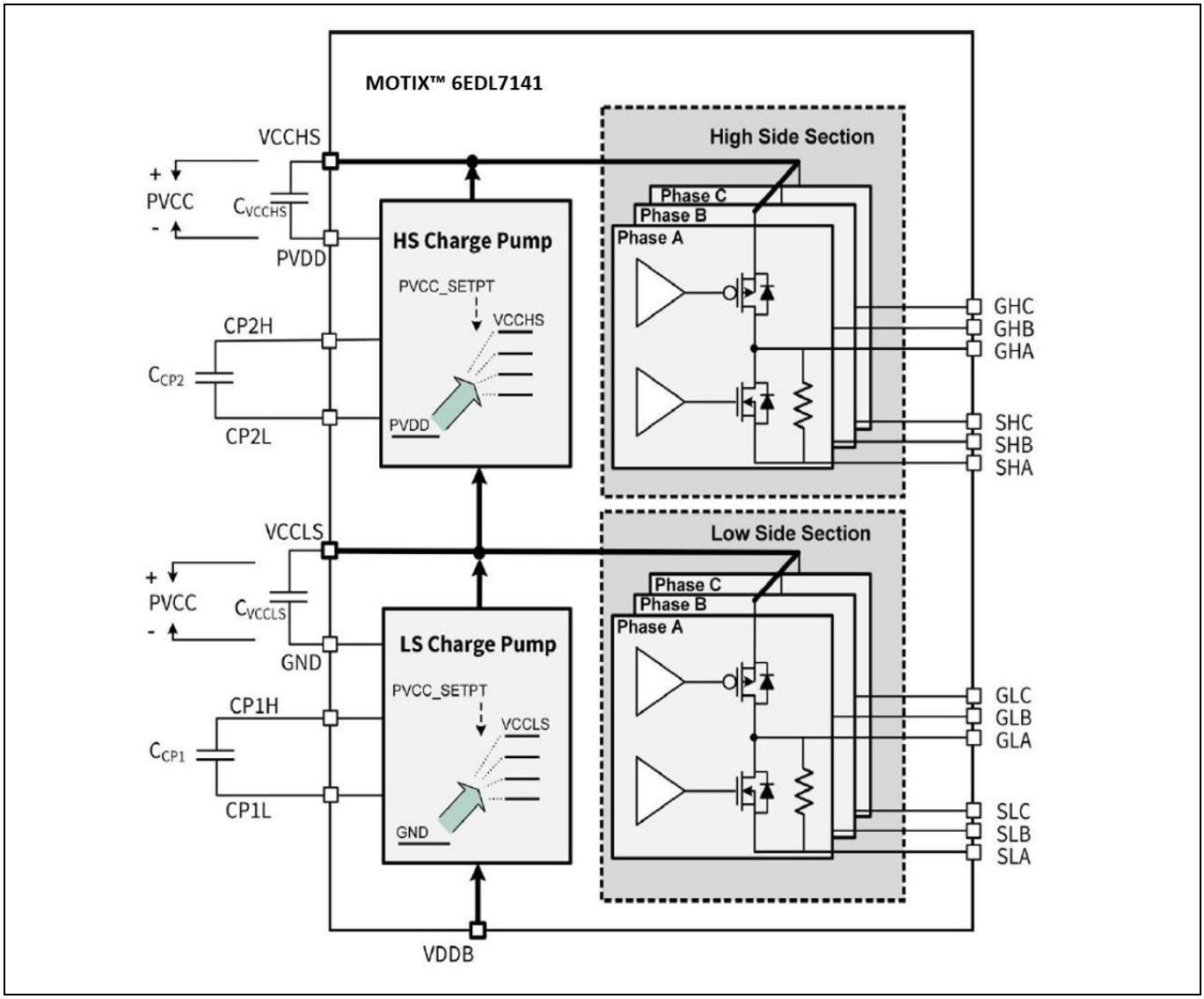

Figure 5 **Gate driver architecture of MOTIX™ 6EDL7141 gate driver**

3.2 Configuration of the buck and linear regulators

The VDDB output can be used to supply external components as long as the current limits of the buck converter, charge pumps, and linear regulator are not exceeded. The voltage is set to 6.5 V if PVCC is 7 V, 7 V if PVCC is 10 V, and 8 V if PVCC is 12 V or 15 V. Intelligent OCPs are also implemented for both buck converter and linear regulator to prevent any damage to the device if the VDDB output becomes overloaded. Additional overtemperature protections (OTS, OTW) are integrated to ensure that the device operates within the correct thermal limits.
Two different switching frequencies, 500 kHz (default value) or 1 MHz, can be configured by the external MCU through the 6EDL SPI connector or SPI LINK connector. The buck inductor L400 value is 22 µH for 500 kHz switching and 10 µH for 1 MHz. The values for the buck output capacitors C418, C419, and C420 are 22 µF with an additional 0.1 µF ceramic capacitor, C421 added to reduce high-frequency (HF) noise. A detailed figure of both the synchronous buck converter and linear voltage regulator circuits is shown in the following figure.

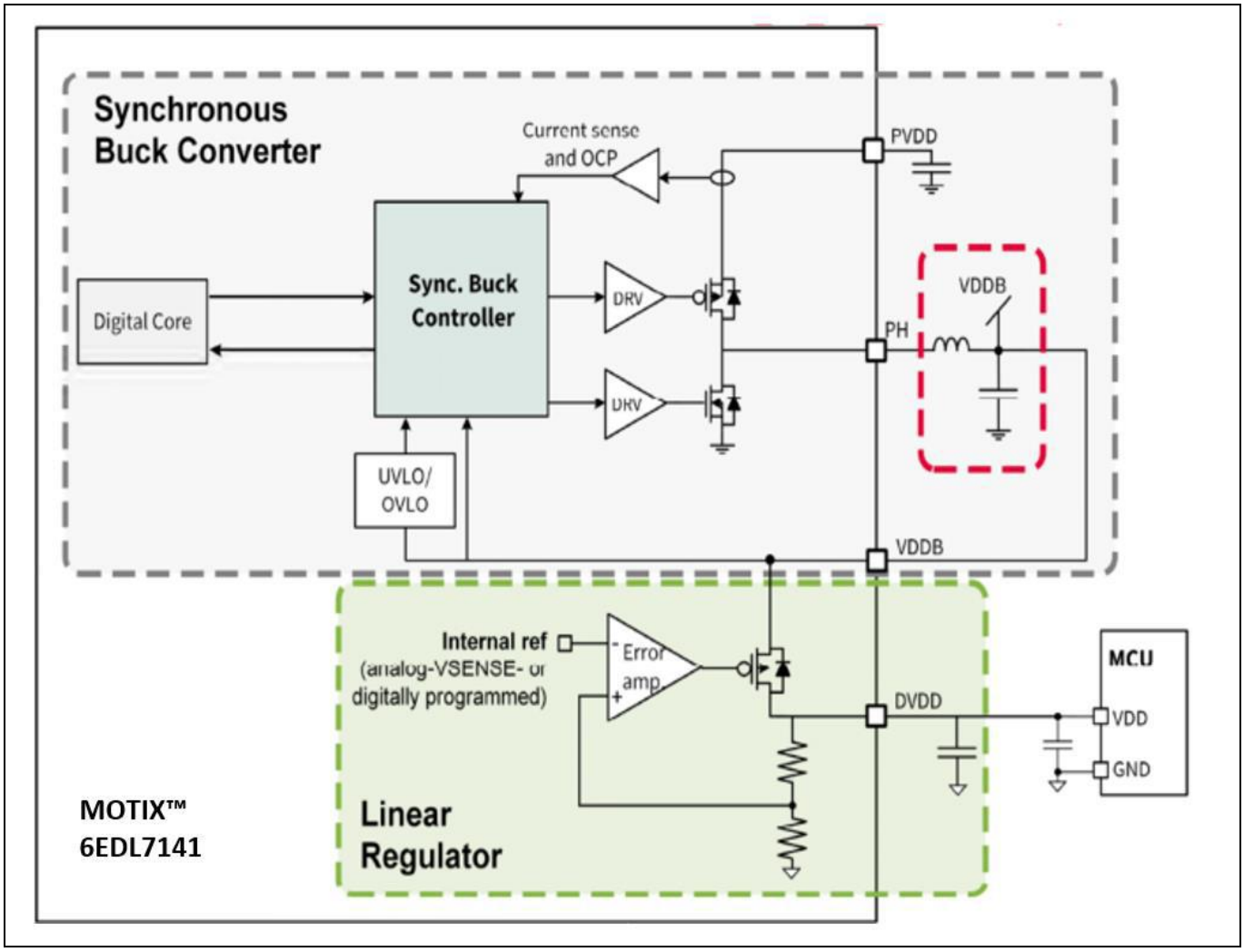

Figure 6 Integrated buck and LDO regulators – block diagram of the MOTIX™ 6EDL7141 gate driver

The following protections are implemented to ensure correct operation of the buck converter:

- Output undervoltage lockout (UVLO)
- Output overvoltage lockout (OVLO)
- OCP, cycle by cycle

In a situation in which the current exceeds the OCP level, the buck converter controller terminates the high-side gate driver pulse until the start of the next PWM period. The low-side operates accordingly after insertion of the dead-time. Once the OCP event takes place, a counter increments each consecutive period that the peak current is reached. After 16 switching cycles, the buck OCP fault is triggered and the nFAULT pin is set low to signal the MCU. The buck converter will continue operation in current limiting mode to ensure that the MCU remains powered. If the OCP is not triggered for three consecutive PWM periods, the counter resets.

The integrated linear regulator output DVDD can be set to either 3.3 V or 5 V by means of an external resistor R415, which is set to 3.01 kΩ on this evaluation board to set DVDD to 3.3 V. The linear regulator can also be used to provide an offset to the CS amplifiers to allow negative current measurements.

DVDD OCP can be configured between four different levels: 50 mA, 150 mA, 300 mA, or 450 mA, with 450 mA being the default value. If the OCP level is reached a fault is reported through the nFAULT pin. The DVDD OCP works in two different stages:

1. Pre-warning mode at 66 percent of selected OCP level:
   The nFAULT pin is pulled down to signal the controller that an OCP warning has occurred. If the current level reduces before reaching the 100 percent level, the operation will continue normally, releasing the nFAULT pin. The pre-warning allows extra time for the MCU to decide how to react to the possible OCP event.
2. Current limiting mode at 100 percent of selected OCP level:
   If current increases beyond the configured OCP level, the DVDD regulator limits its output current. This causes the DVDD voltage to drop, eventually resulting in a DVDD UVLO fault if the UVLO threshold is crossed. This protects DVDD against a short-circuit condition. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device should be operated only under the recommended operating conditions as specified in the datasheet [1].

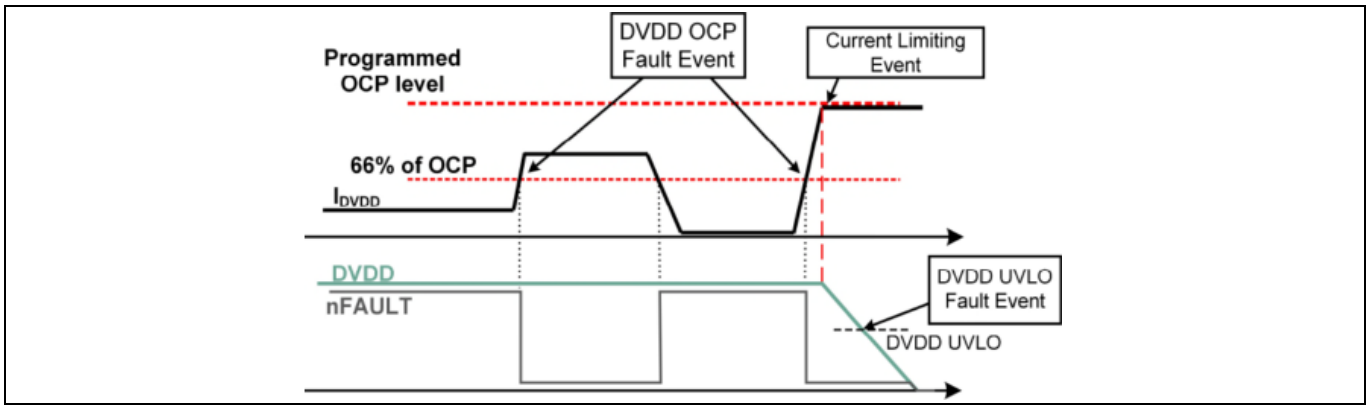

Figure 7 DVDD OCP behavior including pre-warning and current-limiting modes

3.3 Configuration of the charge pumps

The high- and low-side gate driver charge pumps are based on switched capacitor circuits that operate at a determined switching frequency. Selection from one of four frequencies, 781.3 kHz, 390.6 kHz, 195.3 kHz, or 1.56 MHz, allows flexibility for EMC optimization, with 781.3 kHz being the default setting. Another feature in reducing the EMI impact of the charge pump is the spread spectrum feature, which can also be enabled and disabled by setting the registers in the driver IC. This function is enabled by default to provide a frequency variation in the charge pump clock signal to distribute emissions over a wider frequency range, thereby reducing peaks.

The charge pump flying capacitors C422 and C423 are set to 0.22 µF and the tank capacitors C406 is set to 2.2 µF and C407, C408 is set to 2.2 µF and 0.1 µF. The MOTIX™ 6EDL7141 gate driver provides pre-charging of the charge pump output capacitors (C406, C407, and C408) to a voltage just below the buck converter output voltage (VDDB) before the EN_DRV pin is activated. In this way, the charge pump start-up time and therefore, the system start-up time are reduced. In this case, when EN_DRV is activated by the MCU to enable the gate driver stage, the charge pumps need only ramp up the voltage from the existing pre-charge voltage to the selected target value. Pre-charge is disabled by default and can be enabled via setting the relative register.

The start-up time for the charge pumps, defined as the time that the gate drive supply voltages require to reach the target programmed voltage, depends on several factors:

- **Target voltage:** The higher the target voltage, the longer the start-up time for the gate drivers.
- **Charge pump clock frequency:** Higher clock frequency results in faster start-up time.
- **Charge pump tank capacitor values:** A smaller value results in a faster ramp-up time but higher ripple.
- **Charge pump flying capacitors:** Smaller capacitors lead to a slower start-up time.

3.4 Configuration of the current sense amplifiers

MOTIX™ 6EDL7141 gate driver integrates three CS amplifiers that can be used to measure the current in the inverter via shunt resistors. Single, double, or triple shunt measurements are supported, as shown in Figure 8. Each CS amplifier can be enabled individually. Gain and offset are generated internally and are programmable. In this EVAL board design, it selects the triple solution as default, but it supports a single shunt as well.

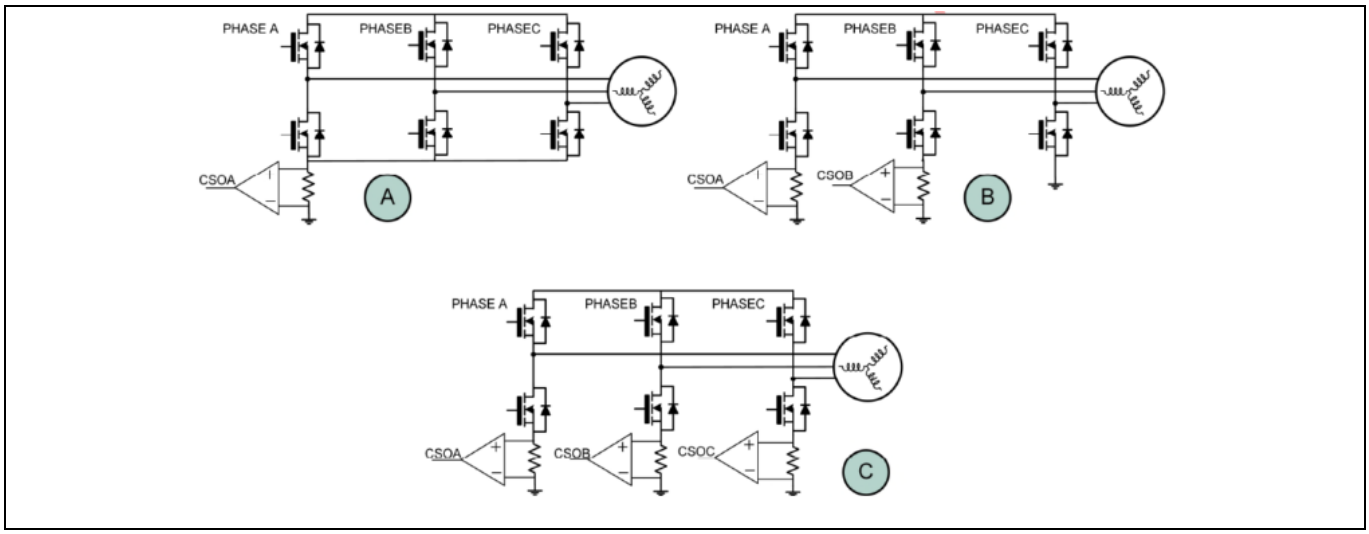

Figure 8 Single (A), dual (B), and triple (C) shunt CS configurations

The CS amplifier block contains the following sub-blocks:

- **CS amplifier:** Connected to an external shunt resistor or internally to an SHx pin for $R_{DS(on)}$ sensing. This module amplifies the shunt voltage or $V_{DS(on)}$ voltage to a level suitable for an MCU ADC input. It includes leading-edge blanking of the signal synchronized to the gate drive, which is active during periods to eliminate noise.
- **Output buffer:** This allows adding a variable offset voltage to the sense amplifier output. The offset amount can be set to one of four different values, either by programming the internally generated level or by applying an external voltage at the V_{REF} input pin. With this implementation, negative shunt currents can also be measured.
- **Positive overcurrent comparator:** Used for detecting the overcurrent conditions on motor windings for positive shunt voltage. This comparator causes the gate drive pulse to be terminated, limiting the motor current.
- **Negative overcurrent comparator:** Used for detecting the overcurrent condition on motor windings for negative shunt currents.
- **OCP DAC:** Used for programming the overcurrent comparator thresholds. One sets the positive level and a second sets the negative level, and these are shared among the different OCP comparators.

Current sense amplifiers will automatically “Auto-Zero”. This happens during operation and ensures the best accuracy of measurements during the lifetime of the device. Additionally, the 6EDL7141 gate driver includes a current sense amplifier user calibration mode that can be used to calculate residual offset when shunt current is known to be zero, for example, when there is no PWM yet propagated to the MOSFETs. A microcontroller firmware can remove this initial residual value from future measurements to improve accuracy.

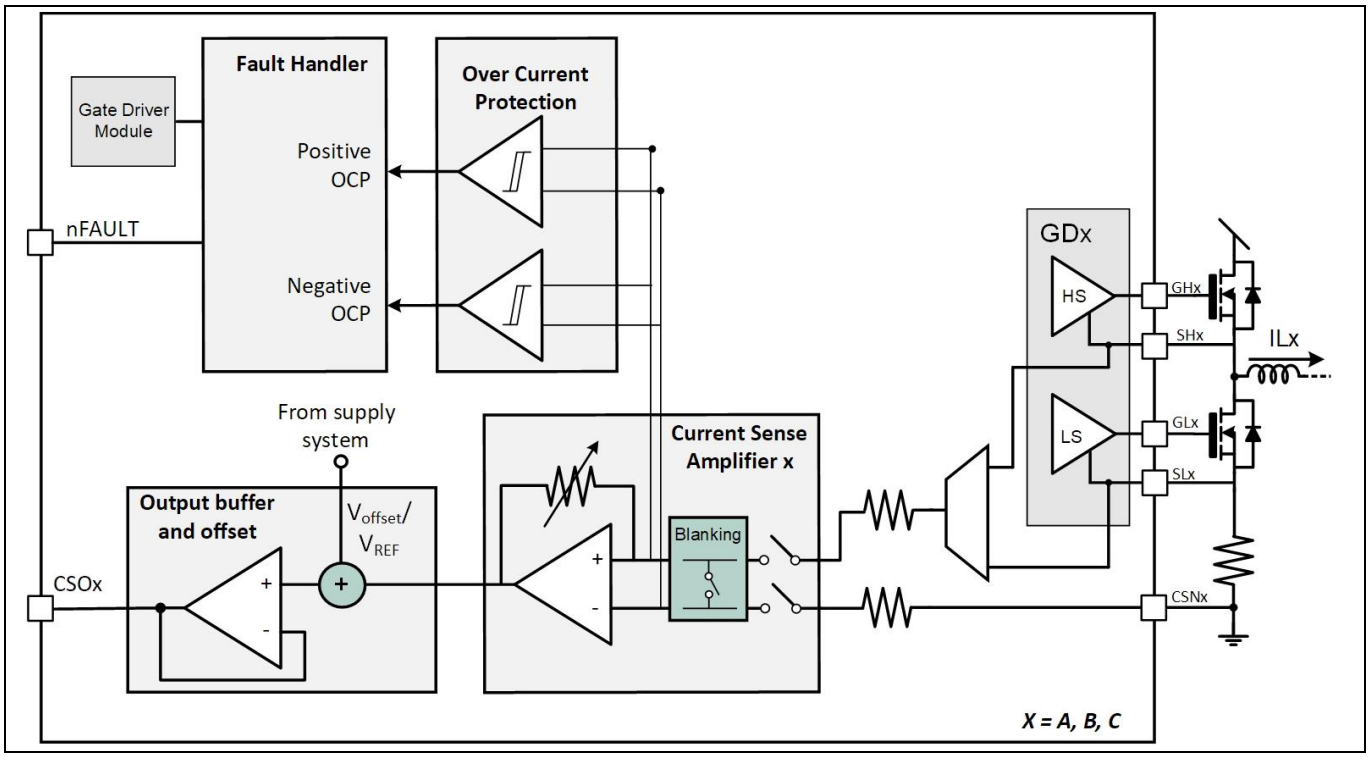

Figure 9 CS amplifier block diagram

The CS amplifiers in MOTIX™ 6EDL7141 gate driver can be configured for $R_{DS(on)}$ sensing to avoid the use of shunt resistors; however, this function is not used in the EVAL_6EDL7141_1KW_36V board, which uses three 1 mΩ shunt resistor.

The CS amplifiers have a default voltage gain of 4. This can be changed by the microcontroller to any of the following values: 8, 12, 14, 20, 24, 32, or 64. Alternatively, select the gain by connecting an external resistor from pin CS_GAIN to ground. To enable analog programming of the CS amplifier via an external resistor, you must ensure that the bitfield CS_GAIN_ANA is set accordingly. The datasheet of MOTIX™ 6EDL7141 gate driver provides the resistor values and register settings for gain selection in both analog and digital modes.

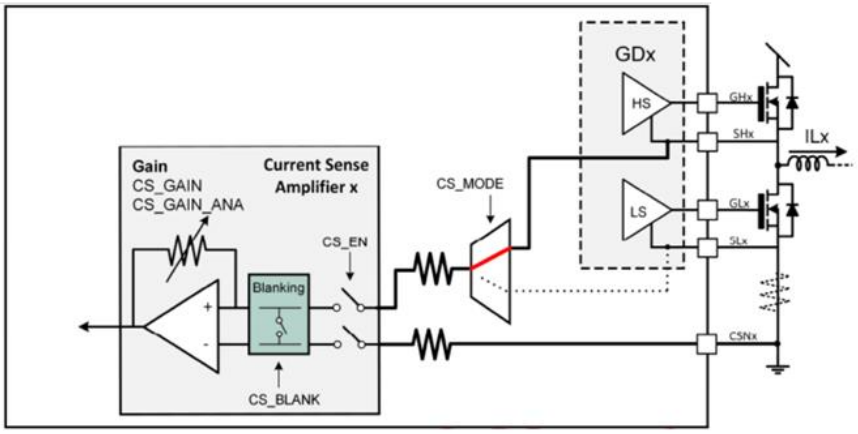

Figure 10 A low-side $R_{DS(on)}$ CS configuration (not used here)

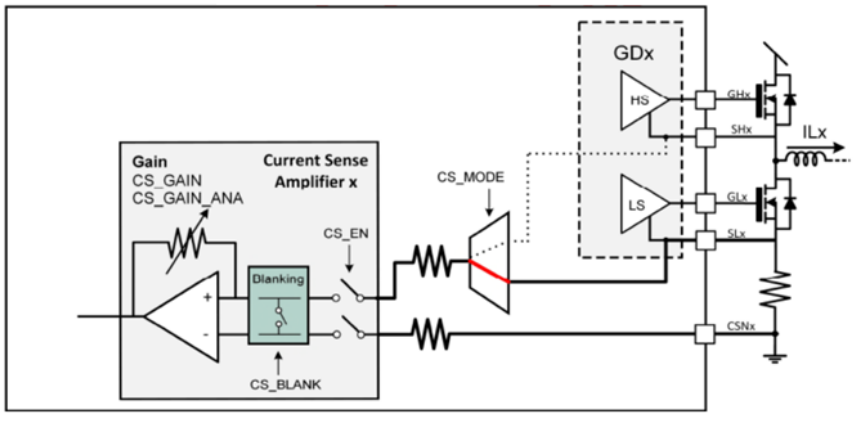

Figure 11 External shunt CS configuration

In many motor drive inverters such as this reference board, the current is sensed via shunt resistors. In this case, the voltage across the shunt needs to be amplified only when the low-side MOSFET is switched on. In other cases, it might be useful to monitor the signal continuously. MOTIX™ 6EDL7141 gate driver supports four different modes of operation of the CS amplifiers regarding when the output pin CSOx is connected to the amplifier stage.

These four modes are as follows:

- **Always off:** CS amplifier output disabled. This is achieved by disabling the amplifier in CSAMP_CFG via bitfield CS_EN register.
- **GL on (default mode):** In this mode, the CSOx pin is connected to the amplifier only when the corresponding GLx signal is active. In single shunt mode, CSOx is connected according to the OR'ing of all two or three GLx signals. If two or three amplifiers are enabled, then the signals for enabling CSOx come

from the corresponding GLx signal. This mode is mandatory if $R_{DS(on)}$ sensing is selected to avoid overvoltage damage to the internal circuitry.

- **GH off:** Similarly to GL on, this mode exposes the output to the GL on period but extends the sensing period to the dead-times, both rising and falling times.
- **Always on:** This mode connects the activated amplifier CSOx signals continuously to the amplifier independently of PWM signals.

As both phase node voltage SHx and SLx pins (CSNy) are subject to ringing due to the switching activity, the blanking module disconnects the inputs for a configurable time (CS_BLANK). The default blanking time is zero, and values between 50 ns and 8 µs can be set in CSAMP_CFG register via the CS_BLANK bitfield. MOTIX™ 6EDL7141 gate driver internal linear voltage regulator (DVDD) can be used for offset generation for CS amplifiers. The default value is 1/2 DVDD, and values of: 5/12, 1/3, and 1/4 DVDD are also available.

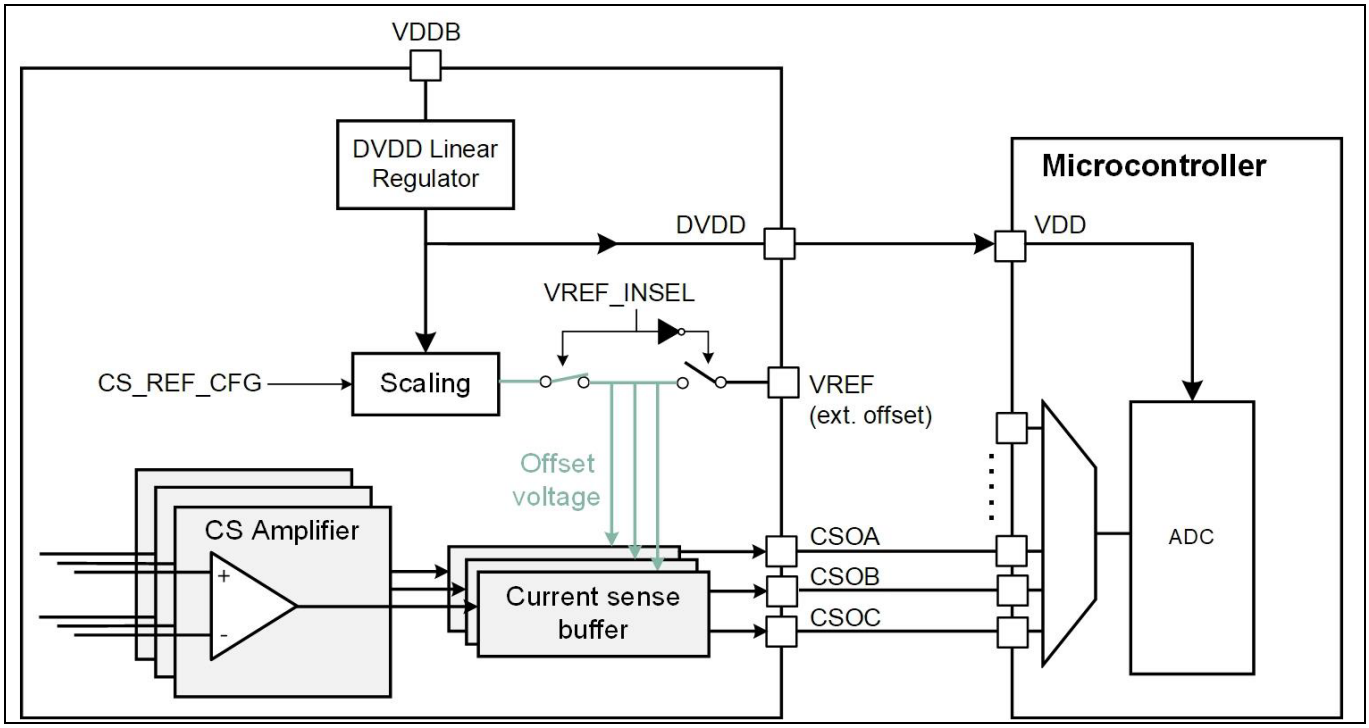

Figure 12 CS amplifier offset generation block diagram

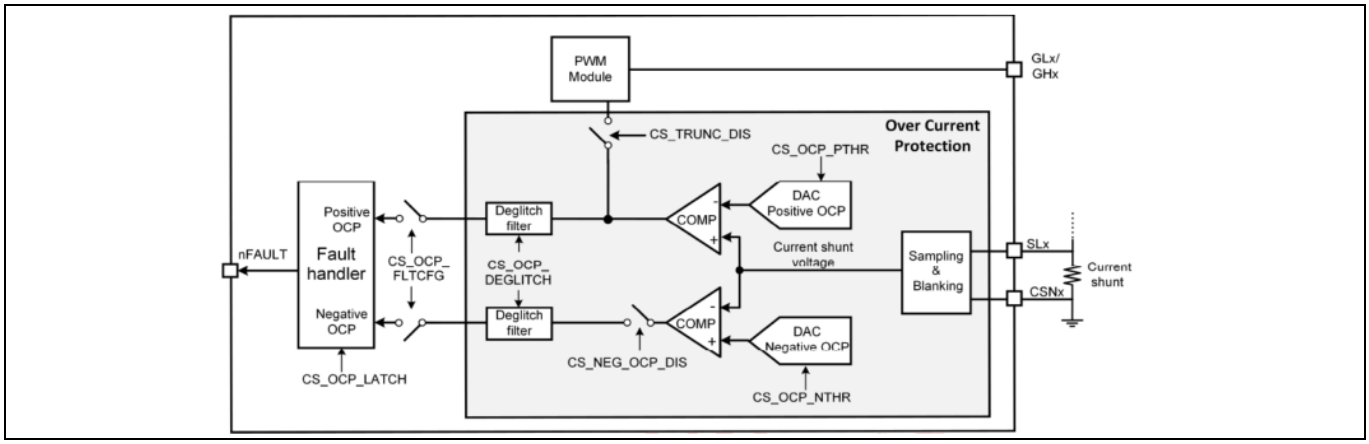

Figure 13 CS amplifier architecture

The reaction to an OCP event is programmable via SPI. Use the following scenarios for different applications:

- Apply PWM truncation immediately after OCP event and report on the nFAULT pin after OCP event-deglitching is disabled if truncation is enabled.
- Disable reporting but keep truncation of PWM.
- Trigger a configurable brake action upon OCP event. If truncation is not desired, a brake event can be configured using one of the available braking modes.
- Disable OCP protection, both nFAULT reporting and truncation of PWM. In such cases, OCP is ignored.

In a latch configuration, the nFAULT pin is held low until the fault is cleared via an SPI command or after a power cycle. If the OCP fault is configured as non-latched, the nFAULT pin remains low while the fault is being detected but will pull-up again when the OCP condition is no longer present. Configuration allows you to set a target number of consecutive events (PWM cycles) required to activate the nFAULT fault signaling.

If a positive OCP event occurs, the high-side PWM is truncated. The result is that the high-side MOSFETs are all switched off and the current flowing in the motor windings therefore, recirculates through the low-side MOSFET body diodes.

3.5 Three-phase power inverter

The power stage consists of two BSC012N06NS MOSFETs in parallel in each phase. OptiMOS™ BSC012N06NS power MOSFETs is available in SuperSO8 package with V_{DS} of 60 V and $R_{DS(on),max}$ of 1.2 mΩ.
EVAL_6EDL7141_1KW_36V is capable of carrying out 1 kW continuous output-rated power at 36 V input.

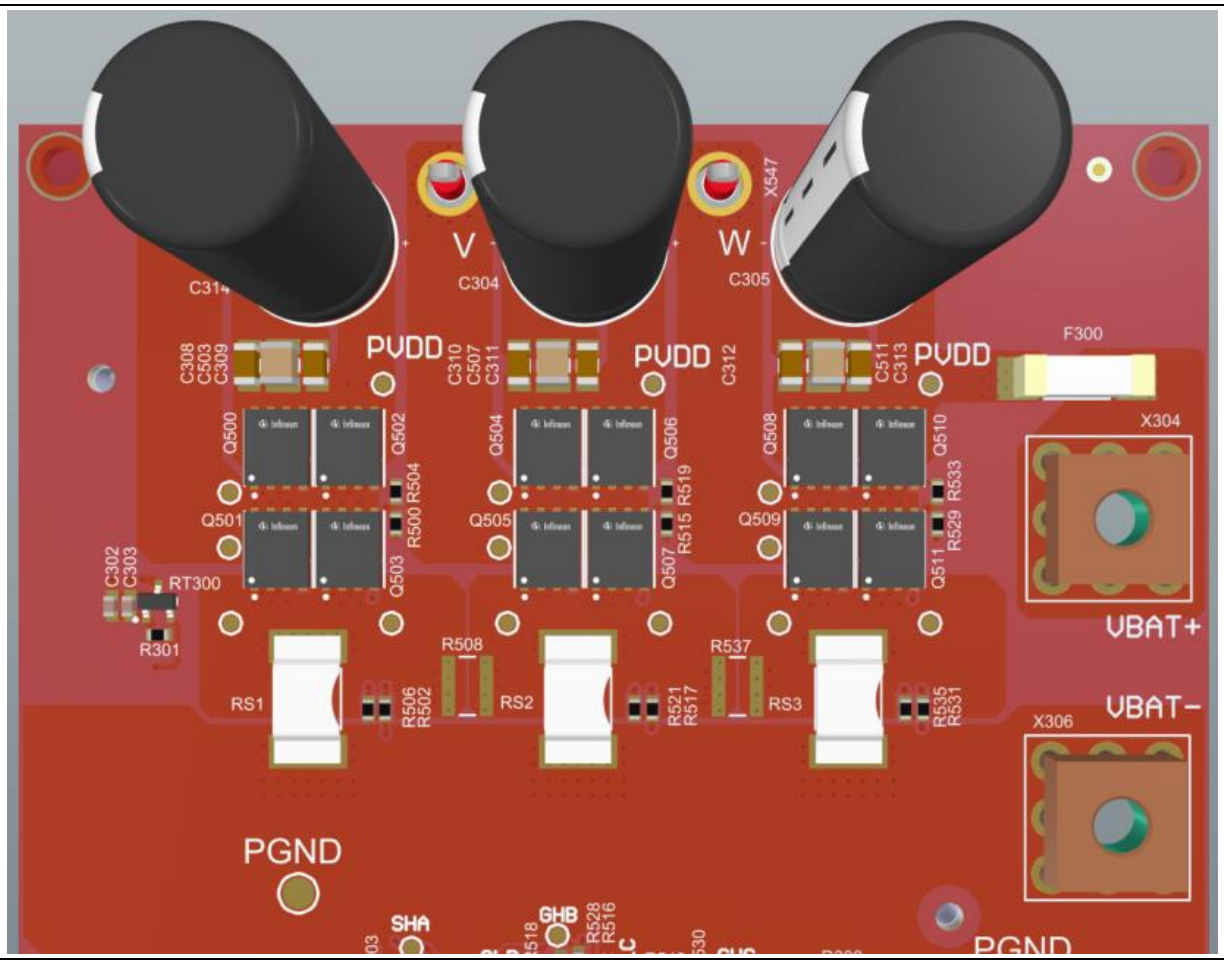

Figure 14 Three-phase power inverter

4 System design

4.1 Schematics

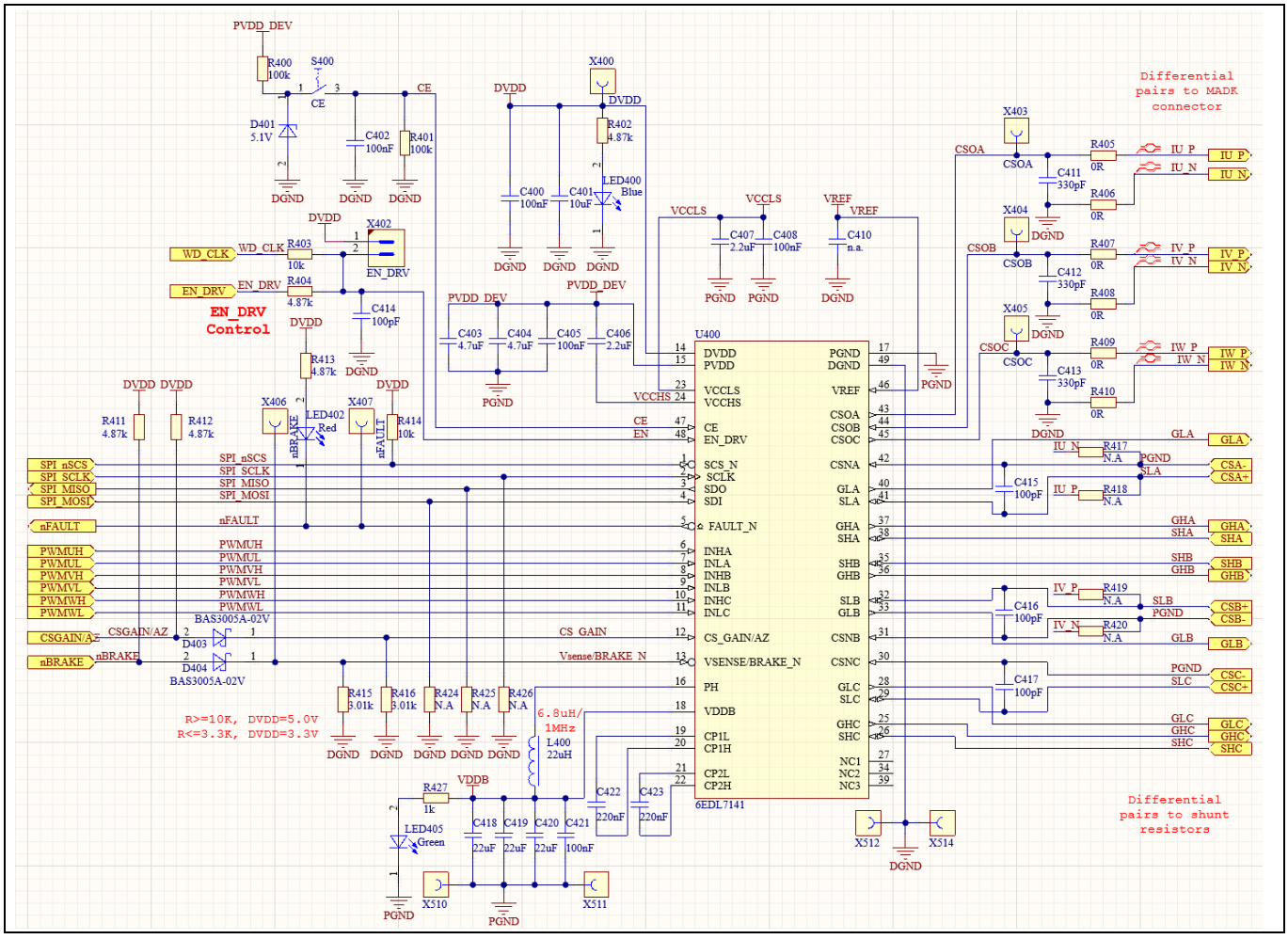

Figure 15 EVAL_6EDL7141_1KW_36V schematic – Gate driver section

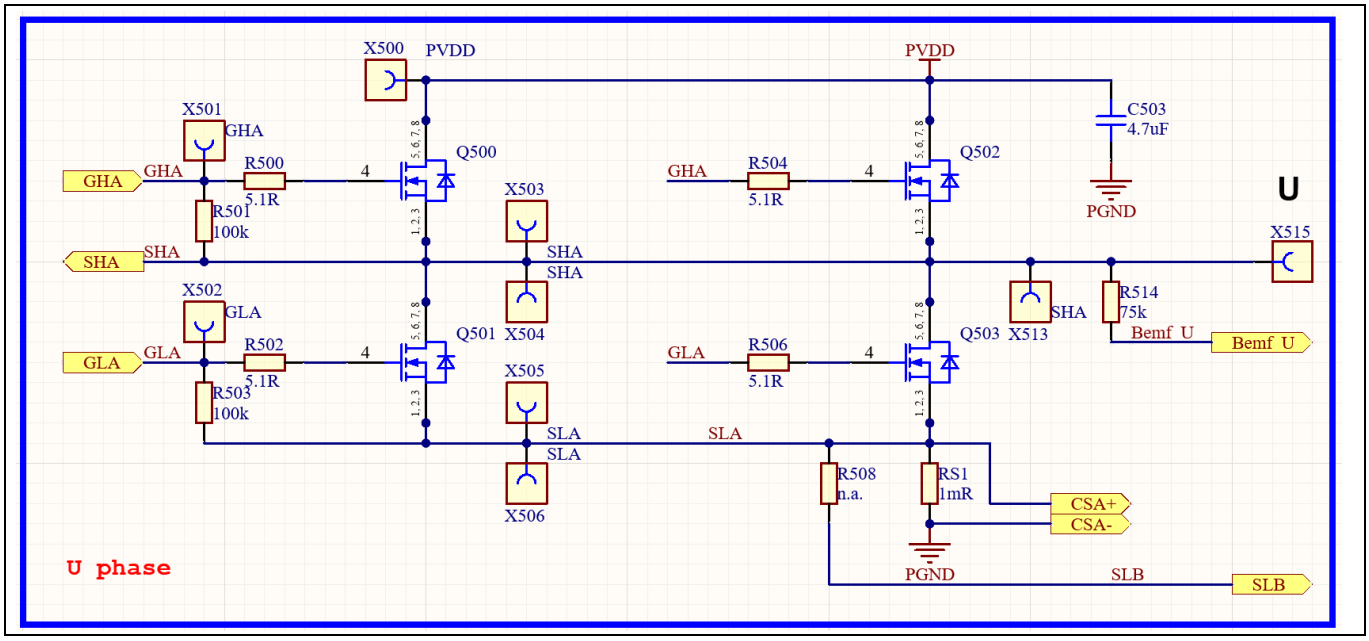

Figure 16 EVAL_6EDL7141_1KW_36V schematic – power stage, phase U

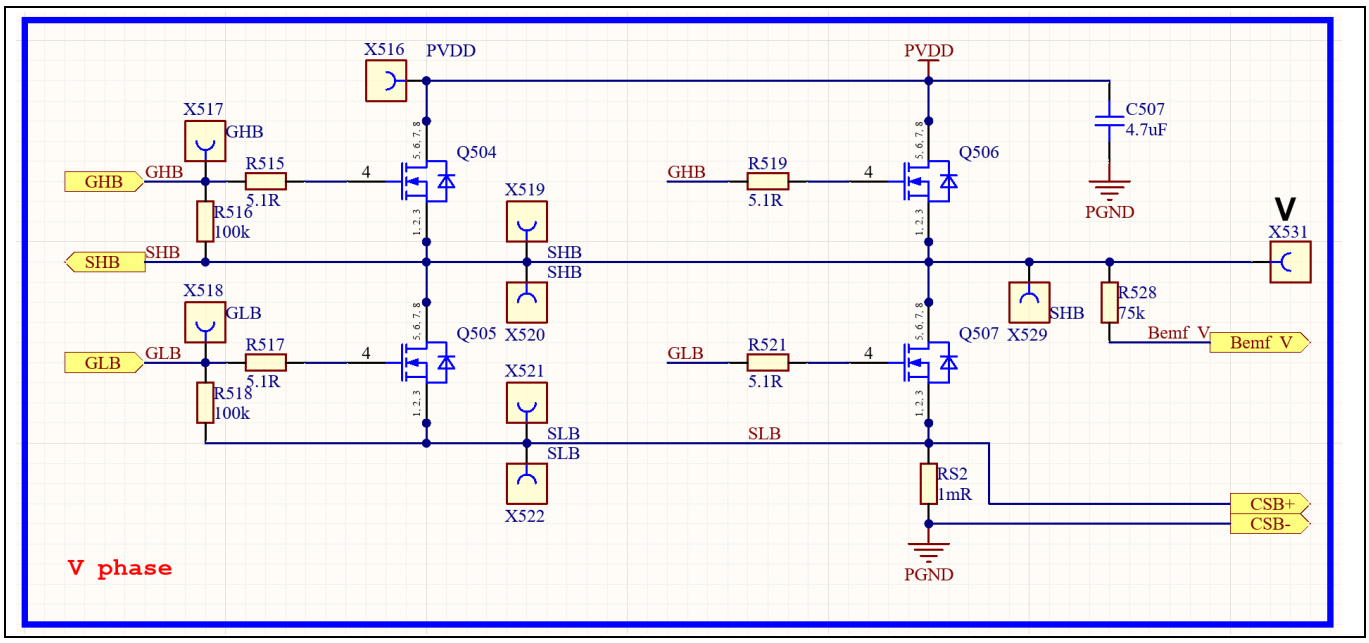

Figure 17 EVAL_6EDL7141_1KW_36V schematic – power stage, phase V

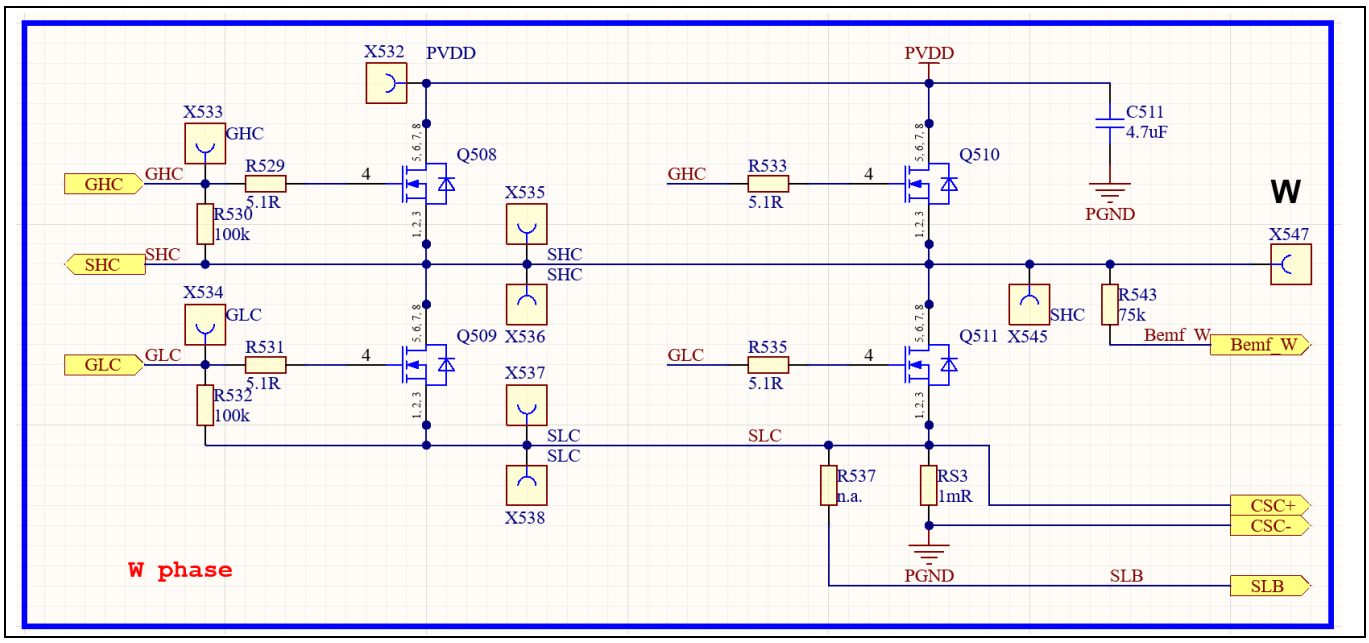

Figure 18 EVAL_6EDL7141_1KW_36V schematic – power stage, phase W

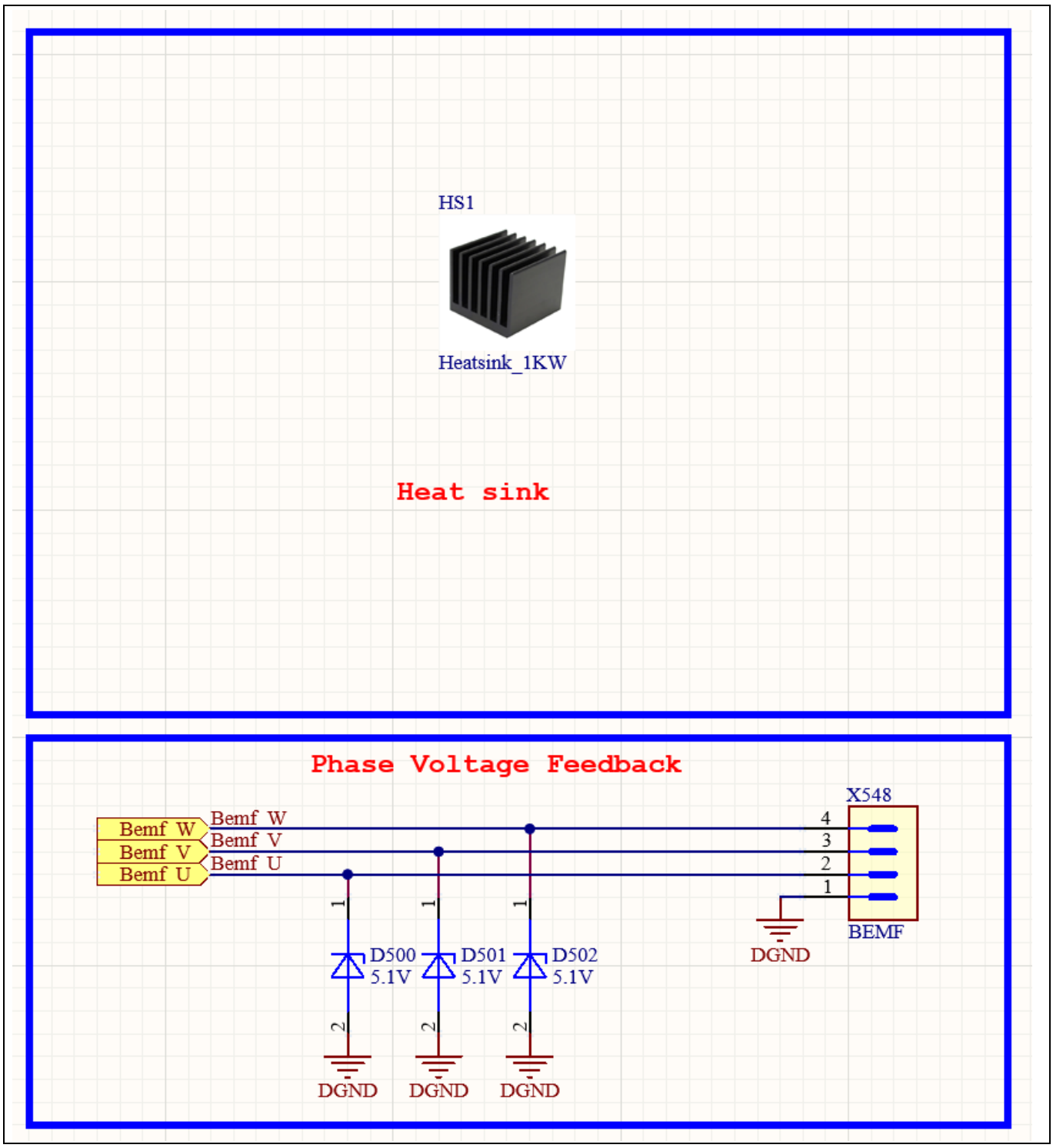

Figure 19 EVAL_6EDL7141_1KW_36V schematic – BEMF and heatsink

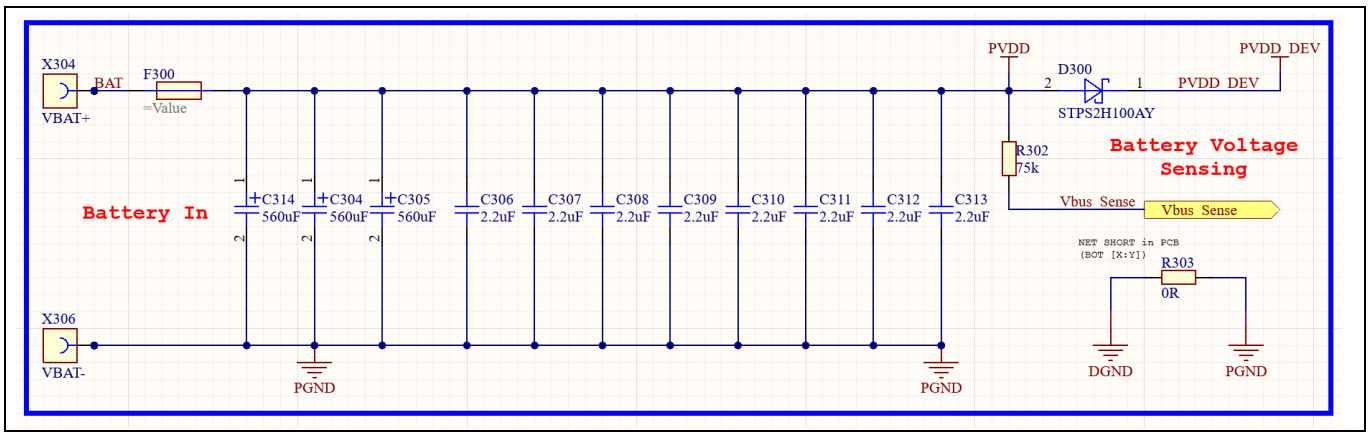

Figure 20 EVAL_6EDL7141_1KW_36V schematic – DC input

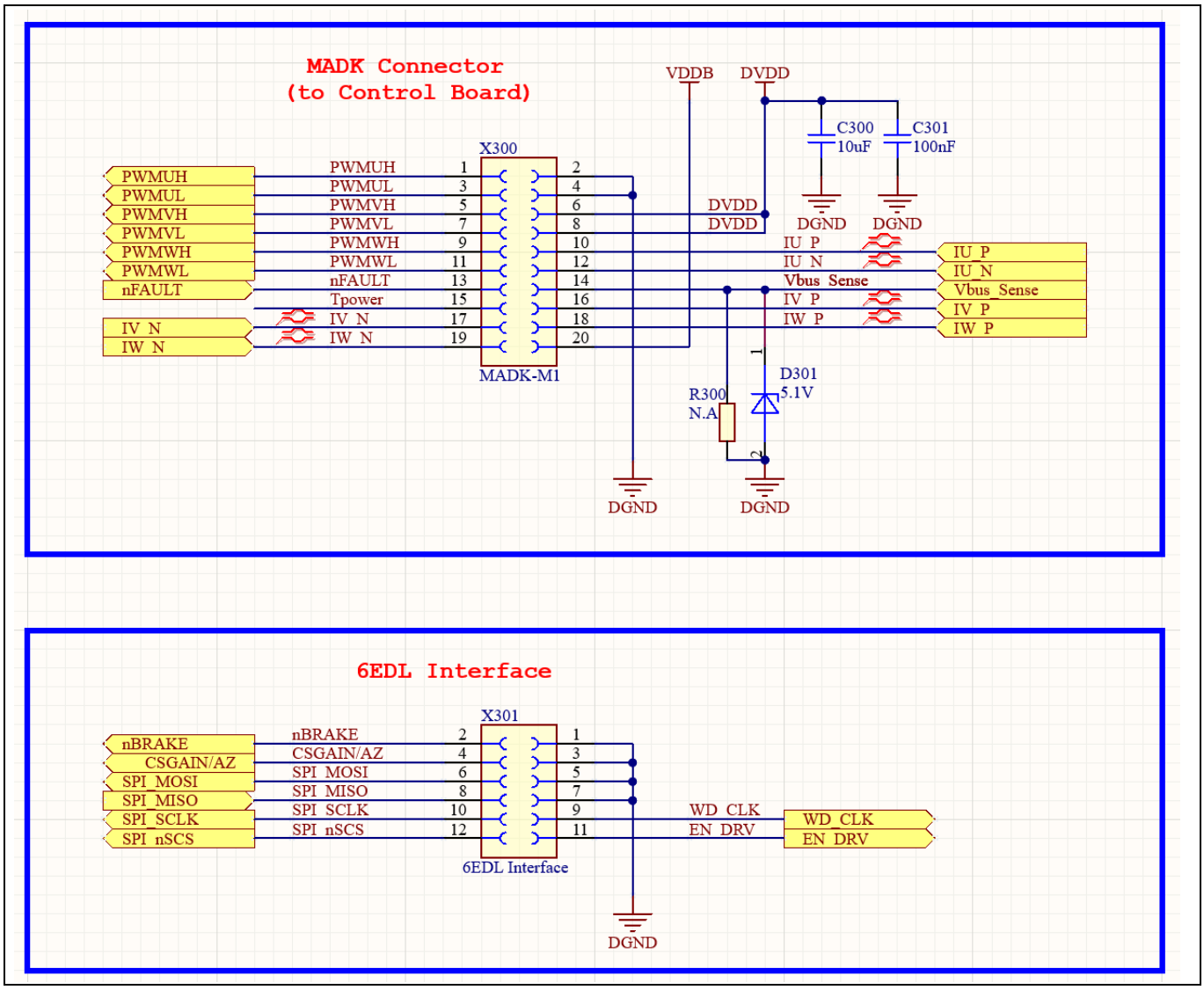

Figure 21 EVAL_6EDL7141_1KW_36V schematic – Connectors

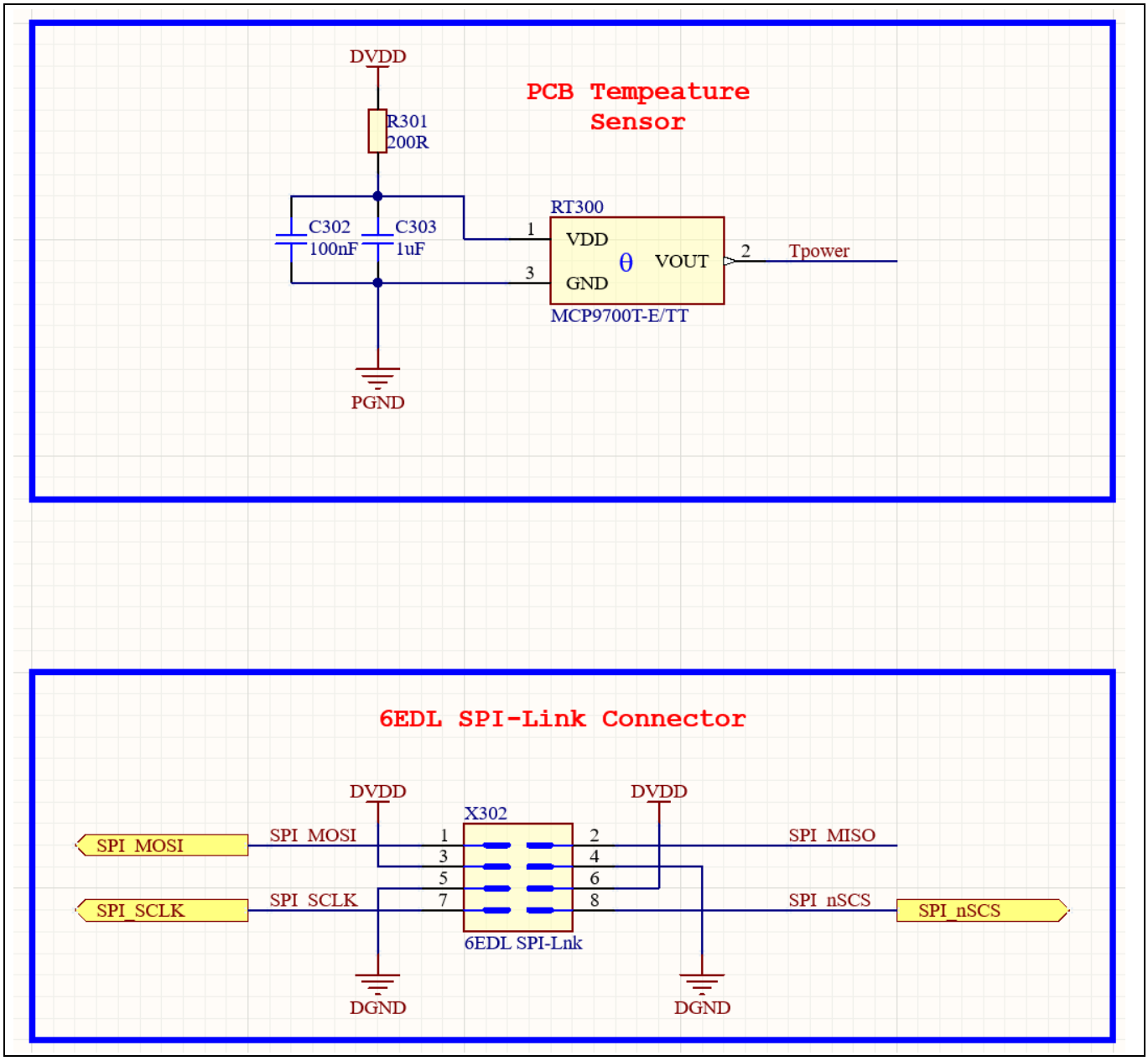

Figure 22 EVAL_6EDL7141_1KW_36V schematic – SPI-Link and temperature

4.2 PCB layout

EVAL_6EDL7141_1KW_36V reference board utilizes a six-layer PCB with 2 oz. on each layer. Components are mounted on the top and bottom sides. The width is 3.7 inches/93.98 mm and the length is 4.5 inches/114.3 mm.

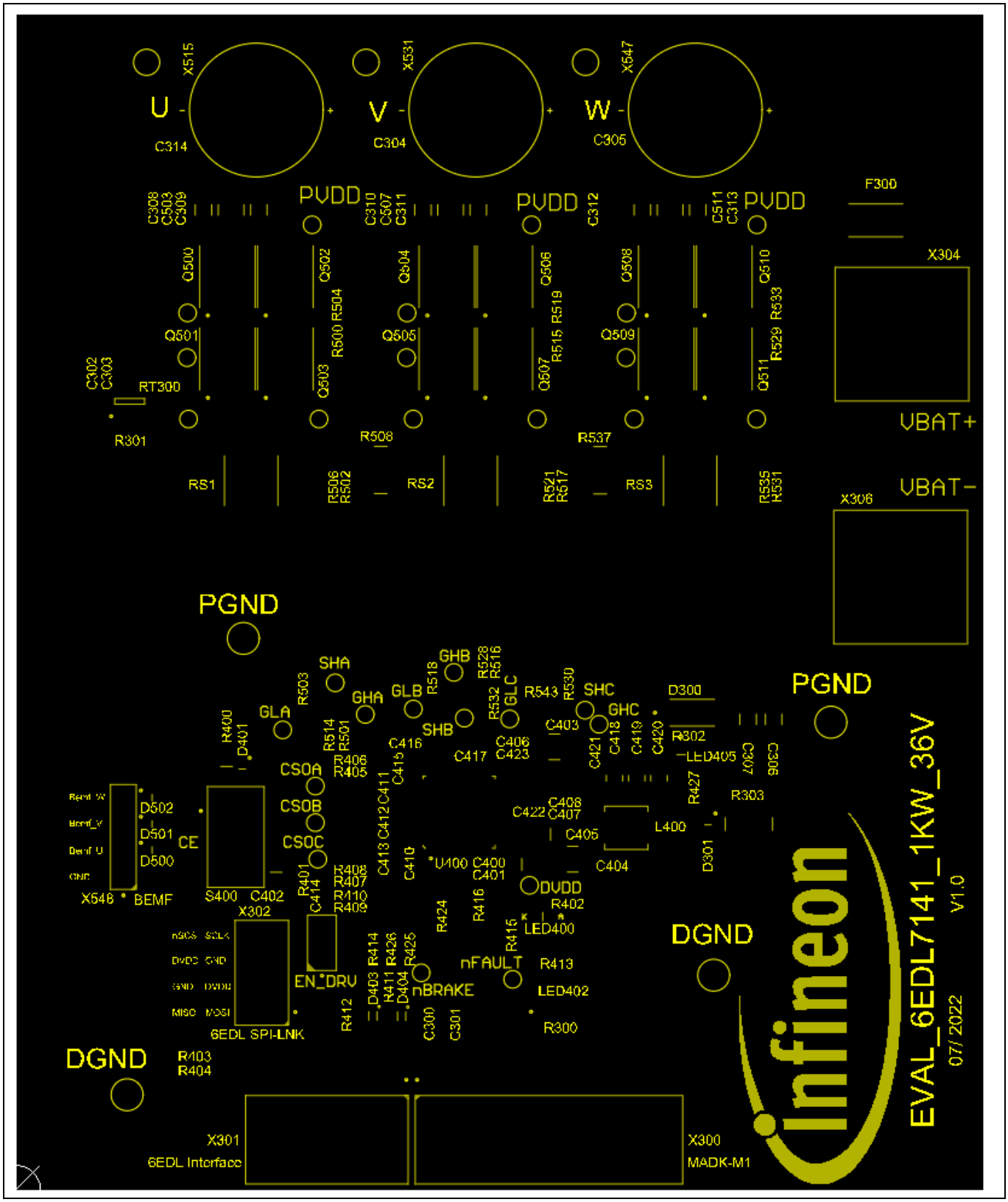

Figure 23 EVAL_6EDL7141_1KW_36V PCB top silkscreen

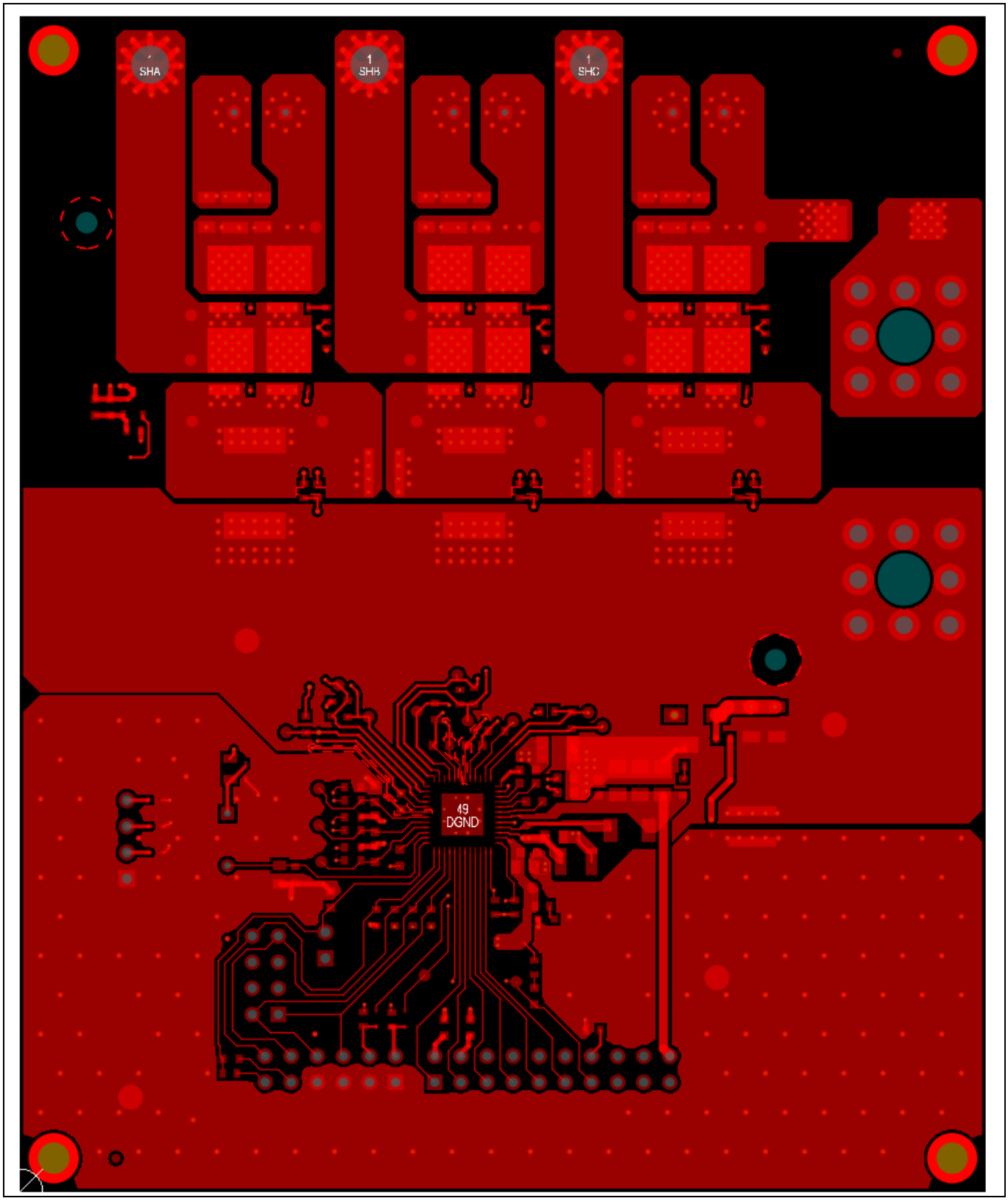

Figure 24 EVAL_6EDL7141_1KW_36V PCB top layer

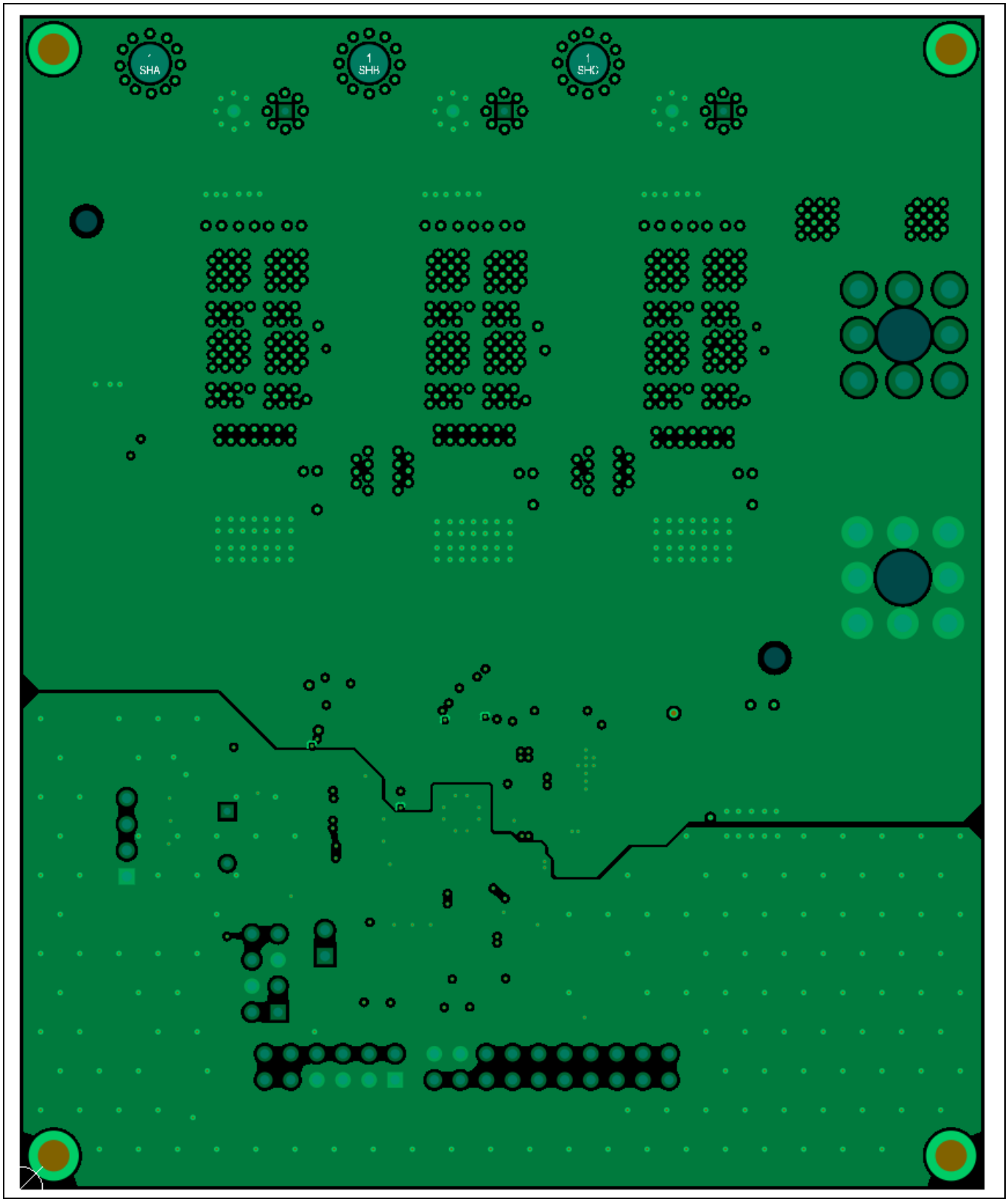

Figure 25 EVAL_6EDL7141_1KW_36V PCB inner layer1

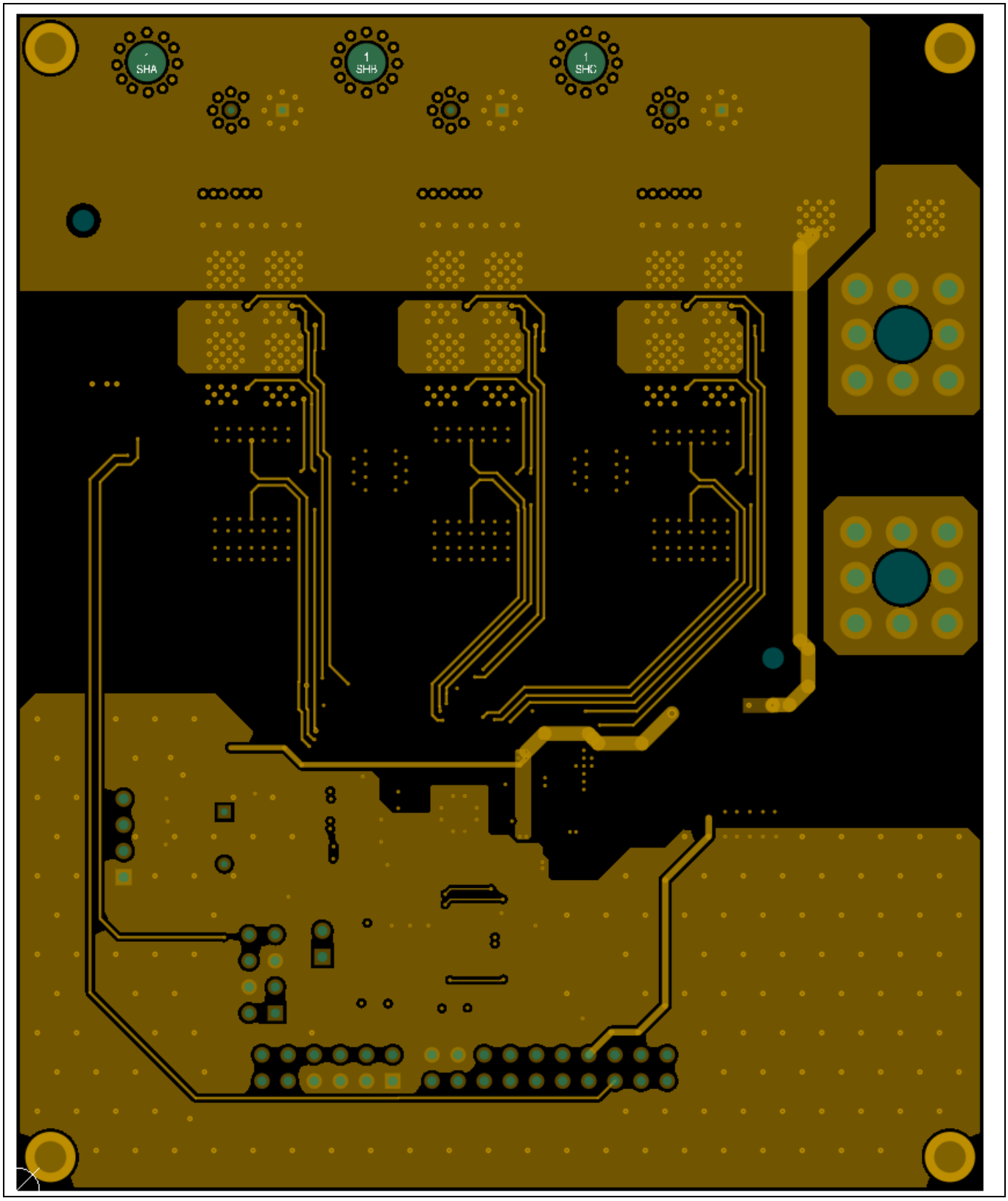

Figure 26 EVAL_6EDL7141_1KW_36V PCB inner layer 2

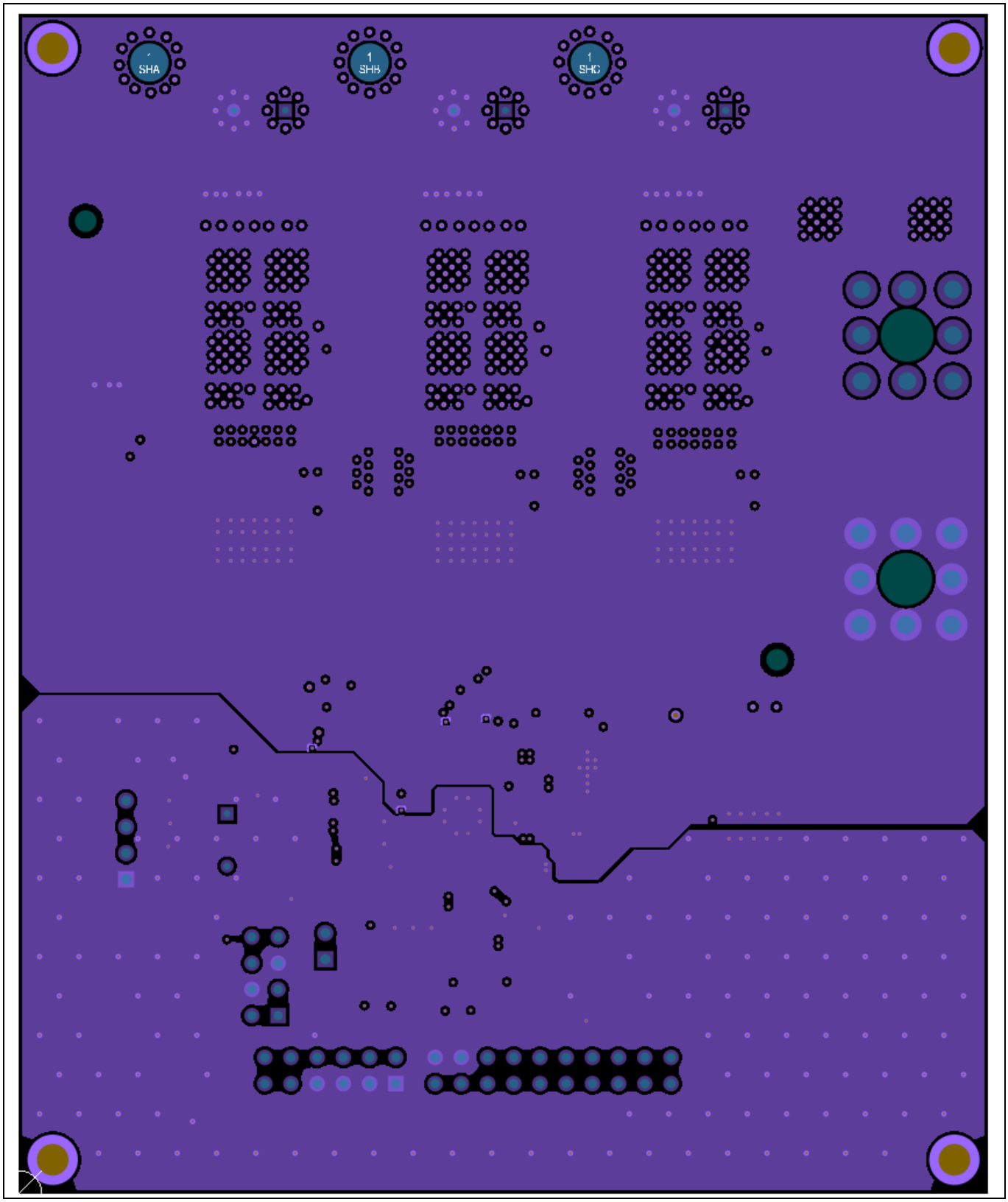

Figure 27 EVAL_6EDL7141_1KW_36V PCB inner layer 3

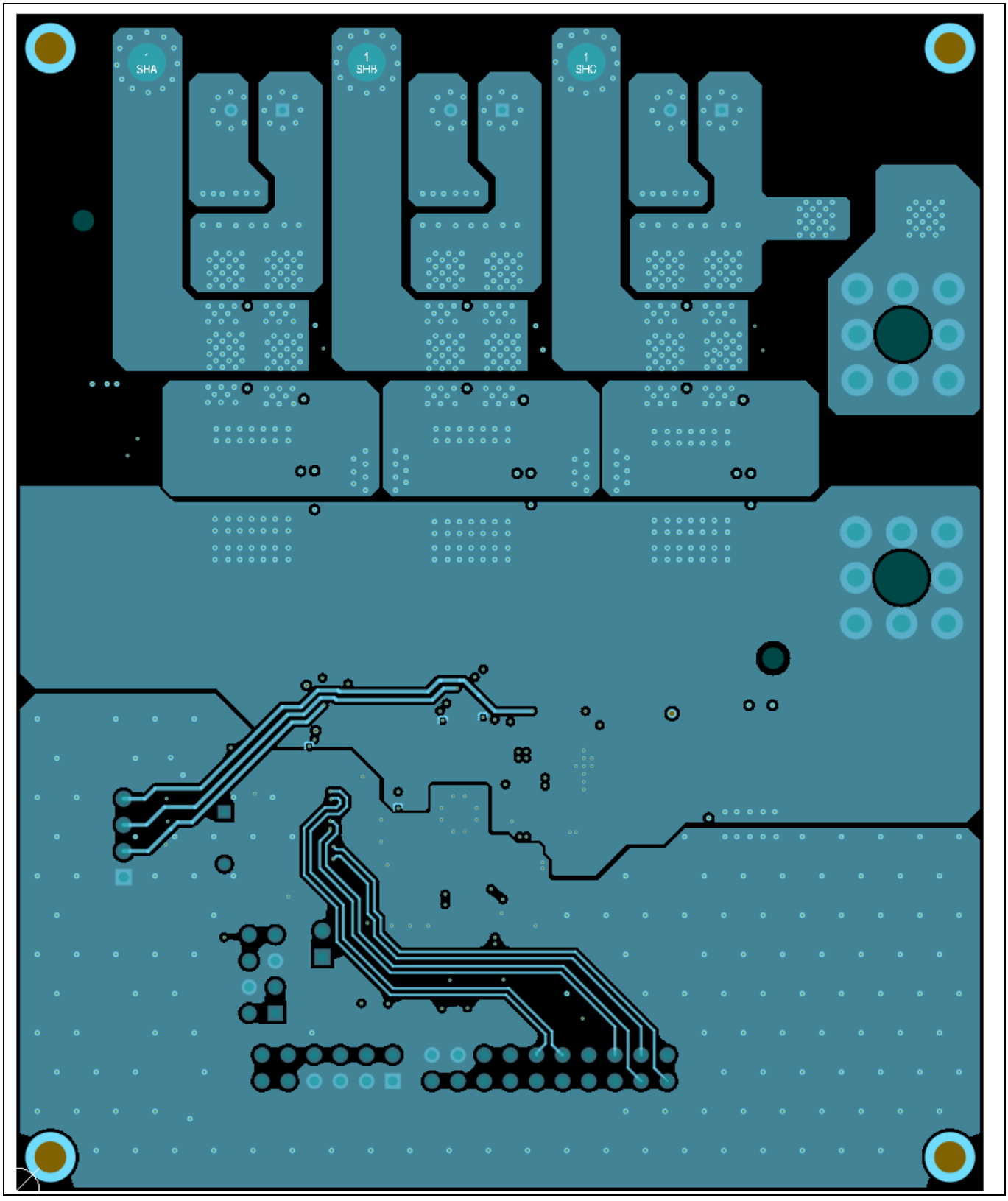

Figure 28 EVAL_6EDL7141_1KW_36V PCB inner layer 4

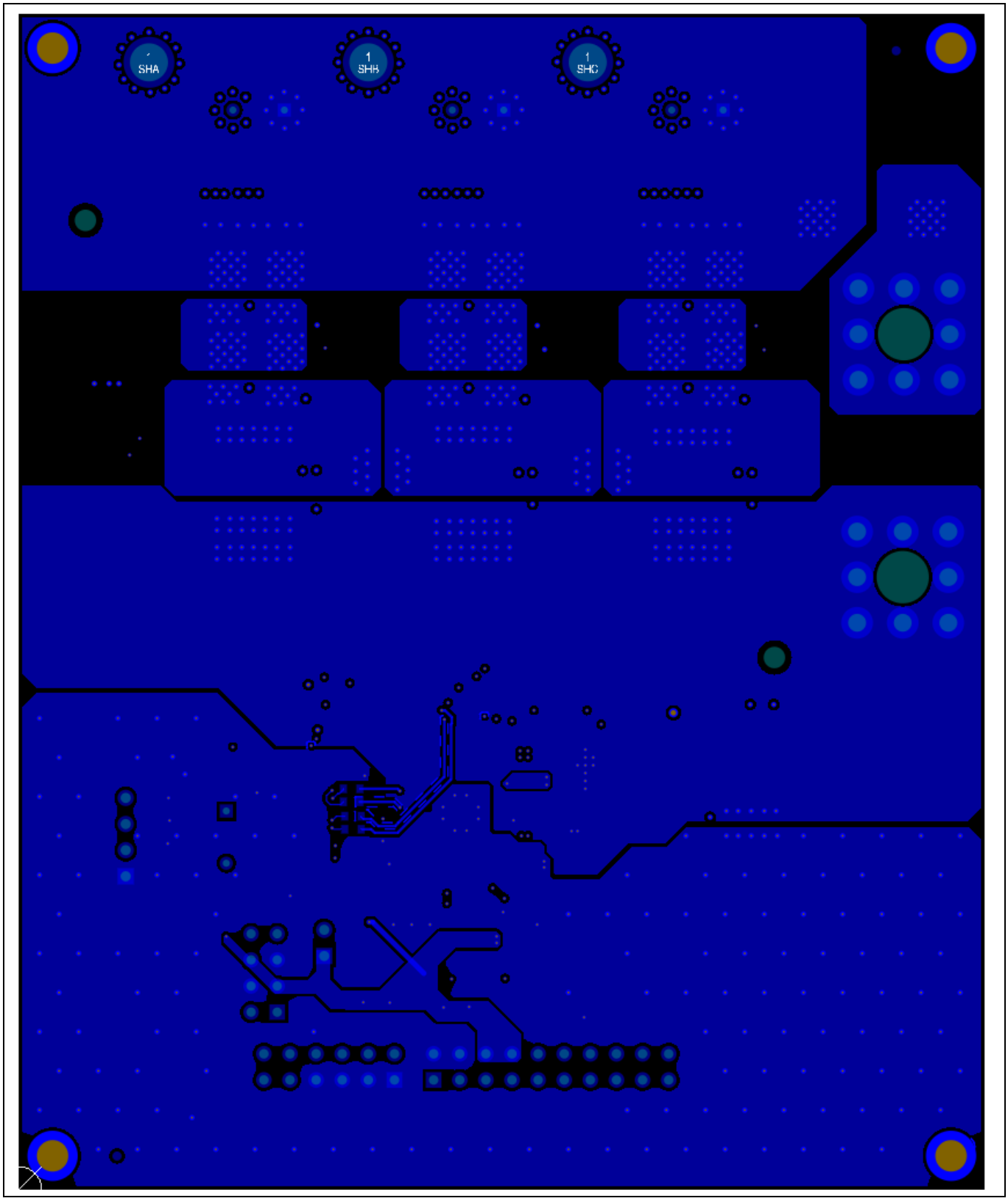

Figure 29 EVAL_6EDL7141_1KW_36V PCB bottom layer

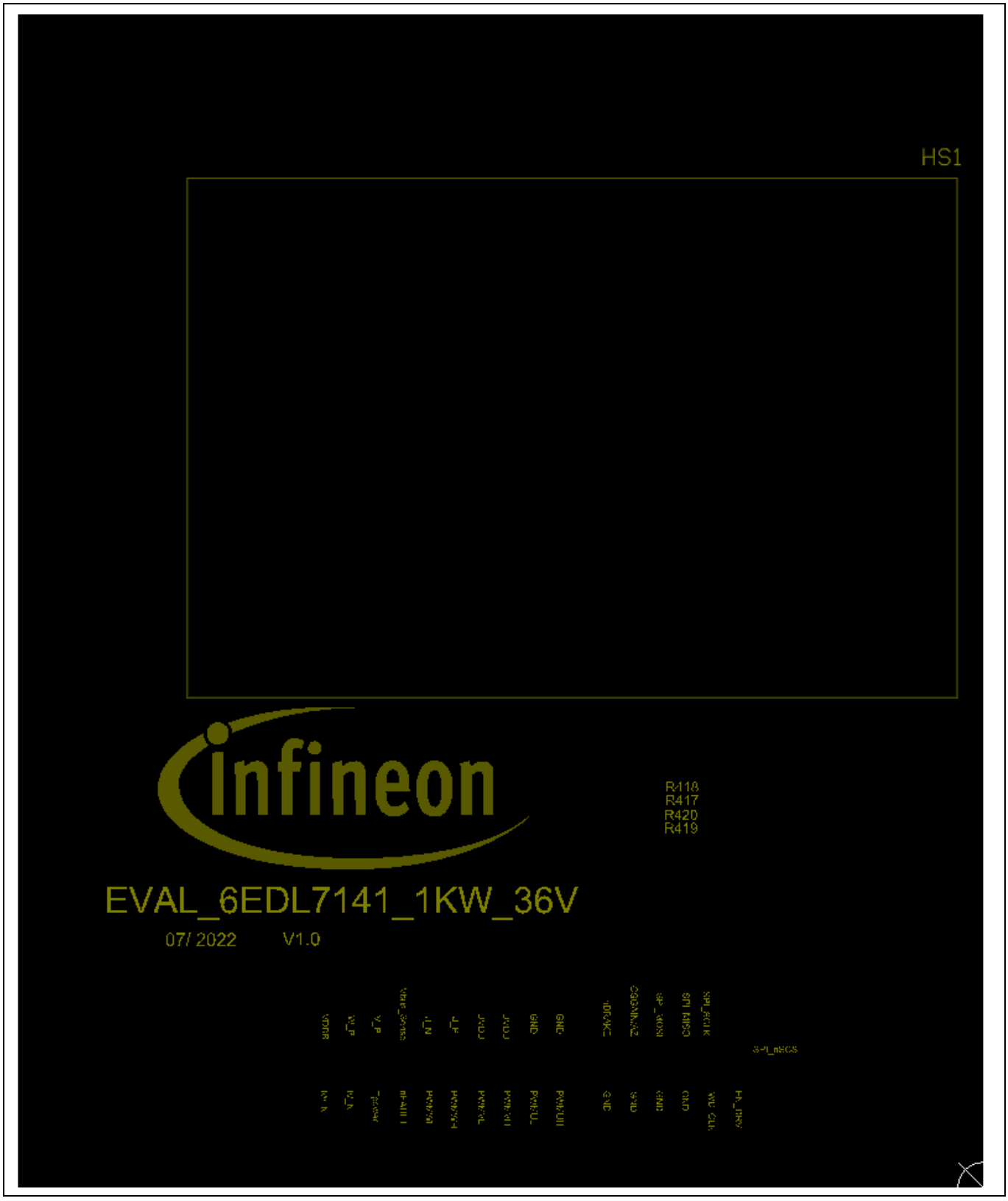

Figure 30 EVAL_6EDL7141_1KW_36V PCB bottom silkscreen

The PCB layout is optimized to minimize radiated EMI. This is achieved by keeping the loops carrying the switching currents as small as possible. The HF switching current loops are illustrated in the following. Note that during the switching transition, the high-side gate drive loop current returns to the main ground rather than back to the gate driver as in a conventional high-side driver. Because of this, keep the high-side gate drive loop as close as possible. The top layer connects the DC bus to the top-side MOSFET drains and the first internal layer returns the MOSFET current via the CS shunt. The switching loop for each phase begins and ends at the electrolytic capacitor and HF decoupling capacitors. The return traces on the first internal layer pass underneath the power traces, therefore, creating very tight HF switching loops.

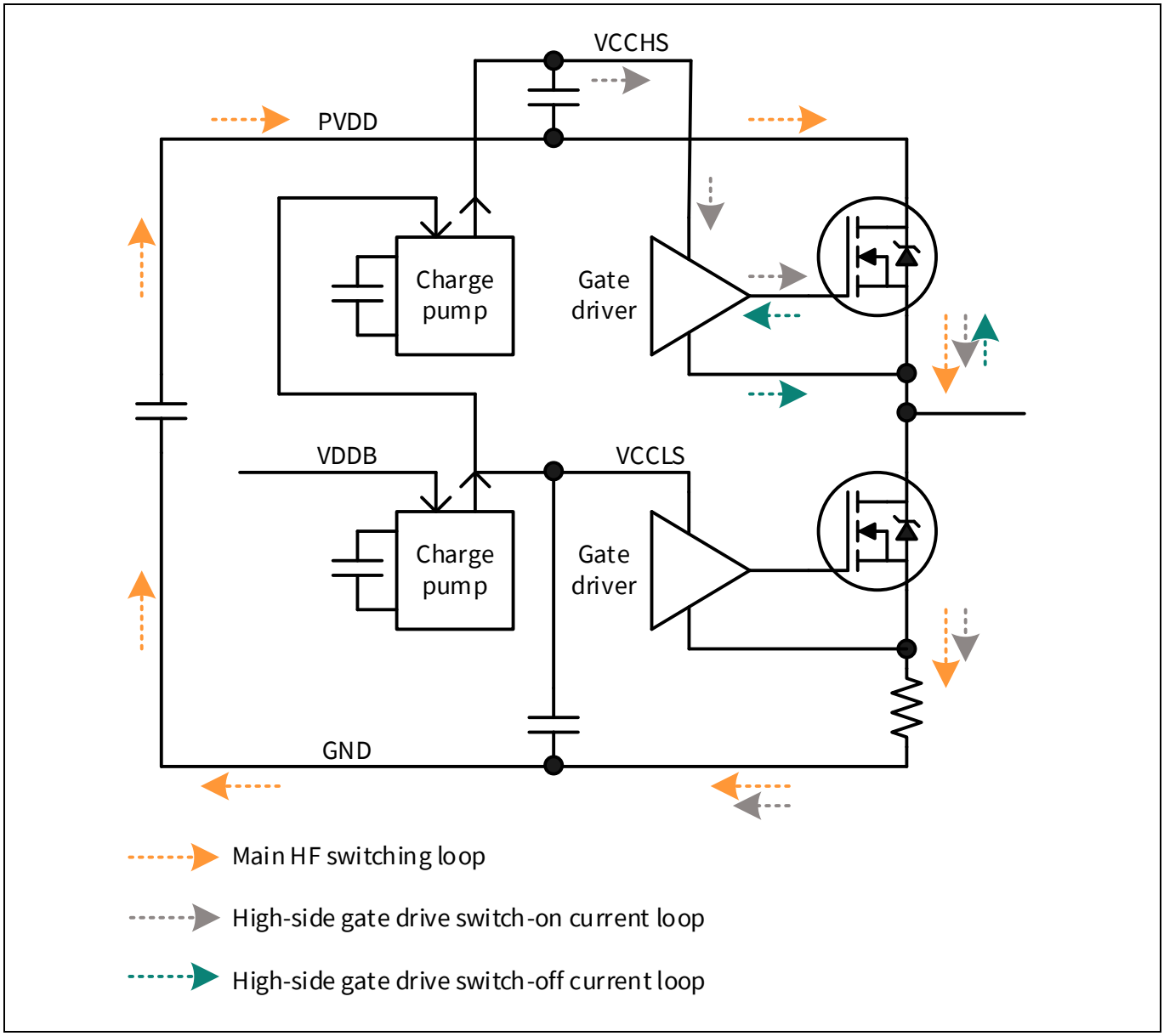

Figure 31 HF current loop for one phase

4.3 Bill of materials

Table 3 EVAL_6EDL7141_1KW_36V - BOM list

Part references	Qty	Value/rating	Manufacturer	Part number
C300	1	10 uF/10 V/0603	Murata	GRM188R61A106KE69
C301, C302, C400, C408, C421	5	100 nF/50 V/0603	AVX	06035C104K4Z2A
C303, C410	2	1 uF/10 V/0603	Murata	GRM188R71A105KA61
C304, C305, C314	3	560 uF/63 V/20%	Nippon Chemi-Con	EKZE630ELL561MK35S
C306, C307, C308, C309, C310, C311, C312, C313	8	2.2 uF/100 V/1206	Murata	GRM31CR72A225KA73
C401	1	10 uF/10 V/0805	Murata	GRM21BR71A106KA73
C402, C405	2	100 nF/100 V/0805	Murata	GRM21BR72A104KAC4
C403, C404, C503, C507, C511	5	4.7 uF/100 V/3225	TDK Corporation	CNA6P1X7R2A475K250AE
C406, C407	2	2.2 uF/25 V/0603	Murata	GRM188R61E225ME84
C411, C412, C413	3	330 pF/100 V/0603	Murata	GRM1885C2A331GA01
C414, C415, C416, C417	4	100 pF/50 V/0603	Kemet	C0603C101F5GAC
C418, C419, C420	3	22 uF/25 V/1206	TDK Corporation	C3216X5R1E226M160AB
C422, C423	2	220 nF/25 V/0603	Murata	GRM188R71E224KA88
D300	1	100 V/2 A/SMA	STMicroelectronics	STPS2H100AY
D301, D401, D500, D501, D502	5	5.1 V/500 mW/SOD523	ON Semiconductor	SZMM5Z5V1T1G
D403, D404	2	30 V/0.5 A	Infineon Technologies	BAS3005A-02V
F300	1	30 A/250 V AC/72 V DC	Cooper Bussmann	1025HC30-RTR
HS1	1	Heatsink/75*50.5 mm	–	Heatsink_1KW
L400	1	22 uH/1 A/4020	Würth Elektronik	74437324220
LED400	1	Blue/3.2 V/0603	Würth Elektronik	150060BS75000
LED402	1	Red/2.0 V/0603	Everlight	19-21SURC/S530-A3/TR8
LED405	1	Green/2.2 V/0603	ROHM Semiconductors	SML-D12P8WT86

Part references	Qty	Value/rating	Manufacturer	Part number
Q500, Q501, Q502, Q503, Q504, Q505, Q506, Q507, Q508, Q509, Q510, Q511	12	60 V/1.2 mΩ/TSON-8-3	Infineon Technologies	BSC012N06NS
R300	1	6.2k/100 mW/1%/0603	Vishay	CRCW06036K20FK
R301	1	200R/100 mW/1%/0603	Vishay	CRCW0603200RFK
R302, R514, R528, R543	4	75k/100 mW/1%/0603	Vishay	CRCW060375K0FK
R303	1	0R/1 W/1218	Vishay	CRCW12180000Z0EA
R400	1	100k/125 mW/1%/0805	Vishay	CRCW0805100KFK
R401, R501, R503, R516, R518, R530, R532	7	100k/100 mW/1%/0603	Yageo	RC0603FR-07100KL
R402, R404, R411, R412, R413	5	4.87k/100 mW/1%/0603	Vishay	CRCW06034K87FK
R403, R414, R424, R425, R426	5	10k/100 mW/1%/0603	Yageo	RC0603FR-0710KL
R405, R406, R407, R408, R409, R410, R417, R418, R419, R420	10	0R/100 mW/0603	Yageo	RC0603JR-070RL
R415, R416	2	3.01k/100 mW/1%/0603	Vishay	CRCW06033K01FK
R427	1	1k/100 mW/1%/0603	Yageo	RC0603FR-071KL
R500, R502, R504, R506, R515, R517, R519, R521, R529, R531, R533, R535	12	5.1R/100 mW/1%/0603	Vishay	CRCW06035R10FK
RS1, RS2, RS3	3	1mR/8 W/1%/3920	Bourns	CSS2H-3920R-1L00F
RT300	1	Sensor/SOT23-3	Microchip Technology	MCP9700T-E/TT
S400	1	Slide/SPST/0.4 VA/28 V	NKK Switches	AS11CP

Part references	Qty	Value/rating	Manufacturer	Part number
U400	1	Gate driver/3-Phase	Infineon Technologies	6EDL7141
X300	1	Connector/20 pins/2.54 mm	Samtec	SSW-110-03-F-D-RA
X301	1	Connector/12 pins/2.54 mm	Samtec	SSW-106-03-F-D-RA
X302	1	Header/8pos/2.54 mm	Samtec	TSW-104-08-F-D
X304, X306	2	Connector/85 A/10 x 10 x 6.5 mm	Würth Elektronik	74655095R
X402	1	Header, vertical, 2x1, through hole, 2.54	Samtec	TSW-102-08-G-S
X548	1	Header, vertical, 4x1, through hole, 2.54	Samtec	TSW-104-07-L-S

4.4 Connector details

Table 4 DC input connector

Pin	Label	Function
X304	VBAT+	Positive of the DC input
X306	VBAT-	Negative of the DC input

Table 5 Motor connector

Pin	Label	Function
X515	U	U phase for the BLDC/PMSM
X531	V	V phase for the BLDC/PMSM
X547	W	W phase for the BLDC/PMSM

Table 6 BEMF connector (X548)

Pin	Label	Function
1	GND	Digital ground
2	Bemf_U	Back electromotive force from U phase
3	Bemf_V	Back electromotive force from V phase
4	Bemf_W	Back electromotive force from W phase

Table 7 SPI-Link connector (X548)

Pin	Label	Function
1	MOSI	SPI data input signal
2	MISO	SPI data output signal
3	DVDD	Digital power

Pin	Label	Function
4	GND	Digital ground
5	–	–
6	DVDD	Digital power
7	SCLK	SPI clock signal
8	GND	Digital ground

Table 8 6EDL interface connector (X301)

Pin	Label	Function
1	GND	Digital ground
2	nBRAKE	Analog programming of DVDD output voltage during start-up. Connect a pull-down resistor to select DVDD voltage: R ≤ 3.3 kΩ → DVDD = 3.3 V R ≥ 10 kΩ → DVDD = 5.0 V After start-up, pin will be in nBRAKE mode: Used for motor braking. Active low
3	GND	Digital ground
4	CSGAIN/AZ	Analog programming for the shunt amplifier gain. Dual function as Auto-Zero: Input to control external Auto-Zero function
5	GND	Digital ground
6	SPI_MOSI	SPI data input signal
7	GND	Digital ground
8	SPI_MISO	SPI data output signal
9	WD_CLK	Configured as watchdog clock
10	SPI_SCLK	SPI clock signal
11	EN_DRV	Enables the gate driver section and internal circuitry based on the configuration
12	SPI_nSCS	Chip Select for SPI. Active low

Table 9 MADK-M1 connector (X300)

Pin	Label	Function
1	PWMUH	PWM input signal for phase U high side. Common PWM signal for PWM mode 1. Connect to DGND if not used.
2	GND	DGND
3	PWMUL	PWM input signal for phase U low side. Input of Hall sensor U in 1PWM modes. Connect to DGND if not used.
4	GND	DGND

Pin	Label	Function
5	PWMVH	PWM input signal for phase V high side. Connect to DGND if not used.
6	DVDD	Digital power
7	PWMVL	PWM input signal for phase V low side. Input of Hall sensor V in 1PWM modes. Connect to DGND if not used.
8	DVDD	Digital power
9	PWMWH	PWM input signal for phase W high side. DIR signal for 1PWM modes. Connect to DGND if not used.
10	IU_P	Low side source connection for phase U. Positive input of shunt amplifier A for shunt sensing. Short to PGND if not used.
11	PWMWL	PWM input signal for phase W low side. Input of Hall sensor C in 1PWM modes. Connect to DGND if not used.
12	IU_N	Current sense amplifier negative input for phase U. Short to PGND or DGND if not used.
13	nFAULT	When low indicates that a fault has occurred; connect external pull-up to MCU power supply.
14	Vbus_Sense	Sensing the DC link voltage through the resistor divider. This Ref board integrates a 75 kΩ pull-up resistor to DC bus+.
15	Tpower	Analog voltage output from the temperature sensor.
16	IV_P	Low side source connection for phase V. Positive input of shunt amplifier B for shunt sensing. Short to PGND if not used.
17	IV_N	Current sense amplifier negative input for phase B. Short to PGND or DGND if not used.
18	IW_P	Low side source connection for phase W. Positive input of shunt amplifier C for shunt sensing. Short to PGND if not used.
19	IW_N	Current sense amplifier negative input for phase C. Short to PGND or DGND if not used.
20	VDDB	Buck output voltage. Connect capacitor between VDDB and PGND.

5 Test results

5.1 Power measurements

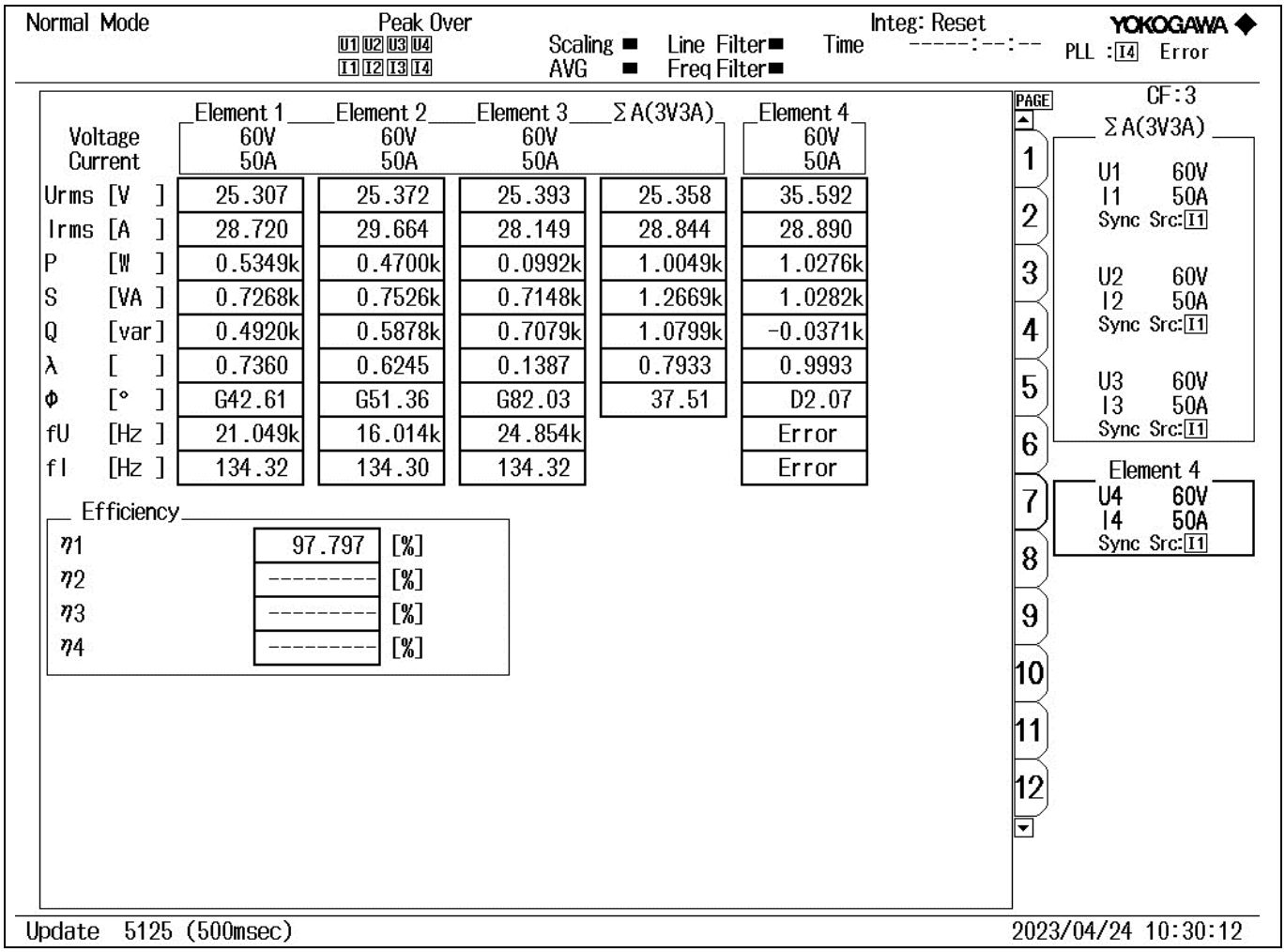

Figure 32 Input and output measurements at nominal input voltage 36 V and 1000 W input power

In the above results, element 4 represents the DC input to the inverter. Elements 1, 2, and 3 are connected to the output phases U, V, and W respectively.

From Figure 32, receives the input power rated of 1.0276 kW, and the output power rated of 1.0049 kW and an efficiency of 97.797%.

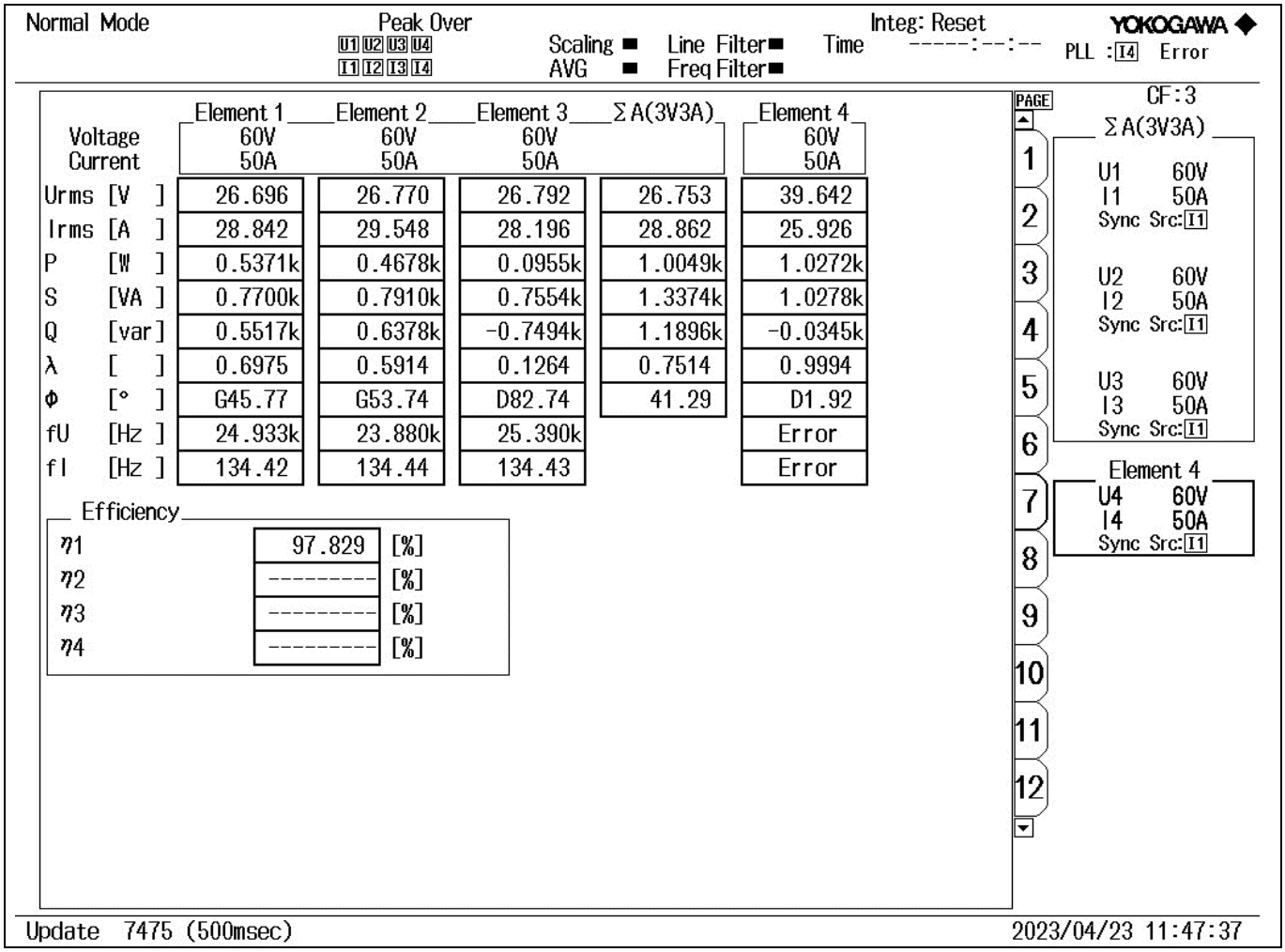

Figure 33 Input and output measurements at nominal input voltage 40 V and 1000 W input power

In the above results, element 4 represents the DC input to the inverter. Elements 1, 2, and 3 are connected to the output phases U, V, and W respectively.

From Figure 33, receives the input power rated of 1.0272 kW, and the output power rated of 1.0049 kW and an efficiency of 97.829%.

5.2 Thermal measurements

Thermal images are taken after 12 minutes of operation to allow the component temperatures to rise and reach steady-state. No heatsinking or forced air-cooling is used.

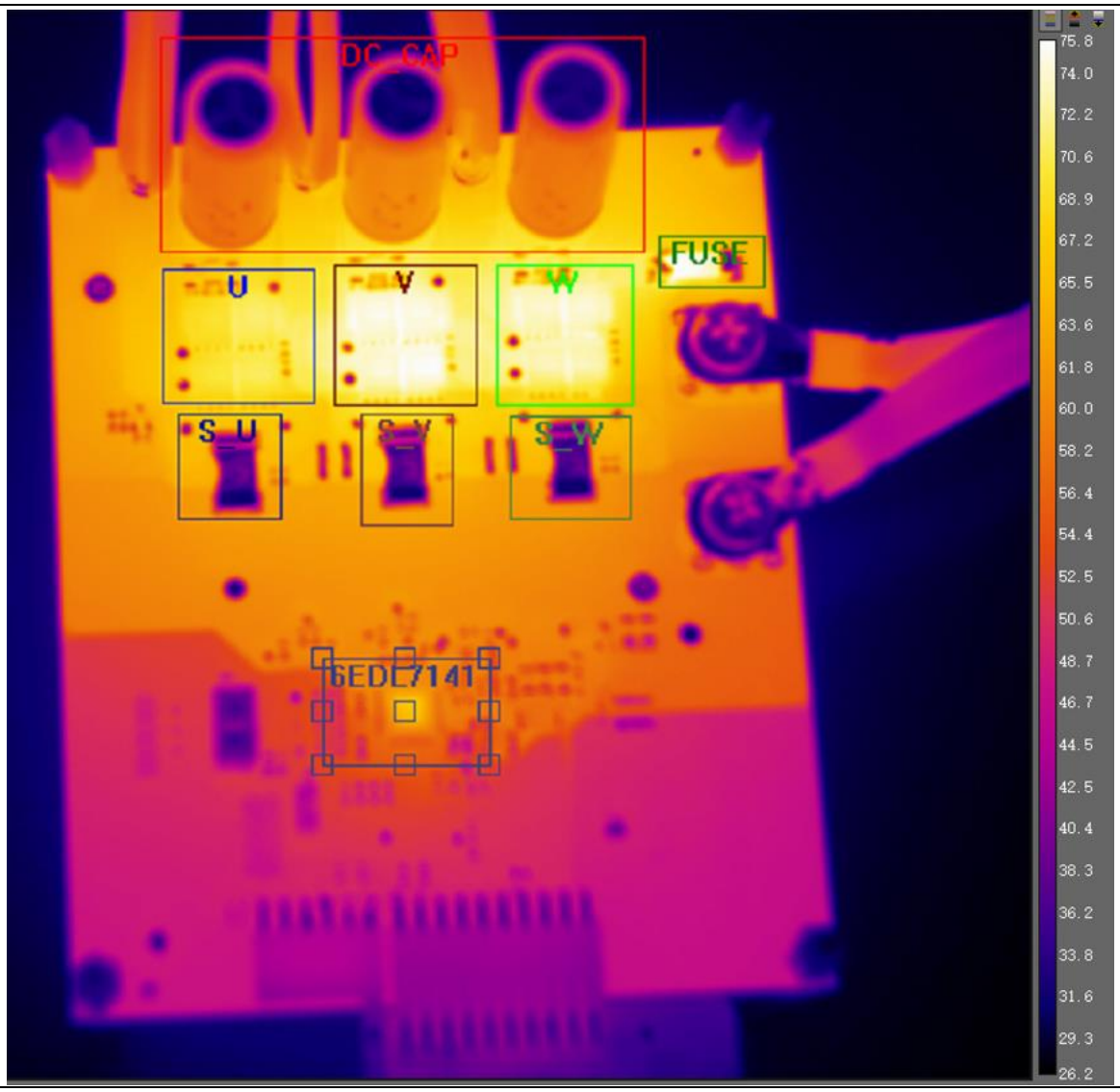

Figure 34 Thermal measurement summary at 36 V input and 1 kW input power run for 12 minutes

The temperature above shows the system at equilibrium after running for 12 minutes with 1 kW input power. Table 10 summarizes the measurements.

Table 10 Temperature of the components

Point of interest	Maximum temperature (°C)
DC input electrolyte capacitors	70.4
DC input fuse	75.8
Phase W MOSFETs	75.0
Phase V MOSFETs	75.6
Phase U MOSFETs	72.0

Point of interest	Maximum temperature (°C)
Phase W current sensing	67.0
Phase V current sensing	69.4
Phase U current sensing	66.7
6EDL7141	66.0

5.3 Operating waveforms

The evaluation board consists of power stage and 6EDL7141 smart integrated motor driver. To measure the hardware performance, it is connected to a control card with a PSoC™ 6 microcontroller to send the logical switching signals to the 6EDL7141 gate driver. The software operates the board with a trapezoidal algorithm. The following waveforms are captured on the EVAL_6EDL7141_1KW_36V board with a 36 V input.

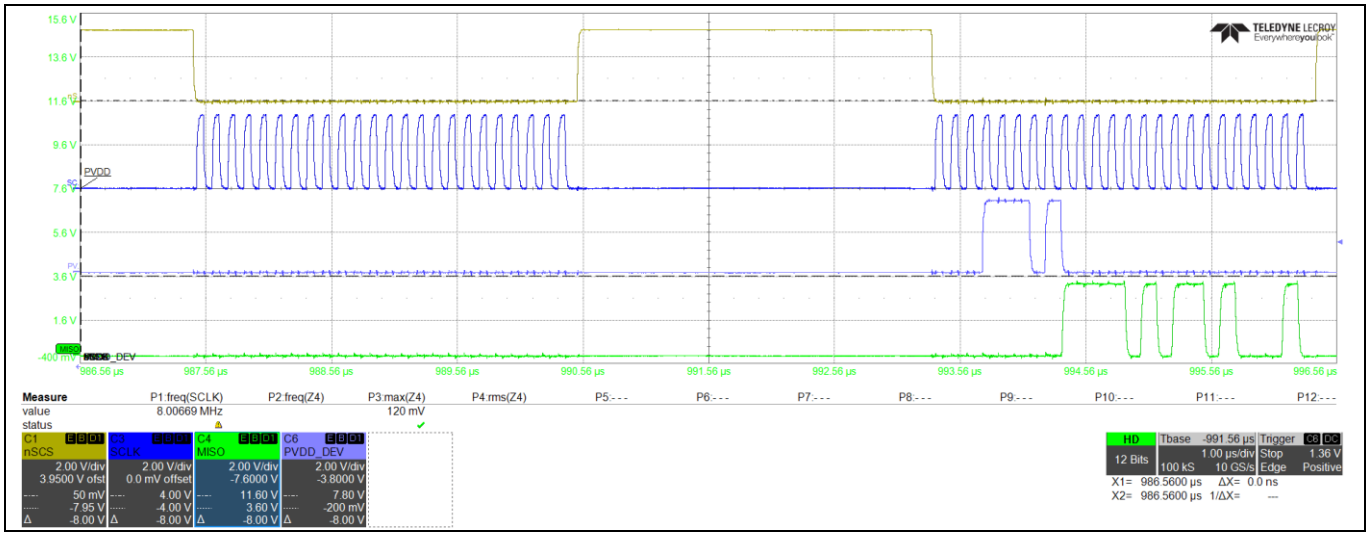

Figure 35 SPI interface signals waveform – SCLK (blue), MISO (green), MOSI (light blue), and nSCS(yellow)

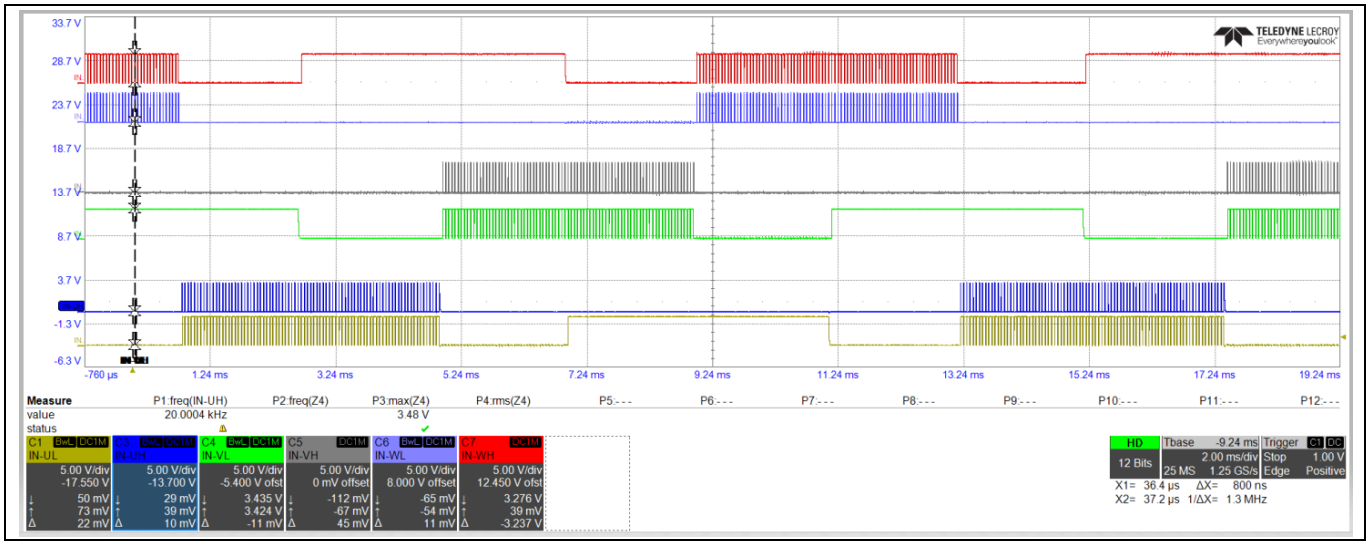

Figure 36 PWM signals input from the control card – U phase low side (yellow), U phase high side (blue), V phase low side (green), V phase high side (gray), W phase low side(light blue), and W phase high side(red)

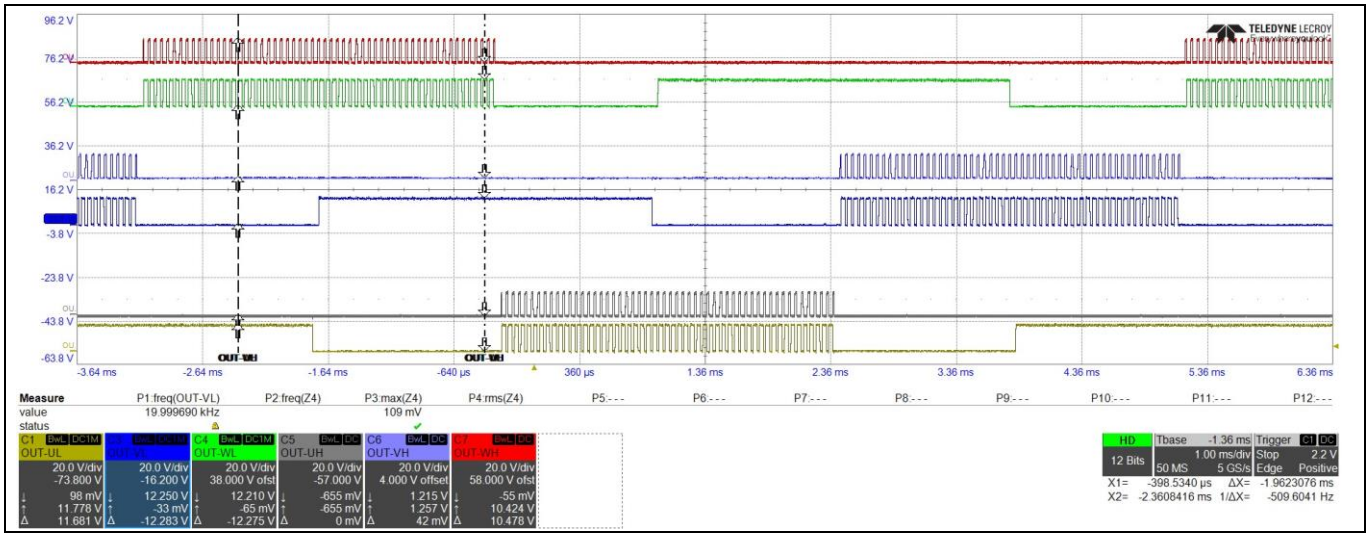

Figure 37 **High- and low-side gate drive pulses, 36 V input (1 ms/div) – $V_{GS\_LS\_phU}$ (yellow), $V_{GS\_HS\_phU}$ (gray), $V_{GS\_LS\_phV}$ (blue) $V_{GS\_HS\_phV}$ (purple), $V_{GS\_LS\_phW}$ (green), and $V_{GS\_HS\_phW}$ (red)**

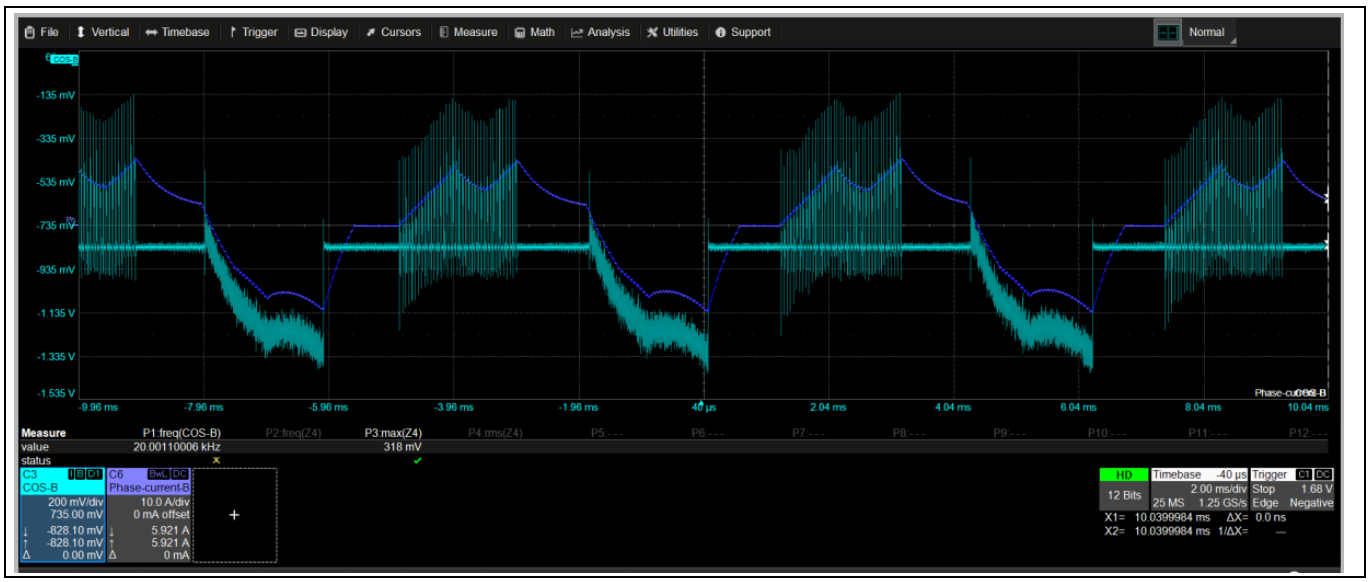

Figure 38 **Phase "V" operating current, 36 V input (500 ms/div) – I_{PHASE_V} (blue) sensing the current probe in the phase wire, I_{PHASE_V} (cyan) signals after the internal amplifier**

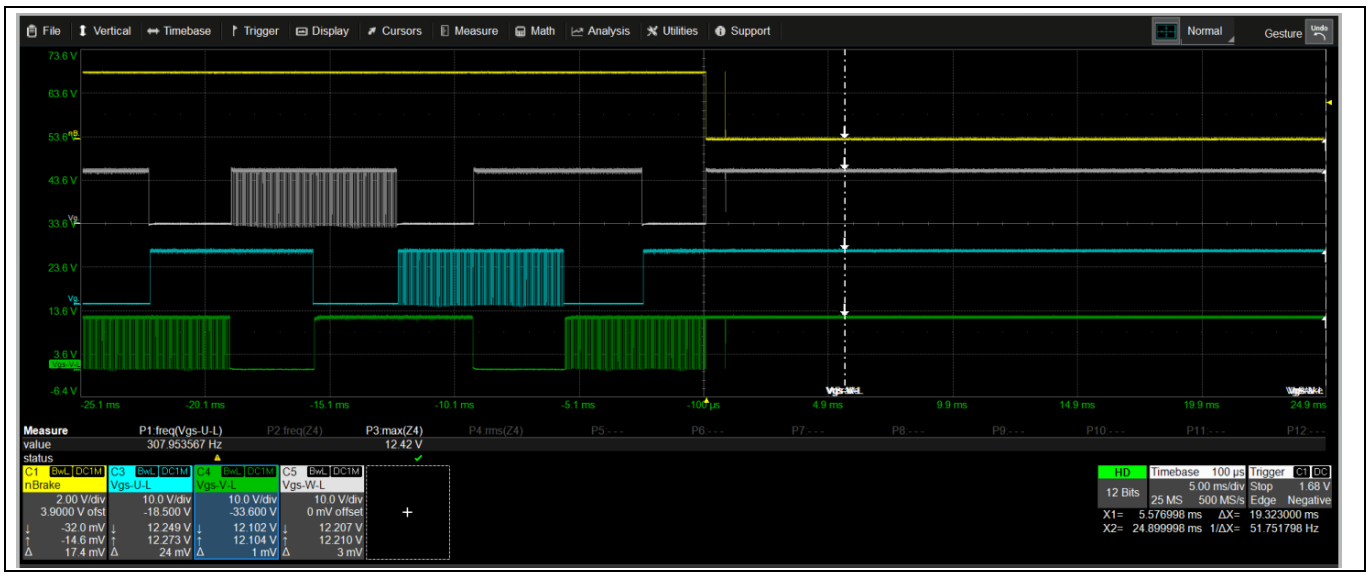

Figure 39 **N_BRAKE signal waveform – N_BRAKE (yellow), U_{GS_LS} (cyan), V_{GS_LS} (green), and W_{GS_LS}(gray)**

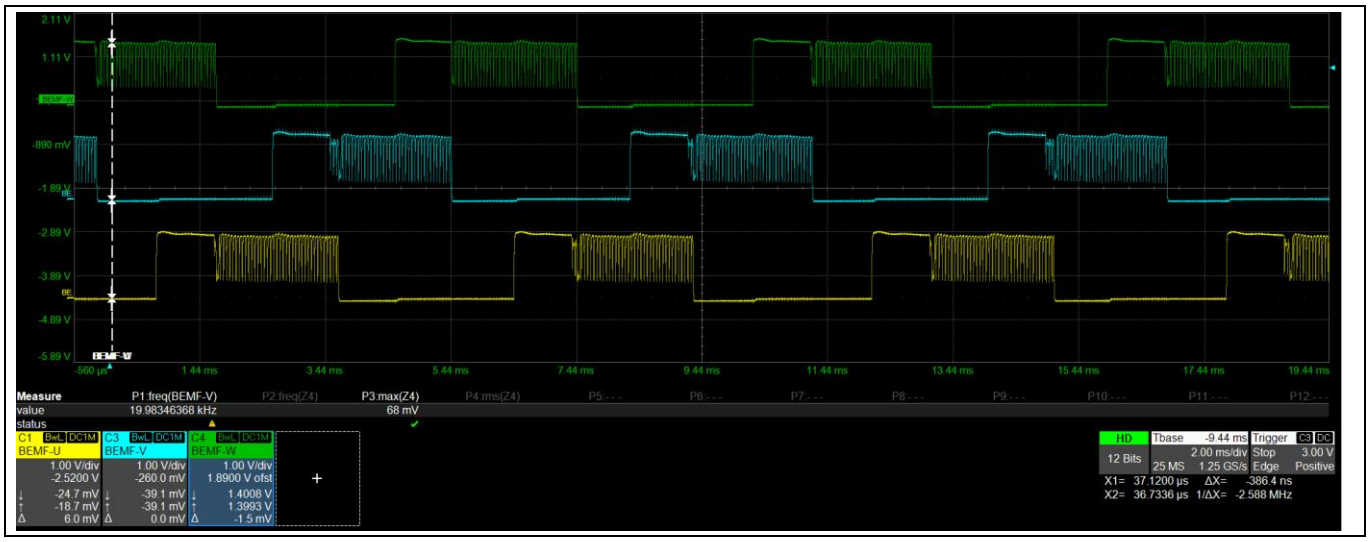

Figure 40 **Three-phase BEMF from the phase nodes – BEMF_U (yellow), BEMF_V (cyan), and BEMF_W(green)**

Figure 41 BEMF_V (yellow), INPUT_V_L (cyan), INPUT_V_H (green), V_{GS_LS} (gray), V_{GS_HS} (blue), $I_{PHASE\_CURRETN}$ (red), I_{PHASE_B} (orange) (signals after the internal amplifier)

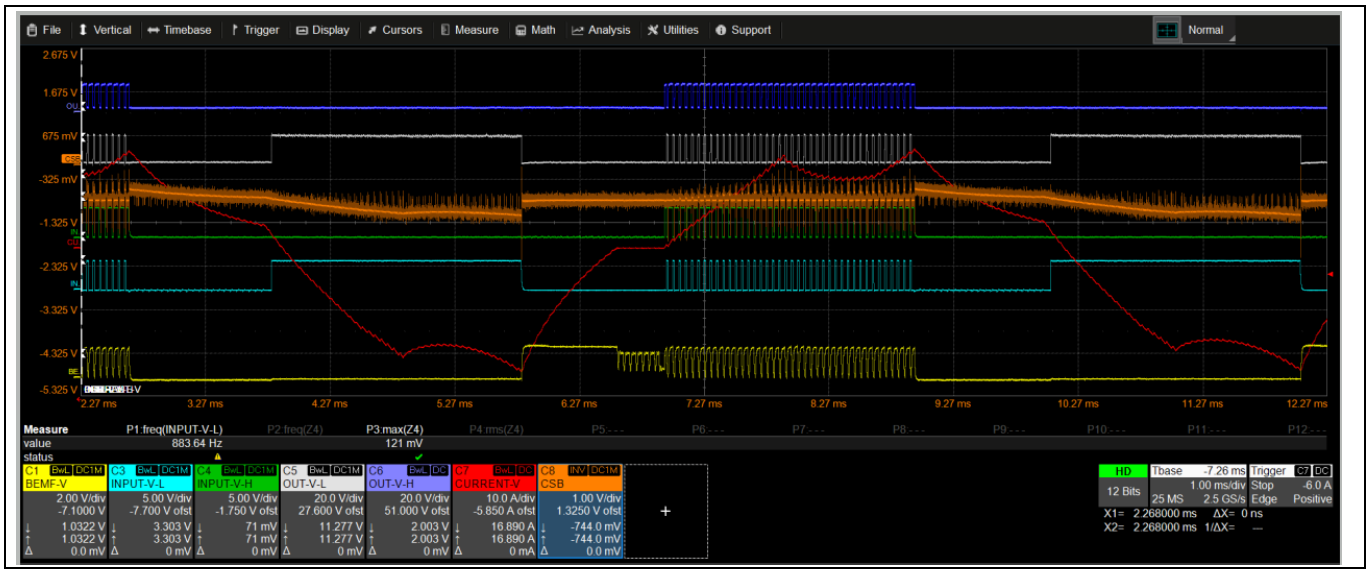

Figure 42 BEMF_V (yellow), INPUT_V_L (cyan), INPUT_V_H (green), V_{GS_LS} (gray), V_{GS_HS} (blue), $I_{PHASE\_CURRETN}$ (red), I_{PHASE_B} (orange) (signals after the internal amplifier)

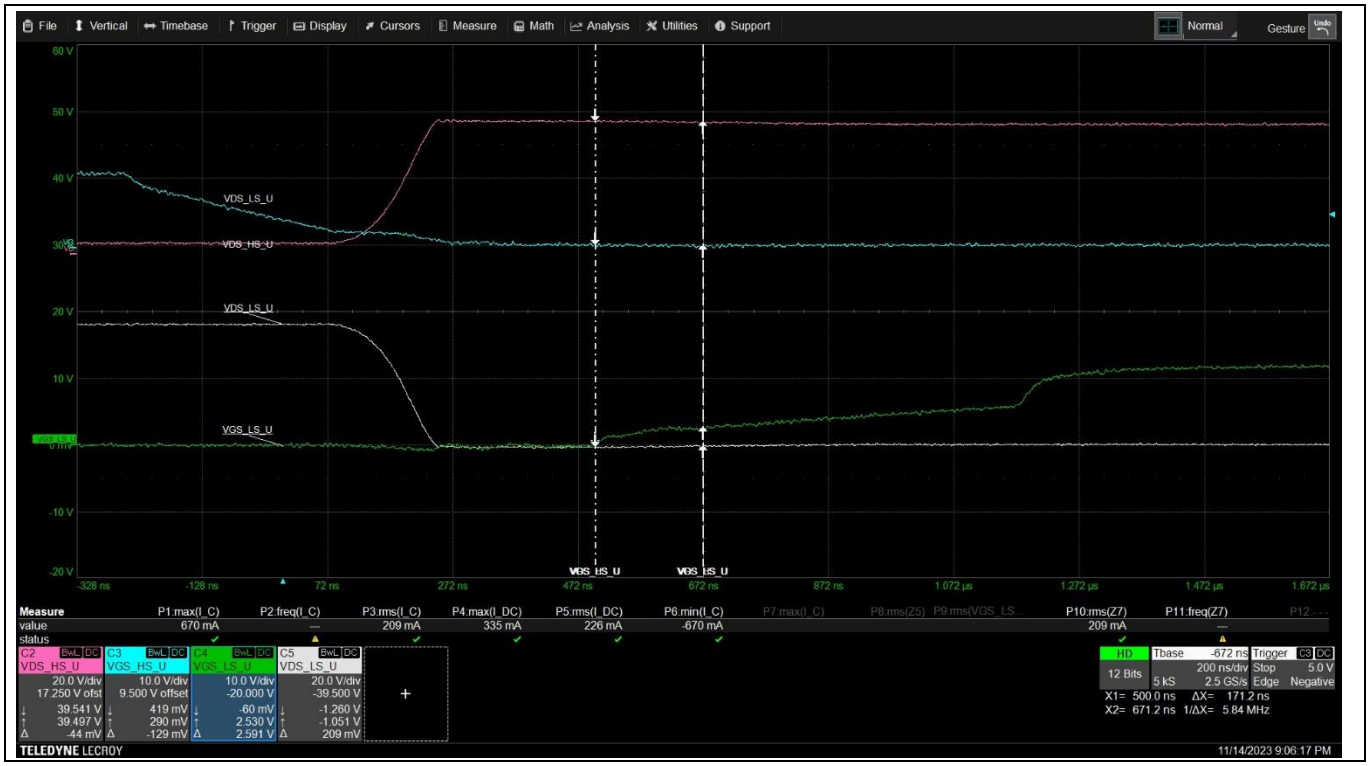

Figure 43 **Drive 1 duration $V_{DS\_HS\_U}$ (red), $V_{GS\_HS\_U}$ (cyan), $V_{DS\_LS\_U}$ (gray), and $V_{GS\_LS\_U}$ (green)**

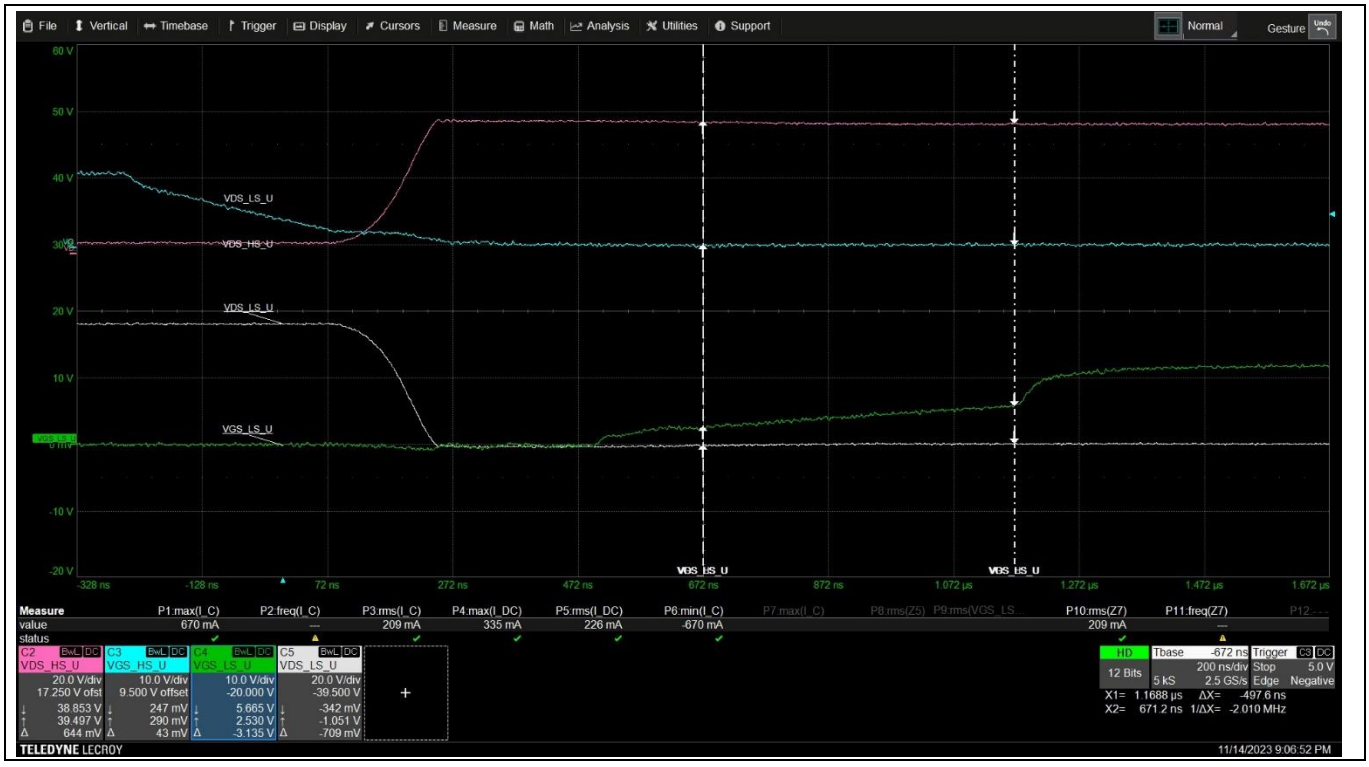

Figure 44 **Drive 2 duration $V_{DS\_HS\_U}$ (red), $V_{GS\_HS\_U}$ (cyan), $V_{DS\_LS\_U}$ (gray), and $V_{GS\_LS\_U}$ (green)**

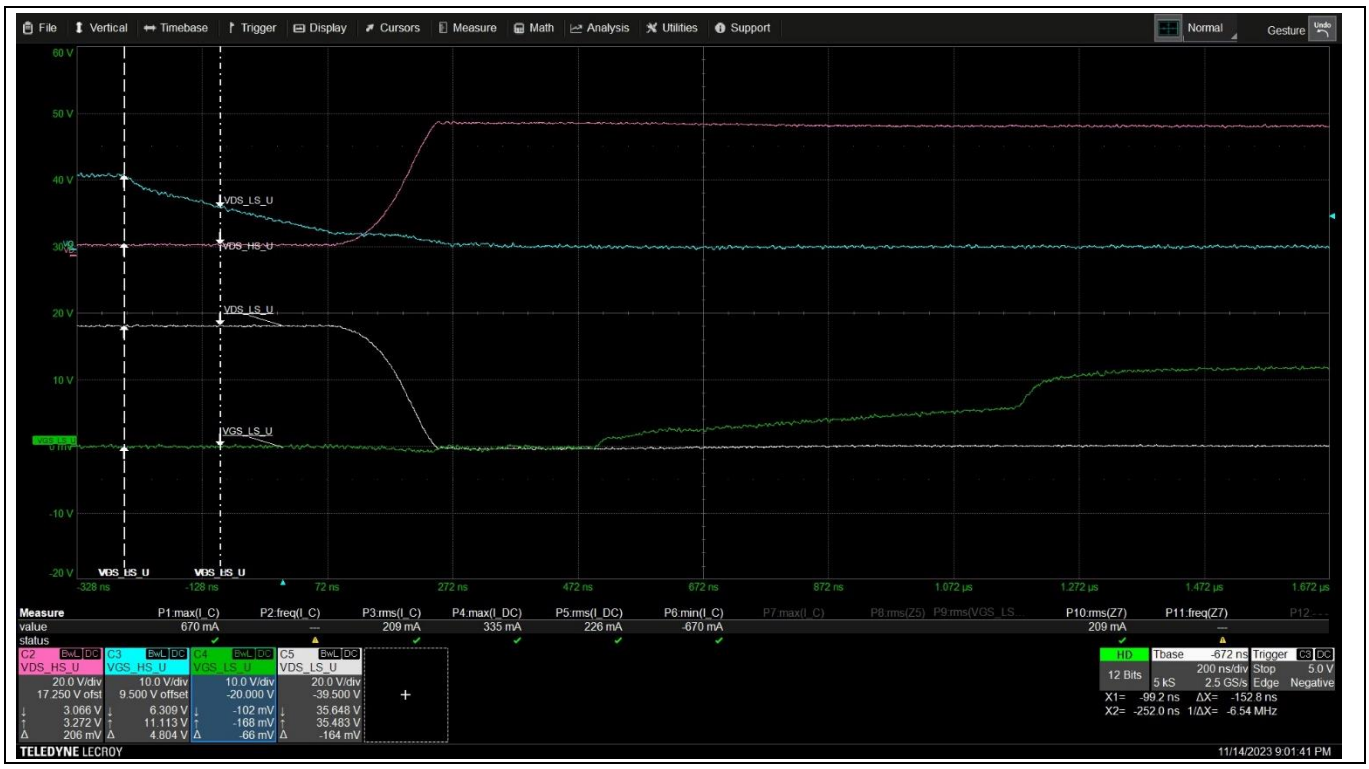

Figure 45 Drive 3 duration $V_{DS\_HS\_U}$ (red), $V_{GS\_HS\_U}$ (cyan), $V_{DS\_LS\_U}$ (gray), and $V_{GS\_LS\_U}$ (green)

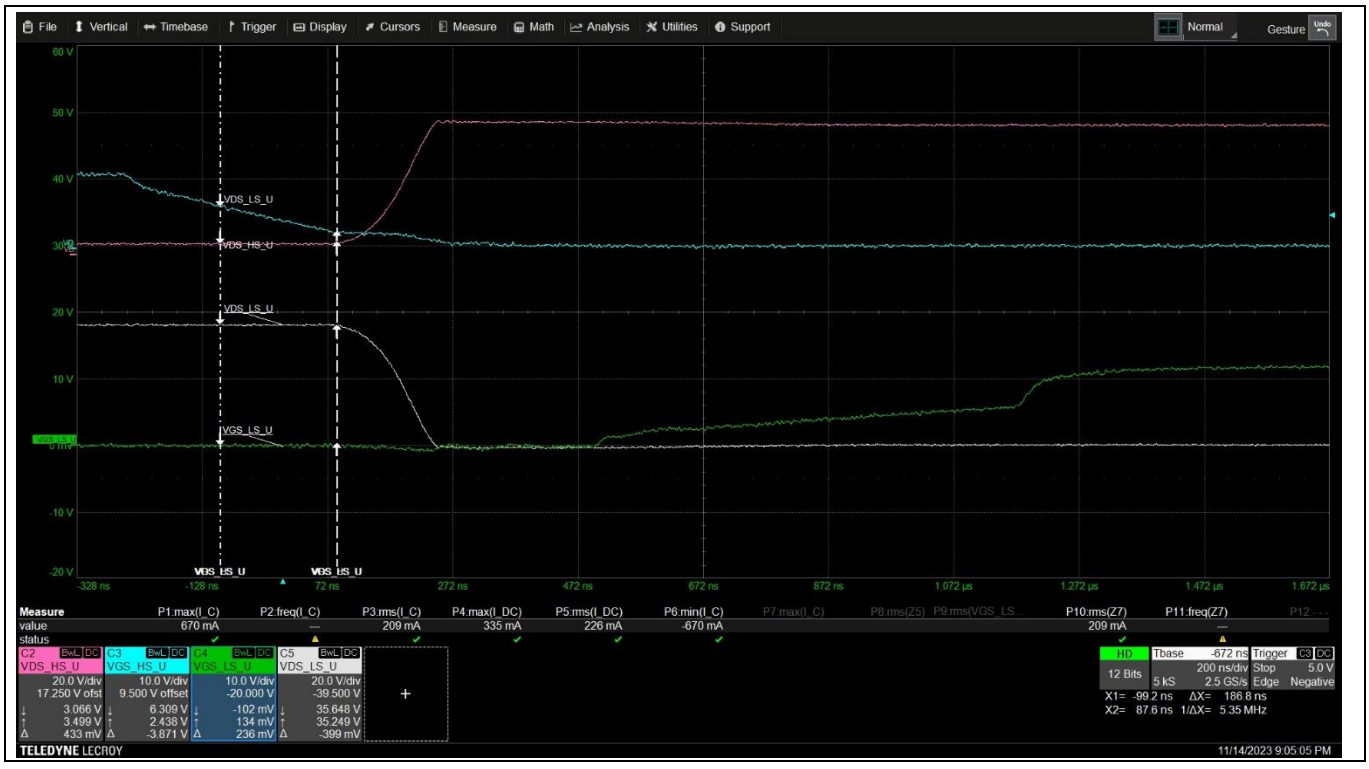

Figure 46 Drive 4 duration $V_{DS\_HS\_U}$ (red), $V_{GS\_HS\_U}$ (cyan), $V_{DS\_LS\_U}$ (gray), and $V_{GS\_LS\_U}$ (green)

References

[1] Infineon Technologies AG: *MOTIX™ 6EDL7141 datasheet*; Available online

[2] Infineon Technologies AG: *OptiMOS™ BSC012N06NS power MOSFET datasheet*; Available online

Revision history

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