User guide to BGT24LTR22

XENSIV™ 24 GHz radar sensor

About this document

Scope and purpose

This user guide offers a detailed exploration of the BGT24LTR22, Infineon's highly integrated multichannel 24 GHz radar transceiver chip. The document provides a thorough examination of the functional components of each circuit block, as well as measurement data for all building blocks across various temperatures. Additionally, it includes a detailed description of all SPI registers, enabling users to effectively configure and control the device.

Intended audience

The intended audience for this document are design engineers, technicians, and developers of electronic systems, working with Infineon’s XENSIV™ 24 GHz radar sensors.

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1 Introduction

The last decade has seen tremendous advances in silicon-based integrated circuits (ICs) for radar applications. Monolithic microwave integrated circuits (MMICs) operating in the 24 GHz industrial, scientific and medical (ISM) band are widely deployed in the market today for several automotive advanced driver assistance systems (ADAS) applications such as blind spot detection (BSD), lane change assist (LCA) and rear cross traffic alert (RCTA). However, the adaptation of radar technology beyond automotive applications has gained huge momentum. Many emerging industrial and consumer applications have adapted radar technology in recent years due to the numerous benefits offered by this technology.

Recently there has been a growing interest in mm-wave frequencies higher than 50 GHz for radar applications (e.g., 56 to 66 GHz, 76 to 71 GHz and above 100 GHz). This is mainly driven by the availability of higher bandwidth at these frequencies, leading to better target detection by the radar, and smaller antenna and MMIC sizes. As devices operating in such mm-wave frequency bands begin to find space in more automotive and industrial applications, the 24 GHz ISM band remains a lucrative option for several evolving low-cost and low-power industrial and consumer applications. The advantages offered by the mm-wave radar technology above 50 GHz, though attractive, come at a high price and design complexity, and it is extremely challenging to adapt them to price- and power-sensitive applications. Also, worldwide frequency regulations are yet to be harmonized for mm-wave radar applications. This makes 24 GHz technology-based radar sensors preferable to their mm-wave counterparts.

Apart from the well-established ADAS automotive segment a vast majority of industrial and consumer applications such as motion detectors, door openers, surveillance systems, unmanned aerial vehicles (UAVs), contactless vital-sensing and simple gesture-recognition systems are increasingly finding space for 24 GHz radar solutions due to their simplicity [6]. Also evolving automotive comfort applications such as hands-free trunk opening and in-cabin lighting, and safety applications such as child presence detection are finding the 24 GHz solutions easily deployable in terms of cost and power consumption requirements. The 24 GHz radar band remains attractive mainly for the following reasons:

- Ability to cover longer distance than mm-wave frequency radar due to lower atmospheric propagation loss
- Lower radome and PCB interconnect losses
- Lower impact of PCB tolerances on sensor performance
- Cheaper PCB material
- ISM band leads to almost worldwide harmonized operation without any major regulatory concerns

The feasibility of 24 GHz radar for several automotive, industrial and consumer applications has led to an increasing demand for highly integrated, low-power, low-noise and small form-factor MMICs in the 24 GHz ISM band. Simple power-efficient 24 GHz Doppler or frequency-shift keying (FSK) radar systems fulfill many application requirements in the industrial and consumer segment, making them highly attractive for low-power price-sensitive application scenarios. Though mm-wave frequency (above 50 GHz) based multichannel frequency-modulated continuous wave (FMCW) radar offers a much better target detection in terms of resolution and accuracy, such systems suffer from high power consumption and intensive computation requirements, leading to expensive CPUs and higher system cost. Multichannel FMCW narrowband radar implemented at the 24 GHz ISM band has been highly successful in mid- to long-range applications in the automotive radar segment for several decades, and the same benefits are now being extended to many industrial and consumer applications with highly integrated and power-efficient MMIC solutions such as the BGT24LTR22.

2 BGT24LTR22 MMIC

This user guide provides a detailed description of Infineon's next-generation, low-power, highly integrated 24 GHz radar transceiver MMIC BGT24LTR22, designed for industrial radar applications. The chip consists of two transmitters and two receivers with an integrated analog baseband (ABB) for IF signal conditioning designed in Infineon's SiGe:C BiCMOS technology B11HFC. The IC is designed for short- to medium-range low-power sensing applications. The major building blocks of the transceiver are described in detail, and its RF and DC performance as measured on the Infineon evaluation board is provided. A complete description of all the SPI register settings to communicate with the chip is also given.

2.1 Key features

- Highly integrated 24 GHz radar front-end MMIC in SiGe:C BiCMOS technology for low-power applications
- Fully integrated low phase-noise (PN) voltage-controlled oscillator (VCO)
  - -85 dBc/Hz PN at 100 kHz offset
- Highly integrated frequency divider
  - High-frequency output – /16 – for external hardware PLL
  - Several low-frequency outputs – for software PLL
- Two single-ended transmit (TX) channels with configurable output power
  - Up to +5 dBm typical output power
  - Output power dynamic range greater than 20 dB
  - TX on/off isolation: min. 40 dB
- Two single-ended receive (RX) channels
  - Typical maximum voltage conversion gain (CG) 26 dB, with typical single-sideband noise figure (NFSSB) 8 dB
  - Direct conversion quadrature mixer with differential outputs
- Integrated ABB section for FMCW radar application
  - High-pass filter (HPF) with tunable cut-off frequencies (20 kHz, 50 kHz, 80 kHz and 100 kHz) and gain (18 dB or 30 dB)
  - Variable-gain amplifiers with up to 30 dB gain (5 dB programmable steps)
  - Anti-aliasing filter (AAF) with 600 kHz cut-off frequency
- Integrated ABB bypass mode for Doppler applications
  - DC-coupled mixer output with 3 dB bandwidth above 100 MHz
- Excellent on-chip TX-to-RX isolation above 40 dB
- Integrated PTAT-based tuning voltage generator for Doppler radar applications in the ISM band
- Integrated power and temperature sensors
- One chip supporting all modulation schemes (Doppler, FSK and FMCW)
- Single supply voltage 1.5 V
- Multimode operation with scalable architecture
  - Master mode (single device): 1TX to 1RX, 1TX to 2RX, 2TX to 2RX
  - Slave mode (multiple devices): built-in cascade feature allowing one device to combine with several other devices with a shared LO, and to expand the number of TX and RX for beamforming applications – e.g., 1TX to 4RX and 2TX to 4RX
- SPI transceiver

- Dedicated hardware pin (TX_EN) for fast on/off switching of the transmitters

2.2 Target applications

- Smart lighting (indoor and outdoor)
- Collision avoidance systems for commercial agricultural vehicles (CAVs)
- Industrial automation (robotics)
- Drone landing assist and collision avoidance
- Traffic monitoring
- Security systems (surveillance and alarm)
- Simple presence detection for smart home appliances
- Automatic door openers
- Simple motion detection and speed measurement with ranging
- Vital sensing
- Simple gesture recognition
- Touchless switches

3 Package and pin description

Figure 1 shows the top view of the BGT24LTR22 MMIC with the pin descriptions. The device is housed in a small, embedded wafer-level ball grid array (eWLB) 52-pin package of 3.63 mm x 3.63 mm dimensions.

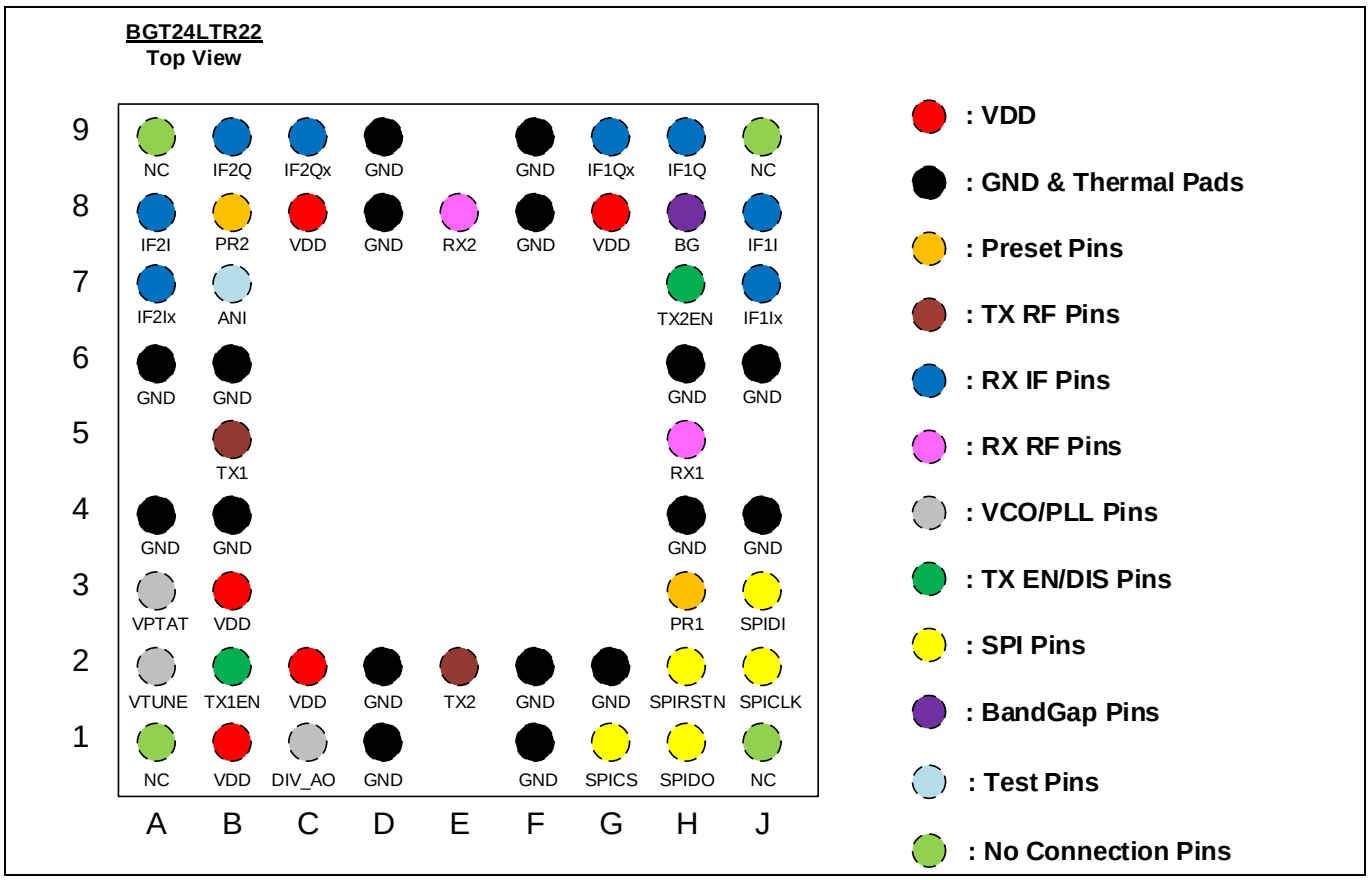


Figure 1 BGT24LTR22 pin-out (top view)

Table 1 Pin definitions and functions

Pin number	Name	Function
A1, A9, J1, J9	NC	No connection – used to route inner row pins to exterior of the MMIC (e.g., SPIRSTN, TX1EN, BG and PR2)
B1, B3, C2, C8, G8	VDD	1.5 V DC supply voltage – pin B3 and G8 can be left floating for area constraint layout
H5	RX1	RF input – receiver 1 – can be left floating when not used
E8	RX2	RF input – receiver 2 – can be left floating when not used
E2	TX2	Bidirectional RF I/O RF output – transmitter 2/LO input 2 – can be left floating when not used
B5	TX1	Bidirectional RF I/O RF output – transmitter 1/LO input 1 – can be left floating when not used
J8, J7	IF1I, IF1Ix	Complementary in-phase downconverter IF output – receiver 1 – DC coupled (both bypass and ABB mode)
H9, G9	IF1Q, IF1Qx	Complementary quadrature phase downconverter IF output – receiver 1 – DC coupled (both bypass and ABB mode)

Pin number	Name	Function
A8, A7	IF2I, IF2Ix	Complementary in-phase downconverter IF output – receiver 2 – DC coupled (both bypass and ABB mode)
B9, C9	IF2Q, IF2Qx	Complementary quadrature phase downconverter IF output – receiver 2 – DC coupled (both bypass and ABB mode)
A4, A6, B4, B6, D1, D2, D8, D9, F1, F2, F8, F9, G2*, H4, H6, J4, J6	GND	Ground
H3	PR1	Mode select – pin 1 – must be tied to ground for SPI programming
B8	PR2	Mode select – pin 2 – must be tied to ground for SPI programming
C1	DIV_AO	Frequency divider output – DC coupled. External decoupling capacitor must be added when necessary.
B2	TX1EN	Enable transmitter 1 – hardware pin to enable the transmitter 1. Must be tied to ground and pulled up only when transmitting.
H7	TX2EN	Enable transmitter 2 – hardware pin to enable the transmitter 2. Must be tied to ground and pulled up only when transmitting.
H8	BG	Bandgap voltage output – connect a 100 nF capacitor to ground (mandatory). Place the capacitor as close to the device as possible.
A2	VTUNE	VCO frequency tuning input
A3	VPTAT	PTAT voltage source output. Can be left floating when not used.
G1	SPICS	SPI chip select (SPICS_n_i)
H1	SPIDO	SPI data out (SPIDO_o)
H2	SPIRSTN	SPI reset pin – connect a 100 nF capacitor to ground. Place the capacitor as close to the device as possible.
J2	SPICLK	SPI clock (SPICLK_i)
J3	SPIDI	SPI data in (SPIDO_i)
B7	ANI	Analog input for testing – only for internal use. Must be left floating.

Note:

- It is mandatory to connect pin G2 to ground for SPI programming
- Often there are questions about whether it is necessary to connect all the VDD pins on the device. The simple answer is, it is recommended to connect all VDD pins if the layout allows that to avoid excessive voltage drop at one particular node of the device. Should the layout not allow this easily, it is safe to leave only the B3 and G8 pins open. All VDD pins are connected internally, inside the MMIC
- Pins H3 and B8, corresponding to PR1 and PR2 respectively, must always be connected to ground to enable programming via SPI. Typically, this can be implemented with a small line close to the MMIC package. It is not necessary to have any pull-down resistor when connecting these pins to ground. The device cannot be programmed if this pin is left open or pulled to VDD
- Pins B2 and H7, corresponding to TX1EN and TX2EN respectively, must always be connected to ground once the device is enabled. It must be pulled to VDD only when a signal transmission is desired. It is not necessary to have any pull-up or pull-down resistor at these pins

- Pin H8 corresponding to BG must be connected with a 100 nF shunt capacitor. This is mandatory, to achieve the best noise figure performance from the chip. The shunt capacitor must be placed as close to the chip as possible
- Pin H2 corresponding to SPIRSTN must be connected with a 100 nF shunt capacitor. This is mandatory to prevent any unwanted reset of the SPI block. The shunt capacitor must be placed as close to the chip as possible

4 MMIC functional description and electrical characteristics

The BGT24LTR22 device is Infineon's next-generation multichannel, multimode highly integrated 24 GHz radar transceiver with a scalable architecture operating from 24.0 GHz up to 24.25 GHz. Figure 2 shows the block diagram of the transceiver.

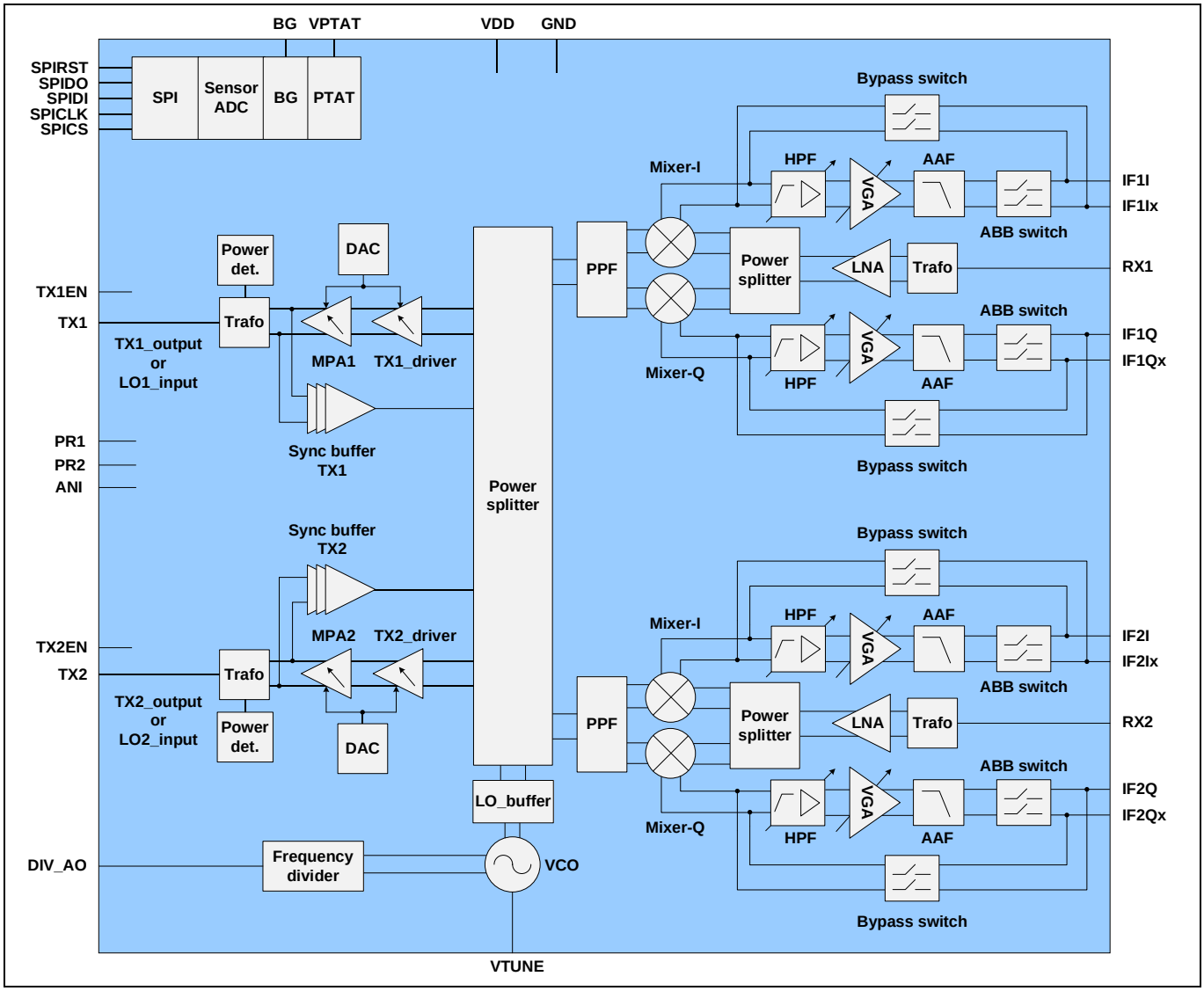


Figure 2 BGT24LTR22 block diagram

The high-frequency signal is generated by a low-PN fundamental-frequency VCO. A network of buffer amplifiers is then used to distribute the fully differential local oscillator (LO) signal efficiently to the TX and RX sections of the chip. A frequency divider circuit is used to monitor the transmitted signal from the VCO, and in combination with an external PLL or MCU/digital-to-analog converter (DAC) is used for frequency locking and FMCW ramp generation. An inbuilt programmable proportional to absolute temperature (PTAT) voltage source is also available to generate a temperature-compensated voltage for the VCO tuning port for simple fixed-frequency CW (Doppler) applications inside the ISM band.

The transmit section consists of a combination of a driver and a medium-power amplifier (MPA). The gain of these blocks is controlled by an integrated DAC. Integrated power detectors allow monitoring of the transmitted power. The bidirectional nature of the transmit section enables synchronization of the MMIC with an external LO signal when used in a cascaded multichannel beamforming system.

The chip features two quadrature receiver stages. Each receive section uses a low-noise amplifier (LNA) in front of a quadrature homodyne down conversion mixer. Derived from the internal VCO signal, an RC polyphase filter (PPF) generates the LO signals for the quadrature mixer. The device also integrates a programmable ABB section with tunable bandpass characteristics for FMCW radar application. The entire device is controlled via a serial-to-peripheral interface (SPI).

The device is manufactured in Infineon's B11HFC BiCMOS technology, offering a cut-off frequency higher than 300 GHz. The MMIC is housed in Infineon's plastic eWLB package, which can be processed in standard SMT flow.

The following sections describe the function of each building block in detail, with measurement results.

4.1 VCO section

Figure 3 shows the block diagram of the high-frequency signal-generation circuitry. The core signal-generation unit consists of a low-PN, free-running fundamental-frequency VCO. An LO buffer amplifier isolates the VCO core from the rest of the circuit, and also provides sufficient amplification for efficient signal distribution to the TX and RX sections of the chip. A portion of the VCO signal is provided to a prescaler circuit, which allows for external frequency control and monitoring. The output frequency of the VCO is controlled by a tuning voltage applied at the VTUNE pin (A2) of the packaged chip. Based on the application scenario, the external frequency control and stabilization can be implemented either by a standalone hardware PLL chip or an MCU/DAC-based scheme, as detailed in Section 4.3.

For applications requiring fixed frequencies, such as Doppler radar, exact frequency control in the 24 GHz ISM band is not necessary in most cases. If we assume the transmit frequency to be at the lower edge of the band but, it is actually at the upper edge, the introduced error is only 0.8 percent. However, it is necessary that the TX signal stays inside the ISM band under all conditions. For such applications, there is an inbuilt PTAT voltage source, the output of which can be connected to the VTUNE pin (A2) to generate a temperature-stable VCO output frequency. This analog control voltage (VPTAT) forces the VCO into the opposite direction in case of temperature drift. The voltage output of the PTAT block can be fine-tuned digitally over the SPI by two independently configurable 8-bit DACs. This can also be done adaptively by monitoring the low-frequency output from the frequency divider each time and readjusting the PTAT voltage. This avoids the need for an external tuning voltage source in the radar system. The PTAT block can only generate a fixed temperature-compensated voltage and is not capable of generating any FMCW ramps.

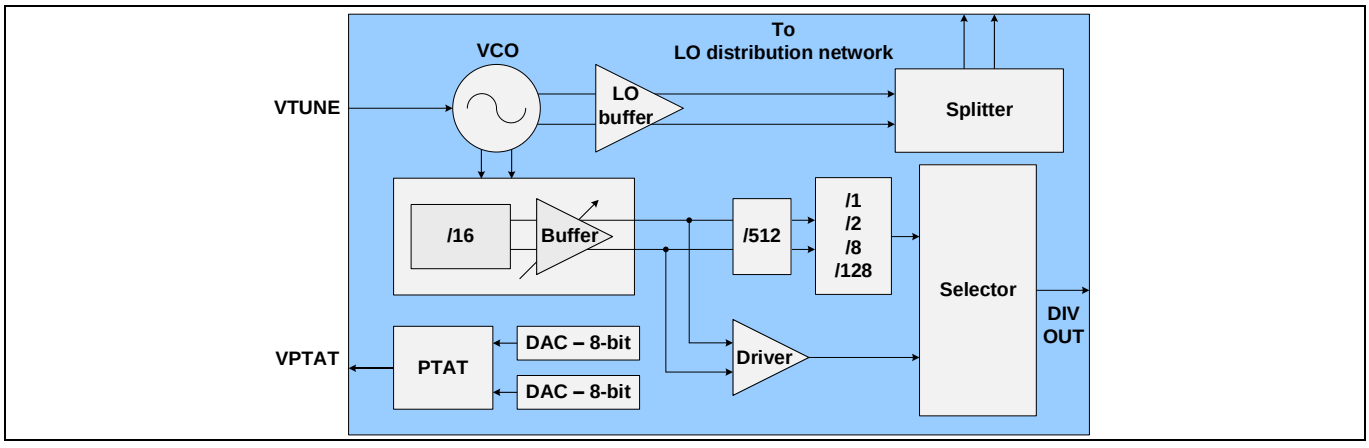


Figure 3 VCO section block diagram

Figure 4 shows the tuning characteristics of the VCO. For this measurement, the tuning voltage was applied via the VTUNE pin (A2) from an external voltage source.

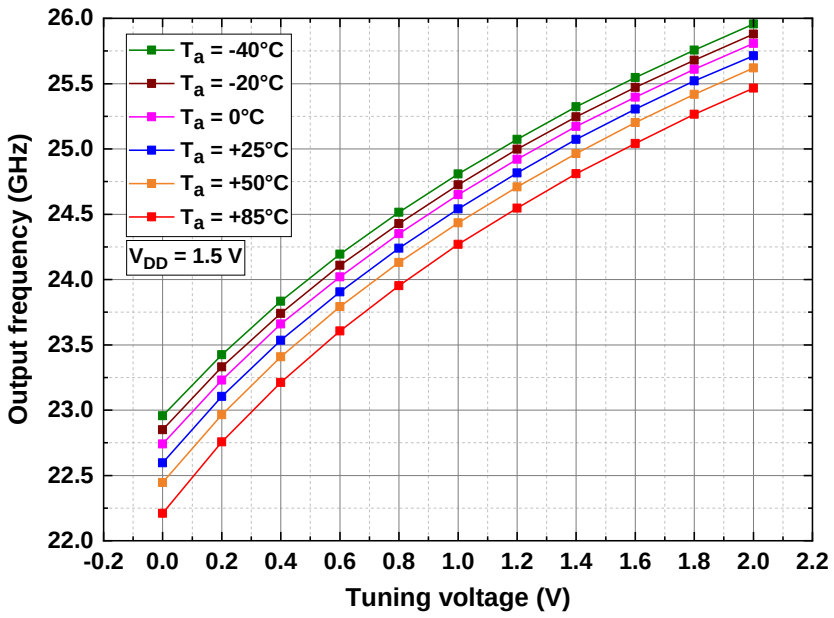


Figure 4 VCO frequency vs. tuning voltage and temperature

For FMCW radar applications, the device is generally operated within a very narrow ISM band from 24.0 GHz to 24.25 GHz. In such cases, it is interesting to understand the linearity of the VCO within the ISM band of operation. Figure 5 shows the frequency response of the VCO inside the ISM band over temperature. The VCO remains fairly linear within the 24.0 to 24.250 GHz band.

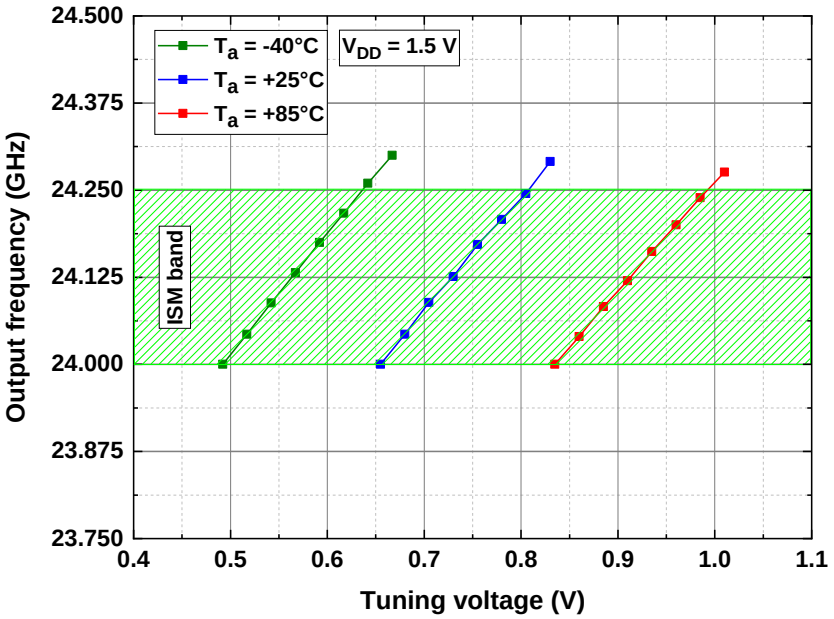


Figure 5 VCO frequency vs. tuning voltage and temperature in the ISM band

All BGT24LTR22 MMICs are internally fused for ISM band operation in production. This means the output from the PTAT voltage source when connected to the VTUNE pin on power-up will automatically put the VCO in the ISM band. In order to implement this, the factory settings for ISM band operation must be loaded into the PTAT block via the SPI before enabling the transmitters by the TXENx pins. Table 4 lists the registers to control the PTAT voltage source.

Table 2 SPI registers for PTAT voltage source configuration

SPI register	Function
Register 11	User-configurable register for the PTAT voltage source Set_VPTAT_Res [7:0] – user-configurable Set_VPTAT_Cur [15:8] – user-configurable
Register 55	Factory-calibrated settings for the PTAT voltage source for ISM band operation Set_VPTAT_Res [7:0] – factory set via e-fuses Set_VPTAT_Cur [15:8] – factory set via e-fuses
Register 32	Bit 15 of register 32 is used to select either register 11 or register 55 for the PTAT voltage source 0 = register 11 1 = register 55

Figure 6 shows the frequency behavior of the VCO when the tuning voltage is applied via the internal PTAT voltage source. It is recommended to connect a shunt capacitor of more than 1 µF very close to the VTUNE pin (A2) of the chip when using this method to control the VCO frequency. This reduces the noise generated by the voltage source. For this measurement, the factory-calibrated settings for the PTAT voltage source were used (register 55).

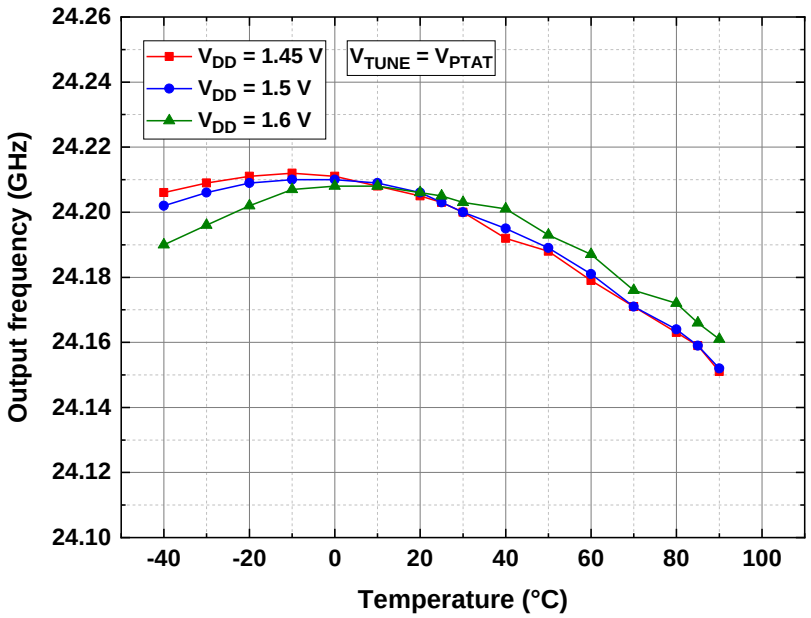


Figure 6 VCO frequency vs. temperature and supply voltage for $V_{TUNE} = V_{PTAT}$

The variation of the PTAT output voltage with temperature is shown in Figure 7.

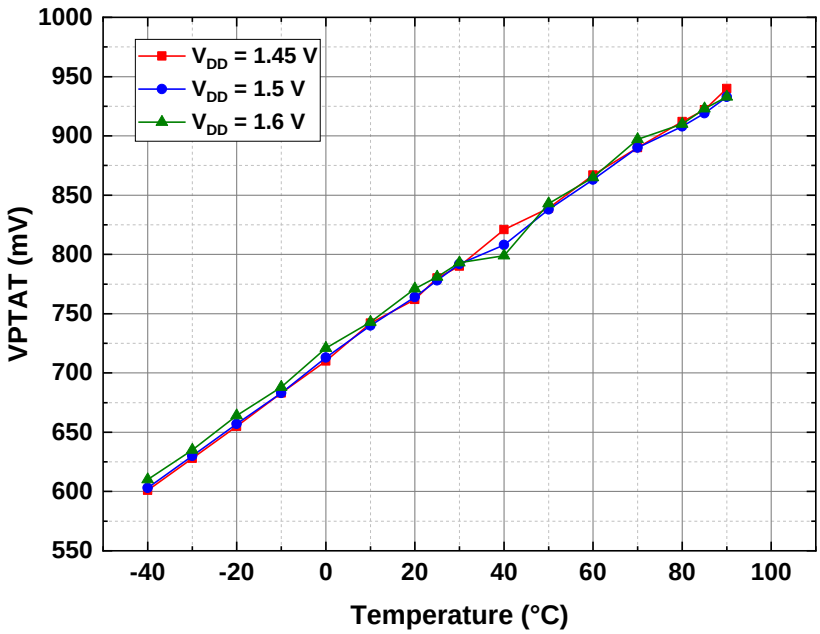


Figure 7 Voltage generated by the PTAT source vs. temperature and supply

This section shows the measured PN and amplitude noise (AN) of the BGT24LTR22 chip. PN is one of the most important parameters for FMCW radar systems. The ability of the MMIC to transmit a signal with a very low PN determines its ability to detect targets successfully at greater distances. A higher PN leads to an increased system noise floor, which can easily impact the detection of targets with low radar cross-section (RCS) at longer distances from the radar. Strong targets in the vicinity of weaker targets can also completely blind the radar to the weak targets. Therefore, it is very important for FMCW radar systems to have a good PN performance. Figure 8 shows the measured PN and AN of the device at different offset frequencies at room temperature. For this measurement, the voltage at the VTUNE pin (A2) was provided by the internal PTAT voltage source with a 22 µF shunt capacitor.

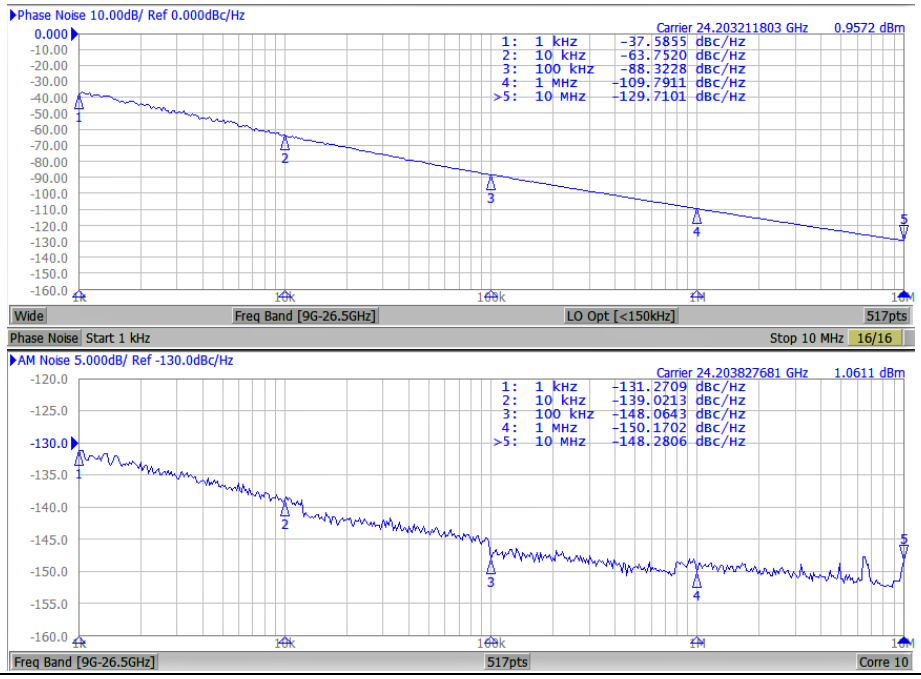


Figure 8 PN and AN at T_a = +25°C and V_{DD} = 1.5 V, V_{TUNE} = V_{PTAT}

Figure 9 shows the variation of VCO PN over temperature at different offset frequencies.

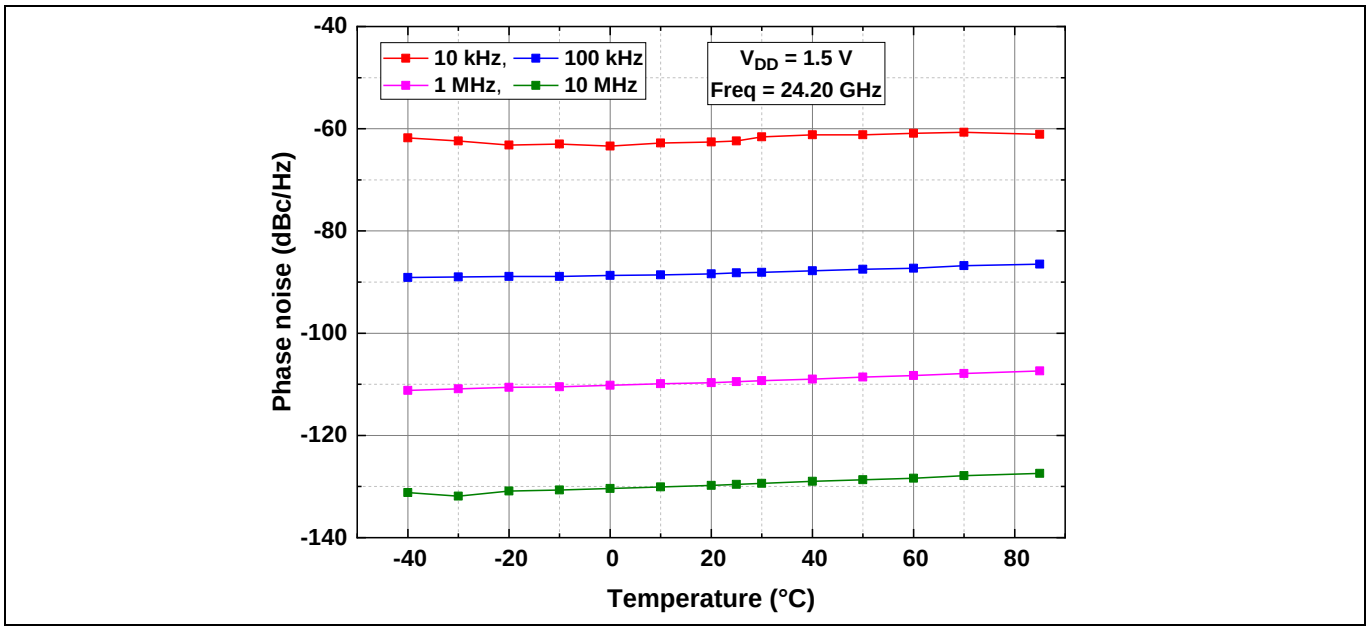


Figure 9 VCO PN vs. temperature at different offset frequencies, V_{TUNE} = V_{PTAT}

The VCO shows a PN lower than -88 dBc/Hz at 100 kHz offset and AN lower than -148 dBc/Hz at 100 kHz offset respectively. For FMCW radar applications, the PN will be finally dependent on parameters such as loop filter bandwidth, charge pump current and other settings of the external frequency control circuit.

4.2 Prescaler/frequency dividers

For frequency stabilization and FMCW ramp generation, the chip includes a frequency divider block with several division factors. The 24 GHz signal generated by the VCO is divided to a low-frequency signal by this frequency divider block. Based on the frequency control mechanism used, the user is allowed to select from five different divider ratios. The first prescaler divides the VCO frequency by 16, and the other prescaler further reduces the output of the first one by several selectable division factors. Figure 10 shows a simplified block diagram of the frequency divider circuit. The selected divider output is available via the DIV_AO pin (C1).

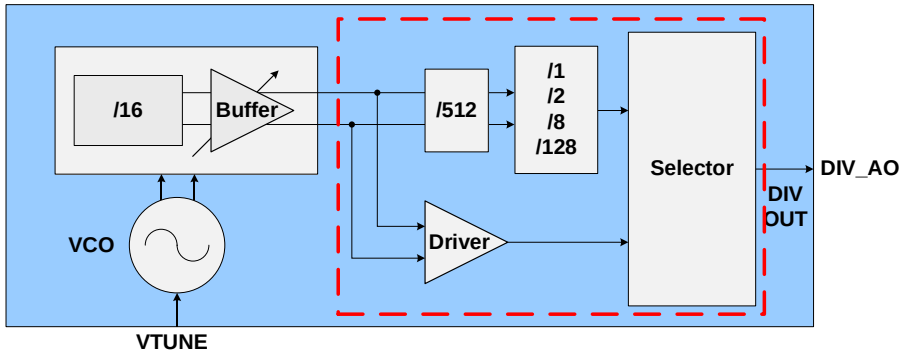


Figure 10 Block diagram: prescaler (inside red dashed line)

4.2.1 Divide-by-16 prescaler

This first prescaler divides the VCO's frequency of oscillation by a factor of 16. So, at a given VCO frequency of 24 GHz, the prescaler's output frequency is 1.5 GHz. This is a convenient frequency to feed into external RF-PLL ICs. A driver amplifier in the divider circuit ensures that the divider provides sufficient output power to drive the external RF-PLL chip under all operating conditions. Figure 11 shows the output power of the 1:16 divider vs. temperature and supply voltage over the entire tuning range of the VCO. When using the 1:16 frequency divider, no special matching structures are necessary. It is sufficient to connect the DIV_AO pin (C1) to the RF input of the PLL directly with a DC blocking capacitor and a standard 50 Ω transmission line.

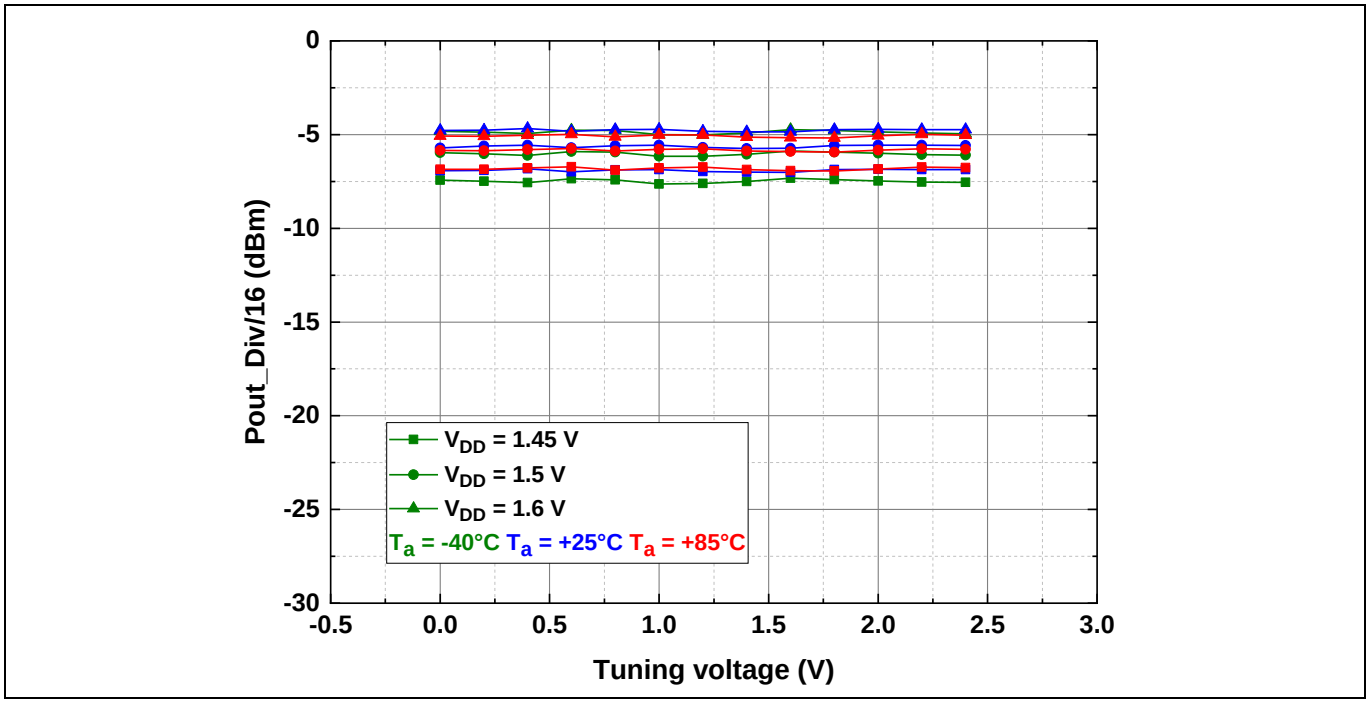


Figure 11 1:16 prescaler output power vs. tuning voltage, temperature and supply voltage

4.2.2 Low-frequency prescalers

For systems that do not use an external hardware RF-PLL for frequency stabilization and chirp generation, the BGT24LTR22 provides four different low-frequency outputs. To achieve this, the output of the 1:16 prescaler is connected to a frequency divider network with several division factors, as shown in Figure 10. The desired division factor is enabled by a 2-bit DAC (SEL_DIVIDER). Table 3 lists the different divider output frequencies for an RF frequency of 24.0 GHz and the corresponding bit settings to enable them.

Table 3 Low-frequency prescaler and selectable divider outputs

Divider setting (SEL_DIVIDER)	Dividing factor	Low-frequency output at DIV_AO (RF freq. = 24.00 GHz)
00	2^13	2.93 MHz
01	2^14	1.46 MHz
10	2^16	366 kHz
11	2^20	22.89 kHz

These low-frequency divider output signals can be monitored via a microcontroller's timer unit (e.g., compare capture unit (CCU)), for example, and can then be used together with the microcontroller's DAC or PWM output to create a software loop to control the VCO's output frequency.

Note: The prescaler may be disabled via the SPI when not in use. Only one prescaler output is selectable at a given time. The output of the prescaler is DC-coupled and therefore requires a DC block when connecting to a spectrum analyzer for measurements.

4.3 VCO control methods

This section provides an overview of three different methods used to control the VCO of the device.

4.3.1 VCO control using integrated PTAT voltage generator

The BGT24LTR22 features an integrated PTAT voltage source. This built-in voltage source is particularly useful in applications that demand a fixed frequency within the 24.00 to 24.250 GHz ISM band, such as Doppler radar systems. By utilizing the PTAT voltage source, it is possible to generate the necessary tuning voltage for the VCO, thereby enabling precise frequency control within the specified range.

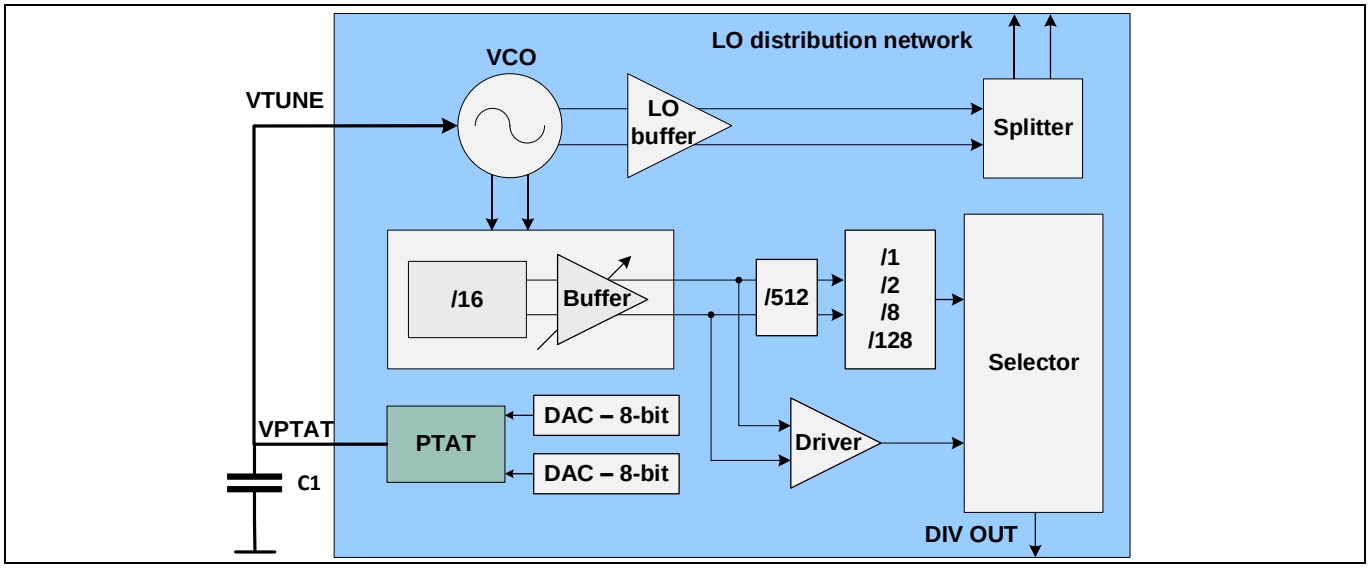


Figure 12 VCO control using the internal PTAT voltage source block diagram

The analog voltage generated by the PTAT is such that it forces the VCO frequency to change only slightly as shown in Figure 6 in case of temperature drift, thereby ensuring that the transmitted frequency remains within the specified ISM band. The output frequency can be constantly monitored via the integrated frequency divider output from the chip, and the PTAT voltage source can be easily fine-tuned by programming a pair of integrated 8-bit DACs. Capacitor C1 (typical value greater than 1 µF) is used to filter the noise generated by the PTAT voltage source.

In typical cases, an external DAC or a phase-locked-loop (PLL) circuit is used to generate such a tuning voltage for the VCO. However, with the introduction of such a digitally controlled temperature-compensated voltage source inside the MMIC, the BGT24LTR22 eliminates the need for an external voltage source for such simple Doppler applications, thereby significantly improving the entire frequency control process and also reducing system BOM cost. (No external PLL or DAC is required for tuning voltage generation for Doppler radar.) Each MMIC is pre-programmed in the factory with PTAT register settings for ISM band operation, which can be loaded from register 55.

4.3.2 VCO control using a hardware PLL

A PLL can be connected to the BGT24LTR22 to control the VCO, as shown in Figure 13. To implement this, the frequency divider needs to be set to a ratio of 1:16 via the SPI.

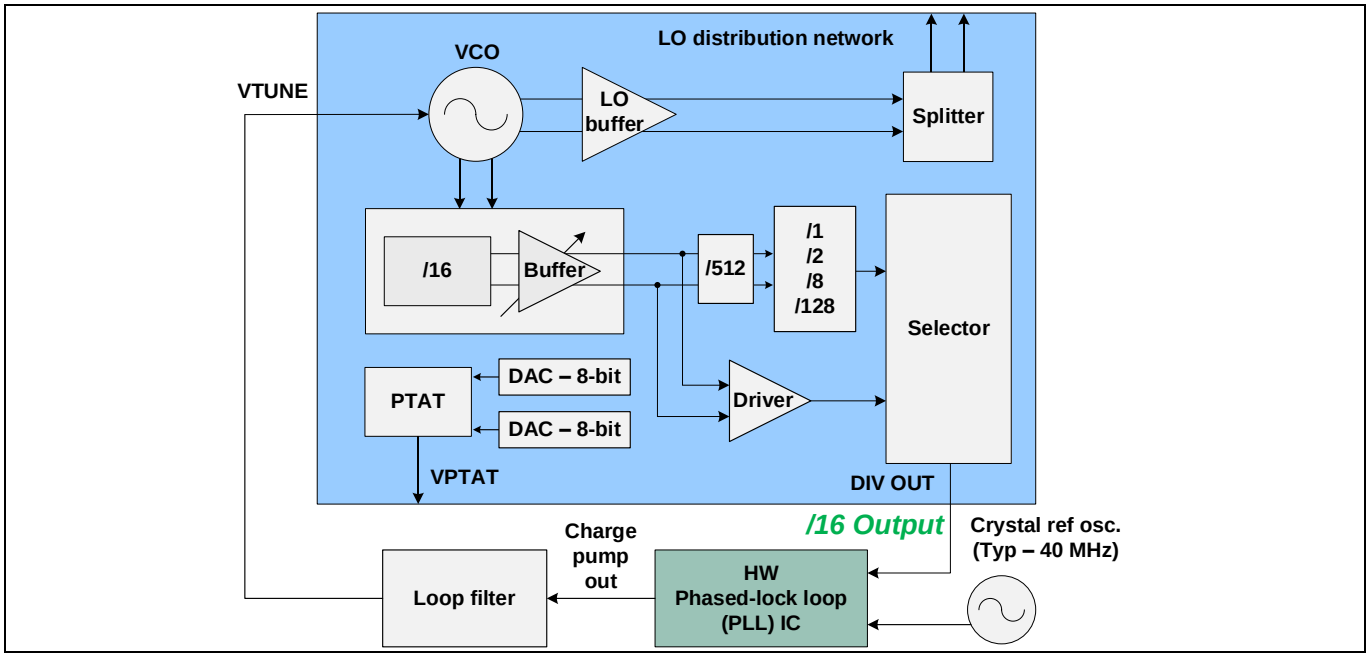


Figure 13 VCO control using a PLL block diagram

The VCO output signal gets divided by a factor of 16 (prescaler), producing a 1.5 GHz divider output signal for the PLL. In the PLL, further dividers (N-divider) are applied to the input divider signal to further reduce the frequency. The phase detector (PD) in PLL compares the N-divider output signal with the reference from a crystal oscillator to control the PLL charge pump (CP). The CP_{OUT} is converted into an analog VCO tuning signal (V_{TUNE}) via the loop filter (LF). This is connected to the tuning port of the VCO (V_{TUNE}). V_{TUNE} finally controls the VCO frequency to achieve a full signal fit between N-divider output signal and the reference signal to achieve a frequency and phase lock. The PLL can then be programmed to generate the desired FSK or FMCW ramps.

4.3.3 VCO control using a software-based open-loop concept

It is possible to control the BGT24LTR22 using a software-based open-loop concept. In this approach, a loop is needed with a voltage source and feedback, which is used to adapt the necessary frequency changes. This implementation has the advantage of reducing PCB space, BOM cost and power consumption by eliminating the HW PLL.

In this software-based open-loop concept – often known as “Software PLL” – there is no VCO phase and frequency locking to a reference signal. Frequency is measured periodically and VCO is tuned accordingly. VCO phase noise (PN) is comparable to the freewheeling VCO (best case) and not improved as in the HW PLL. However, VCO PN is less critical in very short-range radar applications, because PN in the TX, RX and LO path stays mainly correlated for short target distances, resulting in a strong reduction of residual PN in the downconverted IF signal (“range correlation effect”).

Both Doppler radar and stepped-FMCW radar can be realized with the software-based open-loop VCO adjustment/sweeping concept. System performance might be lower than a HW PLL, but is often sufficient for many applications like smart lighting or proximity detection, etc.

Figure 14 describes the implementation of such a concept. The DAC of the MCU is used to generate a tuning voltage for the VCO. V_{TUNE} is generated by the DAC for the start frequency and then filtered in the RC filter (two stages). According to the V_{TUNE} input, the VCO produces the TX/LO signal. The VCO signal is also fed into a frequency divider and gets divided by a factor of 8192. This divided signal is captured by the CCU in the MCU. The divider output signal is measured by counting the number of rising/falling (or both) edges of the MCU's master clock inside a certain number of divider output signal periods (counting gate). The measured frequency is then compared with the required start frequency (24.025 GHz/8192 = 2.9327 MHz). The difference between the measured and required frequency is then evaluated in the decision function. Depending on the result, the bit value gets adapted, and the loop starts again until the measured and desired frequency agree within a certain margin. This routine is repeated for the stop frequency as well (24.225 GHz/8192 = 2.9571 MHz).

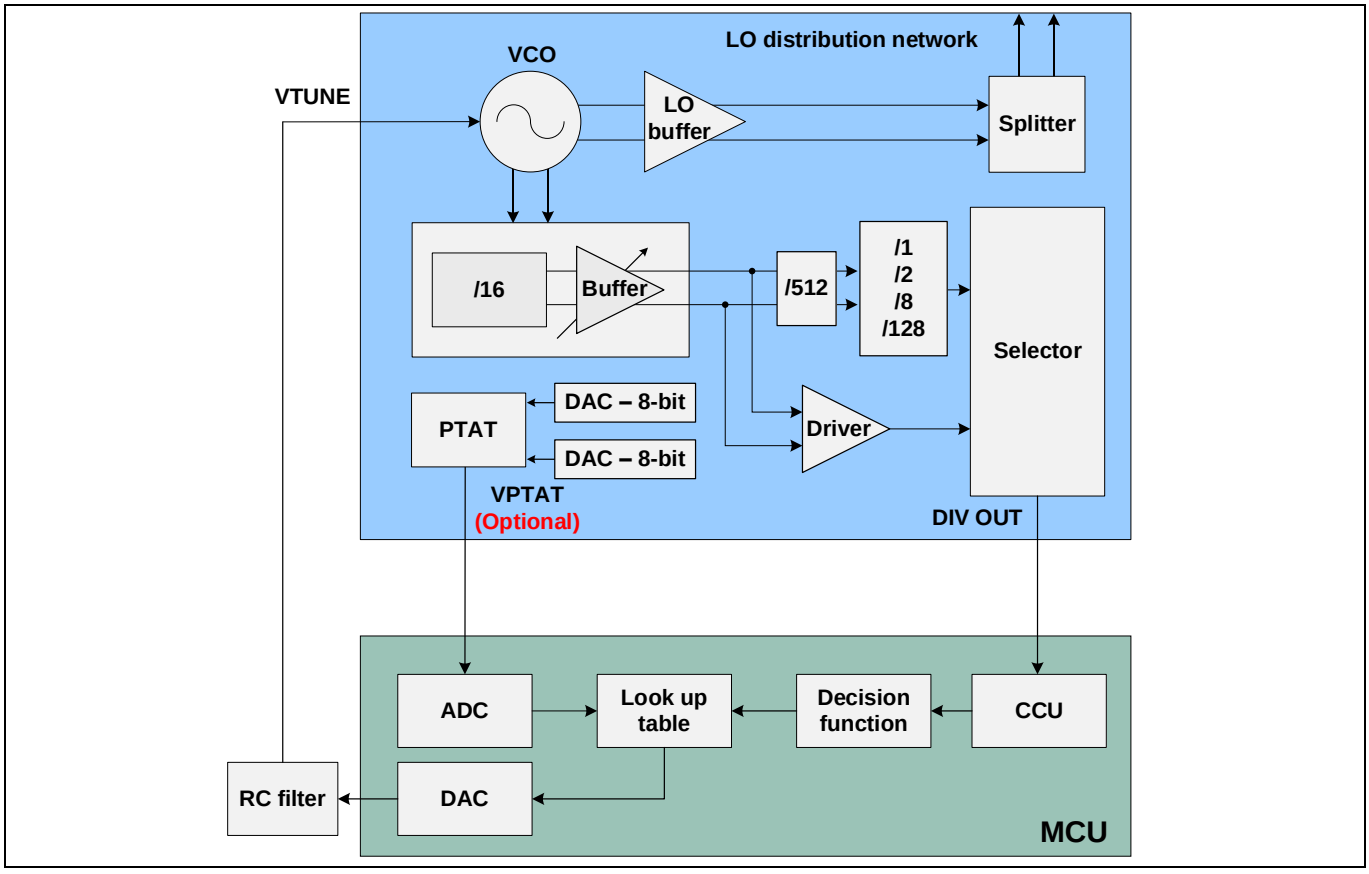


Figure 14 VCO control using a software-based open-loop concept block diagram

4.4 Transmitter section

The BGT24LTR22 transceiver consists of two identical fully differential transmitter sections with single-ended output interface. Figure 15 shows the block diagram of one such TX section. The signal from the VCO after amplification from the LO distribution network is first amplified by a driver amplifier (TX_driver). The output from the driver is further amplified by an MPA. The gain of both the amplifiers is configurable with integrated DACs. The gain of the TX_driver is controlled by a 2-bit DAC (00 – low gain, 01 – medium low gain, 10 – medium-high gain and 11 – high gain) and the MPA gain is controlled by a 4-bit DAC (0_D, 2_D…15_D). The amplified differential output signal is then converted to a single-ended signal by on-chip transformers and fed into the TX output pins of the package. Peak RF power detectors are placed at each of the MPA outputs to enable monitoring of the transmitted power. A dedicated hardware pin is available for enabling/disabling the TX unit. Each TX unit is a fully independent block, and its output power can be configured independently.

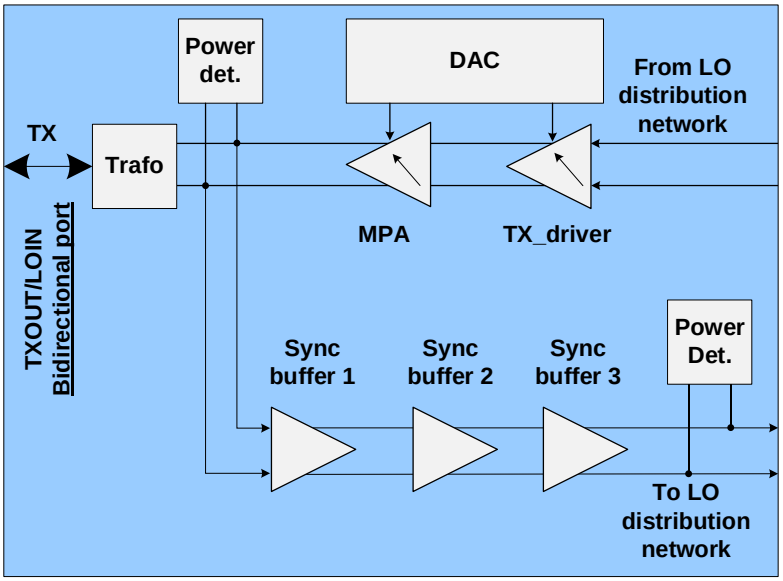


Figure 15 Transmitter section block diagram

A key feature of the BGT24LTR22 MMIC is the bidirectional nature of the TX ports. For single-chip operation, the TX ports are used to transmit the 24 GHz microwave signal to an external antenna. For radar applications that require higher angular resolutions, the bidirectional nature of the TX section enables cascading of several BGT24LTR22 MMICs together. In such applications, one MMIC acts as a master and the cascaded chips act as a slave. In a cascaded operation, the TX port of the slave device acts as the input port for the LO signal from the master chip. This enables a synchronized LO signal for all the chips in the system. The VCO, TX_driver and the MPA of all the cascaded chips must be turned off via the SPI to prevent system malfunction. For the cascaded operation, there are three stages of buffer amplifier called the sync buffers, which help to provide sufficient LO signal drive to the TX and RX sections of the cascaded MMICs, from very low levels of 24 GHz input signal from the master chip. Section 5.1 provides more information on the cascaded operation of the device.

Figure 16 shows the transmitter output characteristics for maximum MPA and TX_driver gain settings over temperature and frequency. Each transmitter can deliver a typical output power of +5 dBm. PCB and connector losses have been compensated for these measurements.

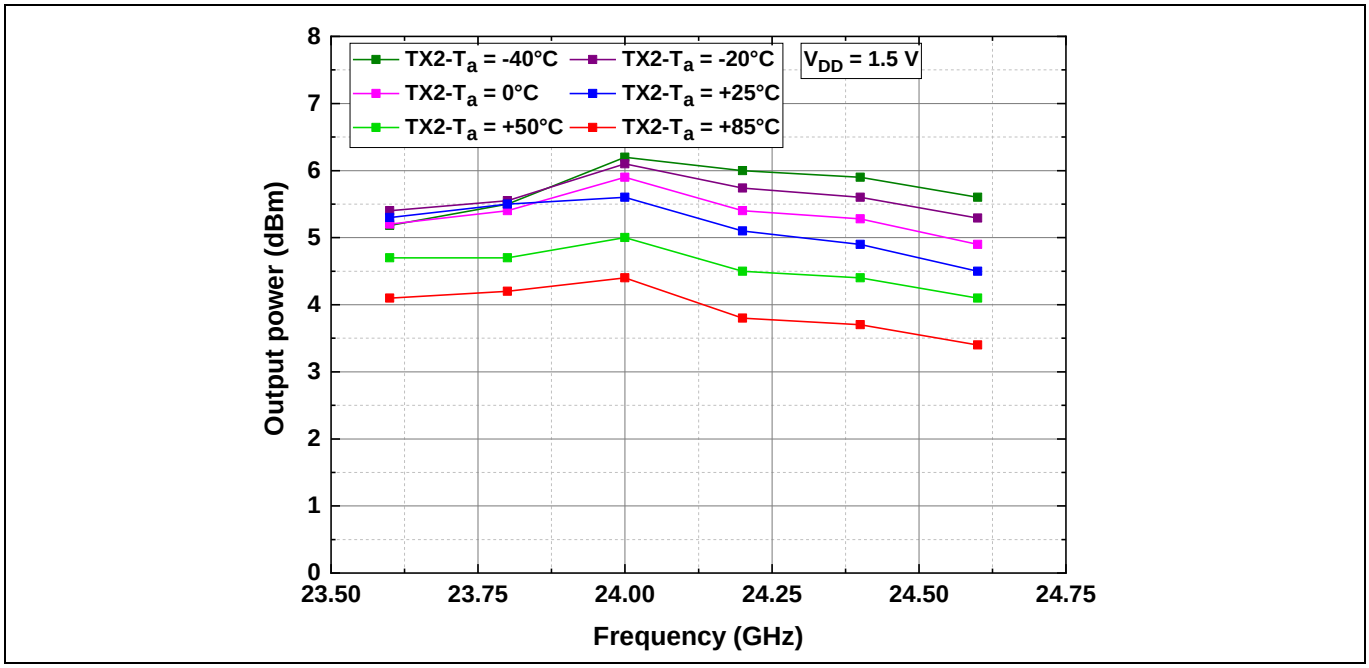


Figure 16 TX output power vs. frequency and temperature

Figure 17 shows the dynamic range of the transmitter under typical operating conditions. Using the configurable gain settings at the MPA and TX_driver, the transmitter can provide a dynamic range greater than 20 dB. PCB and connector losses have been compensated for these measurements.

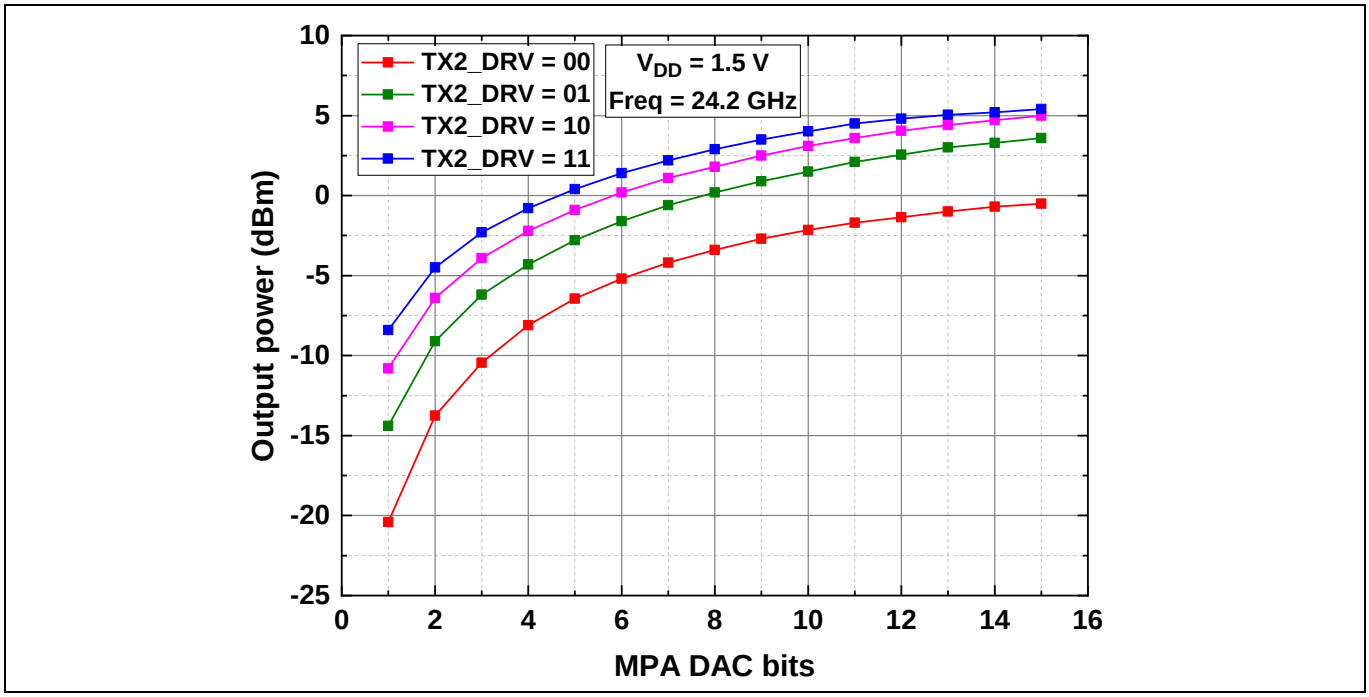


Figure 17 TX output power vs. MPA and TX driver gain settings at 25°C

Figure 18 shows the performance of the transmitter over supply voltage and temperature variation for different MPA and TX_driver gain settings. PCB and connector losses have been compensated for these measurements.

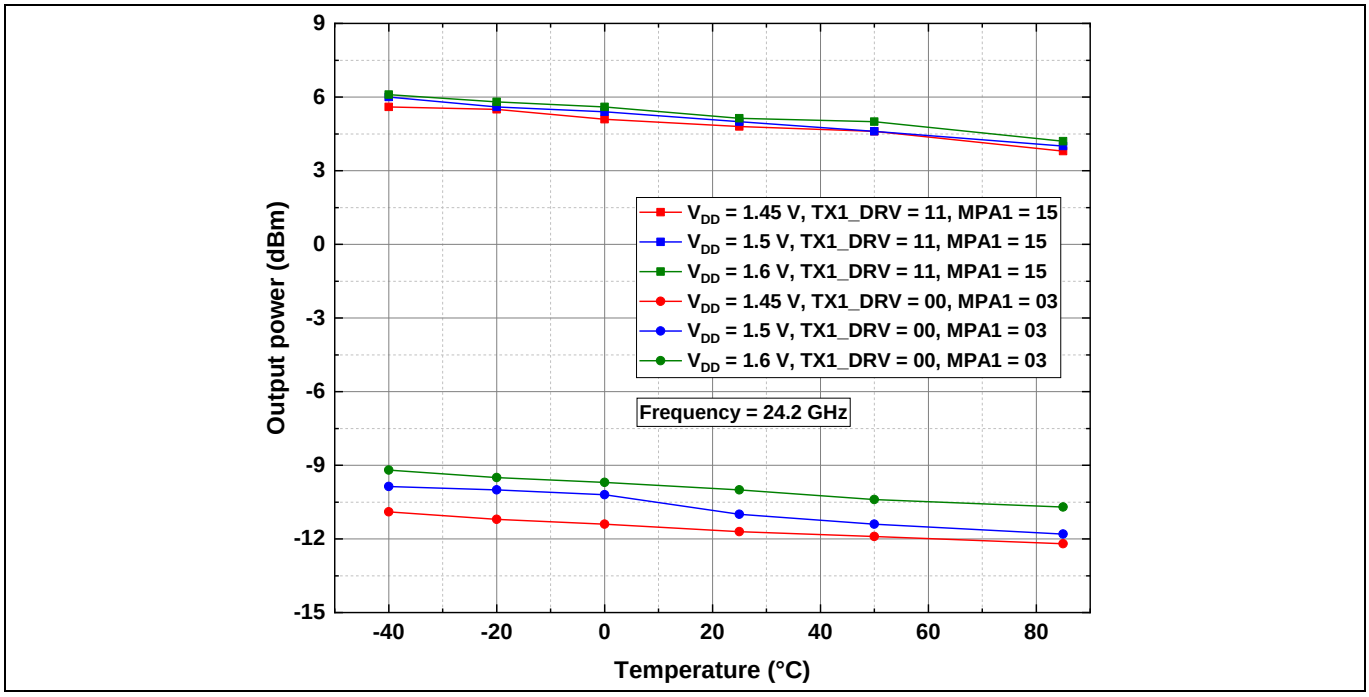
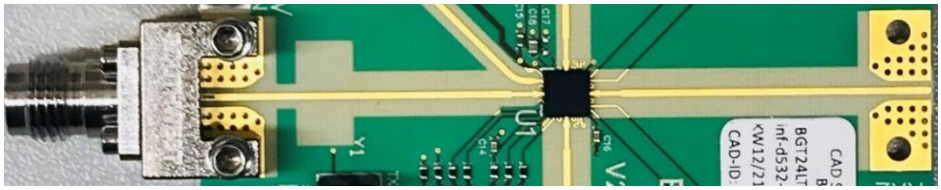


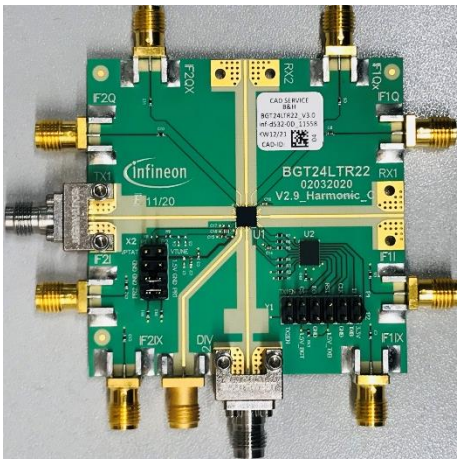
Figure 18 TX output power vs.MPA DAC, TX_driver gain, temperature and power supply

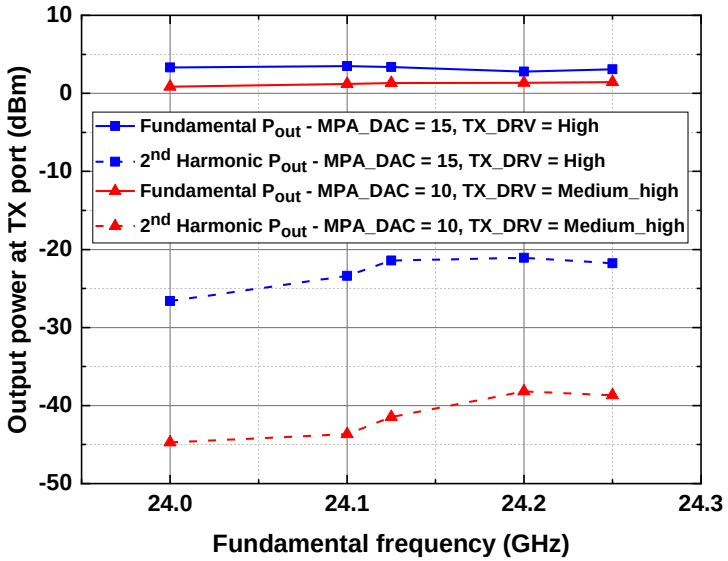
The following section shows the harmonic performance of the BGT24LTR22. The TX_driver and MPAs in the chip are optimized to deliver a typical output power of +5 dBm operating from a low power supply voltage range of 1.45 V to 1.6 V. The TX output stages are therefore working very close to their saturation levels when programmed to deliver the maximum transmitter output power at 24 GHz. Working close to such saturation levels also leads to generation of higher harmonic content from the transmitter.

Figure 19 shows the measured output power of both the fundamental (24 GHz) and its harmonic signal (48 GHz). The devices were soldered onto specially designed PCBs fitted with 2.4 mm high-frequency connectors for this measurement. The goal of this measurement was to show the difference between the output power at the fundamental frequency and its harmonic. Therefore, the PCB losses were NOT de-embedded from these measurements. All the results correspond to the 2.4 mm connector interface. Table 4 lists the measured values. Two different gain settings of the TX blocks are compared.



a) PCB for measuring second harmonic signal with 2.4 mm connector (without any filters)





b) Output power at TX port (dBm) vs. Fundamental frequency (GHz)

Figure 19 Fundamental and second harmonic output power at TX port vs. frequency

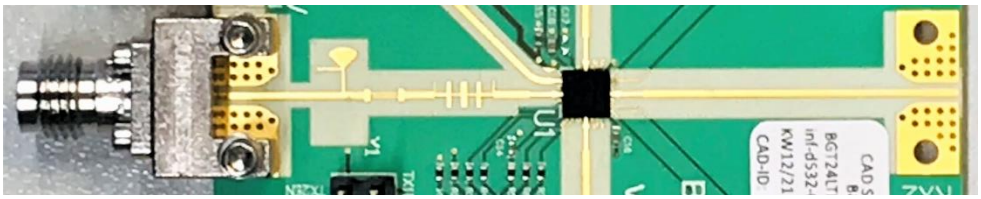
Attention: ***PCB losses are not compensated for the above measurements.***

Table 4 Measured fundamental and second harmonic output power (PCB without any harmonic filters)

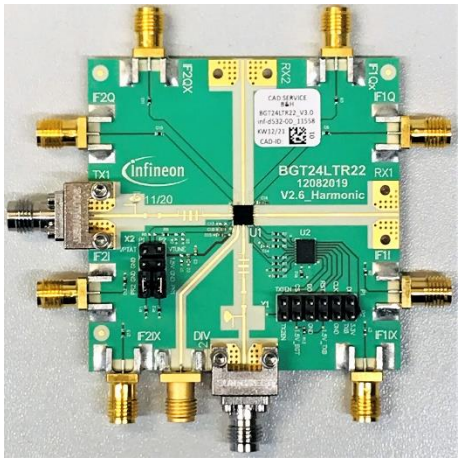
Frequency (GHz)	P_{OUT} (dBm) – fundamental at TX_driver = high MPA = 15_D	P_{OUT} (dBm) – second harmonic at TX_driver = high MPA = 15_D	Second harmonic rejection (dBc)	P_{OUT} (dBm) – fundamental at TX_driver = med_high MPA = 10_D	P_{OUT} (dBm) – second harmonic at TX_driver = high MPA = 15_D	Second harmonic rejection (dBc)
24.00	2.4	-32.9	35.3	0.9	-44.7	45.6
24.125	2.7	-26.3	29	1.3	-41.5	42.8
24.250	2.3	-25.6	27.9	1.4	-38.7	40.1

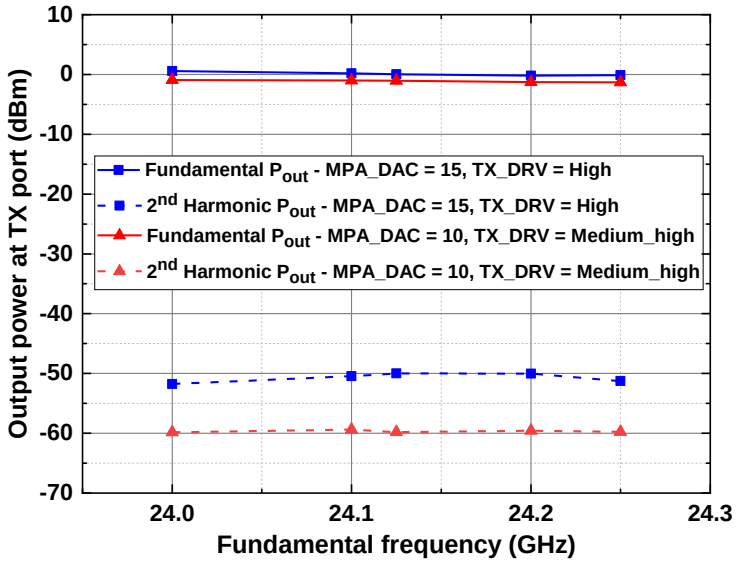
It can be observed from Figure 19 that by reducing the fundamental output power by approximately 1.5 dB the second harmonic levels can be reduced by more than 10 dB. Therefore, for systems not requiring the entire +5 dBm output power from the chip, it is recommended not to use the maximum power transmission settings. The TX of the BGT24LTR22 offers a very high level of configurability, which when carefully utilized can minimize the harmonic levels significantly, thereby minimizing the design efforts on the external harmonic filters on the PCB. The gain settings of the TX_driver impact the harmonic content more than the gain settings of the MPA. Of course, the external harmonic filters provide a higher attenuation to the harmonic content from the device.

However, the external filters also introduce losses in the transmission path. An example is shown in Figure 17, where more than 20 dB attenuation for the second harmonic signal was achieved with an external harmonic filter network. PCB losses were not compensated. The external filters along with the transmission lines, connectors and matching networks introduce an additional loss of approximately 2.5 dB.



a) PCB for measuring second harmonic signal with 2.4 mm connector (with harmonic filters)





b) Output power at TX port (dBm) vs. Fundamental frequency (GHz) with filters

Figure 20 Fundamental and second harmonic output power at TX port vs. frequency with filters

Attention: ***PCB losses are not compensated for the above measurements.***

Table 5 Measured fundamental and second harmonic output power (PCB with harmonic filters)

Frequency (GHz)	P_{OUT} (dBm) – fundamental at TX_driver = high MPA = 15_D	P_{OUT} (dBm) – second harmonic at TX_driver = high MPA = 15_D	Second harmonic rejection (dBc)	P_{OUT} (dBm) – fundamental at TX_driver = med_high MPA = 10_D	P_{OUT} (dBm) – second harmonic at TX_driver = high MPA = 15_D	Second harmonic rejection (dBc)
24.00	0.6	-51.8	52.4	-0.9	-59.9	59
24.125	0.1	-50	50.1	-1	-59.8	58.8
24.250	-0.11	-51.3	51.2	-1.3	-59.8	61.1

4.5 Receiver section

The BGT24LTR22 consists of two independent quadrature receivers with differential outputs. The RX is based on a direct conversion architecture. Figure 21 shows the block diagram of one complete RX section. The RX consists of an RF downconverter chain followed by an ABB section for the IF signal conditioning. The RX offers the flexibility to choose the amplified IF outputs from the internal highly integrated ABB stage or directly extract the downconverted IF signal from the mixer outputs to use with an externally designed ABB, depending on the application requirements. An arrangement of low-loss switches in the receiver IF section allows this flexibility. The bypass switch, when enabled, disables the ABB switch and routes the output of the mixer directly to the external IF pins. Similarly, when the ABB switch is enabled, the bypass switch is disabled and the amplified output from the internal ABB is routed to the external IF pins.

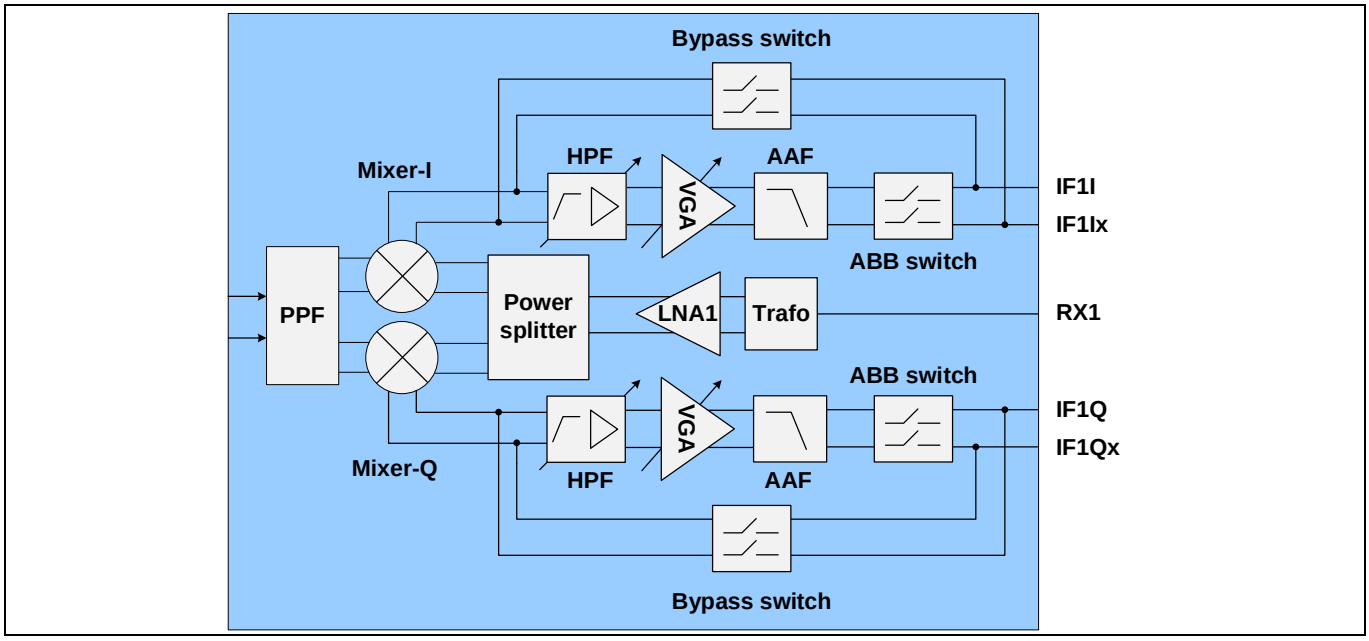


Figure 21 Receiver section block diagram

4.5.1 RX downconverter unit

Figure 22 shows the block diagram of the RX downconverter section without the ABB. The downconverter consists of a differential LNA, and quadrature mixers based on a modified Gilbert-type architecture with differential outputs. The LO signal for the mixers is generated by an RC PFF.

Since most antennas used are single-ended, transformers are used to convert the single-ended signal from the RF input pins to differential signals for the LNA input. A switch at the mixer output (bypass switch) allows the user to access the downconverted IF outputs from the mixer directly by bypassing the internal ABB. The IF signal from the mixer output is DC-coupled. The IF section in this case has a differential impedance of 1 kΩ and therefore must be connected to high-ohmic loads with typical impedance values greater than 10 kΩ, to prevent loading of the mixers. The mixer output is typically broadband (above 100 MHz).

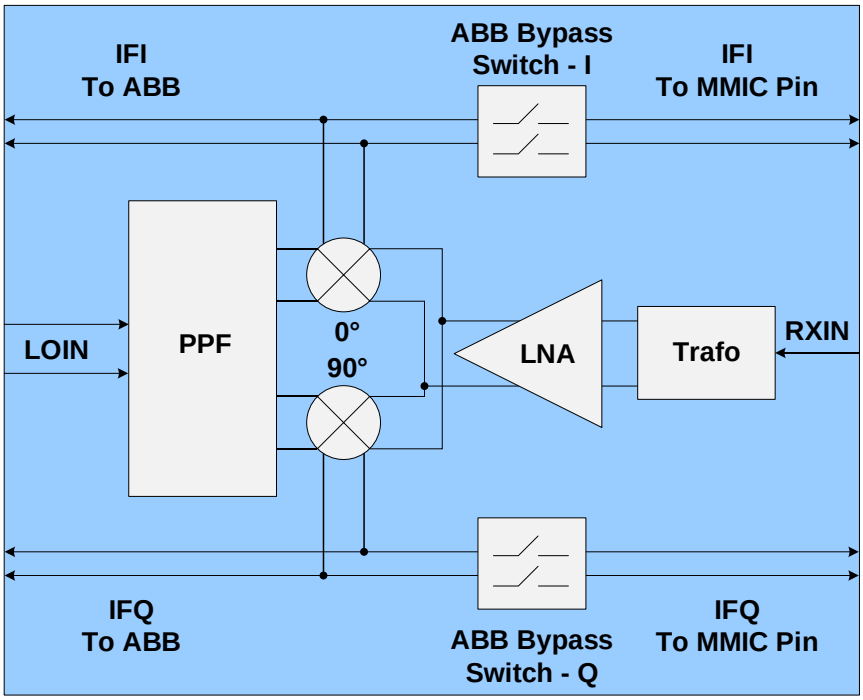


Figure 22 RX downconverter unit block diagram

Figure 23 and Figure 24 show the measured conversion gain (CG) and NFSSB of the RX downconverter vs. frequency and temperature, respectively. The downconverter provides a typical voltage conversion gain of 26 dB and NFSSB of 8 dB. The IQ amplitude imbalance remains between ±1.5 dB, and the channel-to-channel (RX1 to RX2) gain variation remains below 1.5 dB. PCB and connector losses were compensated for these measurements.

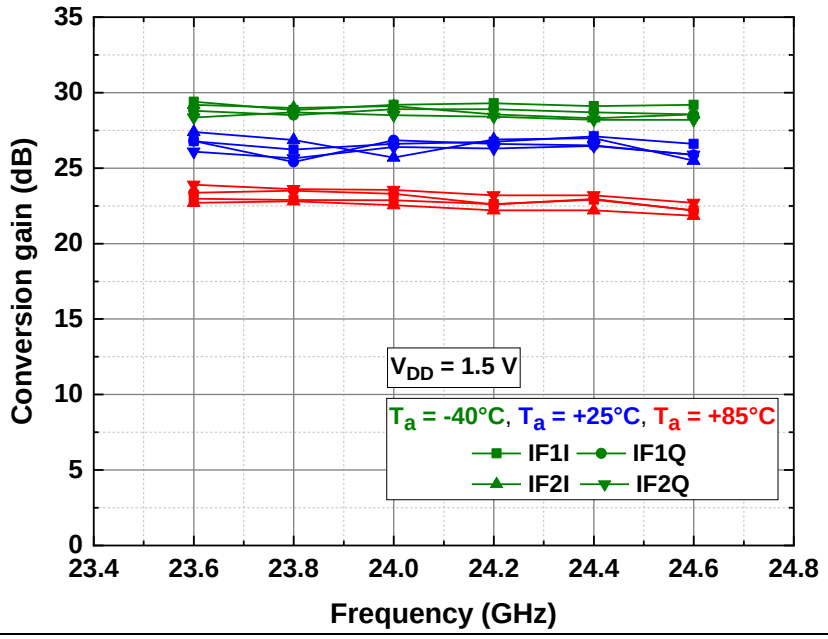


Figure 23 Downconverter conversion gain vs. frequency and temperature at IF = 200 kHz

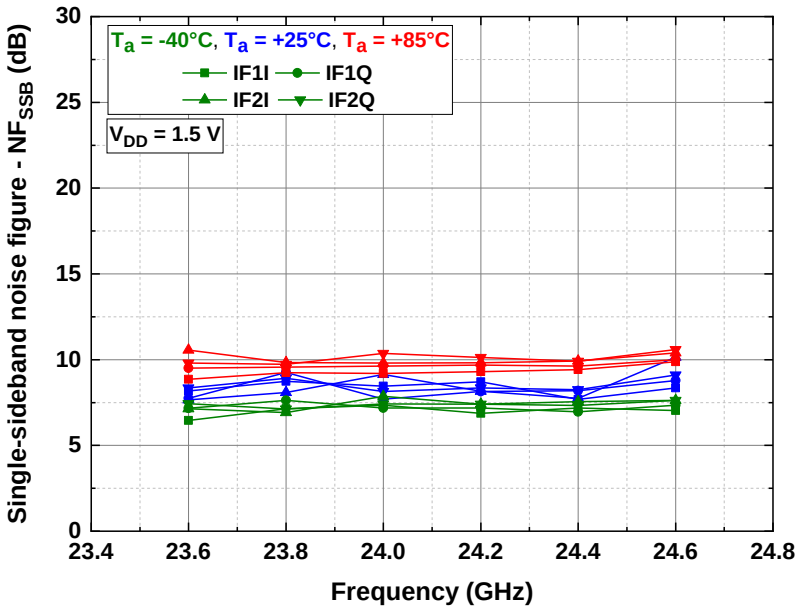


Figure 24 Downconverter NF_{SSB} vs. frequency and temperature at IF = 200 kHz

A major problem with DC architecture is the DC offset at the mixer outputs due to the finite isolation between the TX and RX ports of the device. Because in a DC transceiver the TX/LO and the RX signals are almost at the same frequency, there is a DC offset at the mixer outputs. Based on the non-idealities in the design and technology, this DC offset may be large enough to saturate the entire RX baseband chain and also lead to significant IQ imbalance issues. The BGT24LTR22 design overcomes this problem by providing good isolation between the TX and RX sections of the MMIC. Figure 25 shows the measured TX leakage power at the RX ports when transmitting at maximum output power. All RF ports were terminated with high-frequency 50 Ω connectors for this measurement.

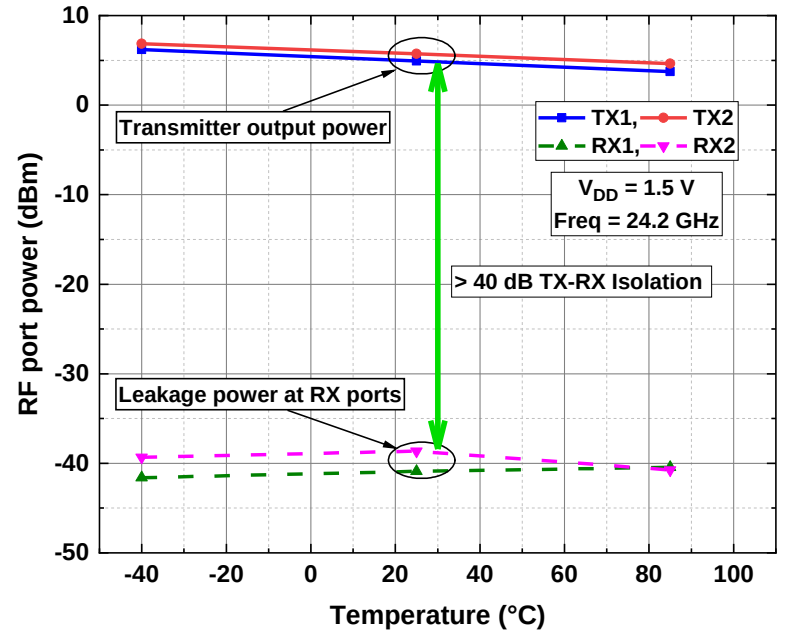


Figure 25 TX leakage power at RF ports at TX_driver = 11, MPA gain = 15_D

The MMIC provides a TX to RX isolation greater than 40 dB over the entire operating temperature range. The TX to RX leakage is also dependent on the frequency, and due to narrow ISM band operation at 24 GHz, it becomes extremely challenging to achieve a good broadband TX to RX isolation performance. Through proper MMIC, package and PCB design techniques, the BGT24LTR22 ensures that the isolation remains better than 40 dB over the entire ISM band, as shown in Figure 26. This good isolation significantly minimizes the DC offset at the IF output of the mixer. It can be observed from Figure 25 and Figure 26 that the variation of the output power between the two transmitter ports of the chip is typically less than 1 dB.

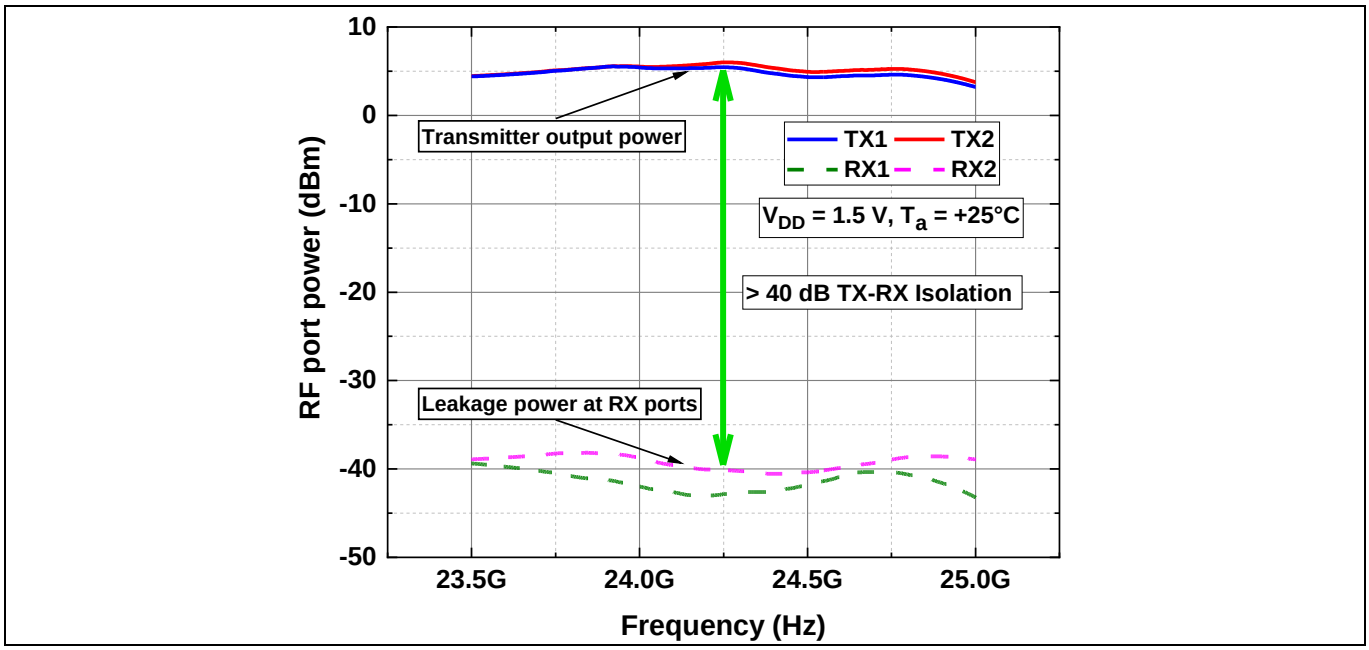


Figure 26 TX leakage power at RF ports vs. frequency at TX_driver = 11, MPA gain = 15_D

The good TX to RX isolation enables operation of the device without any receiver compression effects due to internal leakage signal from the TX. Figure 27 shows the measured input 1 dB compression point. The compression point is 15 dB higher than the TX leakage signal at the RX ports under all operating conditions.

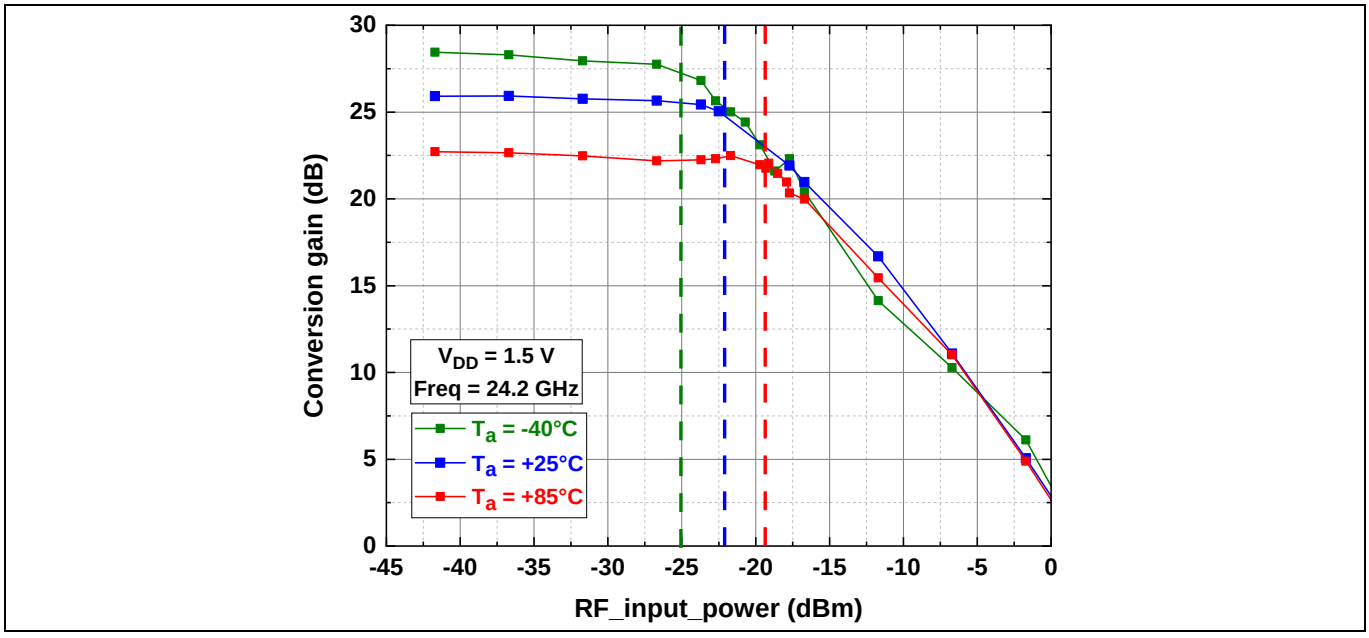


Figure 27 Downconverter input 1 dB compression point vs. temperature at IF = 200 kHz

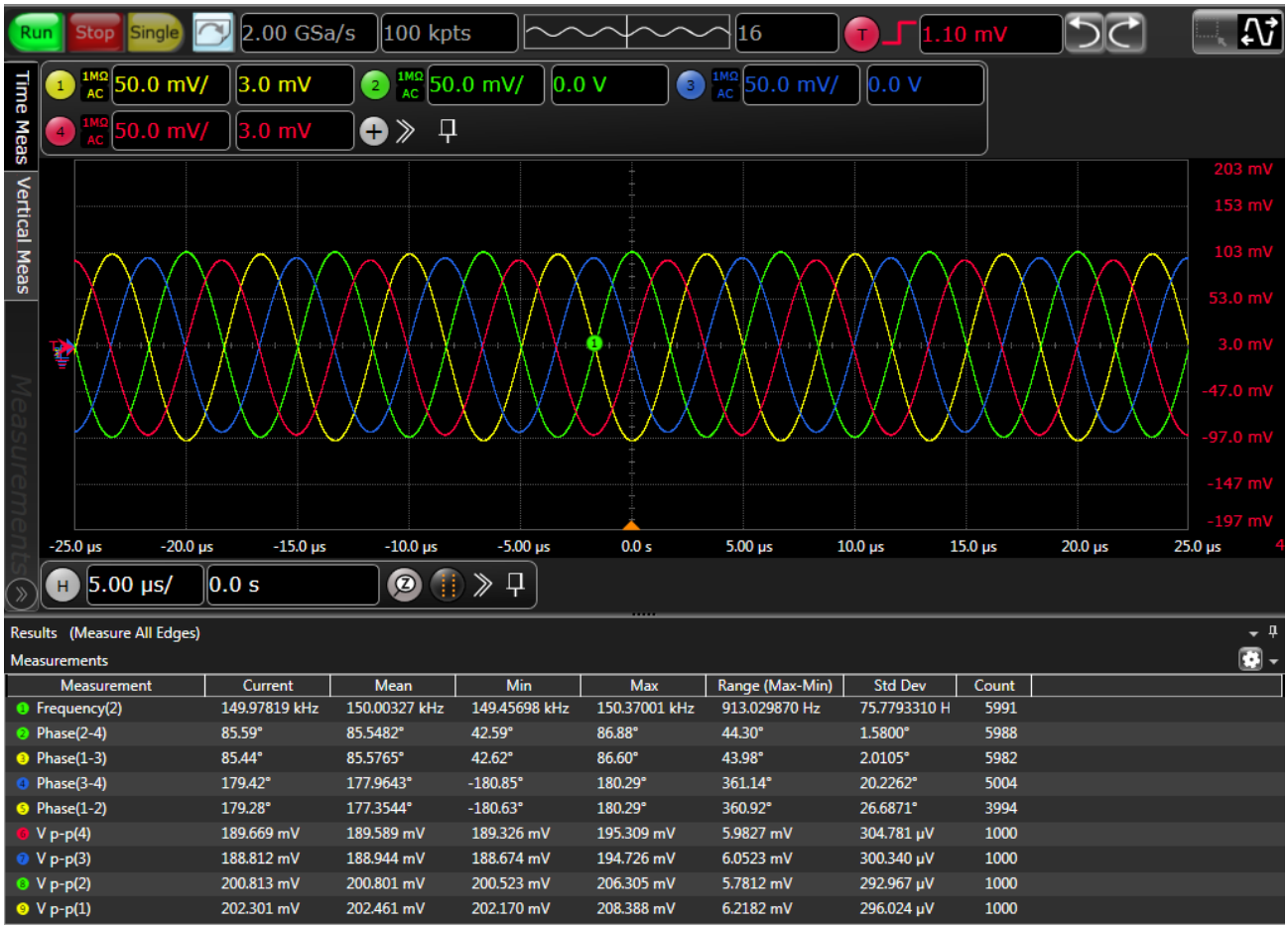
Figure 28 and Figure 29 show the measured IQ amplitude and phase imbalance at both the receiver outputs in the bypass mode.



Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
Frequency(2)	149.98515 kHz	149.99974 kHz	148.85091 kHz	151.12598 kHz	2.2750718 kHz	119.597301 H	41248
Phase(2-4)	87.76°	87.4260°	43.29°	89.05°	45.76°	1.9939°	41262
Phase(1-3)	86.84°	86.8274°	43.15°	87.95°	44.81°	1.6764°	41294
Phase(3-4)	180.15°	40.7554°	-181.04°	180.36°	361.40°	175.0281°	36866
Phase(1-2)	178.90°	174.7051°	-181.25°	180.29°	361.54°	39.3563°	27598
V p-p(4)	199.598 mV	195.581 mV	190.723 mV	199.987 mV	9.2640 mV	4.23981 mV	6896
V p-p(3)	199.112 mV	195.096 mV	190.524 mV	199.343 mV	8.8183 mV	4.03425 mV	6896
V p-p(2)	207.569 mV	202.806 mV	196.757 mV	211.421 mV	14.6636 mV	4.87237 mV	6896
V p-p(1)	207.057 mV	202.887 mV	197.868 mV	207.492 mV	9.6237 mV	4.44534 mV	6896

CH1 – IF1I – yellow | CH2 – IF1Ix – green | CH3 – IF1Q – blue | CH4 – IF1Qx – magenta
IF = 150 kHz | RF freq. = 24.2 GHz | V_{DD} = 1.5 V

Figure 28 RX1 – IF output – IQ amplitude and phase imbalance – typical at T_a = +25°C



Measurement	Current	Mean	Min	Max	Range (Max-Min)	Std Dev	Count
Frequency(2)	149.97819 kHz	150.00327 kHz	149.45698 kHz	150.37001 kHz	913.029870 Hz	75.7793310 H	5991
Phase(2-4)	85.59°	85.5482°	42.59°	86.88°	44.30°	1.5800°	5988
Phase(1-3)	85.44°	85.5765°	42.62°	86.60°	43.98°	2.0105°	5982
Phase(3-4)	179.42°	177.9643°	-180.85°	180.29°	361.14°	20.2262°	5004
Phase(1-2)	179.28°	177.3544°	-180.63°	180.29°	360.92°	26.6871°	3994
V p-p(4)	189.669 mV	189.589 mV	189.326 mV	195.309 mV	5.9827 mV	304.781 µV	1000
V p-p(3)	188.812 mV	188.944 mV	188.674 mV	194.726 mV	6.0523 mV	300.340 µV	1000
V p-p(2)	200.813 mV	200.801 mV	200.523 mV	206.305 mV	5.7812 mV	292.967 µV	1000
V p-p(1)	202.301 mV	202.461 mV	202.170 mV	208.388 mV	6.2182 mV	296.024 µV	1000

CH1 – IF2I – yellow | CH2 – IF2Ix – green | CH3 – IF2Q – blue | CH4 – IF2Qx – magenta
IF = 150 kHz | RF freq. = 24.2 GHz | V_{DD} = 1.5 V

Figure 29 RX2 – IF output – IQ amplitude and phase imbalance – typical at T_a = +25°C

4.5.2 Analog baseband unit

BGT24LTR22 is the first in Infineon's 24 GHz radar MMIC series, which includes a highly integrated programmable ABB unit for IF signal conditioning. The ABB is designed for FMCW radar application and features a tunable HPF followed by a variable-gain amplifier (VGA) and an AAF. The chip consists of four ABB units, each corresponding to I- and Q-channels of the two receivers. Figure 30 shows the block diagram of one of the ABB units. The arrangement of the functional blocks inside the ABB enables strong amplification of a weak signal received from a radar target, simultaneously reducing the impact of the TX to RX crosstalk, which is a major concern in any FMCW radar system. The BGT24LTR22 with its very good TX to RX isolation already compensates for this effect to a great extent. Figure 31 shows the measured frequency response of the complete RX chain including the ABB and RF downconverter for a fixed VGA gain and variable HPF settings. Figure 32 shows the measured frequency response at a given high-pass cut-off frequency for different VGA settings. The output from the ABB is also DC-coupled with a differential output impedance of 400 Ω.

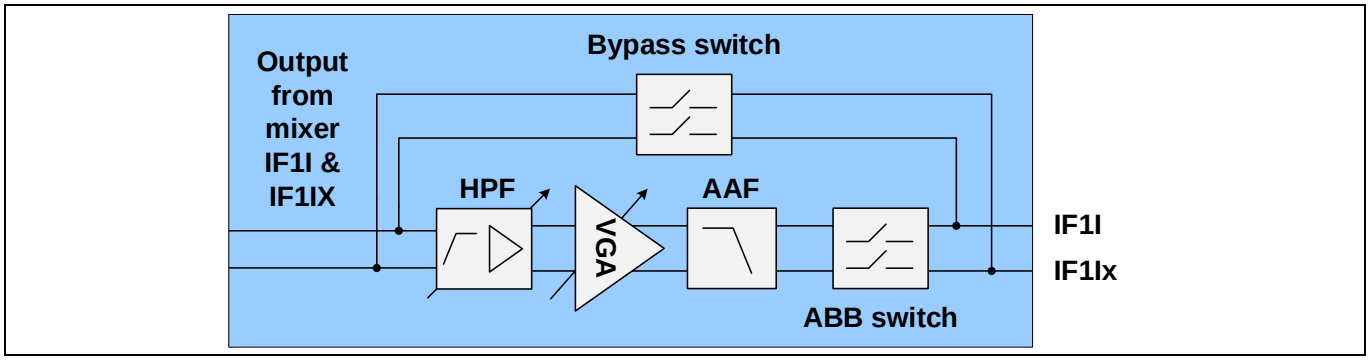


Figure 30 ABB unit block diagram

Table 6 provides a summary of all the programmable options of the ABB section.

Table 6 ABB configurable parameters

Block	Tunable parameter	Value
HPF	Gain	18 dB, 30 dB
	3 dB cut-off frequencies	20 kHz, 50 kHz, 80 kHz, 100 kHz
VGA	Gain	0 dB, 5 dB, 10 dB, 15 dB, 20 dB, 25 dB, 30 dB

The AAF is fourth-order type with a cut-off frequency of 600 kHz.

Note: The HPF and LPF (AAF) cut-off frequencies specified for the ABB section represent only the 3 dB cut-off frequency points. This in no way implies that they are unusable beyond those specified frequency points. Consider for example the frequency response of the ABB in Figure 31. For a HPF cut-off frequency of 20 kHz, the gain of the ABB section at 1 kHz is still significantly higher (greater than 50 dB) and at 1 MHz is also greater than 60 dB. A target corresponding to these frequencies (depending on its RCS) will still produce a strong reflected signal in the FMCW output spectrum. It is therefore strongly recommended to consider this, and also the FMCW ramp parameter (chirp bandwidth and chirp time) settings before replacing the internal ABB with an external one.

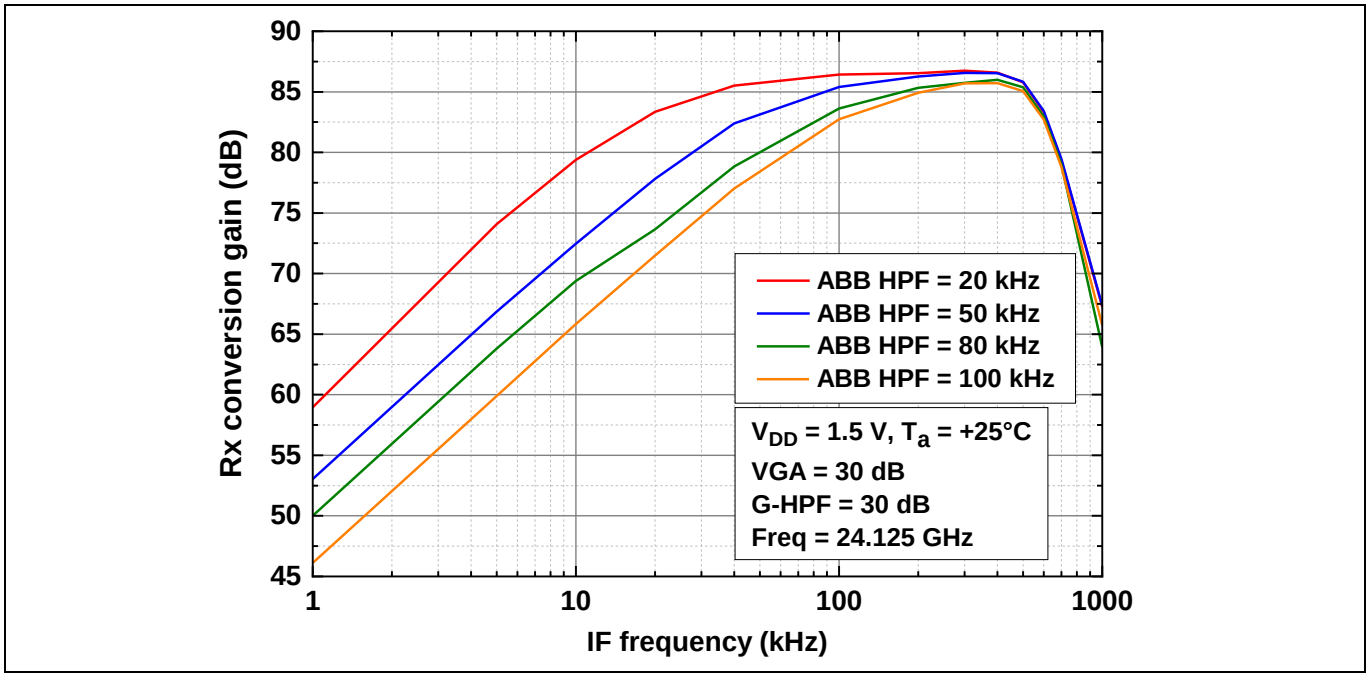


Figure 31 ABB unit – measured frequency response vs. HPF settings

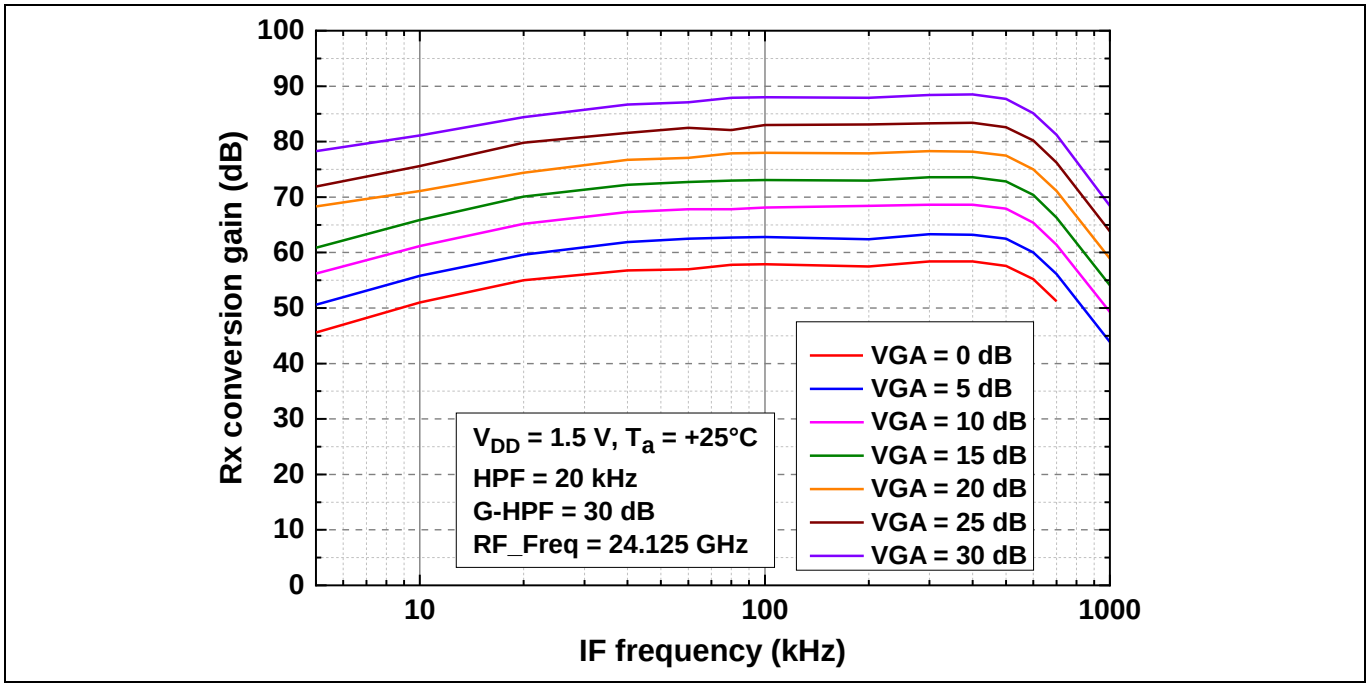


Figure 32 ABB unit – measured frequency response vs. VGA settings

For FMCW radar systems using a slower chirp time (e.g., 256 µs, 512 µs, 1 ms, 1.5 ms) and low bandwidth (e.g., 180 MHz, 200 MHz, 220 MHz, 250 MHz) typically results in target IF beat frequencies in the lower kHz or even sub-kHz range for targets very close to the radar. At first glance, the 20 kHz HPF cut-off frequency setting of the BGT24LTR22 device might lead to a wrong assumption that targets close to the radar could go undetected due to the low gain of the ABB at these frequencies. However, remember that for targets close to the radar antennas, the strength of the signal received is also higher, and a very high gain from the ABB might completely saturate the processing chain due to the strong reflection from the nearby target. Therefore, typically for detection of targets closer to the radar, it is recommended to have the ABB configured for a lower gain setting

to avoid any saturation effect. In such cases, the lower HPF cut-off frequency of 20 kHz to 80 kHz might still be sufficient to reliably detect targets close to the radar. The maximum gain settings of the internal ABB might not be necessary for many applications. It is therefore strongly recommended to experiment with all the settings of the internal ABB for the chosen application scenario before opting for an external op-amp-based solution.

Depending on the radar system, it might not be possible to connect all the eight IF outputs from the BGT24LTR22 directly to the ADCs of an external MCU due to pin limitations. In such situations, any low-cost general-purpose op-amp with unity gain can be used to interface the device to the MCU, as shown in Figure 33. The gain-bandwidth of the external op-amp must be greater than 600 kHz, to accommodate the cut-off frequency of the integrated AAF.

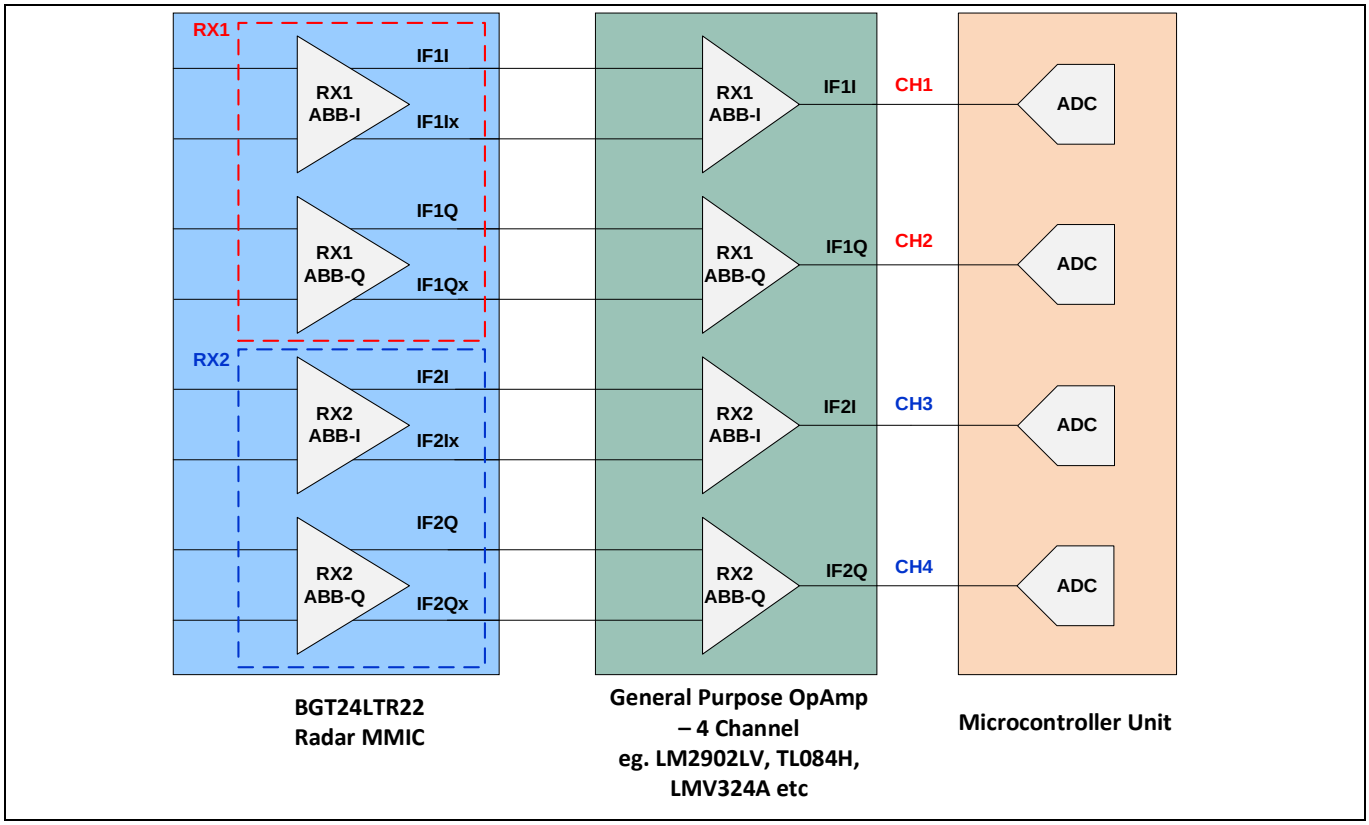


Figure 33 Interfacing the BGT24LTR22 MMIC with an external MCU for signal processing

Based on the application requirements and algorithm used, it might also be sufficient to use the radar data from only one channel from each receiver for signal processing, thereby further reducing the ADC pin requirement on the external MCU.

The ABB has a minor impact (approximately 0.5 dB) on the NF_{SSB} of the entire receive chain. This is mainly due to the excellent noise performance offered by the LNA and mixer.

4.6 Integrated sensors

The BGT24LTR22 consists of several integrated sensors to monitor the device parameters. The analog outputs of the sensors are digitized by the integrated 8-bit ADC and made available via the SPI. This section provides a detailed explanation of the temperature and TX output level sensors.

4.6.1 Temperature sensor

Monitoring of the chip temperature is provided by an on-chip temperature sensor, which delivers a temperature-proportional voltage output. This voltage is digitized by the on-chip ADC and read out via the SPI.

Figure 34 shows the uncalibrated transfer characteristics of the integrated temperature sensor and a formula to calculate the chip temperature from the measured ADC value. This measurement was done by biasing only the temperature sensor and the ADC. All other blocks were kept off. As the temperature sensor and ADC draw very low current, there is very little power dissipation in the chip and the chip temperature may be considered to be the same as the ambient temperature or the evaluation board temperature. Under normal operation, when all the blocks are turned on, the chip temperature will be higher compared to the ambient temperature because the chip's power dissipation is considerably higher in this case. The power dissipation is not fixed, as the current consumption of the chip will depend on how it is configured. Additionally, the ratio of chip temperature to ambient temperature is strongly influenced by the PCB design. Therefore, in a final radar system, it is important to calibrate the temperature sensor of each chip individually.

The formula derived from the measurements described in this section can be used to calculate the temperature of the chip when all blocks are turned on. In typical cases, when the device is operated in the master mode with all blocks turned on, the temperature of the device is approximately 15 °C to 20 °C higher than in the off state. The equation mentioned in Figure 18 can then be used to measure the temperature of the chip when all blocks are turned on.

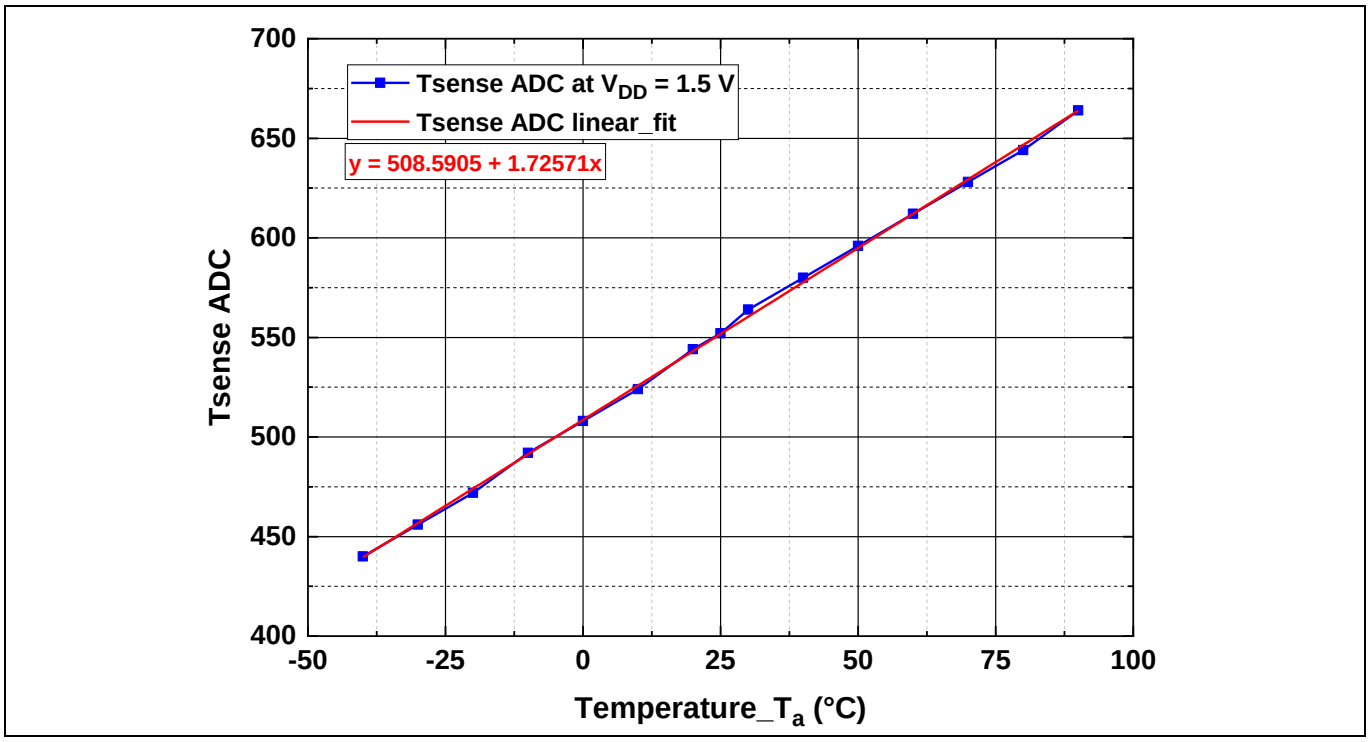


Figure 34 Transfer characteristics of a random device's temperature sensor

Note that the measurements in Figure 34 include the following uncompensated effects:

- ADC conversion error
- Temperature sensor block measurement accuracy error
- Linearity errors

These errors affect the accuracy of the temperature sensor, which varies from sample to sample. Therefore, it is strongly recommended to perform the calibration of the temperature sensor on each sample. The best way to perform the calibration is always to power off all the blocks in the device and then obtain the transfer characteristics accordingly. This transfer characteristics should then be used to measure the actual chip temperature when the device is fully turned on.

4.6.2 TX output level sensor

For output power measurement, power sensors are placed at the output of the MPAs on both the TXs. These sensors can be used to get an indication of the transmitted power at both TX1 and TX2 ports. It should be noted here that the TX output level sensors are not true power sensors but peak voltage detectors. Hence, the actual voltage output of the power sensors is strongly dependent on the terminations at the amplifier outputs.

To eliminate temperature and supply voltage variations, the sensor works by comparing its readings (Power_MPA1) to a reference output voltage signal (Power_TX1) made available via an auxiliary circuit inside the chip. The compensated detector output voltage is given by the difference between Power_MPA1 and Power_TX1 for both power sensors. This voltage difference is proportional to the RF voltage swing at the individual amplifier outputs. Its characteristic is non-directional.

Table 7 Power sensor signals and ADC result output registers

Block	Signal name	Output register	Comment
TX1	Power_MPA1	Register 38	Actual power sensor output
	Power_TX1	Register 39	Reference output
TX2	Power_MPA2	Register 41	Actual power sensor output
	Power_TX2	Register 42	Reference output

Figure 35 shows the measured transfer characteristics of the power sensor of a random device and also gives a formula to calculate the power in dBm from the measured ADC values. The measurement was carried out by monitoring the output frequency on a spectrum analyzer, and a power sensor was used to measure the output power from the chip at the same time.

Equation 1 is used to convert the ADC values to analog voltage. This equation can be used to calculate the analog values from all other ADC channel results too, and is not specific to the power sensor.

Equation 2 and equation 3 represent the formula to convert the ADC values from the power sensor placed at the output of MPA1 and the reference value associated with it, respectively. Equation 4 calculates the delta in mV, which is represented by the x-axis in Figure 35.

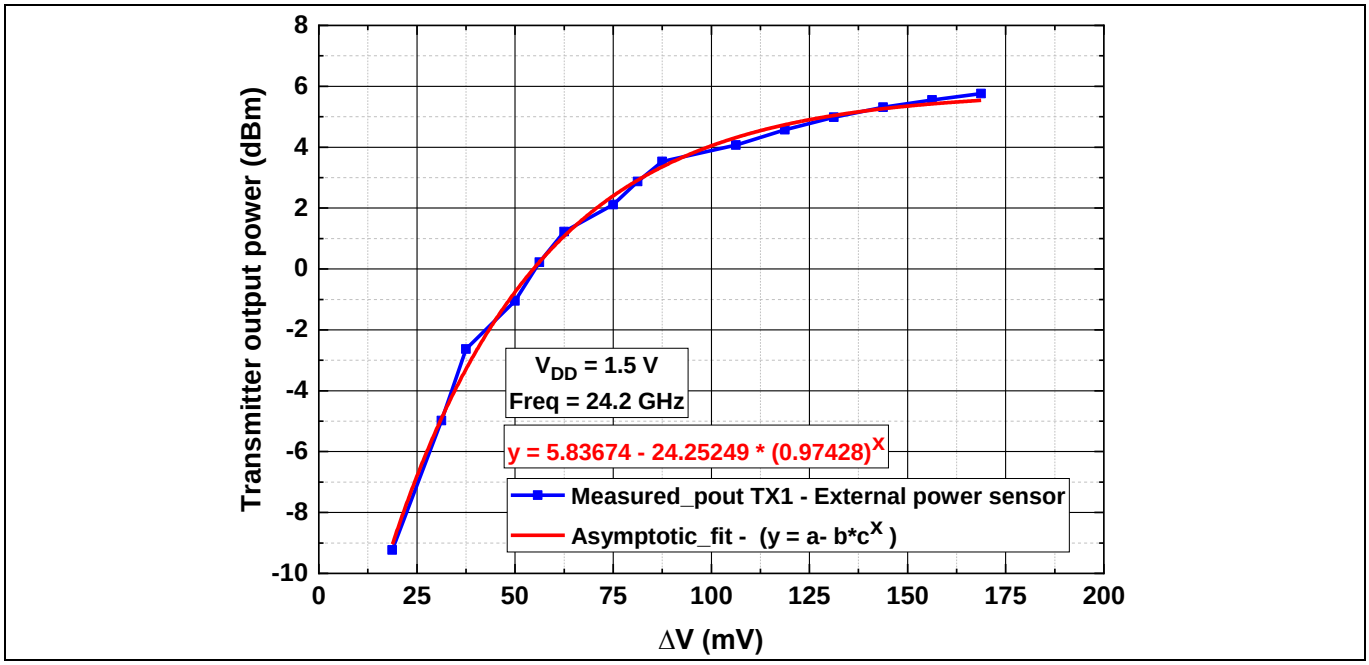


Figure 35 Transfer characteristics of a random device's power sensor

$$Analog\ Value(V) = \frac{ADC\ Output\ Value * 1.6}{1024}$$

Equation 1

$$Psense_MPA1(V) = \frac{ADC\ Output\ Value\ (Register\ 38) * 1.6}{1024}$$

Equation 2

$$Psense_TX1(V) = \frac{ADC\ Output\ Value\ (Register\ 39) * 1.6}{1024}$$

Equation 3

$$\Delta V\ (mV)\ =\ (Psense_MPA1\ (V) - Psense_TX1\ (V))\ *\ 1000$$

Equation 4

Note: The output level sensors in this device are not designed to accurately measure the output power of the chip. They are designed to give a rough indication of the transmitted power to check if there is a malfunction of the chip or the system.

5 Device operating modes and DC characteristics

BGT24LTR22 is the first MMIC in Infineon's 24 GHz radar series that allows the user to operate the device in multiple transmit, receive modes depending on the application scenario. Apart from the typical 2TX to 2RX mode of operation, the device can be configured to operate in several other modes, as described in Figure 36. The highly configurable nature of the device allows complete shutdown of circuit blocks that are not used for a particular operating mode.

For advanced beamforming applications requiring a higher number of transmit and receive antennas, the scalable feature of the BGT24LTR22 device allows cascading of multiple devices, enabling the designer to significantly improve the angular resolution offered by the radar system.

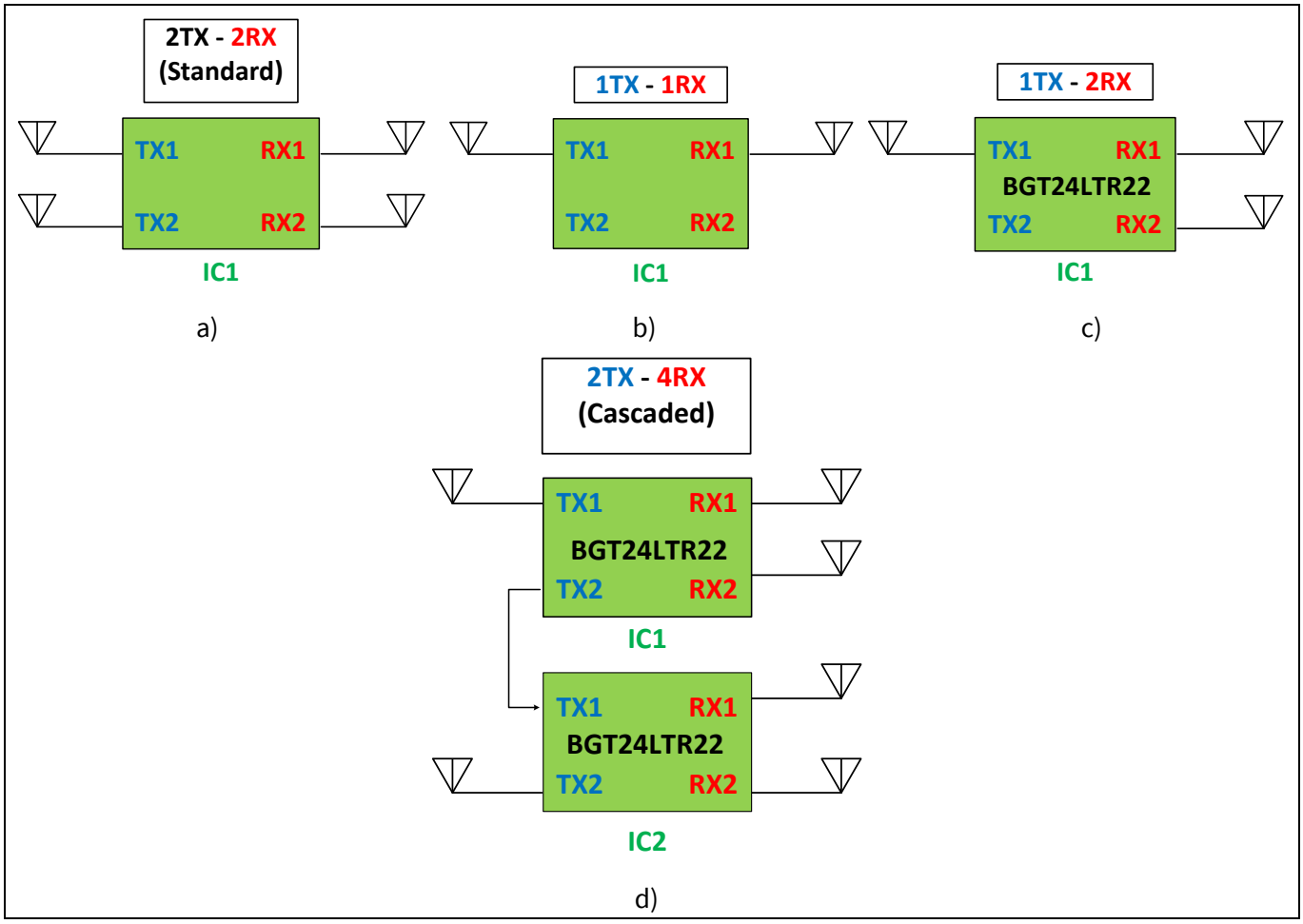


Figure 36 BGT24LTR11 operating modes

The default operating mode is the 2TX to 2RX case, and a block-by-block power consumption of the device is shown in Figure 37 when operated in this mode.

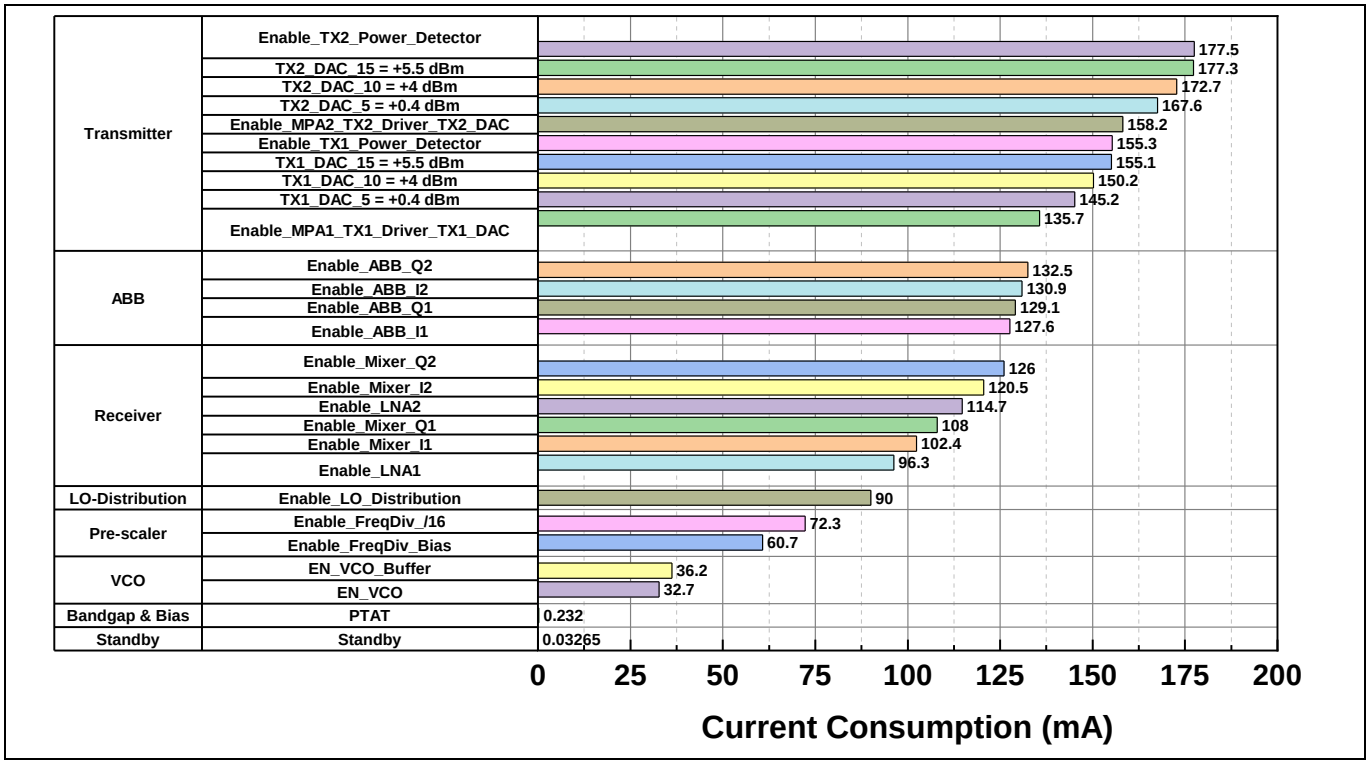


Figure 37 Block-by-block DC power consumption in 2TX to 2RX mode

The current consumption depends on the device configuration. The above case corresponds to the SPI register settings shown in Table 8.

Table 8 Register values for master mode operation – both TX and RX enabled

Register	Circuit block	Value
Register 0	VCO and prescaler	0x0063
Register 1	TX1	0x03FD
Register 2	Power detectors and sync buffers – TX1	0x0030
Register 3	TX2	0x03FD
Register 4	Power detectors and sync buffers – TX2	0x0030
Register 5	RX1 downconverter	0x0007
Register 6	ABB1 – RX1	0x006E
Register 7	RX2 downconverter	0x0007
Register 8	ABB2 – RX2	0x006E
Register 9	Transmitter bandgap biasing	0x0003
Register 10	LO distribution network	0x781D
Register 11	PTAT DAC settings	0x7D90
Register 32	PTAT selector	0x8000
Register 34	ADC	0x0007
Register 55	PTAT DAC factory settings	0x0000

Note: All register values not specified in the above table are at their default settings.

The DC current consumption of the transceiver varies with the TX output power. Typical values are within 135 mA and 178 mA, corresponding to the entire dynamic range of the TX. For applications requiring low power consumption, it is recommended to operate the device with a TX output power specific to the particular use case system budget. Not all applications would require the maximum TX output power. Also, the ultra-low RX NFSSB of 8 dB helps to achieve significantly better signal-to-noise ratio (SNR) with lower TX output power compared to legacy Infineon MMICs. Figure 38 shows the DC current consumption of the device vs. temperature and various SPI settings when both the transmitters are enabled and set to maximum output power levels, and both receiver downconverters including the ABB are turned on. When the prescaler is not used, it can be fully turned off, thereby saving up to 35 mA current. The low-frequency prescaler consumes up to 7 mA lower current than the high-frequency (1:16) prescaler. In addition, the ADC when enabled consumes around 1 mA.

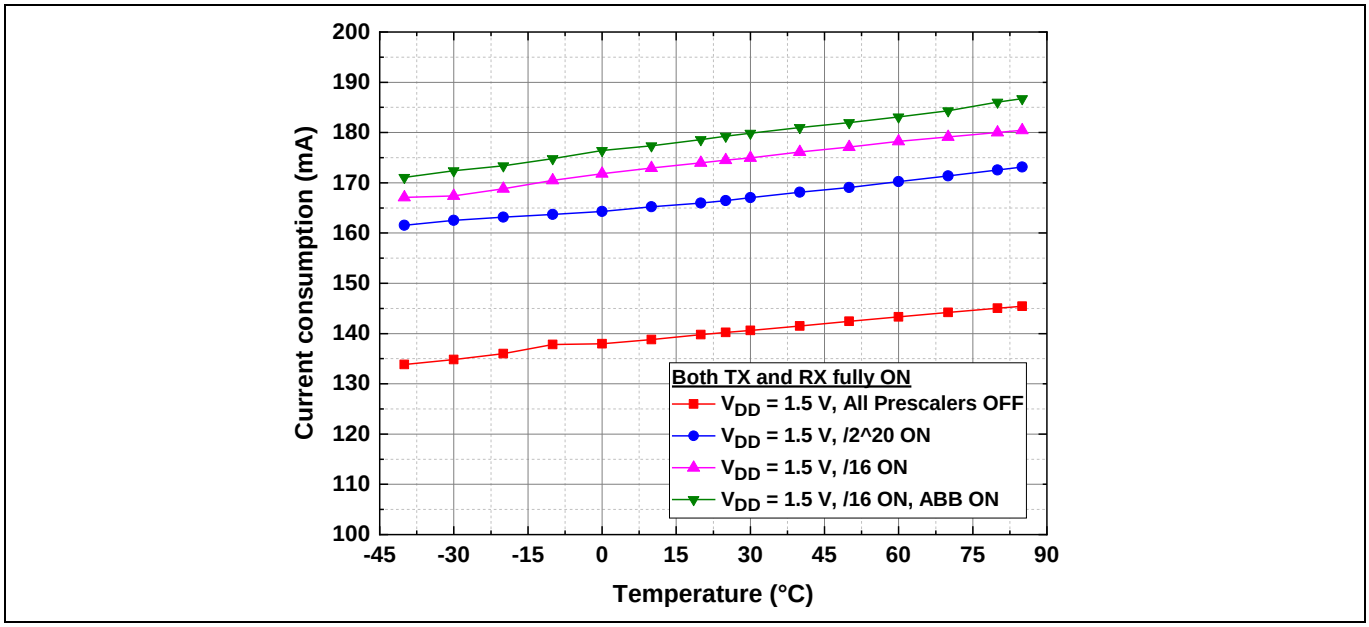


Figure 38 DC current consumption vs. temperature and SPI settings (2TX to 2RX mode)

Figure 39 shows the current consumption of the device vs. temperature when operated in other modes.

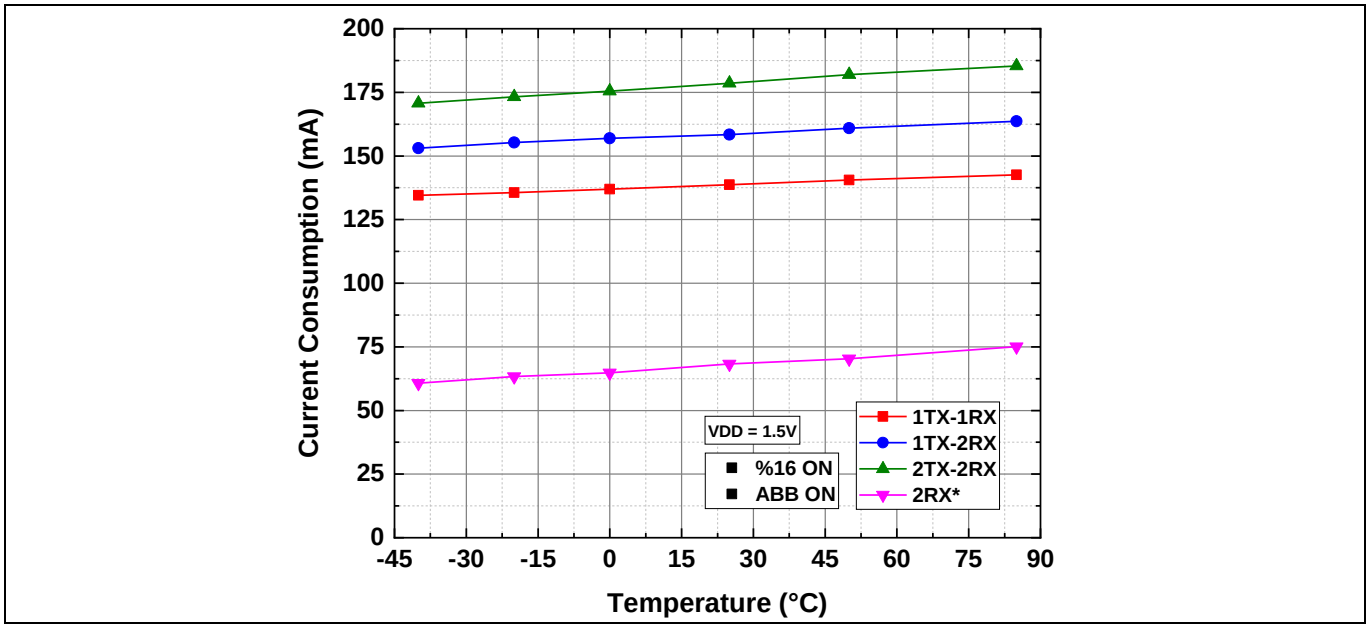


Figure 39 DC current consumption vs. temperature for several operating modes

The BGT24LTR22 MMIC can be put in a complete standby mode. Figure 40 shows the current consumption of the device in the standby mode vs. temperature. The standby current is approximately 35 µA at ambient temperature when all blocks are turned off.

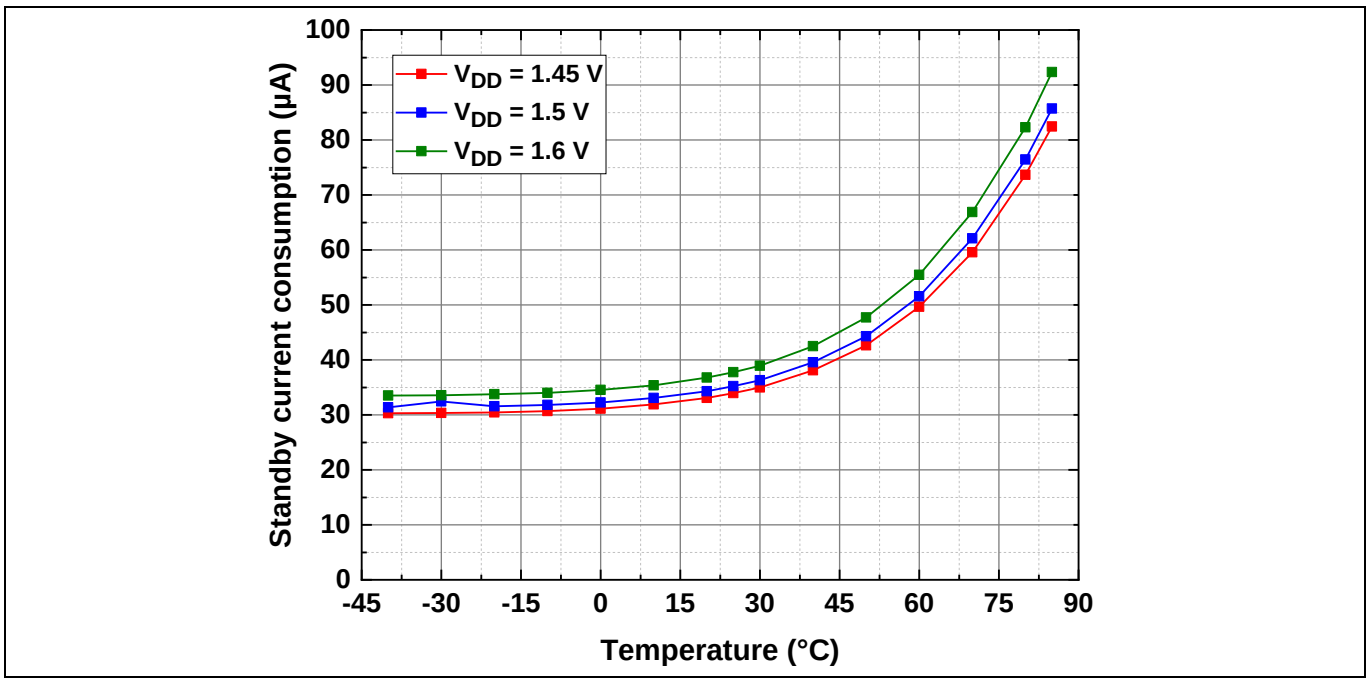


Figure 40 DC current consumption – standby mode

5.1 Cascaded/slave mode operation

Figure 41 shows the block diagram of an implementation of a multichannel beamforming system with two BGT24LTR22 devices.

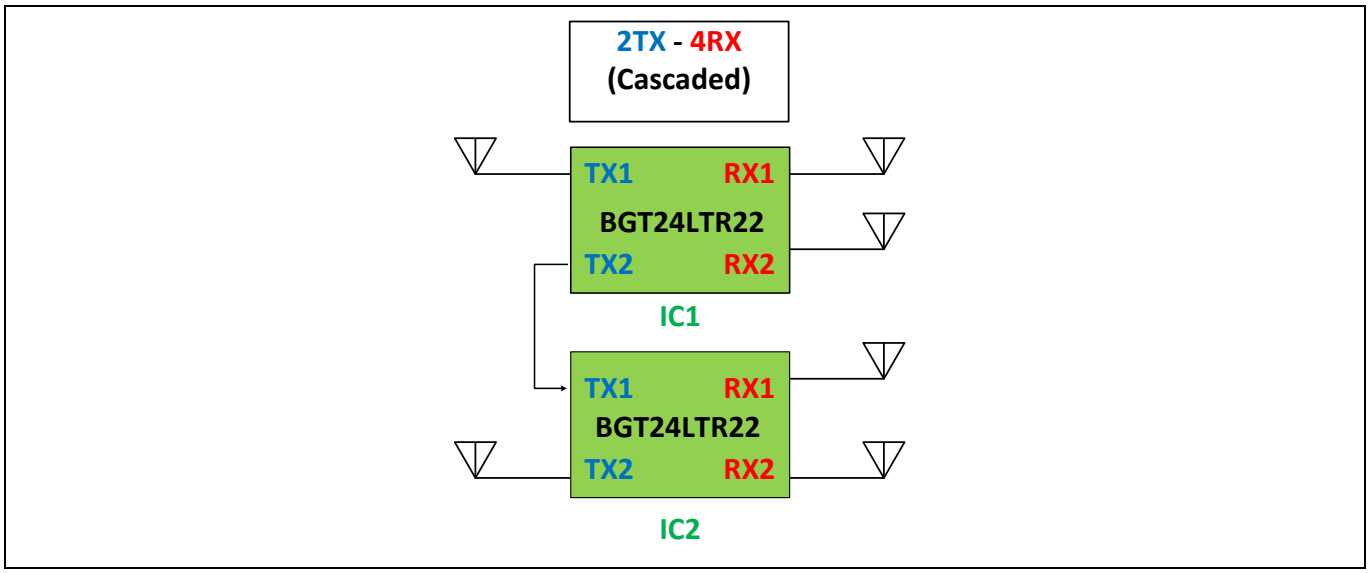


Figure 41 BGT24LTR22 operated in multichannel configuration (cascade/slave mode)

Each TX pin of the BGT24LTR22 device is bidirectional. This means it can either be used to transmit a 24 GHz microwave signal or receive a 24 GHz LO input signal. The feature enables connection of multiple BGT24LTR22 devices together to increase the number of TX and RX channels in the radar system. In such an implementation,

the first BGT24LTR22 MMIC operates as the master chip (IC1) with an LO output signal connected to the transmitter port of the slave MMIC (IC2). Based on layout requirements, any TX port of the slave MMIC can be used as the LO signal input port and any TX port of the master chip can be used as the LO signal output port. The other TX port of the slave MMIC can be either used as a transmitter leading to a 2TX to 4RX configuration or can be left unused leading to a 1TX to 4RX system. It is mandatory to turn off the VCO on all the slave devices. Also, the TX_driver and the MPA on the TX section of the slave device must be turned off.

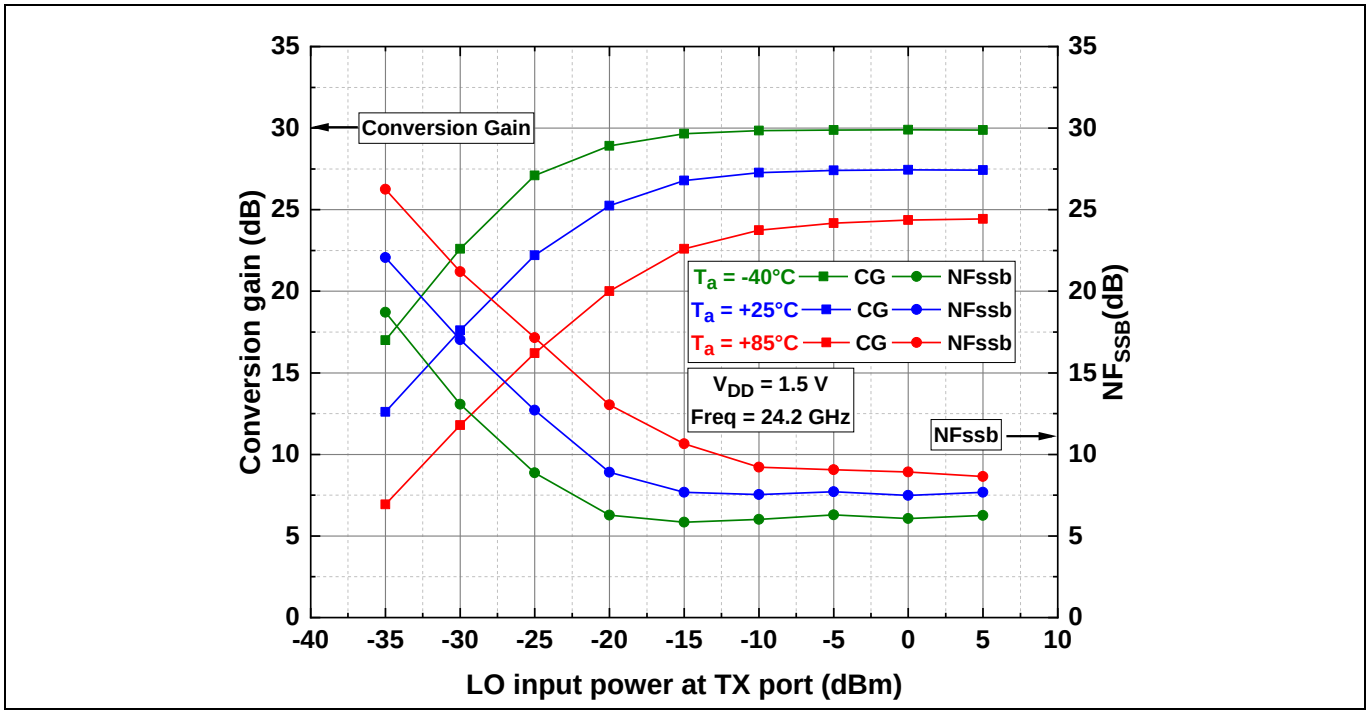


Figure 42 RX conversion gain and NF_{SSB} vs. temperature and LO input power (slave mode)

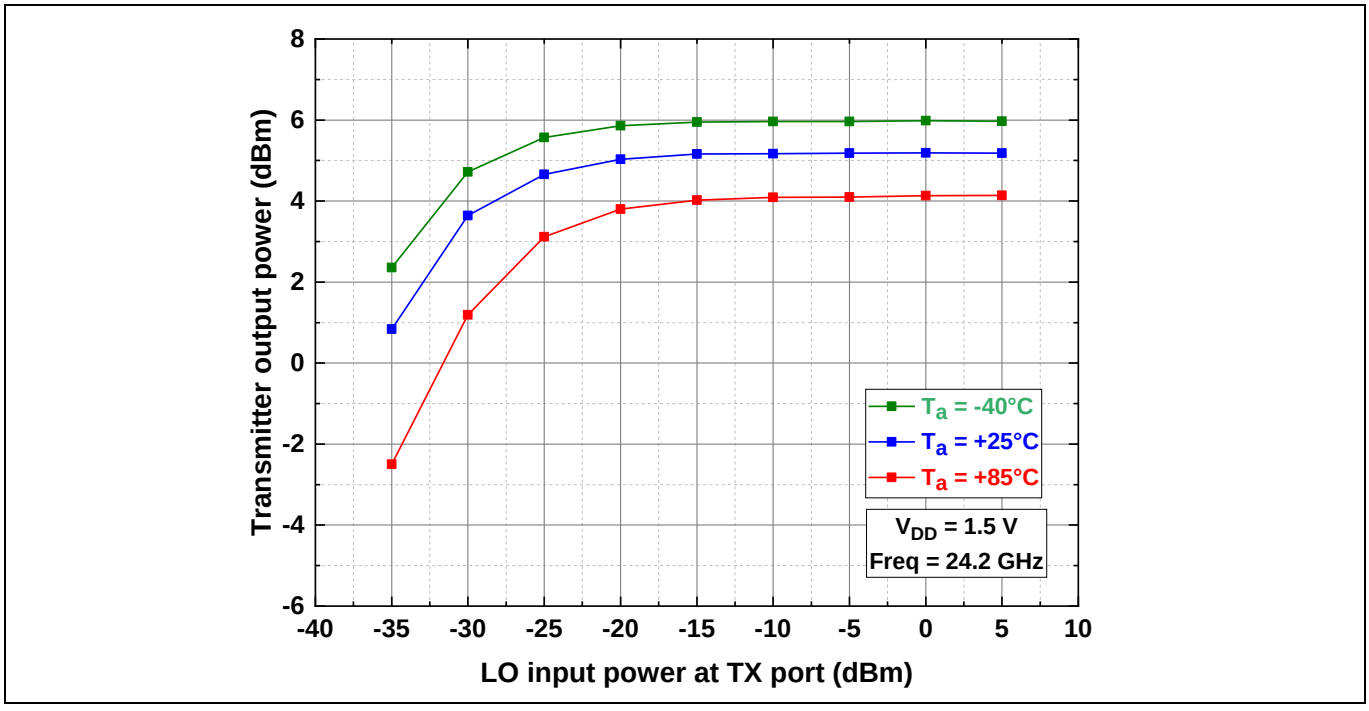


Figure 43 TX output power vs. temperature and LO input power (slave mode)

The MMICs operating in slave mode require sufficient LO power from the master device to provide the best receiver conversion gain, NF_{SSB} and TX output power. Figure 42 shows the RX performance vs. LO input power over temperature, and Figure 43 shows the generated TX output power vs. the LO input power over temperature. It can be observed that the RX already provides its maximum conversion gain and minimum NFSSB with LO input power as low as -10 dBm. The TX can provide the maximum output power even at LO input signals close to -15 dBm. Three stages of sync buffer amplifiers in the LO input section of the slave MMIC enable operation of the device with such low levels of LO input power. Table 9 provides the SPI register settings for a typical slave mode operation scenario. TX1 was used as the LO input signal for this test.

Table 9 Register values for slave mode operation

Register	Circuit block	Value
Register 0	VCO and prescaler	0x0000
Register 1	TX1	0x0000
Register 2	Power detectors and sync buffers – TX1	0x01C0
Register 3	TX2	0x03FD
Register 4	Power detectors and sync buffers – TX2	0x0030
Register 5	RX1 downconverter	0x0007
Register 6	ABB1 – RX1	0x006E
Register 7	RX2 downconverter	0x0007
Register 8	ABB2 – RX2	0x006E
Register 9	Transmitter bandgap biasing	0x0007
Register 10	LO distribution network	0x58E1
Register 11	PTAT DAC settings	0x0000
Register 32	PTAT selector	0x0000
Register 34	ADC	0x0007
Register 55	PTAT DAC factory settings	0x0000

Note: All register values not specified in the above table are at their default settings.

6 SPI interface

The main digital control interface to the BGT24LTR22 is the SPI. The MMIC uses a four-wire SPI to communicate with a host controller. This section describes the functionality of the SPI module and registers and provides a complete guide to configuring the individual blocks of the device. For a complete understanding of the SPI module and its functionality, a detailed block diagram of the chip is revisited in Figure 44.

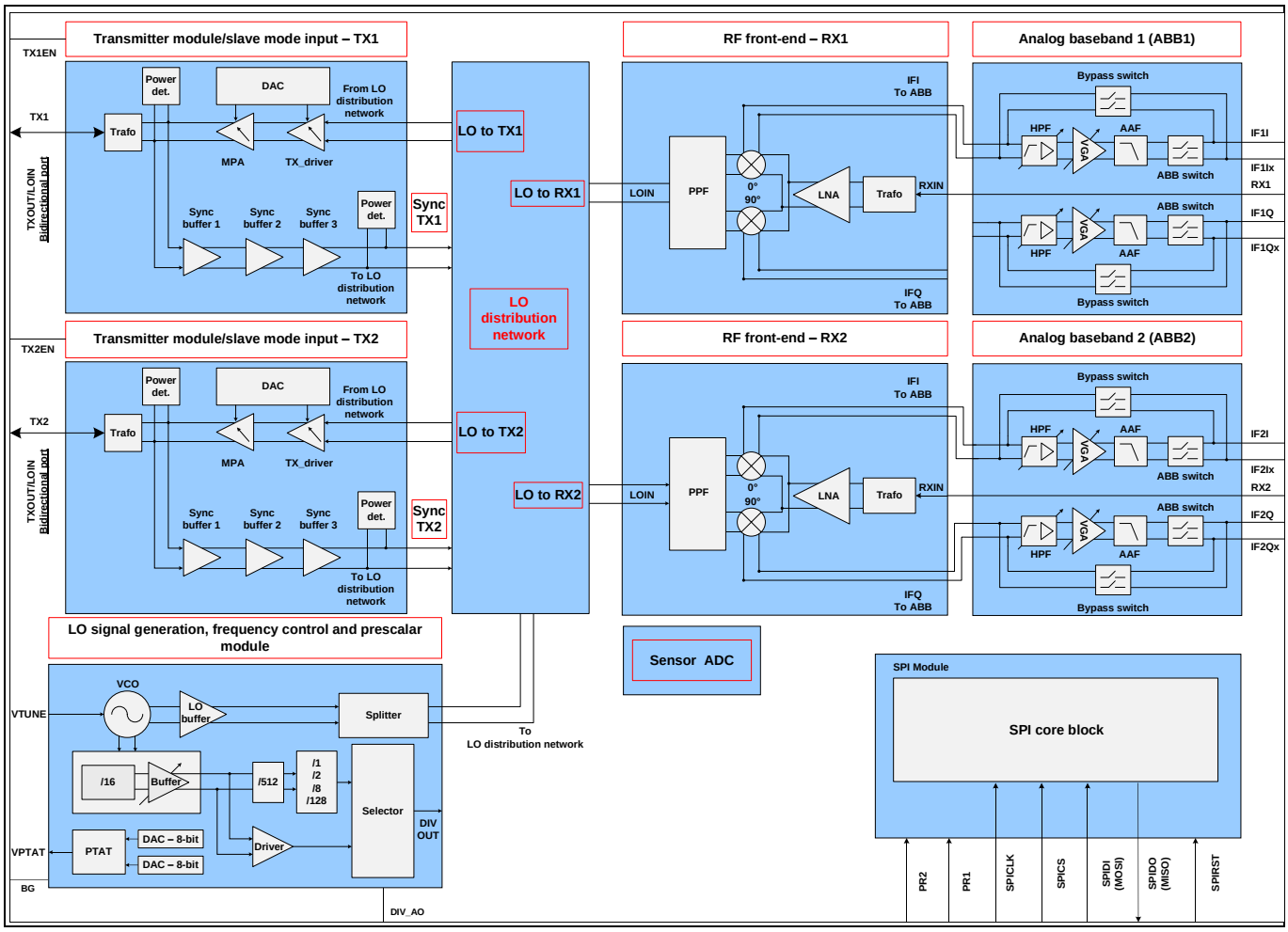


Figure 44 BGT24LTR22 detailed block diagram with all configurable blocks

The following sections of the transceiver are configurable via the SPI:

- Bandgap and biasing network
- LO signal generation (VCO) and frequency control unit (PTAT)
- Frequency divider/prescaler module
- LO signal distribution unit
- Transmitter modules (TX1 and TX2)
- Integrated buffer amplifier network for external LO input signal amplification (sync TX1 and sync TX2)
- Quadrature homodyne RF downconverter units (RX1 and RX2)
- ABB module (ABB1 and ABB2)
- Power detectors and temperature sensors
- Integrated 8-bit ADC

There are three major modes of operation, shown in Table 10. By choosing the appropriate SPI settings, the MMIC can be configured to work in any ONE of the operating modes.

Table 10 BGT24LTR22 operating modes

Operating mode	Functionality
Master mode	Transceiver mode – with one transmitter (either TX1/TX2), two quadrature receive channels and one local oscillator output (either TX1/TX2). When using this mode, either TX1 or TX2 output pins can be used as a local 24 GHz oscillator signal output port to daisy-chain the BGT24LTR22 with other MMICs.
Slave/sync mode – TX1	Twin receiver only mode with external LO input via TX1 port. The internal VCO of the MMIC must be kept in the off mode. (Optionally, based on the specific application use case, the TX2 transmitter can be enabled, and the chip can operate as a transceiver MMIC with one transmitter and two quadrature receiver channels. The signal at the TX1 port acts as LO input to TX2.)
Slave/sync mode – TX2	Twin receiver only mode with external LO input via TX2 port. The internal VCO of the MMIC must be kept in the off mode. (Optionally, based on the specific application use case, the TX1 transmitter can be enabled, and the chip can operate as a transceiver MMIC with one transmitter and two quadrature receiver channels. The signal at the TX2 port acts as LO input to TX1.)

6.1 SPI interface description

The SPI is a basic communication interface to communicate with a host via serial connection link. It enables the host to read or write from registers as well as reading from sampling memory. The SPI bus is a synchronous serial data link that operates in full duplex mode. Devices communicate in slave mode, whereas the master device initiates the data frame. Multiple slave devices are allowed with individual slave select lines. To begin a communication, the master first configures the master clock, using a frequency less than or equal to the maximum frequency the slave device supports. Such frequencies are commonly in the range of 1 MHz to 50 MHz. The master pulls the chip select low for the desired slave. During each SPI clock cycle, a full duplex data transmission occurs. Figure 45 shows the block diagram of the SPI module. The SPI module in the BGT24LTR22 MMIC has the following features:

- Large 7-bit continuous address space
- Fixed payload of 16 bits (2 bytes)
- Chip select (slave select) active in low state

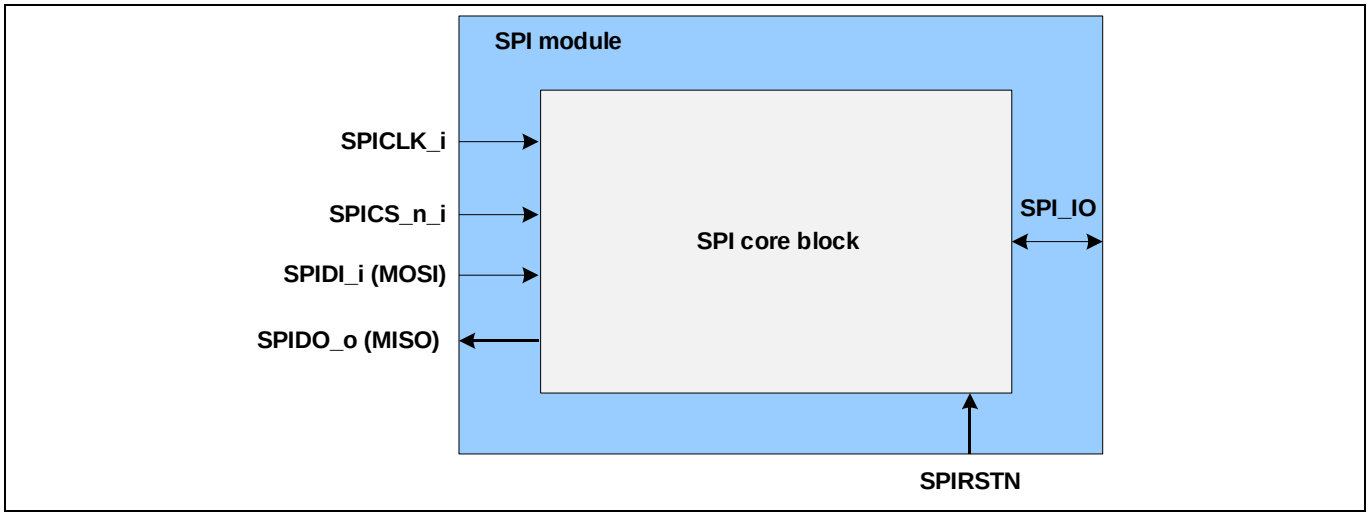


Figure 45 SPI module overview

Each word transferred over the SPI bus has a length of 1 command byte + 2 data bytes. The communication is done bitwise. The transmission is controlled by the start and stop condition defined by a high-to-low transition and a low-to-high transition, respectively, on the SPICS_n_i line. The SPI bus is considered busy after the start condition and free again after the stop condition. After the start condition is initiated, the register address is transferred with the MSB first. The address is 7 bits long and is followed by a single bit, which is a data direction bit indicating a read/write condition. A high level indicates a write operation, and a low level indicates a read operation. Every write mode is a read mode too. The R/W bit is followed by the 2-byte payload, which is also sent by MSB first. At the same time, while the command byte is received, a free from any system level configuration global status register GSR0 (8-bit) is serially shifted out on the SPIDO_o with the MSB first. On the following clock cycle, the selected register content is shifted out on the SPIDO_o with the MSB first. Figure 46 explains the SPI functionality and shows the relation between clock and data in a simplified SPI access.

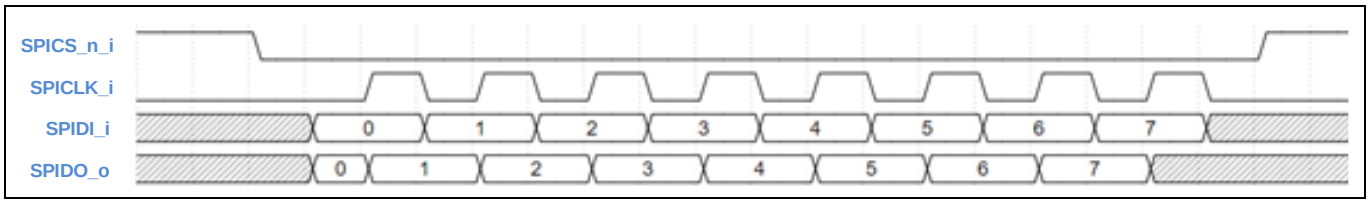


Figure 46 Example SPI data transfer (here just 8 bits in width)

The SPI command is read via the data input SPIDI (serial data in), which is synchronized with the clock input SPICLK provided by the microcontroller. The output word appears synchronously at the data output SPIDO (serial data out). The transmission cycle begins when the chip is selected by the input signal SPICS (chip select not), low active. With the last rising edge of SPICLK, data is written into the register block. The transmission cycle ends with a rising edge on the input signal SPICS. The SPIDO output is switched to tri-state status (high impedance) when the chip is not selected, thereby relaying the SPIDO bus for another use.

The working edge is the rising edge of the clock. The status of SPIDI is shifted into the input register with every working edge. And with every working edge, the state of the SPIDO bus is shifted out of the output register. The following sections describe the timing diagrams for write, read and burst mode operation.

In addition to the standard four-wire SPI pins, the BGT24LTR22 includes an additional pin called the SPIRSTN. The SPIRSTN when set to low ensures that all the SPI registers are reset to their default settings. During power-up, the SPIRSTN pin must be set too low to ensure that all registers have their default values. Only after the power supply reaches a steady-state must the SPIRSTN pin be turned to high to enable programming via the

SPI. During the entire SPI programming process, the SPIRSTN pin must be kept at a high state. The pin has an internal pull-up resistor to V_{DD}.

6.1.1 SPI write mode

A write access starts after the falling edge of SPICS with transfer of the 7-bit address, MSB first. The following eighth bit (RW = read/write bit) is “1”, indicating a write access. After that, the 16-bit payload is sent, also MSB first. At the same time, while the address and RW bit are received, the global status register GSR0 (8-bit) is serially shifted out on SPIDO (also MSB first). During sending of the payload, the previous register content is serially shifted out on SPIDO.

Finally, the rising edge on SPICS indicates the end of the access.

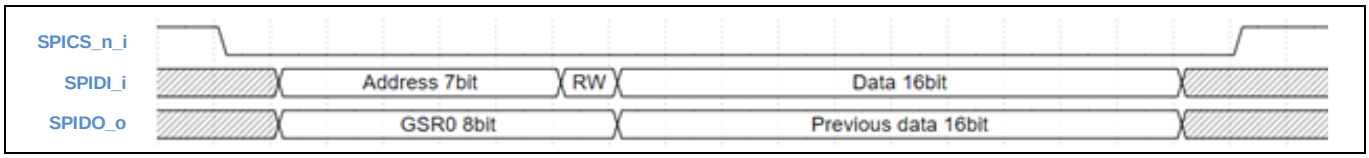


Figure 47 SPI write mode timing – MSB first anytime, RW = “1”

6.1.2 SPI read mode

A read access starts after the falling edge of SPICS with transfer of the 7-bit address, MSB first. The following eighth bit (RW bit) is “0”, indicating a read access. The following 16-bit data are ignored as they are not needed for a read access. At the same time, while the address and RW bit are received, the global status register GSR0 (8-bit) is serially shifted out on SPIDO (also MSB first). Directly after that, the read data is serially shifted out on SPIDO.

Finally, the rising edge on SPICS indicates the end of the access.

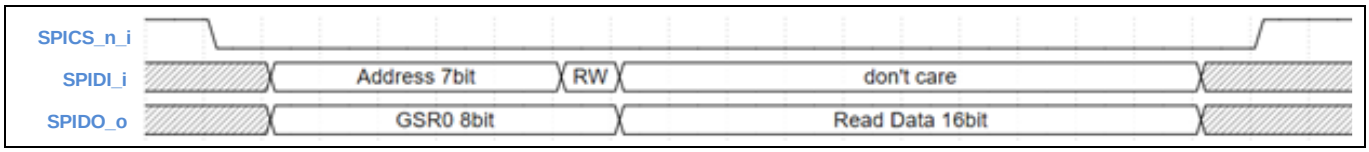


Figure 48 SPI read mode timing – MSB first anytime, RW = “0”

6.1.3 SPI burst mode

The burst mode can be used to read or write several registers instead of reading just single registers. The burst mode command consists of several bit fields and is shown in Table 11.

Table 11 Burst mode command

Field	Bit width	Bit field name	Description
15:9	7	addr	Address to request burst mode = 0x7F
8	1	bit8	Bit to fill the 16-bit command = 1
7:1	7	saddr	Burst mode starting address
0	1	rwb	Burst mode read/write 0 – burst read 1 – burst write

Burst command examples:

- Burst command for start read from register 4: 0xFF08
- Burst command for start write from register 7: 0xFF0F

After the start condition, the 16-bit burst mode command is sent from the SPI master on SPIDI. At the same time, the status register GSR0 (8-bit) and 8-bit dummy data are shifted out on SPIDO. After the command sequence is done, in burst write mode, the write burst data are shifted in from the SPI master on SPIDI or the read burst data are shifted out to the SPI master on SPIDO in burst read mode.
For burst accesses, any number of written/read data blocks can be used. The access is ended by a rising edge of SPICS.

Burst mode read sequence:

In the burst read sequence, the SPI master reads from the device.

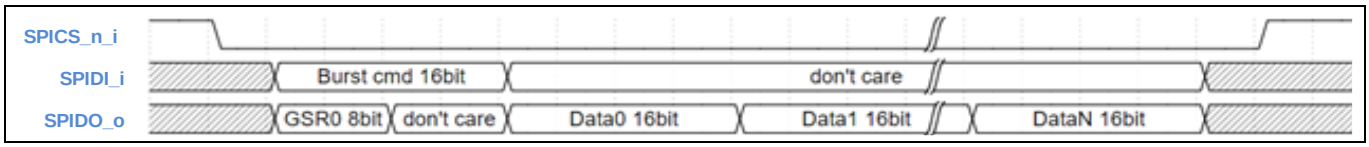


Figure 49 SPI burst read

Burst mode write sequence:

In the burst write mode, the SPI master writes to the device.

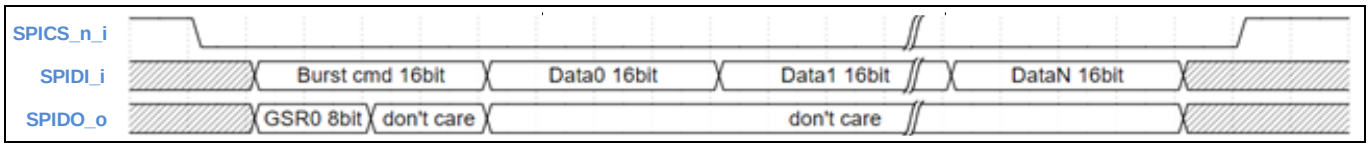


Figure 50 SPI burst write

6.2 SPI registers

This section gives a detailed overview of all the SPI registers in the chip and describes the functionality of the register bit fields in detail.

6.2.1 Register overview

The SPI module in the BGT24LTR22 MMIC includes several registers, which can be configured by the host. Table 12 gives an overview of all the registers. The following sections describe the bit arrangement of each of the registers and explain their functionality in detail.

Table 12 SPI register map overview, including reset values

Register	Mode	Function	Reset value
Register 0	RW	VCO and frequency divider control	0x0000
Register 1	RW	Transmitter control – TX1	0x0000
Register 2	RW	Power detectors and slave mode buffers control – TX1	0x0000
Register 3	RW	Transmitter control – TX2	0x0000
Register 4	RW	Power detectors and slave mode buffers control – TX2	0x0000
Register 5	RW	Receiver RF front-end control – RX1	0x0000
Register 6	RW	ABB unit control – RX1	0x0000
Register 7	RW	Receiver RF front-end control – RX2	0x0000
Register 8	RW	ABB unit control – RX2	0x0000
Register 9	RW	Transmitter bandgap biasing circuit	0x0000
Register 10	RW	LO distribution network	0x0000
Register 11	RW	PTAT voltage source control	0x8000
Register 14	RW	Built-in self-test block – 1 (only for internal use)	0x0000
Register 15	RW	Built-in self-test block – 2 (only for internal use)	0x0000
Register 32	RW	PTAT voltage source selector	0x0000
Register 34	RW	ADC start and general bandgap circuit control	0x0000
Register 35	RW	ADC convert	0x0000
Register 36	RW	ADC status	0x0000
Register 38	RO	ADC result channel 0: TX1 block – MPA, power detector output	n/a
Register 39	RO	ADC result channel 1: TX1 block – transmitter, power detector output	n/a
Register 40	RO	ADC result channel 2: TX1 block – slave mode, sync buffer 3 power detector output	n/a
Register 41	RO	ADC result channel 3: TX2 block – MPA, power detector output	n/a
Register 42	RO	ADC result channel 4: TX2 block – transmitter, power detector output	n/a
Register 43	RO	ADC result channel 5: TX2 block – slave mode, sync buffer 3 power detector output	n/a
Registers 44 to 48	RO	ADC result channels 6 to 10: not used	n/a
Register 49	RO	Reference voltage output of the VCO temperature compensation network (internal use)	n/a

Register	Mode	Function	Reset value
Register 50	RO	PTAT voltage output (VPTAT)	n/a
Register 51	RO	External analog input test (internal use)	n/a
Register 52	RO	ADC bandgap voltage output (internal use)	n/a
Register 53	RO	Integrated on-chip temperature sensor output voltage	n/a
Register 54	RO	Internal use only – testing purpose – ECC data register with status and error bits	0x0000
Register 55	RO	Fused PTAT register settings for ISM band operation	0x0000
Register 57	RW	Internal use only – testing purpose – control bits for e-fuses	0x0000
Register 58	RW	Internal use only – testing purpose – PTAT fuse calibration value	0x0000
GSR0	RO	8-bit SPI status register (global status register 0)	0x0000

6.2.2 Bandgap and biasing circuitry

This section describes the register settings used to configure the bandgap and bias circuits of the chip. The bandgap and the bias network are key for enabling the chip. The following blocks directly depend on them for their operation:

- Transmitter amplifiers
- LO distribution network
- ADC

This is configured by the SPI register 9 and register 34. Figure 51 and Figure 52 show the bit arrangement of register 9 and register 34, respectively.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
n.u												en_sync_TX2_bias	en_sync_TX1_bias	en_PTAT_LowNoise Mode	en_bg_bias

Figure 51 Bit assignment – SPI register 9

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
n.u													en_block_ADC	en_bandgap	en_clk_ADC

Figure 52 Bit assignment – SPI register 34

Table 13 provides a functional description of all the register bits.

Table 13 SPI register 9 – functional description

Field	Bit	Type	Description
n.u	[15:4]	RW	Not used
en_sync_TX2_bias	3	RW	Enables the biasing for sync section – TX2 0_B = disabled 1_B = enabled
en_sync_TX1_bias	2	RW	Enables the biasing for sync section – TX1 0_B = disabled 1_B = enabled
en_PTAT_Low_Noise_Mode	1	RW	Enables the PTAT output buffer 0_B = disabled 1_B = enabled Must be always enabled when using the PTAT output for V_{TUNE}
en_bg_bias	0	RW	Enable/disable the bandgap/biasing circuitry of the TX, LO distribution network and ABB 0_B = disabled 1_B = enabled

Table 14 provides a functional description of all the register bits.

Table 14 SPI register 34 – functional description

Field	Bit	Type	Description
n.u	[15:3]	RW	Not used
en_block_ADC	2	RW	Enable/disable ADC block 0_B = disabled 1_B = enabled
en_bandgap	1	RW	Enable/disable bandgap 0_B = disabled 1_B = enabled
en_clk_ADC	0	RW	Enable/disable ADC clock 0_B = disabled 1_B = enabled

6.2.3 VCO, frequency divider and PTAT control

This section presents the bit arrangement of the registers used to configure the signal generation and frequency control unit and describes in detail the functionality of each of the register bits. Figure 53 shows a simplified block diagram of all the controllable blocks of the signal generation circuit with the integrated

prescaler and PTAT voltage generator for autonomous ISM band operation. Register 0, register 11 and register 32 are together used to control all the functions of the signal generation unit.

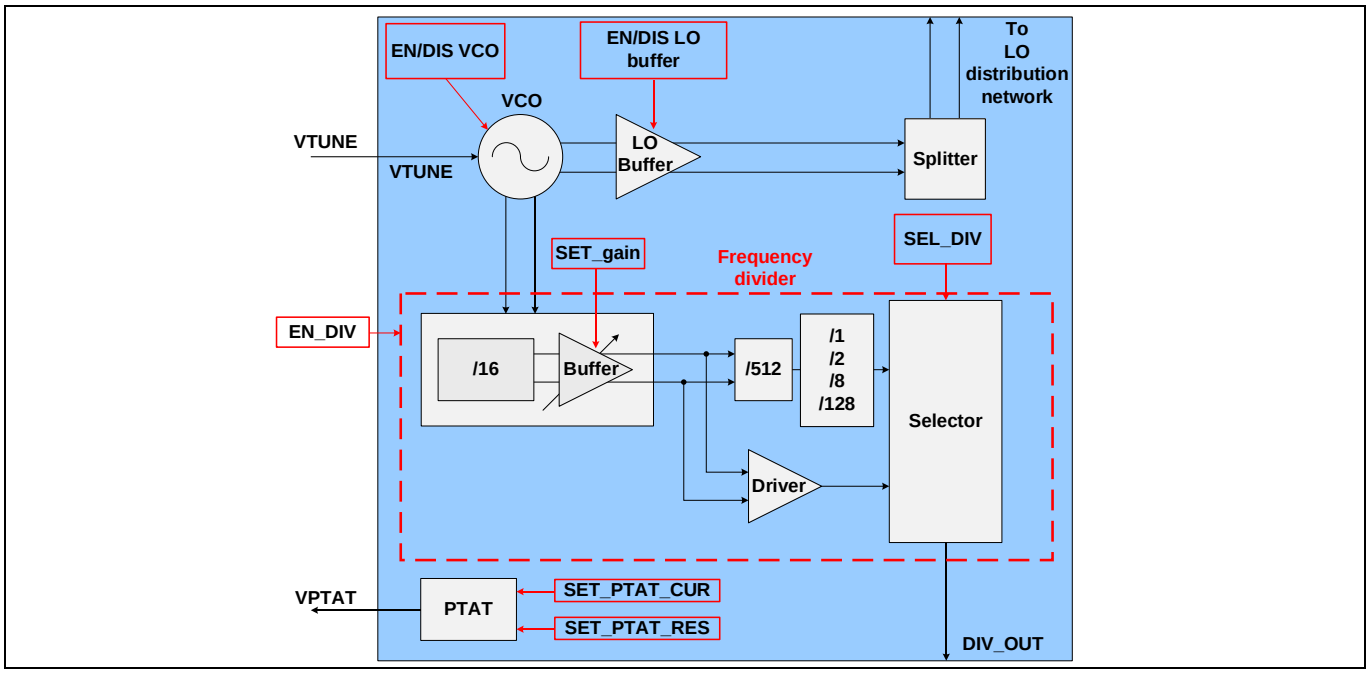


Figure 53 Signal generation unit – blocks controlled by register 0 and register 11

Figure 54 to Figure 56 show the bit assignment for registers 0, 11 and 32, respectively.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
n.u	n.u	n.u	n.u	n.u	n.u	n.u	n.u	n.u	en_divider_bias	en_div16_buffer	en_divL	divL_select [1:0]		en_VCO_buffer	en_VCO

Figure 54 Bit assignment – SPI register 0

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
set_VPTAT_Cur [15:8]								set_VPTAT_Res [7:0]							

Figure 55 Bit assignment – SPI register 11

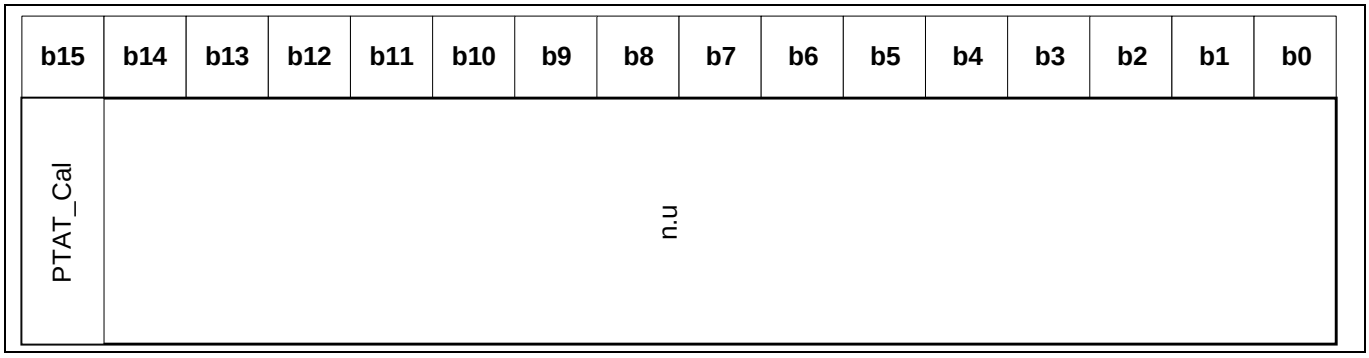


Figure 56 Bit assignment – SPI register 32

Register 0 mainly controls the VCO and the frequency divider block. Table 15 provides a functional description of all the register bits.

Table 15 SPI register 0 – functional description

Field	Bit	Type	Description
n.u	[15:7]	RW	Not used
en_divider_bias	6	RW	Enable/disable the bias circuit for the entire prescaler block 0_B = disabled 1_B = enabled
en_div16_buffer	5	RW	Enable/disable the high-frequency (/16) buffer amplifier 0_B = buffer disabled/Div16 unselected 1_B = buffer enabled/Div16 selected, DivL unselected
en_divL	4	RW	Enable/disable the low-frequency prescaler 0_B = disabled 1_B = enabled
divL_select	[3:2]	RW	Low-frequency divider – output frequency select 0_D = F_{OUT} = 2^13 1_D = F_{OUT} = 2^14 2_D = F_{OUT} = 2^16 3_D = F_{OUT} = 2^20
en_VCO_buffer	1	RW	Enable/disable VCO buffer 0_B = disabled 1_B = enabled
en_VCO	0	RW	Enable/disable VCO 0_B = disabled 1_B = enabled

The BGT24LTR22 device has an internal voltage generator block, which can be connected to the VTUNE port to tune the VCO into a desired frequency. Bits in the SPI register 11 are used to adjust this voltage output, which is available via the MMIC package pin VPTAT. For typical Doppler radar applications, the PTAT voltage source output is directly connected to the tuning port (V_{TUNE}) of the VCO via a simple filter circuit. In such applications, the PTAT control registers offer the possibility to digitally set the output frequency of the transceiver by

providing a digitally tunable output voltage via the VPTAT pin. The voltage, once set, changes proportionally with temperature, thereby keeping the output frequency of the transceiver within the desired ISM band.

Each BGT24LTR22 device is fused in the factory before shipment to provide a PTAT voltage at the VPTAT pin, which when applied to the VTUNE port of the device will automatically put the device into an ISM band frequency of operation. These settings are fused into register 55 of the device. In order to bypass the register 11 settings and load the default factory settings for ISM band operation, bit 15 of register 32 must be set to 1. Doing this enables loading of the factory calibrated settings for the PTAT voltage source. The output voltage from the PTAT source can always be monitored via the integrated ADC on register 50 – channel 12.

Table 16 provides a functional description of register 11.

Table 16 SPI register 11 – functional description

Field	Bit	Type	Description
set_VPTAT_Current	[15:8]	RW	V_{PTAT} current value setting for output frequency adjustment 0_D to 255_D Default value = 10000000
set_VPTAT_Res	[7:0]	RW	V_{PTAT} resistor value setting for output frequency adjustment 0_D to 255_D

Table 17 provides a functional description of register 32. It is mandatory to enable bit 15 of register 32 to load the factory-calibrated settings for the PTAT voltage source. Also, during the entire operation of the device with the PTAT voltage source, the register 9 – bit 1 must be kept enabled. This basically enables a buffer amplifier placed internally at the output of the PTAT voltage source, which minimizes noise from the internal PTAT circuitry.

Table 17 SPI register 32 – functional description

Field	Bit	Type	Description
PTAT_Cal	[15]	RW	V_{PTAT} output voltage settings 0_B = V_{PTAT} output chosen by register 11 settings 1_B = V_{PTAT} output chosen from factory-calibrated ISM band settings in register 55

6.2.4 LO distribution network

BGT24LTR22 consists of a highly configurable LO signal distribution network, which distributes the high-frequency signal generated by the VCO to all the other blocks of the MMIC. A simplified block diagram of the LO distribution network with all configurable blocks is shown in Figure 57.

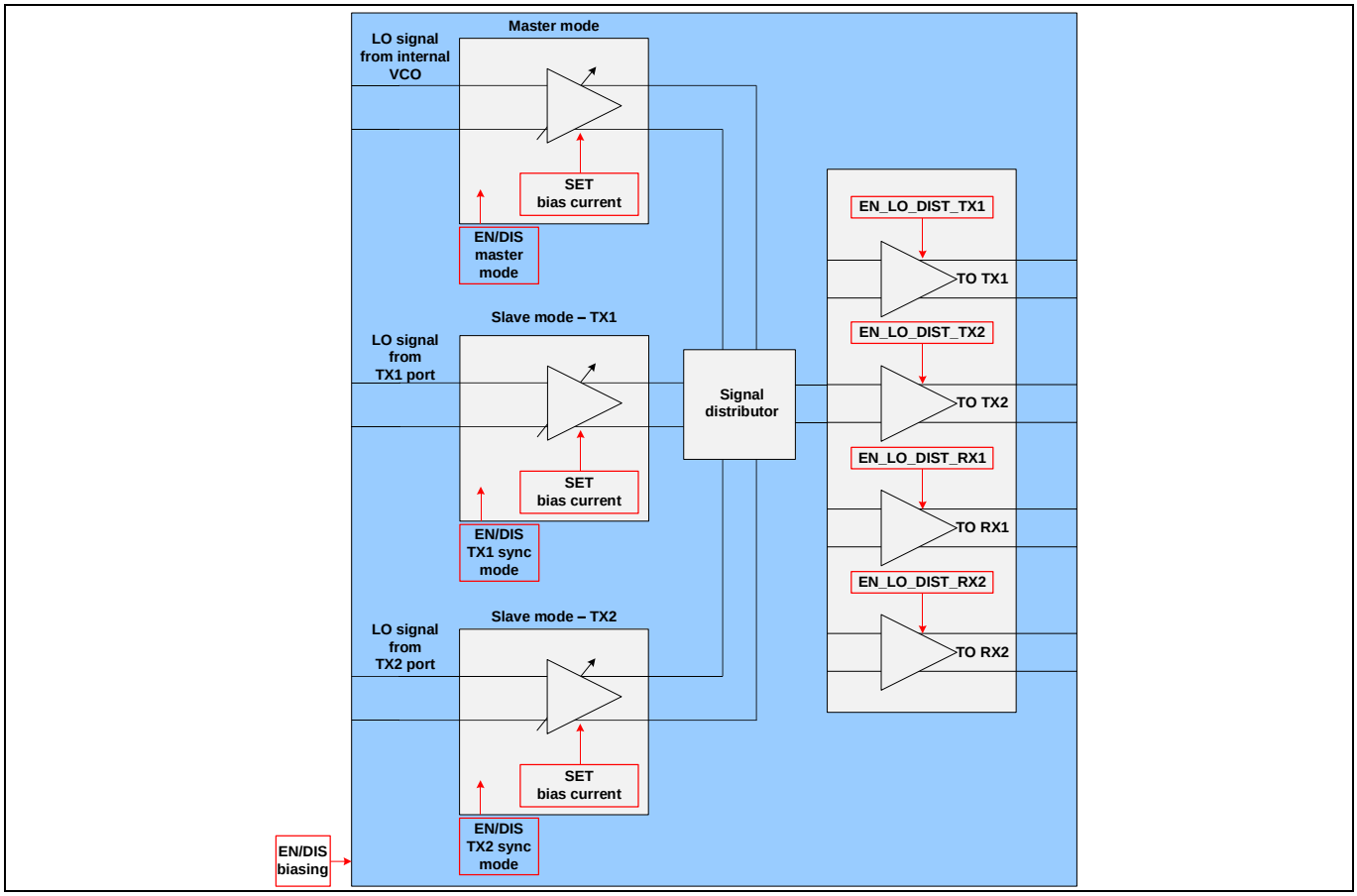


Figure 57 LO distribution network – blocks controlled by register 10

The SPI register 10 controls all the functions of the LO distribution network. Bits in this particular register are used to set the MMIC operating mode presented in Table 10 and effectively distribute the LO signal inside the chip. Figure 58 shows the bit assignment for register 10.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
n.u	en_LO_dist_TX2	en_LO_dist_TX1	en_LO_dist_RX2	en_LO_dist_RX1	Set_Bias_Current Slave_Mode [1:0] TX2		en_Slave_Mode TX2	Set_Bias_Current Slave_Mode [1:0] TX1		en_Slave_Mode TX1	Set_Bias_Current Master_Mode [1:0]		en_Master_Mode	n.u	en_biasing

Figure 58 Bit assignment – SPI register 10

Table 18 provides a functional description of all the register bits.

Table 18 SPI register 10 – functional description

Field	Bit	Type	Description
n.u	15	RW	Not used

Field	Bit	Type	Description
en_LO_dist_TX2	14	RW	Enable/disable the LO distribution network connected to TX2 0_B = disabled 1_B = enabled
en_LO_dist_TX1	13	RW	Enable/disable the LO distribution network connected to TX1 0_B = disabled 1_B = enabled
en_LO_dist_RX2	12	RW	Enable/disable the LO distribution network connected to RX2 0_B = disabled 1_B = enabled
en_LO_dist_RX1	11	RW	Enable/disable the LO distribution network connected to RX1 0_B = disabled 1_B = enabled
sen_Bias_Current_Slave_Mode_TX2	[10:9]	RW	Set the bias current of the LO distribution network in slave mode to TX2 0_D = 0 mA 1_D = 1 mA 2_D = 2 mA 3_D = 3 mA
en_SlaveMode_TX2	8	RW	Enable twin receiver only operating mode with LO input via TX2 port 0_B = disabled 1_B = enabled
set_Bias_Current_Slave_Mode_TX1	[7:6]	RW	Set the bias current of the LO distribution network in slave mode to TX1 0_D = 0 mA 1_D = 1 mA 2_D = 2 mA 3_D = 3 mA
en_SlaveMode_TX1	5	RW	Enable the twin receiver only operating mode with LO input via TX1 port 0_B = disabled 1_B = enabled
Set_Bias_Current_Master_Mode	[4:3]	RW	Set the bias current of the LO distribution network in master mode 0_D = 0 mA 1_D = 1 mA 2_D = 2 mA 3_D = 3 mA

Field	Bit	Type	Description
en_Master_Mode	2	RW	Enable master mode operation. MMIC operates in the two transmit and two receive modes. 0_B = disabled 1_B = enabled
n.u	1	RW	Not used
en_biasing	0	RW	Enable biasing for the LO distribution network 0_B = disabled 1_B = enabled

Note: To enable the LO distribution network biasing, all the bandgap and biasing circuits described in Section 6.2.2 must be enabled.

6.2.5 Transmitter/sync port section

The BGT24LTR22 MMIC consists of two high-frequency transmitter outputs. Figure 59 shows a simplified block diagram of one such unit with all the configurable blocks.

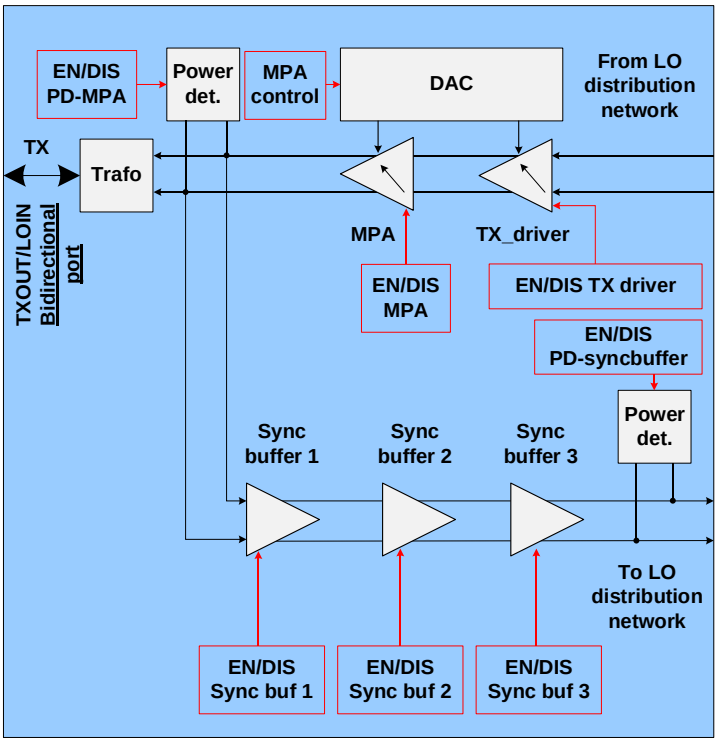


Figure 59 Transmitter/sync network circuitry – blocks controlled by registers 1, 3 and registers 2, 4

The transmitter section is bidirectional and, depending on the operating mode, can be used either to transmit a 24 GHz output signal (master mode) or act as a LO input port for twin receiver only operation (slave/cascade mode). When used in slave mode, the entire transmitting portion including the TX_driver, MPA and VCO must be disabled, and the sync buffer amplifiers must be enabled to amplify and distribute the input high-frequency LO signal. SPI register 1 and register 3 are used to control TX1 and TX2 independently when used in the master mode. Both registers have the same bit assignment, and hence only one of them will be described below. Figure 60 shows the bit assignment common to register 1 and register 3.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
n.u	n.u	n.u	n.u	n.u	n.u	TX_driver gain_ctrl [1:0]		mpa_power_ctrl [3:0]				en_DAC	en_MPA	n.u	en_TX_driver

Figure 60 Bit assignment – SPI register 1 and register 3

The transmitter output power of the MMIC can be controlled by adjusting the 4-bit DAC on the MPA and by configuring the gain of the TX_driver amplifier using a 2-bit logic. Table 19 provides a functional description of all the register bits.

Table 19 SPI register 1 and register 3 – functional description

Field	Bit	Type	Description
n.u	[15:10]	RW	Not used
txdrv_gain_ctrl	[9:8]	RW	Transmitter driver amplifier gain control 0_D = low 1_D = medium low 2_D = medium high 3_D = high
mpa_power_control	[7:4]	RW	Transmitter output power control 0_D = minimum 16_D = maximum
en_DAC	3	RW	Enable/disable the 4-bit DAC 0_B = disabled 1_B = enabled
en_MPA	2	RW	Enable/disable the MPA 0_B = disabled 1_B = enabled
n.u	1	RW	Not used
en_TX_driver	0	RW	Enable/disable the MPA driver 0_B = disabled 1_B = enabled

When the BGT24LTR22 is used in the slave/cascade mode, the entire transmitter unit must be turned off using the register 1 and register 3 bit settings, and the LO buffer signal amplification unit consisting of sync buffer 1, sync buffer 2 and sync buffer 3 must be enabled. The SPI register 2 and register 4 are used to configure the sync port buffer amplifiers corresponding to pins TX1 and TX2, respectively. Each bidirectional transmit section consists of integrated RF power detectors, as shown in Figure 44, which are also configured via register 2 and register 4. Both registers have the same bit assignment, and hence only one of them will be described. Figure 61 shows the bit assignment common to register 2 and register 4.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
n.u	n.u	n.u	n.u	n.u	n.u	n.u	en_sync_buf3	en_sync_buf2	en_sync_buf1	en_pd_sync_buf3	en_pd_MPA	n.u	n.u	n.u	n.u

Figure 61 Bit assignment – SPI register 2 and register 4

Table 20 provides a functional description of all the register bits.

Table 20 SPI register 2 and register 4 – functional description

Field	Bit	Type	Description
n.u	[15:9]	RW	Not used
en_sync_buf3	8	RW	Enable/disable sync buffer 3 0_B = disabled 1_B = enabled
en_sync_buf2	7	RW	Enable/disable sync buffer 2 0_B = disabled 1_B = enabled
en_sync_buf1	6	RW	Enable/disable sync buffer 1 0_B = disabled 1_B = enabled
en_pd_sync_buf3	5	RW	Enable/disable the power detector at the sync buffer 3 output 0_B = disabled 1_B = enabled
en_pd_MPA	4	RW	Enable/disable the power detector at the MPA output/sync port input 0_B = disabled 1_B = enabled
n.u	[3:0]	RW	Not used

6.2.6 Receiver RF front-end unit

The BGT24LTR22 MMIC consists of two integrated homodyne quadrature downconverter receiver front ends with a LNA and modified Gilbert-based downconverters. Figure 62 shows a simplified block diagram of the receiver RF front-end circuitry with the configurable blocks.

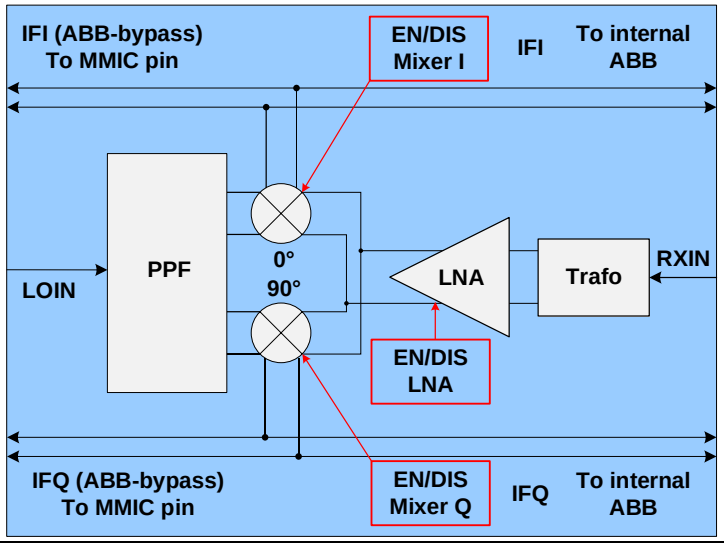


Figure 62 Receiver RF front-end blocks controlled by register 5 and register 7

The LNAs and the mixers of both the receiver front ends can be independently configured. SPI register 5 and register 7 are used for this purpose, corresponding to RX1 and RX2 respectively. Both registers have the same bit assignment and hence only one of them will be described. Figure 63 shows the bit assignment common to register 5 and register 7.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
n.u													en_Mixer_Qphase	en_Mixer_Inphase	en_LNA

Figure 63 Bit assignment – SPI register 5 and register 7

Table 21 provides a functional description of all the register bits.

Table 21 SPI register 5 and register 7 – functional description

Field	Bit	Type	Description
n.u	[15:3]	RW	Not used
en_Mixer_Q_Phase	2	RW	Enable/disable mixer – Q-channel 0_B = disabled 1_B = enabled
en_Mixer_I_Phase	1	RW	Enable/disable mixer – I-channel

Field	Bit	Type	Description
			0_B = disabled 1_B = enabled
en_LNA	0	RW	Enable/disable LNA 0_B = disabled 1_B = enabled

6.2.7 IF section – ABB unit

The BGT24LTR22 includes a highly integrated ABB section to process the low-frequency radar signals produced by the RF downconverter unit. The MMIC consists of four such ABB units, each corresponding to I- and Q-channels of the two receiver front ends. Figure 64 shows a simplified block diagram of one such ABB unit.

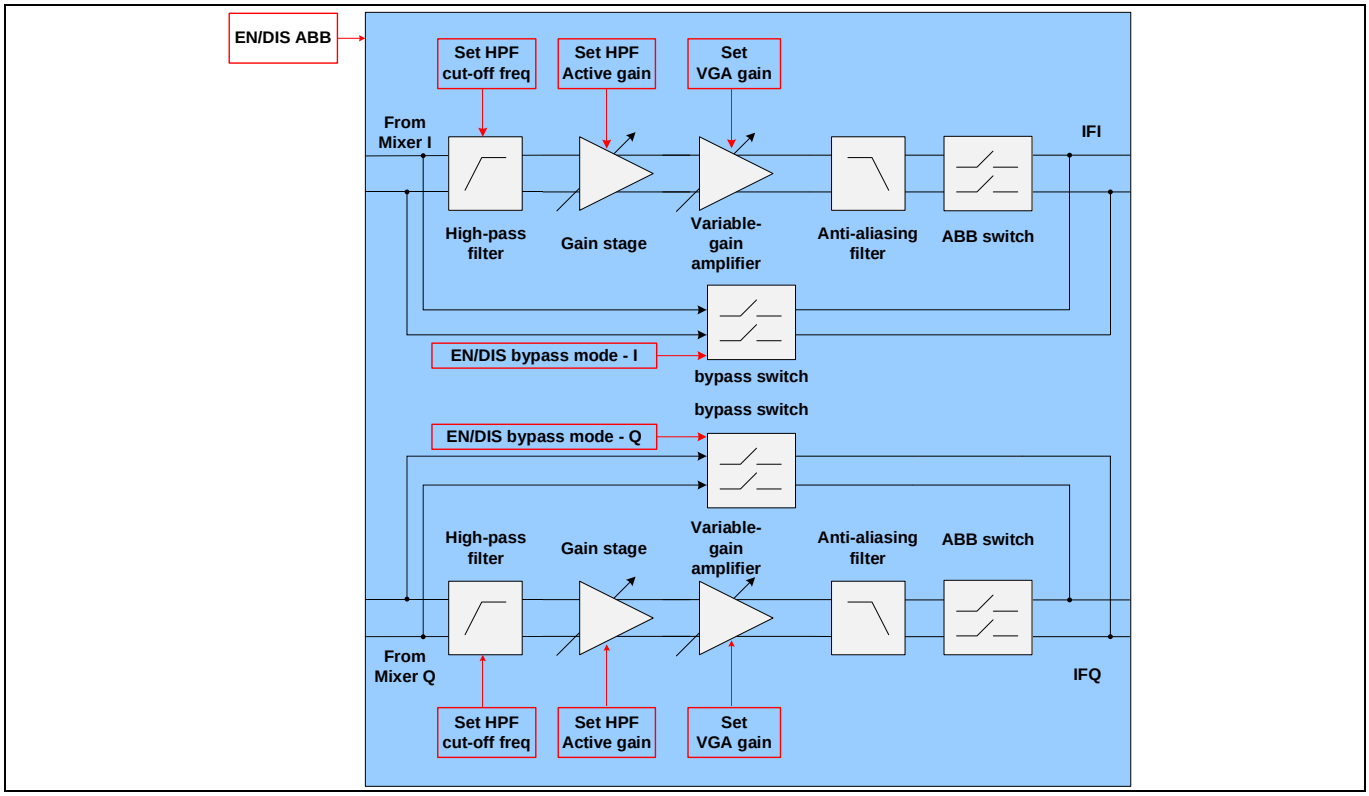


Figure 64 ABB unit – blocks controlled by register 6 and register 8

The ABB unit consists of a HPF with programmable cut-off frequencies followed by a configurable active gain stage. This is followed by a VGA with an integrated AAF. The ABB section is designed to process the IF signal from the RF receiver front end when the BGT24LTR22 MMIC is used in the FMCW radar mode. The arrangement of the functional blocks inside the ABB section enables strong amplification of a weak signal received from a radar target and simultaneously reduces the impact of the TX to RX crosstalk, which is a major concern in the FMCW radar system. Figure 65 shows the frequency response curve of a typical FMCW radar ABB section.

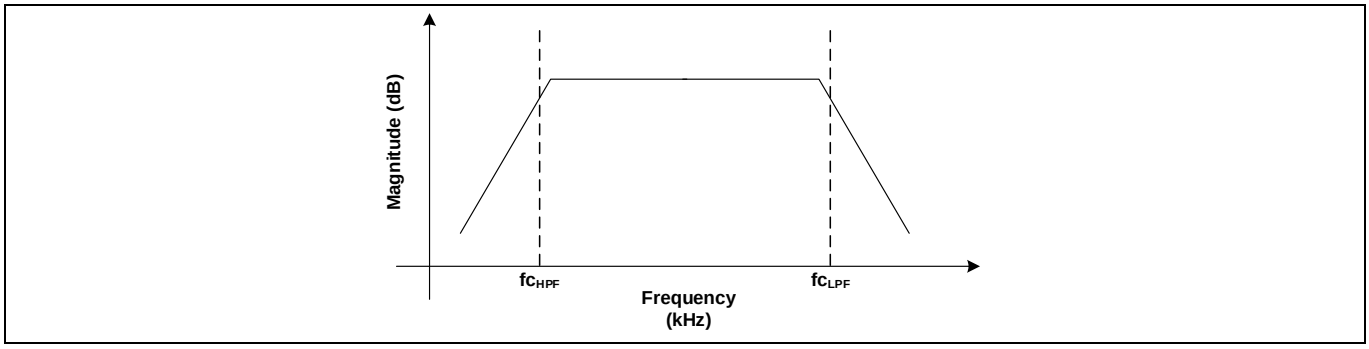


Figure 65 ABB unit – frequency response

Apart from range-Doppler analysis using FMCW radar, the BGT24LTR22 device can also be used for continuous-wave radar operation (Doppler mode) by enabling the bypass mode, wherein the entire ABB section can be bypassed and turned off. This provides direct access to the DC-coupled signals from the mixer of the device without any HPF. This also enables the processing of very low-frequency IF signals corresponding to the Doppler radar mode of operation, which otherwise would have been attenuated by the integrated HPF of the ABB section. The SPI register 6 and register 8 are used to configure all the parameters of the ABB section corresponding to receiver blocks RX1 and RX2, respectively. Both registers have the same bit assignment and hence only one of them will be described. Figure 66 shows the bit assignment common to register 6 and register 8.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
n.u	n.u	n.u	n.u	n.u	en_Bypass_Mode QPhase	en_Bypass_Mode InPhase	set_HPF_freq [1:0]		Set_VGA_Gain [2:0]			Reset_ABB	en_ABB_Qphase	en_ABB_InPhase	en_set_HPF Gain

Figure 66 Bit assignment – SPI register 6 and register 8

Table 22 provides a functional description of all the register bits.

Table 22 SPI register 6 and register 8 – functional description

Field	Bit	Type	Description
n.u	[15:11]	RW	Not used
en_Bypass_Mode_Q	10	RW	Enable/disable bypass mode – Q-channel 0_B = disabled 1_B = enabled
en_Bypass_Mode_I	9	RW	Enable/disable bypass mode – I-channel 0_B = disabled 1_B = enabled
set_HPF_freq	[8:7]	RW	Select the HPF cut-off frequency 0_D = 20 kHz 1_D = 50 kHz

Field	Bit	Type	Description
			2_D = 80 kHz 3_D = 100 kHz
set_ABB_Gain	[6:4]	RW	Configure the VGA gain 0_D = 0 dB 1_D = 5 dB 2_D = 10 dB 3_D = 15 dB 4_D = 20 dB 5_D = 25 dB 6_D = 30 dB
Reset_ABB	3	RW	Disable the ABB 0_B = disabled 1_B = enabled
en_ABB_Qphase	2	RW	Enable/disable the ABB Q-channel 0_B = disabled 1_B = enabled
en_ABB_Iphase	1	RW	Enable/disable the ABB I-channel 0_B = disabled 1_B = enabled
set_HPF_Gain	0	RW	Select the HPF gain stage value 0_B = 30 dB 1_B = 18 dB

6.2.8 Register GSR0 – SPI status register

The general status register – 0 provides an indication for a completed conversion by the ADC. Figure 67 shows the bit assignment of the GSR0 register, with a functional description in Table 23.

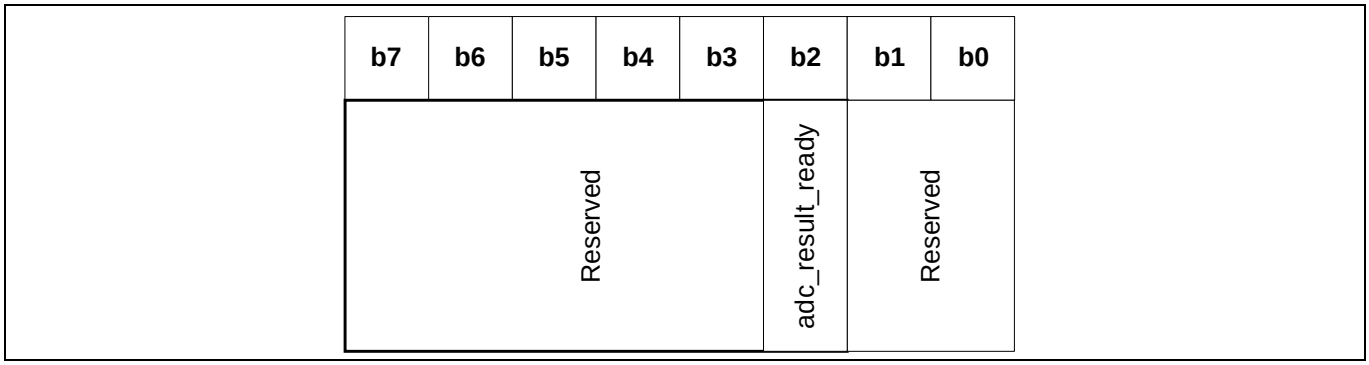


Figure 67 Bit assignment – SPI register GSR0

Table 23 Global status register 0 – functional description

Field	Bit	Type	Description
adc_result_ready	1	RO	ADC result ready Default: 0_B This flag indicates a completed conversion. In case all 16 channels are converted the flag goes to 1 as soon as all 16 conversions are finished. GSR0 is sent as the first 8 bits at every SPI access during transfer of address and RW bit. ADC result ready is reset after access to any of the result registers, register 38 to register 53. The result registers are overwritten only if the ADC conversion of the corresponding channel is restarted. 0_B: ADC still busy or already cleared by access to register 38 to register 53 1_B: result ready for readout

The global status register GSR0 is sent on `SPIDO_o` at the same time as the address and the read/write bit are sent on `SPIDI_i`, MSB leading. There is only one bit used, which is bit 2 “adc_result_ready.” This is a flag for completed conversion. It is cleared by reading out any result register (register 38 to register 53); the ADC clock must be enabled for that.

7 Analog to digital converter

BGT24LTR22 has several inbuilt sensors for measuring TX output power, LO output power, power detectors, MMIC backside temperature, bandgap voltages, VCO tuning voltage, etc. All of the sensor data outputs are accessed by an integrated 16-channel 8-bit ADC. The list of parameters which are accessible via the MMIC ADC is given in Table 24.

Table 24 BGT24LTR22 ADC output result channels

ADC result channel	Parameter
Channel 0 – register 38	MPA 1 power detector value – Power_MPA1
Channel 1 – register 39	MPA 1 reference power detector value – Power_TX1
Channel 2 – register 40	Slave mode operation – TX1 – sync buffer 3 output power detector value
Channel 3 – register 41	MPA 2 power detector value – Power_MPA2
Channel 4 – register 42	MPA 2 reference power detector value – Power_TX2
Channel 5 – register 43	Slave mode operation – TX2 – sync buffer 3 output power
Channel 6 – channel 10	Not used
Channel 11 – register 49	Internal reference voltage output of the VCO temperature compensation network (internal use)
Channel 12 – register 50	PTAT voltage output (V_{PTAT})
Channel 13 – register 51	External analog input for ADC test (only for internal use)
Channel 14 – register 52	ADC bandgap voltage output (internal use)
Channel 15 – register 53	Integrated on-chip temperature sensor output voltage

The ADC module is controlled by control and status bits. The following section describes the ADC conversion sequence in detail.

7.1 ADC conversion sequence

An ADC conversion process in the BGT24LTR22 MMIC typically consists of four phases:

1. Bandgap circuit enable
2. ADC clock enable
3. ADC core enable
4. ADC conversion enable

7.1.1 Enable bandgap

The ADC bandgap circuit is enabled by setting the bandgap_enable bit in register 34. This can be done simultaneously with clk_enable. The bandgap can be enabled or disabled independently of all other modules. The start-up time of the bandgap is temperature and device dependent. Enabling of the ADC is not allowed before the bg_up flag (register 36) is read out as high.

7.1.2 Enable local ADC clock

The local clock generator for the ADC is enabled by setting the clk_enable bit in register 34, without setting any other bits, except bandgap_enable.

7.1.3 Enable ADC

Before enabling the ADC block, the local clock and the bandgap must be available.

Register 34, bit adc_enable, enables the ADC. The adc_ready bit high indicates a finished start-up of the ADC. Conversion cannot be started before adc_ready = “1”.

7.1.4 Start ADC conversion

7.1.4.1 Single conversion

A conversion is started by a SPI write command into register 35, independent from the written data. During a running conversion, no further changes of these bits are allowed.

The ADC performs the following:

- Start a sampling phase
- Start a conversion phase
- Update the corresponding result register
- Set adc_result_ready bit to “1”

7.1.4.2 Sequential conversion

A conversion sequence for all input channels can be requested by writing register 35 with chnr_all set to “1”. In this case the ADC performs the following:

- Convert all 16 channels consecutively and update the corresponding result registers
- Set adc_result_ready bit to ‘1’

The adc_result_ready bit within GSR0 is cleared by reading any of the result registers (registers 38 to 53).

7.2 Conversion time

An example formula for calculation is provided below. Twelve additional clock cycles are needed for post-calibration.

Sampling time is 16 clock cycles. Distribution time (= actual conversion) is 13 clock cycles.

The ADC clock is generated internally and is dependent on temperature and chip sample (min. 15 MHz, max. 50 MHz).

$t_{conv} = (t_{sample} + tdistrib + tepcal) * tadc_clk = (16+13+12) * tadc_clk$

$t_{conv_min} = (t_{sample} + tdistrib + tepcal) * tadc_clk_50M = (16+13+12) * (1/50e^{6}) = 0.82\ \mu s$

$t_{conv_max} = (t_{sample} + tdistrib + tepcal) * tadc_clk_15M = (16+13+12) * (1/15e^{6}) = 2.73\ \mu s$

7.3 ADC power-down sequence

In case a low current consumption mode is required, a full ADC power-down can be invoked in two phases:

1. Disable ADC by setting adc_enable to “0”. The clock must still be running to enable the FSMs to switch to a defined state.
2. Disable clock by setting clock_enable to “0”.

Bandgap can be disabled separately by setting bandgap_enable to “0”. This can be done after step 1 or after step 2.

7.4 ADC registers

Table 25 lists all the registers used to control the ADC modules and read its status.

Table 25 ADC control and status registers

SPI register	Function
Register 34	ADC control register to enable/start the ADC
Register 35	ADC control register to trigger conversion and set all conversion-related parameters
Register 36	ADC status indicator register responsible for the following: – Indicating that ADC is ready to work – Indicating that ADC bandgap is running

The following sections will describe the control and status registers’ bit assignment and functionality in detail.

7.4.1 Register 34 – ADC control

Figure 68 shows the bit assignment of the ADC control register 34.

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Reserved													en_ADC	en_bandgap_ADC	en_clk_ADC

Figure 68 Bit assignment – SPI register 34

Table 26 provides a functional description of the register bits.

Table 26 SPI register 34 – functional description

Field	Bit	Type	Description
Reserved	[15:3]	RW	Reserved for internal use
adc_enable	2	RW	Enable/disable ADC block 0_B: ADC disabled 1_B: ADC enabled Default: 0_B
en_bandgap_ADC	1	RW	Enable/disable ADC bandgap 0_B: ADC disabled 1_B: ADC enabled Default: 0_B = disabled

Field	Bit	Type	Description
en_clk_ADC	0	RW	Enable/disable ADC clock 0_B: ADC disabled 1_B: ADC enabled Default: 0_B

7.4.2 Register 35 – ADC control

Figure 69 shows the bit assignment of the ADC control register 35.

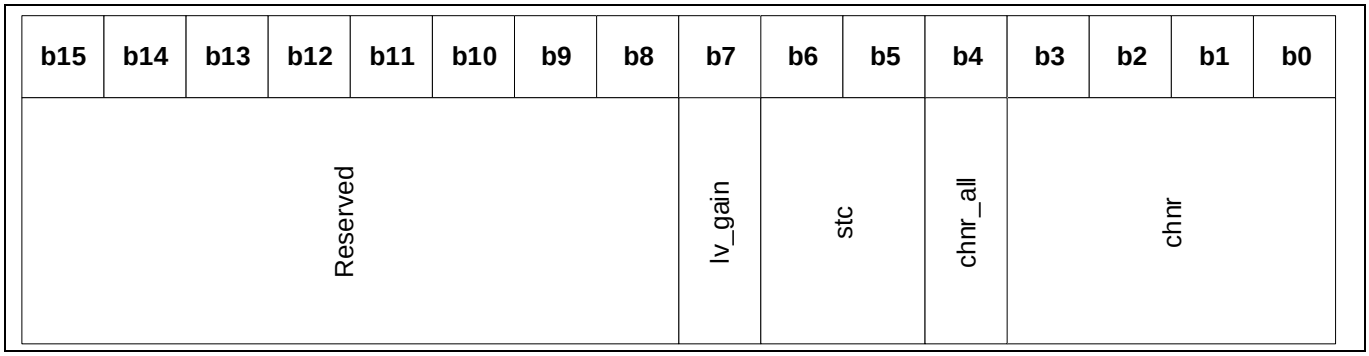


Figure 69 Bit assignment – SPI register 35

Table 27 provides a functional description of the register bits.

Table 27 SPI register 35 – functional description

Field	Bit	Type	Description
Reserved	[15:8]	RW	Reserved for internal use
lv_gain	7	RW	Set gain configuration for all the ADCs' analog input channels 0_B: gain = 0.75, full-scale analog input voltage 1.613 V 1_B: gain = 1.00, full-scale analog input voltage 1.21 V Default: 0_B
stc	[6:5]	RW	Set sampling time of the analog input voltage During the first phase, the analog input voltage is sampled onto the DAC capacitor. This phase is called the sampling phase. The duration of this phase is controlled by the STC bits. 0D = 16 clock counts (fixed value)
chnr_all	4	RW	Conversion channel selection 0_B = channels to convert is selected using the bits specified in the chnr bit field 1_B = all ADC conversion channels are selected and the chnr bit fields are ignored Default = 1_B
chnr	[3:0]	RW	Conversion channel number specification Selects the analog input channel number for sampling (0 to 15) – total 16 channels available Default = 0_D

7.4.3 Register 36 – ADC status

Figure 70 shows the bit assignment of the ADC status register 36.

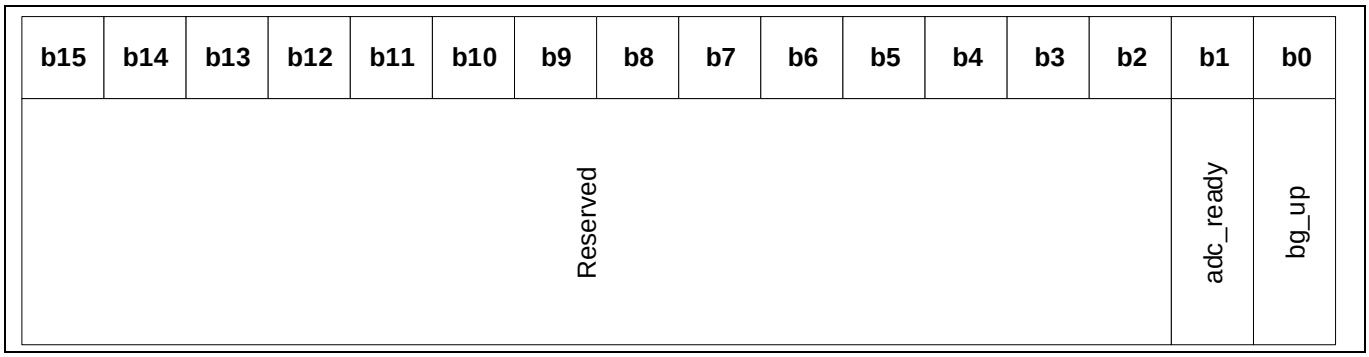


Figure 70 Bit assignment – SPI register 36

Table 28 provides a functional description of the register bits.

Table 28 SPI register 36 – functional description

Field	Bit	Type	Description
Reserved	[15:2]	RW	Reserved for internal use
adc_ready	1	RW	ADC ready flag This flag indicates if the ADC is ready to work 0_B = ADC not activated or still booting 1_B = ADC ready Default = 0_B
bg_up	0	RW	Bandgap operation indicator flag This flag indicates whether the bandgap is running or not 0_B = bandgap is not running or still booting 1_B = bandgap running Default = 0_B

7.4.4 Registers 38 to 53 – ADC result

All the conversion result bits of the ADC module are readable over the SPI bus through the registers 38 to 53 as described in Table 29. A typical result register bit assignment is shown in Figure 71 – the bit assignment is the same for all of the ADC result registers and hence only one block will be shown.

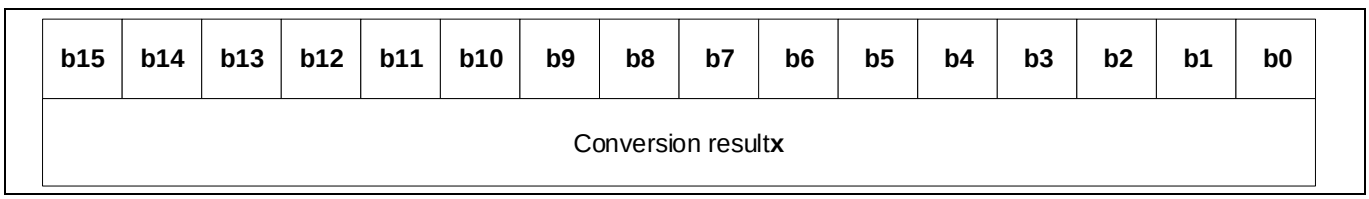


Figure 71 Bit assignment – SPI registers 38 to 53

Table 29 provides a functional description of the SPI registers 38 to 53.

Table 29 SPI registers 38 to 53 – functional description

Field	Bit	Type	Description
Conversion result	[15:0]	RO	Conversion result of an ADC channel X = 0 to 15 The registers are valid after an ADC conversion on any of the channels

References

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[2] Chakraborty et al., “A Scalable Multimode 24 GHz Radar Transceiver for Industrial and Consumer Applications in a 0.13 µm SiGe BiCMOS Technology” in Proc. IEEE BCICTS Conf. Nashville, Tennessee, USA, Nov. 2019PL.; Available online

Revision history

Document revision	Date	Description of changes
1.00	2021-08-27	Initial version
1.10	2023-02-09	Page 14 – Table 2 – RF port impedance values looking into the device for all RF ports updated
1.20	2023-02-14	Miscellaneous document cleanup updates
1.30	2025-04-15	Removed Section 4. MMIC evaluation board Changed document ID Editorial changes

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