EVAL_2EDF7268G_HB

Evaluation board description and getting started guide

About this document

Scope and purpose

This user guide introduces and provides an overview of the EVAL_2EDF7268G_HB gate driver evaluation board featuring the Infineon EiceDRIVER™ 2EDF7268G gate driver IC. The board allows testing of OptiMOS™ power transistor in a PG-TDSON-8 package. The board includes a bias supply circuit for the gate driver that can be configured for unipolar and bipolar supply (with regulation on positive or negative rail) or non-isolated for operation in bootstrap. Using an external inductor, the board can be configured for buck- or boost-mode, double-pulse testing or continuous PWM operation, hard- or soft-switching at output DC-link voltage levels up to 200 V**,** and frequencies up to MHz range.

Intended audience

This document is intended for all technical specialists who want to evaluate the functionality, performance, and features of 2EDF7268G gate driver ICs. The evaluation board is intended to be used under laboratory conditions only by trained specialists.

About this product group

Target applications

- Server, telecom DC-DC converters
- Low voltage drives and power tools
- Solar micro inverter, solar optimizer
- Industrial power supply (SMPS, residential UPS)

Product family

Infineon's EiceDRIVER™ gate driver ICs – spanning non-isolated and galvanically isolated single- and dual-channel solutions—deliver robust, efficient control of Si MOSFETs and GaN HEMTs. With high CMTI, precise timing, and comprehensive protection, the family enhances reliability, boosts power density, and reduces system cost across demanding power conversion and motor-drive designs.

Evaluation board

This board is to be used during the design-in process for evaluating the functionality and the performance of the gate driver IC.

Note: *The PCB and auxiliary circuits are NOT optimized for final customer design.*

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Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems.*

Table 1 Safety precautions

	**Warning:** *The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning***: The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 EVAL_2EDF7268G_HB evaluation board at a glance

The EVAL_2EDF7268G_HB evaluation board is designed to be used by engineers to evaluate the 2EDF7268G EiceDRIVER™ isolated gate driver ICs and discrete power switches from Infineon in a half-bridge configuration. The generic half-bridge topology is configurable for boost or buck operation, double-pulse testing or continuous PWM operation at full power. Test points provide access to connect signals to an oscilloscope for measuring the switching performance of OptiMOS™ power switches and gate driver ICs.

The board includes a HAQ-10T unassembled heatsink.

- **PWM** (see Section 2.2.2): The half-bridge circuit board can be controlled by two PWM signals provided via a pulse generator. The half-bridge dead-time is forced by the EiceDRIVER™ 2EDF7268G gate driver only if the dead-time between INA and INB is shorter than the minimum “safe dead-time” configured on the gate driver via the DTC pin
- **Supply** (see Sections 2.2 and 2.2.1): Gate-to-source voltages are generated if V_{CCI} supply is applied via the DC power supply on the primary side of the gate driver. Other power supply configurations also allow connection to external isolated power supplies to the gate driver secondary side, which then generate the gate-to-source voltages

The output and bus voltage can range up to 200 V. The operating frequency can be up to several MHz, depending on the thermal dissipation of the power switch and gate driver.

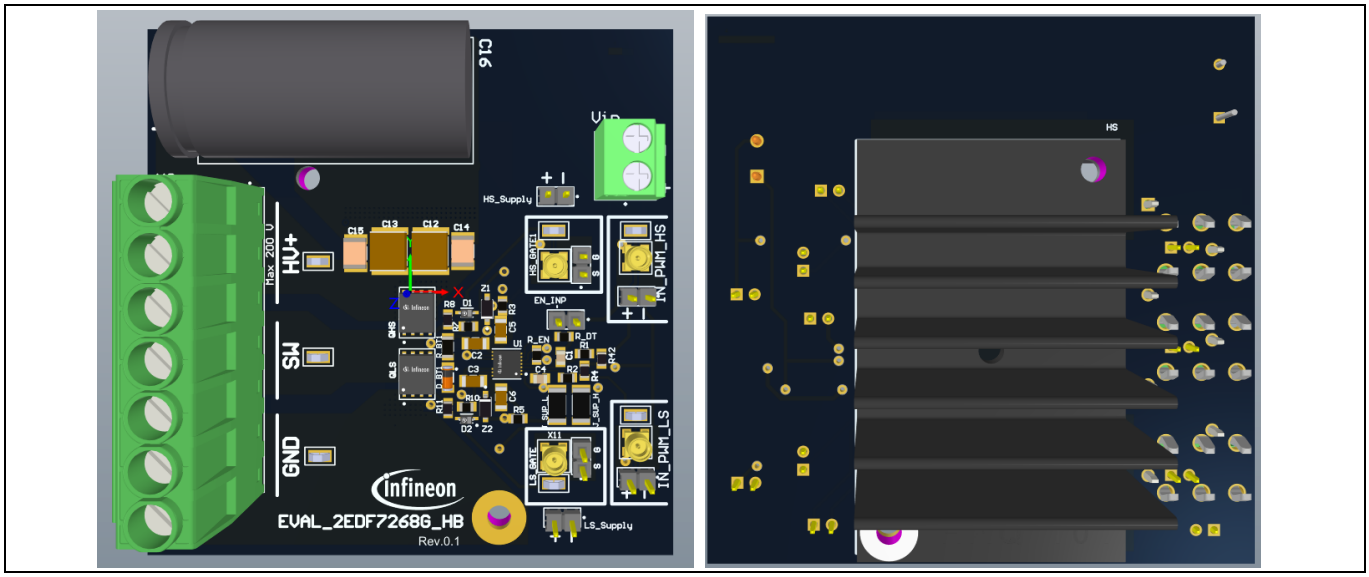

Figure 1 Front and back views of EVAL_2EDF7268G_HB

1.1 Scope of supply

The delivery contains:

- EVAL_2EDF7268G_HB evaluation board One HAQ-10T heatsink for assembly

1.2 Block diagram

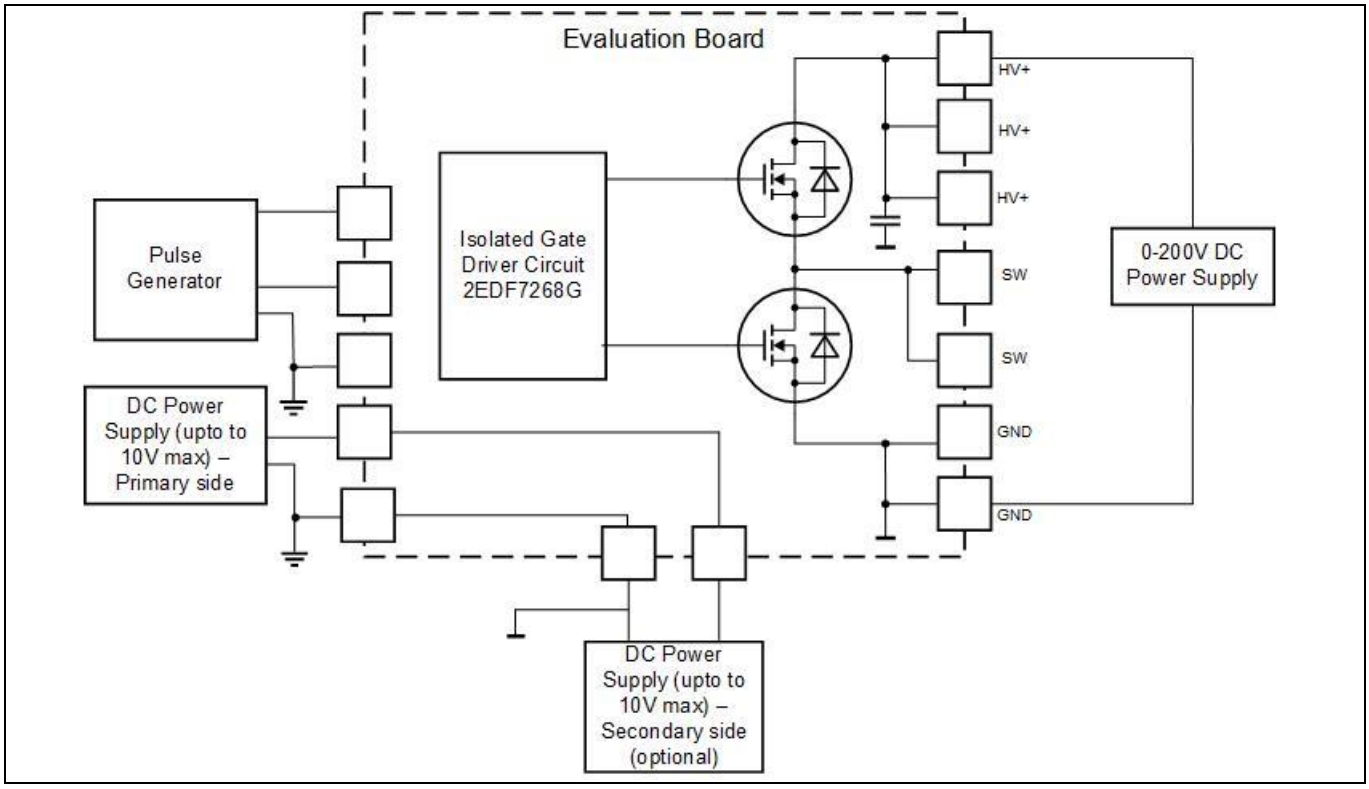

Figure 2 EVAL_2EDF7268G_HB block diagram

1.3 Main features

Infineon BSC600N25NS3 G 250 V OptiMOS™ N-channel MOSFETs in PG-TDSON-8-1 in a half-bridge configuration

- PCB layout designed to ensure optimal switching performance of the half-bridge
- In default configuration (non-isolated), a single external power supply is used to supply the input side as well as the output side of the gate driver. It can also be configured to have an independent isolated power supply for input and output side of the gate driver
- UVLO for all gate driver supply voltages
- Test points for monitoring critical signals

The main features of the 2EDF7268G gate driver are:

- Dual-channel isolated gate driver for Si MOSFETs and GaN HEMTs
- 5 A typical source current and 9 A typical sink current.
- High common-mode transient immunity (CMTI): 100 V/ns
- 22 V absolute maximum output supply voltage
- Undervoltage lockout for OptiMOS™ and GaN switches
- 10 K/$W_{RTH\ JB}$ (exposed pads)
- Fully qualified according to JEDEC for industrial applications
- 13-pin SON 4x4 mm with ≥ 1.2 mm spacing for optimal PCB footprint

1.4 Board parameters and technical data

Table 1 Evaluation board specifications

Parameter	Values			Unit	Note
	Min.	Typ.	Max.		
V_{CCI} input voltage	6.5	8	10	V	Max. value limited through a bypass capacitor
V_{CCI} input current			0.03	A	Max. considers potential operation at 2 MHz
INA, INB logic input levels	0	3.3	17	V	Typ. standard 3.3 V TTL levels
Vin+ to Vin-	0	150	200	V	Limited by gate driver output ch-to-ch creepage
Transistor current, DC	–	–	12	A	Keep case temperature below 125°C
Transistor current, pulse	–	–	35	A	Keep case temperature below 125°C
Operating frequency	–	–	2	MHz	Within thermal dissipation and temperature limits
PWM pulse width	18	–	–	ns	Min. value set by the gate driver
Switching node VSW speed	–	87	–	V/ns	20–80% for 0 A hard-switching, default config
Gate drive voltage levels	–	3.3	–	V	Min. is adjustable via supply configuration and Cc value
Dead-time adjustment range	10	100	1000	ns	Typical value set by driver DTC resistance (R_DT)

Note: The PCB dimensions are 7.7 cm x 7.7 cm.

2 System and functional description

2.1 Getting started

The EVAL_2EDF7268G_HB evaluation board is designed for convenient testing of the gate driver functionality and switching performance of the gate driver and power transistor in a half-bridge configuration. All the necessary supply voltages required to power the gate driver, including both input-side and output-side voltages, are to be provided externally to the board. To eliminate the need for multiple external power supplies and reduce setup complexity, the default configuration (non-isolated) consists of a single external power supply to power the input side of gate driver, the high-side output and the low-side output supplies of the gate driver. This allows users to focus on evaluation and testing. The board is designed to support voltages up to 10 V for the gate driver input supply voltage.

For the output-side supply voltages of the high-side and low-side gate drivers are supplied from the same voltage applied to the gate driver input supply voltage. The output side supply voltages can however be supplied independent of the input side of gate driver by depopulating the resistors J_SUP_H and J_SUP_L.

Similarly, the gate driver output high side can be supplied independent of the gate driver output low side supply by depopulating the R_BT1 resistor. In the default configuration the gate driver output side supplies are set up in a bootstrap configuration.

2.1.1 Prerequisites

- A low-voltage power supply for supplying the input voltage of the board, capable of supplying up to 20 V and 500 mA
- Suitable pulse generator for providing input PWM signals
- High-voltage power supply for supplying the power stage via X2 (HV+) and X2 (GND)
- A suitable inductive load

2.1.2 Power-up sequence

- Connect the signal generator to the input pins of the board: PWMH (IN_PWM_HS) and PWMH (GNDI) for the high-side of gate driver and PWML (IN_PWM_LS) and PWML (GNDI) for the low-side of gate driver. Connect one end of the load to terminal X2 (SW) and the other end to terminal X2 (GND). To perform double-pulse test measurements, connect one end of the inductive load to terminal X2 (SW) and the other end, depending on the double-pulse test requirements, to either X2 (HV+) for low-side testing or X2 (GND) for high-side testing. Connect the high-voltage power supply to the X2 (HV+) terminal and the power ground to the X2 (GND) terminal
- Connect the low-voltage input supply for the board, VDD at the connector Vin, and configure the required bias supply configuration (see Section 2.1.3)

2.1.3 Selecting the driving setup: unipolar vs. bipolar, isolated vs. bootstrap

The board can be configured for MOSFET or GaN operation with unipolar or bipolar gate-to-source voltage, with isolated or non-isolated supply domains, with or without bootstrap as shown in Table 2. The graphical explanation is shown in Figure 2.

Table 2 Bias supply configurations

Config. #	Unipolar vs. bipolar driving		Low-side supplied via		High-side supplied via		Pri-sec isolation
	Unipolar	Bipolar	V_{CCI}	Iso aux	bootstrap	Iso aux	
A (default)		x	x		x		
B		x		x	x		x
C		x		x		x	x
D	x			x	x		x

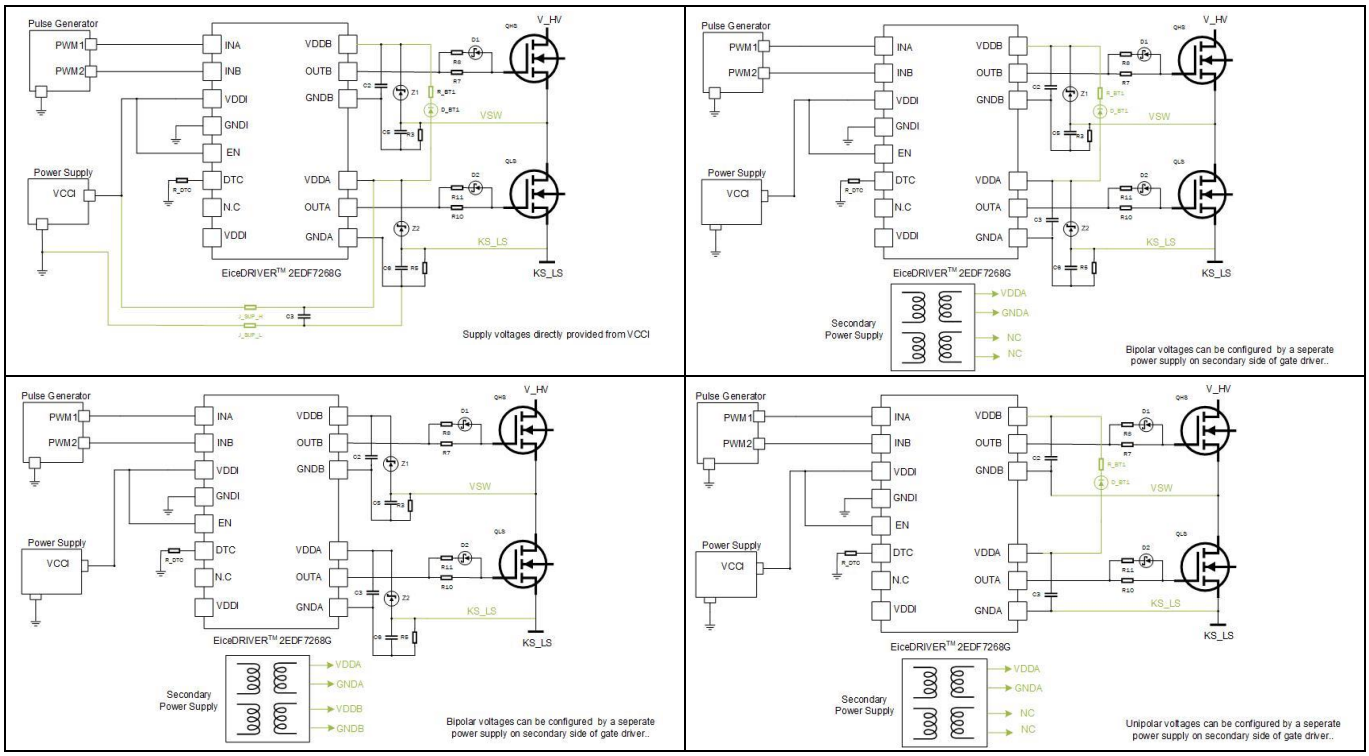

Figure 3 Bias supply configurations – graphical explanation

The desired bias supply configuration can be set by means of populating or depopulating components as shown in Table 3.

Table 3 Jumper selection (“x” stands for populating or soldering the component)

Configuration	J_SUP_H	J_SUP_L	R_BT1	D_BT1	Z1	Z2	C5	C8	R3	R5
A (default)	x	x	x	x	x	x	x	x	x	x
B			x	x	x	x	x	x	x	x
C					x	x	x	x	x	x
D[1]			x	x					x	x

2.2 Sample measurement results

The gate driver supplies are set up in default ‘Configuration A’ as described in Section 2.1.3.

2.2.1 Startup behavior

The board is powered up with the gate drivers in a non-switching state.

2.2.2 Dead-time setup

EiceDRIVER™ 2EDF7268G includes a dead-time control (DTC) and shoot-through protection (STP) that can be activated by means of the resistance R_DT. The driver’s dead-time is set according to the following equation:

$$t_{DT}(ns) = 10 \times R\_DT(k\Omega)$$

Equation 1

A standard 0 to 10 V pulse generator can be used to generate the logic PWM signals; 50 Ω load setting should be considered. The PWMs signals can be applied to INA and INB board connectors via coaxial cables.
The half-bridge dead-time replicates INA and INB dead time unless this is shorter than the “safe dead-time” set on the driver via R_DT.

For example, in Figure 3, the dead-time set on the driver is 100 ns (R_DT = 10 kΩ); because INA and INB dead time are longer (220 ns), the latter (220 ns) is replicated on the gate-to-source signals. In Figure 4 instead, complementary INA and INB are considered with no dead-time; therefore, the driver dead-time of 46 ns (R_DT= 4.6 kΩ) is forced.

The 2EDF series dead-time therefore implements a “first level of protection against half-bridge shoot-through” ensuring no logic overlap due to incorrect programming or noise on the input traces. It is important to highlight that half-bridge shoot-through could still happen due to induced noise on the gate-to-source voltage when the switching node commutates (Miller effect); this can be controlled by proper dimensioning of the negative VGS in off state.

[1] In configuration D, replace the value of R3 and R5 with a 0 Ω jumper to directly connect the Kelvin source of high-side and low-side switches to the respective GNDs.

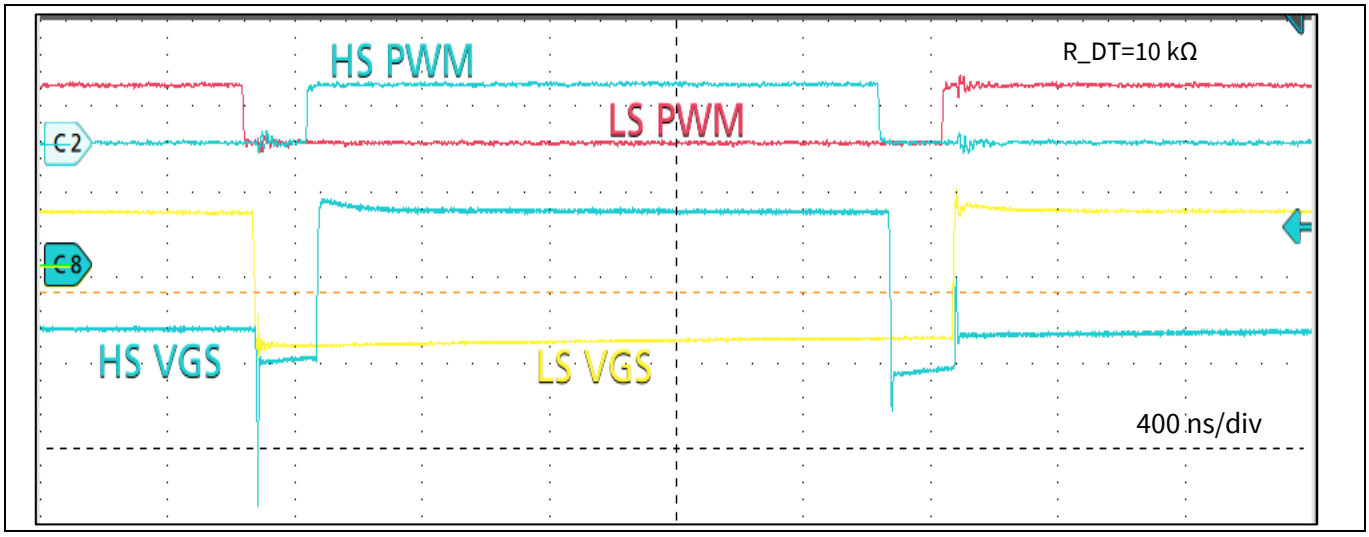

Figure 4 **Example of gate-to-source voltage dead-time set by PWM signals (R_DT=10 kΩ, PWM signals with 220 ns dead-time)**

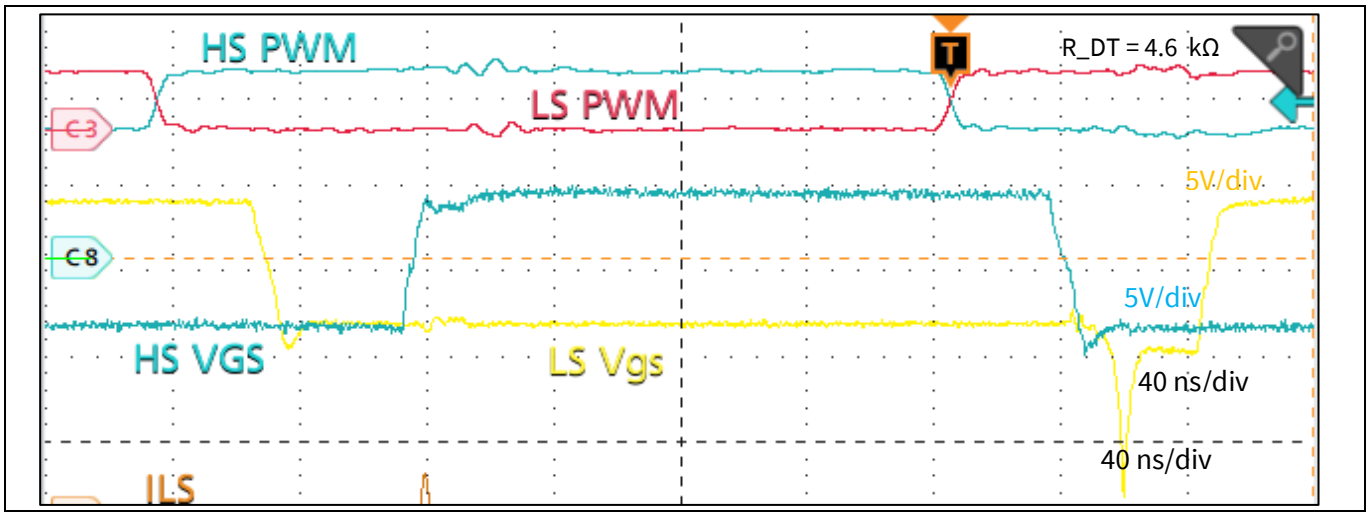

Figure 5 **Example of gate-to-source voltage dead-time set by PWM signals (R_DT=4.6 kΩ, PWM signals with 220 ns dead-time)**

3 System design

Note: See the EVAL_2EDF7268G_HB evaluation board's homepage for comprehensive design support including the schematic, Gerber files, BOM, and the complete Altium Designer project files.

3.1 Schematics

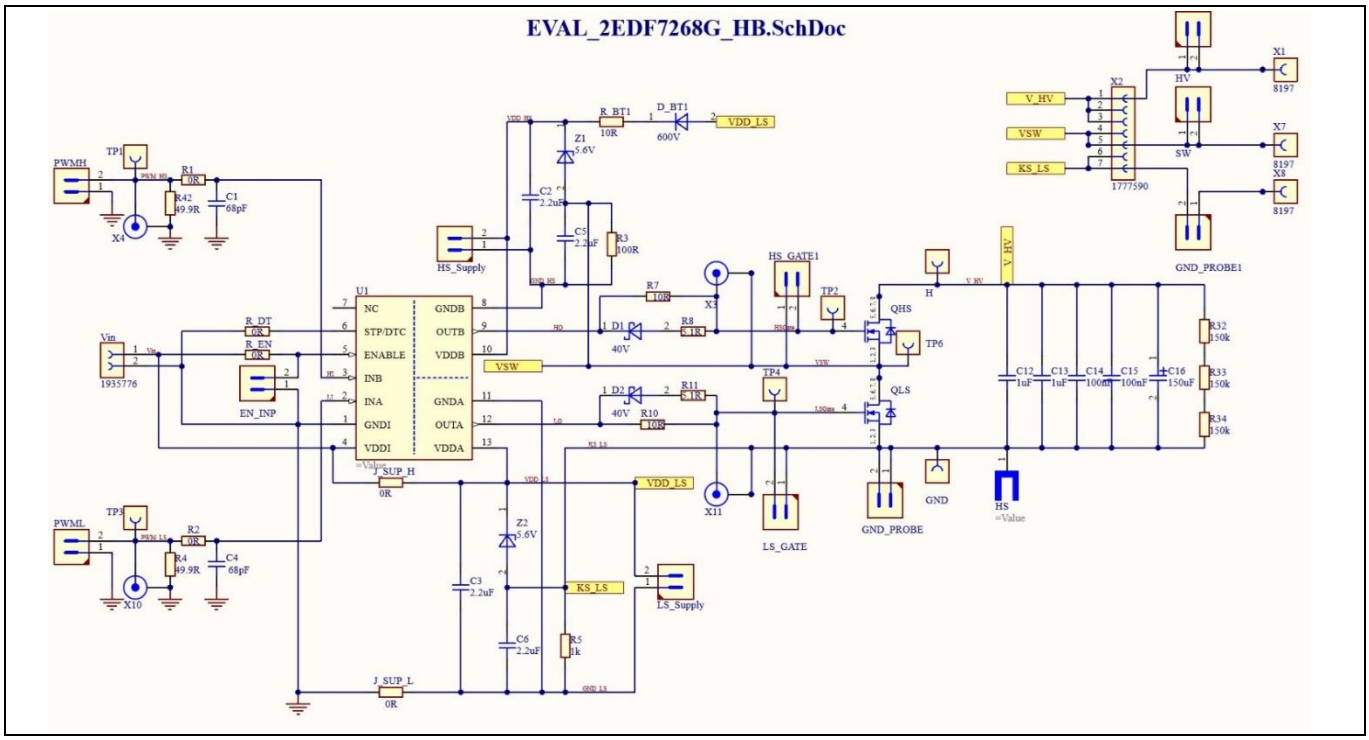

Figure 6 Schematic of EVAL_2EDF7268G_HB evaluation board

3.2 Layout

The EVAL_2EDF7268G_HB is evaluation board is designed on a 4-layer PCB with 70 µm copper thickness. The top and the bottom view of the PCB layout as well as the copper layers of the PCB are shown below.

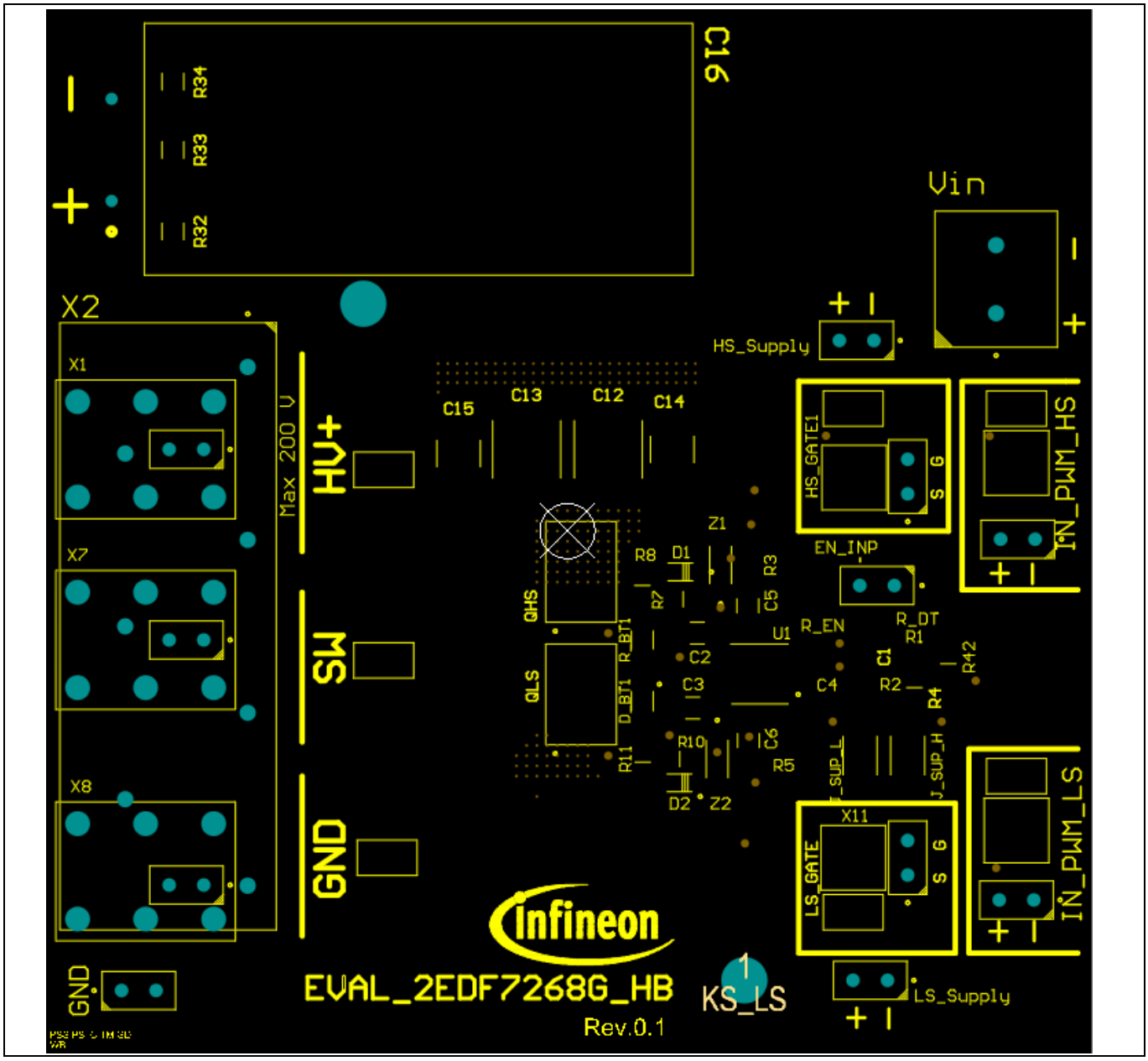

Figure 7 PCB top overlay

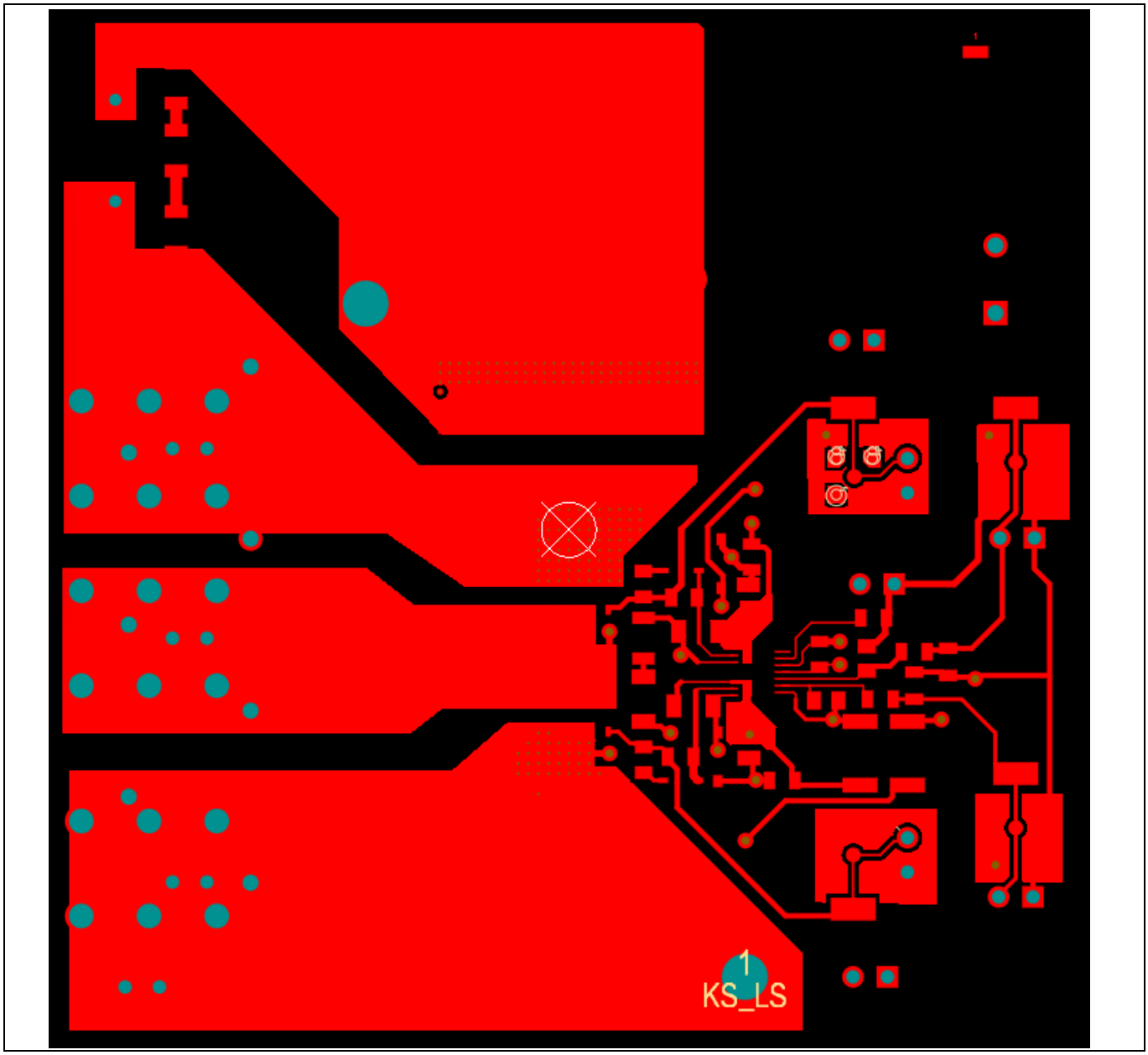

Figure 8 PCB top copper layer

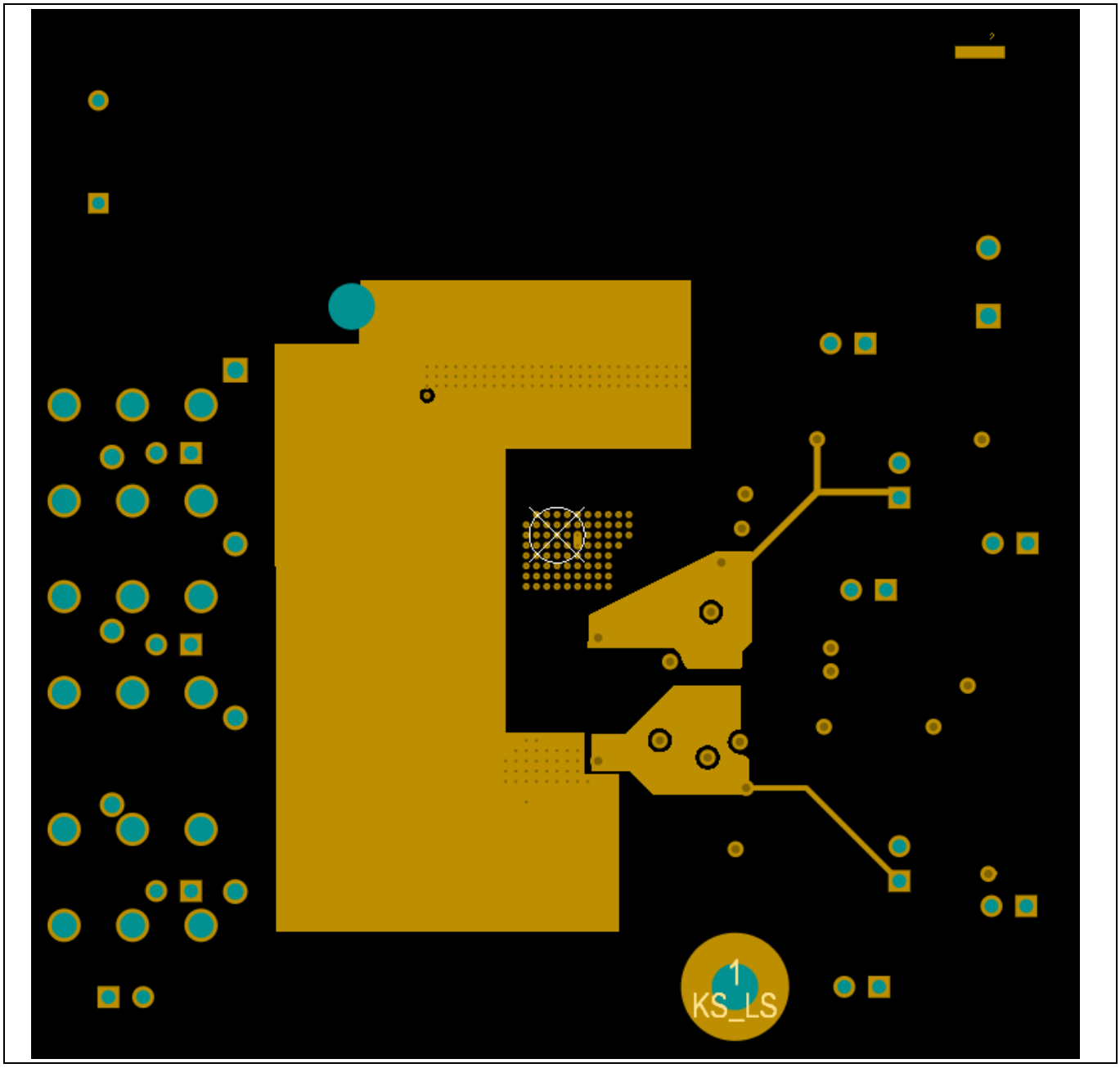

Figure 9 PCB inner copper layer 1

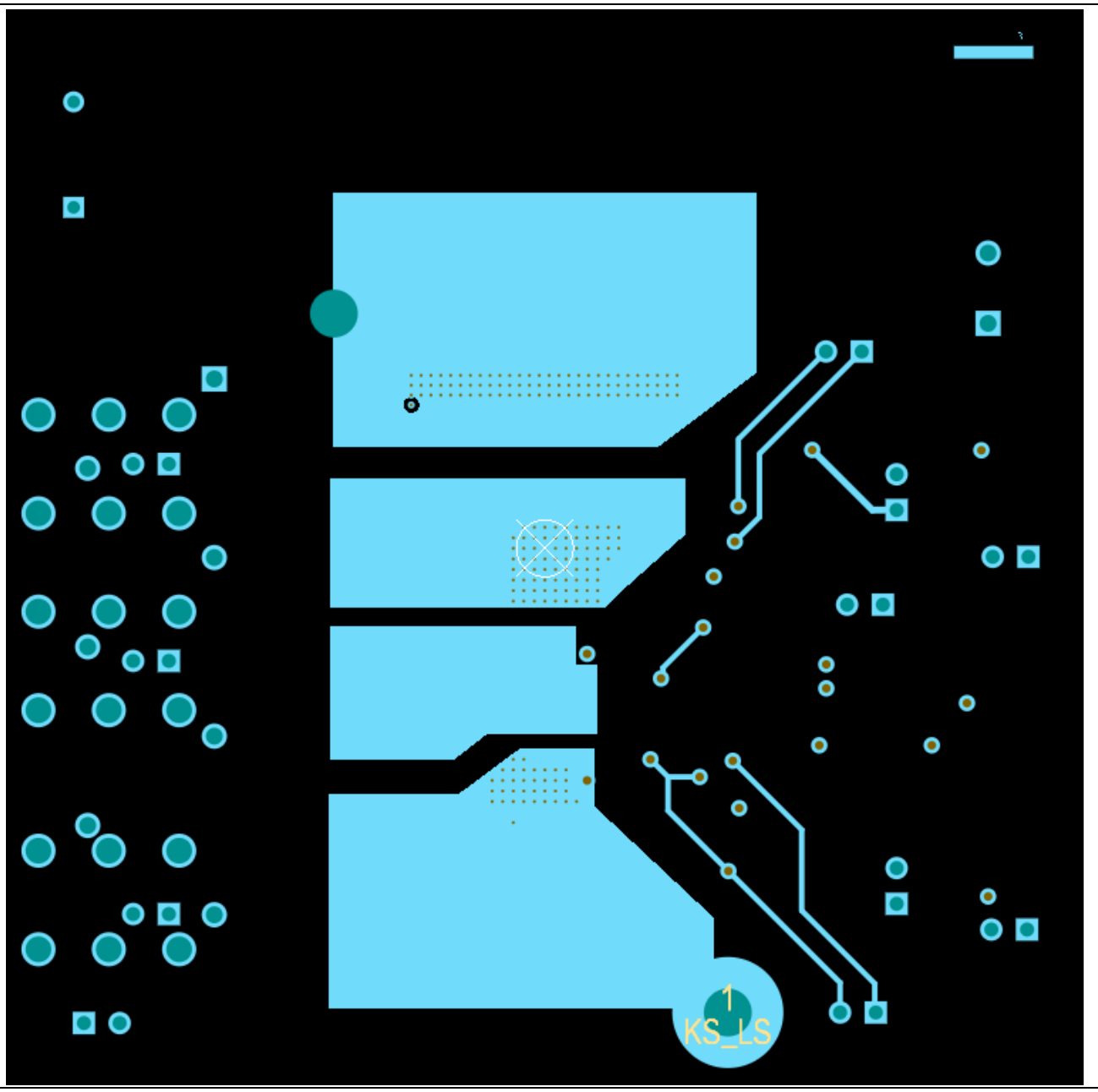

Figure 10 PCB inner copper layer 2

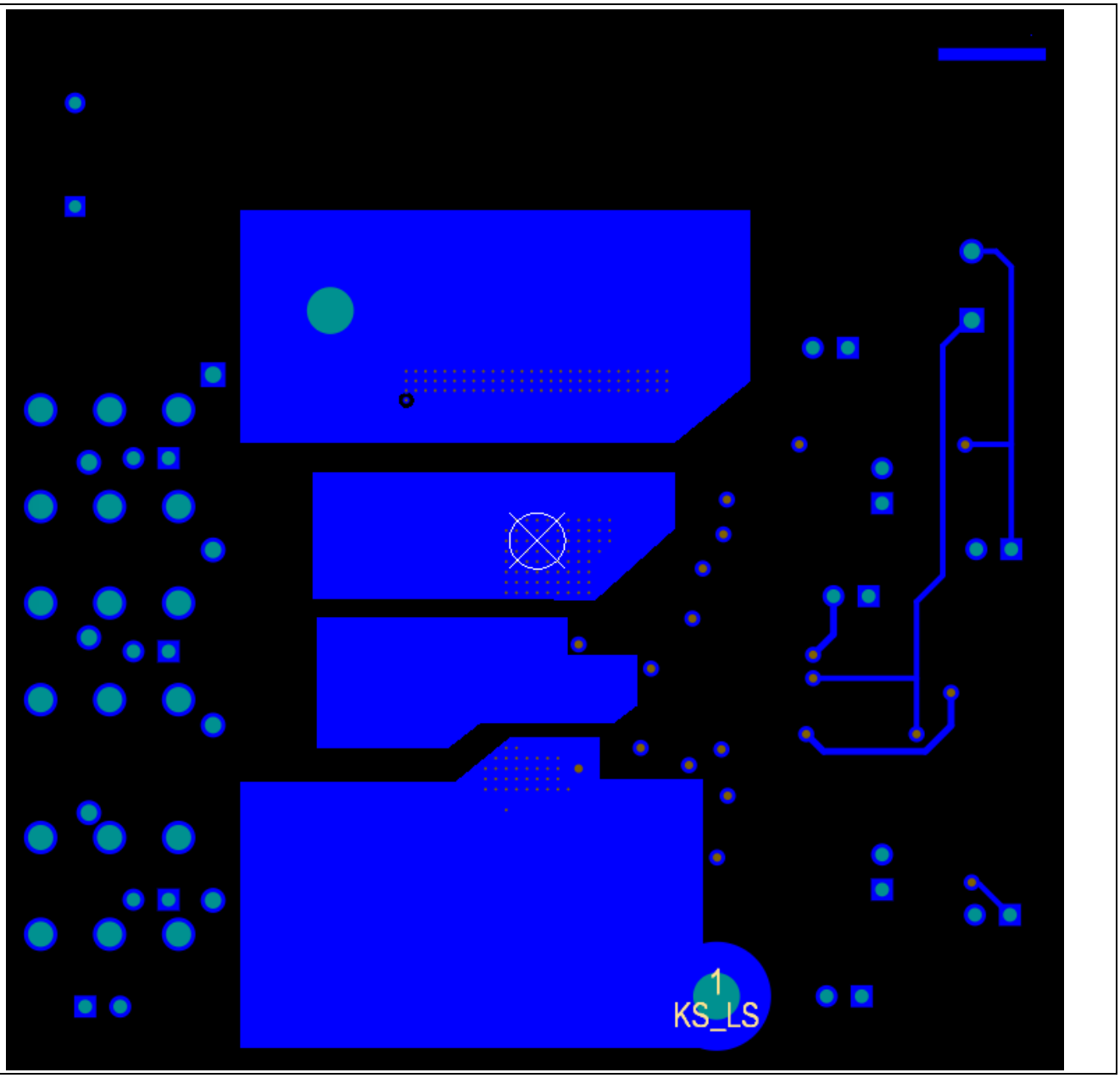

Figure 11 PCB bottom copper layer

3.3 Bill of materials

Table 4 Bill of materials

Designator	Quantity	Description	Manufacturer	Manufacturer P/N
C1, C4	2	CAP / CERA / 68pF / 250V / 5% / C0G (EIA) / NP0 / -55°C to 125°C / 0805(2012) / SMD / -	Murata	GRM21A5C2E680JW01
C2, C3, C5, C6	4	CAP / CERA / 2.2uF / 16V / 10% / X5R (EIA) / -55°C to 85°C / 1206(3216) / SMD / -	Murata	GRM316R61C225KA88D

Designator	Quantity	Description	Manufacturer	Manufacturer P/N
C12, C13	2	CAP / CERA / 1uF / 450V / 20% / X7T (EIA) / -55°C to 125°C / 2220(5750) / SMD / -	TDK Corporation	CGA9P4X7T2W105M250KA
C14, C15	2	Multilayer Ceramic Capacitors MLCC - SMD/SMT 630V 0.1uF X7R 1812 10%	AVX	C1812C104KBRACTU
C16	1	CAP / ELCO / 150uF / 450V / 20% / Aluminum electrolytic / -40°C to 105°C / 7.50mm C X 0.80mm W 18.25mm Dia X 42.00mm H / THT / -	Rubycon	ESH157M450AN7AA
D1, D2	2	Medium Power AF Schottky Diode	Infineon Technologies	BAT165
D_BT1	1	Surface Mount Glass Passivated Junction Rectifier	Vishay	GL34J-E3/83
EN_INP, GND_PROBE, HS_GATE1, LS_GATE	4	Through hole .025 SQ Post Header, 2.54mm pitch, 2 pin, vertical, single row	Samtec	HTSW-102-07-G-S
GND, H, TP1, TP2, TP3, TP4, TP6	7	Test Point, Miniature, Surface Mount, Silver Plate	Keystone Electronics Corp.	5017
HS_Supply, LS_Supply, PWMH, PWML	7	Through hole .025 SQ Post Header, 2.54mm pitch, 2 pin, vertical, single row	Samtec	TSW-102-08-G-S
HS	1	Heatsink, PCB mounting, 1 pin	TDK-Lambda	HAQ-10T
J_SUP_H, J_SUP_L	2	RES / STD / 0R / - / 0R / - / - 55°C to 155°C / 2010(5025) / SMD / -	Vishay	CRCW20100000Z0
QHS, QLS	2	OptiMOS™ 3 Power Transistor, N Channel	Infineon Technologies	BSC600N25NS3 G
R1, R2, R_EN	3	RES / STD / 0R / 125mW / 0R / 0ppm/K / -55°C to 155°C / 0805(2012) / SMD / -	Yageo	RC0805JR-070RL
R_DT	1	RES / STD / 10k / 125mW / 1% / 100ppm/K / -55°C to 155°C / 0805(2012) / SMD / -	Panasonic Electronic Components	ERJ-6ENF1002V
R3	1	RES / STD / 100R / 125mW / 1% / 100ppm/K / -55°C to 155°C / 0805(2012) / SMD / -	Yageo	AC0805FR-10100RL
R5	1	RES / STD / 1k / 125mW / 1% / 100ppm/K / -55°C to 155°C / 0805(2012) / SMD / -	Yageo	AC0805FR-071KL

Designator	Quantity	Description	Manufacturer	Manufacturer P/N
R4, R42	2	RES / STD / 49.9R / 125mW / 1% / 100ppm/K / -55°C to 155°C / 0805(2012) / SMD / -	Vishay	CRCW080549R9FK
R7, R10	2	RES / STD / 10R / 500mW / 5% / 200ppm/K / - / 0805(2012) / SMD / -	Vishay	CRCW080510R0JNEAHP
R8, R11	2	RES / STD / 5.1R / 500mW / 5% / 600ppm/K / -55°C to 155°C / 0805(2012) / SMD / -	Panasonic	ERJP06J5R1V
R32, R33, R34	3	RES / STD / 150k / 250mW / 1% / 100ppm/K / -55°C to 155°C / 1206(3216) / SMD / -	Vishay	RCV1206150KFKEA
R_BT1	1	RES / STD / 10R / 250mW / 1% / 200ppm/K / -55°C to 155°C / 1206(3216) / SMD / -	Yageo	RC1206FR-0710RL
U1	1	Dual Channel Isolated Gate Driver IC	Infineon Technologies	2EDF7258G
Vin	1	Screw Compact Terminal Block, Nominal current 32A, Nominal Voltage 400V, 2 pin 5mm Pitch	Phoenix Contact	1935776
X2	1	PCB Terminal Block, Screw Connection with Tension Sleeve, 41A, 1kV	Phoenix Contact	1777590
X3, X4, X10, X11	4	SMT Jack, Straight, 3.45mm L X 3.45mm W X 5.13mm H body	Samtec	MMCX-J-P-H-ST-SM1
Z1, Z2	2	Zener Diode 5.6 Volt 500 mW SOD-123	ON Semiconductor	MMSZ5V6T1G

3.4 Connector details

The following table shows the pinout of the input-side low-voltage connectors. It includes connectors PWMH, PWML, Vin, and EN_INP.

Table 5 Input-side connector pinout

Connector	Pin	Symbol	Function
PWMH	1	GNDI	Common ground reference for the input side
PWMH	2	IN_PWM_HS	Non-inverting input for the high-side gate driver
PWML	1	GNDI	Common ground reference for the input side
PWML	2	IN_PWM_LS	Non-inverting input for the low-side gate driver
Vin	1	Vin	Supply voltage for input side of the gate drivers
Vin	2	GNDI	Common ground reference for the input side

Connector	Pin	Symbol	Function
EN_INP	1	GNDI	Common ground reference for the input side
EN_INP	2	EN_INP	Enable input signal for the gate drivers

The following table shows the pinout of the output-side power supply connectors. It includes the connectors HS_Supply, LS_Supply, HS_GATE1 and LS_GATE.

Table 6 Output-side connector pinout

Connector	Pin	Symbol	Function
HS_Supply	1	GND_HS	Ground reference for the supply voltage of the high-side gate driver
HS_Supply	2	VDD_HS	Positive supply voltage for the high-side gate driver
LS_Supply	1	GND_LS	Ground reference for the supply voltage of the low-side gate driver
LS_Supply	2	VDD_LS	Positive supply voltage for the low-side gate driver
HS_GATE1	1	VSW	Kelvin source of the high-side switch
HS_GATE1	2	HSGate	Gate of the high-side switch
LS_GATE	1	KS_LS	Kelvin source of the low-side switch
LS_GATE	2	LSGate	Gate of the low-side switch

The following table shows the pinout of the high-voltage power terminal connector X2 and GND_PROBE.

Table 7 High-voltage terminal connector pinout

Connector	Pin	Symbol	Function
X2	1	HV+	High-voltage DC positive input
X2	2	HV+	High-voltage DC positive input
X2	3	HV+	High-voltage DC positive input
X2	4	SW	Half-bridge midpoint for connecting to the load inductor
X2	5	SW	Half-bridge midpoint for connecting to the load inductor
X2	6	GND	High-voltage DC ground connection
X2	7	GND	High-voltage DC ground connection
GND_PROBE	1	GND	High-voltage DC ground connection
GND_PROBE	2	GND	High-voltage DC ground connection

3.5 Measuring points

There are five test points on the board for connection to the oscilloscope to observe the signals of interest. The following includes the description of the test point and recommendation of probes and accessories.

Table 8 Test points and required probe

Test point label	Description	Referred to	Probe	Accessories
TP1	INB input to GNDI	GNDI	Passive 500 MHz[1]	Hook tip(013-0363-xx) for INA, alligator clip(196-3521-xx) for GNDI
			Standard differential probe	–
TP2	High-side gate-to-source voltage	HS Kelvin source	IsoVu (e.g., TIVP1) with TIVPMX10X (+-50V) sensor tip[2]	–
TP3	INA input to GNDI	GNDI	Passive 500 MHz[1]	Hook tip(013-0363-xx) for INA, alligator clip(196-3521-xx) for GNDI
			Standard differential probe	–
TP4	Low-side gate-to-source voltage	LS Kelvin source	1 GHz passive probe with low capacitance (e.g., TPP1000)[3]	–
H	High-voltage positive terminal	LS Kelvin source	High-voltage passive probe (e.g., PHV 1000)	–
GND	Low-side Kelvin source	–	–	–
TP6	Switching node	LS Kelvin source	High-voltage passive probe (e.g., PHV 1000)	–

3.6 Ordering information

Base part number	Package	Standard pack		Orderable part number
EVAL_2EDF7268G_HB	–	Boxed	1	EVAL2EDF7268GHBTOBO1
2EDF7268G	SON-13 4x4	Tape and Reel (TR)	1000	2EDF7268GXTMA1
BSC600N25NS3 G	PG-TDSON-8	Tape and Reel (TR)	5000	BSC600N25NS3 G

[1] Passive probe can be used when GNDI = PGND, then in configuration A or in the other configurations when there is no bulk voltage applied. Otherwise, please use differential probe.

[2] Do not use a standard differential probe for high-side measurements due to limited CMRR.

[3] Do not use a standard differential probe for GaN gate-to-source signals due to high capacitance that distorts the waveforms.

4 Related resources

- Gate Driver ICs Developer Community page
- Isolated Gate Driver ICs family page

References

[1] Infineon Technologies AG: *EiceDRIVER™ 2EDF72x8G datasheet*;

[2] Infineon Technologies AG: *OptiMOS™ 3 BSC600N25NS3 G 250V power transistor*; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2025-09-29	Initial release

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Customer shall not touch the Evaluation Board during operation and keep a safe distance.
Customer shall not touch the Evaluation Board after disconnecting the power supply, several components may still store electrical voltage and can discharge through physical contact. Several parts, like heat sinks and transformers, may still be very hot. Allow the components to cool before touching or servicing.
The electrical installation must be completed in accordance with the appropriate safety requirements.