XDP™ XDP710-002 hot-swap controller PMBus® commands

Wide input voltage range (5.5 V to 80 V) system monitoring and protection IC

About this document

Scope and purpose

This document describes all the PMBus® commands supported by XDP™ XDP710-002 system monitoring and protection IC.

Intended audience

This document is intended for XDP™ XDP710-002 users.

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1 Introduction

In tables where register bit fields are defined, the following conventions are used to indicate undefined and unimplemented function. Furthermore, types of bits and bit fields are defined using the abbreviations as shown in the following table.

Table 1 Bit function terminology

Function of bits	Description
Unimplemented, Reserved	Register bit fields named **0** indicate unimplemented functions with the following behavior: • Reading these bit fields returns 0 • These bit fields should be written with 0 if the bit field is defined as r or rh • These bit fields have to be written with 0 if the bit field is defined as rw These bit fields are reserved. The detailed description of these bit fields can be found in the register descriptions.
rw	The bit or bit field can be read and written.
rwh	As rw, but bit or bit field can also be set or reset by hardware.
r	The bit or bit field can only be read (read-only).
w, wX	The bit or bit field can only be written (write-only). A read of this register will always give a default value back that is described in the register documentation.
w0, w1	The bit or bit field can only be written (write-only). A read of this register will always give the value 0 or 1 back.
r0, r1	The bit or bit field can only be read. The read value is 0 or 1.
rh	This bit or bit field can be modified by hardware (read-hardware, typical example: status flags). A read of this bit or bit field give the actual status of this bit or bit field back. Writing to this bit or bit field has no effect on the setting of this bit or bit field.
s	Bits with this attribute are “sticky” in one direction. If their reset value is once overwritten by software, they can be switched again into their reset state only by a reset operation. Software cannot switch this type of bit into its reset state by writing the register. This attribute can be combined to “rws” or “rwhs”.
f	Bits with this attribute are readable only when they are accessed by an instruction fetch. Normal data read operations will return other values.

2 XDP™ XDP710-002 PMBus® commands

2.1 OPERATION command

This command is used to turn the unit on and off in conjunction with the input from the UV/EN pin.

OPERATION Address: 001_H

OPERATION command AsyncReset value: 80_H

7	6	5	4	3	2	1	0
ON	**Res**						
rw	r						

Field	Bits	Type	Description
ON	7	rw	**ON bit enables or disables the hot-swap output** 0_B **Disable**: Hot-swap output disabled 1_B **Enable**: Hot-swap output enabled

2.2 CLEAR_FAULTS command

This command is used to clear any fault and warning bits that have been set. If the fault or warning is still present when the bit is cleared, the fault bit is immediately set again. This command is write-only without a data byte.

CLEAR_FAULTS Address: 003_H

CLEAR_FAULTS command Reset values see: Table 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLEAR_FAULTS															
w															

Field	Bits	Type	Description
CLEAR_FAULTS	15:0	w	**Clears any fault bits that have been set**

Table 2 Reset values of CLEAR_FAULTS

Reset	Reset value	Note
AsyncReset	$UUUU_H$	Undefined - Not applicable

2.3 CAPABILITY command

This read-only command provides a way for a host system to determine some key capabilities of XDP710.

CAPABILITY Address: 019_H

CAPABILITY command AsyncReset value: $D0_H$

7	6	5	4	3	2	1	0
PCK_ERR_CHK	MAX_BUS_SPEED		SMBALLERT	NUMERIC_FORMAT	Res		
rh	rh		rh	rh	r		

Field	Bits	Type	Description
NUMERIC_FORMAT	3	rh	**Specifies the format of the numeric data** 0_B Numeric data is in direct format 1_B NA
SMBALLERT	4	rh	**Specifies whether the device has an SMBALERT# pin and supports the SMBus alert response protocol** 0_B NA 1_B The device supports the SMBus alert response protocol
MAX_BUS_SPEED	6:5	rh	**Specifies the maximum speed of the bus** 00_B NA 01_B NA 10_B Maximum supported bus speed is 1 MHz 11_B NA
PCK_ERR_CHK	7	rh	**Specifies whether the device supports packet error check** 0_B NA 1_B Packet error checking is supported

2.4 VOUT_OV_WARN_LIMIT command

This command sets the value of the output voltage that causes an output overvoltage (OOV) warning.

VOUT_OV_WARN_LIMIT Address: 042_H

VOUT_OV_WARN_LIMIT command AsyncReset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				VOUT_OV_WARN_LIMIT											
r				rw											

Field	Bits	Type	Description
VOUT_OV_WARN_LIMIT	11:0	rw	**OOV warning can be programmed from 0 V to 22 V, 0 V to 44 V, or 0 V to 88 V (absolute value) depending on the VTLM_RNG settings**

2.5 VOUT_UV_WARN_LIMIT command

This command sets the value of the output voltage that causes an output undervoltage (OUV) warning.

VOUT_UV_WARN_LIMIT Address: 043_H

VOUT_UV_WARN_LIMIT command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				VOUT_UV_WARN_LIMIT											
r				rw											

Field	Bits	Type	Description
VOUT_UV_WARN_LIMIT	11:0	rw	**OUV warning can be programmed from 0 V to 22 V, 0 V to 44 V, or 0 V to 88 V (absolute value) depending on the VTLM_RNG settings**

2.6 VOUT_UV_FAULT_LIMIT command

This command sets the value of the output voltage that causes an output undervoltage (OUV) fault.

VOUT_UV_FAULT_LIMIT Address: 044_H

VOUT_UV_FAULT_LIMIT command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				VOUT_UV_FAULT_LIMIT											
r				rw											

Field	Bits	Type	Description
VOUT_UV_FAULT_LIMIT	11:0	rw	**OUV fault can be programmed from 0 V to 22 V, 0 V to 44 V, or 0 V to 88 V (absolute value) depending on the VTLM_RNG settings**

2.7 IOUT_OC_WARN_LIMIT command

This command sets the level that causes an output overcurrent warning.

IOUT_OC_WARN_LIMIT Address: $04A_H$

IOUT_OC_WARN_LIMIT command AsyncReset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				IOUT_OC_WARN_LIMIT											
r				rw											

Field	Bits	Type	Description
IOUT_OC_WARN_LIMIT	11:0	rw	**OC warning can be programmed as a fraction of V_SNS_CS**

2.8 OT_FAULT_LIMIT command

This command sets the temperature of the FET at which the overtemperature (OT) fault is triggered.

OT_FAULT_LIMIT Address: $04F_H$

OT_FAULT_LIMIT command AsyncReset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				OT_FAULT_LIMIT											
r				rw											

Field	Bits	Type	Description
OT_FAULT_LIMIT	11:0	rw	**OT limit for triggering the fault**

2.9 OT_WARN_LIMIT command

This command sets the temperature of the FET at which the OT warning is triggered.

OT_WARN_LIMIT Address: 051_H

OT_WARN_LIMIT command AsyncReset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				OT_WARN_LIMIT											
r				rw											

Field	Bits	Type	Description
OT_WARN_LIMIT	11:0	rw	**OT limit for triggering the warning**

2.10 VIN_OV_FAULT_LIMIT command

This command sets the value of the input voltage that causes an input overvoltage (OV) fault.

VIN_OV_FAULT_LIMIT Address: 055_H

VIN_OV_FAULT_LIMIT command AsyncReset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				VIN_OV_FAULT_LIMIT											
r				rw											

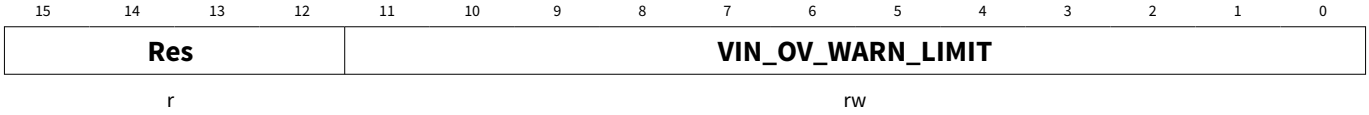
Field	Bits	Type	Description
VIN_OV_FAULT_LIMIT	11:0	rw	**OV fault can be programmed from 0 V to 22 V, 0 V to 44 V, or 0 V to 88 V (absolute value) depending on the VTLM_RNG settings**

2.11 VIN_OV_WARN_LIMIT command

This command sets the value of the input voltage that causes an input OV warning.

VIN_OV_WARN_LIMIT Address: 057_H

VIN_OV_WARN_LIMIT command AsyncReset value: $0FFF_H$



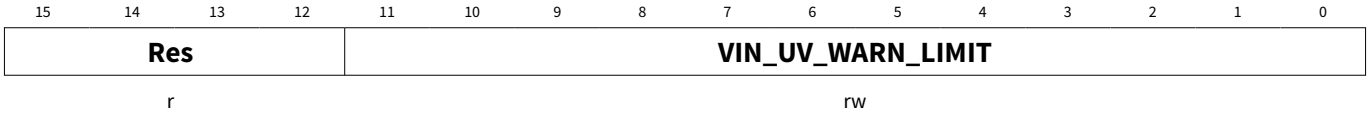
Field	Bits	Type	Description
VIN_OV_WARN_LIMIT	11:0	rw	**OV warning can be programmed from 0 V to 22 V, 0 V to 44 V, or 0 V to 88 V (absolute value) depending on the VTLM_RNG settings**

2.12 VIN_UV_WARN_LIMIT command

This command sets the value of the input voltage that causes an input undervoltage (UV) warning.

VIN_UV_WARN_LIMIT Address: 058_H

VIN_UV_WARN_LIMIT command AsyncReset value: 0000_H



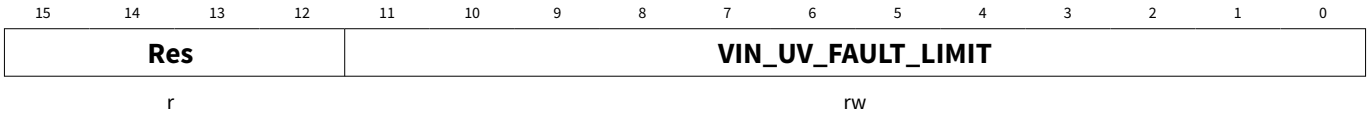
Field	Bits	Type	Description
VIN_UV_WARN_LIMIT	11:0	rw	**UV warning can be programmed from 0 V to 22 V, 0 V to 44 V, or 0 V to 88 V (absolute value) depending on the VTLM_RNG settings**

2.13 VIN_UV_FAULT_LIMIT command

This command sets the value of the input voltage that causes an input UV fault.

VIN_UV_FAULT_LIMIT Address: 059_H

VIN_UV_FAULT_LIMIT command AsyncReset value: 0000_H



Field	Bits	Type	Description
VIN_UV_FAULT_LIMIT	11:0	rw	**UV fault can be programmed from 0 V to 22 V, 0 V to 44 V, or 0 V to 88 V (absolute value) depending on the VTLM_RNG settings**

2.14 PIN_OP_WARN_LIMIT command

This command sets the value of the input power calculated as a product of VIN * IOUT that causes an input overpower (OP) warning.

PIN_OP_WARN_LIMIT Address: $06B_H$

PIN_OP_WARN_LIMIT command AsyncReset value: $FFFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIN_OP_WARN_LIMIT															
rw															

Field	Bits	Type	Description
PIN_OP_WARN_LIMIT	15:0	rw	**OP warning can be programmed from 0 to VTLM_RNG * Ioc**

2.15 STATUS_BYTE command

This command returns one byte of information with a summary of the most critical faults.

STATUS_BYTE Address: 078_H

STATUS_BYTE command AsyncReset value: 40_H

7	6	5	4	3	2	1	0
Res	OFF	Res	IOUT_OC_FAULT	VIN_UV_FAULT	TEMP	CML	NONE_OF_THE_ABOVE
r	rh	r	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
NONE_OF_THE_ABOVE	0	rwh	**This bit indicates if a fault or warning not listed in bits [6:1] has occurred** 0_B Fault or warning has not occurred 1_B Fault or warning has occurred
CML	1	rwh	**This bit indicates if a communication, memory, or logic fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred
TEMP	2	rwh	**This bit indicates if a temperature fault or warning has occurred** 0_B Fault or warning has not occurred 1_B Fault or warning has occurred
VIN_UV_FAULT	3	rwh	**This bit indicates if an input undervoltage fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred
IOUT_OC_FAULT	4	rwh	**This bit indicates if an output overcurrent fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred
OFF	6	rh	**This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled** 0_B Output is on 1_B Output is off

2.16 STATUS_WORD command

This command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status commands. The low byte of the STATUS_WORD is the same command as the STATUS_BYTE.

STATUS_WORD Address: 079_H

STATUS_WORD command AsyncReset value: 0840_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VOUT	**IOUT_POUT**	**INPUT**	**MFR**	**PG_STATUS**	**Res**	**OTHER**	**Res**		**OFF**	**Res**	**IOUT_OC_FAULT**	**VIN_UV_FAULT**	**TEMP**	**CML**	**NONE_OF_THE_ABOVE**
rwh	rwh	rwh	rwh	rh	r	rwh	r		rh	r	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
NONE_OF_THE_ABOVE	0	rwh	**This bit indicates if a fault or warning not listed in bits [6:1] has occurred** 0_B Fault or warning has not occurred 1_B Fault or warning has occurred
CML	1	rwh	**This bit indicates if a communication, memory, or logic fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred
TEMP	2	rwh	**This bit indicates if a temperature fault or warning has occurred** 0_B Fault or warning has not occurred 1_B Fault or warning has occurred
VIN_UV_FAULT	3	rwh	**This bit indicates if an input undervoltage fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred
IOUT_OC_FAULT	4	rwh	**This bit indicates if an output overcurrent fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred
OFF	6	rh	**This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled** 0_B Output is on 1_B Output is off
OTHER	9	rwh	**This bit reflects the status of the STATUS_OTHER command** 0_B Bit in status other is not set 1_B Bit in status other is set

(table continues...)

(continued)

Field	Bits	Type	Description
PG_STATUS	11	rh	**This bit reflects the status of the PWR_GD signal** Note that this bit shows the status of the system power directly, while PWRGD_STATUS in the STATUS_MODE command follows the PWRGD pin status regardless of its polarity with respect to the system power 0_B Output voltage is valid 1_B Output voltage is not valid
MFR	12	rwh	**A bit in the STATUS_MFR_SPECIFIC command has been set** 0_B No bit has been set 1_B A bit has been set
INPUT	13	rwh	**An input voltage, input current, or input power fault, or warning has occurred** 0_B Fault or warning has not occurred 1_B Fault or warning has occurred
IOUT_POUT	14	rwh	**An output current, or output power fault, or warning has occurred** 0_B Fault or warning has not occurred 1_B Fault or warning has occurred
VOUT	15	rwh	**An output voltage fault or warning has occurred** 0_B Fault or warning has not occurred 1_B Fault or warning has occurred

2.17 STATUS_VOUT command

This command returns one data byte with a summary of the output voltage faults and warnings.

STATUS_VOUT Address: $07A_H$

STATUS_VOUT command AsyncReset value: 00_H

7	6	5	4	3	2	1	0
Res	**VOUT_OV_WARN**	**VOUT_UV_WARN**	**VOUT_UV_FAULT**	**Res**			
r	rwh	rwh	rwh	r			

Field	Bits	Type	Description
VOUT_UV_FAULT	4	rwh	**An output undervoltage fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred
VOUT_UV_WARN	5	rwh	**An output undervoltage warning has occurred** 0_B Warning has not occurred 1_B Warning has occurred
VOUT_OV_WARN	6	rwh	**An output overvoltage warning has occurred** 0_B Warning has not occurred 1_B Warning has occurred

2.18 STATUS_IOUT command

This command returns one data byte with a summary of the output current faults and warnings and device status.

STATUS_IOUT Address: $07B_H$

STATUS_IOUT command AsyncReset value: 00_H

7	6	5	4	3	2	1	0
IOUT_OC_FAULT	**Res**	**IOUT_OC_WARN**	**Res**		**P_LIM_MODE**	**Res**	
rwh	r	rwh	r		rh	r	

Field	Bits	Type	Description
P_LIM_MODE	2	rh	**This bit is set when the device is operating in I_REG state** 0_B The device is not operating in I_REG state 1_B The device is operating in I_REG state
IOUT_OC_WARN	5	rwh	**An output overcurrent warning has occurred** 0_B Warning has not occurred 1_B Warning has occurred
IOUT_OC_FAULT	7	rwh	**An output overcurrent fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred

2.19 STATUS_INPUT command

This command returns one data byte with a summary of the system input fault and warning status.

STATUS_INPUT Address: $07C_H$

STATUS_INPUT command AsyncReset value: 00_H

7	6	5	4	3	2	1	0
VIN_OV_FAULT	**VIN_OV_WARN**	**VIN_UV_WARN**	**VIN_UV_FAULT**	**Res**			**PIN_OP_WARN**
rwh	rwh	rwh	rwh	r			rwh

Field	Bits	Type	Description
PIN_OP_WARN	0	rwh	**An input overpower warning has occurred** 0_B Warning has not occurred 1_B Warning has occurred
VIN_UV_FAULT	4	rwh	**An input undervoltage fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred
VIN_UV_WARN	5	rwh	**An input undervoltage warning has occurred** 0_B Warning has not occurred 1_B Warning has occurred

(table continues...)

(continued)

Field	Bits	Type	Description
VIN_OV_WARN	6	rwh	**An input overvoltage warning has occurred** 0_B Warning has not occurred 1_B Warning has occurred
VIN_OV_FAULT	7	rwh	**An input overvoltage fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred

2.20 STATUS_TEMPERATURE command

This command returns one data byte with a summary of the external temperature status.

STATUS_TEMPERATURE Address: $07D_H$

STATUS_TEMPERATURE command AsyncReset value: 00_H

7	6	5	4	3	2	1	0
OT_FAULT	**OT_WARN**	**Res**					
rwh	rwh	r					

Field	Bits	Type	Description
OT_WARN	6	rwh	**An overtemperature warning has occurred** 0_B Warning has not occurred 1_B Warning has occurred
OT_FAULT	7	rwh	**An overtemperature fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred

2.21 STATUS_CML command

This command returns one data byte with a summary of the communication interface and memory status.

STATUS_CML Address: $07E_H$

STATUS_CML command AsyncReset value: 00_H

7	6	5	4	3	2	1	0
INVALID_CMD	**INVALID_DATA**	**PEC_FAIL**	**MEM_FAULT**	**Res**		**OTHER**	**Res**
rwh	rwh	rwh	rwh	r		rwh	r

Field	Bits	Type	Description
OTHER	1	rwh	**A miscellaneous communication fault has occurred** 0_B No fault has occurred 1_B Fault has occurred

(table continues...)

(continued)

Field	Bits	Type	Description
MEM_FAULT	4	rwh	**A one-time programmable (OTP) memory fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred
PEC_FAIL	5	rwh	**Packet error check status** 0_B Packet error check has not failed 1_B Packet error check failed
INVALID_DATA	6	rwh	**Invalid or unsupported data received** 0_B Invalid or unsupported data not received 1_B Invalid or unsupported data received
INVALID_CMD	7	rwh	**Invalid or unsupported command received** 0_B Invalid or unsupported command not received 1_B Invalid or unsupported command received

2.22 STATUS_OTHER command

This command returns one data byte with the SMBALERT# status.

STATUS_OTHER Address: $07F_H$

STATUS_OTHER command AsyncReset value: 00_H

7	6	5	4	3	2	1	0
Res							**SMBALERT**
r							rwh

Field	Bits	Type	Description
SMBALERT	0	rwh	**First to assert the SMBALERT# status** 0_B Not the first to assert SMBALERT# 1_B First to assert SMBALERT#

2.23 STATUS_MFR_SPECIFIC command

This command returns one data byte with a summary of the general device status.

STATUS_MFR_SPECIFIC Address: 080_H

STATUS_MFR_SPECIFIC command AsyncReset value: 00_H

7	6	5	4	3	2	1	0
Res				**STATUS_LATCH_OFF**	**SOC_FAULT**	**WATCHDOG_FAULT**	**FET_HEALTH**
r				rh	rwh	rwh	rwh

Field	Bits	Type	Description
FET_HEALTH	0	rwh	**One of the FET faults occurred (FET_DS, FET_GD, FET_GS)** 0_B No FET faults have occurred 1_B One or more FET faults have occurred
WATCHDOG_FAULT	1	rwh	**A watchdog fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred
SOC_FAULT	2	rwh	**An SOC fault has occurred** 0_B Fault has not occurred 1_B Fault has occurred
STATUS_LATCH_OFF	3	rh	**Device latch-off state** 0_B Device is not in latch-off state 1_B Device is in latch-off state

2.24 READ_EIN command

This command returns the input energy reading.

READ_EIN Address: 086_H

READ_EIN command AsyncReset value: $0000\ 0000\ 0000_H$

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
SAMPLE_COUNT															
rh															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SAMPLE_COUNT								ROLLOVER_COUNT								ENERGY_COUNT															
rh								rh								rh															

Field	Bits	Type	Description
ENERGY_COUNT	15:0	rh	**Output of an accumulator that continuously sums samples of the instantaneous input power**
ROLLOVER_COUNT	23:16	rh	**Unsigned integer that periodically rolls over from its maximum positive value to zero**
SAMPLE_COUNT	47:24	rh	**Unsigned integer that counts the number of samples of the instantaneous input power**

2.25 READ_VIN command

This command returns the input voltage reading.

READ_VIN Address: 088_H

READ_VIN command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**READ_VIN**											
r				rh											

Field	Bits	Type	Description
READ_VIN	11:0	rh	**Input voltage reading in direct format**

2.26 READ_VOUT command

This command returns the output voltage reading.

READ_VOUT Address: $08B_H$

READ_VOUT command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**READ_VOUT**											
r				rh											

Field	Bits	Type	Description
READ_VOUT	11:0	rh	**Output voltage reading in direct format**

2.27 READ_IOUT command

This command returns the reading of the current flow through the sense resistor.

READ_IOUT Address: $08C_H$

READ_IOUT command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**READ_IOUT**											
r				rh											

Field	Bits	Type	Description
READ_IOUT	11:0	rh	**FET drain current reading in direct format**

2.28 READ_TEMPERATURE_1 command

This command returns the reading of the external temperature measured between the TSNS_P and TSNS_N pins.

READ_TEMPERATURE_1 Address: $08D_H$

READ_TEMPERATURE_1 command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**READ_TEMPERATURE_1**											
r				rh											

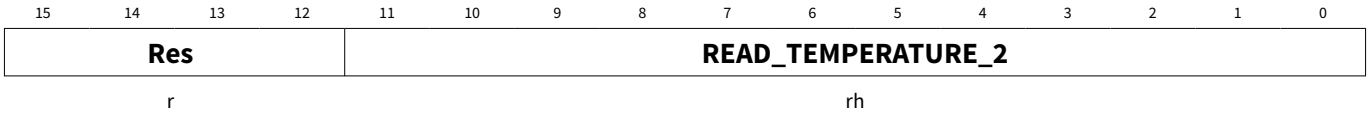
Field	Bits	Type	Description
READ_TEMPERATURE_1	11:0	rh	**External temperature reading in direct format**

2.29 READ_TEMPERATURE_2 command

This command returns the reading of the on-chip temperature measured by the internal temperature sensor.

READ_TEMPERATURE_2 Address: $08E_H$

READ_TEMPERATURE_2 command AsyncReset value: 0000_H



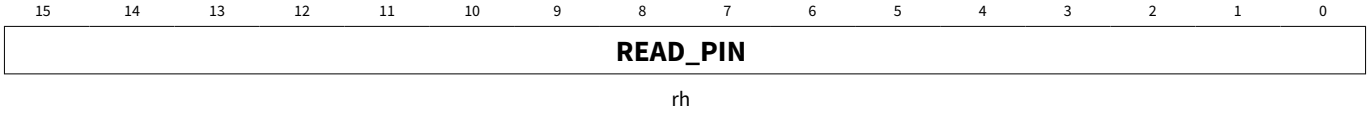
Field	Bits	Type	Description
READ_TEMPERATURE_2	11:0	rh	**Internal temperature reading in direct format**

2.30 READ_PIN command

This command returns the input power reading.

READ_PIN Address: 097_H

READ_PIN command AsyncReset value: 0000_H



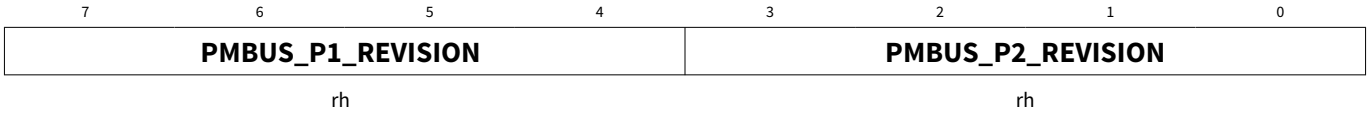
Field	Bits	Type	Description
READ_PIN	15:0	rh	**Input power reading in direct format**

2.31 PMBUS_REVISION command

This command stores the revision of the PMBus® to which the device is compliant.

PMBUS_REVISION Address: 098_H

PMBUS_REVISION command AsyncReset value: 33_H



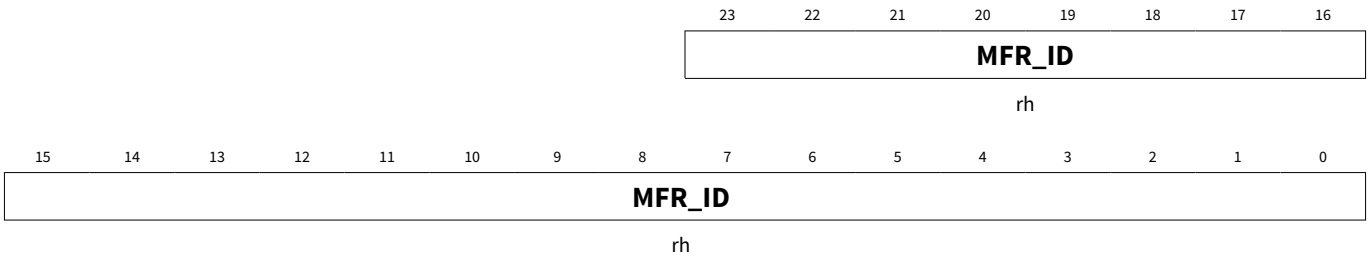
Field	Bits	Type	Description
PMBUS_P2_REVISION	3:0	rh	**0x3 indicates part 2 is revision 1.3**
PMBUS_P1_REVISION	7:4	rh	**0x3 indicates part 1 is revision 1.3**

2.32 MFR_ID command

Manufacturer ID according to ISO/IEC 8859-1 [A05].

MFR_ID Address: 099_H

MFR_ID command AsyncReset value: $00\ 4649_H$



Field	Bits	Type	Description
MFR_ID	23:0	rh	**Manufacturer's ID**

2.33 MFR_MODEL command

Manufacturer model command.

MFR_MODEL Address: $09A_H$

MFR_MODEL command Reset values see: Table 3



Field	Bits	Type	Description
MFR_MODEL	63:0	rh	**This command contains a string that identifies the model of the device**

Table 3 Reset values of MFR_MODEL

Reset	Reset value	Note
AsyncReset	$0000\ 3031\ 3750\ 4458_H$	-

2.34 MFR_REVISION command

This command stores the manufacturer's revision number.

MFR_REVISION Address: $09B_H$

MFR_REVISION command AsyncReset value: 0001_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MFR_REVISION															
rh															

Field	Bits	Type	Description
MFR_REVISION	15:0	rh	**Silicon version**

2.35 PMBUS_CFG command

Configuration command for PMBus® device address and speed selection.

PMBUS_CFG Address: $0D0_H$

PMBUS_CFG command AsyncReset value: 10_H

7	6	5	4	3	2	1	0
PMBUS_SPEED	**PMBUS_BASE_ADDR**			**PMBUS_DEVICE_ADDR**			
rw	rw			rw			

Field	Bits	Type	Description
PMBUS_DEVICE_ADDR	3:0	rw	**LSB part of the PMBus address [3:0]**
PMBUS_BASE_ADDR	6:4	rw	**MSB part of the PMBus address [6:4]**
PMBUS_SPEED	7	rw	**Operating PMBus speed** 0_B Fast Mode Plus - 1 MHz 1_B Standard or Fast Mode - 400 kHz

2.36 MODE command

Mode configuration and FET selection.

MODE Address: $0D1_H$

MODE command AsyncReset value: $7F_H$

7	6	5	4	3	2	1	0
Res	**MODE**	**FET_SELECT**					
r	rw	rw					

Field	Bits	Type	Description
FET_SELECT	5:0	rw	**FET_SELECT bits select FET and SOA curve to be used from a list of pre-programmed ones** 00_H BSC027N10NS5ATMA1 - DC line 01_H BSC035N10NS5ATMA1 - DC line 02_H BSC040N10NS5ATMA1 - DC line 03_H IPTG011N08NM5 - DC line 04_H IPTC012N08NM5 - DC line 05_H IPB017N10N5LFATMA1 - DC line 06_H BSC093N15NS5 - DC line 07_H BSC074N15NS5 - DC line 08_H IPTG014N10NM5 - DC line 09_H IPTC015N10NM5 - DC line $0A_H$ IPT015N10N5ATMA1 - DC line $0B_H$ IPB017N10N5ATMA1 - DC line $0C_H$ IPB018N10NM6 - DC line $0D_H$ IPT013N08NM5LF - DC line $0E_H$ IPB020N10N5ATMA1 - DC line $0F_H$ IPB020N10N5LFATMA1 - DC line 10_H IPB027N10N5ATMA1 - DC line 11_H IPB032N10N5ATMA1 - DC line 12_H IPB033N10N5LFATMA1 - DC line 13_H IPB072N15N3 - DC line 14_H IPB042N10N3 - DC line 15_H Reserved … $1F_H$ Reserved 20_H BSC027N10NS5ATMA1 - 10 ms line 21_H BSC035N10NS5ATMA1 - 10 ms line 22_H BSC040N10NS5ATMA1 - 10 ms line 23_H IPTG011N08NM5 - 10 ms line 24_H IPTC012N08NM5 - 10 ms line 25_H IPB017N10N5LFATMA1 - 10 ms line 26_H BSC093N15NS5 - 10 ms line 27_H BSC074N15NS5 - 10 ms line 28_H IPTG014N10NM5 - 10 ms line 29_H IPTC015N10NM5 - 10 ms line $2A_H$ IPT015N10N5ATMA1 - 10 ms line $2B_H$ IPB017N10N5ATMA1 - 10 ms line $2C_H$ IPB018N10NM6 - 10 ms line $2D_H$ IPT013N08NM5LF - 10 ms line $2E_H$ IPB020N10N5ATMA1 - 10 ms line $2F_H$ IPB020N10N5LFATMA1 - 10 ms line 30_H IPB027N10N5ATMA1 - 10 ms line 31_H IPB032N10N5ATMA1 - 10 ms line 32_H IPB033N10N5LFATMA1 - 10 ms line 33_H IPB072N15N3 - 10 ms line

(table continues...)

(continued)

Field	Bits	Type	Description
			34_H IPB042N10N3 - 10 ms line 35_H Reserved … $3E_H$ Reserved $3F_H$ SOA command
MODE	6	rw	**MODE bit selects the UV, OV, and OUV fault sources in fully digital mode (FDM)** Either analog comparators at the UV/EN, OV, and FB pins are used to trigger the UV, OV, and OUV faults or ADC conversions results are compared digitally with the VIN_UV_FAULT_LIMIT, VIN_OV_FAULT_LIMIT, and VOUT_UV_FAULT_LIMIT to trigger the faults 0_B **ACM**: Analog comparators mode 1_B **DCM**: Digital comparators mode

2.37 SOA command

Configures the safe operating area (SOA) of the FET if it is not pre-programmed. This command is a 16-bit FIFO.

SOA command structure:

- Words 0 to 39: SOA current at 1 V to 80 V. Odd voltages being in the lower byte of each word, even voltages being in the higher byte of each word.
- Word 40: Higher byte: 1 ms factor[15:12], 100 µs factor[11:8], resolution breakpoint[7:0]
- Word 41: i_coeff[7:5], p_coeff[4:2], idac_fs_sel[1:0]
- Word 42: CRC16[15:0]

Boost mode 1 ms factor: If boost mode is enabled and 1 ms pulse is selected in the BOOSTMODE_DC bits, the programmed SOA value is multiplied by this factor to determine the level of the current pulse.

Boost mode 100 µs factor: Current pulse level = programmed SOA * 100 µs factor if 100 µs pulse is selected in the BOOSTMODE_DC bits.

Resolution breakpoint: This value must be programmed according to the FET's SOA DC line and it is the first voltage point where the allowed current level is equal or higher than 0.5 A. Above this point, the current regulation range is 0.5 A and the resolution of the control loop is 1.95 mA. Below this point, the range is 127.5 A and the resolution changes to 0.5 A.

How to enter data:

User FET data can be entered into the SOA command and can be selected by setting the FET_SELECT command to SOA OTP. SOA is a 16-bit command that loads into a 42 deep 16-bit word FIFO with a CRC16 to make sure that the data entered is not corrupted.

Word	Byte 1 contents								Byte 0 contents							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SOA current at 2 V								SOA current at 1 V							
1	SOA current at 4 V								SOA current at 3 V							
…	…								…							
38	SOA current at 78 V								SOA current at 77 V							
39	SOA current at 80 V								SOA current at 79 V							
40	1 ms factor				100 µs factor				Resolution breakpoint							
41									I_COEFF			P_COEFF			IDAC_FS_SEL	

42	CRC16

- First write to SOA register with data for word 0
- Continue filling the FIFO until all SOA data words are filled
- Enter word 40 Byte 0 with resolution breakpoint: This value must be programmed according to the FET's SOA DC line and it is the first voltage point where the allowed current level is equal or higher than 0.5 A. Above this point, the current regulation range is 0.5 A and resolution of the control loop is 1.95 mA. Below this point, the range is 127.5 A and the resolution changes to 0.5 A.

To calculate the value to be entered below the resolution breakpoint:

$$SOA(decimal\ value) = SOA\ in\ Amperes * \frac{255}{range} = SOA\ in\ Amperes * \frac{255}{127.5A}$$

Figure 1 SOA register equation 1

And above the resolution breakpoint:

$$SOA(decimal\ value) = SOA\ in\ Amperes * \frac{256}{range} = SOA\ in\ Amperes * \frac{256}{0.5A}$$

Figure 2 SOA register equation 2

XDP710 automatically interprets the data above and below the breakpoint accordingly.

- Enter word 40 Byte 1 with boost multiplication factors coded so that multiplication is in powers of 2, for example, 0000 = 1; 0001 = 2; 0010 = 4; etc. These factors must be calculated as the ratio between the size of the 1 ms or 100 µs SOA lines respectively, and the DC SOA line. If boost mode is enabled, the programmed SOA value is multiplied by one of these factors (depending on the pulse length selected in BOOSTMODE_DC bits) to determine the level of the current pulse. The start-up behavior is as follows:
  - For full boost:
    - Above breakpoint, pulse = programmed SOA at higher resolution * multiplication factor
    - Below breakpoint, pulse = programmed SOA at lower resolution * multiplication factor
  - For auto boost:
    - Above breakpoint, pulse = programmed SOA at higher resolution * multiplication factor
    - Below breakpoint, charging continues with normal start-up. Regulation level = programmed SOA at lower resolution
  - For normal start up:
    - Above breakpoint, regulation level = 0.25 A (programmed values are ignored)
    - Below breakpoint, regulation level = programmed SOA at lower resolution
- Enter word 41 with the gate regulation current and I and P coefficients

IDAC_FS_SEL	Value	Description
0x0	0	31 µA
0x1	1	62 µA
0x2	2	124 µA
0x3	3	248 µA

- Enter word 42 with CRC16 code for previous entered data
- Once the FIFO is full, the SOA_FULL status bit field is set to 1'b1
- If the FIFO is full, the CRC check is performed and the SOA_CRC status bit is set to 1'b1 if the data matches CRC

The CRC16-CCITT algorithm must be used:

- Width = 16 bits

- Truncated polynomial = 0x1021
- Initial value = 0xFFFF

SOA Address: $0D2_H$

SOA command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOA															
w															

Field	Bits	Type	Description
SOA	15:0	w	**16 bits data**

2.38 REG_CFG command

Regulation configuration command.

REG_CFG Address: $0D3_H$

REG_CFG command AsyncReset value: 0803_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			**BOOSTMODE_DC**			**BOOSTMODE_TMR**	**BOOSTMODE_EN**		**RMS_EN**	**RSNS**					
r			rw			rw	rw		rw	rw					

Field	Bits	Type	Description
RSNS	5:0	rw	**The RSNS bit field is used to set the ratio of the voltage at the current sense pins to the sensed current, in other words, the value of the sense resistor** 00_H 0.2 mΩ 01_H 0.25 mΩ 02_H 0.3 mΩ 03_H 0.33 mΩ 04_H 0.4 mΩ 05_H 0.47 mΩ 06_H 0.5 mΩ 07_H 0.6 mΩ 08_H 0.67 mΩ 09_H 0.7 mΩ $0A_H$ 0.75 mΩ $0B_H$ 0.8 mΩ $0C_H$ 0.9 mΩ $0D_H$ 1 mΩ $0E_H$ 1.1 mΩ $0F_H$ 1.2 mΩ 10_H 1.25 mΩ 11_H 1.3 mΩ 12_H 1.4 mΩ 13_H 1.5 mΩ 14_H 1.6 mΩ 15_H 1.7 mΩ 16_H 1.8 mΩ 17_H 1.9 mΩ 18_H 2 mΩ 19_H 2.1 mΩ $1A_H$ 2.2 mΩ $1B_H$ 2.3 mΩ $1C_H$ 2.4 mΩ $1D_H$ 2.5 mΩ $1E_H$ 2.6 mΩ $1F_H$ 2.7 mΩ 20_H 2.8 mΩ 21_H 3 mΩ 22_H 3.1 mΩ 23_H 3.2 mΩ 24_H 3.3 mΩ 25_H 3.4 mΩ 26_H 3.5 mΩ 27_H 3.6 mΩ 28_H 3.7 mΩ 29_H 3.8 mΩ $2A_H$ 3.9 mΩ

(table continues...)

(continued)

Field	Bits	Type	Description
			$2B_H$ 4 mΩ $2C_H$ 4.1 mΩ $2D_H$ 4.2 mΩ $2E_H$ 4.3 mΩ $2F_H$ 4.4 mΩ 30_H 4.5 mΩ 31_H 4.6 mΩ 32_H 4.7 mΩ 33_H 4.8 mΩ 34_H 4.9 mΩ 35_H 5 mΩ 36_H 5.5 mΩ 37_H 6 mΩ 38_H 6.5 mΩ 39_H 7 mΩ $3A_H$ 7.5 mΩ $3B_H$ 8 mΩ $3C_H$ 8.5 mΩ $3D_H$ 9 mΩ $3E_H$ 9.5 mΩ $3F_H$ 10 mΩ
RMS_EN	6	rw	**The RMS_EN bit enables or disables the RMS calculation function of the overcurrent (OC) protection** If enabled, protection level is based on the RMS calculation instead of the instant measurement. RMS is a sub-function of OC. Therefore, OC must be enabled if RMS function is desired 0_B **Disable**: RMS disabled 1_B **Enable**: RMS enabled
BOOSTMODE_EN	8:7	rw	**BOOSTMODE_EN bits enable or disable the boost mode feature and selects between automatic or full boost mode** 00_B Boost mode deactivated 01_B Full boost mode 10_B Automatic boost mode 11_B Reserved (not to be used)
BOOSTMODE_TMR	9	rw	**BOOSTMODE_TMR sets the time for which the current is to be regulated** 0_B 100 µs pulse 1_B 1 ms pulse

(table continues...)

(continued)

Field	Bits	Type	Description
BOOSTMODE_DC	12:10	rw	**BOOSTMODE_DC defines the percentage of the period for which the BOOSTMODE_TMR pulse is present** 000_B 2% 001_B 5% 010_B 10 % 011_B 15% 100_B 20% 101_B 30% 110_B 40% 111_B 50%

2.39 V_SNS_CFG command

Voltage sense configuration command.

V_SNS_CFG Address: $0D4_H$

V_SNS_CFG command AsyncReset value: 0028_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						**VIN_UV_HYST**				**OVIN_FAULT_LIMIT**		**Res**		**VTLM_RNG**	
r						rw				rw		r		rw	

Field	Bits	Type	Description
VTLM_RNG	1:0	rw	**VTLM_RNG sets the monitored voltage range for input and output voltages** 00_B 88 V 01_B 44 V 10_B 22 V 11_B Reserved
OVIN_FAULT_LIMIT	5:4	rw	**OVIN_FAULT_LIMIT bit field sets the value of the input voltage that causes an on-chip input overvoltage (OVin) fault** 00_B 70 V 01_B 75 V 10_B 80 V 11_B 85 V

(table continues...)

(continued)

Field	Bits	Type	Description
VIN_UV_HYST	9:6	rw	**Programmable digital hysteresis for UV at respective VTLM_RNG voltages** 0_H Typical hysteresis of 2/1/0.5 V at respective VTLM_RNG voltage full scale 88/44/22 V 1_H Typical hysteresis of 3/1.5/0.75 V at respective VTLM_RNG voltage full scale 88/44/22 V 2_H Typical hysteresis of 4/2/1 V at respective VTLM_RNG voltage full scale 88/44/22 V 3_H Typical hysteresis of 5/2.5/1.25 V at respective VTLM_RNG voltage full scale 88/44/22 V 4_H Typical hysteresis of 6/3/1.5 V at respective VTLM_RNG voltage full scale 88/44/22 V 5_H Typical hysteresis of 7/3.5/1.75 V at respective VTLM_RNG voltage full scale 88/44/22 V 6_H Typical hysteresis of 8/4/2 V at respective VTLM_RNG voltage full scale 88/44/22 V 7_H Typical hysteresis of 9/4.5/2.25 V at respective VTLM_RNG voltage full scale 88/44/22 V 8_H Typical hysteresis of 9.5/4.75/2.375 V at respective VTLM_RNG voltage full scale 88/44/22 V 9_H Typical hysteresis of 10/5/2.5 V at respective VTLM_RNG voltage full scale 88/44/22 V A_H Typical hysteresis of 10.5/5.25/2.625 V at respective VTLM_RNG voltage full scale 88/44/22 V B_H Typical hysteresis of 11/5.5/2.75 V at respective VTLM_RNG voltage full scale 88/44/22 V C_H Typical hysteresis of 11.5/5.75/2.875 V at respective VTLM_RNG voltage full scale 88/44/22 V D_H Typical hysteresis of 12/6/3 V at respective VTLM_RNG voltage full scale 88/44/22 V E_H Typical hysteresis of 12.5/6.25/3.125 V at respective VTLM_RNG voltage full scale 88/44/22 V F_H Typical hysteresis of 13/6.5/3.25 V at respective VTLM_RNG voltage full scale 88/44/22 V

2.40 I_SNS_CFG command

Current sense configuration command.

I_SNS_CFG Address: $0D5_H$

I_SNS_CFG command AsyncReset value: $B418_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CS_RNG_TRIM								**CS_RNG**		**SOC_FAULT_LIMIT**			**START_ILIM**		
rw								rw		rw			rw		

Field	Bits	Type	Description
START_ILIM	2:0	rw	**START_ILIM bit field sets the startup current (IST) limit** 000_B 100% of OC 001_B 75% of OC 010_B 50% of OC 011_B 25% of OC 100_B 15% of OC 101_B 12.5% of OC 110_B 9% of OC 111_B 5% of OC
SOC_FAULT_LIMIT	5:3	rw	**SOC_FAULT_LIMIT bits set the level of the voltage drop on the sense resistor at which the SOC fault is triggered** **Configuration of SOC levels (in mV):** **I_SNS_CFG.CS_RNG[1:0] = 00B or 01B** 000_B 12.5 001_B 18.75 010_B 25 011_B 37.5 100_B 50 101_B 75 110_B 100 111_B 150 **I_SNS_CFG.CS_RNG[1:0] = 10B or 11B** 000_B 25 001_B 37.5 010_B 50 011_B 75 100_B 100 101_B 150 110_B 200 111_B 300
CS_RNG	7:6	rw	**CS_RNG bit field sets the current sense differential voltage range Vsns_cs** 00_B 12.5 mV 01_B 25 mV 10_B 50 mV 11_B 100 mV
CS_RNG_TRIM	15:8	rw	**CS_RNG_TRIM bits set the level below the V_{SNS_CS} voltage measured at the current sense pins that causes an output overcurrent fault** If the RMS_EN bit in the REG_CFG command is set, the CS_RNG_TRIM bits specify the RMS current level (as a proportion of V_{SNS_CS}) at which the OC fault is triggered. The maximum value of this bit field is 0xB4. If a value higher than this is programmed, it is limited to 0xB4

2.41 I_SNS_OFFSET_COMP command

This command specifies a systematic offset to compensate the current sense measurements in the application.

I_SNS_OFFSET_COMP Address: $0D6_H$

I_SNS_OFFSET_COMP command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					**I_SNS_OFFSET_COMP**										
r					rw										

Field	Bits	Type	Description
I_SNS_OFFSET_COMP	10:0	rw	**Value is a signed integer from -1024 to 1023, specified in 2's complement**

2.42 TSNS_LVL_CTRL command

Limit for change between pre-programmed 65°C and 125°C SOA lines during startup.

TSNS_LVL_CTRL Address: $0D7_H$

TSNS_LVL_CTRL command AsyncReset value: $07BF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**TSNS_LVL_CTRL**											
r				rw											

Field	Bits	Type	Description
TSNS_LVL_CTRL	11:0	rw	**Always leave this command to its default value 0x07BF. The change is made at 105°C**

2.43 WATCHDOG_TMR command

Turn-on watchdog configuration.

WATCHDOG_TMR Address: $0D8_H$

WATCHDOG_TMR command AsyncReset value: 67_H

7	6	5	4	3	2	1	0
EN_DG				**WATCHDOG**			
rw				rw			

Field	Bits	Type	Description
WATCHDOG	3:0	rw	**WATCHDOG sets an upper limit, in ms, on how long the unit can attempt to power up the output without fully enhancing the FET** 0_H 5 ms 1_H 10 ms 2_H 20 ms 3_H 50 ms 4_H 75 ms 5_H 100 ms 6_H 200 ms 7_H 500 ms 8_H 750 ms 9_H 1000 ms A_H 2000 ms B_H 3000 ms C_H 5000 ms D_H 7500 ms E_H 10000 ms F_H 15000 ms
EN_DG	7:4	rw	**EN_DG bit field sets the deglitch time, in ms, from the moment when the UV/EN pin crosses the V_UVEN_UTH until the INIT_SOA_REG phase starts** 0_H 0 ms 1_H 4 ms 2_H 8 ms 3_H 16 ms 4_H 32 ms 5_H 64 ms 6_H 128 ms 7_H 256 ms 8_H 300 ms 9_H 400 ms A_H 512 ms B_H Reserved … F_H Reserved

2.44 V_TMR command

Voltage faults timers.

V_TMR Address: $0D9_H$

V_TMR command AsyncReset value: $0FFF_H$

15	14 13 12	11 10 9	8 7 6	5 4 3	2 1 0
Res	**OVIN_TMR**	**Res**	**OUV_TMR**	**OV_TMR**	**UV_TMR**
r	rw	r	rw	rw	rw

Field	Bits	Type	Description
UV_TMR	2:0	rw	**UV_TMR specifies the amount of operating time in undervoltage conditions before fault is triggered** 000_B 0 ms 001_B 1 ms 010_B 5 ms 011_B 10 ms 100_B 50 ms 101_B 100 ms 110_B 500 ms 111_B 1000 ms
OV_TMR	5:3	rw	**OV_TMR specifies the amount of operating time in overvoltage conditions before fault is triggered** 000_B 0 ms 001_B 1 ms 010_B 5 ms 011_B 10 ms 100_B 50 ms 101_B 100 ms 110_B 500 ms 111_B 1000 ms
OUV_TMR	8:6	rw	**OUV_TMR specifies the amount of operating time in output undervoltage conditions before fault is triggered** 000_B 0 ms 001_B 1 ms 010_B 5 ms 011_B 10 ms 100_B 50 ms 101_B 100 ms 110_B 500 ms 111_B 1000 ms
OVIN_TMR	14:12	rw	**OVIN_TMR specifies the amount of operating time in input overvoltage conditions before the fault is triggered** 000_B 0 µs 001_B 10 µs 010_B 20 µs 011_B 50 µs 100_B 100 µs 101_B 200 µs 110_B 500 µs 111_B 1000 µs

2.45 PIN_POLARITY command

Configures polarity of PWRGD, FAULT, and WARN pins.

PIN_POLARITY Address: $0DA_H$

PIN_POLARITY command AsyncReset value: 01_H

7	6	5	4	3	2	1	0
Res					**WARN_POLARITY**	**FAULT_POLARITY**	**PWRGD_POLARITY**
r					rw	rw	rw

Field	Bits	Type	Description
PWRGD_POLARITY	0	rw	**Configures polarity of the PWRGD pin** 0_B Active low 1_B Active high
FAULT_POLARITY	1	rw	**Configures polarity of the FAULT pin** 0_B Active low 1_B Active high
WARN_POLARITY	2	rw	**Configures polarity of the WARN pin** 0_B Active low 1_B Active high

2.46 GPO_CFG command

General purpose output (GPO) configuration command.

GPO_CFG Address: $0DB_H$

GPO_CFG command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		**SMBALERT**		**GPO3_CFG**		**GPO2_CFG**		**GPO1_CFG**		**GPO0_CFG**		**GPO3_ST**	**GPO2_ST**	**GPO1_ST**	**GPO0_ST**
r		rwh		rwh		rwh		rwh		rwh		rwh	rwh	rwh	rwh

Field	Bits	Type	Description
GPO0_ST	0	rwh	**ST bits set the state (high or low) of the pins when they are configured as GPOs** GPO0_ST bit does not have any effect when the pin is configured as FAULT or SMBALERT# 0_B Output low 1_B Output high

(table continues...)

(continued)

Field	Bits	Type	Description
GPO1_ST	1	rwh	**ST bits set the state (high or low) of the pins when they are configured as GPOs** GPO1_ST bit does not have any effect when the pin is configured as WARN or LED 0_B Output low 1_B Output high
GPO2_ST	2	rwh	**ST bits set the state (high or low) of the pins when they are configured as GPOs** GPO2_ST bit does not have any effect when the pin is configured as CGDN 0_B Output low 1_B Output high
GPO3_ST	3	rwh	**ST bits set the state (high or low) of the pins when they are configured as GPOs** GPO3_ST bit does not have any effect when the pin is configured as PMBus enable or SMBALERT# 0_B Output low 1_B Output high
GPO0_CFG	5:4	rwh	**Configures GPO0 as FAULT, GPO, or SMBALERT#** Note that the SMBALERT# can be output here or in GPO3. Only one GPO must be configured as SMBALERT# 00_B Pin is configured as FAULT 01_B Pin reflects GPO0_ST status 10_B Reserved, output is low 11_B Pin is configured as SMBALERT#, depending on the GPO_CFG.SMBALERT
GPO1_CFG	7:6	rwh	**Configures GPO1 as WARN, GPO, or LED** 00_B Pin is configured as WARN 01_B Pin reflects GPO1_ST status 10_B Pin is configured as LED 11_B Reserved
GPO2_CFG	9:8	rwh	**Configures GPO2 as GPO or CGDN** 00_B Pin is configured as functional 01_B Pin reflects GPO2_ST status 10_B Pin is configured as CGDN with pull-up resistor (input) 11_B Reserved
GPO3_CFG	11:10	rwh	**Configures GPO3 as GPO, PMBus enable, or SMBALERT#** Note that the SMBALERT# can be output here or in GPO3. Only one GPO must be configured as SMBALERT# 00_B Pin is configured as functional 01_B Pin reflects GPO3_ST status 10_B PMBus enable (active high) with pull-up resistor (input) 11_B Pin is configured as SMBALERT#, depending on the GPO_CFG.SMBALERT

(table continues...)

(continued)

Field	Bits	Type	Description
SMBALERT	13:12	rwh	**SMBALERT configuration** 00_B SMBALERT# is disabled, open drain, meaning the output level is high 01_B SMBALERT# configured only for faults 10_B SMBALERT# configured only for warnings 11_B SMBALERT# configured for faults and warnings

2.47 IOUT_UC_WARN_LIMIT command

This command sets the current level that triggers an output undercurrent warning.

IOUT_UC_WARN_LIMIT Address: $0DC_H$

IOUT_UC_WARN_LIMIT command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**IOUT_UC_WARN_AVG**			**IOUT_UC_WARN_LIMIT**											
r	rw			rw											

Field	Bits	Type	Description
IOUT_UC_WARN_LIMIT	11:0	rw	**UC warning can be programmed as a fraction of V_SNS_CS**
IOUT_UC_WARN_AVG	14:12	rw	**IOUT_UC_WARN_AVG field specifies the number of samples to be averaged for UC warning limit** 000_B 1 001_B 2 010_B 4 011_B 8 100_B 16 101_B 32 110_B 64 111_B 128

2.48 ONCHIP_TSD_FAULT_LIMIT command

This command set the temperature of the device in degrees Celsius measured by the internal temperature sensor at which the on-chip thermal shut down fault is triggered.

ONCHIP_TSD_FAULT_LIMIT Address: $0DD_H$

ONCHIP_TSD_FAULT_LIMIT command AsyncReset value: 03_H

7	6	5	4	3	2	1	0
Res							**ONCHIP_TSD_FAULT_LIMIT**
r							rw

Field	Bits	Type	Description
ONCHIP_TSD_FAULT_LIMIT	1:0	rw	**Internal temperature fault limit configuration** 00_B 130°C 01_B 135°C 10_B 140°C 11_B 145°C

2.49 ENABLE_FAULTS command

This command enables or disables the faults.

ENABLE_FAULTS Address: $0DE_H$

ENABLE_FAULTS command AsyncReset value: $3EFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**OT**	**UR**	**UV**	**OV**	**OVIN**	**OUV**	**Res**	**WD**	**OC**	**SOAR**	**SOC**	**TSD**	**FET_DS**	**FET_GD**	**FET_GS**
r	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FET_GS	0	rw	**Enables or disables FET short gate-source (SGS) fault** 0_B Fault is disabled 1_B Fault is enabled
FET_GD	1	rw	**Enables or disables FET short gate-drain (SGD) fault** 0_B Fault is disabled 1_B Fault is enabled
FET_DS	2	rw	**Enables or disables FET short drain-source (SDS) fault** 0_B Fault is disabled 1_B Fault is enabled
TSD	3	rw	**Enables or disables thermal shut-down (TSD) fault** 0_B Fault is disabled 1_B Fault is enabled
SOC	4	rw	**Enables or disables severe overcurrent (SOC) fault** 0_B Fault is disabled 1_B Fault is enabled
SOAR	5	rw	**Enables or disables safe operating area regulation (SOAR) fault** 0_B Fault is disabled 1_B Fault is enabled
OC	6	rw	**Enables or disables overcurrent (OC) fault** 0_B Fault is disabled 1_B Fault is enabled

(table continues...)

(continued)

Field	Bits	Type	Description
WD	7	rw	**Enables or disables watchdog (WD) fault** 0_B Fault is disabled 1_B Fault is enabled
OUV	9	rw	**Enables or disables output undervoltage (OUV) fault** 0_B Fault is disabled 1_B Fault is enabled
OVIN	10	rw	**Enables or disables input overvoltage (OVIN) fault** 0_B Fault is disabled 1_B Fault is enabled
OV	11	rw	**Enables or disables overvoltage (OV) fault** 0_B Fault is disabled 1_B Fault is enabled
UV	12	rw	**Enables or disables undervoltage (UV) fault** 0_B Fault is disabled 1_B Fault is enabled
UR	13	rw	**Enables or disables unsuccessful retry (UR) fault** 0_B Fault is disabled 1_B Fault is enabled
OT	14	rw	**Enables or disables overtemperature (OT) fault** 0_B Fault is disabled 1_B Fault is enabled

2.50 MASK_FAULTS command

This command determines which faults are reflected in the FAULT pin.

MASK_FAULTS Address: $0DF_H$

MASK_FAULTS command AsyncReset value: $3EFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**OT**	**UR**	**UV**	**OV**	**OVIN**	**OUV**	**Res**	**WD**	**OC**	**SOAR**	**SOC**	**TSD**	**FET_DS**	**FET_GD**	**FET_GS**
r	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FET_GS	0	rw	**Masks or unmasks SGS fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin
FET_GD	1	rw	**Masks or unmasks SGD fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin

(table continues...)

(continued)

Field	Bits	Type	Description
FET_DS	2	rw	**Masks or unmasks SDS fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin
TSD	3	rw	**Masks or unmasks TSD fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin
SOC	4	rw	**Masks or unmasks SOC fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin
SOAR	5	rw	**Masks or unmasks SOAR fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin
OC	6	rw	**Masks or unmasks OC fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin
WD	7	rw	**Masks or unmasks WD fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin
OUV	9	rw	**Masks or unmasks OUV fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin
OVIN	10	rw	**Masks or unmasks OVIN fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin
OV	11	rw	**Masks or unmasks OV fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin
UV	12	rw	**Masks or unmasks UV fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin
UR	13	rw	**Masks or unmasks UR fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin
OT	14	rw	**Masks or unmasks OT fault** 0_B Fault is not reflected in the FAULT pin 1_B Fault is reflected in the FAULT pin

2.51 STATUS_FAULTS command

This command summarizes the faults status.

STATUS_FAULTS Address: $0E0_H$

STATUS_FAULTS command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	**OT**	**UR**	**UV**	**OV**	**OVIN**	**OUV**	**Res**	**WD**	**OC**	**SOAR**	**SOC**	**TSD**	**FET_DS**	**FET_GD**	**FET_GS**
r	rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
FET_GS	0	rwh	**Specifies the status of SGS fault** 0_B Fault is not detected 1_B Fault is detected
FET_GD	1	rwh	**Specifies the status of SGD fault** 0_B Fault is not detected 1_B Fault is detected
FET_DS	2	rwh	**Specifies the status of SDS fault** 0_B Fault is not detected 1_B Fault is detected
TSD	3	rwh	**Specifies the status of TSD fault** 0_B Fault is not detected 1_B Fault is detected
SOC	4	rwh	**Specifies the status of SOC fault** 0_B Fault is not detected 1_B Fault is detected
SOAR	5	rwh	**Specifies the status of SOAR fault** 0_B Fault is not detected 1_B Fault is detected
OC	6	rwh	**Specifies the status of OC fault** 0_B Fault is not detected 1_B Fault is detected
WD	7	rwh	**Specifies the status of WD fault** 0_B Fault is not detected 1_B Fault is detected
OUV	9	rwh	**Specifies the status of OUV fault** 0_B Fault is not detected 1_B Fault is detected
OVIN	10	rwh	**Specifies the status of OVIN fault** 0_B Fault is not detected 1_B Fault is detected

(table continues...)

(continued)

Field	Bits	Type	Description
OV	11	rwh	**Specifies the status of OV fault** 0_B Fault is not detected 1_B Fault is detected
UV	12	rwh	**Specifies the status of UV fault** 0_B Fault is not detected 1_B Fault is detected
UR	13	rwh	**Specifies the status of UR fault** 0_B Fault is not detected 1_B Fault is detected
OT	14	rwh	**Specifies the status of OT fault** 0_B Fault is not detected 1_B Fault is detected

2.52 ENABLE_WARNS command

This command enables or disables the warnings.

ENABLE_WARNS Address: $0E1_H$

ENABLE_WARNS command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			COMM	OP	UV	OV	OUV	OOV	OOC	OUC	SOAR	OT	TSD	FET_GS	INEG
r			rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
INEG	0	rw	**Enables or disables negative current (INEG) warning** 0_B Warning is disabled 1_B Warning is enabled
FET_GS	1	rw	**Enables or disables gate-source low voltage (VGSL) warning** 0_B Warning is disabled 1_B Warning is enabled
TSD	2	rw	**Enables or disables thermal shut-down (TSD) warning** 0_B Warning is disabled 1_B Warning is enabled
OT	3	rw	**Enables or disables overtemperature (OT) warning** 0_B Warning is disabled 1_B Warning is enabled
SOAR	4	rw	**Enables or disables safe operating area regulation (SOAR) warning** 0_B Warning is disabled 1_B Warning is enabled

(table continues...)

(continued)

Field	Bits	Type	Description
OUC	5	rw	**Enables or disables output undercurrent (OUC) warning** 0_B Warning is disabled 1_B Warning is enabled
OOC	6	rw	**Enables or disables output overcurrent (OOC) warning** 0_B Warning is disabled 1_B Warning is enabled
OOV	7	rw	**Enables or disables output overvoltage (OOV) warning** 0_B Warning is disabled 1_B Warning is enabled
OUV	8	rw	**Enables or disables output undervoltage (OUV) warning** 0_B Warning is disabled 1_B Warning is enabled
OV	9	rw	**Enables or disables overvoltage (OV) warning** 0_B Warning is disabled 1_B Warning is enabled
UV	10	rw	**Enables or disables undervoltage (UV) warning** 0_B Warning is disabled 1_B Warning is enabled
OP	11	rw	**Enables or disables overpower (OP) warning** 0_B Warning is disabled 1_B Warning is enabled
COMM	12	rw	**Enables or disables communications (COMM) warning** 0_B Warning is disabled 1_B Warning is enabled

2.53 MASK_WARNS command

This command determines which warnings are reflected in the WARN pin.

MASK_WARNS Address: $0E2_H$

MASK_WARNS command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			COMM	OP	UV	OV	OUV	OOV	OOC	OUC	SOAR	OT	TSD	FET_GS	INEG
r			rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
INEG	0	rw	**Masks or unmasks INEG warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin

(table continues...)

(continued)

Field	Bits	Type	Description
FET_GS	1	rw	**Masks or unmasks VGSL warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin
TSD	2	rw	**Masks or unmasks TSD warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin
OT	3	rw	**Masks or unmasks OT warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin
SOAR	4	rw	**Masks or unmasks SOAR warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin
OUC	5	rw	**Masks or unmasks OUC warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin
OOC	6	rw	**Masks or unmasks OOC warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin
OOV	7	rw	**Masks or unmasks OOV warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin
OUV	8	rw	**Masks or unmasks OUV warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin
OV	9	rw	**Masks or unmasks OV warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin
UV	10	rw	**Masks or unmasks UV warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin
OP	11	rw	**Masks or unmasks OP warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin
COMM	12	rw	**Masks or unmasks COMM warning** 0_B Warning is not reflected in the WARN pin 1_B Warning is reflected in the WARN pin

2.54 STATUS_WARNS command

This command summarizes the warnings status.

STATUS_WARNS Address: $0E3_H$

STATUS_WARNS command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			COM M	OP	UV	OV	OUV	OOV	OOC	OUC	SOA R	OT	TSD	FET_ GS	INEG
r			rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
INEG	0	rwh	**Specifies the status of INEG warning** 0_B Warning is not detected 1_B Warning is detected
FET_GS	1	rwh	**Specifies the status of VGSL warning** 0_B Warning is not detected 1_B Warning is detected
TSD	2	rwh	**Specifies the status of TSD warning** 0_B Warning is not detected 1_B Warning is detected
OT	3	rwh	**Specifies the status of OT warning** 0_B Warning is not detected 1_B Warning is detected
SOAR	4	rwh	**Specifies the status of SOAR warning** 0_B Warning is not detected 1_B Warning is detected
OUC	5	rwh	**Specifies the status of OUC warning** 0_B Warning is not detected 1_B Warning is detected
OOC	6	rwh	**Specifies the status of OOC warning** 0_B Warning is not detected 1_B Warning is detected
OOV	7	rwh	**Specifies the status of OOV warning** 0_B Warning is not detected 1_B Warning is detected
OUV	8	rwh	**Specifies the status of OUV warning** 0_B Warning is not detected 1_B Warning is detected
OV	9	rwh	**Specifies the status of OV warning** 0_B Warning is not detected 1_B Warning is detected

(table continues...)

(continued)

Field	Bits	Type	Description
UV	10	rwh	**Specifies the status of UV warning** 0_B Warning is not detected 1_B Warning is detected
OP	11	rwh	**Specifies the status of OP warning** 0_B Warning is not detected 1_B Warning is detected
COMM	12	rwh	**Specifies the status of COMM warning** 0_B Warning is not detected 1_B Warning is detected

2.55 PWRGD_DG_TMR command

This command sets the deglitch time after the PWRGD signal assertion (bits [7:4]) and deassertion (bits [3:0]).

PWRGD_DG_TMR Address: $0E4_H$

PWRGD_DG_TMR command AsyncReset value: $F0_H$

7	6	5	4	3	2	1	0
PWRGD_DG_TMR				**PWRGDN_DG_TMR**			
rw				rw			

Field	Bits	Type	Description
PWRGDN_DG_TMR	3:0	rw	**Programmable from 0 ms to 15 ms in 1 ms steps. 1 LSB = 1 ms**
PWRGD_DG_TMR	7:4	rw	**Programmable from 0 ms to 15 ms in 1 ms steps. 1 LSB = 1 ms**

2.56 SOA_TMR command

FET SOA protection timers.

SOA_TMR Address: $0E5_H$

SOA_TMR command AsyncReset value: $003A_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			**RMS_SAMPLE_TMR**		**SOC_DG_TMR**		**SOC_TMR**			**SOAR_TMR**			**SOAD_TMR**		
r			rw		rw		rw			rw			rw		

Field	Bits	Type	Description
SOAD_TMR	2:0	rw	**SOAD_TMR sets the deglitch time after SOA violation conditions have been detected and before SOA regulation phase starts** 000_B 0 ms 001_B 0.5 ms 010_B 1 ms 011_B 2 ms 100_B 4 ms 101_B 6 ms 110_B 8 ms 111_B 10 ms
SOAR_TMR	5:3	rw	**SOAR_TMR specifies the operating time in OC or SOA regulation (I_REG) state before fault is triggered** 000_B 0 ms 001_B 1 ms 010_B 5 ms 011_B 10 ms 100_B 50 ms 101_B 100 ms 110_B 500 ms 111_B 1000 ms
SOC_TMR	8:6	rw	**SOC_TMR specifies the time that the device operates in SOC condition before fault is triggered** 000_B 0 ms 001_B 0.01 ms 010_B 0.1 ms 011_B 1 ms 100_B 10 ms 101_B 100 ms 110_B 500 ms 111_B 1000 ms
SOC_DG_TMR	10:9	rw	**SOC_DG_TMR specifies the deglitch time of the analog comparator that detects the SOC condition** 00_B 0 ns 01_B 200 ns 10_B 500 ns 11_B 1000 ns
RMS_SAMPLE_TMR	12:11	rw	**RMS_SAMPLE_TMR specifies the number of samples taken for the RMS current protection calculation. In other words, the integration time** 00_B 1.64 ms 01_B 13.11 ms 10_B 104.86 ms 11_B 838.86 ms

2.57 TURN_OFF_CTRL command

Fast and two-step turn off settings.

TURN_OFF_CTRL Address: $0E6_H$

TURN_OFF_CTRL command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			GATE_PD_TMR										GATE_SLOW_PD		GATE_FAST_PD
r			rw										rw		rw

Field	Bits	Type	Description
GATE_FAST_PD	0	rw	**GATE_FAST_PD sets the current level for the first phase of the two-step turn off** • If GATE_FAST_PD = 0: GATE_SLOW_PD and GATE_PD_TMR are ignored. Gate discharges with a single continuous phase of 1.5 A • If GATE_FAST_PD = 1: - When GATE_PD_TMR = 0: GATE_FAST_PD is ignored. Gate discharges with a single continuous phase of GATE_SLOW_PD - When GATE_PD_TMR different than 0: Gate discharges with two-step turn off 0_B 1.5 A 1_B 50 mA
GATE_SLOW_PD	2:1	rw	**Sets the current level of the second phase of the two-step turn off** 00_B 250 µA 01_B 500 µA 10_B 750 µA 11_B 1250 µA
GATE_PD_TMR	12:3	rw	**GATE_PD_TMR sets the time of the first phase of the two-step controlled turn off** • This timer can be configured from 0 ns to 25575 ns in 25 ns steps • When timer is set to 0 ns, gate discharges slowly with GATE_SLOW_PD • The minimum allowed time to be programmed in GATE_PD_TMR (if it is not 0) is 250 ns

2.58 RETRY command

Retry settings.

RETRY Address: $0E7_H$

RETRY command AsyncReset value: $3FBF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	GATE_REC_EN	MASK_WDG	MASK_OUV	MASK_OC	MASK_SOC	MASK_SOAR	RETRY_COUNTER			RETD_TMR			COOLD_TMR		
r	rw	rw	rw	rw	rw	rw	rw			rw			rw		

Field	Bits	Type	Description
COOLD_TMR	2:0	rw	**COOLD_TMR bits set the cool-down period in seconds between power-up retries** 000_B 0 s 001_B 1 s 010_B 2 s 011_B 4 s 100_B 8 s 101_B 16 s 110_B 32 s 111_B 64 s
RETD_TMR	5:3	rw	**RETD_TMR bits set the retry ok deglitch timer in seconds, which controls the time, after PWRGD signal is achieved in a retry attempt, after which the retry counter is reset** 000_B 0 s 001_B 0.5 s 010_B 1 s 011_B 2 s 100_B 3 s 101_B 4 s 110_B 6 s 111_B 8 s
RETRY_COUNTER	8:6	rw	**RETRY_COUNTER bits set the number of times the system will retry power-up after a retry configured fault has occurred** 000_B 0 (latch-off after the first retry fault) 001_B 1 010_B 2 011_B 4 100_B 8 101_B 16 110_B 32 111_B Infinite
MASK_SOAR	9	rw	**MASK_x bits define if the cool down period is enabled or disabled after a specific fault retry** The RETRY_COUNTER setting is also ignored if these bits are cleared 0_B **Disable**: Cool-down period after SOAR fault disabled and RETRY_COUNTER setting ignored 1_B **Enable**: Cool-down period after SOAR fault enabled and retry setting is given by RETRY_COUNTER

(table continues...)

(continued)

Field	Bits	Type	Description
MASK_SOC	10	rw	**MASK_x bits define if the cool-down period is enabled or disabled after a specific fault retry** The RETRY_COUNTER setting is also ignored if these bits are cleared 0_B **Disable**: Cool-down period after SOC fault disabled and RETRY_COUNTER setting ignored 1_B **Enable**: Cool-down period after SOC fault enabled and retry setting is given by RETRY_COUNTER
MASK_OC	11	rw	**MASK_x bits define if the cool-down period is enabled or disabled after a specific fault retry** The RETRY_COUNTER setting is also ignored if these bits are cleared 0_B **Disable**: Cool-down period after OC fault disabled and RETRY_COUNTER setting ignored 1_B **Enable**: Cool-down period after OC fault enabled and retry setting is given by RETRY_COUNTER
MASK_OUV	12	rw	**MASK_x bits define if the cool-down period is enabled or disabled after a specific fault retry** The RETRY_COUNTER setting is also ignored if these bits are cleared 0_B **Disable**: Cool-down period after OUV fault disabled and RETRY_COUNTER setting ignored 1_B **Enable**: Cool-down period after OUV fault enabled and retry setting is given by RETRY_COUNTER
MASK_WDG	13	rw	**MASK_x bits define if the cool-down period is enabled or disabled after a specific fault retry** The RETRY_COUNTER setting is also ignored if these bits are cleared 0_B **Disable**: Cool-down period after watchdog fault disabled and RETRY_COUNTER setting ignored 1_B **Enable**: Cool-down period after watchdog fault enabled and retry setting is given by RETRY_COUNTER
GATE_REC_EN	14	rw	**GATE_REC_EN bit enables the gate fast recovery feature** 0_B **Disable**: Gate fast recovery disabled 1_B **Enable**: Gate fast recovery enabled

2.59 TELEMETRY_EN command

This command enables or disables each of the telemetry features.

TELEMETRY_EN Address: $0E8_H$

TELEMETRY_EN command AsyncReset value: 7600_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ_EIN_EN	**READ_VIN_EN**	**READ_VOUT_EN**	**READ_IOUT_EN**	**READ_TEMP_1_EN**	**READ_TEMP_2_EN**	**READ_PIN_EN**	**READ_VIN_PEAK_EN**	**READ_VOUT_PEAK_EN**	**READ_IOUT_PEAK_EN**	**READ_PIN_PEAK_EN**	**READ_TEMP_1_PEAK_EN**	**READ_VIN_VALLEY_EN**	**READ_VOUT_VALLEY_EN**	**READ_IOUT_VALLEY_EN**	**READ_TEMP_1_VALLEY_EN**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
READ_TEMP_1_VALLEY_EN	0	rw	**Enables or disables external temperature valley reading** 0_B Feature disabled 1_B Feature enabled
READ_IOUT_VALLEY_EN	1	rw	**Enables or disables output current valley reading** 0_B Feature disabled 1_B Feature enabled
READ_VOUT_VALLEY_EN	2	rw	**Enables or disables output voltage valley reading** 0_B Feature disabled 1_B Feature enabled
READ_VIN_VALLEY_EN	3	rw	**Enables or disables input voltage valley reading** 0_B Feature disabled 1_B Feature enabled
READ_TEMP_1_PEAK_EN	4	rw	**Enables or disables external temperature peak reading** 0_B Feature disabled 1_B Feature enabled
READ_PIN_PEAK_EN	5	rw	**Enables or disables input power peak reading** 0_B Feature disabled 1_B Feature enabled
READ_IOUT_PEAK_EN	6	rw	**Enables or disables output current peak reading** 0_B Feature disabled 1_B Feature enabled
READ_VOUT_PEAK_EN	7	rw	**Enables or disables output voltage peak reading** 0_B Feature disabled 1_B Feature enabled
READ_VIN_PEAK_EN	8	rw	**Enables or disables input voltage peak reading** 0_B Feature disabled 1_B Feature enabled
READ_PIN_EN	9	rw	**Enables or disables input power calculation** 0_B Feature disabled 1_B Feature enabled
READ_TEMP_2_EN	10	rw	**Enables or disables internal temperature reading** 0_B Feature disabled 1_B Feature enabled
READ_TEMP_1_EN	11	rw	**Enables or disables external temperature reading** 0_B Feature disabled 1_B Feature enabled
READ_IOUT_EN	12	rw	**Enables or disables output current reading** 0_B Feature disabled 1_B Feature enabled

(table continues...)

(continued)

Field	Bits	Type	Description
READ_VOUT_EN	13	rw	**Enables or disables output voltage reading** 0_B Feature disabled 1_B Feature enabled
READ_VIN_EN	14	rw	**Enables or disables input voltage reading** 0_B Feature disabled 1_B Feature enabled
READ_EIN_EN	15	rw	**Enables or disables energy calculation** 0_B Feature disabled 1_B Feature enabled

2.60 TELEMETRY_AVG command

This command sets the number of averaging samples for reporting power (P_TELEMETRY_AVG), voltage (V_TELEMETRY_AVG), and current (I_TELEMETRY_AVG) telemetry.

TELEMETRY_AVG Address: $0E9_H$

TELEMETRY_AVG command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res							**P_TELEMETRY_AVG**			**V_TELEMETRY_AVG**			**I_TELEMETRY_AVG**		
r							rw			rw			rw		

Field	Bits	Type	Description
I_TELEMETRY_AVG	2:0	rw	**Current telemetry averaging** 000_B 1 001_B 2 010_B 4 011_B 8 100_B 16 101_B 32 110_B 64 111_B 128
V_TELEMETRY_AVG	5:3	rw	**Voltage telemetry averaging** 000_B 1 001_B 2 010_B 4 011_B 8 100_B 16 101_B 32 110_B 64 111_B 128

(table continues...)

(continued)

Field	Bits	Type	Description
P_TELEMETRY_AVG	8:6	rw	**Power telemetry averaging** 000_B 1 001_B 2 010_B 4 011_B 8 100_B 16 101_B 32 110_B 64 111_B 128

2.61 WRITE_OTP command

Write OTP configuration command.

WRITE_OTP Address: $0EA_H$

WRITE_OTP command AsyncReset value: 00_H

7	6	5	4	3	2	1	0
Res					**SEL_SEC**		**WRITE_OTP**
r					rw		w

Field	Bits	Type	Description
WRITE_OTP	0	w	**The WRITE_OTP bit, when set, writes the information to the selected section** 0_B **DISABLE**: No writing to OTP 1_B **ENABLE**: Write OTP
SEL_SEC	2:1	rw	**OTP is divided in three sections: User OTP, MTP, and SOA. The SEL_SEC bits select the section to be written** 00_B **USER**: User programing OTP 01_B **SOA**: SOA programing 10_B **MTP**: MTP programing 11_B **RESERVED**: Reserved

2.62 STATUS_MEM command

Memory status command.

STATUS_MEM Address: $0EB_H$

STATUS_MEM command AsyncReset value: 00_H

7	6	5	4	3	2	1	0
PROG_BLOCK	**OTP_FAIL**	**MTP_FULL**	**MTP_USER**	**OTP_USER**	**SOA_PRG**	**SOA_FULL**	**SOA_CRC**
rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
SOA_CRC	0	rh	**CRC check status on the data inside the FIFO** 0_B **FAIL**: CRC has not been performed or did not pass 1_B **PASS**: CRC passed
SOA_FULL	1	rh	**Indication if the FIFO (data + CRC) is full or not** 0_B **EMPTY**: SOA FIFO not full 1_B **FULL**: SOA FIFO is full and CRC has been performed
SOA_PRG	2	rh	**SOA section of the OTP if it has been programmed or virgin** 0_B **VIRGIN**: Section is virgin 1_B **PROGRAMMED**: Section has been programmed
OTP_USER	3	rh	**Indication if the configuration registers in OTP have been programmed or not** 0_B **VIRGIN**: Configuration commands have not been programmed 1_B **PROGRAMMED**: Configuration commands have been programmed
MTP_USER	4	rh	**Indication if MTP is in use or not** 0_B **NOT_USED**: MTP is not in use 1_B **USED**: MTP is in use
MTP_FULL	5	rh	**Indication if all the MTP memory has been used** 0_B **NOT_FULL**: Not all MTP pages have been used 1_B **FULL**: All MTP pages have been used
OTP_FAIL	6	rh	**Indication if the programming or the readout of the OTP has been successful or not** 0_B **PASS**: See PROG_BLOCK 1_B **FAIL**: See PROG_BLOCK
PROG_BLOCK	7	rh	**Indication if programming is allowed or if it has been blocked because of voltage or temperature out of range** 0_B **ENABLED**: OTP_FAIL is unset: OTP, MTP, or OTP SOA programming has succeeded if the OTP_USER, MTP_USER, or SOA_PRG bits are set. Otherwise, programming has not started OTP_FAIL is set: OTP or MTP programming started but failed during programming because of OTP issue. Part must be discarded 1_B **BLOCKED**: OTP_FAIL is unset: OTP or MTP programming has been blocked because temperature or input supply are out of range OTP_FAIL is set: OTP or MTP programming started but failed during programming because temperature or voltage going out of range during programming. Part must be discarded

2.63 RESTART command

This command turns-off the hot-swap for 10 seconds. Then it is automatically turned back on. This command is write-only without a data byte.

RESTART Address: $0EC_H$

RESTART command Reset values see: Table 4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESTART															
w															

Field	Bits	Type	Description
RESTART	15:0	w	**This command turns-off the hot-swap for 10 seconds. Then it is automatically turned back on**

Table 4 Reset values of RESTART

Reset	Reset value	Note
AsyncReset	$UUUU_H$	Undefined - Not applicable

2.64 READ_IOUT_RMS command

This command retrieves the calculated squared RMS value of the current flow over the sense resistor. To enable and configure RMS calculation, RMS_EN bit in REG_CFG command and READ_IOUT_EN in TELEMETRY_EN command must be enabled. The number of samples for the calculation can be configured by means of the RMS_SAMPLE_TMR in the SOA_TMR command.

READ_IOUT_RMS Address: $0ED_H$

READ_IOUT_RMS command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ_IOUT_RMS															
rh															

Field	Bits	Type	Description
READ_IOUT_RMS	15:0	rh	**RMS current measurement squared**

2.65 READ_PIN_EXT command

This command returns the input power of the system as a product of VIN * IOUT.

READ_PIN_EXT Address: $0EE_H$

READ_PIN_EXT command AsyncReset value: $00\ 0000_H$

23	22	21	20	19	18	17	16
READ_PIN_EXT							
rh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
READ_PIN_EXT															
rh															

Field	Bits	Type	Description
READ_PIN_EXT	23:0	rh	**Returns the input power calculation in PMBus direct format**

2.66 READ_VIN_PEAK command

This command stores the maximum VIN value read. The command is automatically cleared when the data is read.

READ_VIN_PEAK Address: $0EF_H$

READ_VIN_PEAK command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**READ_VIN_PEAK**											
r				rh											

Field	Bits	Type	Description
READ_VIN_PEAK	11:0	rh	**Stores the maximum VIN value read**

2.67 READ_VOUT_PEAK command

This command stores the maximum VOUT value read. The command is automatically cleared when the data is read.

READ_VOUT_PEAK Address: $0F0_H$

READ_VOUT_PEAK command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**READ_VOUT_PEAK**											
r				rh											

Field	Bits	Type	Description
READ_VOUT_PEAK	11:0	rh	**Stores the maximum VOUT value read**

2.68 READ_IOUT_PEAK command

This command stores the maximum IOUT value read. The command is automatically cleared when the data is read.

READ_IOUT_PEAK Address: $0F1_H$

READ_IOUT_PEAK command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				**READ_IOUT_PEAK**											
r				rh											

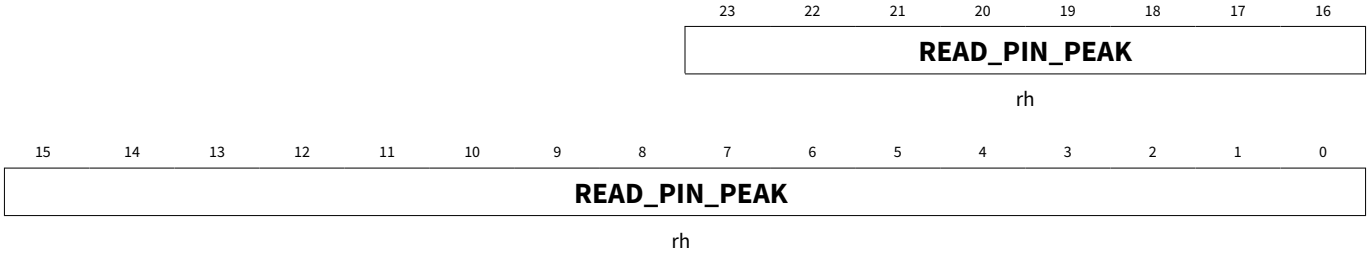
Field	Bits	Type	Description
READ_IOUT_PEAK	11:0	rh	**Stores the maximum IOUT value read**

2.69 READ_PIN_PEAK command

This command stores the maximum PIN value read. The command is automatically cleared when the data is read.

READ_PIN_PEAK Address: $0F2_H$

READ_PIN_PEAK command AsyncReset value: $00\ 0000_H$



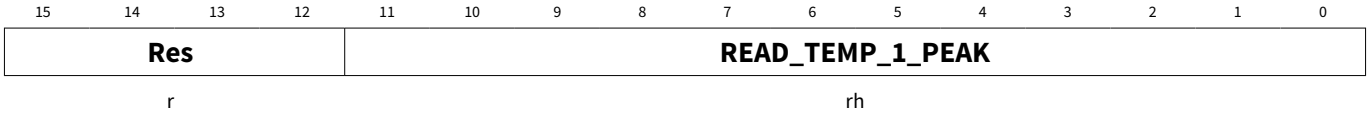
Field	Bits	Type	Description
READ_PIN_PEAK	23:0	rh	**Stores the maximum PIN value read**

2.70 READ_TEMP_1_PEAK command

This command stores the maximum external temperature value read. The command is automatically cleared when the data is read.

READ_TEMP_1_PEAK Address: $0F3_H$

READ_TEMP_1_PEAK command AsyncReset value: 0000_H



Field	Bits	Type	Description
READ_TEMP_1_PEAK	11:0	rh	**Stores the maximum external temperature value read**

2.71 READ_VIN_VALLEY command

This command stores the minimum VIN value read. The command is automatically cleared when the data is read.

READ_VIN_VALLEY Address: $0F4_H$

READ_VIN_VALLEY command AsyncReset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				READ_VIN_VALLEY											
r				rh											

Field	Bits	Type	Description
READ_VIN_VALLEY	11:0	rh	**Stores the minimum VIN value read**

2.72 READ_VOUT_VALLEY command

This command stores the minimum VOUT value read. The command is automatically cleared when the data is read.

READ_VOUT_VALLEY Address: $0F5_H$

READ_VOUT_VALLEY command AsyncReset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				READ_VOUT_VALLEY											
r				rh											

Field	Bits	Type	Description
READ_VOUT_VALLEY	11:0	rh	**Stores the minimum VOUT value read**

2.73 READ_IOUT_VALLEY command

This command stores the minimum IOUT value read. The command is automatically cleared when the data is read.

READ_IOUT_VALLEY Address: $0F6_H$

READ_IOUT_VALLEY command AsyncReset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				READ_IOUT_VALLEY											
r				rh											

Field	Bits	Type	Description
READ_IOUT_VALLEY	11:0	rh	**Stores the minimum IOUT value read**

2.74 READ_TEMP_1_VALLEY command

This command stores the minimum external temperature value read. The command is automatically cleared when the data is read.

READ_TEMP_1_VALLEY Address: $0F7_H$

READ_TEMP_1_VALLEY command AsyncReset value: $0FFF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				READ_TEMP_1_VALLEY											
r				rh											

Field	Bits	Type	Description
READ_TEMP_1_VALLEY	11:0	rh	**Stores the minimum external temperature value read**

2.75 STATUS_MODE command

This command shows the operating mode, configured FET, device address, and start up current.

STATUS_MODE Address: $0F9_H$

STATUS_MODE command AsyncReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GATE_STATUS		PWRGD_STATUS	SELECTED_IST			SELECTED_DEVICE_ADDRESS				SELECTED_FET				STATUS_MODE	
rh		rh	rh			rh				rh				rh	

Field	Bits	Type	Description
STATUS_MODE	1:0	rh	**Shows current operating mode** 00_B **FDM_DCM**: Fully digital mode with digital comparators 01_B **FDM_ACM**: Fully digital mode with analog comparators 10_B **AADM**: Analog assisted digital mode 11_B Reserved
SELECTED_FET	5:2	rh	**Shows configured FET** 0_H BSC027N10NS5ATMA1 1_H BSC035N10NS5ATMA1 2_H BSC040N10NS5ATMA1 3_H IPTG011N08NM5 4_H IPTC012N08NM5 5_H IPB017N10N5LFATMA1 6_H BSC093N15NS5 7_H BSC074N15NS5 8_H IPTG014N10NM5 9_H IPTC015N10NM5 A_H IPT015N10N5ATMA1 B_H IPB017N10N5ATMA1 C_H IPB018N10NM6 D_H IPT013N08NM5LF E_H IPB020N10N5ATMA1 F_H Programmed in MODE.FET_SELECT command bit

(table continues...)

(continued)

Field	Bits	Type	Description
SELECTED_DEVICE_ADDRESS	9:6	rh	**LSB part of the PMBus address [3:0]** 0_H PMBus address [3:0] - 4'b0000 1_H PMBus address [3:0] - 4'b0001 2_H PMBus address [3:0] - 4'b0010 3_H PMBus address [3:0] - 4'b0011 4_H PMBus address [3:0] - 4'b0100 5_H PMBus address [3:0] - 4'b0101 6_H PMBus address [3:0] - 4'b0110 7_H PMBus address [3:0] - 4'b0111 8_H PMBus address [3:0] - 4'b1000 9_H PMBus address [3:0] - 4'b1001 A_H PMBus address [3:0] - 4'b1010 B_H PMBus address [3:0] - 4'b1011 C_H PMBus address [3:0] - 4'b1100 D_H PMBus address [3:0] - 4'b1101 E_H PMBus address [3:0] - 4'b1110 F_H Programmed in PMBUS_CFG.PMBUS_DEVICE_ADDR command bit
SELECTED_IST	12:10	rh	**Shows selected IST** 000_B OC range 25 mV; Startup current limit: Set by START_ILIM bits in I_SNS_CFG register (100% of OC range by default) 001_B OC range 25 mV; Startup current limit: 50% of OC range 010_B OC range 25 mV; Startup current limit: 25% of OC range 011_B OC range 25 mV; Startup current limit: 12.5% of OC range 100_B OC range 12.5 mV; Startup current limit: 12.5% of OC range 101_B OC range 12.5 mV; Startup current limit: 25% of OC range 110_B OC range 12.5 mV; Startup current limit: 50% of OC range 111_B OC range 12.5 mV; Startup current limit: Set by START_ILIM bits in I_SNS_CFG command (100% of OC range by default) or in case of FDM
PWRGD_STATUS	13	rh	**PWRGD signal status** Note that this bit follows the PWRGD pin status, while PG_STATUS in STATUS_WORD command shows the status of the system power directly 0_B PWRGD pin is deasserted 1_B PWRGD pin is asserted
GATE_STATUS	15:14	rh	**Shows the status of the GATE pin (VGS comparators)** 00_B GATE pin is low (VGS1 = 0 and VGS2 = 0) 01_B GATE pin is high (VGS1 = 1 and VGS2 = 1) 10_B GATE pin is in regulation (VGS1 = 0 and VGS2 = 1) 11_B Reserved

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Document version	Date of release	Description of changes
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