EZ-PD™ CCG7SA4F automotive rear-seat charger (RSC) solution demo test report

About this document

Scope and purpose

This document provides test results of single-port EZ-PD™ CCG7SA4F USB Type-C PD and buck-boost controller in automotive 65 W rear-seat charger solution demo.

Intended audience

Automotive rear-seat charger, head-unit charger, and rear-seat entertainment power electronics hardware designers using EZ-PD™ CCG7SA4F USB Type-C PD and buck-boost controller.

Abbreviations and definitions

Table 1 Abbreviations

Abbreviation	Definition
CC-CV	constant current – constant voltage
CE	conducted emission
CH'x'	oscilloscope channel numbers
DCM	discontinuous current mode
DP/DM	USB data plus/data minus lines
DUT / EUT	device under test/equipment under test
ESD	electrostatic discharge
FCCM	forced continuous conduction mode
FET	MOSFET (metal oxide semiconductor field effect transistor)
OCP	overcurrent protection
OTP	overtemperature protection
OVP	overvoltage protection
PDO	Power Delivery output
P-P	peak-to-peak
PPS	programmable power supply
PSM	pulse skip mode
SCP	short-circuit protection
SW1, SW2	buck converter switch node, boost converter switch node
UI	user interface
USB PD	Universal Serial Bus Power Delivery
V_{BUS}	bus voltage at Type-C i.e., after Provider/NGDO FET
V_{BUS}/V_{OUT}	output voltage of the DUT
V_{IN}/V_{IN_DC}	input DC voltage to the DUT

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1 Introduction

The EZ-PD™ CCG7SA4F automotive rear-seat charger (RSC) solution demo test report presents electrical performance parameters like efficiency, ripple, regulation, constant-voltage, and constant-current operation, output current transient response, output voltage transition, startup turn-on delay, startup rise time, and fault protection performance. This test report presents the thermal performance of the rear-seat charger at room temperature. This test report showcases the switch voltage stress waveforms and stress test performance waveforms.

This test report presents regulatory standards pre-compliance performance of the EZ-PD™ CCG7SA4F RSC solution demo board per the following standards:

Table 2 List of standards applicable to EZ-PD™ CCG7SA4F RSC solution demo

Test	Standards
Electrical transient tests	• **ISO 7637-2**: Road vehicles – Electrical disturbances from conduction and coupling
Environmental conditions and testing	• **ISO 16750-2**: Road vehicles – Environmental conditions and testing for electrical and electronic equipment • **CISPR 25 Class 5**: Conducted emission test scans • **ISO 10605**: Road vehicles – Test methods for electrical **disturbances** from electrostatic discharge (ESD)

This test report captures USB IF regulatory pre-compliance performance of QuadraMAX, Ellisys, GRL, and LeCroy.

The USB PD automotive RSC needs to deliver a wide range of configured positive output voltage and power from a nominal 12 V automotive battery. A four-switch buck-boost converter (FSBBC) is a suitable topology, which can support variable input voltages and configurable output voltage applications such as USB PD where high efficiency and power density are also required. The FSBBC configuration can act like a buck, boost, or buck-boost converter to provide an output voltage with the same polarity as the input voltage. Improved efficiency of the FSBBC is observed due to synchronous rectification. Along similar lines, buck-only and boost-only operations can be achieved.

Constant-frequency peak current-mode control (PCMC) is a popular control technique for switched-mode power converters. PCMC offers built-in overcurrent protection, robust dynamic responses, simplified loop compensator design, and rejection of input voltage disturbances.

EZ-PD™ CCG7SA4F, a single-port USB Type-C PD controller with an integrated buck-boost DC-DC controller, controls the rear-seat charging solution board. It complies with the latest USB Type-C and PD specifications and is targeted for automotive charger applications such as head-unit chargers, rear-seat chargers, and rear-seat entertainment.

Integration offered by EZ-PD™ CCG7SA4F not only reduces the BOM but also provides a footprint-optimized solution for automotive charging needs. EZ-PD™ CCG7SA4F has integrated gate drivers for VBUS NFET on the provider path. EZ-PD™ CCG7SA4F has integrated buck-boost side NFETs. It also includes hardware-controlled protection features on the VBUS. EZ-PD™ CCG7SA4F supports a wide input voltage range (4 V–24 V with 40 V tolerance) and programmable switching frequency (150 kHz – 600 kHz) in an integrated PD solution. The USB PD Type-C rear seat charger reference board with EZ-PD™ CCG7SA4F controller application note provides insights to design a rear-seat charger solution.

A high-level block diagram of the EZ-PD™ CCG7SA4F-based single-output USB PD automotive rear-seat charger is shown in Figure 1.

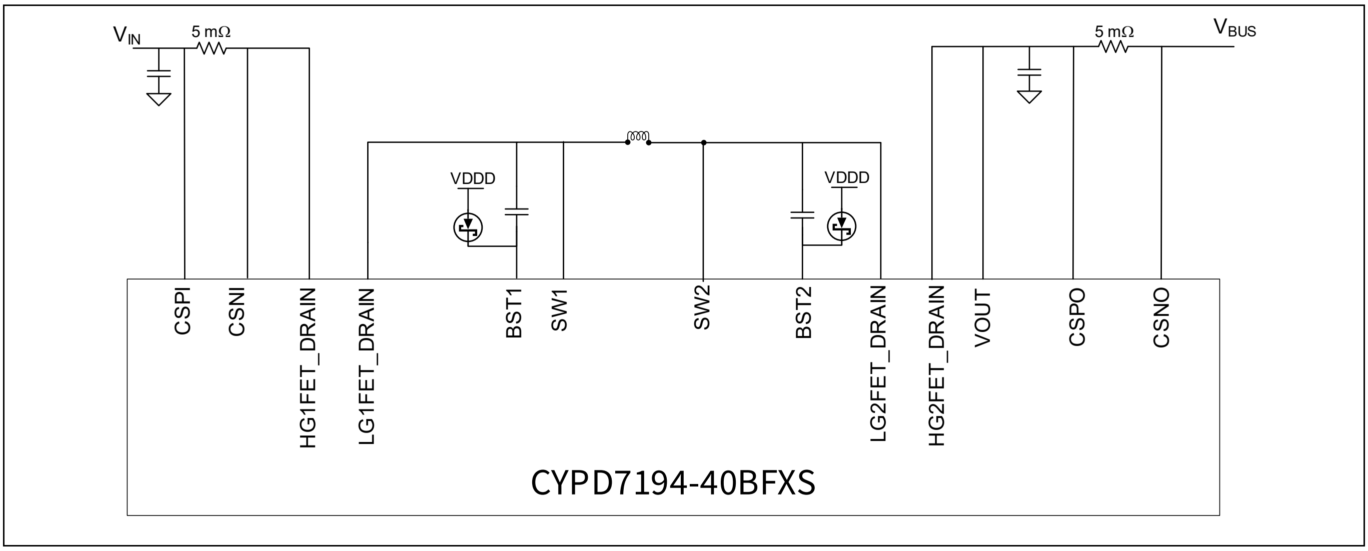


Figure 1 **EZ-PD™ CCG7SA4F-based single-output USB PD automotive 65 W rear-seat charger**

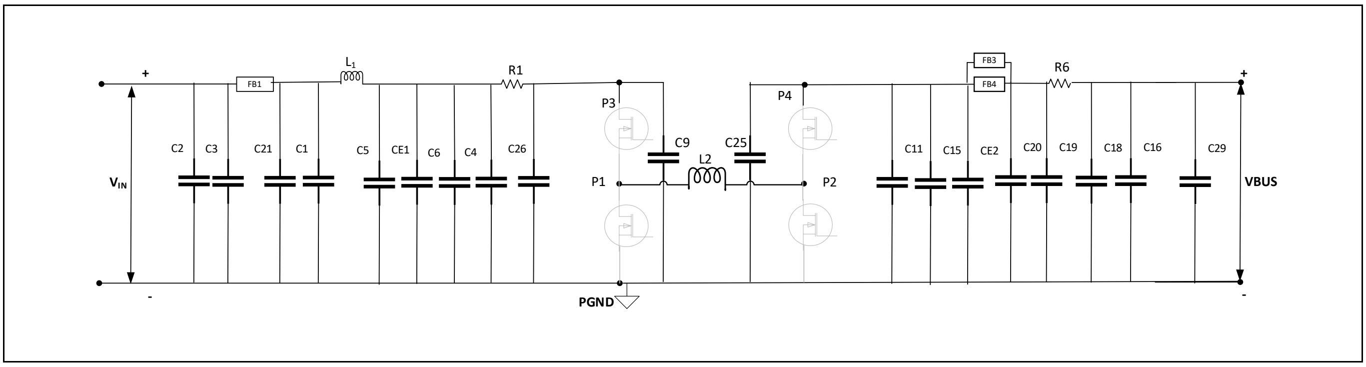


Figure 2 **High-level block diagram of 65 W RSC solution board power stage**

Table 3 Critical components BOM

Designator	Description	Part number	Manufacturer
U1	EZ-PD™ CCG7SA4F automotive single-port USB Type-C PD and buck-boost controller (40-pin QFN)	CYPD7194-40BFXS	Infineon
FB1	FERRITE BEAD 50 OHM 1206 1LN	BLM31SN500SH1L	Murata
FB3, FB4	Powerline ferrite bead 0805, 06 A 4.0 mΩ	BLM21SN300SH1D	Murata
L1	Fixed inductors 220 nH Shld 20%	XGL3530-181MEC	CoilCraft
L2	Fixed inductors 6.8 µH 20%	XGL6060-682MEC	CoilCraft
C1, C3, C4, C11, C15, C20, C21	CAP CER 10UF 50V X7R 1206 AEC-Q200	CGA5L1X7R1H106K160AC	TDK Corporation
C9, C25, C26	CAP CER 4.7UF 50V X7R 0805 AEC-Q200	CGA4J1X7R1H475K125AE	TDK Corporation
C16	CAP CER 0.1UF 50V X7R 0603 AEC-Q200	GCM188R71H104KA57J	Murata
C18	CAP CER 10000PF 50V X7R 0402	CL05B103KB5VPNC	Samsung
C2	CAP CER 10000PF 50V X7R 0603 AEC-Q200	GCD188R71H103KA01D	Murata
C5, C6	CAP CER 1UF 50V X7R 0805 AEC-Q200	GCM21BR71H105KA03K	Murata
C19	CAP CER 10000PF 50V X7R 0603	CL10B103KB8WPNC	Samsung
C29	CAP CER 1UF 10V X7R 0603	CL10B105KP8VPNC	Samsung

RSC solution PCB details are shown in Table 4.

Table 4 PCB details

PCB layer	Copper thickness	Details
Top layer	2 oz.	Components, power traces
Second layer	2 oz.	Ground layer
Third layer	2 oz.	High-frequency traces, control-signal traces
Bottom layer	2 oz.	Ground and power components thermal pads
Board size	–	45 mm × 32 mm
Board thickness	–	1.6 mm

2 EZ-PD™ CCG7SA4F automotive 65 W RSC solution demo specifications

Table 5 Test specifications

Parameter	Value
Input voltage	5.5 V_{DC} – 18 V_{DC}
Max output power	65 W on port with a maximum load current of 3.25 A
Output voltage	**Fixed PDOs**: 5 V/3.25 A, 9 V/3.25 A, 15 V/3.25 A, 20 V/3.25 A **PPS**: 5 V–16 V, 3.25 A; 5 V–21 V, 3.25 A with PPS power limit **AVS**: 9.0 V to 15.0 V, 3.25 A; 15.0 V to 20.0 V, 3.25 A
Peak efficiency	Table 8
Protections	1. Input overvoltage protection 2. Input undervoltage protection 3. V_{BUS} overvoltage protection (OVP) 4. V_{BUS} undervoltage protection (UVP) 5. Overcurrent protection (OCP) 6. Short-circuit protection (SCP) 7. Overtemperature protection (OTP) 8. VBUS-to-CC short protection 9. V_{CONN} overcurrent protection 10. V_{CONN} short-circuit protection 11. Reverse-current protection (RCP)
Power throttling	1. Programmable input voltage throttling: a) 18 V_{DC} ≥ V_{IN} ≥ 11 V_{DC} 65 W b) 11 V_{DC} > V_{IN} ≥ 09 V_{DC} 48.75 W c) 09 V_{DC} > V_{IN} ≥ 5.5 V_{DC} 32.5 W 2. Programmable thermal throttling: a) -40°C ≤ T < 90°C 65 W b) +90°C ≤ T < 105°C 32.5 W
Charging standards supported	1. USB-C PD v3.2.1.1 2. Apple Charging 2.4 A 3. Qualcomm QC 2.0, 3.0, 4.0, 5.0 4. Samsung AFC 5. USB BC 1.2

Note: The maximum delivered power will be based on input voltage throttling.

3 Test setup

The RSC solution board, firmware version details, and EZ-PD™ CCG7SA4F configuration details are shown in Table 6.

Table 6 DUT hardware and software configurations

DUT contents	Description	Remarks
Hardware – configuration		
EZ-PD™ CCG7SA4F automotive rear-seat charger (RSC) solution demo	REF_CCG7SA4F_65W_RSC_REV04	Circuit schematics, BOM, and PCB layout
Firmware		
Firmware version	Build #320	GURNANI-80 *B
CCG7S – configuration		
System clock	24 MHz	Default configuration
Gate drive strength Pull-up drive strength: LG1, LG2 – 2.9 Ω, HG1, HG2 – 3.3 Ω Pull-down drive strength: LG1, LG2 – 3.1 Ω, HG1, HG2 – 3.4 Ω	0x7	Default configuration
Spread spectrum – triangle	10%	Default configuration (nominal switching frequency 400 kHz)

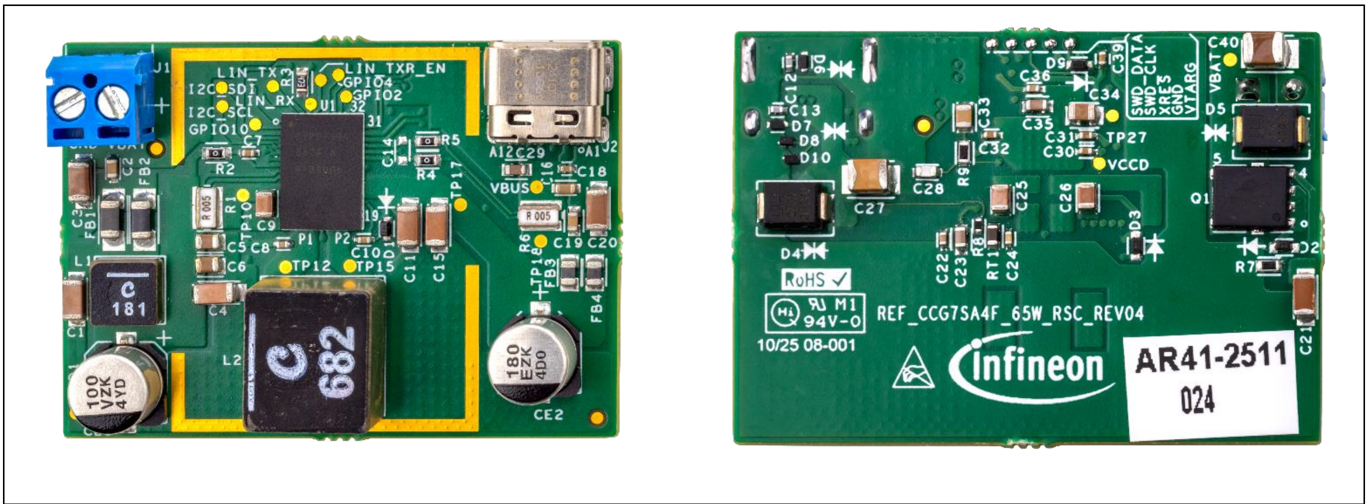


Figure 3 EZ-PD™ CCG7SA4F automotive 65 W RSC solution board top and bottom views

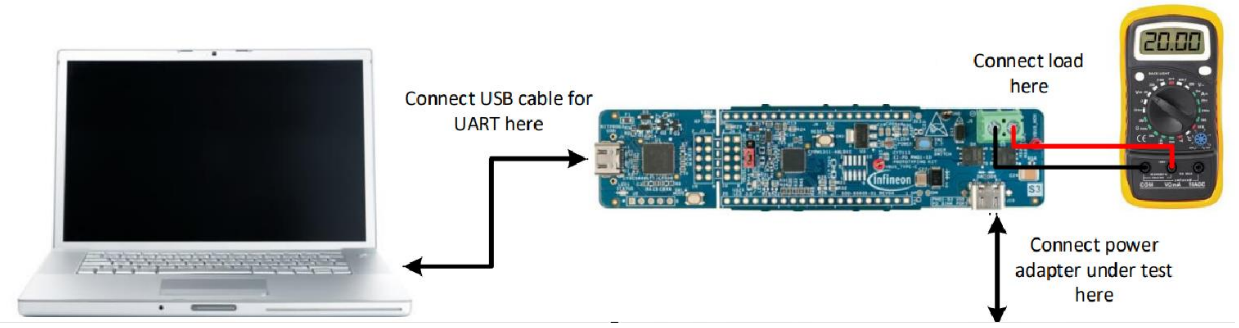
3.1 Device under test (DUT) setup

The DUT is connected to EZ-PD™ PMG1-S3 kit using a USB Type-C cable. After a successful connection is established, the EZ-PD™ PMG1-S3 UI does a PDO discovery and displays the results. The RSC solution demo kit is preconfigured with seven PDOs:

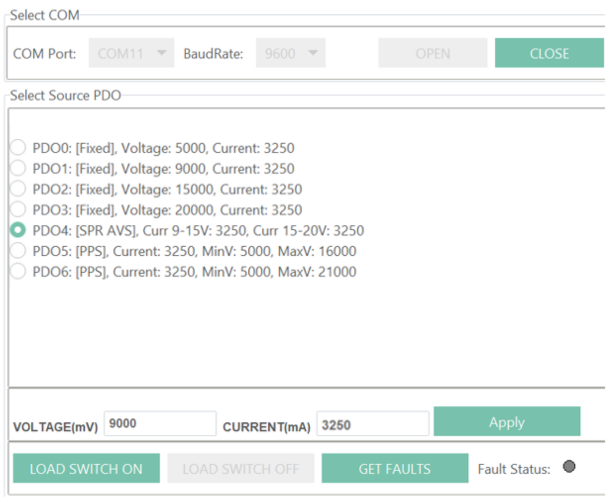
- Fixed PDOs: 5 V/3.25 A, 9 V/3.25 A, 15 V/3.25 A, 20 V/3.25 A
- Programmable power supply (PPS): 5 V–16 V, 3.25 A; 5 V–21 V, 3.25 A (PPS power limited)
- Adjustable voltage supply (AVS): 9.0 V to 15.0 V, 3.25 A; 15.0 V to 20.0 V, 3.25 A

It is possible to choose either a suitable preconfigured PDO or configure a new one using the EZ-PD™ Configuration Utility. The tests in the following sections utilize the preconfigured PDOs.

To know more about EZ-PD™ PMG1-S3 tester, visit CY7113 EZ-PD™ PMG1-S3 webpage.



DUT setup



Port 0 PDOs

Figure 4 EZ-PD™ PMG1-S3 tester and user interface

3.2 Test equipment

The test equipment used to measure efficiency, ripple, regulation, and transient response are shown in Table 7.

Table 7 Test equipment details

Test setup	Description
DC source	GWINSTEK PSB - 2400L
Oscilloscope	Tektronix MDO 3034
Digital multimeter (I_{OUT})	Keysight 34465A
Data logger (V_{BUS}, $I_{IN,}$ V_{IN})	Keysight 34970A
Electronic load	GWINSTEK PEL-3021
Input current (I_{IN}) measurement shunt	Vishay Y14730R00500B0R
Thermal camera	FLIR E75

4 Power management test results

Efficiency captured using the test setup is provided in Appendix: Efficiency measurement test setup.

Note: Unless otherwise specified, all measurements were taken at room temperature.

4.1 Peak efficiency table

Peak efficiency test results are tabulated in Table 8.

Table 8 Peak efficiency

V_{BUS} (V)	5.5 V_{IN}	9 V_{IN}	11 V_{IN}	12 V_{IN}	15 V_{IN}	18 V_{IN}
5.0 V	94.98% - 1.63 A	95.03%-2.43 A	94.42%-2.84 A	94.62% - 2.84 A	93.85% - 3.25 A	93.19% - 3.25 A
9.0 V	96.24% - 1.22 A	95.72%-2.03 A	96.8%-2.436 A	97.06% - 2.84 A	96.44% - 3.25 A	95.89% - 3.25 A
12 V	95.65% - 1.00 A	96.71%-1.62 A	95.5%-2.03 A	96.58% - 2.63 A	97.50% - 3.00 A	96.98% - 3.00 A
15 V	95.11% - 1.07 A	96.16%-1.62 A	96.84%-2.03 A	97.60% - 2.03 A	96.79% - 2.84 A	97.78% - 3.25 A
20 V	94.30% - 0.80 A	95.56%-1.62 A	96.14%-2.03 A	96.95% - 2.03 A	97.59% - 2.44 A	96.26% - 2.84 A
21 V	94.14% - 0.80 A	95.41%-1.62 A	96.07%-2.03 A	96.80% - 1.88 A	97.47% - 2.25 A	96.11% - 3.00 A

Note:

1. *Peak efficiency: 97.78% (At V_{IN}:18 V_{DC}, V_{BUS}: 15 V, I_{OUT}: 3.25 A)*
2. *For efficiency calculations V_{BUS} is measured across the output capacitors (C27) with 30 minutes warmup*
3. *Input voltage-based power throttling is enabled*

Full-load efficiency test results are tabulated in Table 9.

Table 9 Full-load efficiency

V_{BUS} (V)	5.5 V_{IN}	9 V_{IN}	11 V_{IN}	12 V_{IN}	15 V_{IN}	18 V_{IN}
5.00 V	93.90 % - 3.25 A	94.81%-3.25 A	94.36%-3.25 A	94.60 % - 3.25 A	93.85 % - 3.25 A	93.19 % - 3.25 A
9.00 V	94.34 % - 3.25 A	95.43%-3.25 A	96.71%-3.25 A	97.02 % - 3.25 A	96.44 % - 3.25 A	95.89 % - 3.25 A
12.00 V	95.32 % - 1.60 A	96.59%-2.4 A	95.32%-3 A	96.53 % - 3.00 A	97.50 % - 3.00 A	96.98 % - 3.00 A
15.00 V	93.50 % - 2.13 A	95.42%-3.20 A	96.53%-3.25 A	97.41 % - 3.25 A	96.76 % - 3.25 A	97.78 % - 3.25 A
20.00 V	92.92 % - 1.60 A	95.07%-2.40 A	95.60%-3.25 A	96.61 % - 3.25 A	97.52 % - 3.25 A	96.23 % - 3.25 A
21.00 V	92.53 % - 1.60 A	94.87%-2.4 A	95.75%-3 A	96.53 % - 3.00 A	97.42 % - 3.00 A	96.11 % - 3.00 A

4.2 Efficiency graphs

Efficiency measurements were taken at 5.5 V, 9 V, 12 V, 15 V, and 18 V DC input to the DUT; V_{BUS} PDO, PPS voltages are 5 V, 9 V, 12V, 15 V, 20 V, and 21 V. The port was loaded from 0 A to the maximum rated output current of 3.25 A. The efficiency and power loss graphs are based on the test setup of Figure 60.

Efficiency, losses at 5.5 V DC input, V_{BUS} 5 V, 9 V, 12V, 15 V, 20 V, 21 V, and I_{OUT} 0 A to 3.25 A maximum (based on the input voltage power throttling) on the port as shown in Figure 5.

Efficiency, losses at 09 V DC input, V_{BUS} 5 V, 9 V, 12 V, 15 V, 20 V, 21 V, and I_{OUT} 0 A to 3.25 A maximum (based on the input voltage power throttling) on the port as shown in Figure 6.

Efficiency, losses at 12 V DC input, V_{BUS} 5 V, 9 V, 12 V, 15 V, 20 V, 21 V, and I_{OUT} 0 A to 3.25 A on the port as shown in Figure 7.

Efficiency, losses at 15 V DC input, V_{BUS} 5 V, 9 V, 12 V, 15 V, 20 V, 21 V, and I_{OUT} 0 A to 3.25 A on the port as shown in Figure 8.

Efficiency, losses at 18 V DC input, V_{BUS} 5 V, 9 V, 12 V, 15 V, 20 V, 21 V, and I_{OUT} 0 A to 3.25 A on the port as shown in Figure 9.

4.2.1 Efficiency and power losses at 5.5 V_{DC} input

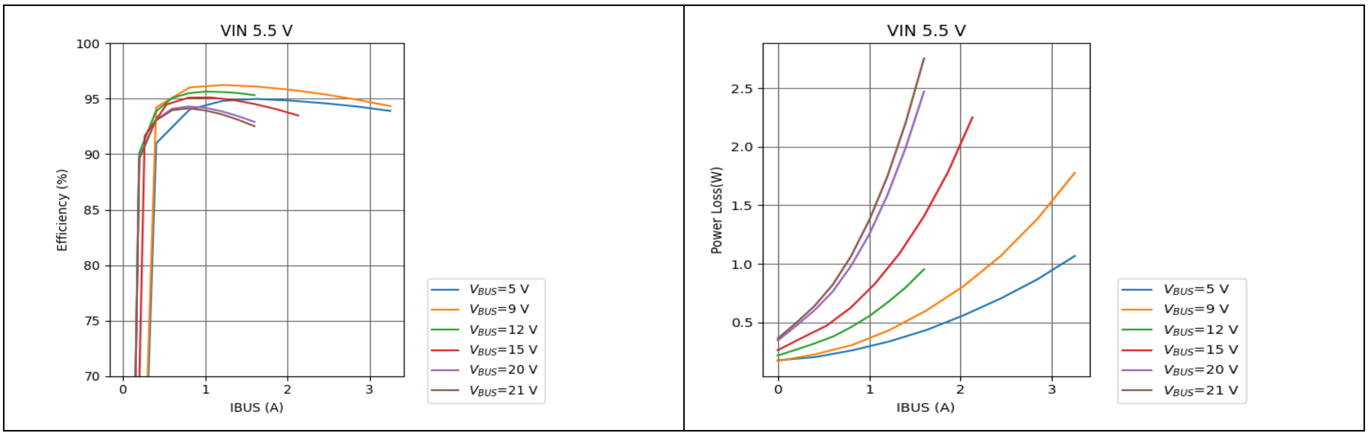


Figure 5 **Efficiency and power losses at 5.5 V_{DC} input**

4.2.2 Efficiency and power losses at 9.0 V_{DC} input

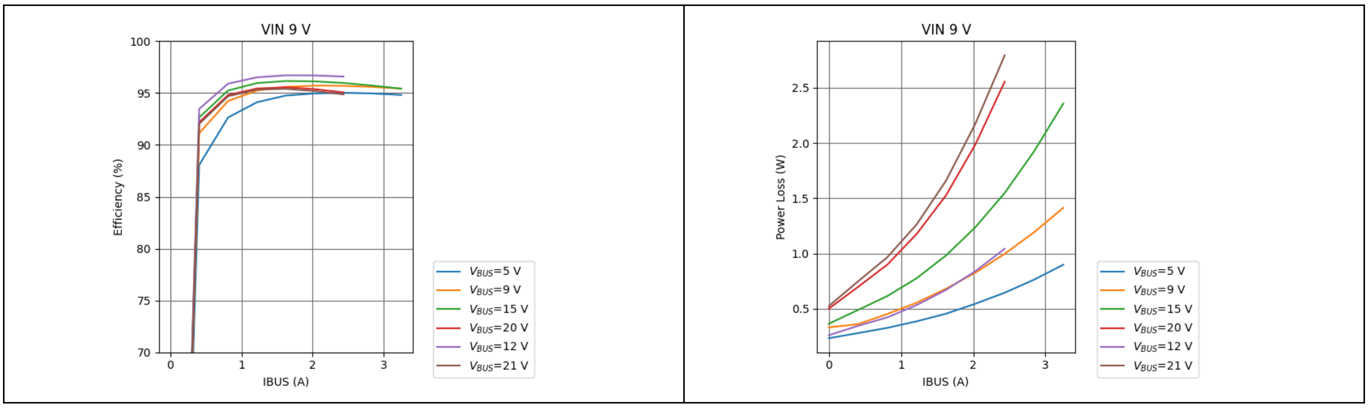


Figure 6 **Efficiency and power losses at 9.0 V_{DC} input**

4.2.3 Efficiency and power losses at 12.0 V_{DC} input

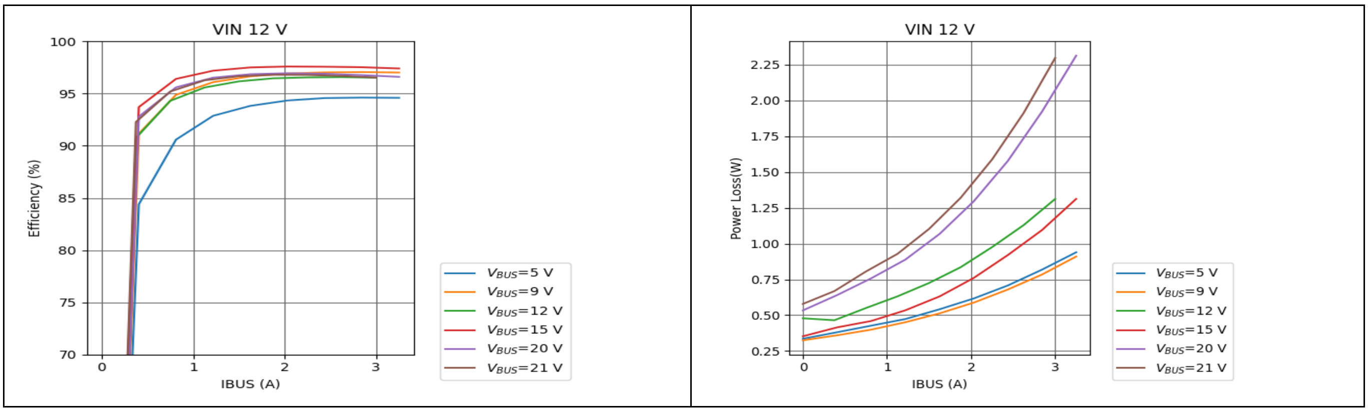


Figure 7 **Efficiency and power losses at 12.0 V_{DC} input**

4.2.4 Efficiency and power losses at 15.0 V_{DC} input

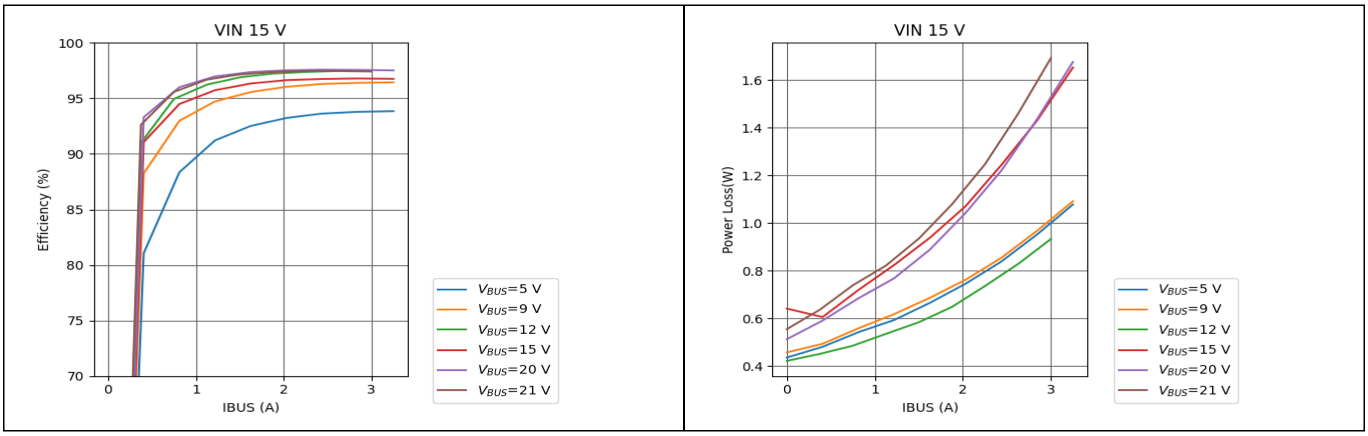


Figure 8 **Efficiency and power losses at 15.0 V_{DC} input**

4.2.5 Efficiency and power losses at 18.0 V_{DC} input

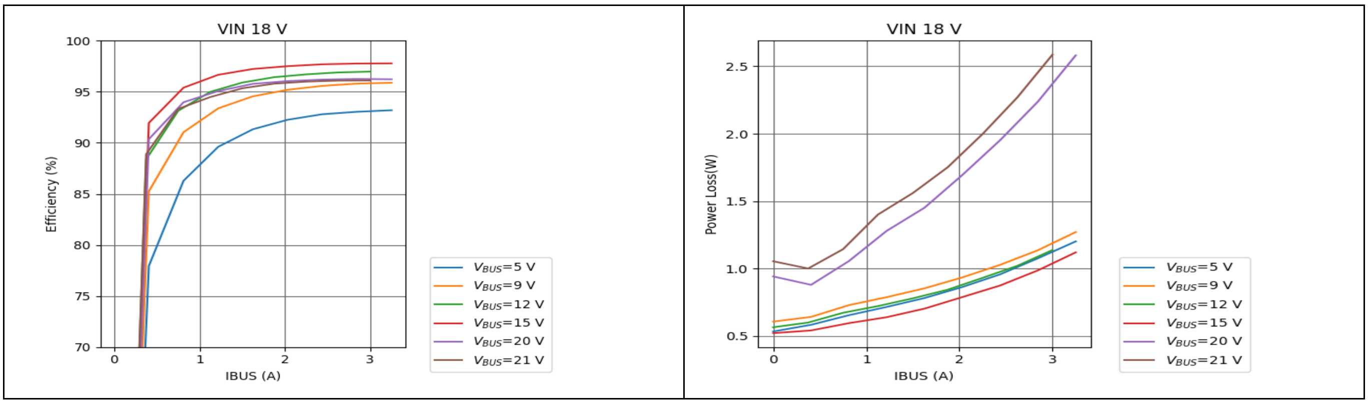


Figure 9 **Efficiency and power losses at 18.0 V_{DC} input**

4.3 Output voltage and current regulation

Output voltage regulation was measured both in the constant voltage (CV) and constant current (CC) modes.

4.3.1 Output voltage regulation (CV mode)

Output constant voltage regulation measured from 0 A and 3.25 A load currents are shown in Figure 10, Figure 11, Figure 12, Figure 13, and Figure 14.

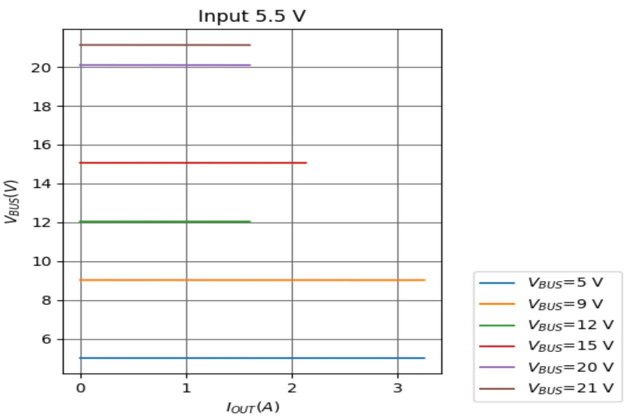


Figure 10 CV regulation at 5.5 V_{DC} input

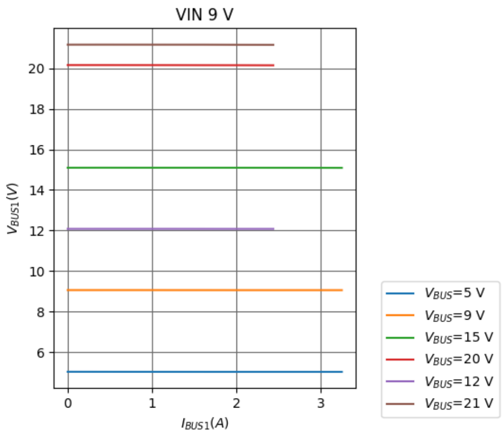


Figure 11 CV regulation at 9.0 V_{DC} input

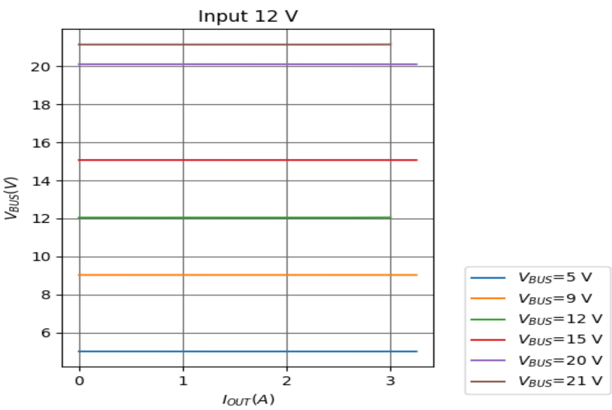


Figure 12 CV regulation at 12.0 V_{DC} input

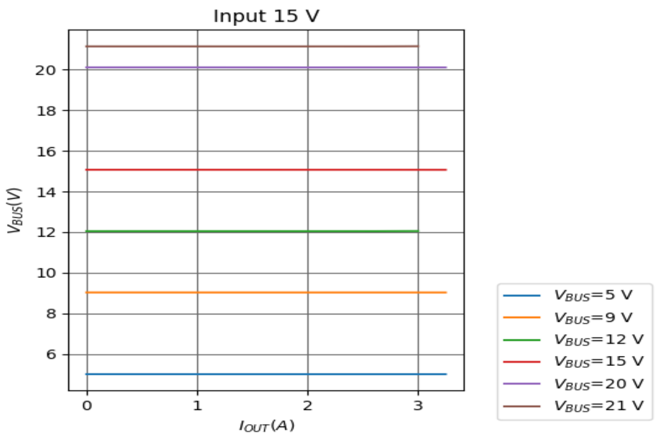


Figure 13 CV regulation at 15.0 V_{DC} input

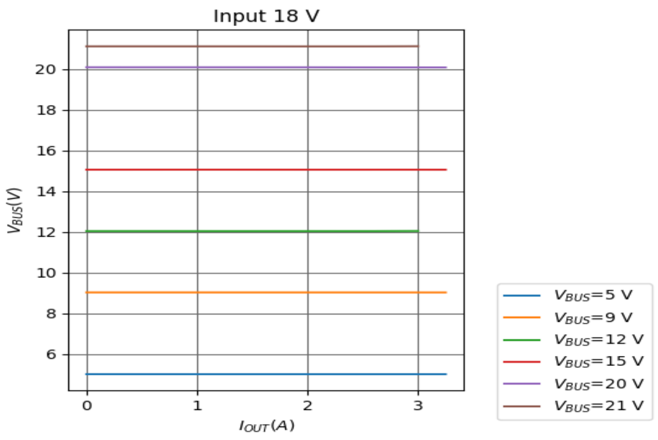


Figure 14 CV regulation at 18.0 V_{DC} input

4.3.2 Output current regulation (CC mode)

Output constant current (CC) regulation of port measured at 1 A and 3 A output currents are shown in Figure 15, Figure 16, Figure 17, and Figure 18.

4.3.3 CC regulation curve at 12 V_{DC} input and rated output current of 1 A

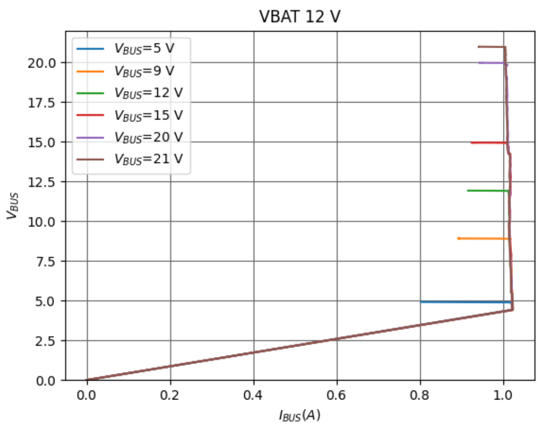


Figure 15 CC regulation curve at 12.0 V_{DC} input and 1 A output current

4.3.4 CC regulation curve at 12 V_{DC} input and rated output current of 3.00 A

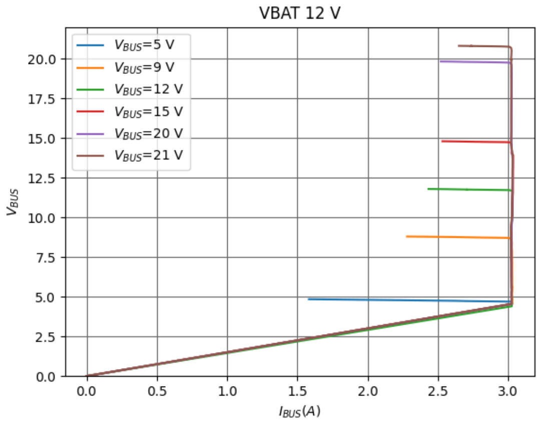


Figure 16 CC regulation curve at 12.0 V_{DC} input and 3 A output current

4.3.5 CC regulation curve at 18 V_{DC} input and rated output current of 1 A

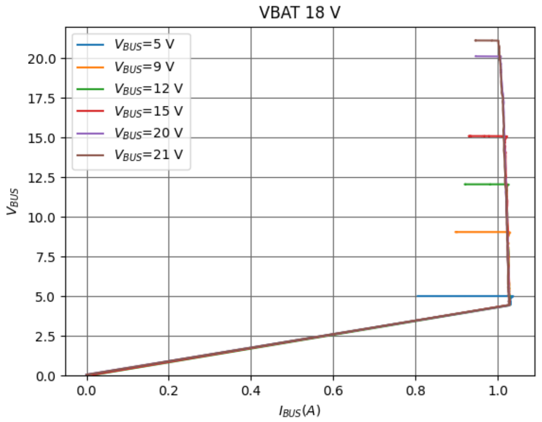


Figure 17 CC regulation curve at 18.0 V_{DC} input and 1 A output current

4.3.6 CC regulation curve at 18.0 V_{DC} input and rated output current of 3 A

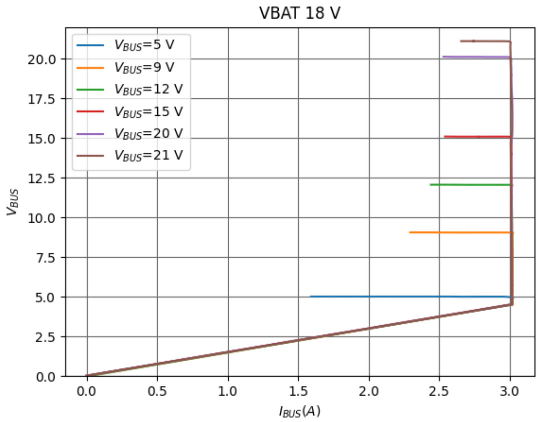


Figure 18 CC regulation curve at 18 V_{DC} input and 3 A output current

4.4 Output voltage regulation

Output voltage regulation measured at V_{IN}: 5.5 V_{DC}, 9 V_{DC}, 11 V_{DC}, 12 V_{DC}, 15 V_{DC}, 18 V_{DC}, V_{BUS}: 5 V, 9 V, 12 V, 15 V, 20 V, 21 V, I_{OUT}: 0 A and 3 A are shown in Table 10 and Table 11.

Table 10 Regulation: 5.5 V_{DC}, 9.0 V_{DC}, and 11.0 V_{DC} input

I_{OUT} (A)	V_{BUS} (V_{DC})	@V_{IN} 5.5 V_{DC} % regulation	I_{OUT} (A)	V_{BUS} (V_{DC})	@V_{IN} 9 V_{DC} % regulation	I_{OUT} (A)	V_{BUS} (V_{DC})	@V_{IN} 11 V_{DC} % regulation
0.00	5.0201	0.053	0.00	5.0422	0.089	0.00	5.0408	0.090
3.25	5.0175	–	3.25	5.0377	–	3.25	5.0363	–
0.00	9.0366	0.029	0.00	9.0663	0.040	0.00	9.0640	0.010
3.25	9.0339	–	3.25	9.0631	–	3.25	9.0630	–
0.00	12.0491	0.009	0.00	12.0846	0.010	0.00	12.0867	0.030
1.60	12.0479	–	2.40	12.0836	–	3.00	12.0825	-
0.00	15.0674	0.018	0.00	15.0961	0.040	0.00	15.1022	0.040
2.13	15.0647	–	3.25	15.0908	–	3.25	15.0963	–
0.00	20.1007	0.026	0.00	20.1544	0.050	0.00	20.1468	0.040
1.60	20.0955	–	2.40	20.1436	–	3.25	20.1378	–
0.00	21.1326	0.019	0.00	21.1616	0.040	0.00	21.1760	0.060
1.60	21.1286	–	2.40	21.1533	–	3.00	21.1632	–

Table 11 Regulation: 12 V_{DC}, 15 V_{DC} and 18 V_{DC} input

I_{OUT} (A)	V_{BUS} (V_{DC})	@V_{IN} 12 V_{DC} % regulation	I_{OUT} (A)	V_{BUS} (V_{DC})	@V_{IN} 15 V_{DC} % regulation	I_{OUT} (A)	V_{BUS} (V_{DC})	@V_{IN} 18 V_{DC} % regulation
0.00	5.0198	0.041	0.00	5.0203	0.042	0.00	5.0202	0.042
3.25	5.0177	–	3.25	5.0182	–	3.25	5.0181	–
0.00	9.0363	0.018	0.00	9.0364	0.016	0.00	9.0361	0.015
3.25	9.0347	–	3.25	9.0350	–	3.25	9.0347	–
0.00	12.0491	0.040	0.00	12.0493	0.045	0.00	12.0497	0.037
3.00	12.0539	–	3.00	12.0548	–	3.00	12.0543	–
0.00	15.0663	0.010	0.00	15.0666	0.024	0.00	15.0661	0.011
3.25	15.0648	–	3.25	15.0630	–	3.25	15.0644	–
0.00	20.0986	0.016	0.00	20.0988	0.015	0.00	20.0981	0.046
3.25	20.0953	–	3.25	20.0959	–	3.25	20.0888	–
0.00	21.1325	0.021	0.00	21.1305	0.029	0.00	21.1250	0.022
3.00	21.1369	–	3.00	21.1367	–	3.00	21.1297	–

4.5 Output voltage ripple measurement

Output voltage peak-to-peak ripple was measured across the output capacitor C27 using a short ground loop connected to the probe.

4.5.1 Output voltage ripple measurement test setup

Ripple has been measured using the oscilloscope probe as shown in Figure 19.

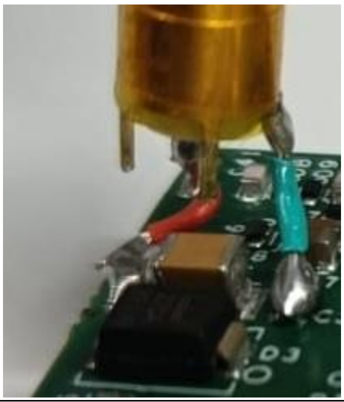


Figure 19 Output voltage ripple measurement test setup

4.5.2 Output voltage ripple peak-to-peak (mV)

Output voltage peak-to-peak ripple tabulated in Table 12.

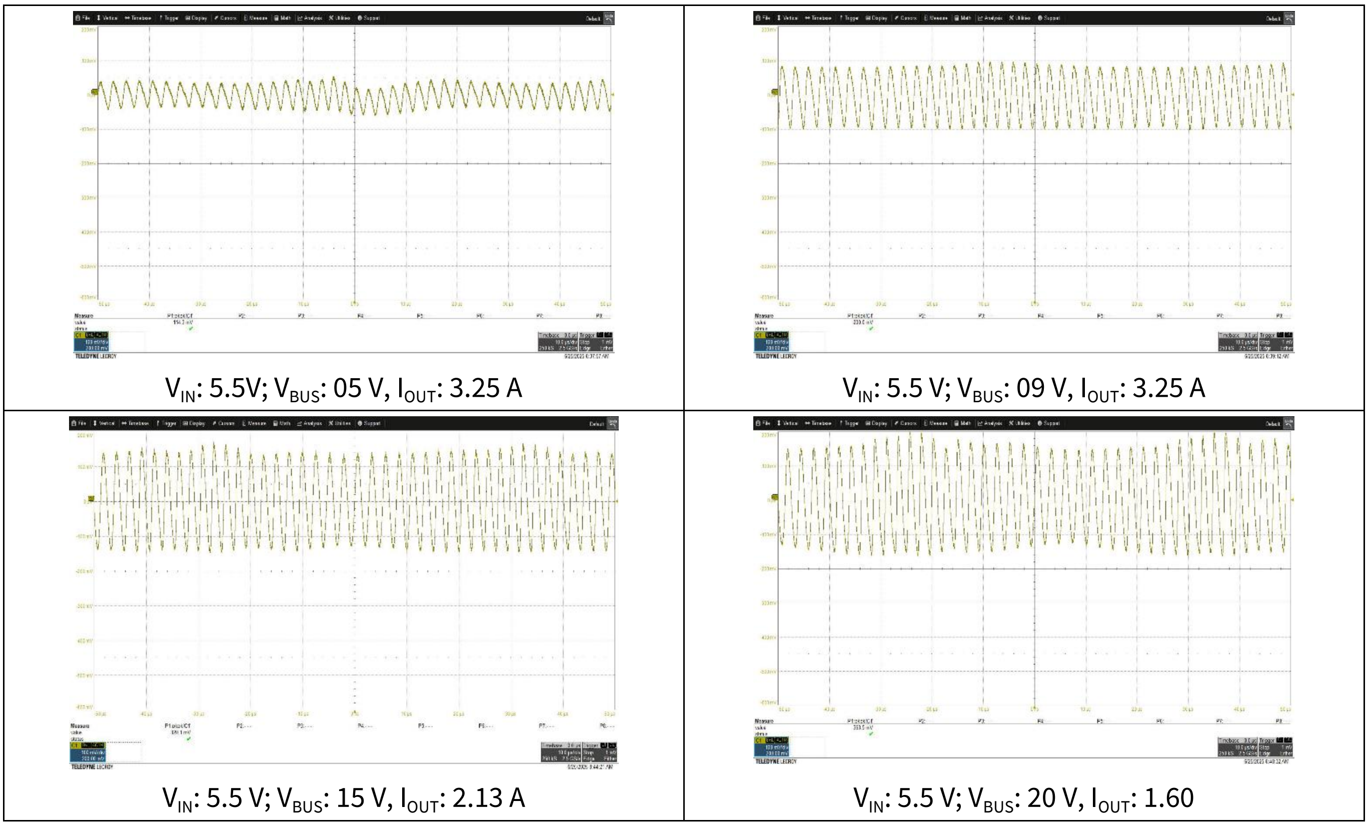
Table 12 Peak-to-peak (mV) ripple

V_{BUS} ripple peak-to-peak (mV)

V_{BUS} - I_{OUT}	@V_{IN} 5.5 V	V_{BUS} - I_{OUT}	@V_{IN} 9 V	V_{BUS} - I_{OUT}	@V_{IN} 11 V	V_{BUS} - I_{OUT}	@V_{IN} 12 V	@V_{IN} 15 V	@V_{IN} 18 V
05 V - 0.00 A	19.7265	05 V - 0.00 A	21.6796	05 V - 0.00 A	38.0859	05 V - 0.00 A	57.0312	33.7890	11.5234
05 V - 3.25 A	114.257	05 V - 3.25 A	43.3593	05 V - 3.25 A	57.0312	05 V - 3.25 A	57.6171	50.1953	49.2187
09 V - 0.00 A	114.257	09 V - 0.00 A	56.2500	09 V - 0.00 A	38.0859	09 V - 0.00 A	57.2265	53.9062	35.5468
09 V - 3.25 A	200.000	09 V - 3.25 A	122.6567	09 V - 3.25 A	52.1484	09 V - 3.25 A	58.9843	59.5703	63.0859
12 V - 0.00 A	18.3593	12 V - 0.00 A	37.4534	12 V - 0.00 A	51.7578	12 V - 0.00 A	39.8437	48.8281	41.4062
12 V – 1.60 A	199.023	12 V – 2.40 A	94.9218	12 V – 3.00 A	143.359	12 V – 3.00 A	133.9843	68.9453	65.8203
15 V - 0.00 A	24.414	15 V - 0.00 A	31.6406	15 V - 0.00 A	29.1015	15 V - 0.00 A	131.0546	51.1718	59.1796
15 V – 2.13 A	320.117	15 V – 3.25 A	179.4921	15 V – 3.25 A	170.312	15 V – 3.25 A	136.1328	160.5468	77.1484
20 V - 0.00 A	27.1484	20 V - 0.00 A	34.1796	20 V - 0.00 A	42.9687	20 V - 0.00 A	41.9921	43.5546	44.1406
20 V - 1.60 A	363.476	20 V – 2.40 A	230.0781	20 V – 3.250 A	234.570	20 V – 3.25 A	262.1093	200.3906	252.148
21 V - 0.00 A	28.3203	21 V - 0.00 A	37.1093	21 V - 0.00 A	41.0156	21 V - 0.00 A	41.6015	46.2890	42.1875
21 V – 1.60 A	379.882	21 V – 2.40 A	241.2109	21 V – 3.00 A	229.687	21 V – 3.00 A	258.3984	208.5937	251.562

4.5.3 Output voltage ripple peak-to-peak measurement graphs

Output voltage peak-to-peak ripple waveforms at full load (based on the input voltage power throttling) are shown in Figure 20, Figure 21, Figure 22, Figure 23, and Figure 24.



V_{IN}: 5.5V; V_{BUS}: 05 V, I_{OUT}: 3.25 A

V_{IN}: 5.5 V; V_{BUS}: 09 V, I_{OUT}: 3.25 A

V_{IN}: 5.5 V; V_{BUS}: 15 V, I_{OUT}: 2.13 A

V_{IN}: 5.5 V; V_{BUS}: 20 V, I_{OUT}: 1.60

Figure 20 Ripple measurement – Input voltage: 5.5 V_{DC} (CH1: V_{BUS})

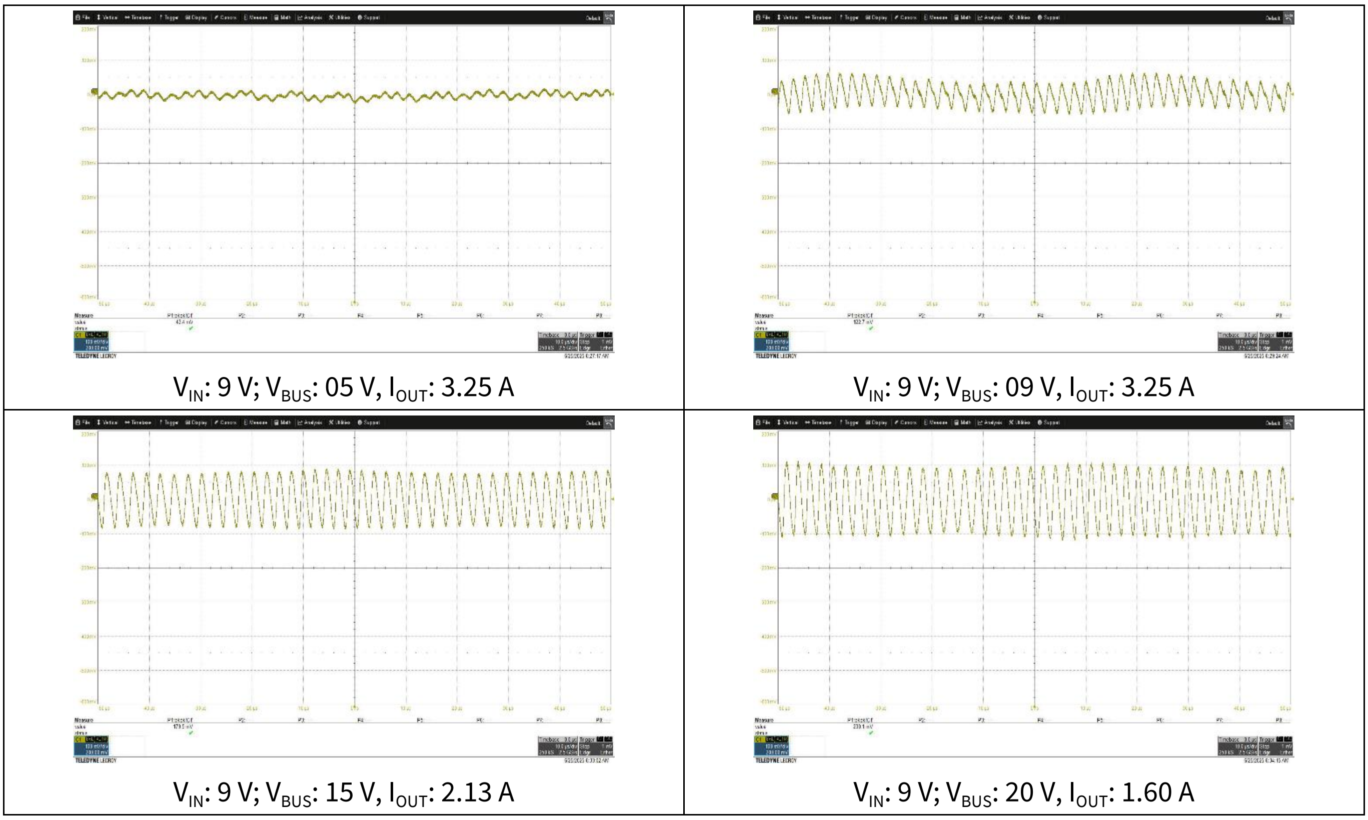


Figure 21 Ripple measurement – Input voltage: 9 V_{DC} (CH1: V_{BUS})

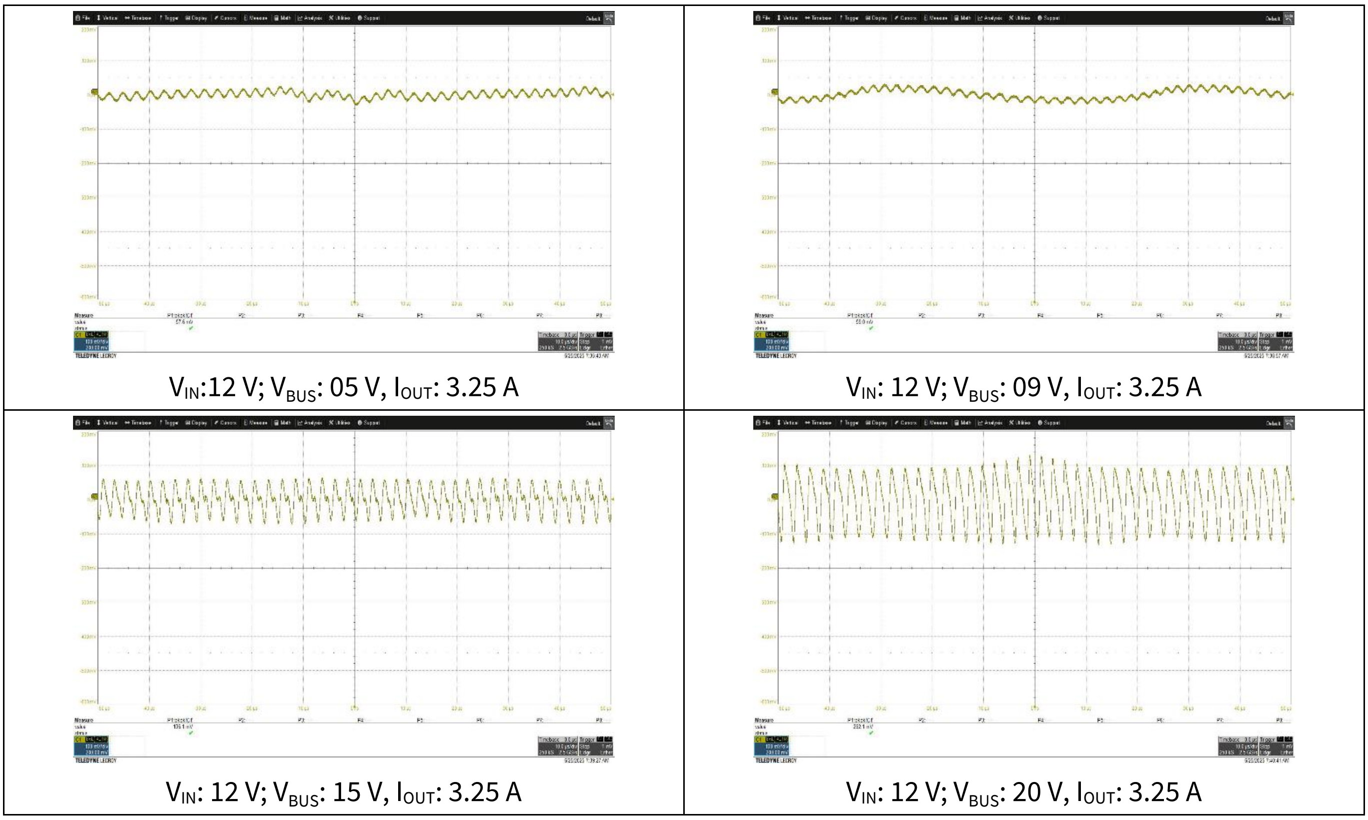
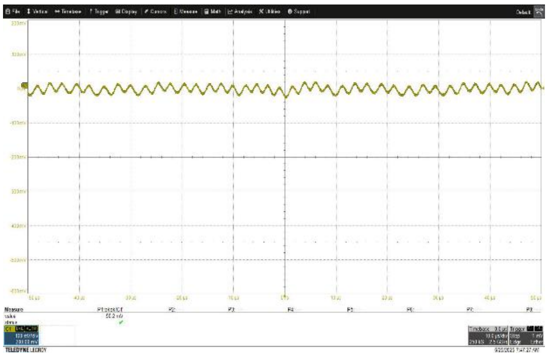
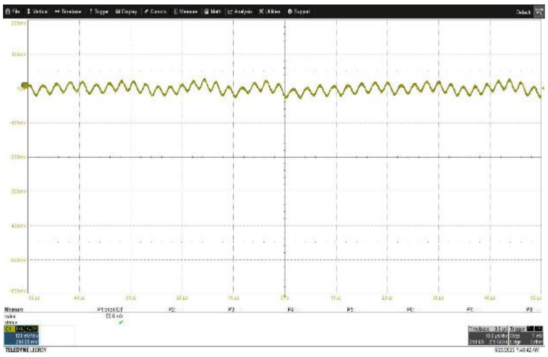


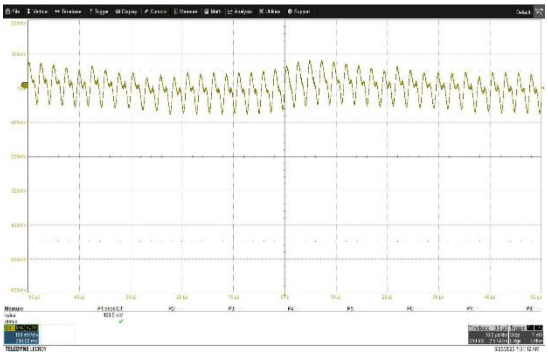
Figure 22 Ripple measurement – Input voltage: 12 V_{DC} (CH1: V_{BUS})



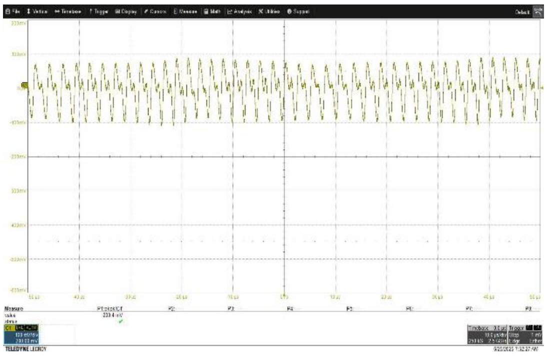
V_{IN}:15 V; V_{BUS}: 05 V, I_{OUT}: 3.25 A



V_{IN}: 15 V; V_{BUS}: 09 V, I_{OUT}: 3.25 A

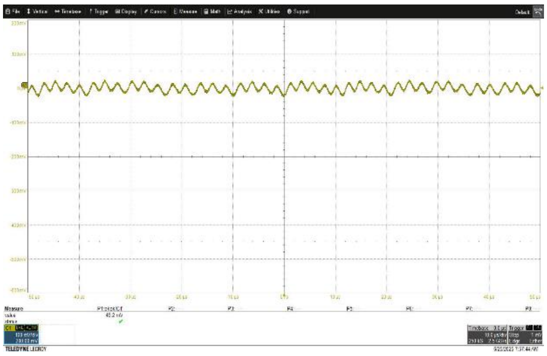


V_{IN}: 15 V; V_{BUS}: 15 V, I_{OUT}: 3.25 A

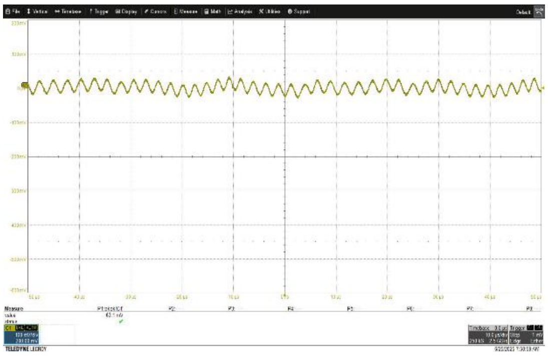


V_{IN}: 15 V; V_{BUS}: 20 V, I_{OUT}: 3.25 A

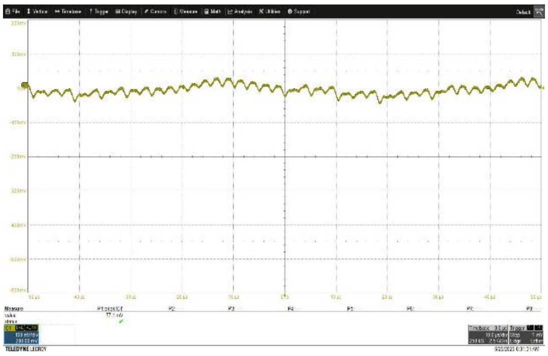
Figure 23 **Ripple measurement – Input voltage: 15 V_{DC} (CH1: V_{BUS})**



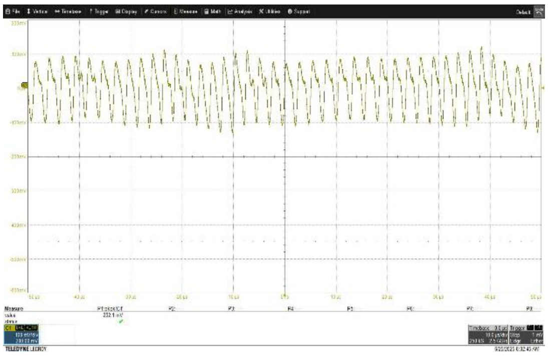
V_{IN}:18 V; V_{BUS}: 05 V, I_{OUT}: 3.25 A



V_{IN}: 18 V; V_{BUS}: 09 V, I_{OUT}: 3.25 A



V_{IN}: 18 V; V_{BUS}: 15 V, I_{OUT}: 3.25 A



V_{IN}: 18 V; V_{BUS}: 20 V, I_{OUT}: 3.25 A

Figure 24 **Ripple measurement – Input voltage: 18 V_{DC} (CH1: V_{BUS})**

4.6 Output voltage dynamic response waveforms

V_{IN}:12 V, output voltage response when the output current is from 0 A – 1 A – 0 A is shown in Figure 25.

V_{IN}:12 V, output voltage response when the output current is from 1.5 A – 2.5 A – 1.5 A is shown in Figure 26.

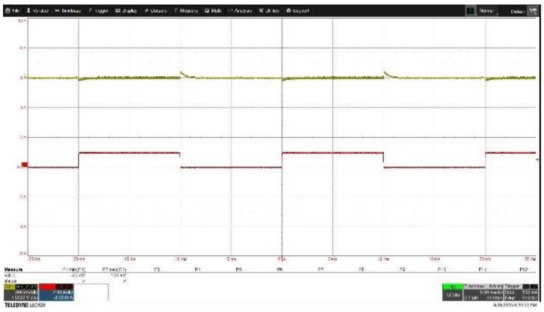
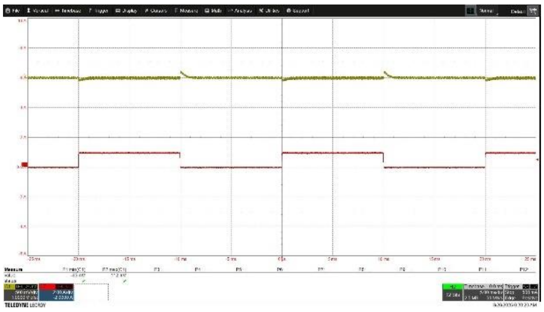
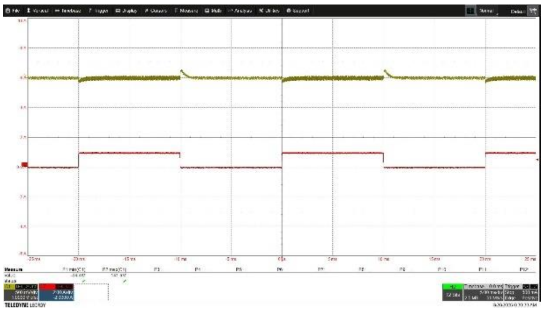
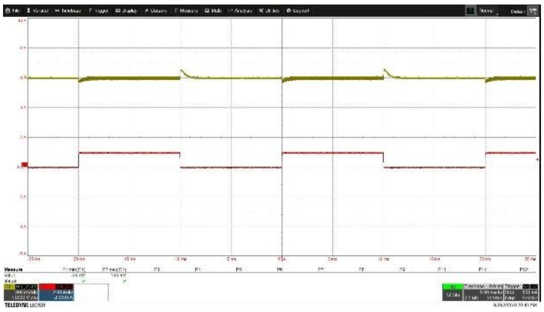
 V_{BUS}: 5.0 V; (CH1: V_{BUS}; CH2: I_{OUT})	 V_{BUS}: 9.0 V; (CH1: V_{BUS} ; CH2: I_{OUT})
 V_{BUS}: 12.0 V; (CH1: V_{BUS}; CH2: I_{OUT})	 V_{BUS}: 15.0 V; (CH1: V_{BUS} ; CH2: I_{OUT})
 V_{BUS}: 20.0 V; (CH1: V_{BUS}; CH2: I_{OUT})	 V_{BUS}: 21.0 V; (CH1: V_{BUS} ; CH2: I_{OUT})

Figure 25 Output dynamic response waveforms - Input 12 V_{DC}; Load current transition 0 A to 1 A to 0 A

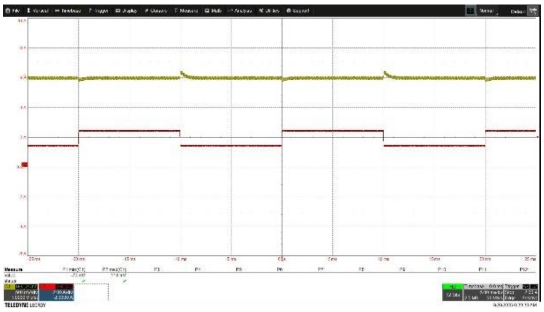
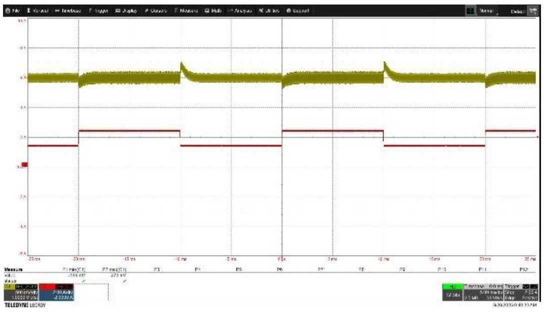
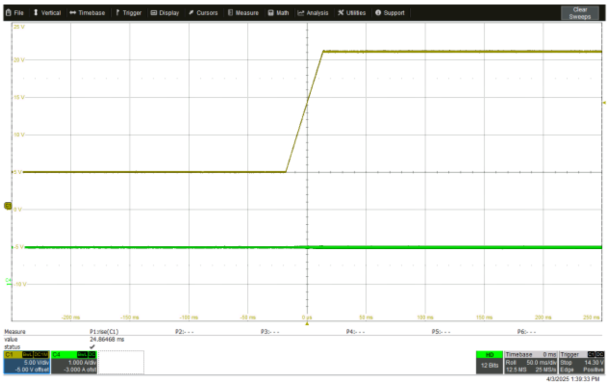
 V_{BUS}: 5.0 V; (CH1: V_{BUS}; CH2: I_{OUT})	 V_{BUS}: 9.0 V; (CH1: V_{BUS} ; CH2: I_{OUT})
 V_{BUS}: 12.0 V; (CH1: V_{BUS}; CH2: I_{OUT})	 V_{BUS}: 15.0 V; (CH1: V_{BUS} ; CH2: I_{OUT})
 V_{BUS}: 20.0 V; (CH1: V_{BUS}; CH2: I_{OUT})	 V_{BUS}: 21.0 V; (CH1: V_{BUS} ; CH2: I_{OUT})

Figure 26 Output dynamic response waveforms - Input 12 V_{DC}; Load current transition 1.5 A to 2.5 A to 1.5 A

4.7 Output voltage transition

Output voltage transition at 12 V_{DC} input and load (1 A) is measured, as shown in Figure 27 and Figure 28.



I_{OUT}: 1 A (CH1: V_{BUS}; CH4: I_{OUT})

Figure 27 Input 12 V_{DC}; V_{BUS} transition from 5.0 V to 21.0 V

I_{OUT}: 1 A (CH1: V_{BUS}; CH4: I_{OUT})

Figure 28 Input 12 V_{DC}; V_{BUS} transition from 21.0 V to 5.0 V

I_{OUT}: 1 A (CH1: V_{BUS}; CH4: I_{OUT})

Figure 29 Input 12 V_{DC}; V_{BUS} transition from 5.0 V to 12.0 V

I_{OUT}: 1 A (CH1: V_{BUS}; CH4: I_{OUT})

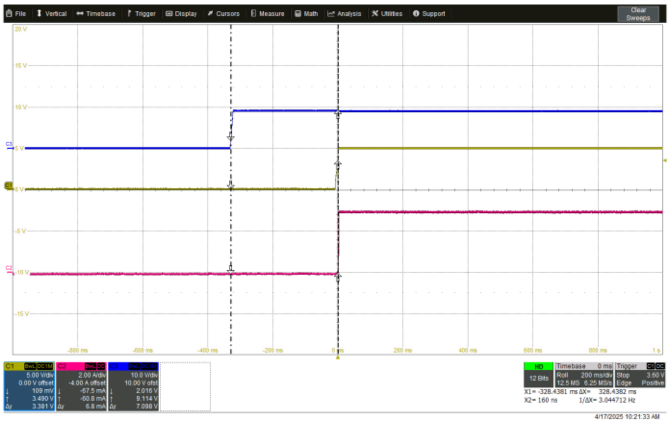
Figure 30 **Input 12 V_{DC}; V_{BUS} transition from 12.0 V to 5.0 V**

4.8 Start-up turn-on delay

Turn-on delay with respect to DUT input voltage and the output voltage is measured at full load (3 A) and is shown in Figure 31, Figure 32, Figure 33, Figure 34, and Figure 35.

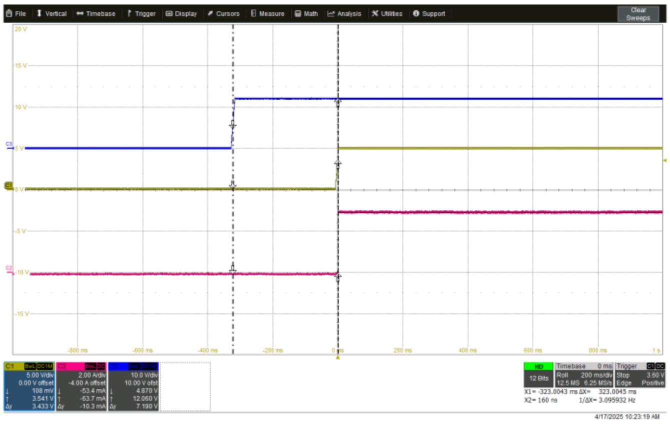
CH1: V_{BUS}; CH2: I_{OUT}; CH3: V_{IN}

Figure 31 **Input 5.5 V_{DC}; V_{BUS}: 5 V; I_{OUT}: 3 A**



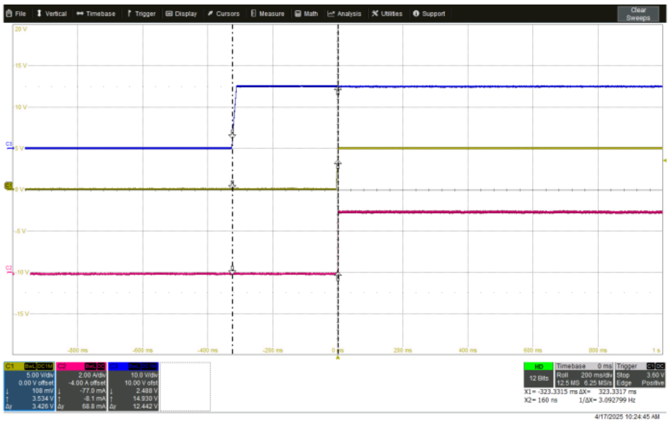
CH1: V_{BUS}; CH2: I_{OUT}; CH3: V_{IN}

Figure 32 **Input 9 V_{DC}; V_{BUS}: 5 V; I_{OUT}: 3 A**



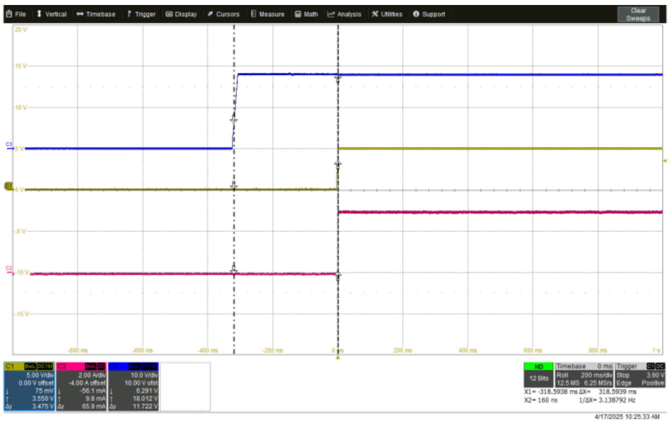
CH1: V_{BUS}; CH2: I_{OUT}; CH3: V_{IN}

Figure 33 **Input 12 V_{DC}; V_{BUS}: 5 V; I_{OUT}: 3 A**



CH1: V_{BUS}; CH2: I_{OUT}; CH3: V_{IN}

Figure 34 **Input 15 V_{DC}; V_{BUS}: 5 V; I_{OUT}: 3 A**



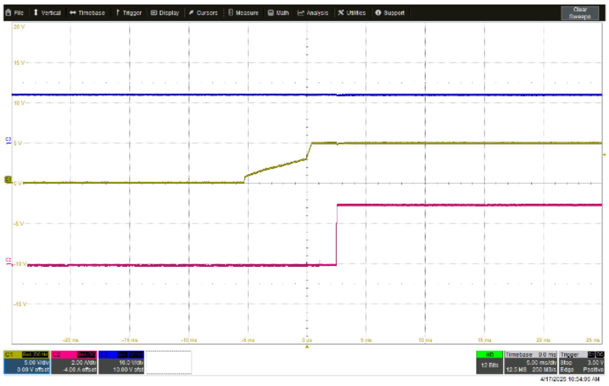
CH1: V_{BUS}; CH2: I_{OUT}; CH3: V_{IN}

Figure 35 **Input 18 V_{DC}; V_{BUS}: 5 V; I_{OUT}: 3 A**

4.9 Startup output voltage waveform

Startup output voltage during a cold start is measured at no load and full load is shown in Figure 36.

I_{OUT}: 0.0 A (CH1: V_{BUS}; CH2: I_{OUT}; CH3: V_{IN})

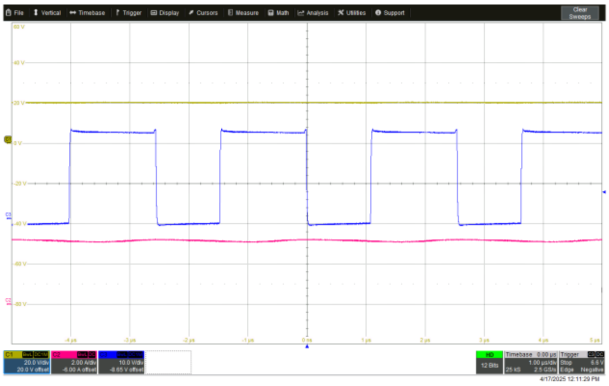


I_{OUT}: 3.0A (CH1: V_{BUS}; CH2: I_{OUT}; CH3: V_{IN})

Figure 36 **Input 12.0 V_{DC}; V_{BUS}: 5 V**

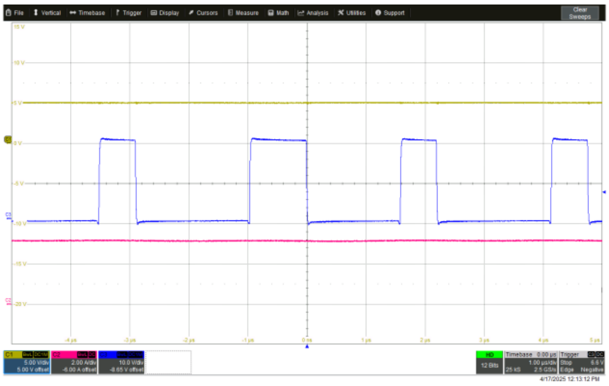
4.10 Switch voltage stress

Power MOSFETs switch node voltage stress measured in boost mode (Figure 37) and buck mode (Figure 38) at full load.



CH1: V_{BUS}; CH2: I_{OUT}; CH3: SW2

Figure 37 **Switch node voltage - Input 12.0 V_{DC}; V_{BUS}: 20 V; I_{OUT}: 3.25 A**



CH1: V_{BUS}; CH2: I_{OUT}; CH3: SW1

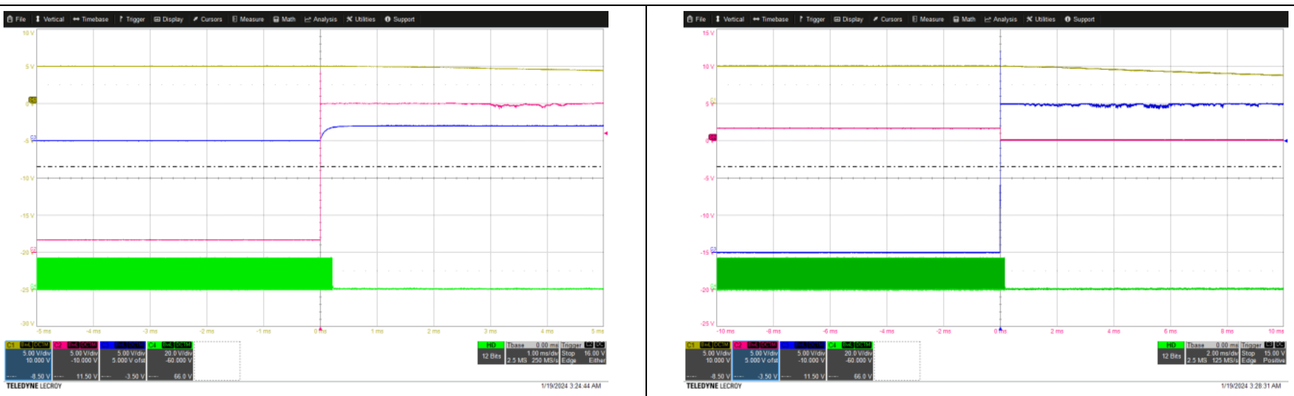
Figure 38 **Switch node voltage - Input 18.0 V_{DC}; V_{BUS}: 5.0 V; I_{OUT}: 3 A**

4.11 Faults test waveforms

The RSC solution board was subjected to supported fault protections and are shown in Figure 39.

4.11.1 V_{Bus} to CCx line faults test waveforms

V_{BUS} to CC1 active line fault is shown in Figure 39. V_{IN} = 12 V_{DC}; V_{BUS}: 20 V.



V_{BUS} to CC1 fault
CH1: V_{BUS}; CH2: CC1; CH3: CC2; CH4: HG1

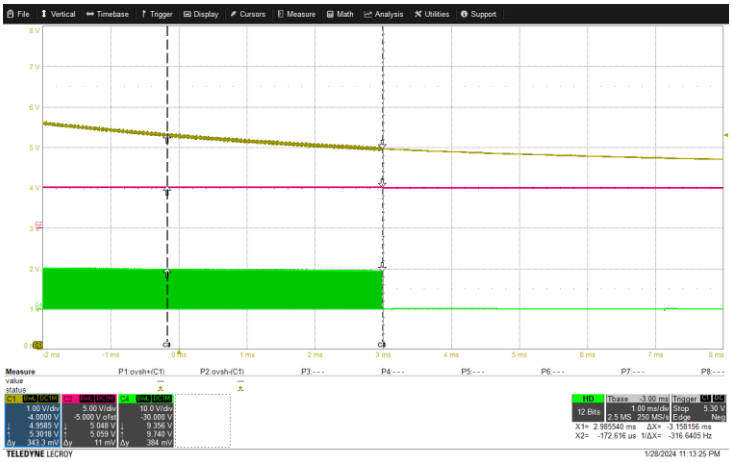
V_{BUS} to CC2 fault
CH1: V_{BUS}; CH2: CC1; CH3: CC2; CH4: HG1

Figure 39 **V_{BUS} to CC1 and V_{BUS} to CC2 active line fault**

4.11.2 Input undervoltage protection (UVP)

DUT input undervoltage waveforms are shown in Figure 40.

Test conditions: V_{BUS}: 5.0 V, I_{OUT}: 0 A.



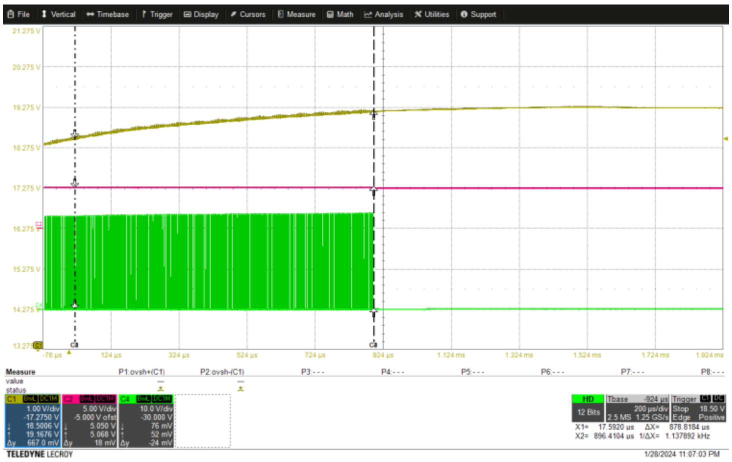
CH1: V_{IN}; CH2: V_{BUS}; CH3: HG1

Figure 40 **Input undervoltage protection**

4.11.3 Input overvoltage protection (OVP)

DUT input overvoltage protection waveforms are shown in Figure 41.

Test conditions: V_{BUS}: 5.0 V, I_{OUT}: 0 A.



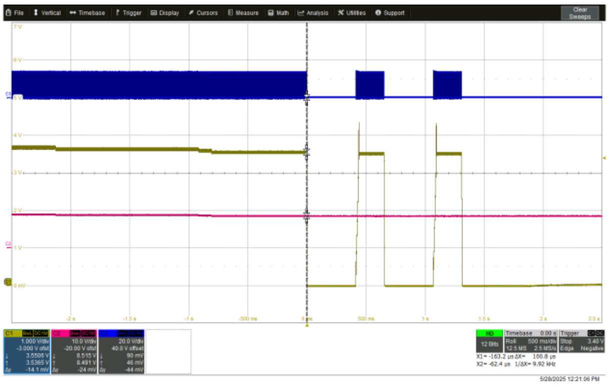
CH1: V_{IN}; CH2: V_{BUS}; CH3: HG1

Figure 41 Input overvoltage protection

4.11.4 Output undervoltage protection (UVP)

DUT output undervoltage protection waveforms are shown in Figure 42.

Test conditions: V_{IN}: 12.0 V_{DC}; V_{BUS}: 5.0 V, I_{OUT}: 0 A.



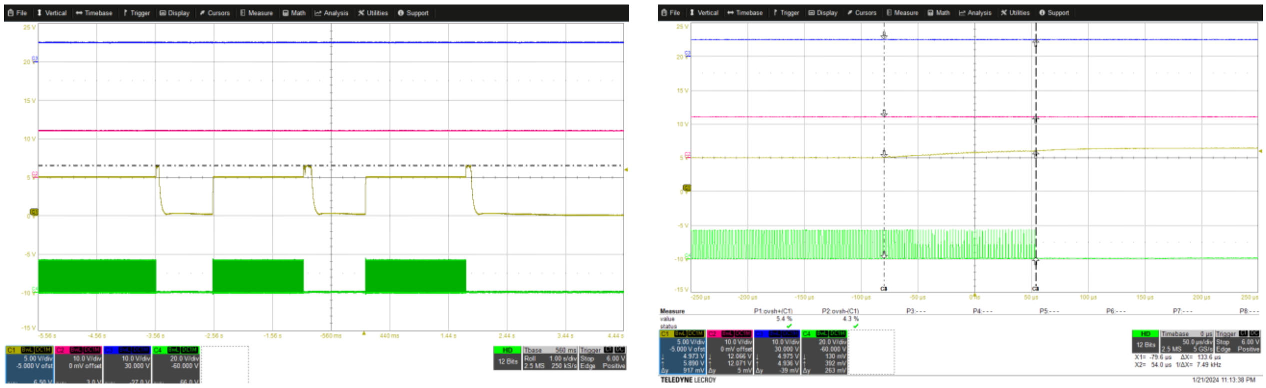
CH1: V_{BUS}; CH2: V_{IN}; CH3: HG1;

Figure 42 Output undervoltage protection

4.11.5 Output overvoltage protection (OVP)

DUT output overvoltage protection waveforms are shown in Figure 43.

Test conditions: V_{IN}: 12.0 V_{DC}; V_{BUS}: 5.0 V, I_{OUT}: 0 A.



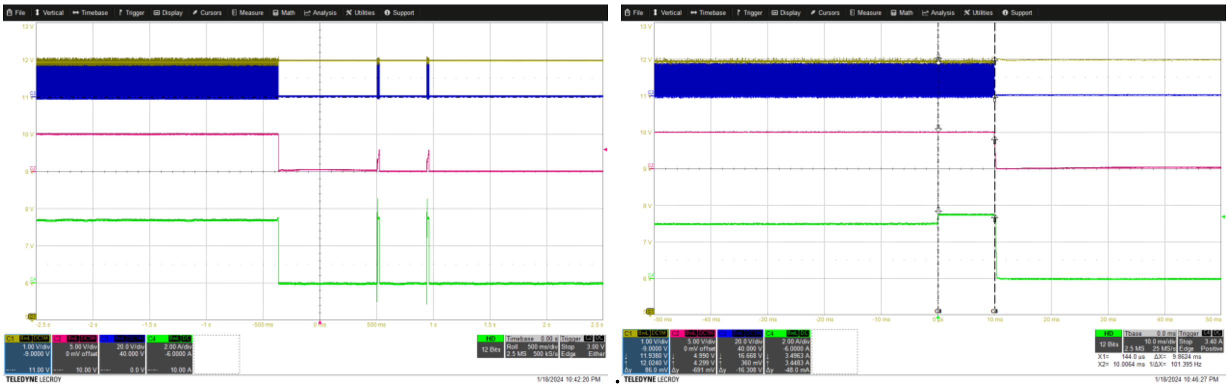
CH1: V_{BUS}; CH2: V_{IN}; CH3: VDDD; CH4: HG1

Figure 43 Output overvoltage protection

4.11.6 Output overcurrent protection (OCP)

DUT output overcurrent protection waveforms are shown in Figure 44.

Test conditions: V_{IN}: 12.0 V_{DC}; V_{BUS}: 5.0 V.



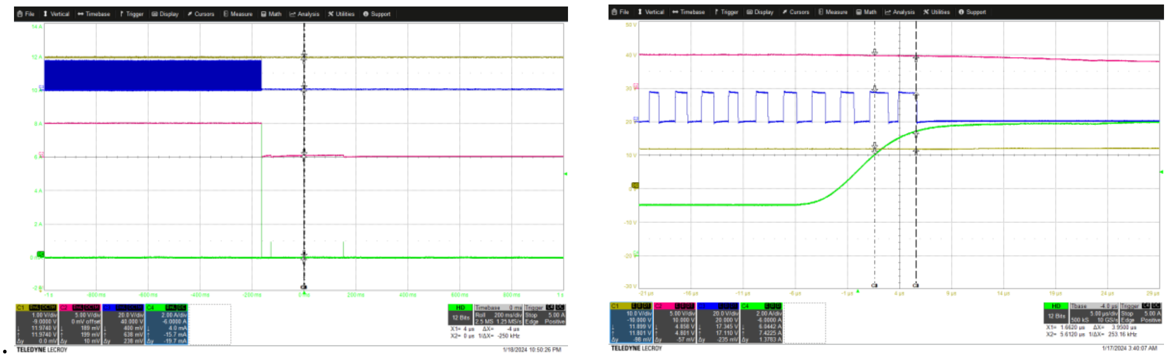
CH1: V_{IN}; CH2: V_{BUS}; CH3: HG1; CH4: I_{OUT}

Figure 44 Output overcurrent protection

4.11.7 Output short-circuit protection (SCP)

DUT output short-circuit protection waveforms are shown in Figure 45.

Test conditions: V_{IN}: 12.0 V; V_{BUS}: 5.0 V.



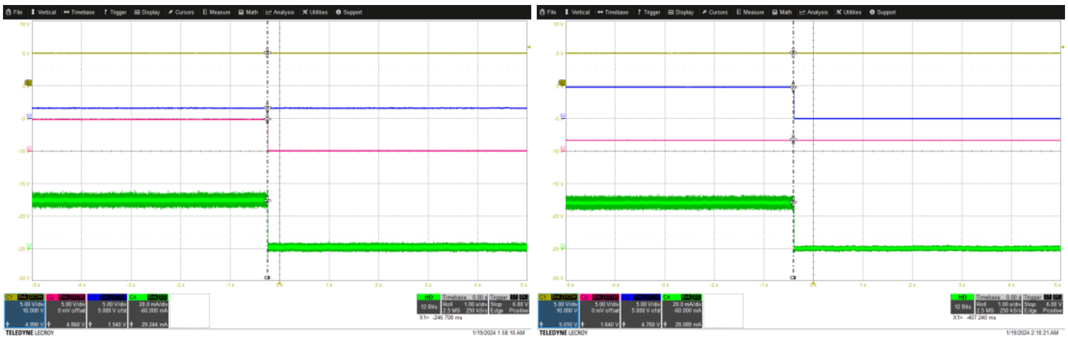
CH1: V_{IN}; CH2: V_{BUS}; CH3: HG1; CH4: I_{OUT}

Figure 45 Output short-circuit protection

4.11.8 V_{CONN} overcurrent protection (OCP)

DUT V_{CONN} overcurrent protection waveforms are shown in Figure 46.

Test conditions: V_{IN}: 12.0 V; V_{BUS}: 5.0 V.



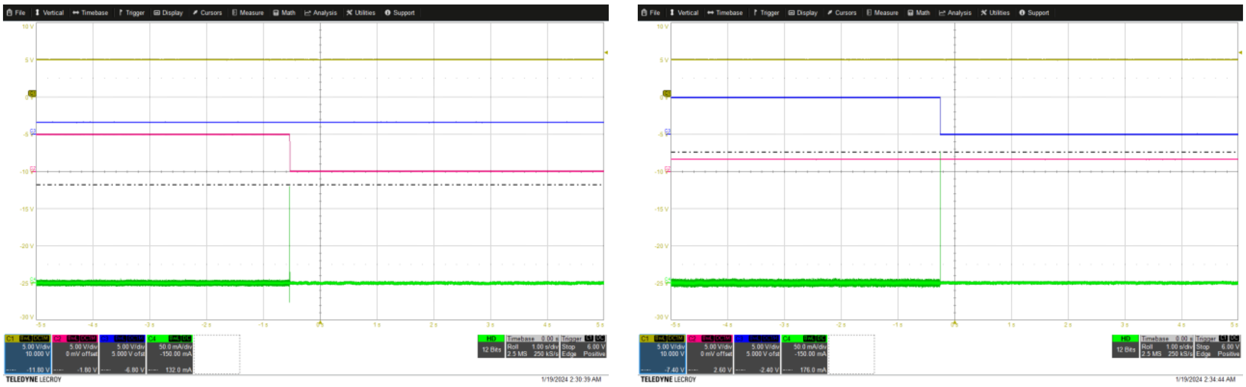
CH1: V_{BUS}; CH2: CC1; CH3: CC2; CH4: V_{CONN} current

Figure 46 V_{CONN} overcurrent protection

4.11.9 V_{CONN} short-circuit protection (SCP)

DUT V_{CONN} short-circuit protection waveforms are shown in Figure 47.

Test conditions: V_{IN}: 12.0 V; V_{BUS}: 5.0 V.



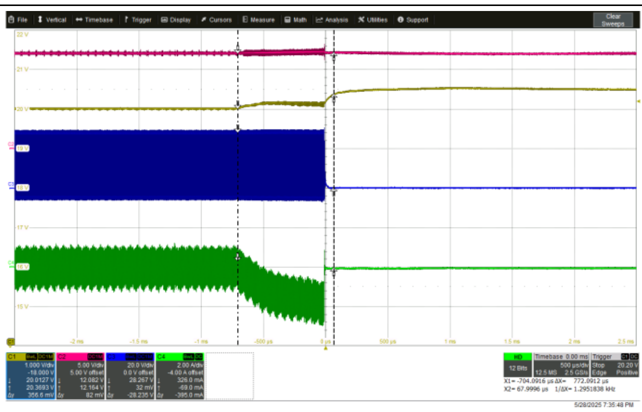
CH1: V_{BUS}; CH2: CC1; CH3: CC2; CH4: V_{CONN} current

Figure 47 **V_{CONN} short-circuit protection**

4.11.10 Reverse-current protection (RCP)

Reverse-current protection waveforms are shown in Figure 48.

Test conditions: V_{IN}: 12.0 V; V_{BUS}: 20.0 V.



CH1: V_{BUS}; CH2: V_{IN}; CH3: HG2; CH4: I_L

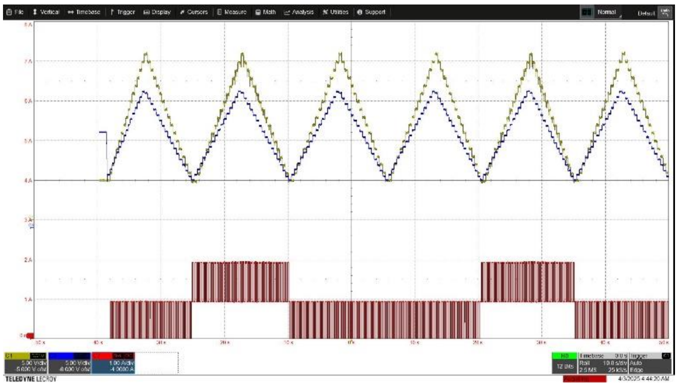
Figure 48 **Reverse-current protection**

4.12 Stress test waveforms

The RSC solution board was subjected to electrical stress conditions.

Electrical stress test: As follows for a duration of 15 minutes. Captured waveforms are shown in Figure 49.

- V_{IN}: Continuously changing from 05 V–18 V
- V_{BUS}: Continuously changing from 5 V–21 V and vice versa (PPS)
- I_{OUT}: Changing from 0 A to 1 A; 1 A to 2 A



CH1: V_{BUS}; CH3: V_{in}; CH7: I_{OUT}

Figure 49 **V_{BUS}: Continuously changing from 5 V-21 V (PPS) vice versa; I_{OUT}: 0 A-1 A; 1 A-2 A**

4.13 Current consumption

The EZ-PD™ CCG7SA4F RSC solution board measured currents are tabulated in Table 13.

Table 13 **Current consumption EZ-PD™ CCG7SA4F RSC board**

Test condition	Current	Remarks
Full active – Silicon current (into the silicon, pin #8)	19 mA 19 mA 25 mA	Buck mode operation (V_{IN}: 12 V_{DC}; V_{BUS}: 5 V) Boost mode operation (V_{IN}: 12 V_{DC}; V_{BUS}: 20 V) Buck-Boost mode operation (V_{IN}: 12 V_{DC}; V_{BUS}: 12 V)
Full active – Board current (measured at input connector) Port attached	29 mA 43 mA 44 mA	Buck mode operation (V_{IN}: 12 V_{DC}; V_{BUS}: 5 V) Boost mode operation (V_{IN}: 12 V_{DC}; V_{BUS}: 20 V) Buck-Boost mode operation (V_{IN}: 12 V_{DC}; V_{BUS}: 12 V)
Board current (measured at input connector) Port unattached	80 uA	V_{IN}: 12 V_{DC}

5 Thermal performance

DUT temperature measurements are captured at ambient temperature and at an elevated temperature.

5.1 Thermal image

- **Test condition**: V_{IN} = 13.5 V_{DC}, V_{BUS} = 20 V, I_{OUT} = 3.25 A
- **Lab ambient temperature**: 29.8°C. Thermal scan captured in open frame after 45 minutes (see Figure 50 and Table 14)

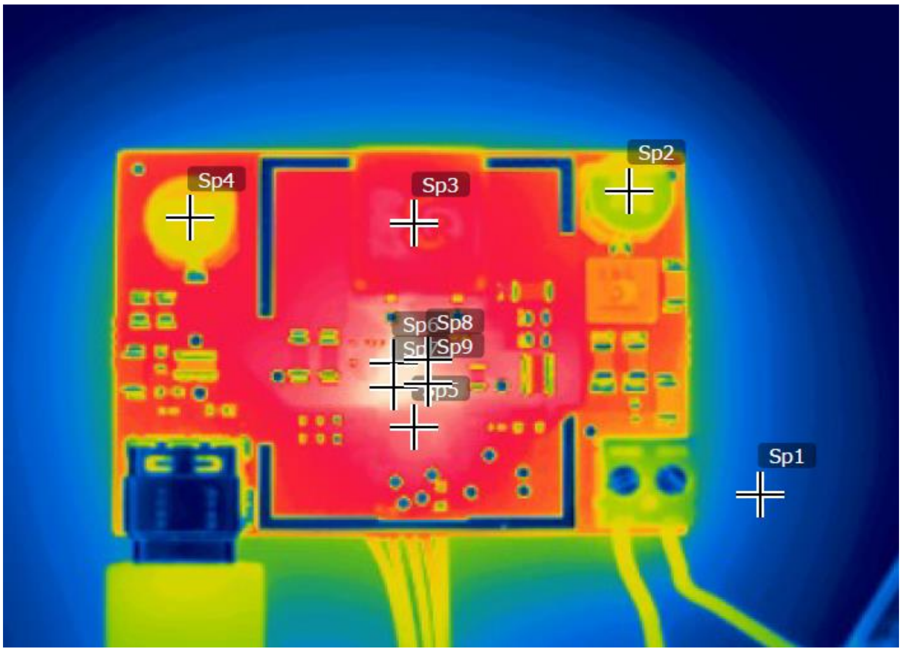


Figure 50 DUT (top) thermal image at ambient temperature, without standoff, V_{IN}:13.5 V_{DC}; V_{BUS}: 20 V, I_{OUT}:3.25 A

Table 14 Temperature measurement

Markers	Designator	Component	Temperature (°C)
Sp1	–	Ambient	29.8
Sp2	CE1	Input bulk capacitor	44.1
Sp3	L2	Power inductor	56.4
Sp4	CE2	Output bulk capacitor	45.9
Sp5	U1	CCG7SA4F	61.6
Sp6	LG2	Low side boost FET	72.2
Sp7	HG2	High side boost FET	73.8
Sp8	LG1	Low side buck FET	65.7
Sp9	HG1	High side buck FET	67.8

5.2 Temperature measurement at an elevated temperature inside an enclosure

- Test condition: V_{IN} = 13.5 V_{DC}, V_{BUS_C} = 20 V, I_{OUT} = 3.25 A
- Ambient temperature: 60°C and individual component temperatures captured using thermocouple tabulated in Table 15.
- Enclosure dimensions : 196 mm (L) × 60 mm (W) × 31 mm (H)

Table 15 RSC solution board component temperatures at an ambient of 60°C kept inside an enclosure

Designator	Component	Temperature at 60°C ambient (°C)
CE1	Input bulk capacitor	85.9
L2	Power inductor	98.2
CE2	Output bulk capacitor	88.7
U1	CCG7SA4F	101.7

6 Bode plots

Note: *Detailed test procedures and reports are available on request.*

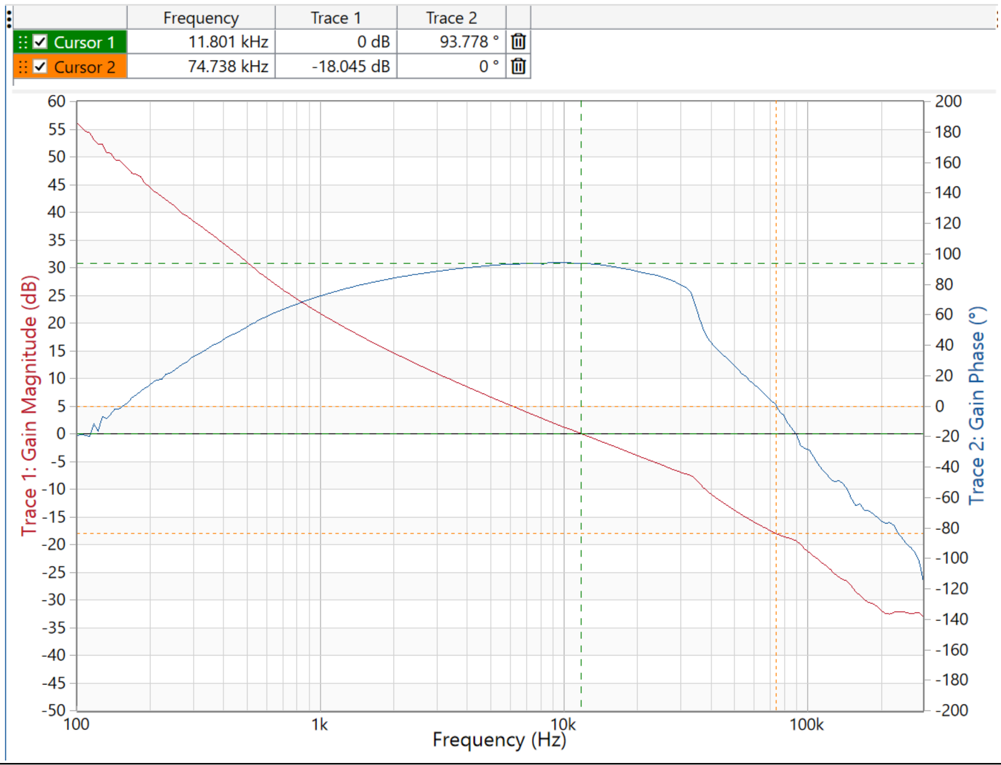


Figure 51 **Bode plot: - V_{IN}: 12 V_{DC}, V_{BUS}: 5 V; I_{OUT}: 3.25 A**

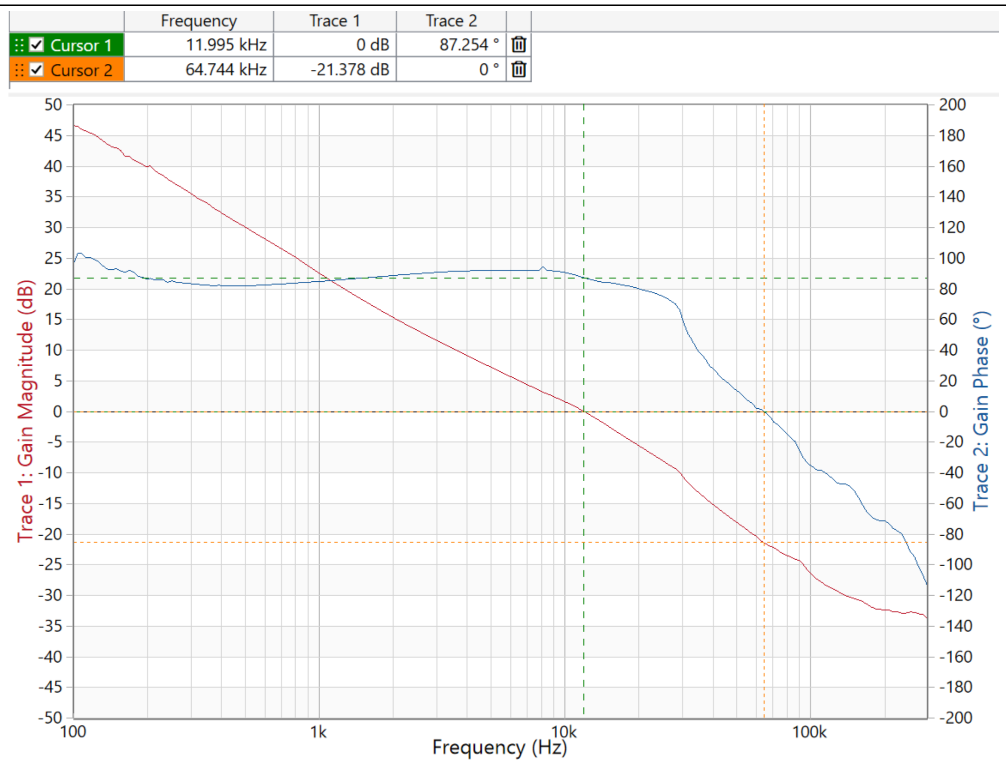


Figure 52 **Bode plot: - V_{IN}: 12 V_{DC}, V_{BUS}: 9 V; I_{OUT}: 3.25 A**

Bode plots

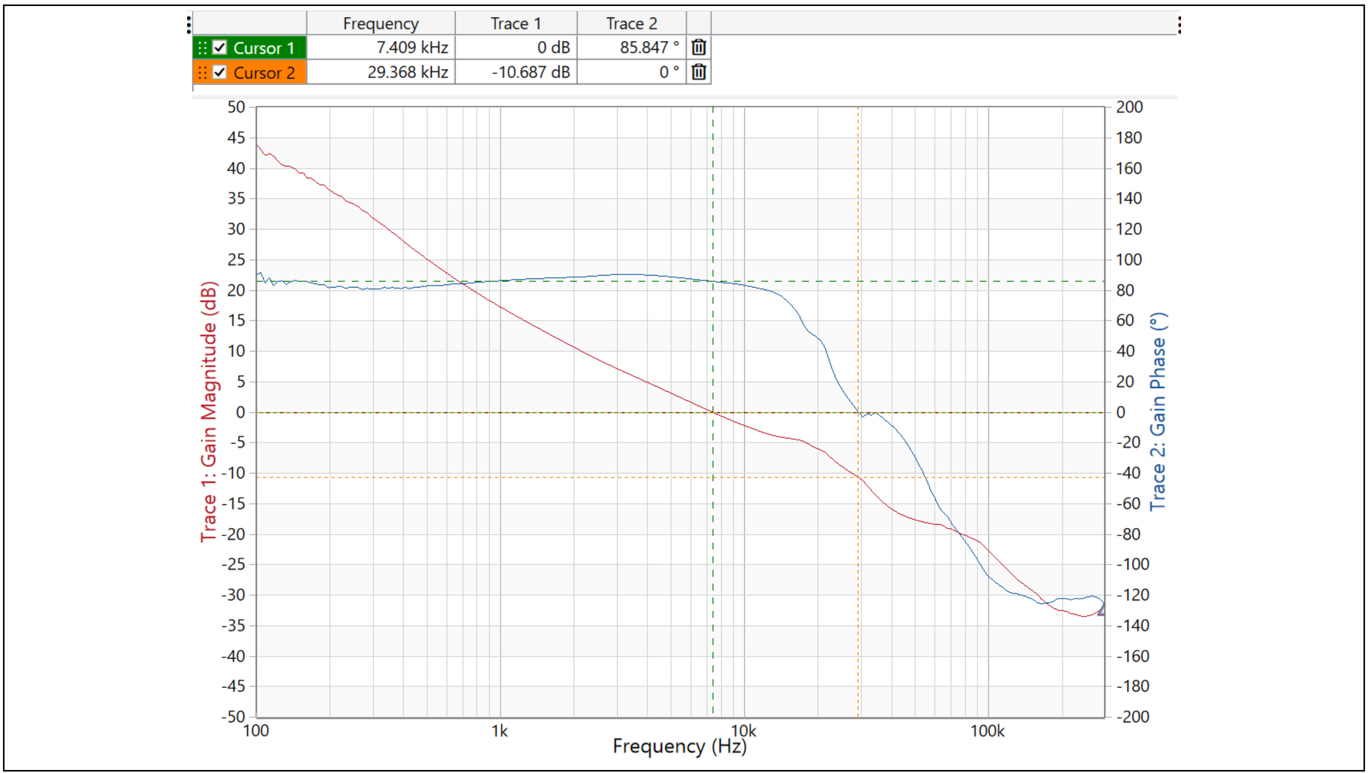


Figure 53 **Bode plot: - V_{IN}: 12 V_{DC}, V_{BUS}: 15 V; I_{OUT}: 3.25 A**

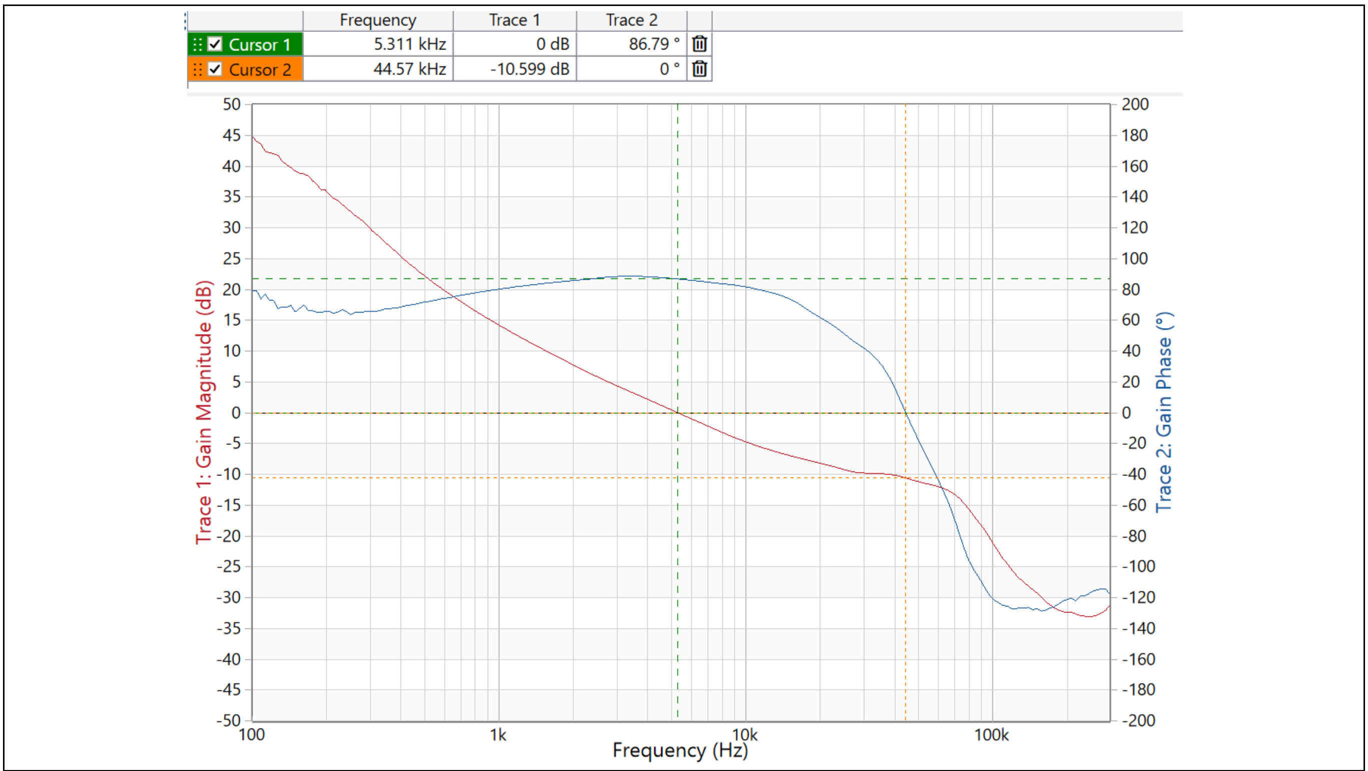


Figure 54 **Bode plot: - V_{IN}: 12 V_{DC}, V_{BUS}: 20 V; I_{OUT}: 3.25 A**

7 Circuit schematics, BOM, and PCB layout

Note: For schematics, BOM, and PCB layout, contact Infineon support.

8 Regulatory tests

The following regulatory pre-compliance tests are performed on the CCG7S RSC solution board.

8.1 ISO 10605: Road vehicles – Test methods for electrical disturbances from electrostatic discharge (ESD)

ESD test discharge pulses were applied on both the USB Type-C receptacles per the standard [8]. The test setup per ISO 10605 is shown in Figure 55.

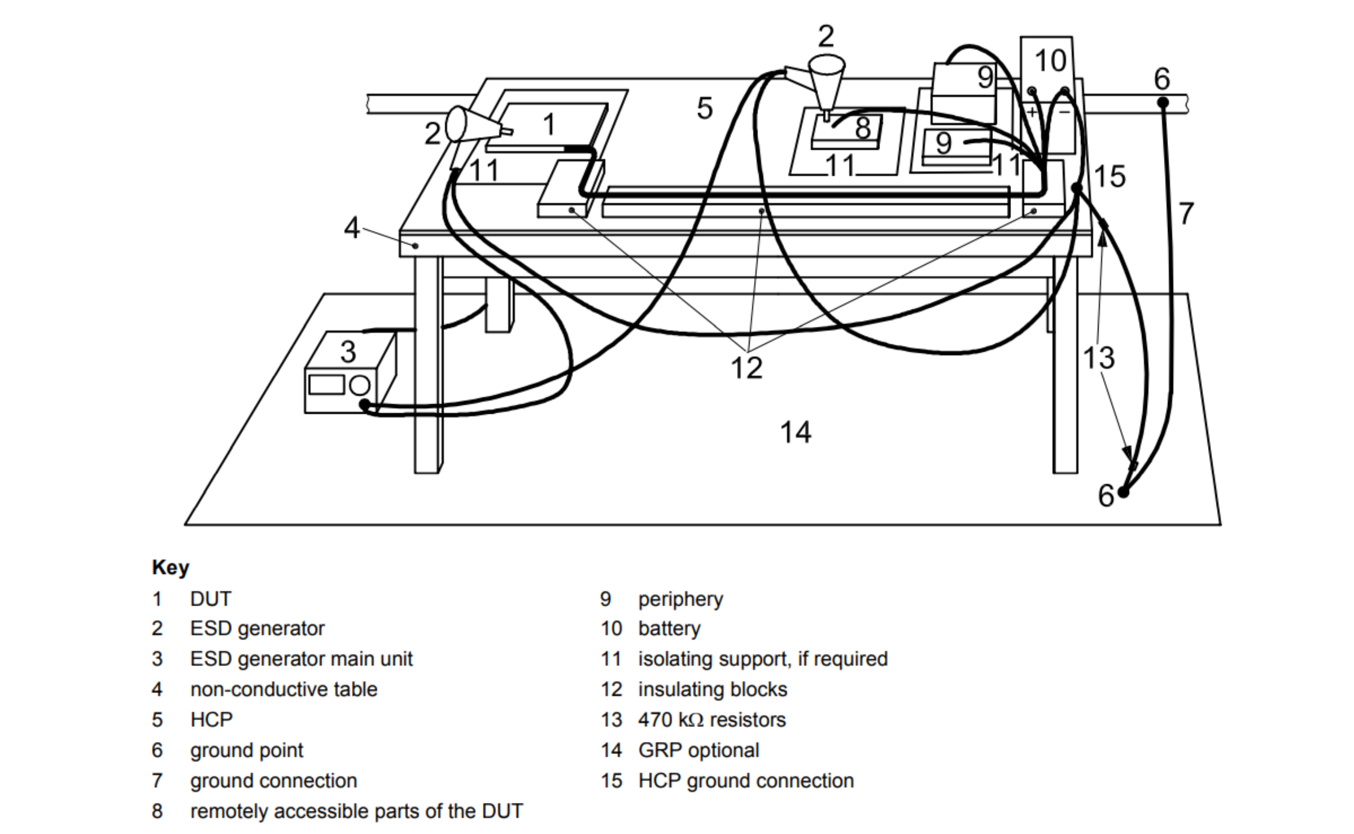


Figure 55 ESD test setup per ISO 10605 (source: ISO 10605 specification)

ISO 10605 ESD test parameters are shown in Table 16.

Table 16 ISO 10605 test parameters

Parameters	Characteristics
Storage capacitance	330 pF
Discharge resistance	330 Ω
Number of discharge cycles	10
Holding time	5 seconds
Output voltage contact-discharge mode	8 kV
Output voltage air-discharge mode	15 kV
Output polarity	Positive and negative

ESD test setup as shown in Figure 56.

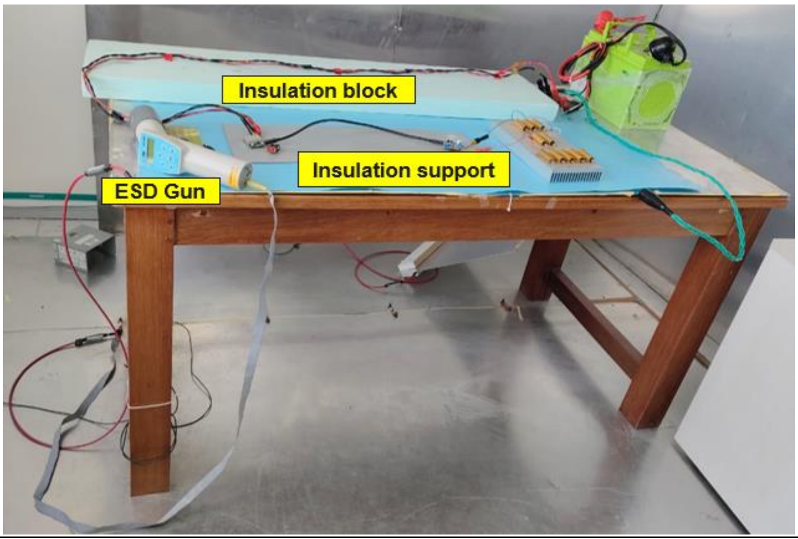
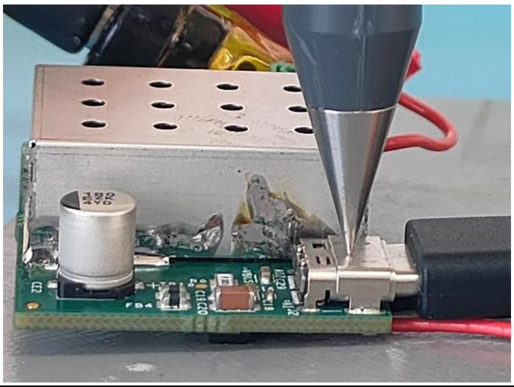


Figure 56 **ESD test setup**



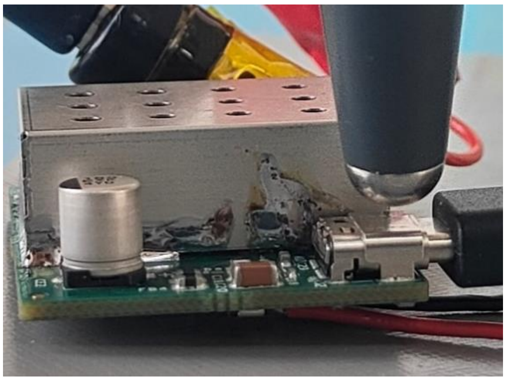


Figure 57 **Contact discharge, air discharge test setup**

Key ESD test setup details are:

- Keep the supply battery on the test table, with the negative terminal of the battery directly connected to the HCP
- Connect the discharge return cable of the ESD generator to the HCP
- Ensure that the length of the test harness between the DUT and the battery is 1.5 meters
- Place the test harness on a non-conductive, low-relative-permittivity (dielectric constant) material ($\varepsilon r \leq 1,4$), with a thickness of (50 ± 5) mm
- On the HCP, apply indirect discharge pulses 50 mm from the DUT input connector
- Apply direct type discharges (contact or air discharge mode) directly to the DUT parts that are accessible by vehicle users, e.g., USB Type-C connector
- Note that the indirect type discharges (contact discharge mode) simulate discharges that occur to other conductive objects in the vicinity of the DUT. Apply these through an intervening metal, such as an HCP
- In contact discharge mode, ensure that the tip of the ESD generator's discharge electrode is brought in contact with the DUT before the discharge switch is actuated to apply the discharge
- In air discharge mode, ensure that the discharge electrode is charged to the test voltage and then brought with the required speed of approach to the DUT. Apply the discharge through an arc that occurs when the tip approaches close enough to the DUT to break down the dielectric material between the tip and test point

- Apply the direct contact and direct air discharge ESD pulses on both ports of the USB Type-C connector
- For direct discharge, hold the ESD generator's discharge tip perpendicular to the surface of the DUT when possible; if not possible, ensure an angle of at least 45° to the surface of the DUT
- For discharges to coupling planes (i.e., indirect discharges), ensure that the discharge tip is in the same plane as the HCP while contacting the edge of the plane
- Include 2 x 470 kΩ resistors in the safety ground connection between HCP and ground point for powered-up tests

The air and contact direct discharge and HCP indirect discharge test results are shown in Table 17. The test conditions are V_{BUS} 20 V I_{OUT} 3.25 A.

Table 17 ESD test results

Test condition	Severity level	Observations
Direct contact discharge	± 8 kV	Status I
Direct air discharge	± 15 kV	Status I

Note: The port is loaded with its full rated output current while performing the ESD tests.

8.2 ISO 7637-2: Road vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only

The *ISO 7637-2 Road Vehicles – Electrical Disturbances from Conduction and Coupling – Part 2: Electrical Transient Conduction Along Supply Lines Only* standard specifies test methods and procedures to ensure the compatibility to conducted electrical transients of equipment installed on passenger cars and commercial vehicles fitted with 12 V or 24 V electrical systems. It describes bench tests for both the injection and measurement of transients. It is applicable to all types of road vehicles independent of the propulsion system (for example, spark ignition or diesel engine, electric motor).

These bench test methods are for measuring the transient emission on the supply lines and for the immunity of devices against transients. Each pulse is modeled to simulate a transient that could be created by a real event in the automotive.

Test pulse severity levels for nominal 12 V system are shown in Figure 58.

Test pulse[a]	Selected test level[b]	Test pulse severity level, U_s[cd] V			Min. number of pulses or test time	Burst cycle/ pulse repetition time	
		IV	III	I / II		min.	max.
1		–150	–112	–75	500 pulses	0,5 s	[e]
2a		+112	+55	+37	500 pulses	0,2 s	5 s
2b		+10	+10	+10	10 pulses	0,5 s	5 s
3a		–220	–165	–112	1 h	90 ms	100 ms
3b		+150	+112	+75	1 h	90 ms	100 ms

a Test pulses as in 5.6.

b Values agreed between vehicle manufacturer and equipment supplier.

c The amplitudes are the values of U_s as defined for each test pulse in 5.6.

d The former levels I and II are revised because they did not ensure sufficient immunity in subsequent road vehicles' design.

e The maximum pulse repetition time shall be chosen such that it is the minimum time for the DUT to be correctly initialized before the application of the next pulse and shall be ⩾0,5 s.

Figure 58 Test pulse severity levels for a nominal 12 V system

ISO 7637-2 and ISO 16750-2 test setup are shown in Figure 59.

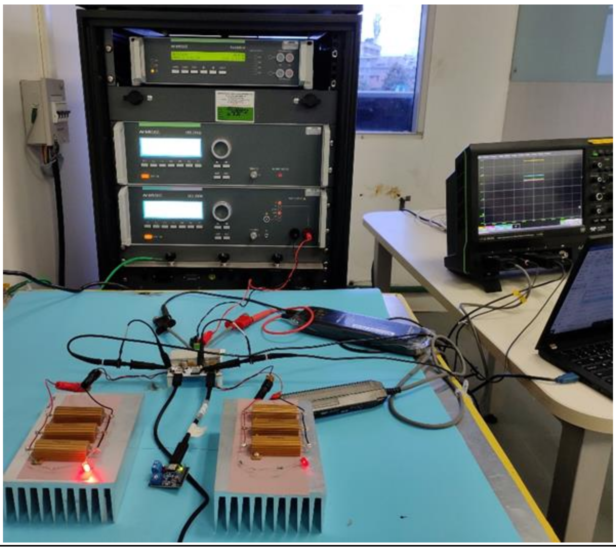


Figure 59 ISO 7637-2 and ISO 16750-2 test setup

The RSC solution board is subjected to ISO 7637-2 pulses, and the results are tabulated in Table 18.

Table 18 ISO 7637-2 test results

Test pulse	Severity level	Observations
1	IV	Status II
2a	IV	Status I
2b	IV	Status II
3 A	IV	Status I
3b	IV	Status I

8.3 ISO 16750-2: Road vehicles – Environmental conditions and testing for electrical and electronic equipment – Part 2: Electrical loads

This part of ISO 16750 applies to electric and electronic systems/components for road vehicles. This part of ISO 16750 describes the potential environmental stresses and specifies tests and requirements recommended for the specific mounting location on/in the road vehicle. This part of ISO16750 describes the electrical loads; electromagnetic compatibility (EMC) is not covered. Electrical loads are independent from the mounting location but can vary due to the electrical resistance in the vehicle wiring harness and connection system.

The RSC solution board is subjected to ISO 16570-2 pulses, and the results are tabulated in Table 19.

Table 19 ISO 16750-2 test results

Test pulse (ISO 16750-2:2012(E))	Severity level	Expected class	Observed class
			FCCM
4.2 Direct current supply voltage	Level IV	Class A	Class A
4.3.1.1 Overvoltage (Tmax – 20°C)	–	Class C (min) Class A (max)	Class A
4.3.1.2 Overvoltage: jump start	–	Class D (min) Class B (max)	Class B
4.4 Superimposed alternating voltage	Level II	Class A	Class A
4.5 Slow decrease and increase of supply voltage	–	Class D (min) Class C (max)	Class B
4.6 Discontinuities in supply voltage 4.6.1 Momentary drop in supply voltage	–	Class B	Class B
4.6.2 Reset behavior at voltage drop	–	Class C	Class B
4.6.3 Starting profile	Level IV	Class A	Class A
4.7 Reversed voltage	–	Class A	Class A
4.8 Ground reference and supply offset)	–	Class A	Class A
4.9 Open-circuit tests 4.9.1 Single line interruption	–	Class C	Class C[1]
4.9 Open circuit tests 4.9.2 Multiple line interruption	–	Class C	Class C[2]
4.10 Short-circuit protection	–	Class C	Class C[3]

Note:

1. *Output Type-C connector disconnected and reconnected*
2. *Output Type-C connector disconnected and reconnected*
3. *Output short-circuit at the DUT end; after reconnecting, the USB Type-C cable contract is made*
4. *Port is loaded to its full rated output current while performing the ISO7637-2 and ISO16750-2 tests*

9 Appendix: Efficiency measurement test setup

Efficiency measurements are captured with the test setup (RSC board input connector to output connector); measurement points are shown in Section 9.1.

9.1 Efficiency measurement: Input connector to the Type-C connector on the board

The measurement includes reverse polarity protection MOSFET, input differential mode inductor, input ferrite beads, output ferrite beads, NGDO FET/provide FET, V_{BAT}-to-ground protection FET, and its sense resistor. Measurement equipment connectivity is shown in Figure 60.

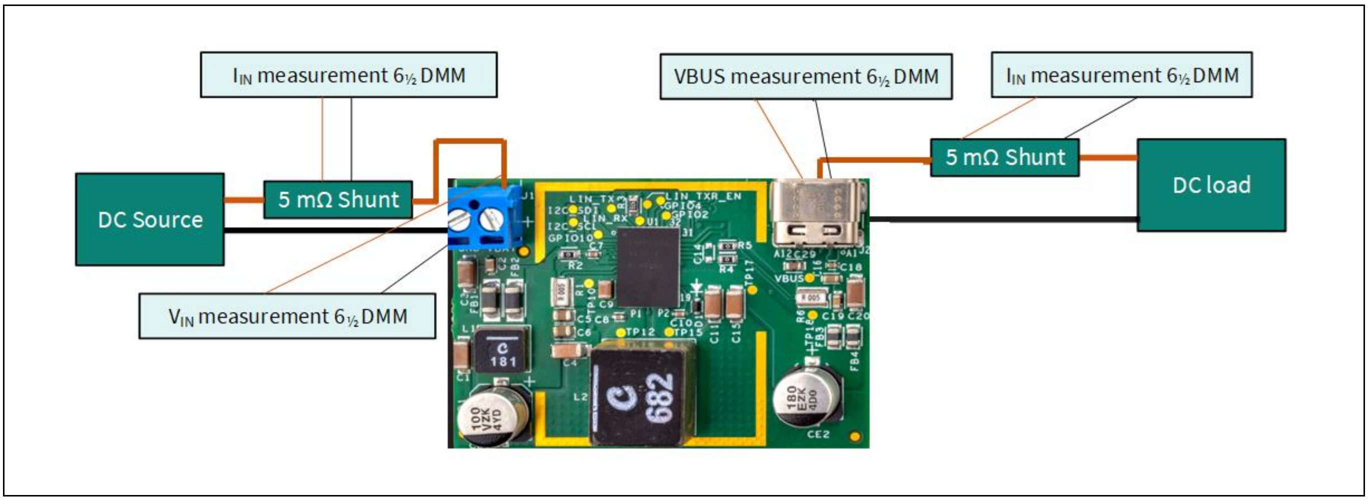


Figure 60 **Efficiency measurement - Input connector to the Type-C connector on the board**

References

Contact Infineon Support to obtain these documents.

[1] Infineon Technologies AG: *002-41345: EZ-PD™ CCG7SA4F Automotive Rear Seat Charger Solution Demo Kit (REF_CCG7SA4F_65W_RSC) user guide*

[2] Infineon Technologies AG: *002-41638: EZ-PD™ CCG7SA4F controller-based rear seat charger power stage design calculator*

[3] Infineon Technologies AG: *002-34222: Hardware Design Guidelines for EZ-PD™ CCG7X in Automotive Applications*

[4] Infineon Technologies AG: *AN241514: USB PD Type-C rear seat charger reference board with EZ-PD™ CCG7SA4F controller*

[5] Infineon Technologies AG: *002-40408: EZ-PD™ CCG7SA4F Automotive single-port USB Type-C with PD and buck-boost controller*

[6] Infineon Technologies AG: *002-34406: EZ-PD™ CCG7Sxx MCU architecture reference manual*

[7] Infineon Technologies AG: *002-34828: EZ-PD™ CCG7Sxx Registers reference manual*

[8] Infineon Technologies AG: *ISO 10605 Road vehicles – Test methods for electrical disturbances from electrostatic discharge*

[9] Infineon Technologies AG: *CISPR 25 Edition 4.0 2016-10: Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers*

[10] Infineon Technologies AG: *ISO 16750-2 Road vehicles – Environmental conditions and testing for electrical and electronic equipment – Part 2: Electrical loads*

[11] Infineon Technologies AG: *ISO 7637-2 Road vehicles – Electrical disturbances from conduction and coupling — Part 2: Electrical transient conduction along supply lines only*

Revision history

Document revision	Date	Description of changes
**	2025-06-12	Initial release
*A	2025-06-27	Table 6: Firmware build is updated Section 4.1: Efficiency numbers are updated Section 4.2: Efficiency and power loss graphs are updated Section 4.3.1: Output voltage regulation graphs are updated Section 4.4: % Regulation has been updated Section 4.5.2: Peak to peak voltage ripple is updated Section 4.5.3: Peak to peak voltage ripple is updated
*B	2025-10-28	Formatting and pagination issues are resolved USB-IF pre-compliance section removed
*C	2026-01-20	Board current unattached state added Elevated temperature enclosure dimensions added

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