RIC74424EVAL1 user guide

Open loop dual output gate driver with R9 FETs

About this document

RIC74424 is a high speed, dual channel low side gate driver. This evaluation board is designed to help the user evaluate RIC74424 with any other rad hard MOSFET in a SupIR-SMD, SMD-0.5 or SMD-0.5e package. It comes prepopulated with IRHNJ9A7130 and IRHNS9A7064. This user manual includes overview, setup instructions, test results, schematic, printed circuit board layout drawings and bill of material. More information is available on the RIC74424 product landing page and RIC74424 datasheet.

Intended audience

This document is intended for engineers who are familiar with MOSFET or IGBT based converters, inverters and gate drivers and are looking to evaluate and design RIC74424 into their application.

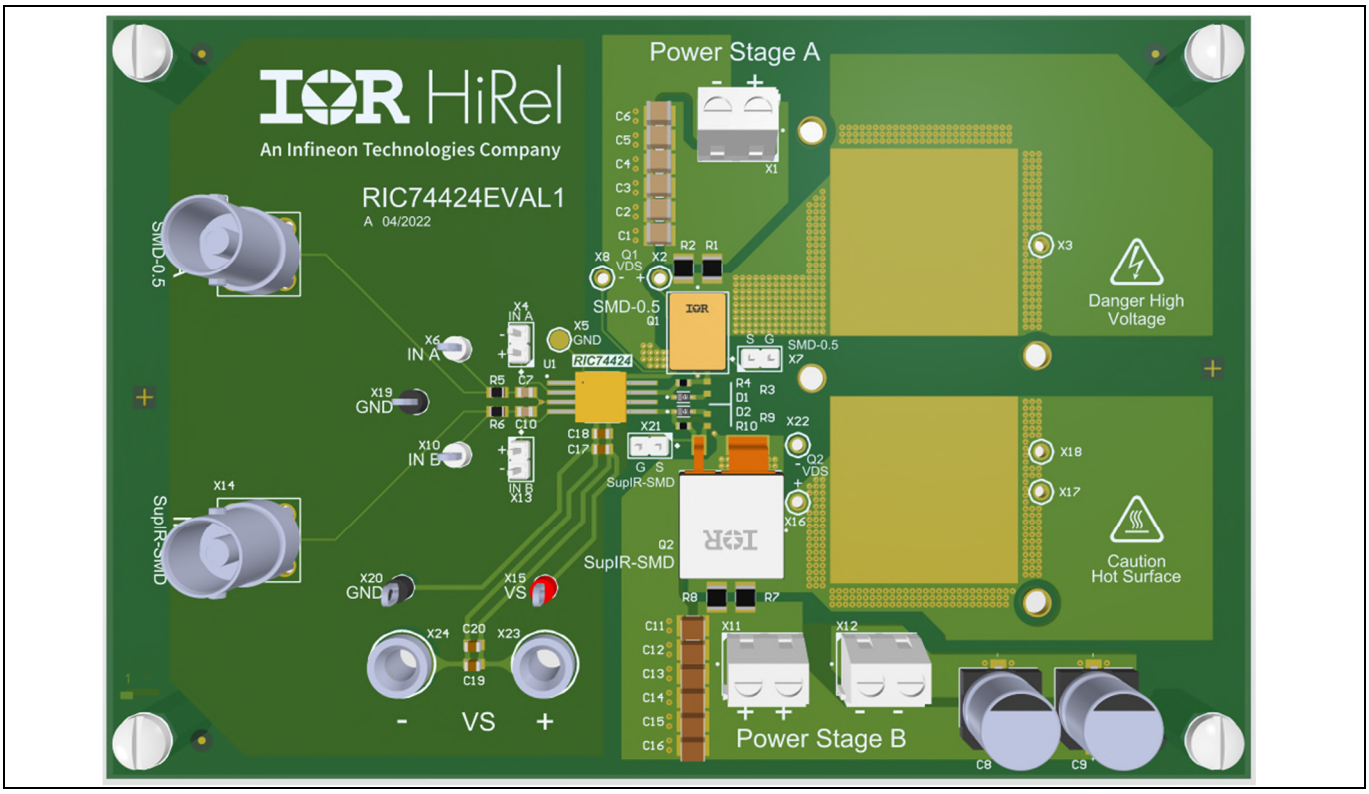


Figure 1 RIC74424EVAL1

Table 1 Safety warning

	**Warning:** RIC74424EVAL1 has capacitance across Power Stage A and Power Stage B connectors on board. If high voltage is applied to Power Stage A or Power Stage B please be sure to follow all safety precautions and ensure that voltage is fully discharged before handling.
	**Warning:** Operation under certain conditions may cause the board to become hot. Ensure that all safety precautions are followed before handling.

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1 Introduction

RIC74424 is a high speed, non-inverting, dual channel low side gate driver. RIC74424EVAL1 comes pre-populated with IRHNJ9A7130 (100 V, 35 A in SMD-0.5 package) and IRHNS9A7064 (60V, 100 A in SupIR-SMD package). Either FET can be replaced with any other FET in a SMD-0.5, SMD-0.5e or SupIR-SMD package that are commonly used for rad hard MOSFET such as R9 MOSFET and rad hard PowerMOS. RIC74424EVAL1 default configuration is setup for dynamic test measurements, such as propagation delay and rise/fall time. It can be modified to support additional tests.

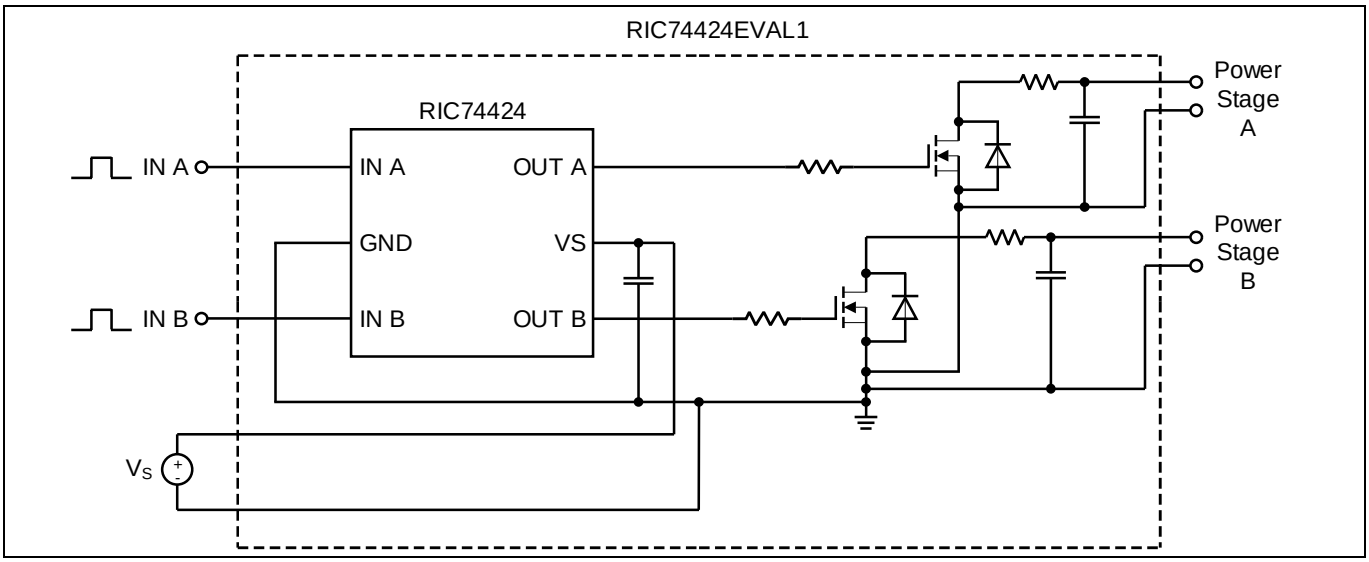


Figure 2 Simplified schematic of RIC7S113EVAL1

1.1 Feature list

- Independent bias power input with banana jack and test point connectors
- Dual, independent power stage for each FET
- Independent BNC and test point connections for both PWM inputs
- Power transistor footprint supports SupIR-SMD, SMD-0.5 and SMD-0.5e packages
- PCB layout and test points optimized for ease of use for engineering evaluation

1.2 Recommended operating conditions

For proper operation, the device should be used within the recommended operating conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated.

Table 2 RIC74424EVAL1 recommended operating conditions

Symbol	Definition	Min	Typ	Max	Units
V_{PSA}	Power stage voltage on Power Stage A (default IRHNJ9A7130)			100	V
V_{PSB}	Power stage voltage on Power Stage B (default IRHNS9A7064)			60	V
V_S	VS bias voltage	5		20	V
V_{IN}	Logic input voltage (IN A, IN B)	0		VS	V
t_{on}	FET on time[1]			10	µs
t_p	Period between FET on time[1]	10			ms

[1] Refer to section 2.3.2 Power stage for details

2 Functional description

2.1 Bias power

For proper operation, an external bias power supply is required for VS. The drive voltage of RIC74424 is set by the voltage on VS. It is recommended to keep VS within the recommended operating range for RIC74424, which is 5 V to 20 V. Bias voltage for VS can either be applied thru the banana jacks or the test points. The banana jack and test points have independent traces to the VS bypass capacitors C17 and C18, which allow for Kelvin measurements of VS for improved measurement accuracy. Connection details are summarized in Table 3.

Table 3 VS connections

VS polarity	Banana jack	Test point
Positive (+)	X23	X15
Return (-)	X24	X20

2.2 Logic inputs

RIC74424EVAL1 has independent PWM inputs for IN A and IN B. BNC connectors are available for both inputs to allow for direct connection with waveform generators. Alternatively, test points are also available. Both inputs have a low pass RC filter between both connectors and RIC74424, which intended to eliminate any potential undesired high frequency noise. Depending on actual performance this filter can be adjusted or removed. Additional test points, which are connected to the IN A and IN B pin after the low pass RC filter, are provided to allow for precise measurement of the input voltage on the RIC74424 IN A and IN B pins. These test points are a 100 mil connector to allow for direct use with high accuracy active differential oscilloscope probes. Connection details are summarized in Table 4.

Table 4 Input connector details

Channel	FET	BNC input connector	Test point input connector		Low pass RC filter	Test point measurement	
			Positive (+)	Negative (-)		Positive (+)	Negative (-)
A	SMD-0.5/e (Q1)	X9	X6	X19	R5, C7	X4 pin 1	X4 pin 2
B	SupIR-SMD (Q2)	X14	X10	X19	R6, C10	X13 pin 1	X13 pin 2

2.3 Output

RIC74424EVAL1 is configured to drive two independent FET, each with their own gate drive and power stage.

2.3.1 Gate drive

The default configuration for RIC74424EVAL1 has a single gate drive resistor for both turn on and turn off. The gate drive strength can be modified to be asymmetrical, where turn on and off strength are different, by populating the second gate drive resistor. A diode is pre-populated in a way where this second resistor adds a resistor in parallel during turn off transition, reducing the total resistance. Test points for the gate to source measurement of both FET are also provided. These test points are a 100 mil connector to allow for direct use with high accuracy active differential oscilloscope probes. Details are summarized in Table 5.

Attention: ***Gate to source test points introduce small amounts of parasitic inductance, which increases measured voltage overshoot and ringing. For critical measurements of amplitude and settling time, it is recommended to place oscilloscope probes directly on gate and source pins of the FET.***

Table 5 Gate drive details

Channel	FET	Gate turn on resistor (default populated)	Gate turn off resistor (default not-populated)	Test point measurement	
				Positive (+)	Negative (-)
A	SMD-0.5/e (Q1)	R4	R3	X7 pin 2	X7 pin 1
B	SupIR-SMD (Q2)	R10	R9	X21 pin 2	X21 pin 1

2.3.2 Power stage

RIC74424EVAL1 features two independent power stages, the first with a footprint supporting either SMD-0.5 or SMD-0.5e package and the second with a footprint supporting SupIR-SMD package. These packages are commonly used for a number of rad hard FET, such as rad hard R9 MOSFET and rad hard PowerMOS families.

The power stage is configured for a switching time test circuit, where a DC supply voltage is connected to the drain of the FET through an external drain resistor. The intended operation is that a DC voltage is applied to the power stage input connector, which is applied to the drain of the FET. The FET is then momentarily turned on, which causes the drain voltage to decrease to about 0 V. The current through the channel of the FET is limited by the drain resistor and FET drain to source on state resistance ($R_{DS(on)}$). When the FET is turned off, the drain voltage rises back to the DC supply voltage. This switching transition allows for rise and fall time measurements. Capacitors are populated on both power stage inputs to help hold up the DC supply voltage during this switching transition. If the FET or external resistance is changed, additional capacitance may be needed.

The current through the channel of the FET is limited by the drain resistor. While this drain resistor are two higher power rated devices in a 1210 package (500 mW each, for 1 W total), they are not intended to always be on. If the FET is on too frequently these resistors can overheat and fail. As a result, it is recommended to limit the frequency that the FET is on. This can be done by reducing the on-time pulse width and frequency when on-time pulses occur. The exact limit depends on operating conditions, such as operating voltages and ambient temperature, but general recommendation is to limit the on-time pulse width less than 10 µs and limit the frequency when the FET is on to greater than 10 ms. Details are shown in Figure 3. If the desired operating times are close or exceed the recommended limits, it is recommended to slowly bring up the test while measuring drain resistor temperature.

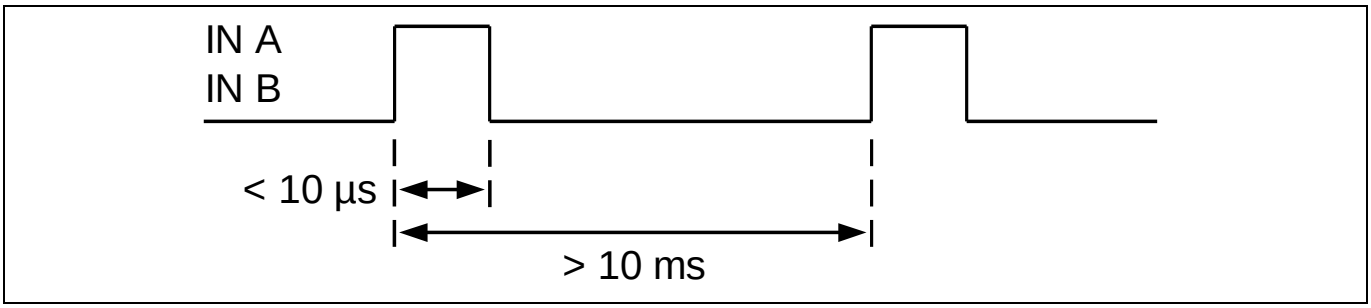


Figure 3 Timing diagram for recommended gate input signal

Test points for drain to source voltage (V_{DS}) measurements are provided for accurate measurements. It is recommended that ground spring connections are used with oscilloscope probes to reduce measurement error. Details on components for power stage and test points are in Table 6.

Table 6 Power stage details

Channel	FET package	Default FET populated	Power stage connector		DC supply capacitors	Drain resistors	V_{DS} test point measurement	
			Positive (+)	Negative (-)			Positive (+)	Negative (-)
A	SMD-0.5/e	IRHNJ9A7130	X1 pin 1	X1 pin 2	C1, C2, C3, C4, C5, C6	R1, R2	X2	X8
B	SupIR-SMD	IRHNS9A7064	X11 pin 1 and 2	X12 pin 1 and 2	C8, C9, C11, C12, C13, C14, C15, C16	R7, R8	X16	X22

2.4 Optional heat sink

For higher power tests an external heat sink may be desired. RIC74424EVAL1 has an exposed copper area that is intended to connect with a heatsink. Exposed copper area and fastener holes are sized for Advanced Thermal Solutions Inc. pushPIN™ series of heatsinks with x-y size of 25 mm × 25 mm, such as ATS-05H-75-C2-R0 or ATS-P1-139-C3-R0.

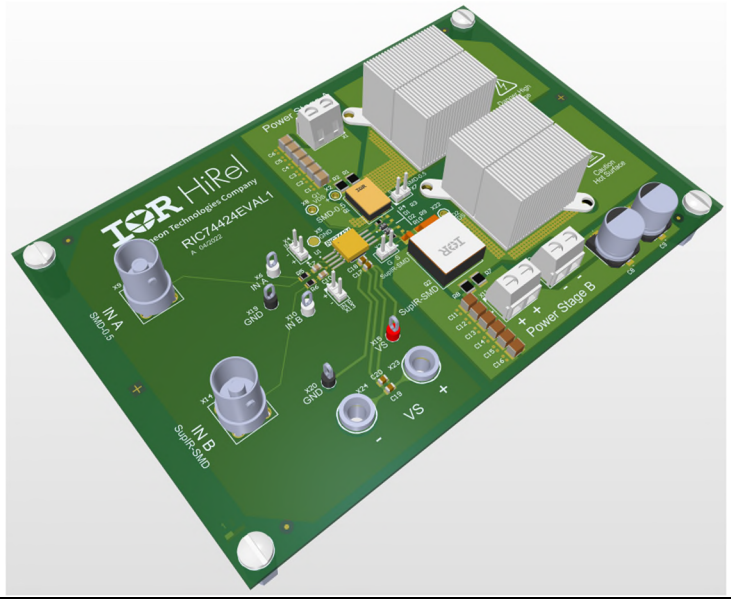


Figure 4 RIC74424EVAL1 with optional heatsink assembled

2.5 Test points

To simplify measurement and improve accuracy test points are provided. For efficiency measurements, it is recommended that VS and drain to source voltage are measured from the corresponding test point to prevent cable and connector loss from impacting measurement. For all gate to source measurement, a 100 mil header is provided to allow for use with a low capacitance, high frequency active differential probe for improved measurement accuracy. For all other measurements with oscilloscope probes, it is recommended that ground spring connections are used to improve measurement accuracy.

Attention: ***Gate to source test points introduce small amounts of parasitic inductance, which increases measured voltage overshoot and ringing. For critical measurements of amplitude and settling time, it is recommended to place oscilloscope probes directly on gate and source pins of the FET.***

Table 7 Test points

Measurement	Device	Test point	
		Positive (+)	Negative (-)
IN A voltage	RIC74424	X4 pin 1	X4 pin 2
IN B voltage	RIC74424	X13 pin 1	X13 pin 2
VS bias voltage	RIC74424	X15	X20
Q1 gate to source	SMD-0.5/e FET	X7 pin 2	X7 pin 1
Q1 drain to source	SMD-0.5/e FET	X2	X8
Q2 gate to source	SupIR-SMD FET	X21 pin 1	X21 pin 2
Q2 drain to source	SupIR-SMD FET	X16	X22

2.6 NC pins and metal lid

In space and other high radiation environments that RIC74424 is targeted to work in, it is often times undesired to have electrically floating conductors since they can build up charge and cause electrostatic discharge (ESD) among other undesired effects. To prevent this all of the NC pins on RIC74424 are connected to GND. While the metal lid on RIC74424 is not connected to a known potential by default, it can be connected to GND with a wire through the exposed pad X5.

3 Recommended operation

3.1 Equipment

The following equipment is recommended to operate RIC74424EVAL1

- 5 V to 20 V power supply capable of at least 100 mA for VS bias supply
- DC voltage power supply with voltage and current capability high enough for power level of planned test
- Signal generator to provide PWM input for IN A and IN B capable of at least 0 V to 5 V with minimum pulse width less than 1 ns
- Oscilloscope and probes for measurement with at least 200 MHz bandwidth to capture high slew rate and high frequency ringing
- Multimeter or source meter with resolution of at least 100 nA to measure quiescent current of bias power rails

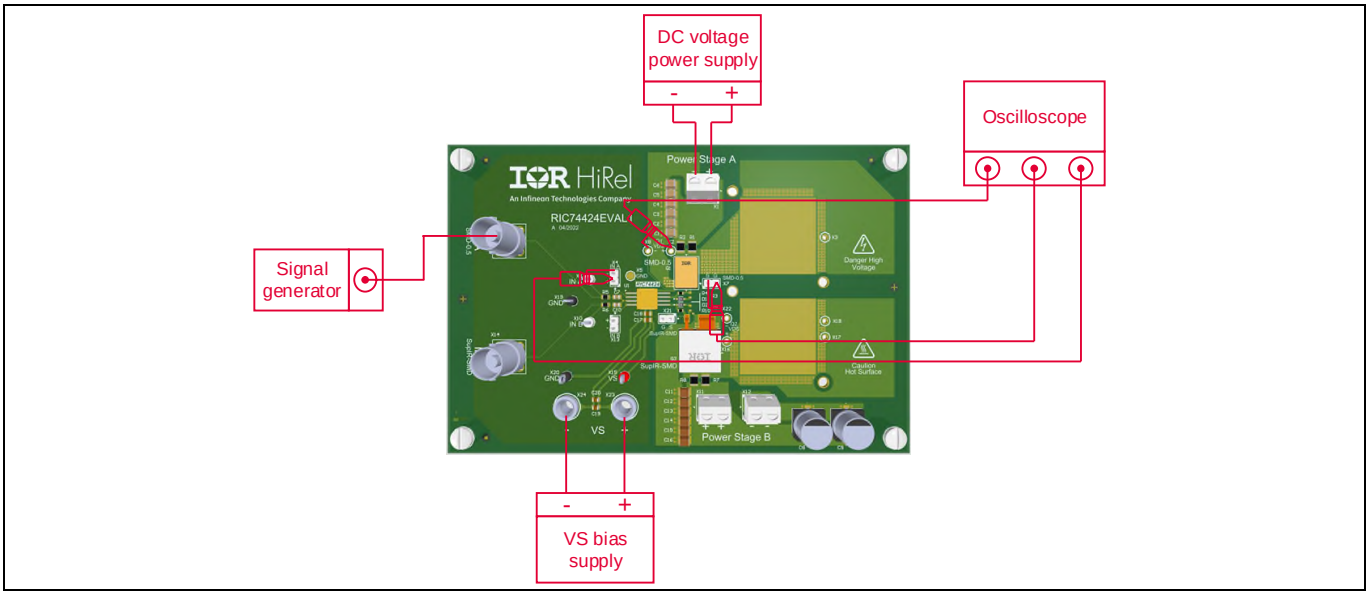


Figure 5 Recommended configuration of RIC74424EVAL1 when testing Q1 (SMD-0.5/e)

3.1.1 Power up

The following procedure is recommended for powering up RIC74424EVAL1:

1. Connect VS bias supply, DC voltage power supply, signal generator and measurement probes
2. Enable VS
3. Enable DC voltage power supply
4. Enable signal generator

3.1.2 Power down

The following procedure is recommended for powering down RIC74424EVAL1:

1. Disable DC voltage power supply
2. Disable signal generator
3. Disable VS
4. Remove VS bias supply, DC voltage power supply, signal generator and measurement probes

4 Test results

4.1 Switch time test circuit

The following section shows test results for a switch time test circuit. IN A and IN B are a single pulse 0V to 5V signal with 1 µs on time. All measurements are measured with respect to ground.

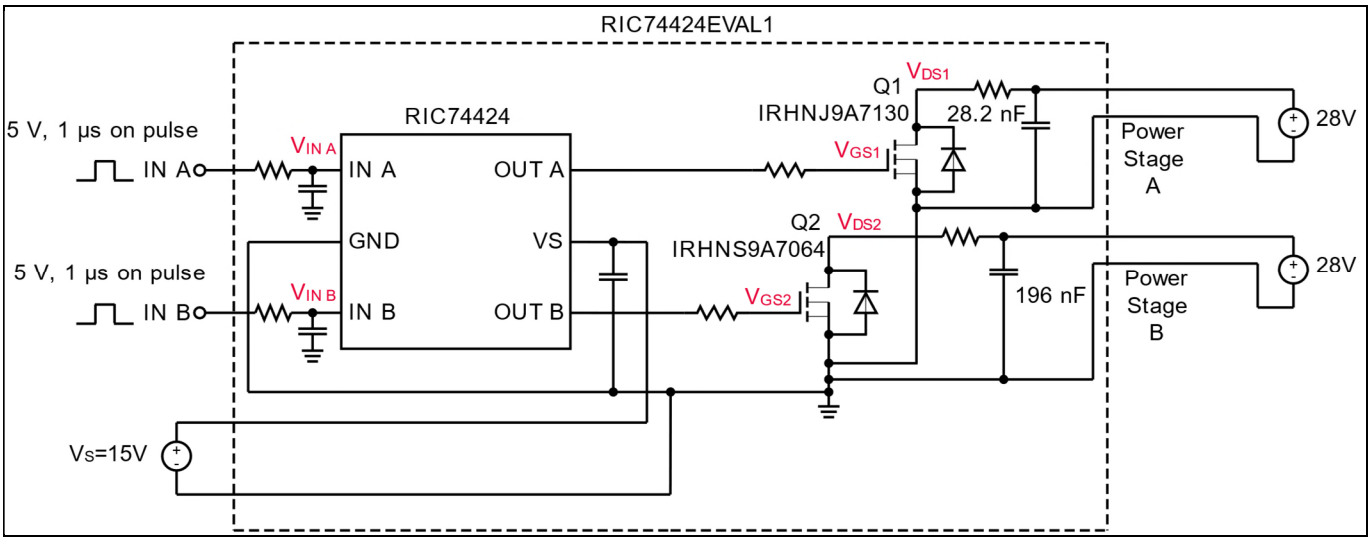


Figure 6 Simplified schematic of RIC74424EVAL1 configured in switch time test circuit

4.1.1 Q1 (IRHNJ9A7130, SMD-0.5 package) waveforms

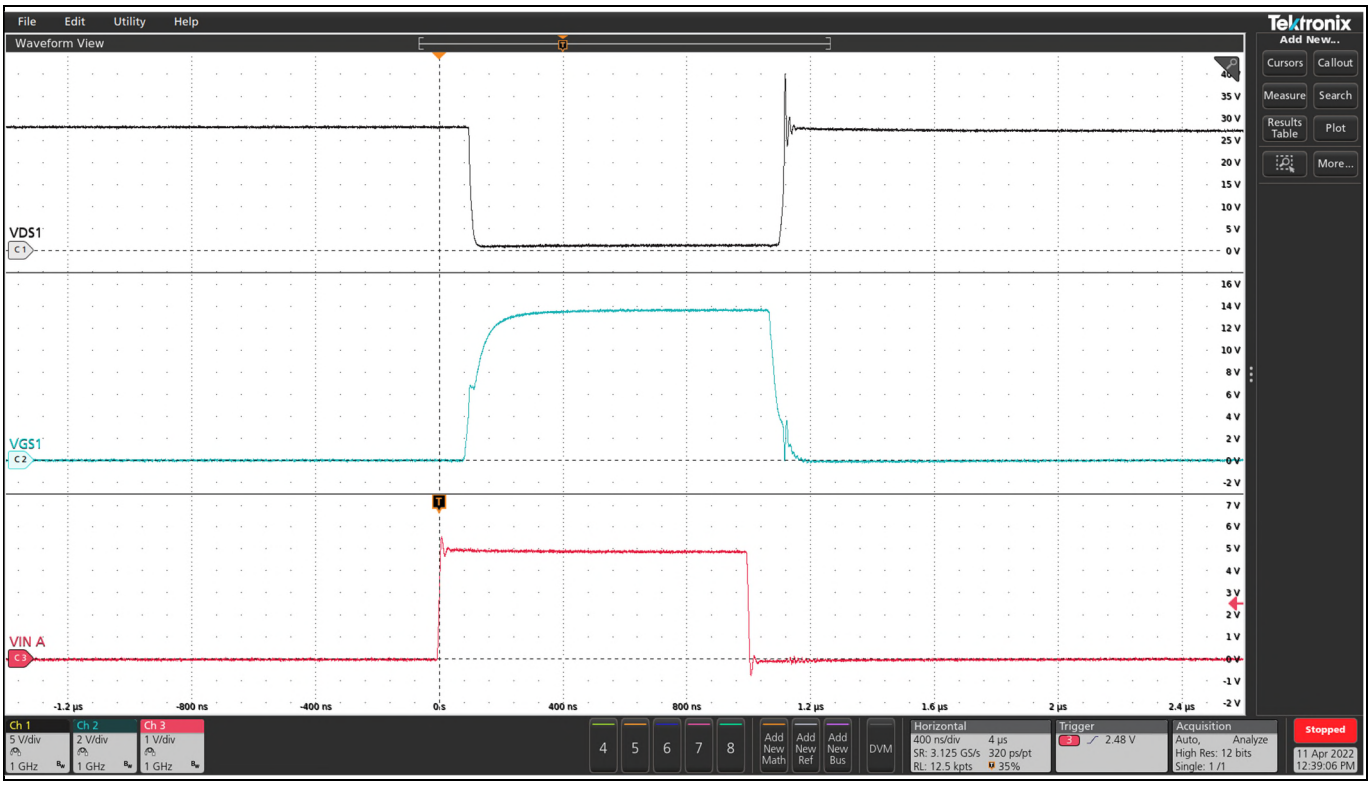


Figure 7 V_{DS1} (C1, black), V_{GS1} (C2, blue) and $V_{IN\,A}$ (C3, red) during turn on and turn off of Q_1

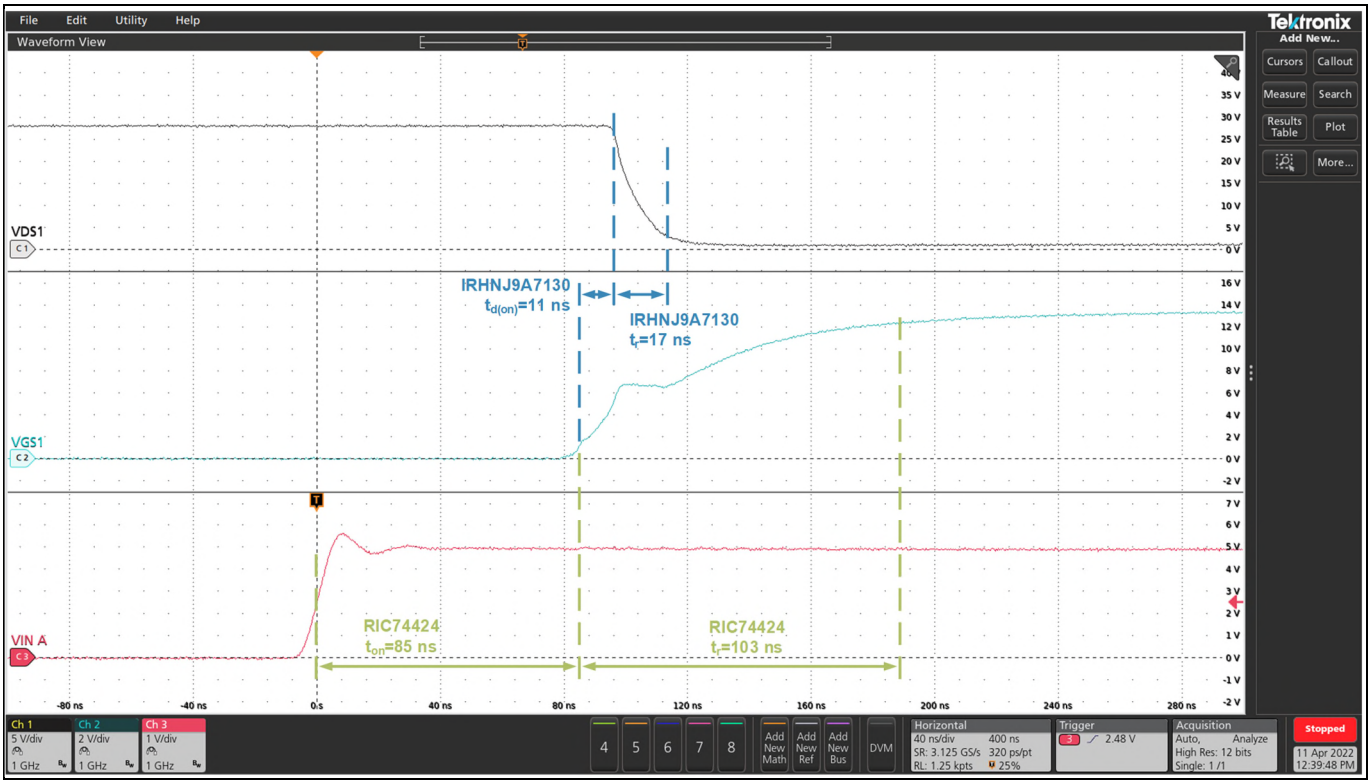


Figure 8 V_{DS1} (C1, black), V_{GS1} (C2, blue) and $V_{IN\,A}$ (C3, red) during turn on of Q_1

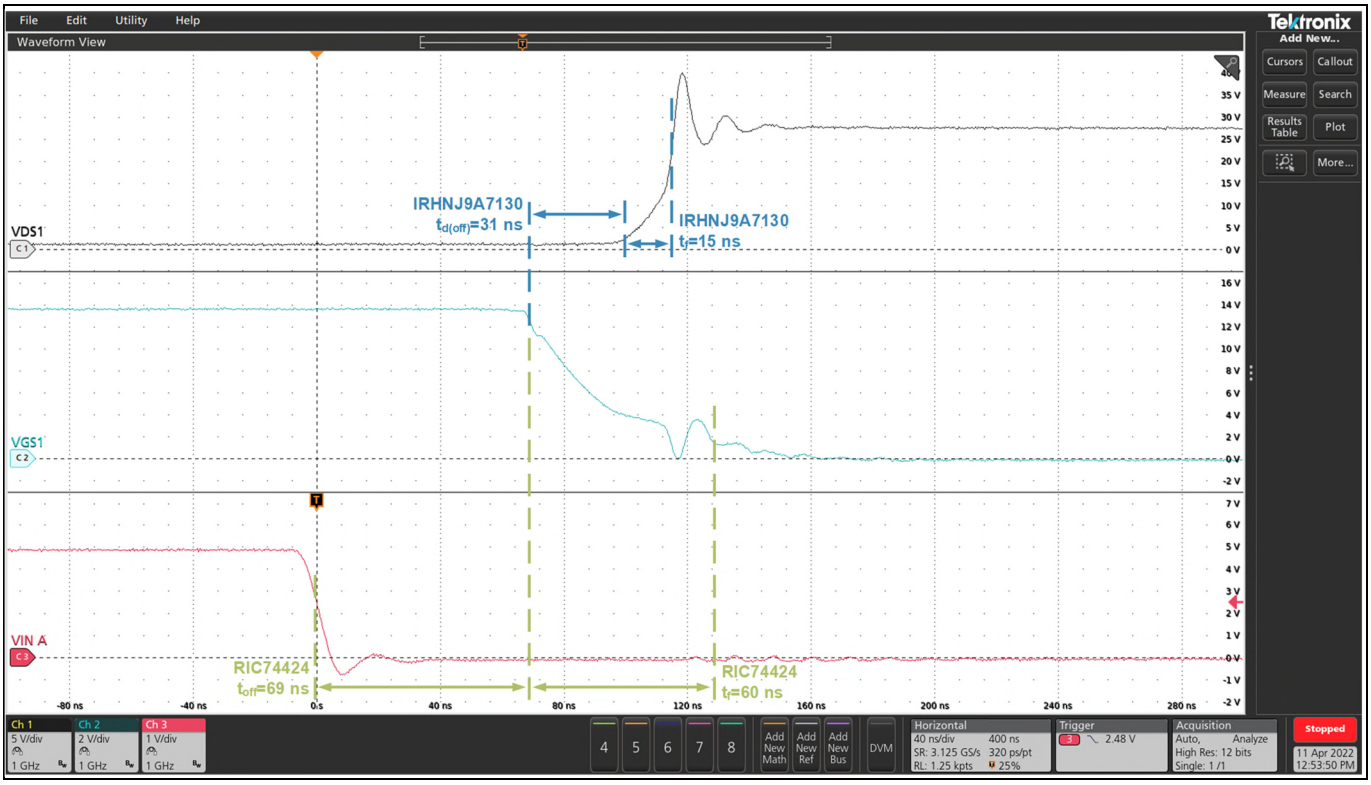


Figure 9 V_{DS1} (C1, black), V_{GS1} (C2, blue) and $V_{IN\,A}$ (C3, red) during turn off of Q_1

4.1.2 Q2 (IRHNS9A7064, SupIR-SMD package) waveforms

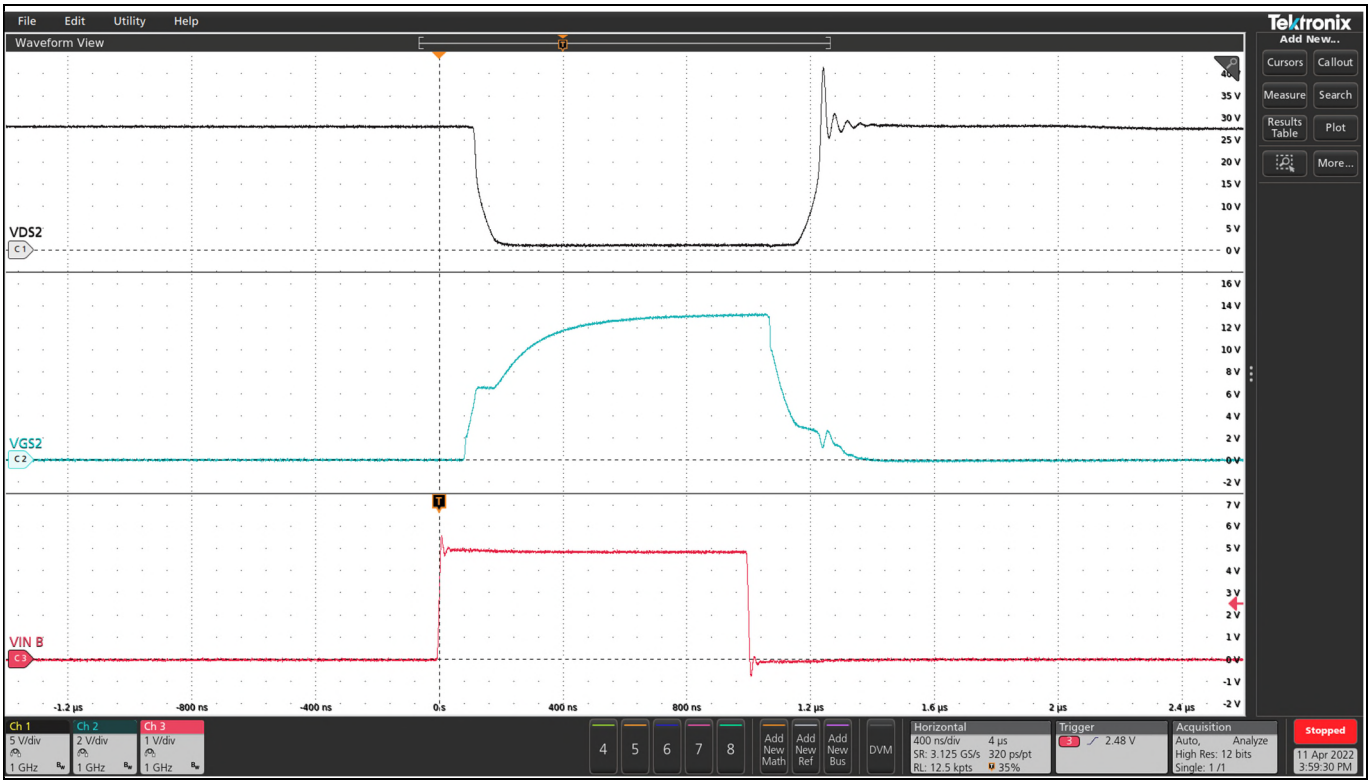


Figure 10 V_{DS2} (C1, black), V_{GS2} (C2, blue) and $V_{IN\,B}$ (C3, red) during turn on and turn off of Q_2

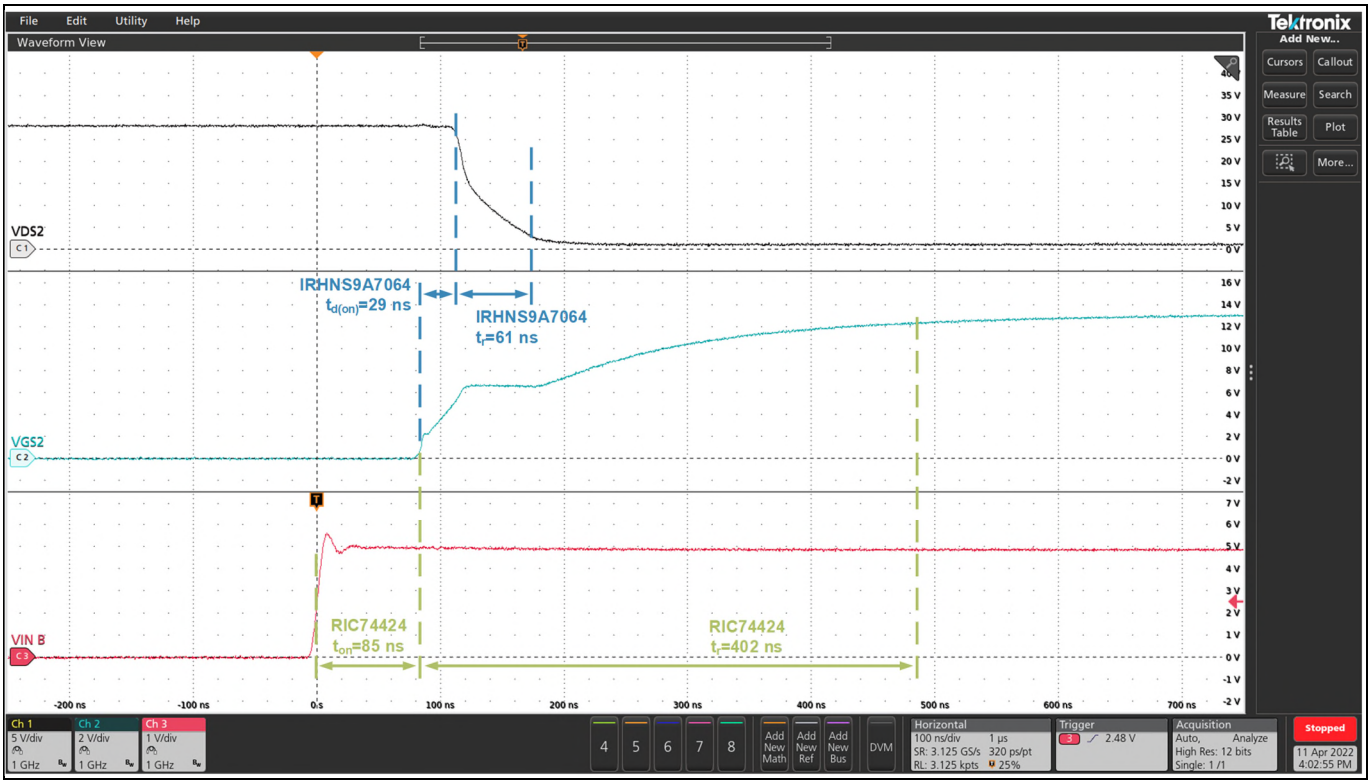


Figure 11 V_{DS2} (C1, black), V_{GS2} (C2, blue) and $V_{IN\,B}$ (C3, red) during turn on of Q_2

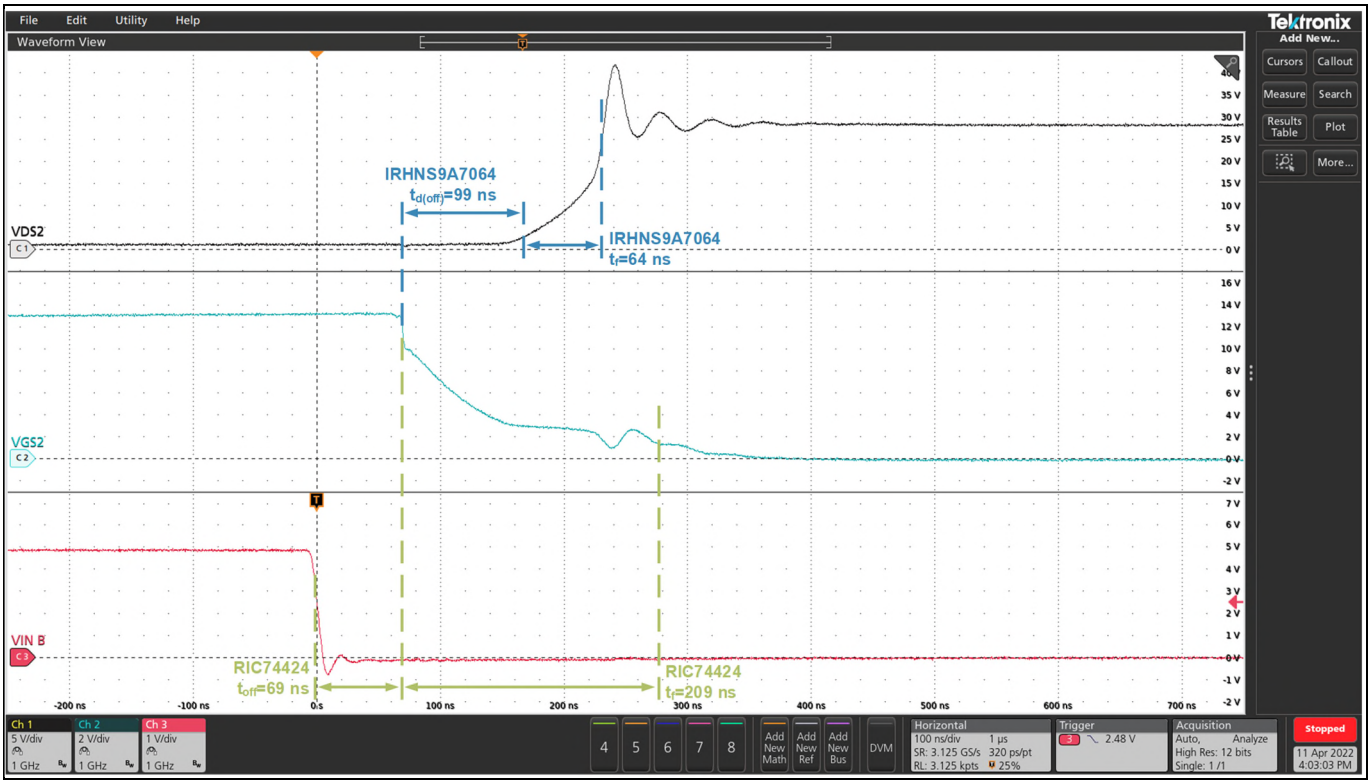


Figure 12 V_{DS2} (C1, black), V_{GS2} (C2, blue) and $V_{IN\,B}$ (C3, red) during turn off of Q_2

5 Schematic

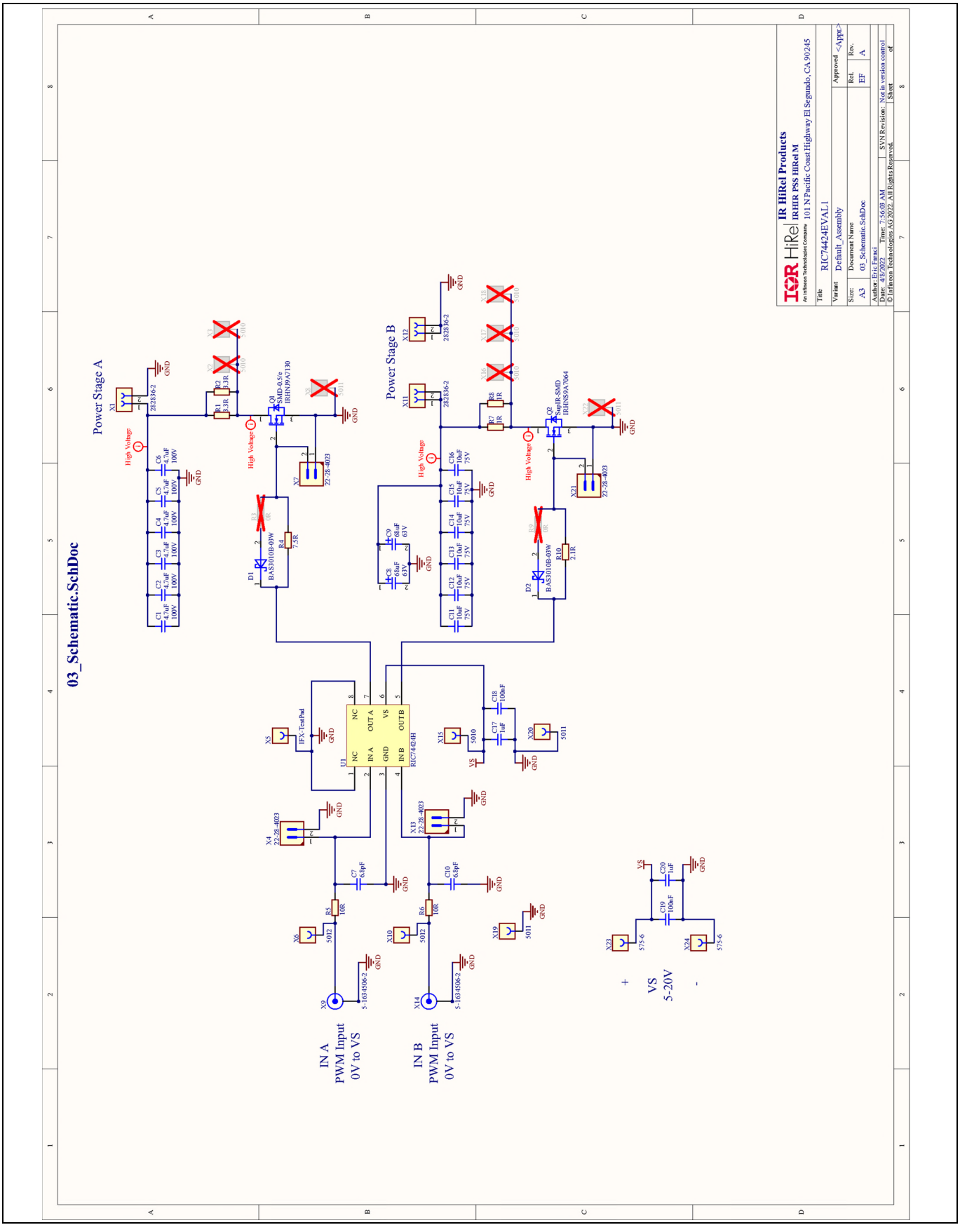


Figure 13 RIC74424EVAL1 schematic

6 PCB layout

RIC74424EVAL1 is a 62 mil thick, 2 layer PCB with 2 oz copper for top and bottom layer. All components are on the top layer. Altium design files and fabrication files are available on the RIC74424EVAL1 landing page.

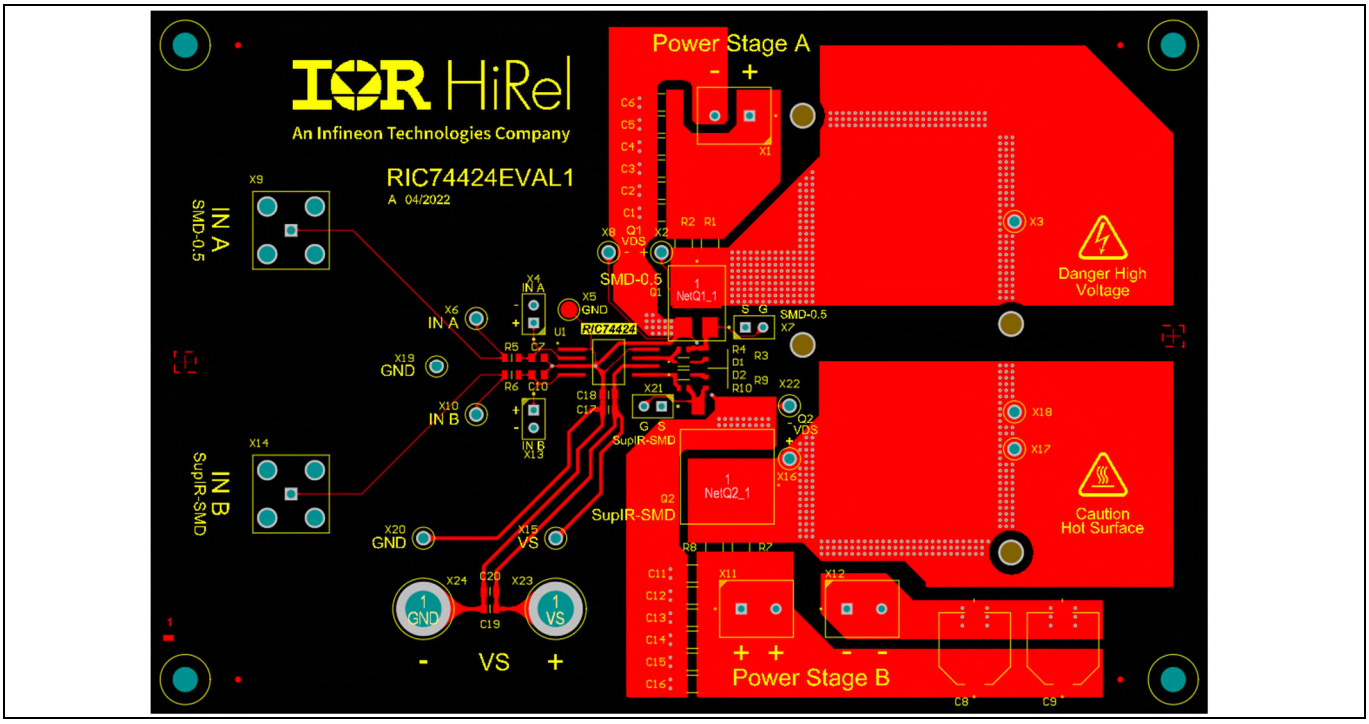


Figure 14 Top view of RIC74424EVAL1 top layer copper (red) and silkscreen (yellow)

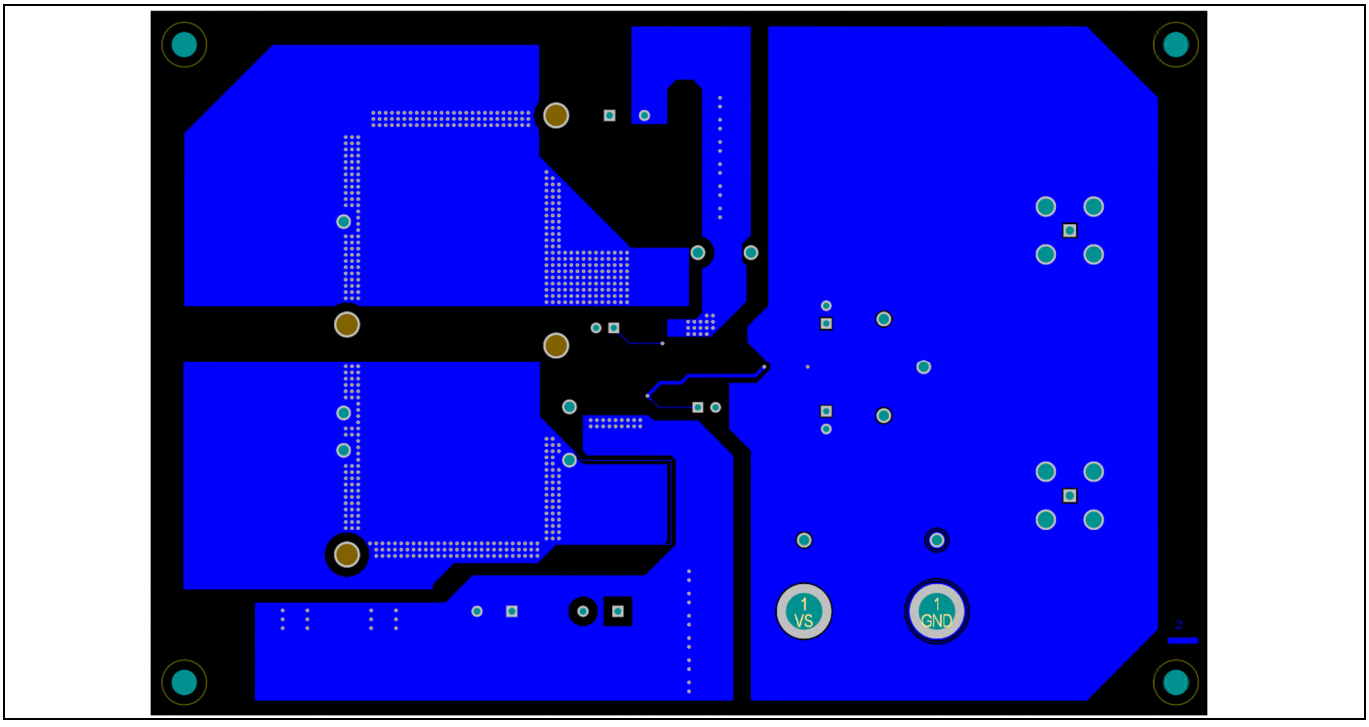


Figure 15 Bottom view of RIC74424FEVAL1 bottom layer copper (blue) and silkscreen (yellow)

7 Bill of materials

Components used on RIC74424EVAL1 are listed below. Alternatives with identical parameters may be used.

Table 8 Bill of materials

Quantity	Designator	Description	Manufacturer	Part number
6	C1, C2, C3, C4, C5, C6	CAP / CERA / 4.7uF / 100V / 10% / X7R (EIA) / -55°C to 125°C / 1210(3225) / SMD / -	TDK Corporation	CNA6P1X7R2A475K250AE
6	C11, C12, C13, C14, C15, C16	CAP / CERA / 10uF / 75V / 10% / X7R (EIA) / -55°C to 125°C / 1210(3225) / SMD / -	TDK Corporation	CGA6P1X7R1N106K250AC
2	C17, C20	CAP / CERA / 1uF / 50V / 10% / X7R (EIA) / -55°C to 125°C / 0805(2012) / SMD / -	MuRata	GRM21BR71H105KA12L
2	C18, C19	CAP / CERA / 100nF / 50V / 5% / X7R (EIA) / -55°C to 125°C / 0805(2012) / SMD / -	MuRata	GRM21BR71H104JA01
2	C7, C10	CAP / CERA / 6.8pF / 50V / 0.5% / C0G (EIA) / NP0 / -55°C to 125°C / 0805(2012) / SMD / -	Kemet	C0805C689D5GAC7800
2	C8, C9	CAP / ELCO / 68uF / 63V / 20% / - / -55°C to 125°C / 10.30mm L X 10.30mm W X 10.00mm H / SMD / -	Nichicon	PCR1J680MCL1GS
2	D1, D2	Medium Power AF Schottky Diode	Infineon Technologies	BAS3010B-03W
4	MP1, MP2, MP3, MP4	6-32, Binding Head Screw, Nylon 6/6	Keystone Electronics Corp.	9434
4	MP5, MP6, MP7, MP8	F-F Nylon Stand, 6-32 Thread Size	Keystone Electronics Corp.	1903C
1	Q1	Rad hard, 100V, 35A, single, N-channel MOSFET, R9 in a SMD-0.5 package	IR HiRel	IRHNJ9A7130
1	Q2	Rad hard, 60V, 100A, single, N-Channel MOSFET, R9 in a SupIR-SMD package	IR HiRel	IRHNS9A7064
2	R1, R2	RES / STD / 3.3R / 500mW / 1% / 100ppm/K / -55°C to 155°C / 1210(3225) / SMD / -	Vishay	CRCW12103R30FK
1	R10	RES / STD / 2.1R / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW06032R10FK
1	R4	RES / STD / 7.5R / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW06037R50FK
2	R5, R6	RES / STD / 10R / 125mW / 1% / 100ppm/K / -55°C to 155°C / 0805(2012) / SMD / -	Vishay	CRCW080510R0FK
2	R7, R8	RES / STD / 1R / 500mW / 1% / 100ppm/K / -55°C to 155°C / 1210(3225) / SMD / -	Vishay	CRCW12101R00FK

Bill of materials

Quantity	Designator	Description	Manufacturer	Part number
1	U1	Radiation Hardened Non-Inverting Dual Output MOSFET Drivers	IR HiRel	RIC74424H
3	X1, X11, X12	Terminal Block PCB Mount, 2 Pin	TE Connectivity	282836-2
1	X15	PC Test Point-Multipurpose THT, Red	Keystone Electronics Corp.	5010
2	X19, X20	PC Test Point-Multipurpose THT, Black	Keystone Electronics Corp.	5011
2	X23, X24	Banana Jack Connector	Keystone Electronics Corp.	575-6
4	X4, X7, X13, X21	2.54mm Pitch KK header, Breakaway, Vertical, 2 Circuits, 0.38um Gold Selective Plating	Molex	22-28-4023
2	X6, X10	PC Test Point-Multipurpose THT, White	Keystone Electronics Corp.	5012
2	X9, X14	BNC Straight PCB Socket	TE Connectivity	5-1634506-2

Revision history

Document version	Date of release	Description of changes
Rev A	4/26/2022	Initial release

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