RIC70115EVAL1 user guide

Half-bridge RIC70115 gate drivers with 100 V IG1NT052N10R GaN transistors evaluation board

About this document

Scope and purpose

RIC70115EVAL1 is an evaluation board for RIC70115, a radiation-hardened (RH), single-channel, high- or low-side gate driver with optimized features to control gallium nitride (GaN) High Electron Mobility Transistor (HEMT) such as RH 100 V IG1NT052N10R.

This user guide includes overview, setup instructions, test results, schematic, printed circuit board layout (PCB) drawings, and bill of materials (BOM).

Intended audience

This document is intended for engineers who are familiar with GaN power transistor-based converters, inverters, and gate drivers in aerospace systems looking to evaluate and design Infineon's RIC70115 or IG1NT052N10R into their application.

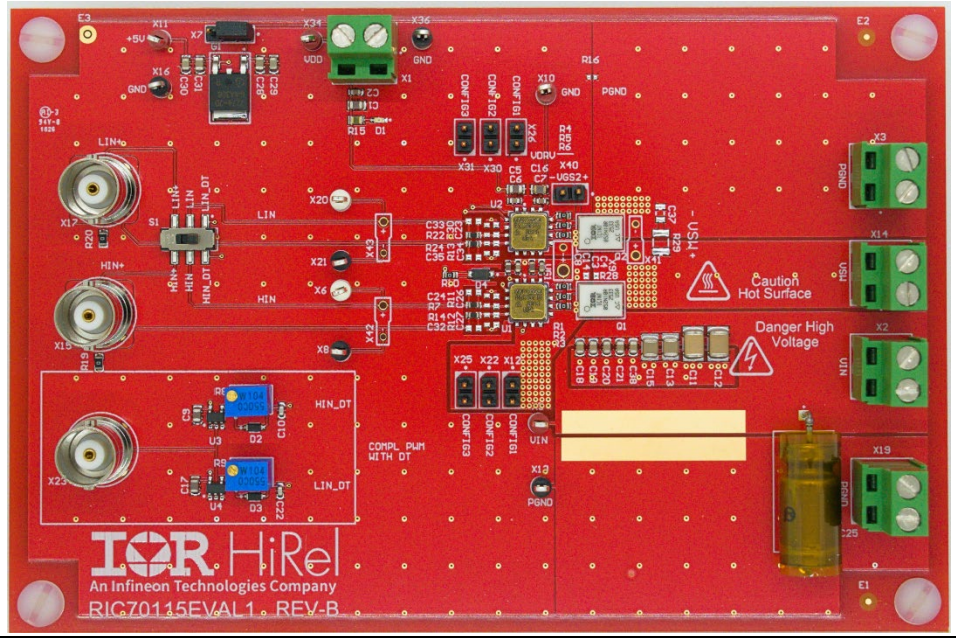

Figure 1 RIC70115EVAL1

Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

Warning: *RIC70115EVAL1 has a large amount of bulk capacitance across V_{IN} connector on board. If high voltages are applied to V_{IN} . Please make sure to follow all safety precautions and ensure that the bulk capacitor voltage is fully discharged before handling.*

Table of contents

1 Introduction

RIC70115EVAL1 is an evaluation board for RIC70115, a radiation hardened (RH) gate driver with optimized features to control GaN HEMTs, such as IG1NT052N10R.

This evaluation board is designed to help evaluate RIC70115 as a high-side and low-side gate driver for GaN HEMTs.

RIC70115 has the following features:

- Implements truly differential input (TDI) to withstand potential common-mode voltage on the input pins and enable support for high-side operation
- An internal LDO to maintain a drive voltage of 4.8 V over a wide bias supply range
- A high gate drive current and low propagation delay to support fast-switching speeds of GaN HEMTs
- A Miller clamp to protect the sensitive gate electrode of GaN HEMTs from high Miller currents

RIC70115 comes in an industry-standard 16-pin ceramic LCC package. Logic on the board supports either one or two external PWM inputs. IG1NT052N10R is a 100 V RH GaN HEMT with a low maximum Rds(on) of 6 mΩ in the PowIR-SMD package.

RIC70115EVAL1 comes populated with two RIC70115 gate driver ICs and two IG1NT052N10R GaN HEMT in an open-loop, half-bridge configuration to support switch-mode topologies like buck, boost or any single-ended and double-ended converter topologies. This evaluation board requires either two PWM input signals to control both gate drivers, or one PWM input signal if the onboard deadtime generation circuit is utilized.

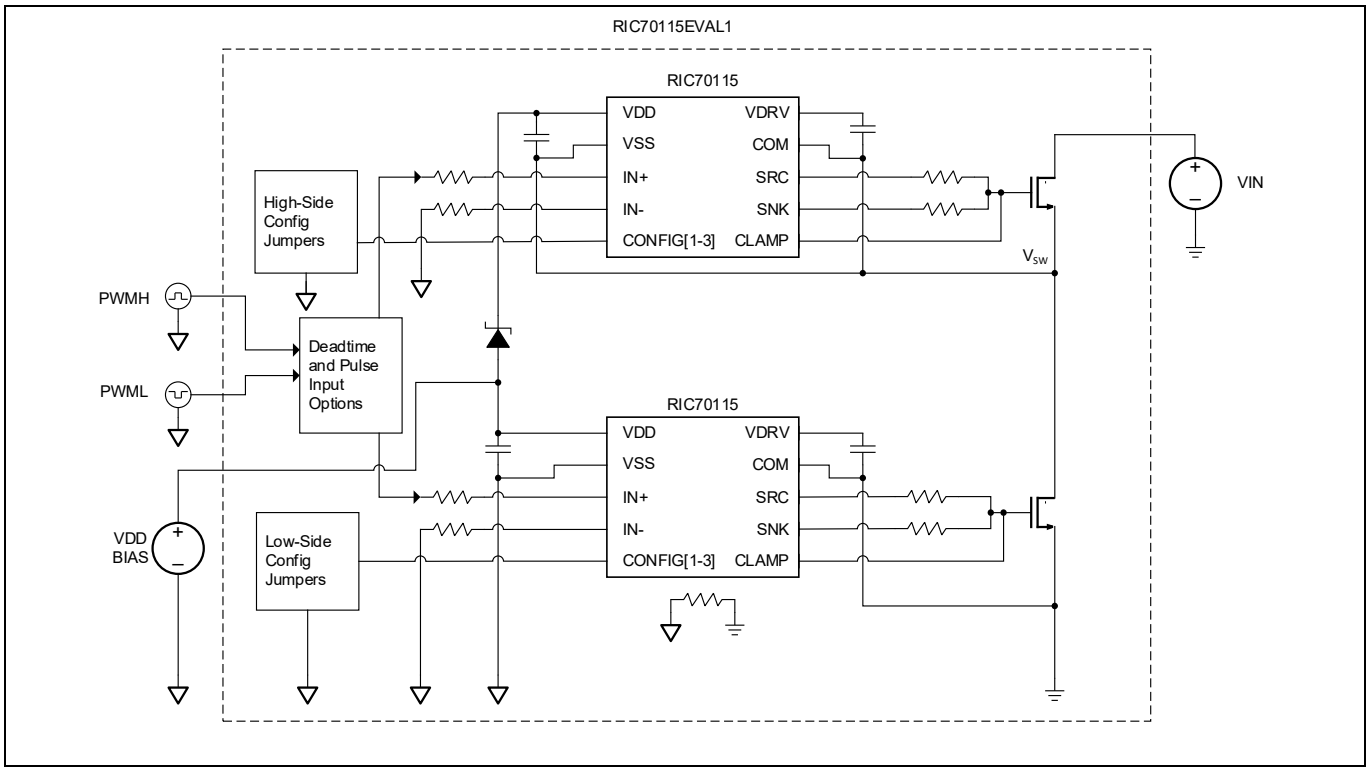

Figure 2 Simplified schematic of RIC70115EVAL1 at default

1.1 Features

- Half-bridge power stage populated with two RIC70115 gate driver ICs and two IG1NT052N10R SG GaN transistors
- Onboard tunable deadtime generation network for 5 V TTL signals
- Flexible open-loop power stage configurable for a variety of operating conditions
- PCB layout optimized to support efficient, high-speed switching GaN transistor operation
- Resistors in series with SRC, SNK, and CLAMP pins to configure drive strength of RIC70115 and showcase the performance of the Miller clamp within RIC70115

1.2 Recommended Operating Conditions

For optimal operation, the device should be used within the recommended operating conditions. All voltage parameters are absolute voltages referenced to V_{SS} unless otherwise stated.

Table 2 RIC70115EVAL1 recommended operating conditions

Symbol	Definition	Min	Typ	Max	Units
VDD	VDD bias voltage to COM	–	–	15	V
	VDD bias voltage to VSS	5	–	13.2	V
VCC	Bias power for dead time generation circuit	5	–	5.5	V
VDRV	Drive voltage	4.75	–	5.0	V
COM	Logic supply offset voltage	–3	–	0	V
VIN	Power stage input voltage	0	–	80	V
VPWM_IN	Logic input voltage	3.3		5	V

2 Functional Description

Figure 16 in Section 5 contains a schematic of RIC70115EVAL1 to reference for all components mentioned in the following subsections.

2.1 Bias Power

For proper operation, an external bias power supply is required for V_{DD}. V_{DD} provides the bias power to the low-side gate driver and through a bootstrap bias circuit to the high-side gate driver.

V_{CC} is the bias supply, dependent on V_{DD}, for the single-input deadtime generation circuit (see Section 2.2.1 for more information on this sub circuit). V_{CC} and V_{DD} can be biased at the same or different voltage; however, V_{CC} must be between 5 V to 5.5 V. Follow Table 3 below to connect or separate V_{DD} and V_{CC}.

Table 3 Bias power supply jumper settings

Bias power configuration	X7 pin 1 to 2 (V_{DD} to LDO)	X7 pin 2 to 3 (VDD to VCC)
$V_{CC} = V_{DD}$	Open	Short
$V_{CC} \neq V_{DD}$	Short	Open

2.2 Logic Inputs

To support truly differential input (TDI) offered by RIC70115, several precise input resistors (±0.1 % tolerance) are connected to the two command signal inputs (IN+ and IN-) of each RIC70115. The input logic of each IC reads the differential voltage between its IN+ and IN- pins. Each IC has four high-precision resistors (R7 and R14 for U1 and R22 and R24 for U2) oriented in a symmetrical pattern at the inputs.

In addition, copper is cut out around the input resistors to prevent any electromagnetic interference into these pins. In low-side operation, TDI logic between IN+ and IN- of U2 improves the immunity to any common-mode noise like ground bounce. TDI logic enables U1 to become a high-side gate driver by allowing the high-side IC to float up with power stage voltages. RIC70115EVAL1 uses 47 kΩ TDI resistors, which support 3.3 V input logic voltage assuming a maximum DC bus voltage of 150V at VSS for a typical FPGA sinking around 3mA. These resistors can be modified to accommodate 5 V input logic operation (see Table 4).

Table 4 Input resistor configurations for U1 and U2

Logic voltage (V)	$R_{in+}=R_{in-}$
3.3	47 kΩ
5.0	75 kΩ

2.2.1 Configure PWM Input Setting

RIC70115EVAL1 can be configured so that the user can use one or two external PWM input to drive both HS and LS gate drivers. To select the desired configuration, the S1 DPDT switch must be configured according to Table 5. If one external PWM is used, the S1 switch position should be moved to the right and if two external PWM are desired, it should be moved to the left.

Table 5 Logic input supply jumper settings

External PWM inputs	S1 position
1	Right
2	Left

2.2.2 One External PWM Input Configuration – DT generator circuit

To support a single external PWM input through X23, an optional complementary 5 V PWM signal with tunable deadtime (DT) is generated via an onboard sub circuit through an AND logic gate (U3) and an inverter (U4) with associated RC circuitry. R8 and R9 are 1 kΩ trim pots and C10 and C22 are 330 pF capacitors. Both components together will define the delay on the PWN signals. The DT is defined as the time interval where both GaN HEMT are turned off and it will depend mainly on the RC time constants at each PWM input, but it will also depend on the IN+/IN- logic thresholds, propagation delay, blanking time, driver strength of the driver and gate charge of the FETs. **Always verify that there is sufficient deadtime between the gate drive signals output by U1 and U2 to avoid any cross conduction in the half bridge.** Figure 3 and Figure 4 show the DT for three different R8 and R9 configurations in an open loop configuration. (HIN-VSS) and (LIN-VSS) waveforms are the PWM input pulses while LS_GATE and HS_GATE waveforms are the driver pulses.

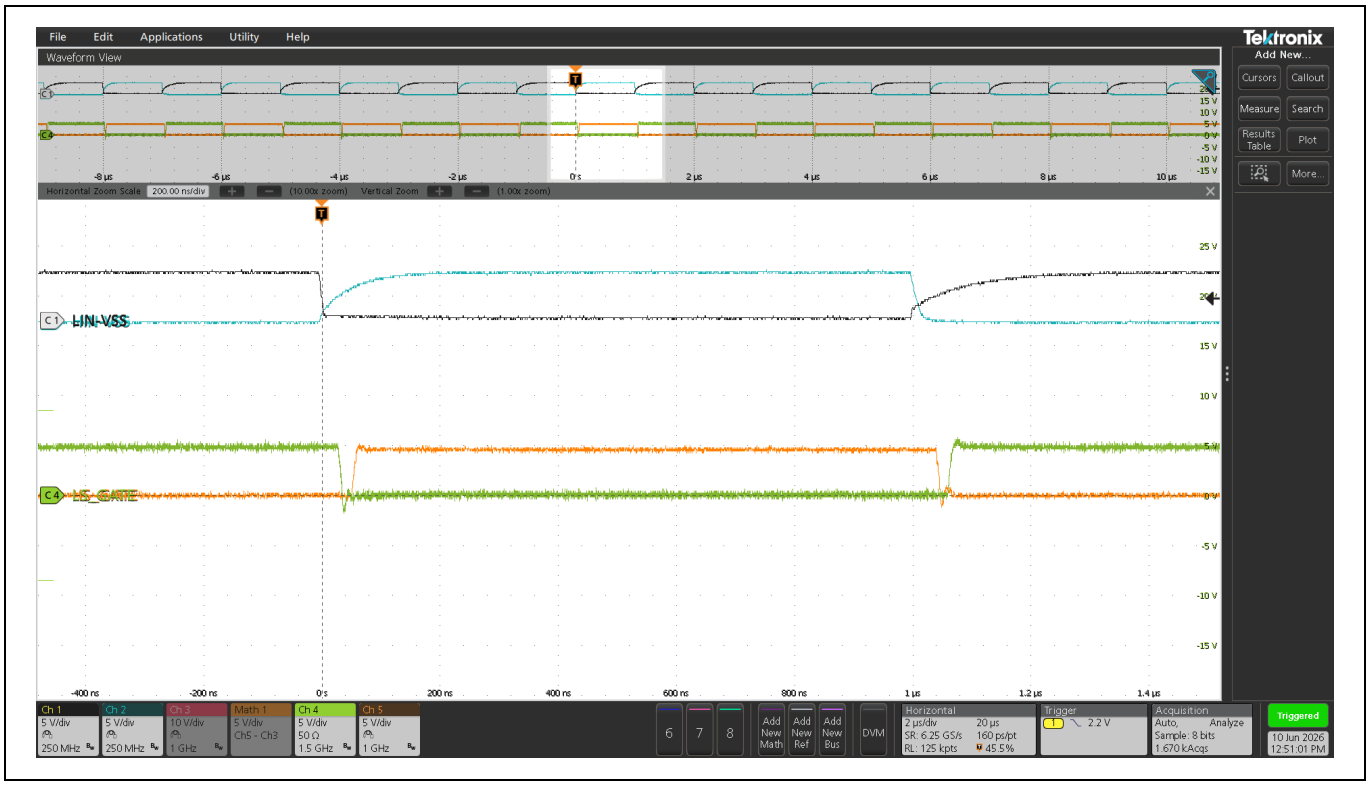

Figure 3 Deadtime between Q1 and Q2 using R8=100Ω and R9=200Ω

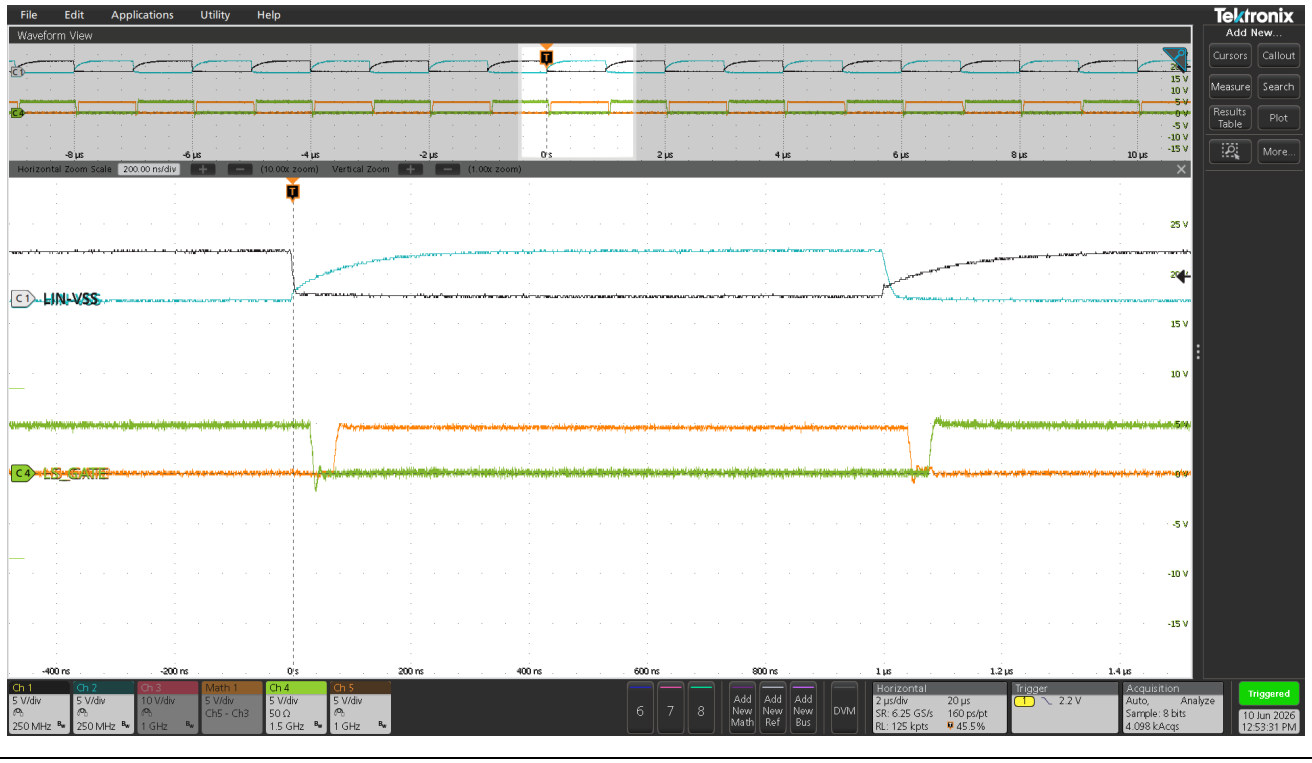

Figure 4 Deadtime between Q1 and Q2 using R8=200Ω and R9=300Ω

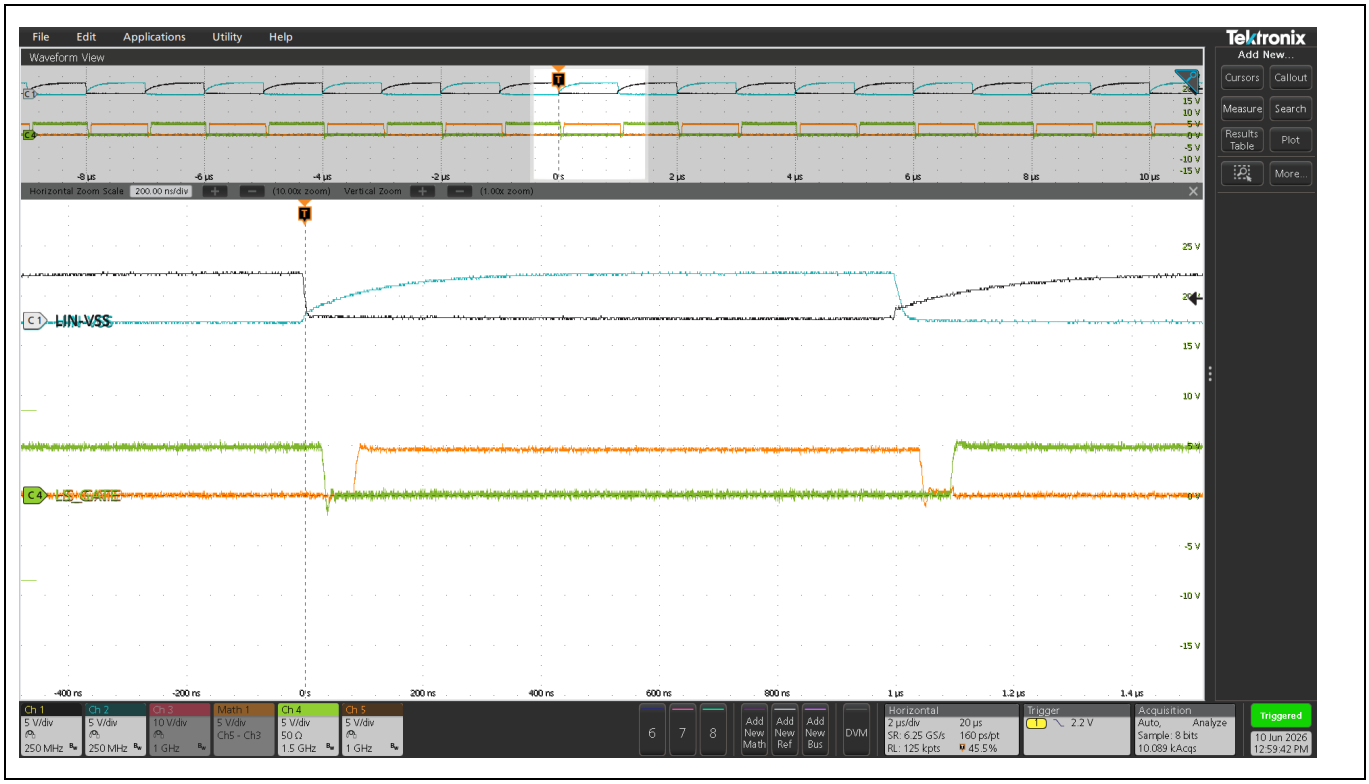

Figure 5 Deadtime between Q1 and Q2 using R8=300Ω and R9=400 Ω

Attention: The deadtime generation circuit for the single PWM input supports 5 V input logic. If a V_{DD} greater than 5 V is required, configure X7 to have V_{DD} (pin 2 of X7) connected to the LDO input (pin 3 of X7).

2.2.3 Two External PWM Inputs

When two independent PWM input settings are used, it is critical that there is sufficient deadtime between the logic HIN and logic LIN for both inputs to prevent Q1 and Q2 cross-conduction.

2.2.4 Blanking Time

To help prevent spurious switching during common-mode transient events, RIC70115 features a programmable input blanking time. According to Table 6, each IC will only respond to input signals that maintain a pulse width exceeding the minimum blanking time requirement. Any manifesting noise that has a pulse width below the configured blanking time will be ignored by the corresponding RIC70115. As a result, the propagation delay will also increase if a larger amount of blanking time is required. See Section 4.2 for a demonstration on the utility of different blanking times.

Attention: Each RIC70115 device (U1 and U2) supports multiple blanking time options independent of each other. Whenever a new blanking time setting is configured, ensure that the U1 and U2 gate drive waveforms have sufficient deadtime between them to prevent any cross-conduction across Q1 and Q2.

Table 6 Blanking time based on CONFIG pin schemes

CONFIG3 U1: X25 U2: X31	CONFIG2 U1: X22 U2: X30	CONFIG1 U1: X12 U2: X26	Blanking time typ. (ns)
Open	Open	Open	0
Open	Open	V_{SS}	20
Open	V_{SS}	Open	37
Open	V_{SS}	V_{SS}	58
V_{SS}	Open	Open	77
V_{SS}	Open	V_{SS}	97
V_{SS}	V_{SS}	Open	116
V_{SS}	V_{SS}	V_{SS}	135

2.3 Power Stage

RIC70115EVAL1 power stage is an open-loop half bridge, where the V_{IN} connector is connected to the drain of the high-side switch Q1, and switch-node (SW) is connected to the drain of the low-side switch Q2. It can be used in various power stages such as synchronous buck or boost amongst others. Placeholders for a snubber circuit (R29 and C37) have been included to reduce excessive voltage ringing at SW.

The recommended maximum V_{IN} voltage of the power stage is 80 V. The capacitors connected at VIN-PGND are rate for 125 V or higher, the IG1NT052N10R RH GaN HEMTs are rated for 100 V and RIC70115 is designed to handle 150 V of common mode voltage. If a VIN voltage higher than 80 V is required, the user needs to be aware of the voltage rating of all these parameters. A 100µF hermetically sealed tantalum capacitor is incorporated into the V_{IN} capacitor bank to provide a large amount of RMS current in a small size, which allows RIC70115EVAL1 to operate in a wide range of operating conditions.

2.4 Test Points

To simplify the measurement and improve the accuracy, several test points are provided. For power stage and gate loop waveform measurements, it is recommended that V_{IN}, V_{SW}, Q1 V_{GS}, and Q2 V_{GS} voltages are measured from the corresponding test point (see Table 7) to limit the impact of cable and connector losses on the measurement. For high-side (Q1) gate to source measurement (Q1 V_{GS}), two voltage probes referenced to PGND should be used: Q1 V_G and V_{SW}. Then, a math function in the oscilloscope should subtract both to obtain Q1 V_{GS} waveform.

Equation 1 High-side gate voltage measurement when the voltages are measured with respect to ground

Table 7 Test points

Net	Positive (+) test point	Negative (-) test point
V_{IN}	X5	X13
V_{SW}	X41 pin 1	X41 pin 2
Q1 V_G	X9 pin 1	X9 pin 2
Q2 V_{GS}	X40 pin 1	X40 pin 2
PWM_{HIN}	X42 pin 1	X42 pin 2
PWM_{LIN}	X43 pin 1	X43 pin 2
V_{DD}	X34	X36

2.4.1 Waveform Measurements

For most measurements, a passive probe can be used to measure the voltage waveforms of both Q1 and Q2, if they have suitable bandwidth and connectivity. The recommended minimum bandwidth for all voltage probes and oscilloscopes is 1 GHz. For Q2 V_{GS}, a high-bandwidth active differential probe like the TDP1500 is highly recommended to capture the fast gate drive transients.

The loop between the probe tip, measurement points, and GND connection should not exceed 10 mm, preferably shorter. Several measurement points that require enhanced measurement fidelity (V_{SW}, Q1 V_G, Q2 V_{GS}, PWM_{HIN} and PWM_{LIN}) have test points that support a “spring clip,” tip and barrel probe tip solution.

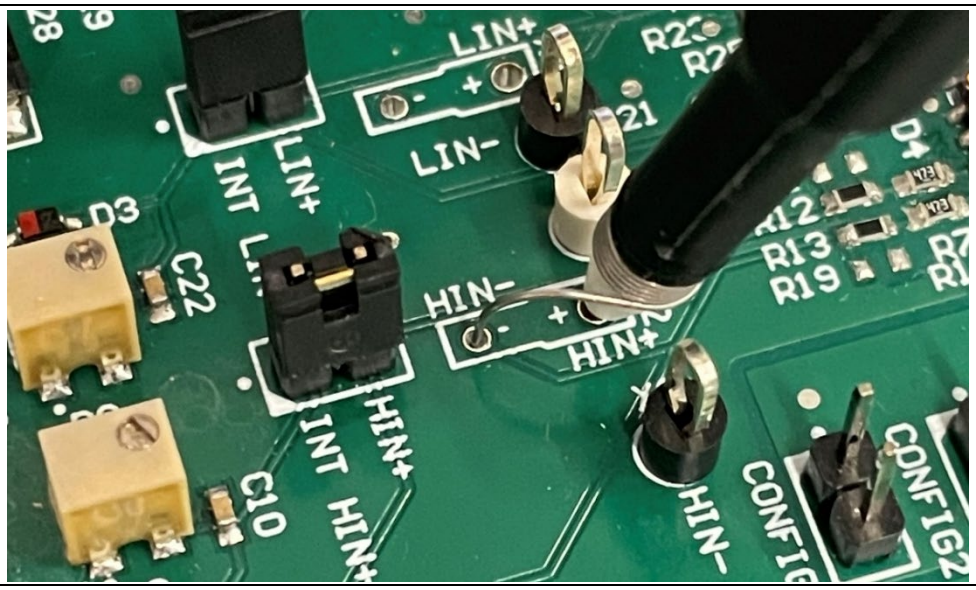

Figure 6 Low-inductance spring-clip passive probe

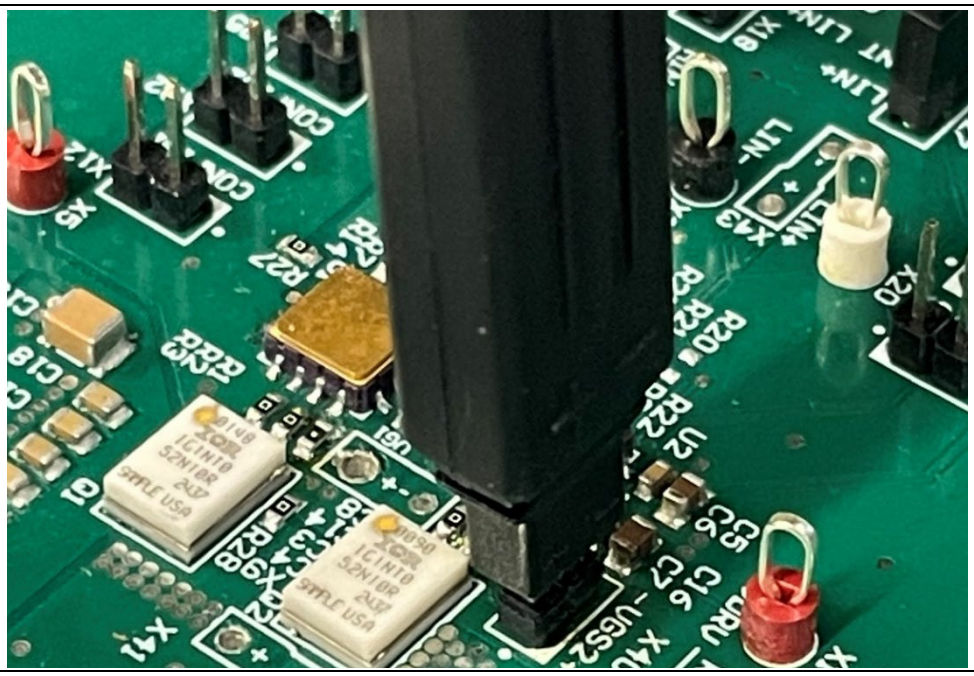

Figure 7 High-bandwidth active probes like TDP1500 for high-speed U2 gate drive measurement

2.5 Split Ground Support

Two different grounds exist on the board, V_{SS} and GND, as shown in the circuit schematic. Both grounds are connected through the internal Kelvin connection of the low side GaN HEMT IG1NT052N10R. This connection assures that both grounds have the same potential while preventing noise coupling from the power ground to the primary control ground. As an option, a placeholder for a 0 Ω resistor R16 is available if the user wants another connection point.

3 Recommended operation

3.1 Equipment

The following equipment are recommended to operate RIC70115EVAL1 over the full range of conditions:

- 5 V to 12 V VDD bias supply capable of at least 25 mA for the VDD connector
- VIN power supply up to 80 V capable of enough output current for the power level of the planned test
- Signal generator to provide PWM input for LIN+/LIN- and HIN+/HIN- which can support voltages from 0 V to 5 V
- Oscilloscope and probes for measurement with a 1GHz bandwidth recommended to capture high slew rate and high-frequency ringing
- Multimeters capable to measure VIN, Vout, Iin and Iout if a power stage is used.

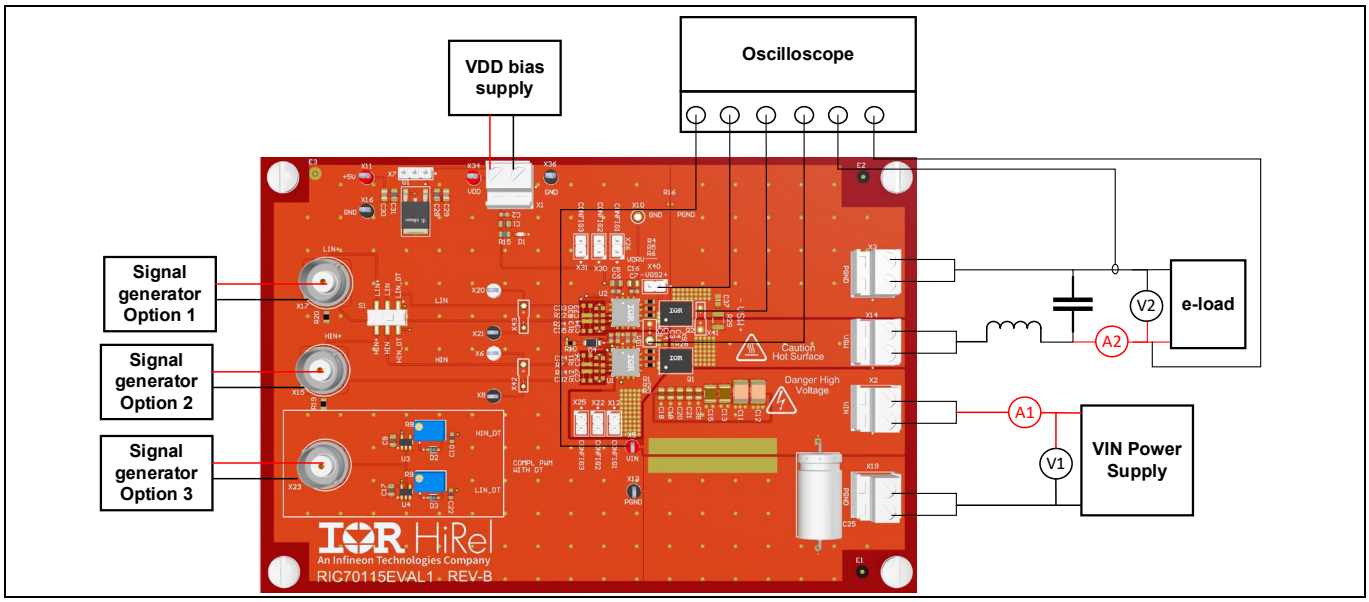

Figure 8 Recommended setup of RIC70115EVAL1

3.2 Powering up RIC70115EVAL1

1. Verify that PWM input jumpers are set for the required configuration per Table 5
2. Connect VDD bias supply, VIN power supply, power stage load (if used), PWM input, oscilloscope measurement probes and multimeters
3. Enable the VDD supply
4. Enable the PWM inputs
5. Verify that sufficient deadtime is maintained between outputs of U1 and U2 to help prevent cross-conduction of Q1 and Q2
6. Enable the power stage load (if used)
7. Enable the VIN supply

3.3 Powering down RIC70115EVAL1

1. Disable the VIN supply
2. Disable the power stage load (if used)
3. Disable the PWM
4. Disable the VDD supply
5. Measure VIN to ensure that the voltage on bulk capacitors is fully discharged
6. Remove the VDD bias supply, VIN power supply, power stage load (if used), PWM input, and measurement probes

4 Test results

All measurements were made with a common ground reference.

4.1 No-load

This section shows test results in a no-load configuration. The input to the device bias is V_{DD} = 5 V, PWM_{LIN} and PWM_{HIN} are 0 V to 5 V magnitude, 500 kHz, 50 % duty cycle square waves and V_{IN}=5 V.

Simplified schematic of RIC70115EVAL1 configured in no-load

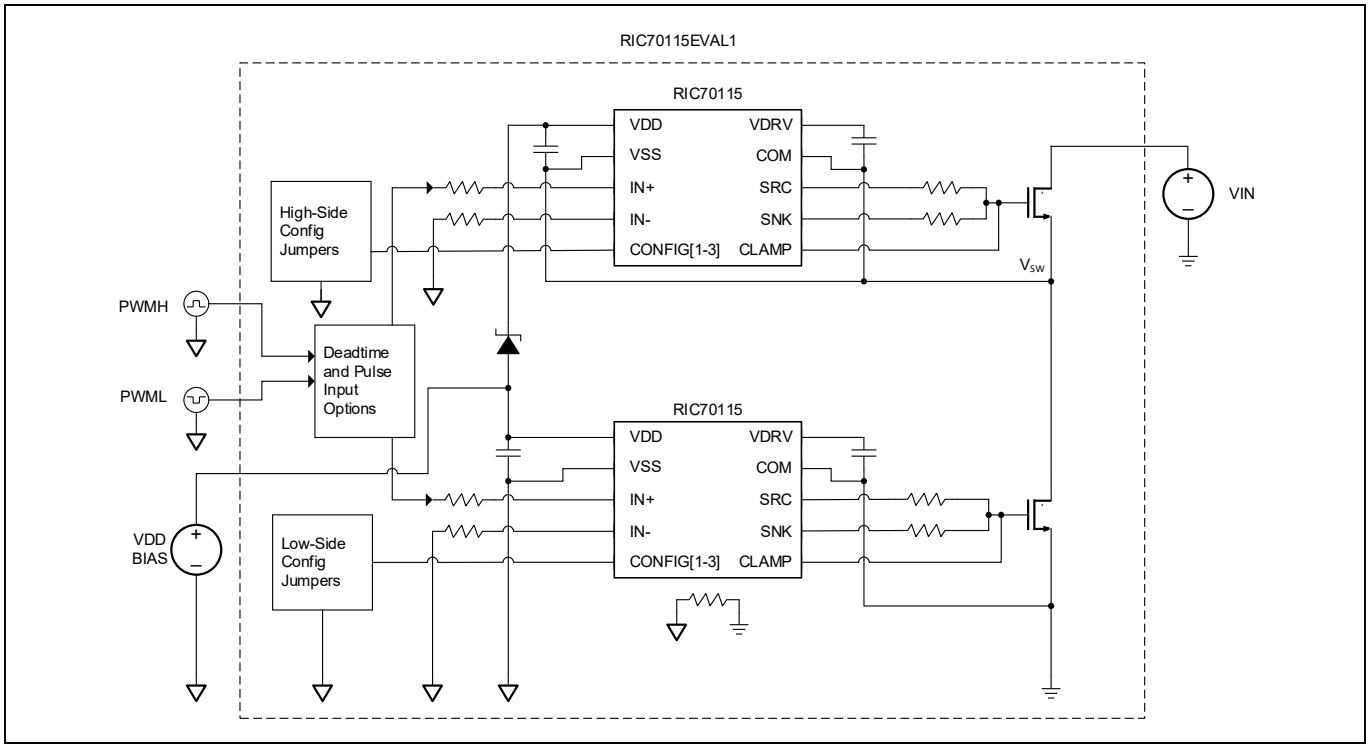

Figure 9 Simplified schematic of RIC70115EVAL1 configured in no-load

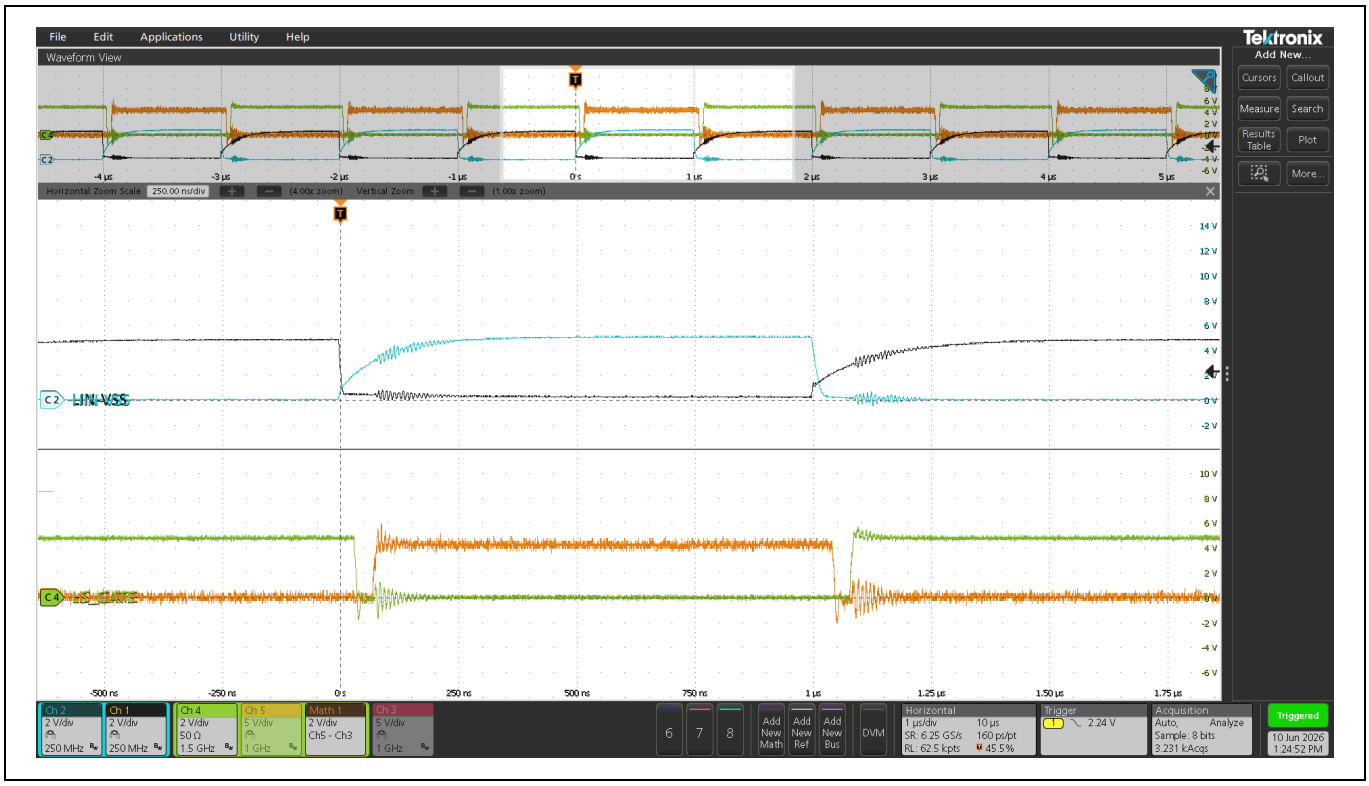

Figure 10 PWM_{HIN}, PWM_{LIN}, Q1 V_{GS} and Q2 V_{GS} with V_{IN} = 5 V and 0ns blanking time set on both U1 and U2

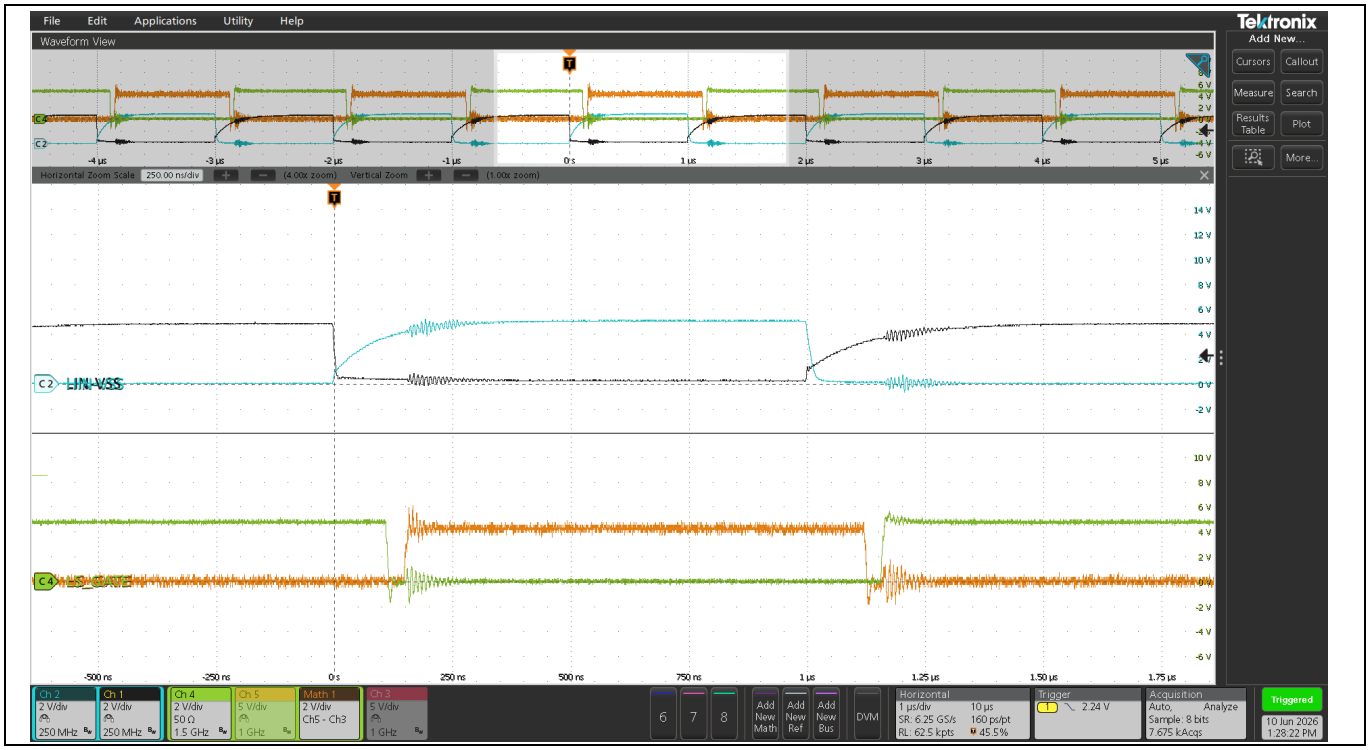

Figure 11 PWM_{HIN}, PWM_{LIN}, Q1 V_{GS} and Q2 V_{GS} with V_{IN} = 5 V and 77ns blanking time set on both U1 and U2

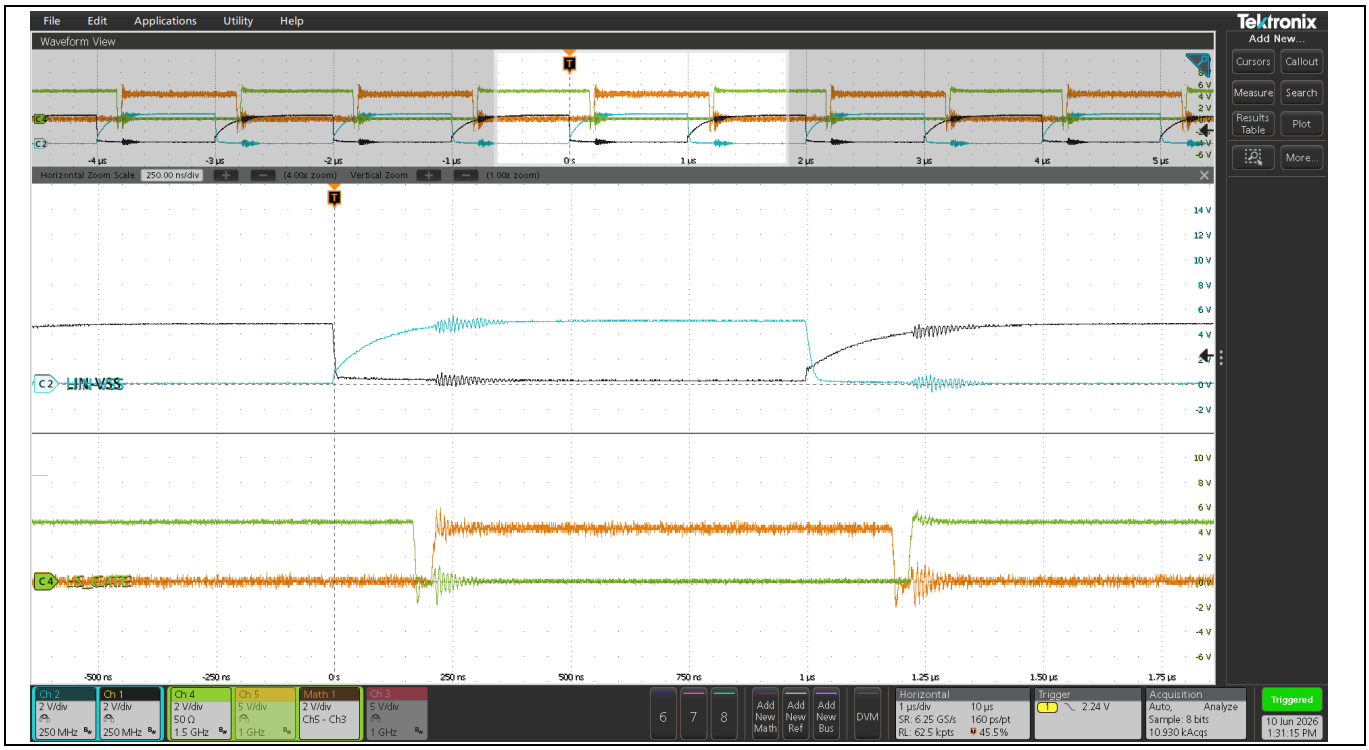

Figure 12 PWM_{HIN}, PWM_{LIN}, Q1 V_{GS} and Q2 V_{GS} with V_{IN} = 5 V and 135ns blanking time set on both U1 and U2

4.2 Synchronous buck converter

This section shows the test results of a synchronous buck converter with V_{IN} = 12 V DC, L_{OUT} = 6.8 µH using one high-current inductor SER2915H-682, C_{OUT} = 100 µF for the output capacitance, and an electronic load are connected to V_{SW}. An RC snubber based of a 10nF ceramic capacitor and a 1.6Ω resistor was utilized across the SW node to absorb the high-frequency oscillations. An additional input capacitance of 136uF based of two 68uF tantalum capacitors were added to reduce the V_{IN} ripple at high loads. At the same time an additional 50nF based of five 10nF ceramic capacitors were used to reduce the high-frequency ripple from V_{IN}. The device input bias is V_{DD} = 5 V and PWM_{IN} is a 0 V to 5 V magnitude, 500 kHz, and 42% duty cycle square wave fed into the deadtime circuit to create complementary input signals for U1 and U2. For both U1 and U2, a minimum amount of blanking time was used.

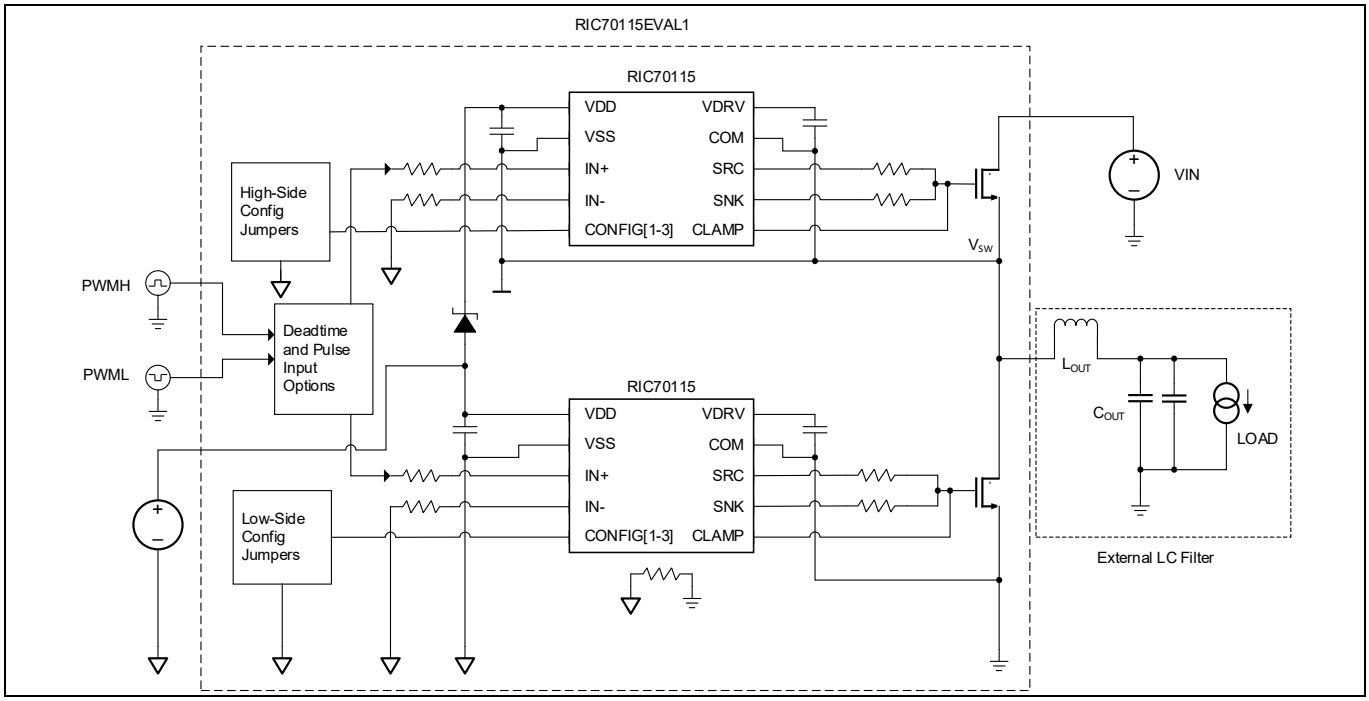

Figure 13 Simplified schematic of RIC70115EVAL1 configured to support a 12 V, 500 kHz, synchronous buck converter

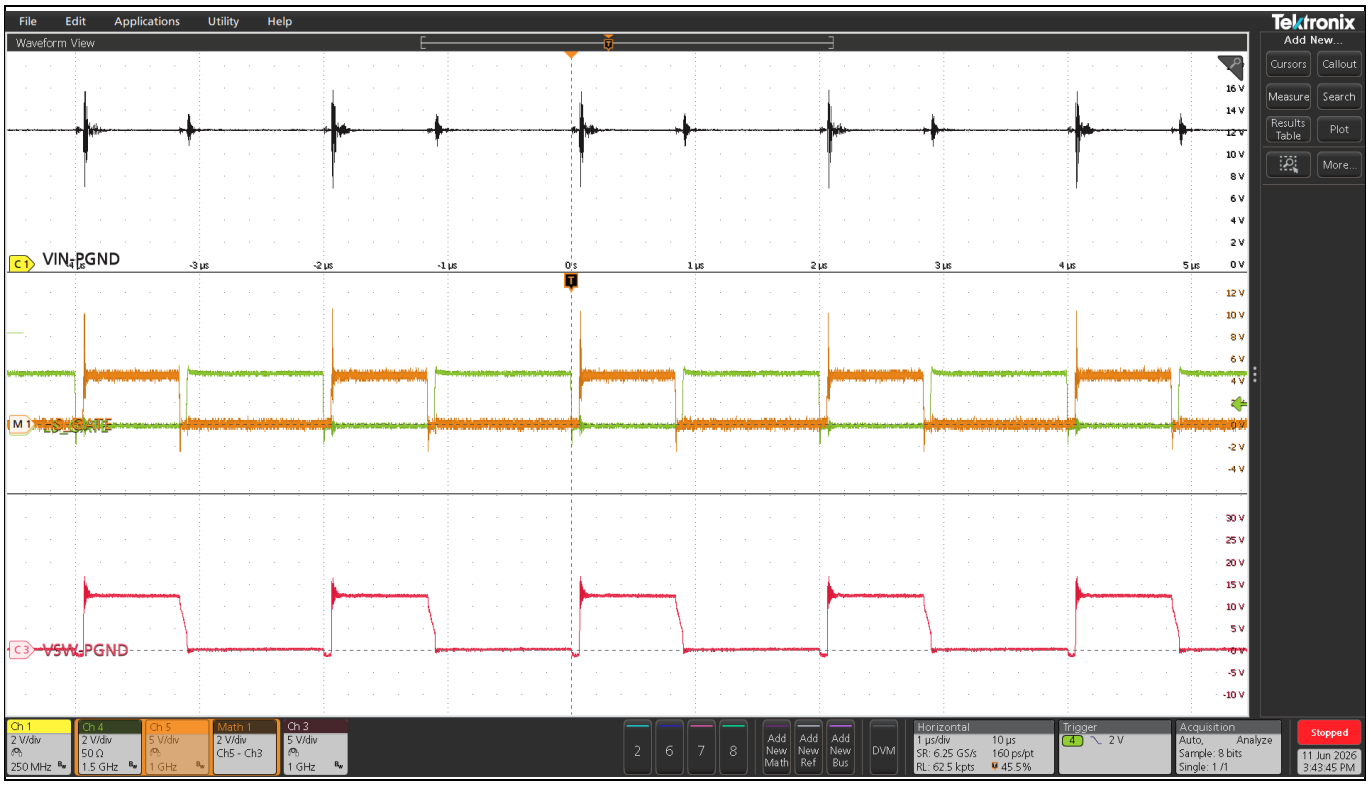

Figure 14 V_{IN} = 5 V, V_{SW} and I_{OUT} = 1 A switching at 500 kHz

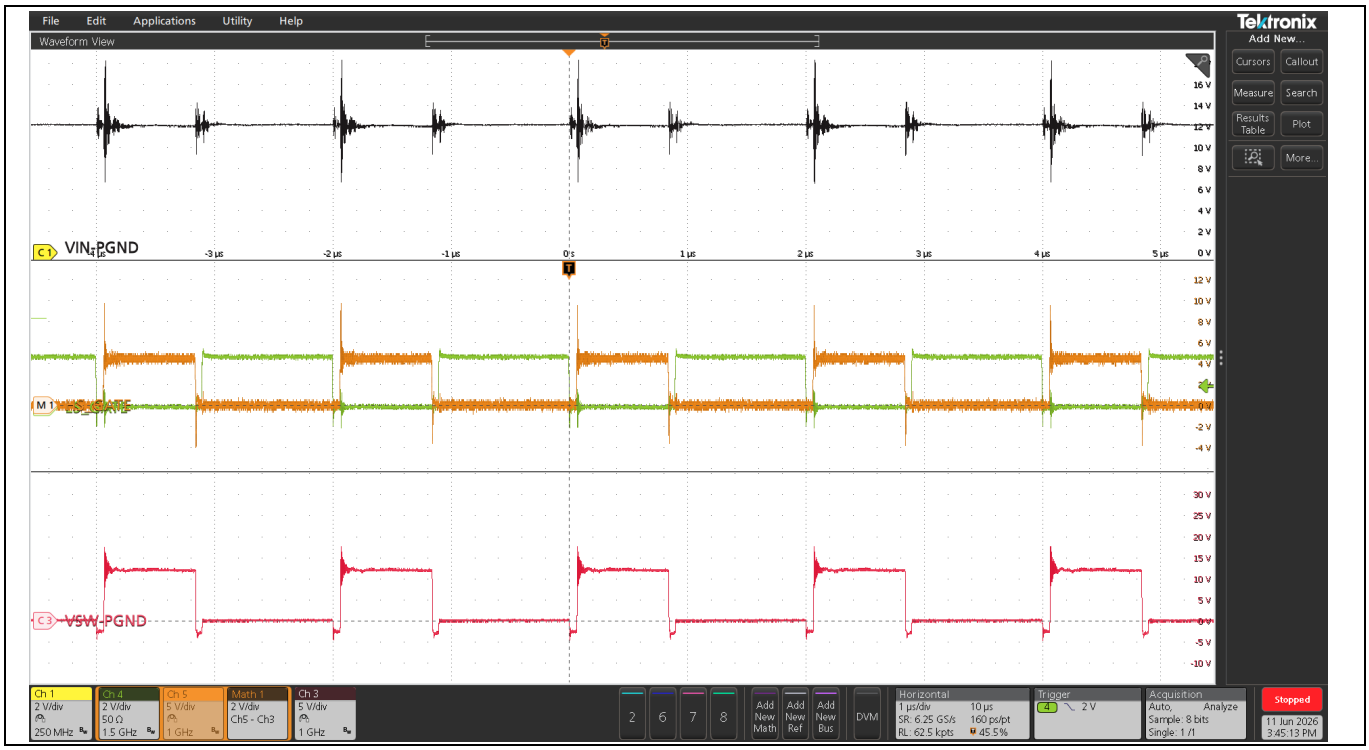

Figure 15 V_{IN} = 5 V, V_{SW} rising edge, and I_{OUT} = 10 A switching at 500 kHz

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5 Schematic

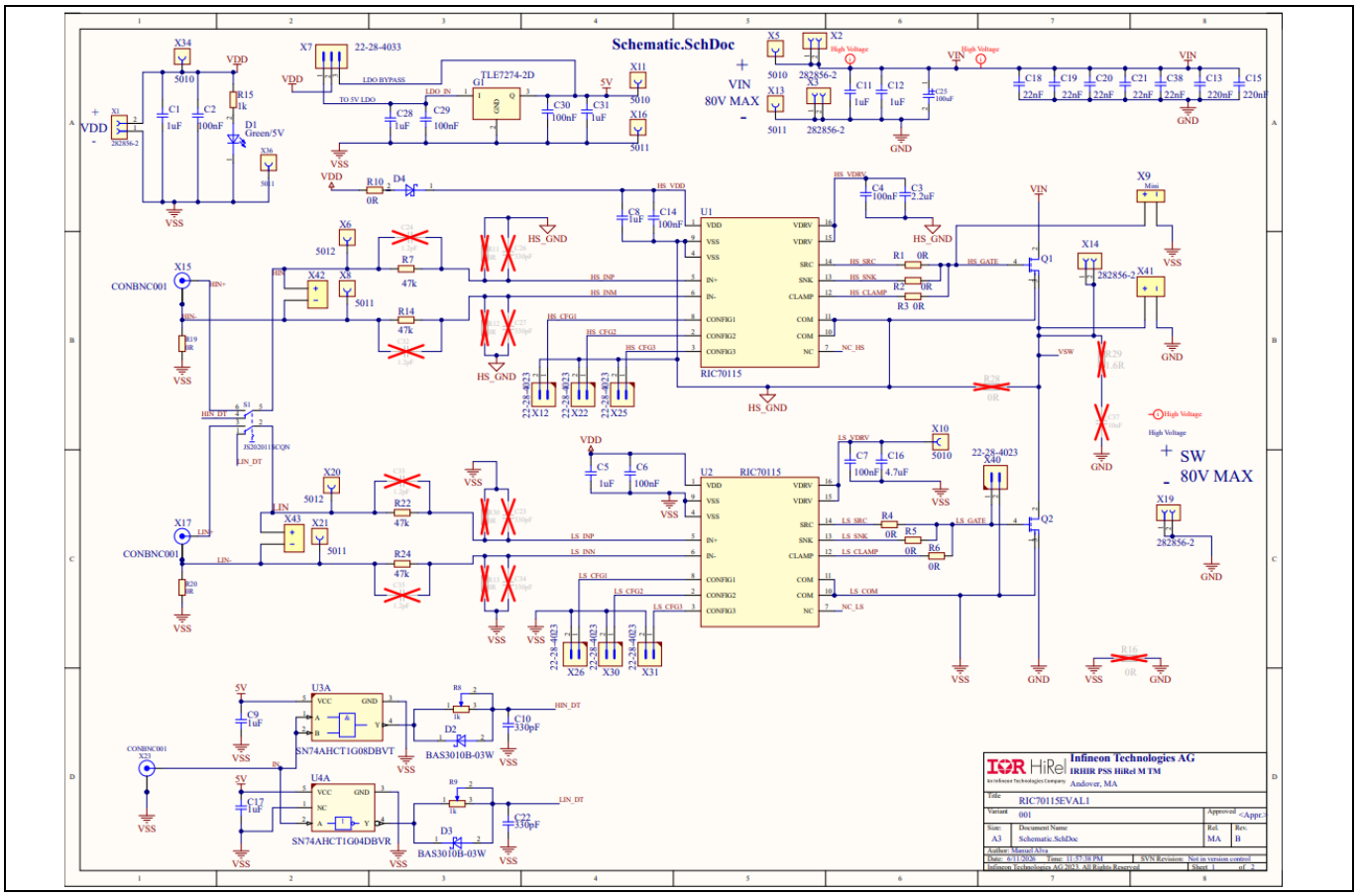

Figure 16 Schematic of RIC70115EVAL1

6 PCB Layout

RIC70115EVAL1 is a 62-mil thick, 4-layer PCB with 2-oz copper for the top, bottom and mid layers. All components are on the top layer.

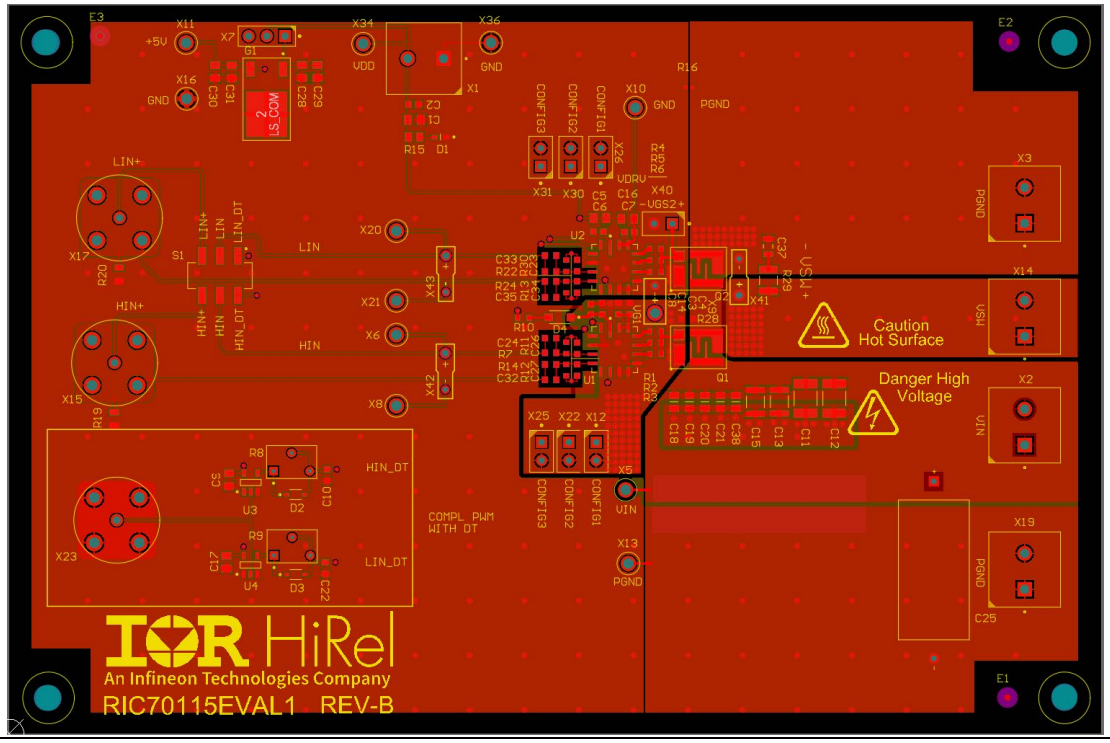

Figure 17 Top layer of RIC70115EVAL1

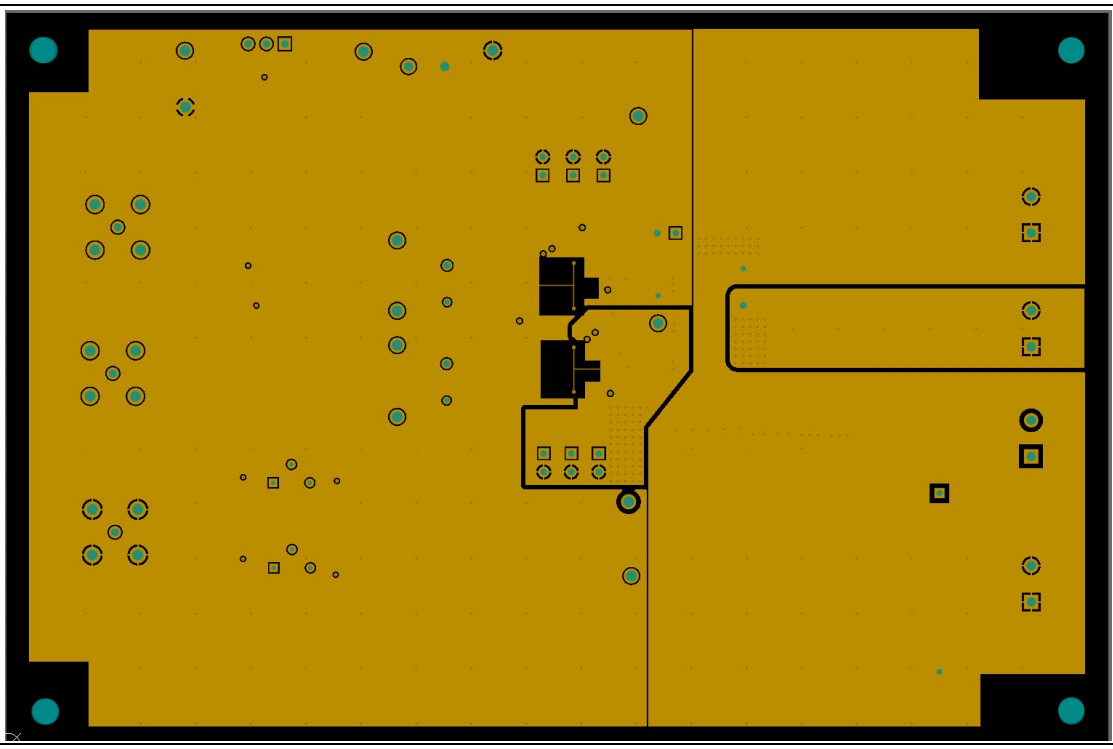

Figure 18 1st mid layer of RIC70115EVAL1

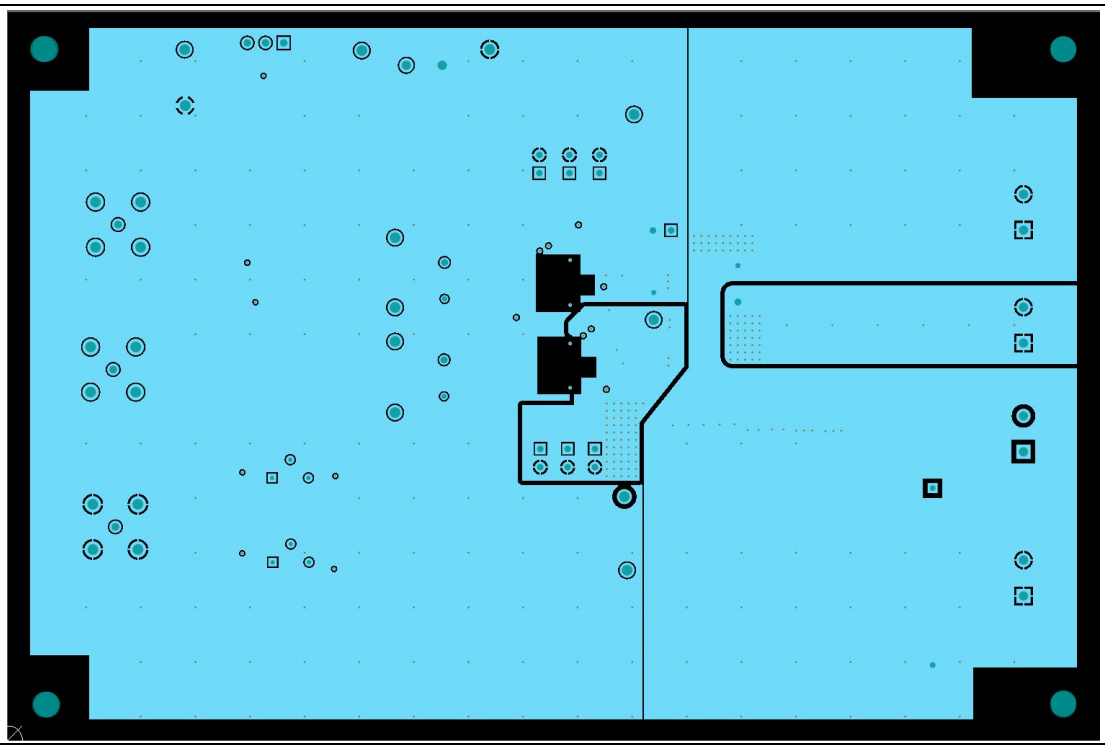

Figure 19 2nd mid layer of RIC70115EVAL1

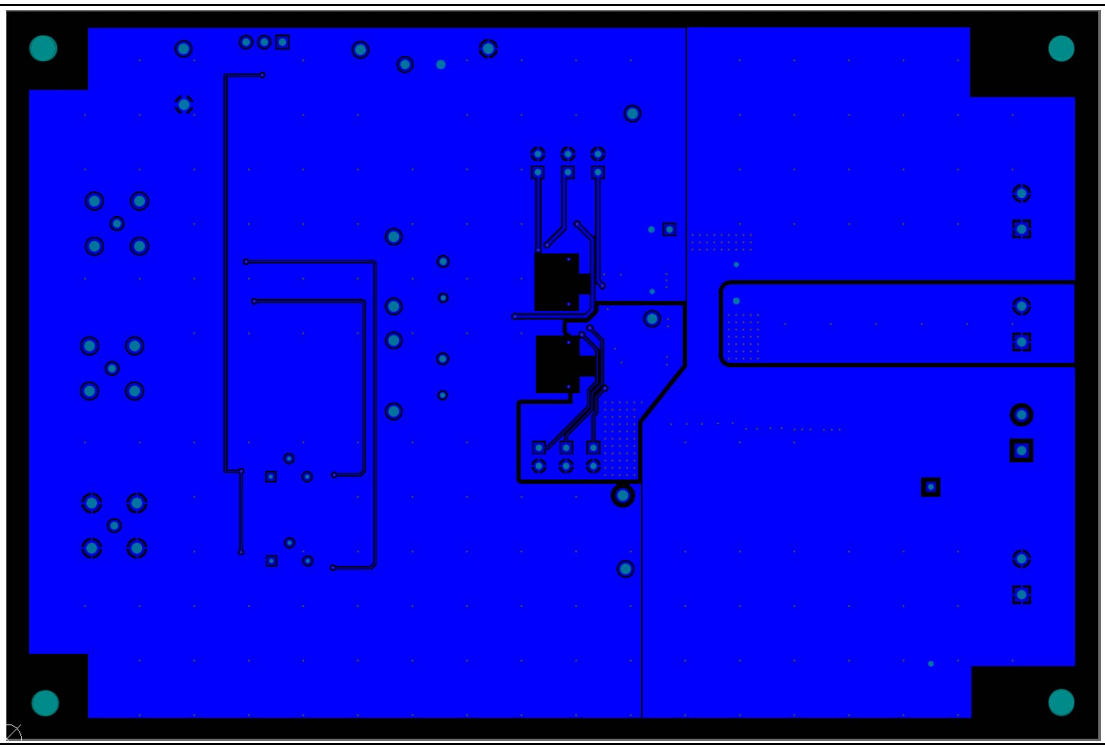

Figure 20 Bottom layer of RIC70115EVAL1

7 Bill of materials

Table 8 Bill of materials

Designator	Quantity	Manufacturer Part Number	Description	Manufacturer
C1, C5, C9, C17	4	CGA4J1X8L1H105K125AC	CAP / CERA / 1uF / 50V / 10% / X8L (EIA) / -55°C to 150°C / 0805(2012) / SMD / -	TDK Corporation
C2, C6, C7	3	C1608X8R1H104K080AB	CAP / CERA / 100nF / 50V / 10% / X8R (EIA) / -55°C to 150°C / 0603(1608) / SMD / -	TDK Corporation
C3	1	GRM188R61H225KE11	CAP / CERA / 2.2uF / 50V / 10% / X5R (EIA) / -55°C to 85°C / 0603(1608) / SMD / -	MuRata
C4, C14	2	GRM188R71H104JA93	CAP / CERA / 100nF / 50V / 5% / X7R (EIA) / -55°C to 125°C / 0603(1608) / SMD / -	MuRata
C8	1	CGA3E3X5R1H105K080AB	CAP / CERA / 1uF / 50V / 10% / X5R (EIA) / -55°C to 85°C / 0603(1608) / SMD / -	TDK Corporation
C10, C22	2	C0603C331J3GAC	CAP / CERA / 330pF / 25V / 5% / C0G (EIA) / NP0 / -55°C to 125°C / 0603(1608) / SMD / -	Kemet
C11, C12	2	18122C105JAT2A	CAP / CERA / 1uF / 200V / 5% / X7R (EIA) / -55°C to 125°C / 1812(4532) / SMD / -	Kyocera
C13, C15	2	GRM32DR72D224KW01	CAP / CERA / 220nF / 200V / 10% / X7R (EIA) / -55°C to 125°C / 1210(3225) / SMD / -	MuRata
C16	1	GRM21BC71H475KE11L	CAP / CERA / 4.7uF / 50V / 10% / X7S (EIA) / -55°C to 125°C / 0805(2012) / SMD / -	MuRata
C18, C19, C20, C21, C38	5	GRM21BR72D223KW03	CAP / CERA / 22nF / 200V / 10% / X7R (EIA) / -55°C to 125°C / 0805(2012) / SMD / -	MuRata
C25	1	134D107X9125T6	CAP / - / 100uF / 125V / 10% / - / -55C to 85C / THT/Radial / THT /	Vishay
C25 Alternative	0	173D107X9020YWE3	CAP TANT 100UF 10% 20V AXIAL	Vishay Sprague
C28, C31	2	08053C105K4Z2A	CAP / CERA / 1uF / 25V / 10% / X7R (EIA) / -55°C to 125°C / 0805 / SMD / -	AVX
C29, C30	2	C0805C104J5RAC	CAP / CERA / 100nF / 50V / 5% / X7R (EIA) / -55°C to 125°C / 0805(2012) / SMD / -	Kemet
D1	1	LTST-C191KGKT	SMD LED, Green, 576.5nm	LiteOn Optoelectronics
D2, D3	2	BAS3010B-03W	Medium Power AF Schottky Diode	Infineon Technologies

RIC70115EVAL1 user guide

Half-bridge RIC70115 gate drivers with 100 V IG1NT052N10R GaN transistors evaluation board

Bill of materials

Designator	Quantity	Manufacturer Part Number	Description	Manufacturer
D4	1	SS10200FL	High Voltage Surface Mount Schottky Barrier Diode	WON-TOP Electronics
G1	1	TLE7274-2D	5-V Low Dropout Voltage Regulator	Infineon Technologies
MP1, MP2, MP3, MP4	4	9434	6-32, Binding Head Screw, Nylon 6/6	Keystone Electronics Corp.
MP5, MP6, MP7, MP8	4	1903C	F-F Nylon Stand, 6-32 Thread Size	Keystone Electronics Corp.
Q1, Q2	2	IG1NT052N10R	Rad hard, 100 V, 52 A, GaN transistor in PowIR-SMD package – PowIR-SMD, 100 krad TID, COTS	Infineon Technologies
R1, R2, R3, R4, R5, R6, R10	7	AC0603JR-070RL	RES / STD / 0R / 100mW / 0R / 0ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Yageo
R7, R14, R22, R24	4	M55342K12B47B0PT0	RES / STD / 47k / 100mW / 0.1% / 100ppm/K / -65°C to 150°C / 0603(1608) / SMD / -	Vishay
R8, R9	2	3266Y-1-102LF	RES / Variable Resistor & Potentiometer / 1kR / 250mW / 10% / 100 ppm/K / -55C to 125C / THT / THT /	Bourns
R15	1	PCAN0805E1001BST5	RES / STD / 1k / 1W / 0.1% / 25ppm/K / -55°C to 155°C / 0805(2012) / SMD / -	Vishay
R19, R20	2	RC0805JR-070RL	RES / Resistor Chip / 0R / 125mW / R / 0 ppm/K / -55C to 155C / 0805 (2012) / SMD /	Yageo
S1	1	JS202011SCQN	Sub-Miniature Slide Switches, DPDT models, 300mA, 6V	C&K
U1, U2	2	RIC70115	Rad hard high and low side TDI gate driver for GaN SG HEMTs and Si FETs	Infineon Technologies
U3	1	SN74AHCT1G08DBVT	Single 2-Input Positive-AND Gate	Texas Instruments
U4	1	SN74AHCT1G04DBVR	Single Inverter Gate with Network Switches	Texas Instruments
X1, X2, X3, X14, X19	5	282856-2	Terminal Block, PCB Mount Side Entry Wire,	TE Connectivity
X5, X10, X11, X34	4	5010	PC Test Point-Multipurpose THT, Red	Keystone Electronics Corp.
X6, X20	2	5012	PC Test Point-Multipurpose THT, White	Keystone Electronics Corp.
X7	1	22-28-4033	2.54mm Pitch KK Header, Breakaway, Vertical, 3 Circuits, 0.38µm Gold Selective Plating, Mating Pin Length 6.09mm	Molex

Bill of materials

Designator	Quantity	Manufacturer Part Number	Description	Manufacturer
X8, X13, X16, X21, X36	5	5011	PC Test Point-Multipurpose THT, Black, TEST POINT, PC, MULTIPURPOSE, BLACK	Keystone Electronics Corp.
X12, X22, X25, X26, X30, X31, X40	7	22-28-4023	2.54mm Pitch KK header, Breakaway, Vertical, 2 Circuits, 0.38um Gold Selective Plating	Molex
X15, X17, X23	3	CONBNC001	BNC Jack PCB Through-Hole Connector	Linx Technologies

Revision history

Document revision	Date	Description of changes
Revision 1.0		Initial revision

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