CoolSiC™-based DC EV charger reference design and demonstration system

REF-EV50KW2SICKIT

About this document

Scope and purpose

This application note describes a virtual reference design for DC electric vehicle (EV) charging subunits with up to 50 kW using Infineon CoolSiC™ modules. The design combines a highly efficient and modular power conversion concept with the target to achieve a wide output voltage range, which is also capable of bi-directional operation.Only design files and internal test results are provided.

Intended audience

This document addresses technical specialists working on DC EV charging solutions and similar application fields. The concept of the reference design is modular, enabling any or all functional blocks and components of the pre-developed hardware and software to be re-used according to individual needs.

Reference design

The reference design described in this document provides a blueprint of how to combine a well-defined set of the latest Infineon products, e.g., CoolSiC™ MOSFETs, EiceDRIVER™ drivers, and AURIX™ microcontrollers, with all the passive components that are required to build a highly efficient 50 kW DC EV charger subunit. The deliverables are Altium project files for the main power conversion PCB which has the CoolSiC™ modules.

Document structure

The user guide is composed of 2 documents:

REF-EV50KW2SICKIT: The current and main document that contains the system description

REF-2LC50K6MRW2CD: Power conversion board description

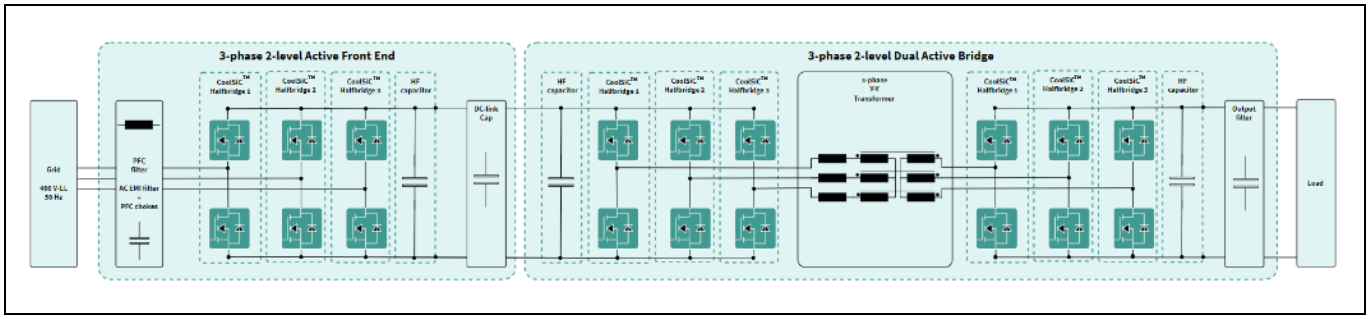


Figure 1 Block diagram of the 50 kW reference design

Please note: The design does not necessarily meet safety, EMI and quality standards (e.g., UL, CE) requirements.

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 **Safety precautions**

	**Warning:** *The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning***: The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the system, wait for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the system before you disconnect or reconnect wires or perform maintenance work. Wait after removing power to discharge the bus capacitors. Do not attempt to service the system until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with power electronics should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

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1 The reference design at a glance

1.1 Introduction: modular design approach

This application note describes a reference design for fast, DC electric vehicle (EV) charger subunits with up to 50 kW. The design combines a highly efficient and modular power conversion concept with a wide output voltage range, which is also capable of bi-directional operation.

This concept offers the flexibility to re-use any or all components of the proposed system blueprint for speeding up individual design activities:

- **Power topologies:** A broad range of modifications are possible by using the same power conversion board(s) and only changing the peripheral reactive components. For example, two-level AC/DC converters, non-isolated multi-phase buck converters, boost converters, resonant three-phase LLC or CLLC, and three-phase DAB or ZVS converters can be designed by adopting suitable filter or transformer configurations.
- **Thermal management:** The thermal approach can be adjusted to individual system-level requirements as for example forced air, liquid, or convection-type cooling, e.g., by replacing heat sinks with cold plates.

A demonstration system was assembled and tested at Infineon, which is the basis for the following specification and measurement results in this document.

1.2 Top-level specifications

Table 2 System specifications of the tested DC EV charger demonstration system

Parameter	Minimum	Typical	Maximum	Units
System-level operation				
Ambient temperature		25		°C
Peak efficiency		96		%
Cooling		Forced air		
Bi-directionality*		Grid to vehicle (G2V) and vehicle to grid (V2G)		
AC side (3-phase)				
Line frequency		50		Hz
Line voltage		400		V_{LL_rms}
Power factor @ 45 kW		0.99		
Current THD @ 45 kW	5.3		9.5	%
DC side (DAB output)				
Power**		45	50	kW
Output voltage***	350	570	750	V
Voltage ripple@ 570 V and 45 kW		17		V_{pk_pk}

* The hardware design is capable of bi-directional operation, but the demo software did not support grid synchronization for V2G mode

**Exceeding 45 kW was causing DC-link voltage to drop below the specified values

*** Tested voltage ranges are listed in the operation chart in Figure 34

1.3 Key design building blocks

The topology of the DC EV charger reference design and demonstration system described in this application note can be seen in Figures 2. It consists of two converters:

- 2-level, 3-phase, active front-end converter (AFE) for AC-DC conversion
- 3-phase, dual-active bridge (DAB) converter for DC-DC conversion

The 3-phase bridge in the AFE as well as the primary and the secondary side of the DAB, is realized using identical power conversion boards, following the modular approach described earlier.

The design is capable of transferring power in both directions. However, transferring power to the grid was not tested due to software limitations.

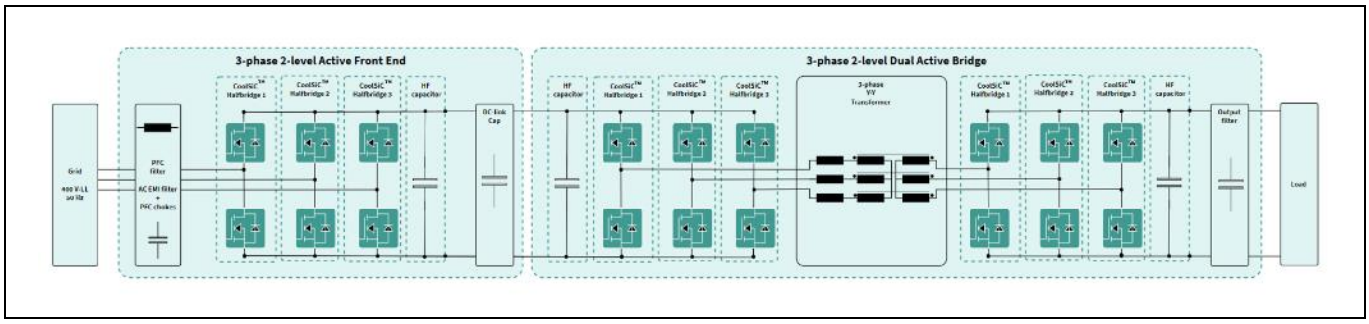


Figure 2 EV charger topology of choice

The complete DC EV charger demonstration system consists of the following key building blocks:

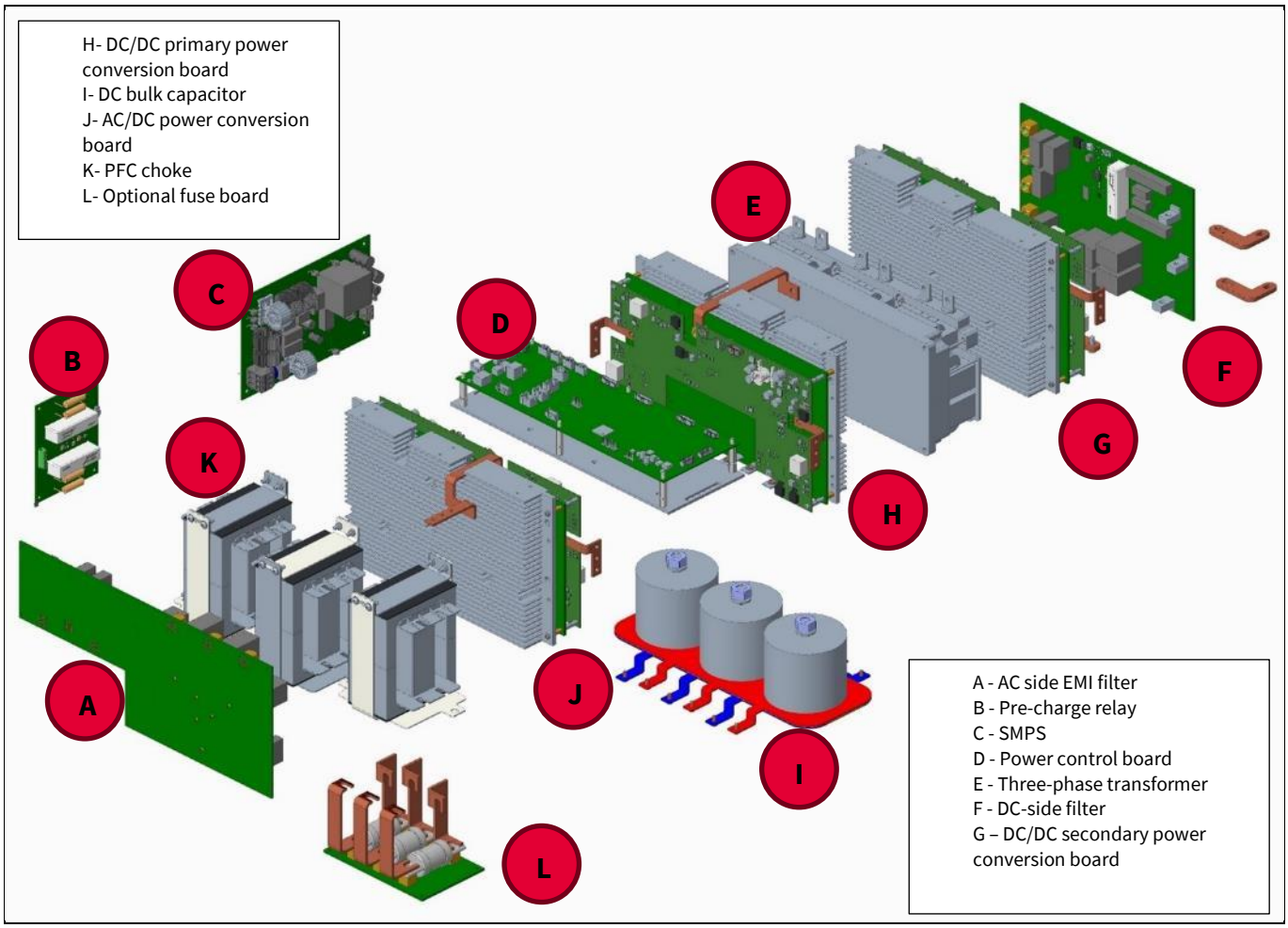


Figure 3 Key building blocks of the DC EV charger demonstration system

As shown in Figure 3, the AC-side EMI filter board (A) is connected to three-phase power lines through a three-phase contactor. The EMI filter board includes common-mode and differential filters. After EMI filtering, power is transmitted to the PFC inductors (K) and the AC/DC power conversion board (J), acting here as the active power factor correction unit.

Mounted on a laminated bus bar, the DC-link capacitor (I) connects the AC/DC and primary DC/DC (H) power conversion boards. A three-phase, high-frequency isolating transformer (E) connects the primary and secondary (G) DC-DC power conversion boards. Bus bars are used for connecting the secondary DC/DC power conversion board and the output filter (F). Also, a pre-charge board (B) is used to prevent inrush currents, and to charge the DC-link capacitor (I).

The power control board (D) communicates with all three power conversion boards as well as the input and output filter boards. A switch-mode power supply (SMPS) (C) is used to provide auxiliary 24 V DC.

1.4 Preferred Infineon products

To realize the demonstration system, three main semiconductor board types were used, carrying the following Infineon semiconductor products:

- power conversion boards with FF6MR12W2M1H_B11 Easy2B SiC modules
- a power control board with an AURIX™ TC377TP96F300S microcontroller
- an auxiliary power supply board (SMPS)

Along with these PCBs, passives, heatsinks and other mechanical components were used to realize the EV charger subunit demonstration system.

Design files for the power conversion board are provided, but not for any of the other mentioned PCBs and components.

1.5 Semiconductor boards used

1.5.1 Power conversion board

The power conversion board REF-2LC50K6MRW2CD uses CoolSiC™ MOSFET modules in a B6 configuration with the corresponding best-fit EiceDRIVER™ gate drivers on a “piggy-back” PCB. This purely analog, self-protected block provides a broad range of integrated temperature, current and voltage sensing for faster implementation, control and debugging.

The selected piggy-back configuration reduces the overall form factor and minimizes the parasitic inductance in the gate driver switching loop. It can be used for various topologies in AC/DC and DC/DC power conversion stages and is suitable for both air and liquid cooling.

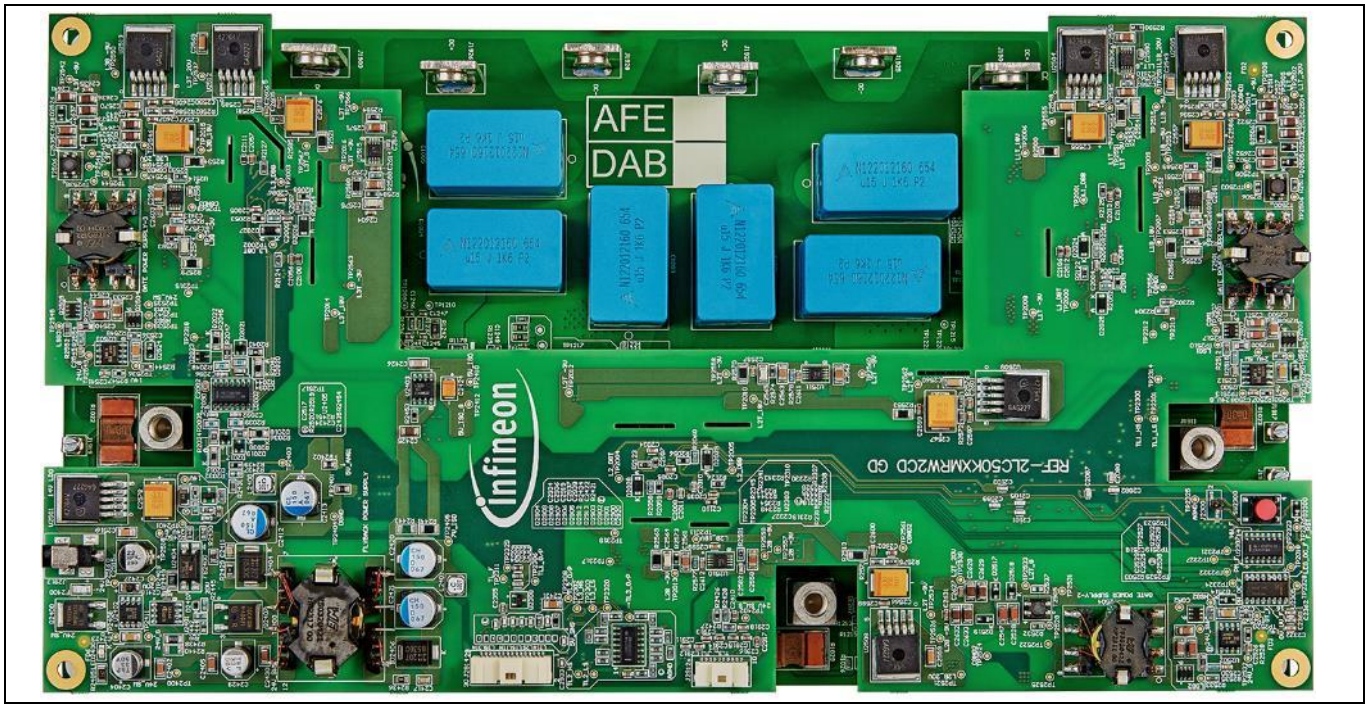


Figure 4 Power conversion board

For the 50 kW DC EV charger reference design, two types of topologies are implemented using these power conversion boards, requiring only a minor change of components:

- 2-level, active front-end converter (AFE) for AC/DC conversion
- 3-phase, dual-active bridge (DAB) converter for DC/DC conversion

The detailed specification and design information such as the block diagram and schematics for the power conversion board REF-2LC50K6MRW2CD are provided in a separate document.

1.5.2 Power control board

The power control board of the demonstration system was monitoring and controlling various parameters of the power conversion boards such as voltage, current, phase and temperature. These parameters were fed as differential analog signals to the power control board, which supports up to 46 differential ADC channels and 35 single-ended ADC channels.

Based on these inputs from the power conversion boards, the power control board was performing basic fault diagnostics, and drive LEDs to indicate the Fault/Status of the system and to generate PWM signals.

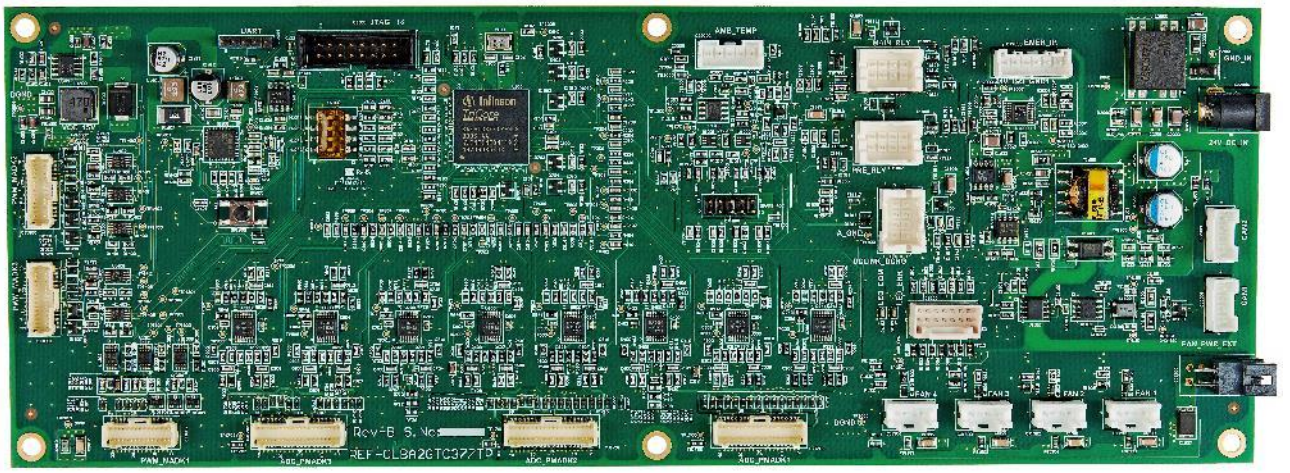


Figure 5 Mechanical layout of the used power control board

Differential ADC signals from three power conversion boards were converted into a single-ended system using a differential to single-ended line receiver. The signals were then sent to the ADC of the MCU AURIX™ TC377TP96F300S. To implement suitable shutdown mechanisms, the power controller was monitoring the analog signals from the NTC and the PCB sensors.

The power control board was supporting up to 28 PWM output channels. Low-side gate drivers were used to amplify the PWM signals generated from the MCU to 15 V to drive the gate drivers on the power conversion board.

Power conversion boards and the power control board were communicating via the CAN2.0B protocol. The user's PC and the power control board were interfaced by an external CAN-to-Ethernet converter.

The power control board was supporting an external shutdown-button input and control a maximum of four external fans. The board power supply section consisted of a 15 V buck switching regulator for the PWM, PMIC for the controller power supply, ADC power supply, as well as an isolated supply for the CAN section.

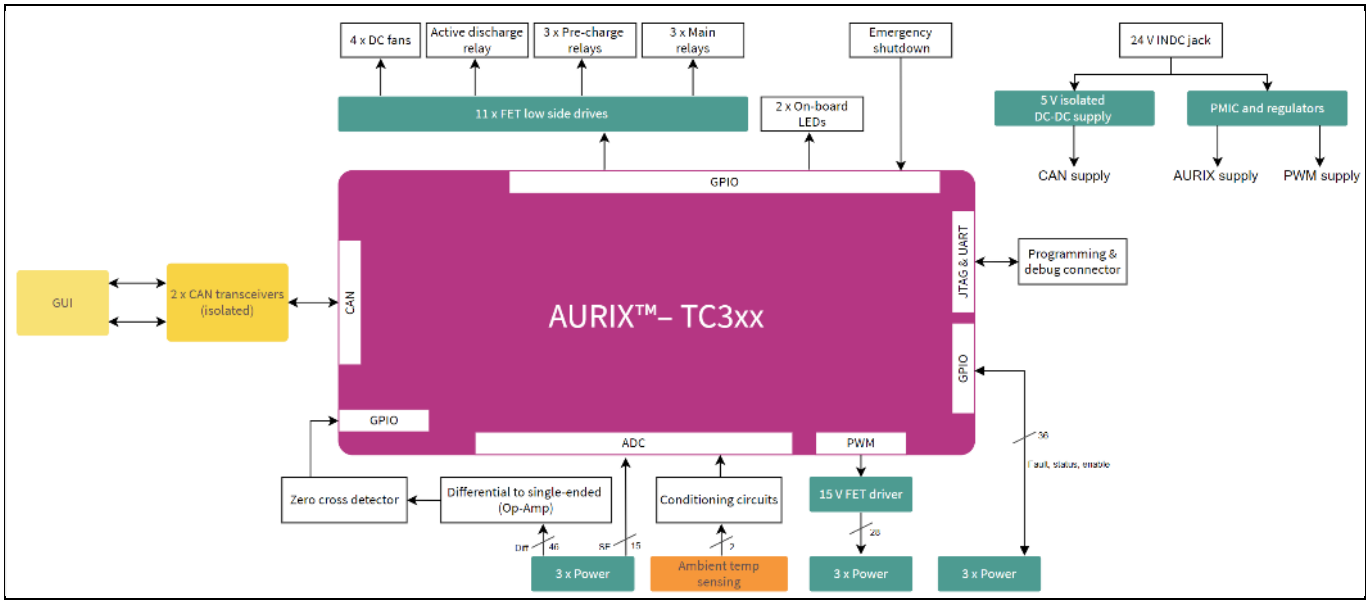


Figure 6 Block diagram of the power control board

1.5.3 Auxiliary power supply board (SMPS)

The SMPS board of the demonstration system was supplying 24 V DC power with up to 120 W to the power control board as well as to the power conversion boards. It was featuring a 1700 V CoolSiC™ MOSFET in a TO-263 7L surface-mounted device (SMD) package as the main switch, which is well-suited for high input voltage DC-links.

Thanks to its low $R_{ds(on)}$, the board achieved high efficiency and a low temperature rise of the device. The flyback controller was working in quasi-resonant mode to reduce EMI noise.

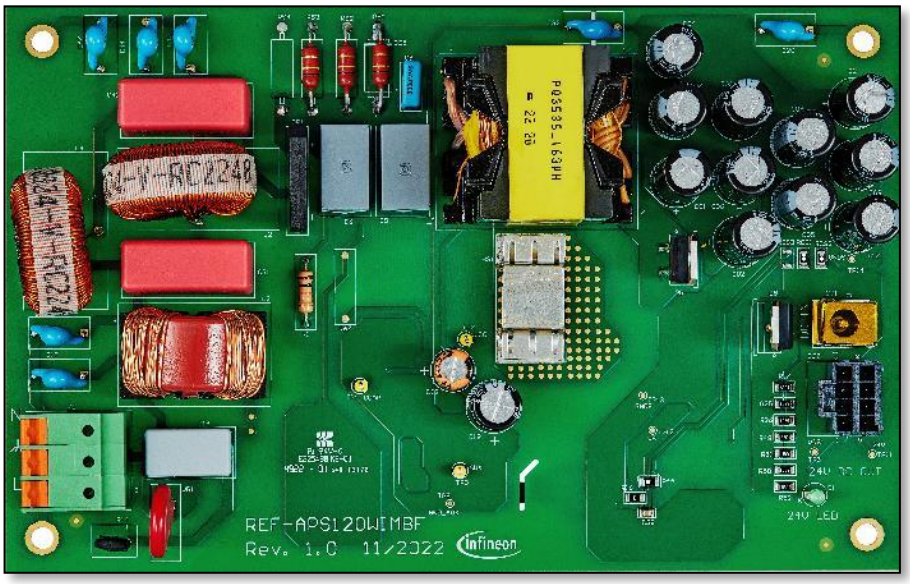


Figure 7 Mechanical layout of the SMPS board

2 System functional description

2.1 2-level, active front-end converter (AFE) for AC/DC stage

2.1.1 Specifications and main components

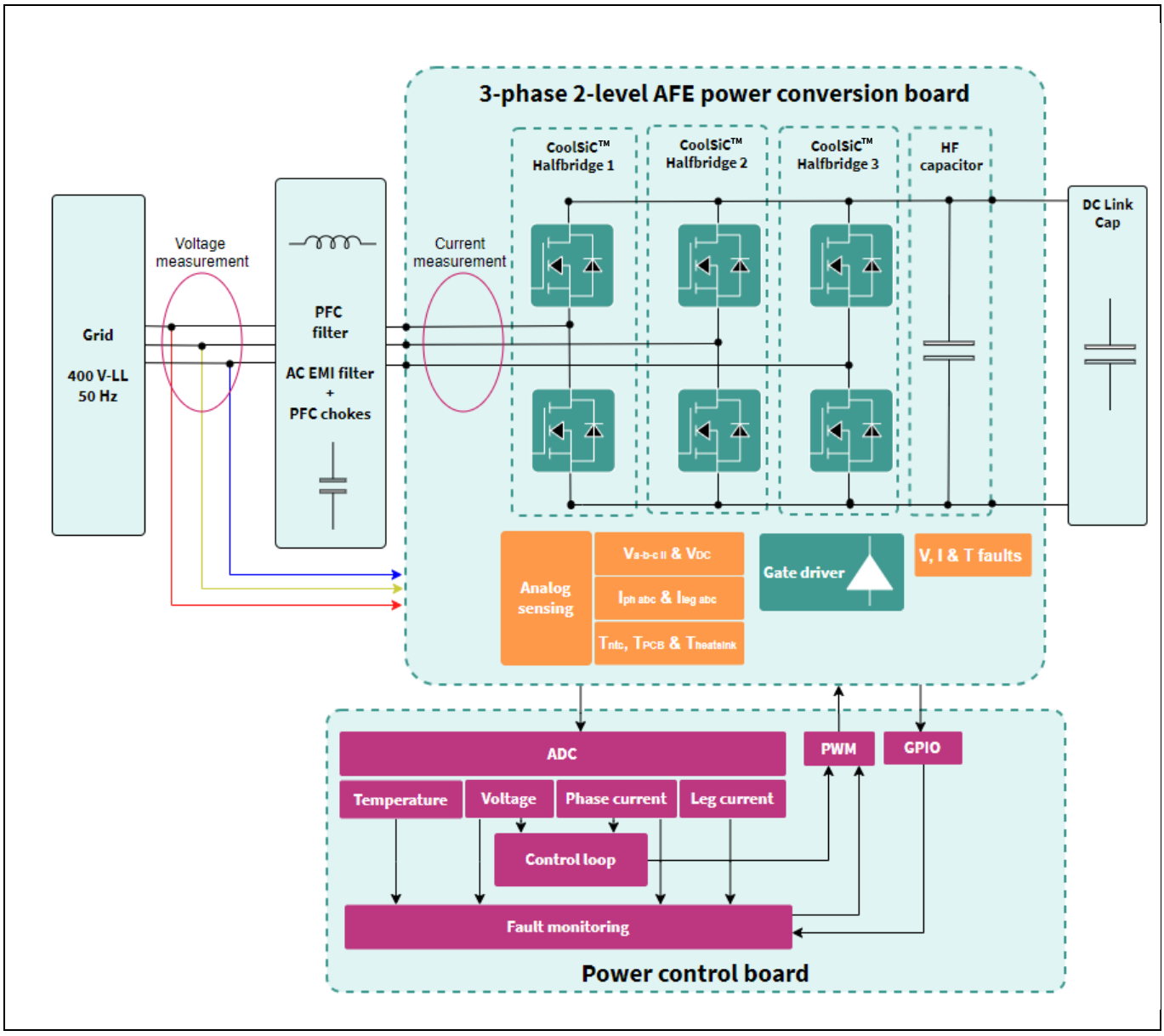


Figure 8 AFE block diagram

Table 3 Specifications of the AFE, as measured on the demonstration system

Parameter	Specifications	Minimum value	Nominal value	Maximum value	Unit
Input*	AC line frequency		50		Hz
	Input voltage, line-to-line (RMS)		400		V_{LL_rms}
	Power factor @ 45 kW		0.99		
	Current THD @ 45 kW	5.3		9.5	%
Output	PFC output (VDC)	700		840	V
	Output power**		45	50	kW
	DC-link voltage ripple @ 45 kW, 570 V DAB output		17		V
Performance	Switching frequency		48		kHz

*The demonstration system was designed for the European grid (400 V_{LL_rms} and 50 Hz)

**Exceeding 45 kW would cause the DC-link voltage to drop slightly below the specified values

AFE is a three-phase, two-level, three-wire topology used for rectification, power factor correction, and voltage boosting from the grid to the DC link. It also has bi-directional power flow capability. Its main required components are:

- PFC filter (AC EMI filter board + PFC chokes)
- Power conversion board
- DC-link capacitor

2.1.2 PFC choke and DC-link capacitors

In a three-phase AFE, the inductor currents modulate in amplitude and duty cycle for a constant switching frequency with respect to the modulation. The inductor current carries high-frequency current ripples and is responsible for boosting the input voltage to maintain a desired DC-link voltage. The inductance of the PFC choke is determined based on the current ripple requirements, switching frequency DC-link voltage and modulation method used. More information can be found in [6].

$$I_{i/p_{peak}} = \sqrt{2} * \frac{P_o}{\sqrt{3} * V_{LL_rms} * \eta} = \sqrt{2} * \frac{45\ kW}{\sqrt{3} * 400\ V * 0.96} = 96\ A \quad (1)$$

$$L_c = \frac{V_{DC}}{6 * f_{sw} * \Delta i_{i/p_{peak}}} = \frac{800\ V}{6 * 48\ kHz * (0.25 * 96)} = 116\ \mu H \quad (2)$$

Three inductors with a value of 110 µH were chosen for this design. The part number is P303231D002 from TDK.

The calculation of the DC-link capacitor depends on the topology of choice, voltage ripple requirements and line frequency. More information can be found in [7].

$$C_{LF} = \frac{\sqrt{3} * P_o}{240 * f_{line} * \Delta V_{pp} * V_{llrms}} = \frac{\sqrt{3} * 45\ kW}{240 * 50\ Hz * (0.05 * 800)\ V * 400\ V} = 406\ \mu F \quad (3)$$

Three film capacitors were used in this design, each having 140 µF, with part number B25620B1147K101 from TDK.

2.1.3 DC-link variation based on the required output voltage

Table 4 DC-link voltage variation based on DAB required output DC voltage

DAB output voltage required	DC-link voltage
350 V ≤ V_o ≤ 500 V	500 V x 1.4 = 700 V
500 V ≤ V_o ≤ 600 V	1.4 V_o
600 V ≤ V_o	600 V x 1.4 = 840 V

Since the AFE is a boost circuit, it can raise the input voltage to higher output DC-link voltages. The AFE circuit is controlled to maintain the DC-link voltage at levels between 700 VDC and 840 VDC.

The decision to vary the DC-link voltage was made to increase the soft-switching range of the DAB DC-DC converter. The demonstration system was only tested for 400 VLL rms input voltage, but was designed to also operate at 460 V_{LL_rms}, which means that the rectified voltage could reach 650 V. Based on that, a minimum value of 700 VDC for the DC-link has been set in the demo software.

For DAB, if the voltage transfer ratio is kept at a value of one, soft switching can be obtained across both the primary and secondary sides.

The voltage transfer ratio d is given by:

$$d = \frac{nV_o}{V_{in}} \quad (4)$$

Where n is the primary to secondary turns ratio of the transformer and is equal to 1.4 in this design. By making the DC-link voltage equal to 1.4 times the required output voltage, soft switching can be ensured across both the primary and secondary legs.

Nevertheless, a maximum voltage for the DC-link voltage was set at 840 VDC. This choice was based on observations during testing. Due to the parasitic inductance of the PCB, there was a spike in the drain-source voltage of the MOSFET. In the lower voltage ranges below 850 V, the spike was observed to be between 100 to 150 V. The maximum DC-link voltage was therefore limited to 840 V. To prevent a false turn-on, the negative gate-source voltage for the AFE was set to -5 V. This is contrary to the DAB power conversion board, in which the negative voltage was set to -3 V.

2.1.4 3-phase 2-level AFE control

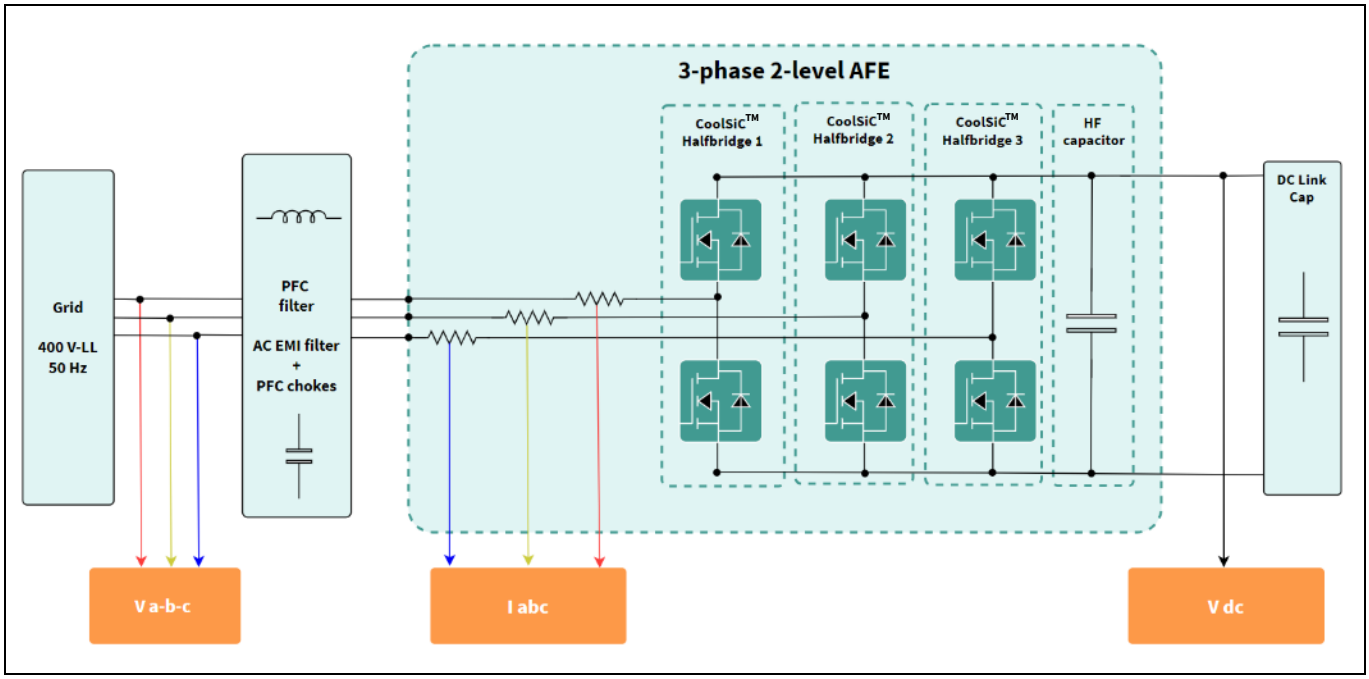


Figure 9 Measured signals needed for AFE control

The control loop of the three-phase AFE converter was implemented using the synchronous reference frame. In the d-q synchronous reference frame, the d-axis component corresponds to active power while the q-axis component corresponds to the reactive power. The active power channel stabilizes the DC side voltage (outer voltage loop), and the reactive power channel can regulate the power factor (inner current loop).

For the implementation the grid voltages, currents and also the output voltage on the DC-link need to be measured. In the demonstration system, the 3-phase voltages were measured at the grid before the PFC filter, so cables from the grid side needed to be connected to the power conversion board where the voltage measurement circuitry was located. The currents, however, were measured after the PFC filter, directly on the board and no additional connections were necessary.

Table 5 Variables

Parameter	Description
V_{dc}	DC-link voltage
$V_{a\text{-}b\text{-}c}$	Three-phase, line-to-line voltages
V_{abc}	Three-phase voltages
V_d	Direct axis voltage
V_q	Quadrature axis voltage
ω_g	Grid frequency (2*π*50) rad/s
L	Grid filter inductance
R	DC resistance
C	DC-link capacitance
$K_{p_{PLL}}, K_{i_{PLL}}$	PLL PI controller parameters
K_{p_c}, K_{i_c}	Current PI controller parameters

Parameter	Description
K_{p_v}, K_{i_c}	Voltage PI controller parameters

2.1.4.1 Phase-locked loop

The grid voltages and currents are converted to d-q frame using the Park and Clarke transformation. A phase-locked loop (PLL) was implemented for synchronization with the grid, and to obtain the phase angle of the grid voltages used for the Park transformation. Figure 10 shows a block diagram of the PLL implementation.

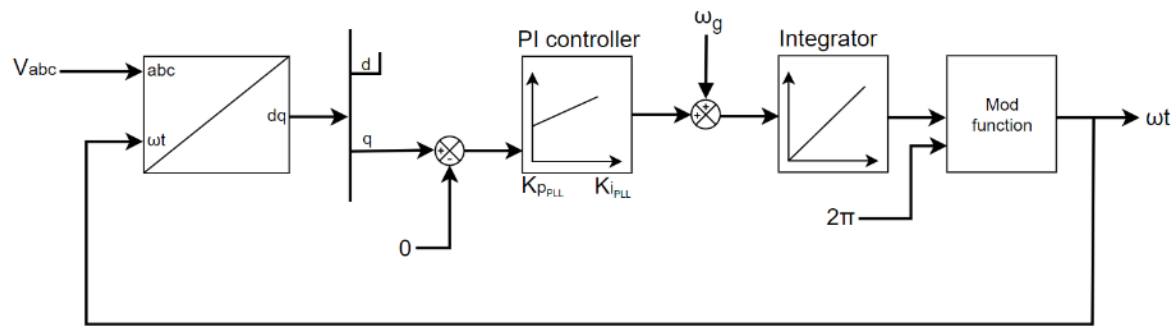


Figure 10 PLL implementation

A PI controller regulates and locks the q-component of the voltage to zero. The error is fed to the controller, and its output corresponds to the frequency. The grid frequency is also feedforwarded in the path. An integrator is then used to determine the angle. Determining PI controller values:

PI values are tuned manually to obtain optimal results. The values used in this design are:

$$K_{p_{PLL}} = 0.6$$

$$K_{i_{PLL}} = 30$$

2.1.4.2 Voltage-oriented control

The control loop consisted of an inner decoupled current controller and an outer DC voltage regulator. The inner current controller was controlling the input line currents to track the reference current. One advantage of this control scheme is that the active and reactive power can be controlled separately by controlling i_d and i_q. Unity power-factor operation is achieved when the q-axis reference current vector is in phase with the grid voltage. Ideally, since the voltages and currents for the AFE are not measured at the same point, the i_q^* reference should not be set exactly to zero to compensate for the reactive power for the filter. In this design, the i_q^* reference has been set to zero for simplicity reasons.

The outer DC voltage controller was regulating the current indirectly to maintain a constant DC voltage. The output of the current controller was the voltage reference that is used by the modulator (space vector modulation (SVM) in this design) to generate the required PWM signals. The speed of the outer DC voltage regulator will be slower than that of the inner current controller. Figure 11 shows a block diagram for the control implementation.

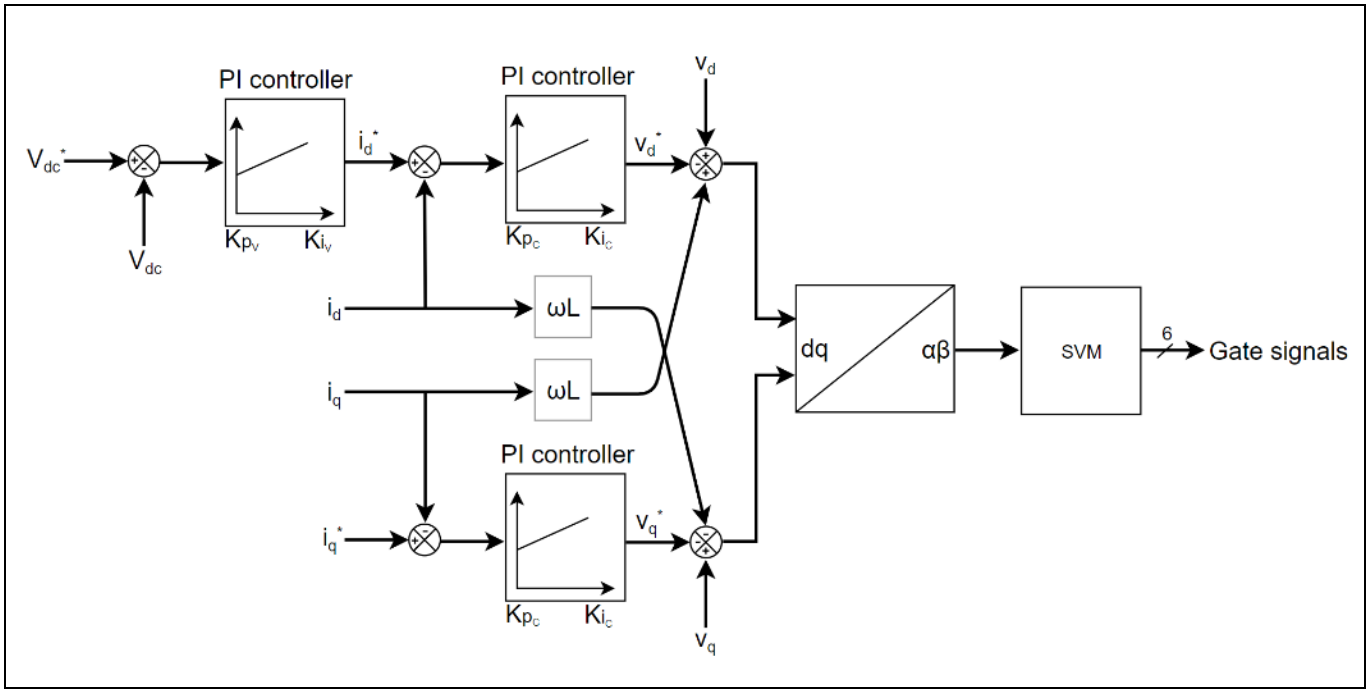


Figure 11 VOC implementation

The control used decouples the d and q-components of the currents so that they are completely independent. This, in turn, simplifies the control, because now the plant can be simply modeled as a first-order lag system depending on the inductance of the PFC choke and its DC resistance, as shown in Figure 12.

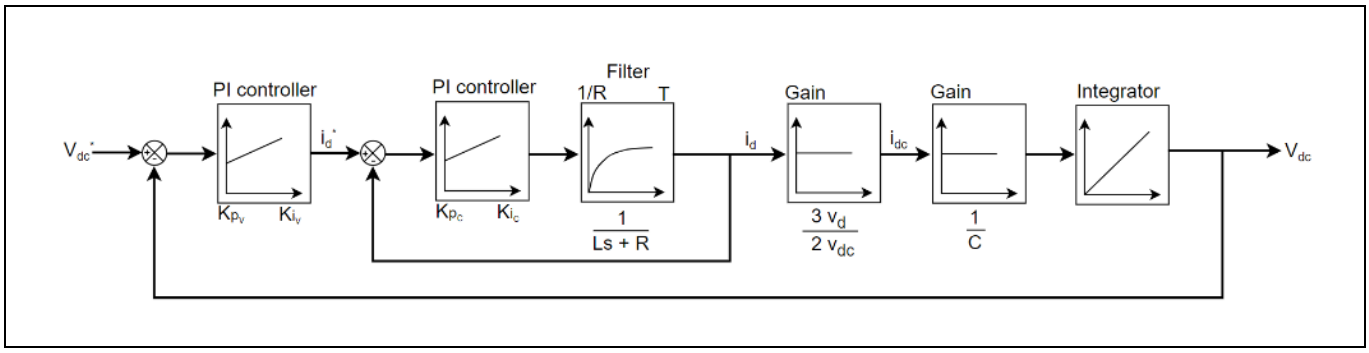


Figure 12 Closed-loop model

For the inner current controller, the plant transfer function is given by:

$$\frac{i_d}{v_d} = \frac{1}{Ls+R} \quad (5)$$

The controller values are then obtained using pole placement for pole-zero cancellation. The current controller bandwidth is chosen as 1.066 kHz and the corresponding PI values are given by:

$$K_{p_c} = 0.8$$

$$K_{i_c} = 28.1$$

For designing the voltage controller, the dynamics of the voltage across the output capacitor are to be considered, given by:

$$\frac{V_{dc}}{i_{dc}} = \frac{1}{Cs} \quad (6)$$

The controller was designed to achieve a phase margin of 70° at a crossover frequency of 100 Hz. The controller values are given by:

$$K_{p_v} = 0.28$$

$$K_{i_v} = 18.8$$

2.2 3-phase, dual-active bridge (DAB) converter for DC/DC stage

2.2.1 Specifications and main components

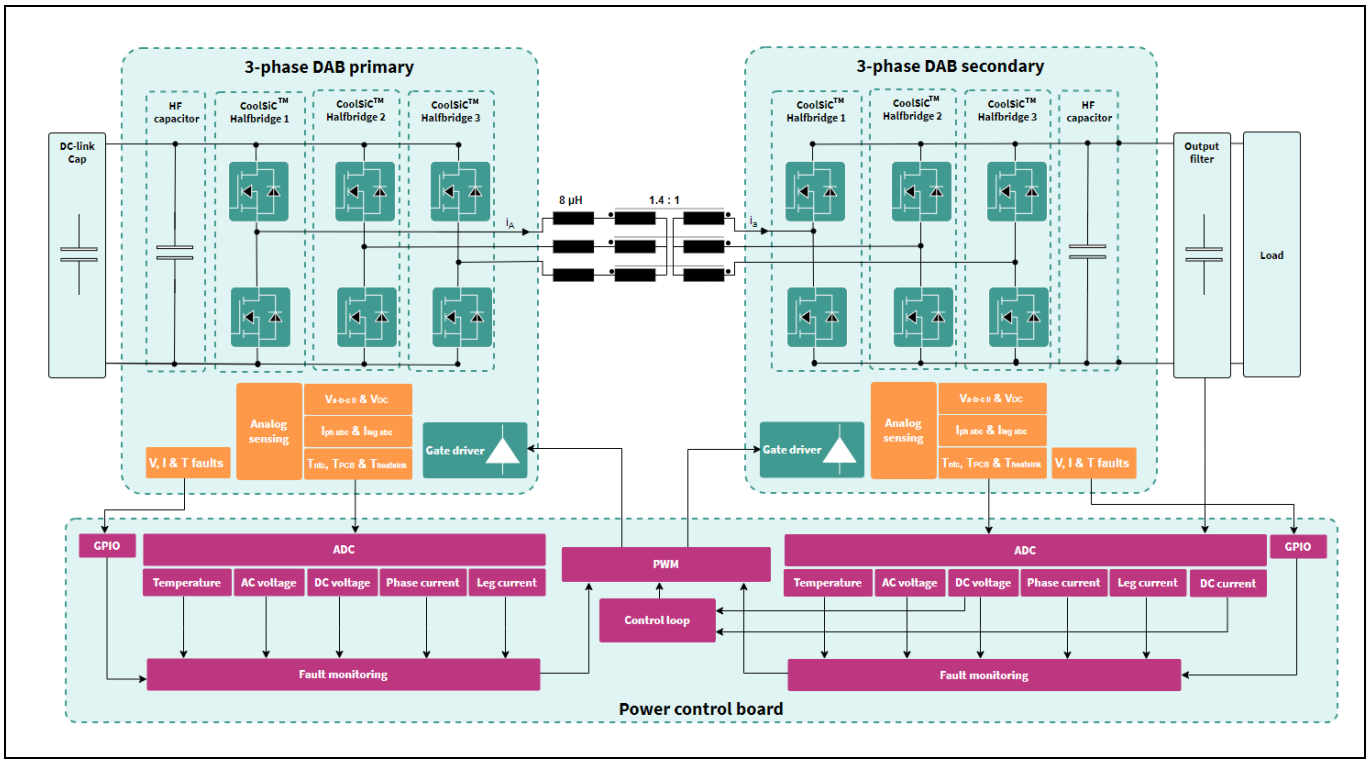


Figure 13 DAB block diagram

Table 6 Specifications of the DC/DC power converter, as measured on the demonstration system

Parameter	Specifications	Minimum Value	Nominal Value	Maximum Value	Unit
Input	DC-link voltage	700	800	840	V
Output	Output voltage*	350	570	750	V
	Output power**	-	45	50	kW
	Output current***	-	-	100	A
	Output voltage ripple	-		17	$V_{pk\text{-}pk}$
Performance	Switching frequency		100		kHz

*Tested voltage ranges are listed in the operation chart in Figure 34

**Exceeding 45 kW was causing DC-link voltage to drop slightly below the specified values

***The demonstration system was tested and verified up to 75 A due to limitations in the Infineon test setup

2.2.1.1 Power transfer in 3-phase DAB

DAB operates using the same theory of operation of a transmission line in power systems, where power can be transferred between two ends by varying the phase angle between the voltages at both ends. More information about the theory of operation can be found in [8].

Figure 14 shows the voltage waveforms between each of the phases and the star point, the voltage on the inductor, and the current through the inductor for both the primary and secondary sides. The converter has two modes of operation. The first mode is when the phase shift between the primary and secondary sides is below 60° and the second mode is when the phase shift lies between 60° and 120°.

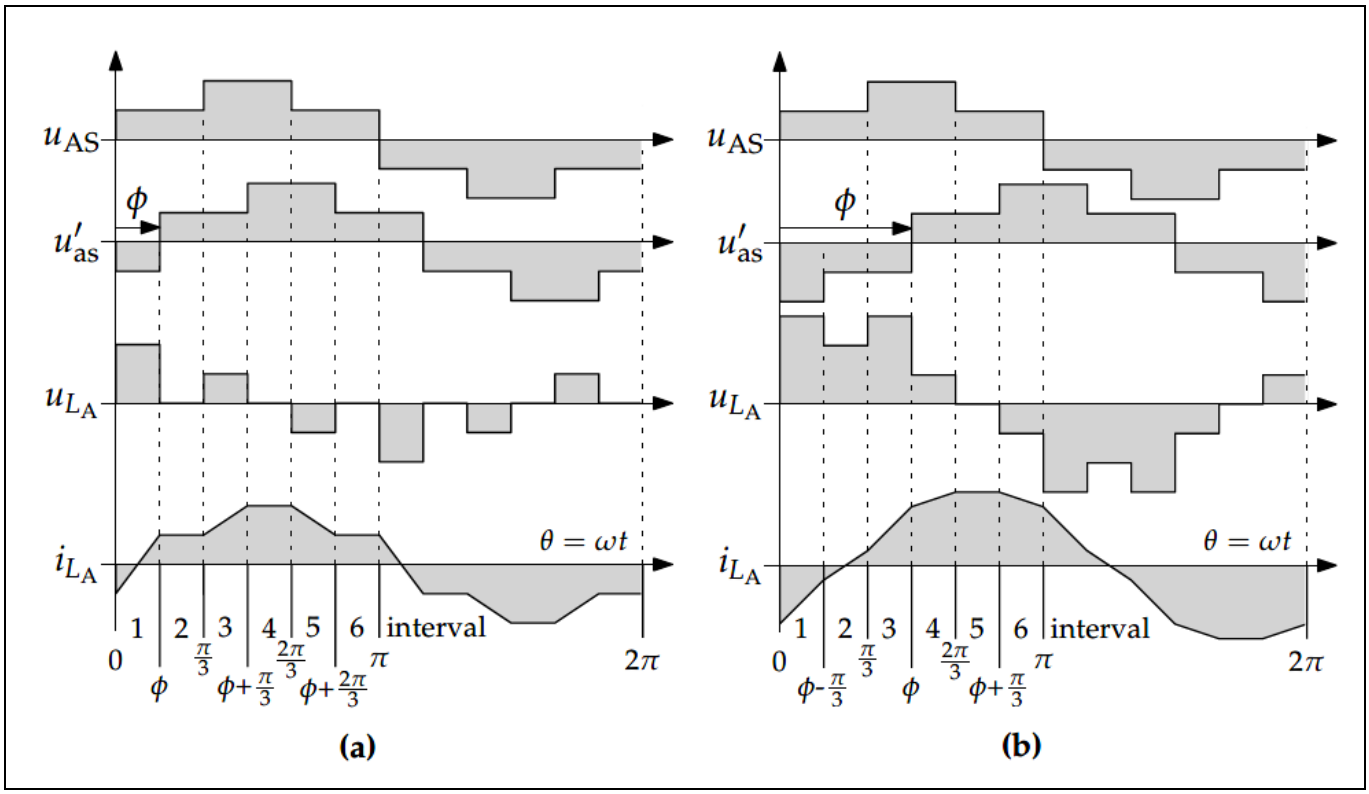


Figure 14 Idealized voltage and current waveforms of the 2-level, 3-phase DAB converter with a star-star connected transformer for (a) phase shift 0 ≤ Φ ≤ π/3 and (b) π/3 ≤ Φ ≤ 2π/3, assuming a transformer turns ratio of 1 and equal input and output voltages [8]

This topology achieves maximum power transfer when the phase shift between the primary and secondary sides is 90°. However, in this demonstration system, the operation was limited in the demo control software only to the first mode of operation less than 60°, as the rms currents through the transformer are higher in the second mode.

The power transfer equation for the first mode is given by:

$$P = \frac{V_1 n V_2}{\omega L}\phi\left(\frac{2}{3} - \frac{\phi}{2\pi}\right) \quad (7)$$

The main components of this topology include the two bridges, the transfer inductor, which in this design is not a separate element, but is the leakage inductance of the transformer, the transformer, and the output capacitors.

2.2.1.2 ZVS, leakage inductance and transformer turns ratio

Based on the current directions in Figure 13 and the inductor current waveforms in Figure 14, it can be concluded that to achieve ZVS in the primary side $i_{L_A}(0)$ should be less than zero, and to achieve ZVS in the secondary side $i_{L_A}(1)$ should be greater than zero.

For the primary side, the current at $i_{L_A}(0)$ is given by:

$$I_0 = \frac{(nV_2 - V_1)2\pi - 3nV_2\phi}{9\omega L} \quad (8)$$

Solving the inequality $I_0 < 0$ to get the minimum phase shift required for ZVS:

$$\phi_{min} = \frac{2\pi}{3}\frac{(d-1)}{d} \quad (9)$$

Where the voltage transfer ratio $d = \frac{nV_2}{V_1}$, and n is the turns ratio.

Substituting ϕ_{min}, the minimum power required to achieve ZVS in the primary side is:

$$P_{min} = \frac{V_1^2(d^2-1)}{9fLd} \quad (10)$$

For the secondary side, the current at $i_{L_A}(1)$ is given by:

$$I_1 = \frac{3V_1\phi - V_1 2\pi + nV_2 2\pi}{9\omega L} \quad (11)$$

Solving the inequality $I_1 > 0$ to get the minimum phase shift required for ZVS:

$$\phi_{min} = \frac{2\pi}{3}(1-d) \quad (12)$$

Substituting ϕ_{min}, the minimum power required to achieve ZVS in the secondary side is:

$$P_{min} = \frac{V_1^2 d(1-d^2)}{9fL} \quad (13)$$

By fixing the DC-link voltage to 800 V, using a transformer turns ratio 1.4 and a leakage inductance of 8 µH, the ZVS boundary for both the primary and secondary sides over the output voltage range can be observed as shown in Figure 15. The maximum power transfer for each point on the output voltage range can be plotted as well.

One conclusion is that there is a point at which both sides can achieve ZVS. This point corresponds to d = 1. Another conclusion can be drawn by varying the leakage inductance of the transformer. It is observed that a lower value for the inductance leads to more power transfer for the same operation points. A higher value for the leakage inductance, however, facilitates ZVS.

For this demonstration system, a transformer with a turns ratio of 1.4 and a leakage inductance of 8 µH was chosen. The part number is P302640D003 from TDK.

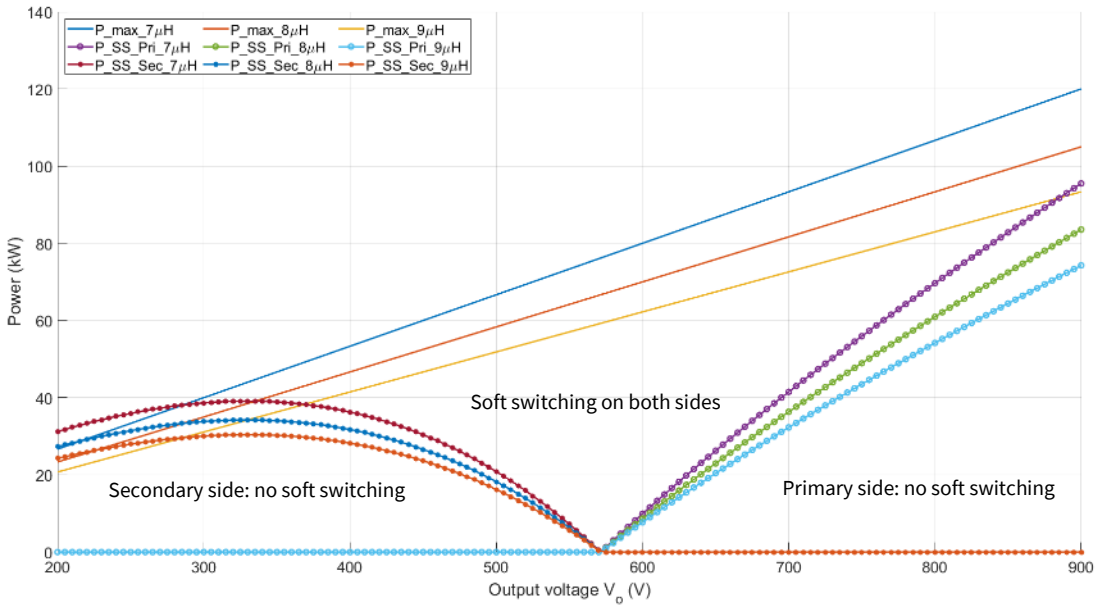


Figure 15 The influence of the voltage transfer ratio and the transformer leakage inductance on ZVS and power transfer

To increase the output voltage range at which ZVS can be achieved, a DC-link with controllable variable voltage was implemented, as discussed in Section 2.1.3. This strategy allows d to be equal to unity for the whole range between 500 V and 600 V. The DC-link voltage value corresponding to the output voltage ranges can be seen in Table 6.

Table 7 DC-link voltage variation based on DAB required output DC voltage

DAB output voltage required	DC-link voltage
350 V ≤ V_o ≤ 500 V	500 V x 1.4 = 700 V
500 V ≤ V_o ≤ 600 V	1.4 V_o
600 V ≤ V_o	600 V x 1.4 = 840 V

The power vs. output voltage curve can then be plotted again, as shown in Figure 16. It can be seen that the range in which ZVS can be achieved on both sides has increased.

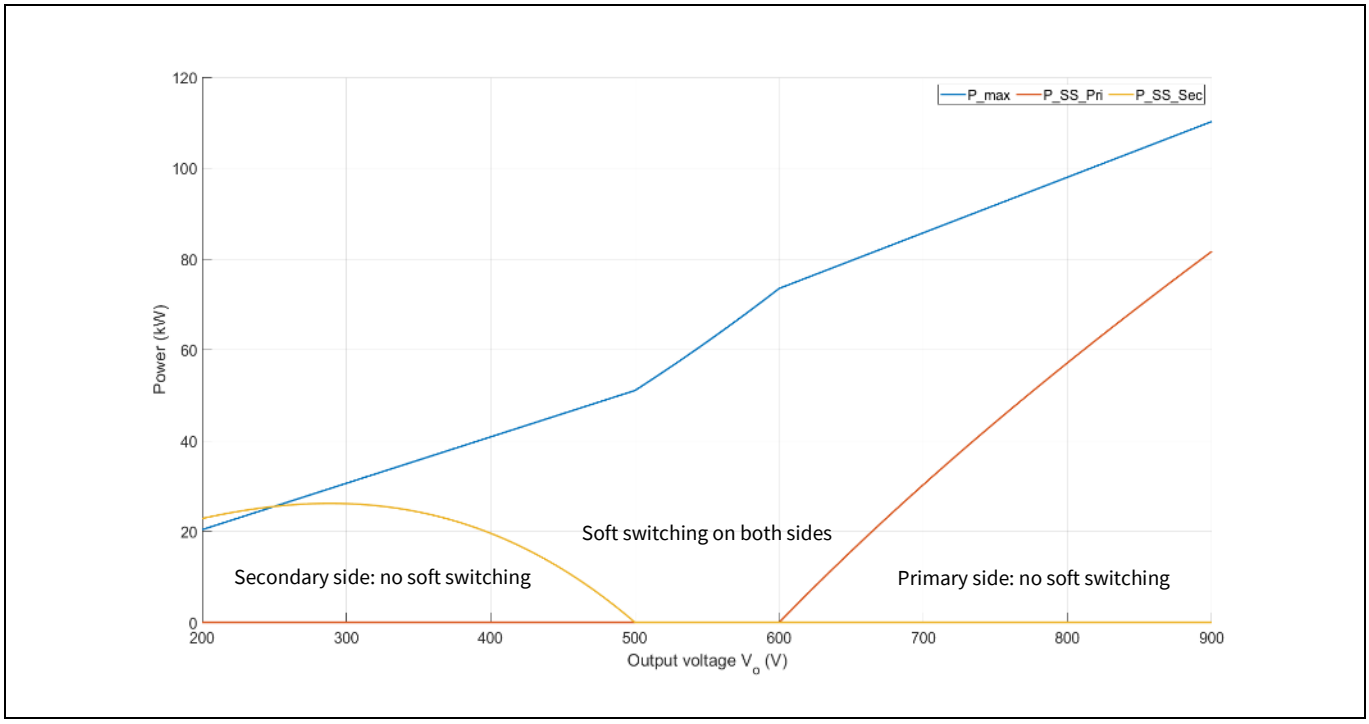


Figure 16 Effect of varying the DC-link voltage on ZVS

2.2.1.3 3-phase, 2-level DAB control

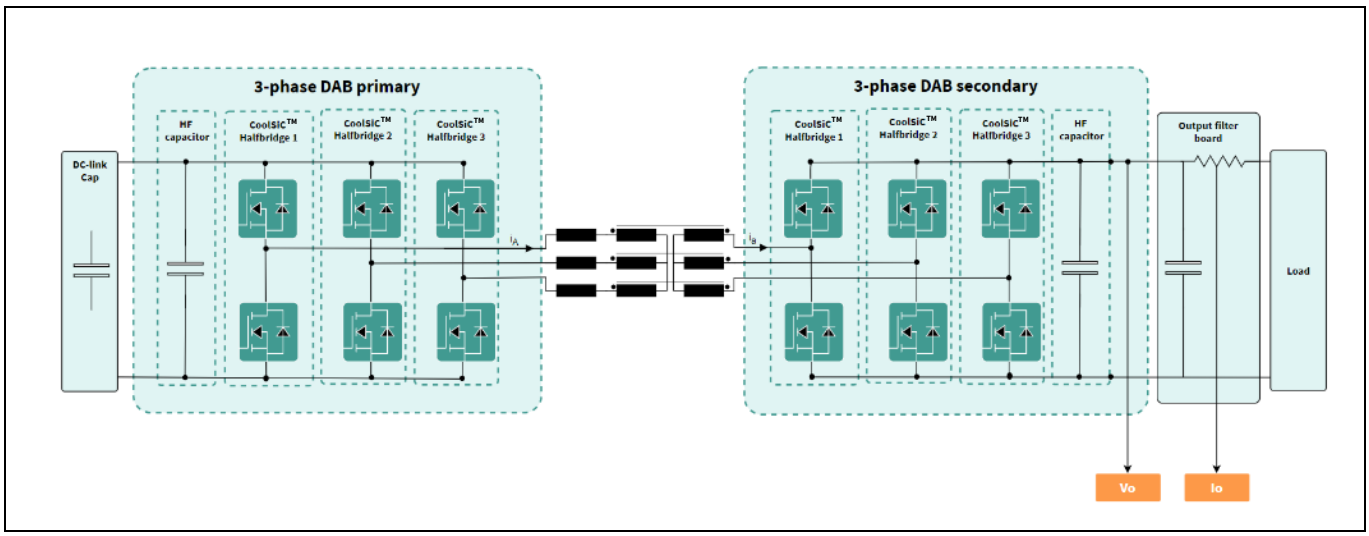


Figure 17 Measured signals required for DAB control

For the control of DAB for battery-charging applications, two measurements are necessary, the output DC current and the output DC voltage, for the converter to charge the battery according to Figure 18.
The three modes of operation are:

- Constant current mode (CC)
- Constant voltage mode (CV)
- Constant power mode (CP)

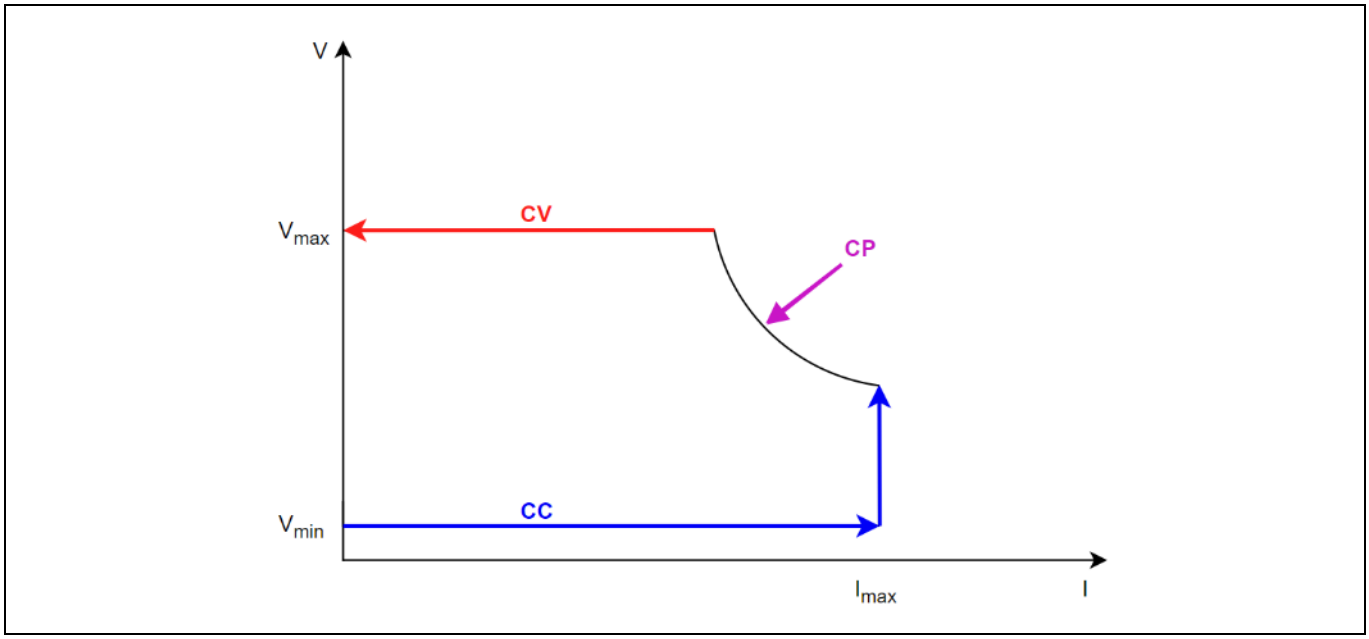


Figure 18 Battery charging curve

The DAB converter in this demonstration system was operated with the single-phase shift (SPS) modulation technique. In this scheme, both bridges are operated with 50% duty and fixed frequency, and phase shift is given to either of the bridges depending on the direction of the power flow. For forward mode, a positive phase shift is given to the secondary bridge, and for reverse mode, phase shift is applied to the primary bridge. Maximum phase shift is limited to 60° to prevent increased transformer RMS currents in the system. The control strategy for DAB is implemented based on the battery charging curve, i.e., constant current (CC), constant power (CP) and constant voltage (CV) by sensing the load current and load voltage.

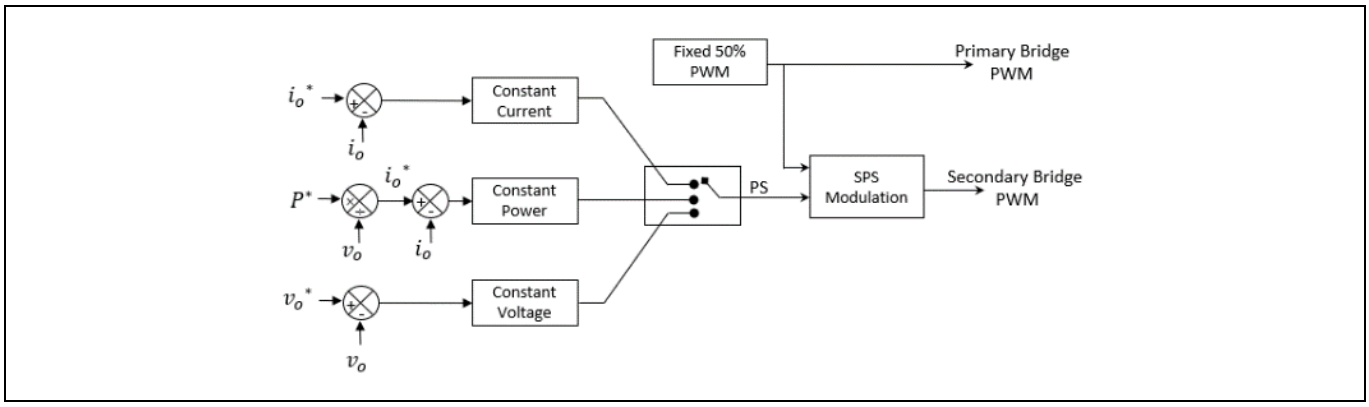


Figure 19 Closed-loop control of DAB

The state-space model of DAB is obtained from the generalized state-space averaging technique [9]. The state-space model is solved using MATLAB to obtain the plant transfer functions for different outputs and control signals. Finally, the control-to-output small-signal transfer functions are obtained. The model is validated between low frequency, and close to the switching frequency in [9]

$$\frac{V_o(s)}{\delta(s)} = G_{CV}, \qquad \frac{I_o(s)}{\delta(s)} = G_{cc} = G_{cp}$$

where G_{CV}, G_{CC}, G_{CP} are the plant transfer function for CV mode, CC mode and CP mode, respectively. The open loop transfer function is unstable, and hence the Type-II compensator is designed to boost the phase margin and

stabilize the system. The PI controllers are derived in continuous domain, and are converted to discrete domain using Tustin's bilinear transformation at a sampling period of 20 us.

2.2.1.3.1 Constant current mode (CC)

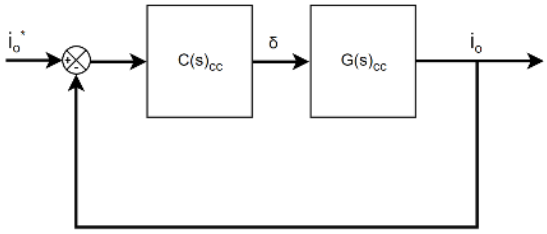


Figure 20 Constant current control loop

The compensator transfer function is given by:

$$C(s)_{cc} = \frac{1442s + 5.138e^7}{s^2 + 1.108e^5 s}$$

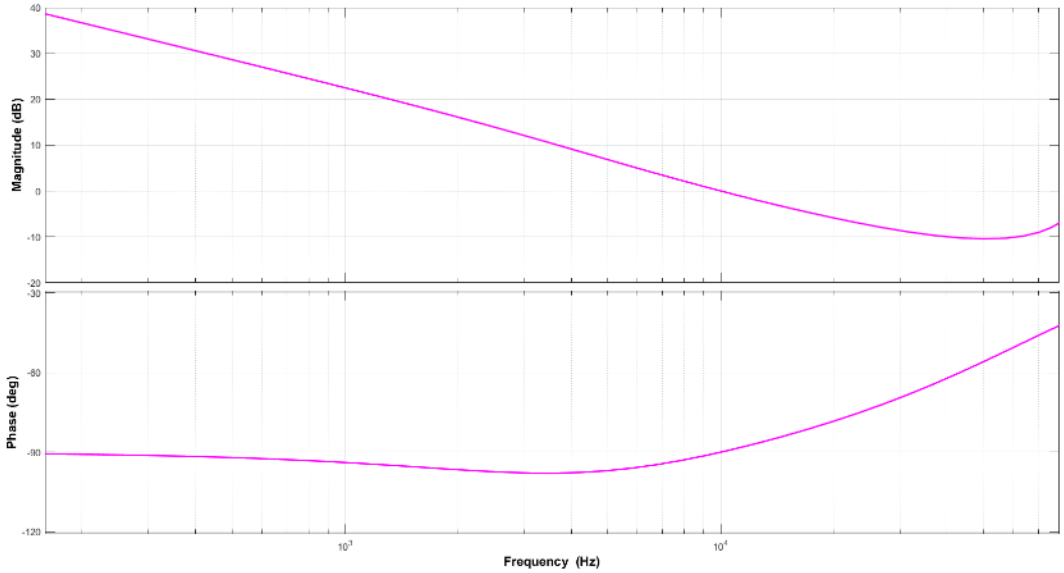


Figure 21 Bode plot of the converter after compensation

2.2.1.3.2 Constant power mode (CP)

For constant power operation, the controller used in constant current mode is used. To keep the power constant, the value of the current reference is reduced as voltage increases while charging. The current reference is derived from the required power set point and output voltage at that instant and is fed to the constant current controller.

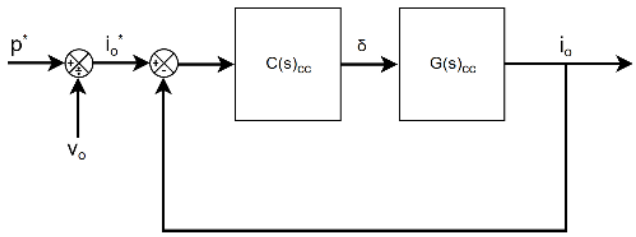


Figure 22 Constant current control loop

The compensator transfer function is given by:

$$C(s)_{cc} = \frac{1442s + 5.138e^7}{s^2 + 1.108e^5 s}$$

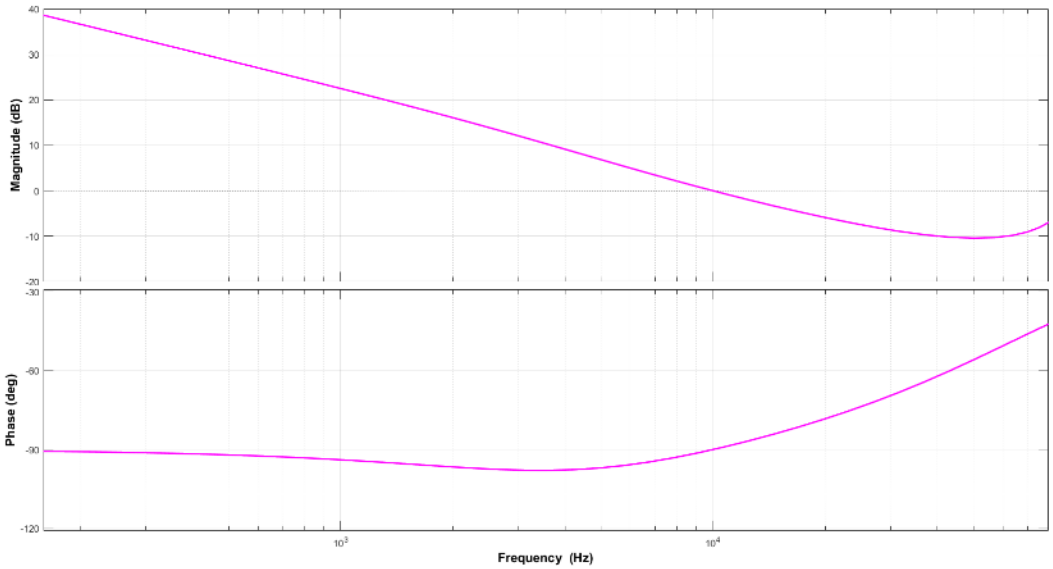


Figure 23 Bode plot of the converter after compensation

2.2.1.3.3 Constant voltage mode (CV)

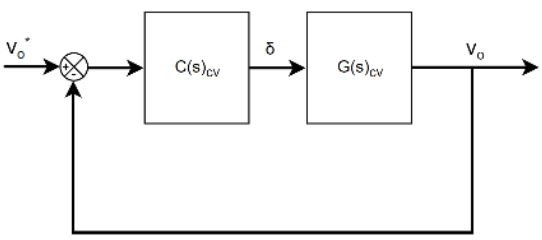


Figure 24 Constant voltage control loop

The compensator transfer function is given by:

$$C(s)_{cv} = \frac{759.1s + 1.089e^7}{s^2 + 2.751e^5 s}$$

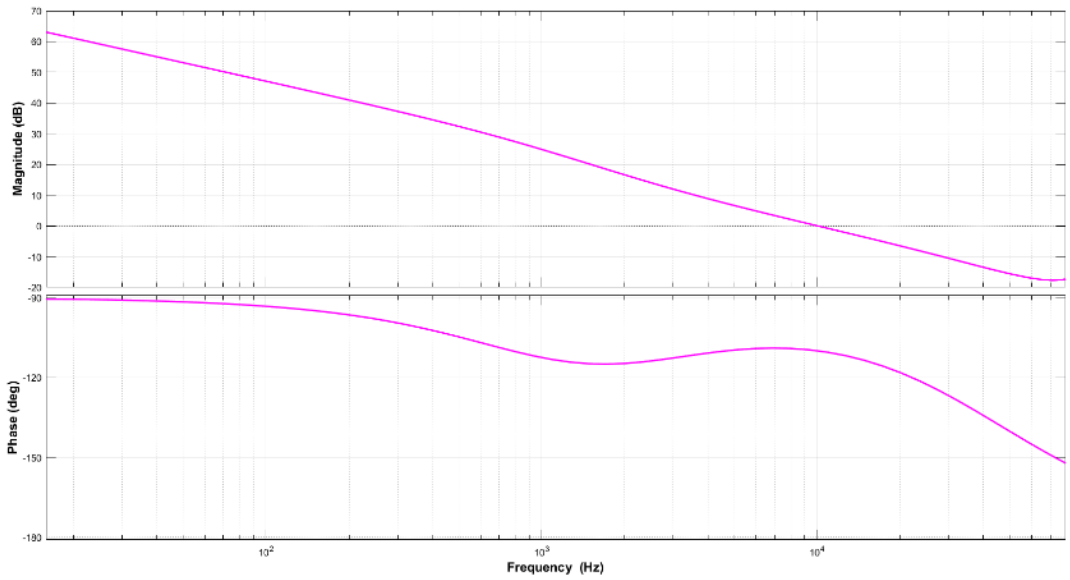


Figure 25 Bode plot of the converter after compensation

2.3 Reverse operation

The reverse-mode operation was done as a proof of concept to test the bidirectionality of the converter. However, grid synchronization was not implemented in the demo control software. In other words, the converter hardware is capable of bidirectional operation, but the control software was not capable of synchronising it with the grid in reverse mode.

Table 8 Specifications of the converter in reverse mode

Parameter	Specifications	Minimum Value	Nominal Value	Maximum Value	Unit
Input	Input voltage on DAB*	500	-	600	V
Output	DC-link voltage		700		V
	Output power	20	-	45	kW
	Output AC voltage	Variable (no grid synchronization)			V
	Output voltage frequency		50		Hz
Performance	DAB switching frequency		100		kHz
	AFE switching frequency		48		kHz

*Other voltages haven't been tested (Not specified)

For reverse-mode operation, the transfer of active power is regulated by the AFE stage, and the DC-link voltage is maintained by the DAB stage by operating in constant voltage control mode.

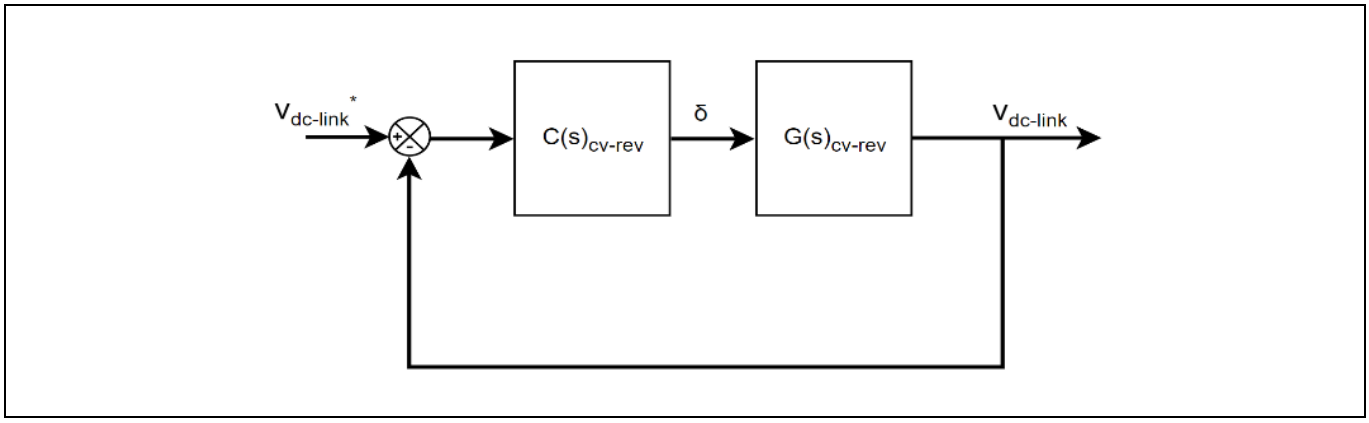


Figure 26 DAB control in reverse mode

The compensator transfer function is given by:

$$C(s)_{cv} = \frac{3.553e^{6}s + 3.882e^{8}}{s^{2} + 3.614e^{7}s}$$

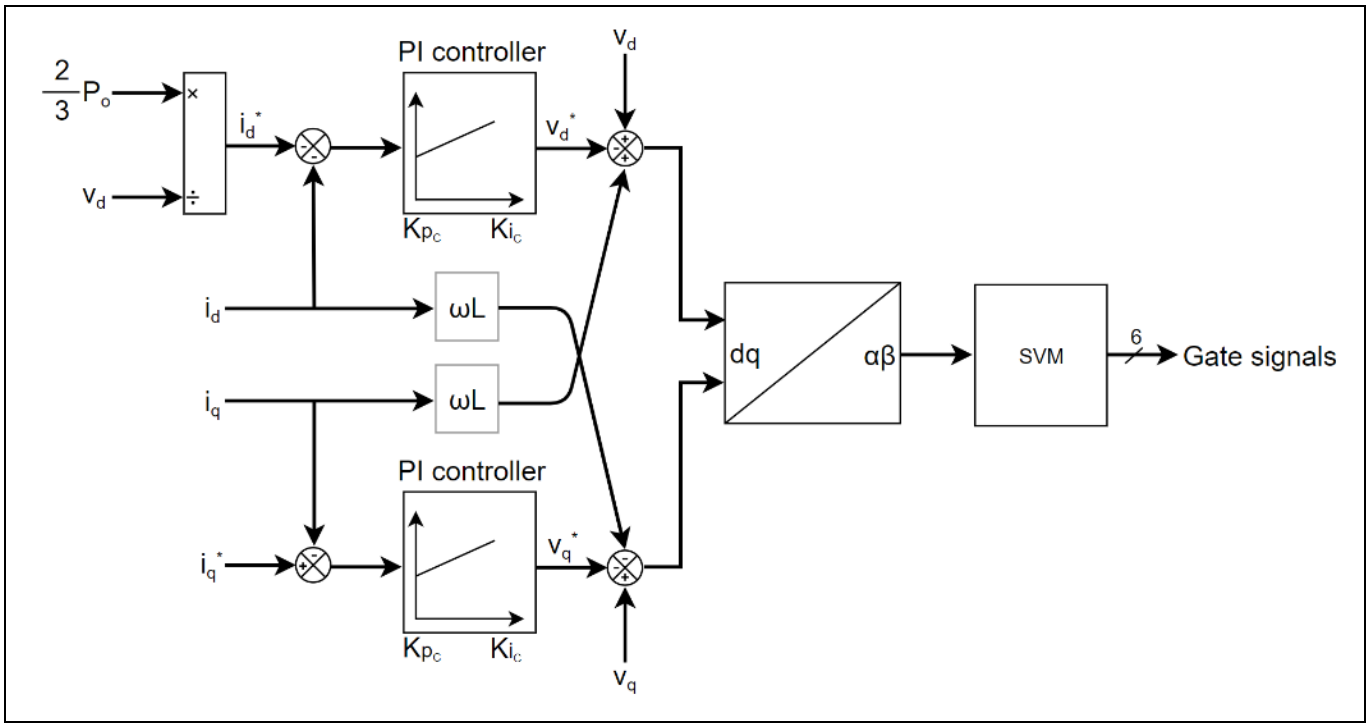


Figure 27 AFE control in reverse mode

3 Gate driver

3.1 AFE gate driver

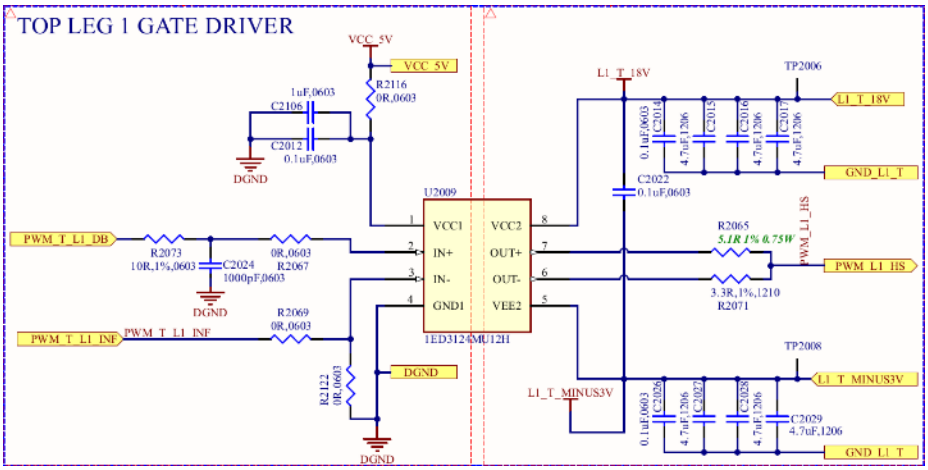


Figure 28 AFE gate driver circuit

Table 9 Gate drive for AFE

Parameter	Minimum	Nominal	Maximum	Unit
Positive gate voltage (taken from the low-dropout regulator (LDO) output of gate driver power supply)	17.64	18	18.36	V
Negative gate voltage (taken from gate driver power supply)	-5.13	-4.81	-4.5	V
Gate voltage swing	22.77	22.81	22.86	V
Switching frequency		48000		Hz
On-resistance	5.1			Ω
Off-resistance	3.3			Ω

Table 10 Module and gate driver used in the AFE stage

	Part number
Module choice	FF4MR12W2M1H_B11
Gate driver choice	1ED3124MU12H

3.2 DAB gate driver

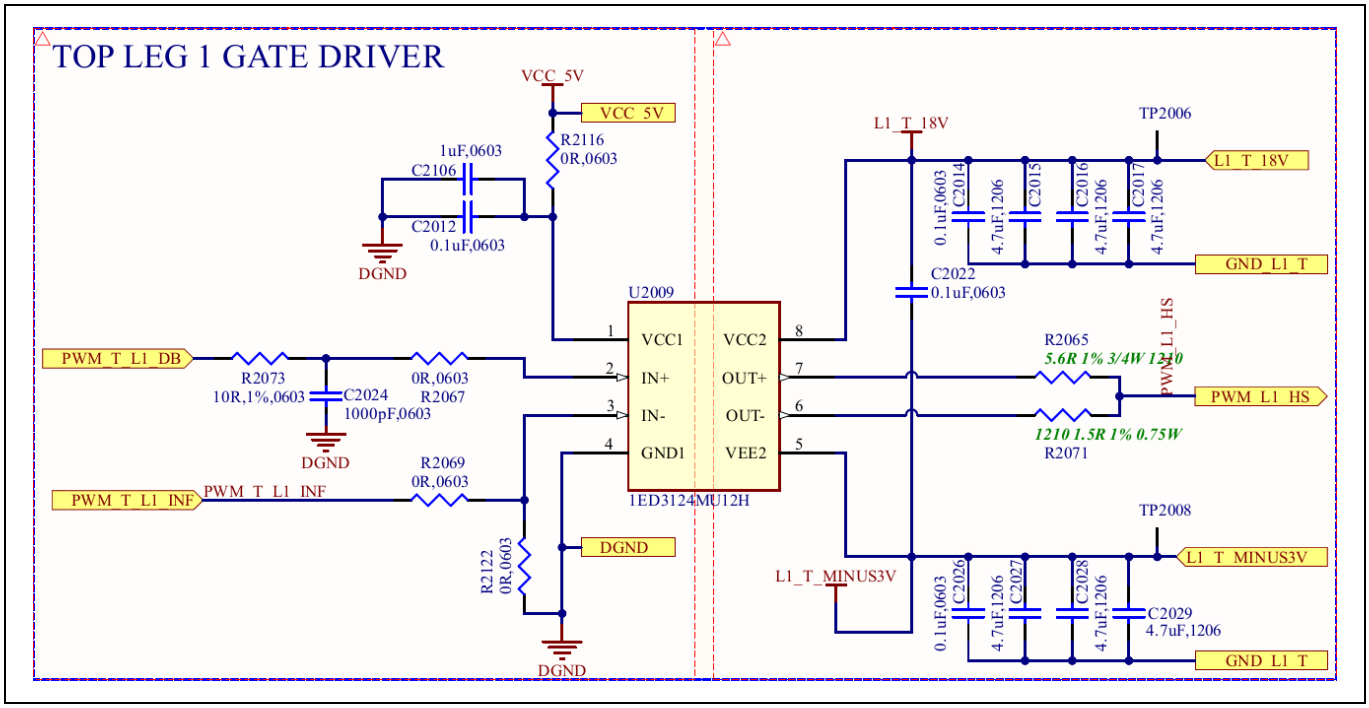


Figure 29 DAB gate driver circuit

Table 11 Requirements for DAB

Parameter	Minimum	Nominal	Maximum	Unit
Positive gate voltage (taken from LDO output of gate driver power supply document)	17.64	18	18.36	V
Negative gate voltage (taken from gate driver power supply document)	-3.22	-3	-2.8	V
Gate voltage swing	20.86	21	21.16	V
Switching frequency		100000		Hz
On-resistance	5.6			Ω
Off-resistance	1.5			Ω

Table 12 Module and gate driver used in the DAB stage

	Part number
Module choice	FF6MR12W2M1H_B11
Gate driver choice	1ED3124MU12H

3.3 PWM disable and dead-band generation

As a protection feature, a level-shifter circuit has been implemented that can disable the PWM inputs to the gate driver in case of a fault. A hardware dead-band generation circuit has also been implemented, where the capacitor value can be fine-tuned based on dead-time requirements.

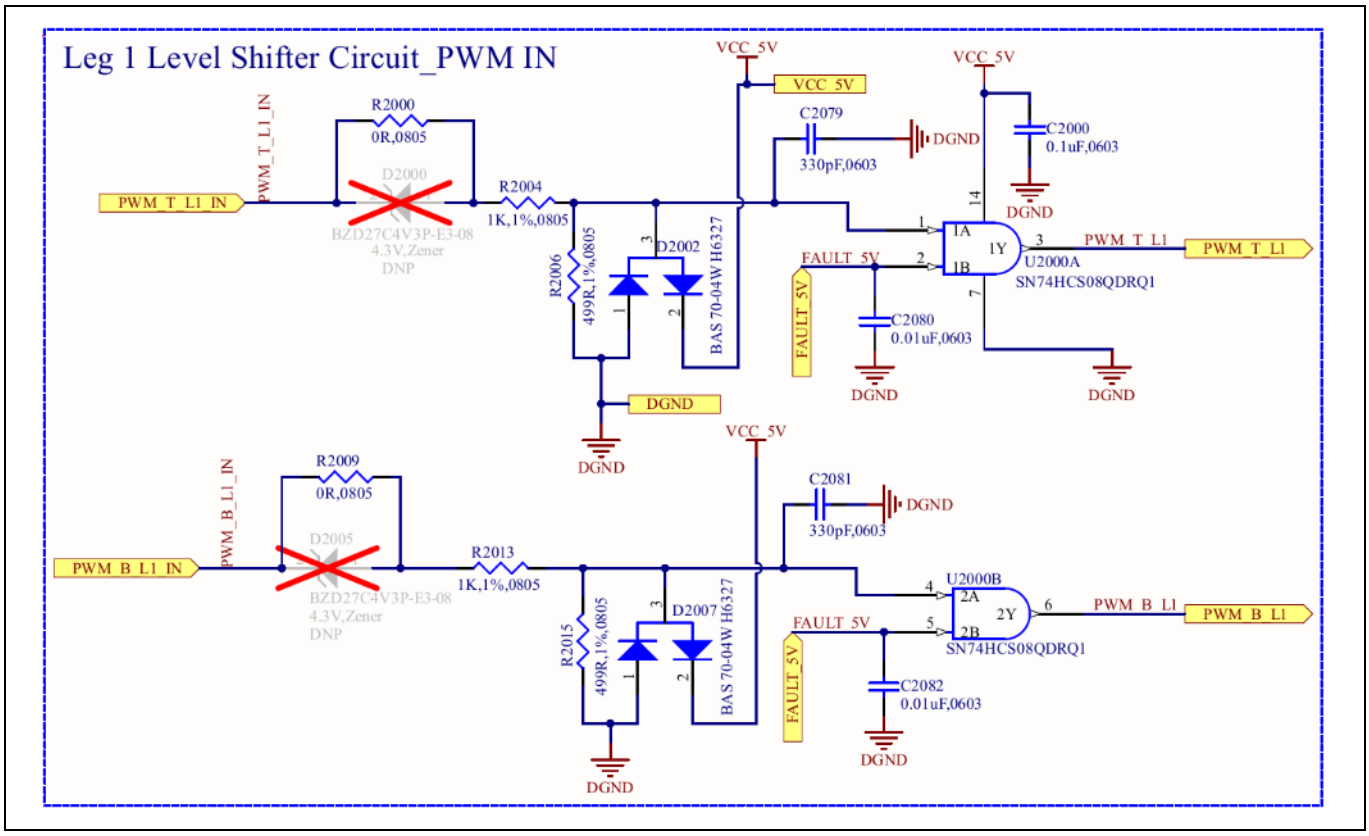


Figure 30 Level-shifter circuit

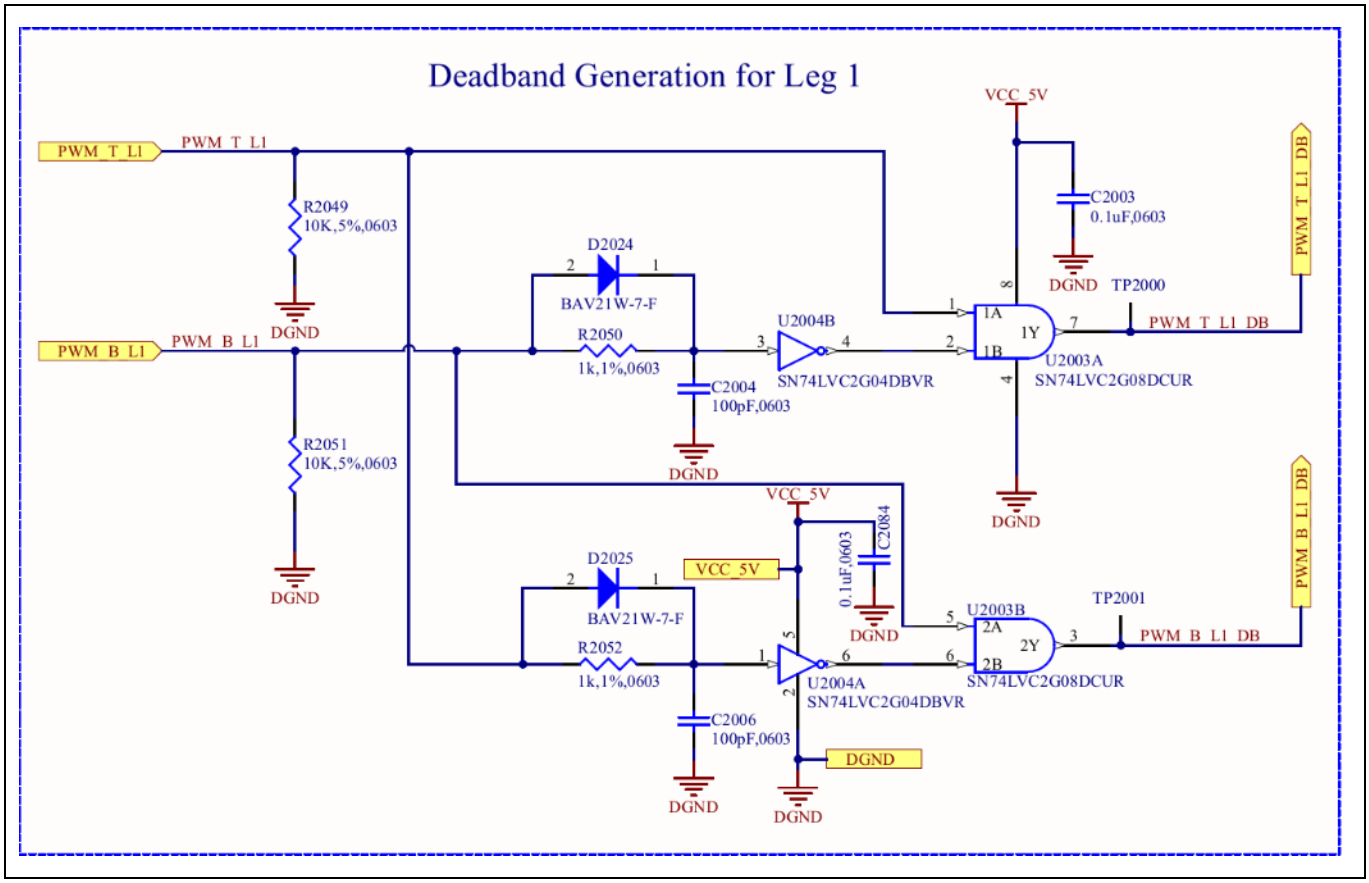


Figure 31 Deadband generation circuit

4 Assembly

4.1 Boards and components

The mechanical assembly shown below gives an indication of the various components that were used to realize the EV charger subunit demonstration system.

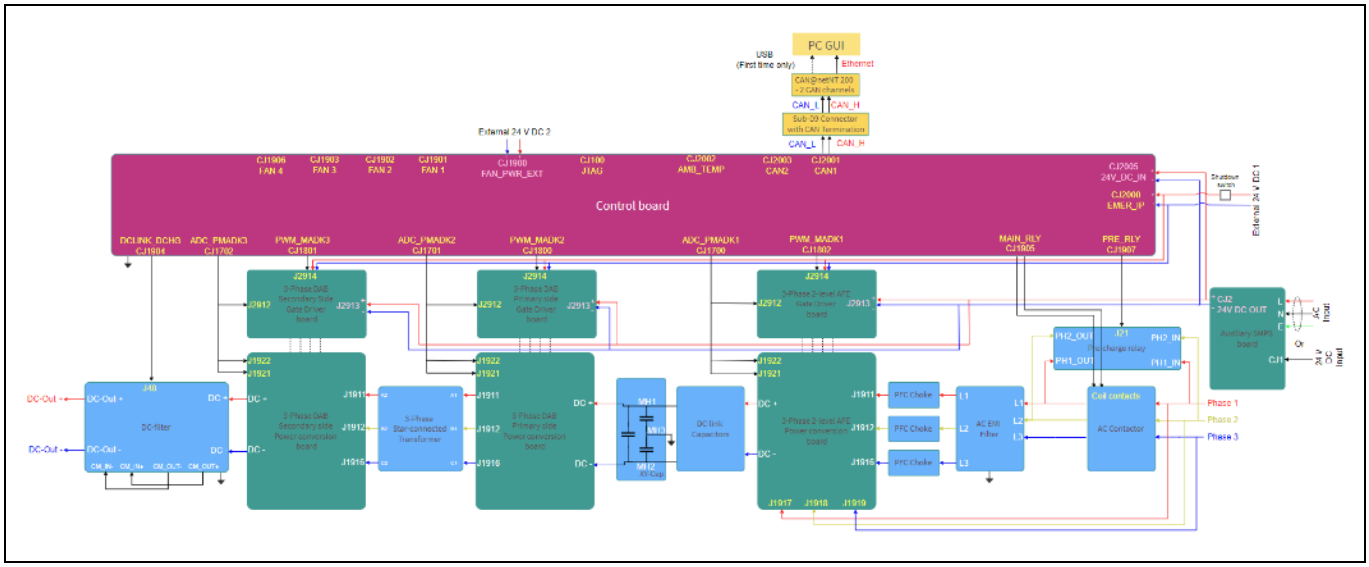


Figure 32 Assembly block diagram

Several boards and passive components were necessary to assemble the demonstration system. The components used in this design include:

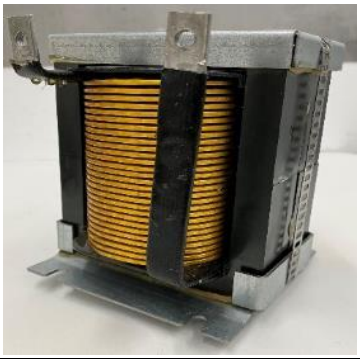
- 1x AC contactor (AF80-30-00-11 24-60V50/60HZ 20-60VDC contactor) from ABB
- 1x pre-charge relay board
- 1x AC EMI filter board (P303281D002) from TDK
- 1 x REF-2LC50K6MRW2CD (power conversion board for AC/DC stage)
- 3x DC-link capacitors (B25620) from TDK
- 1x XY capacitor board
- 1x 3-phase HF transformer (P302640D002) from TDK
- 2 x REF-2LC50K6MRW2CD (power conversion boards for DC/DC stages)
- 1x DC output filter board
- 1 x power control board
- 1 x auxiliary power supply board

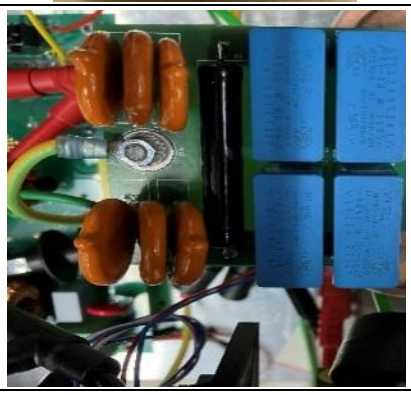
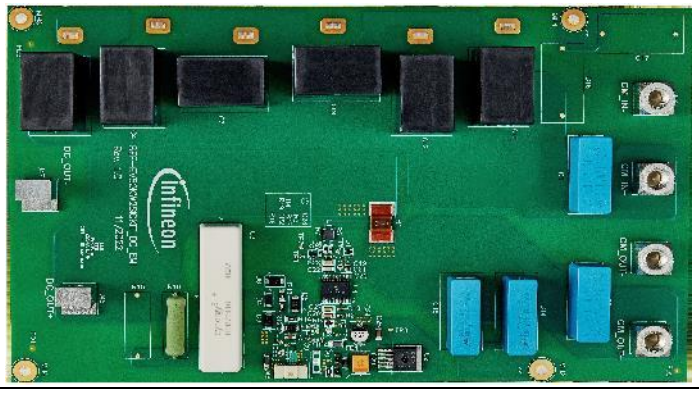
Besides these boards and passive components, specific heat sinks, busbars and wire harnesses were needed.

As a reference, the busbar used for connecting the DC-link capacitor to the AFE, and the DAB stages is shown in the appendix.

Infineon offers the Altium files and the BOMs for the power conversion board, AC EMI filter board, DC-filter board, pre-charge board and fuse board.

Table 13 Parts not offered by Infineon

Description	Part
1x AC contactor (AF80-30-00-11 24-60V50/60HZ 20-60VDC contactor) from ABB	 [10]
1x pre-charge relay board (Used as a path for inrush current to charge the output bulk capacitor before the PFC operates) (Altium files and BOM can be provided)	
1x AC EMI filter board (P303281D002) from TDK	
3x 1-phase PFC reactor (P303231D002) from TDK	

Description	Part
3x DC-link capacitors (B25620) from TDK (Connected on the busbar shown in the appendix)	
1x XY capacitor board (This board was added based on noise observations during bench-level testing) (Altium files and BOM can be provided)	
1x 3-phase HF transformer (P302640D002) from TDK	
1x DC output filter board (Altium files and BOM can be provided)	

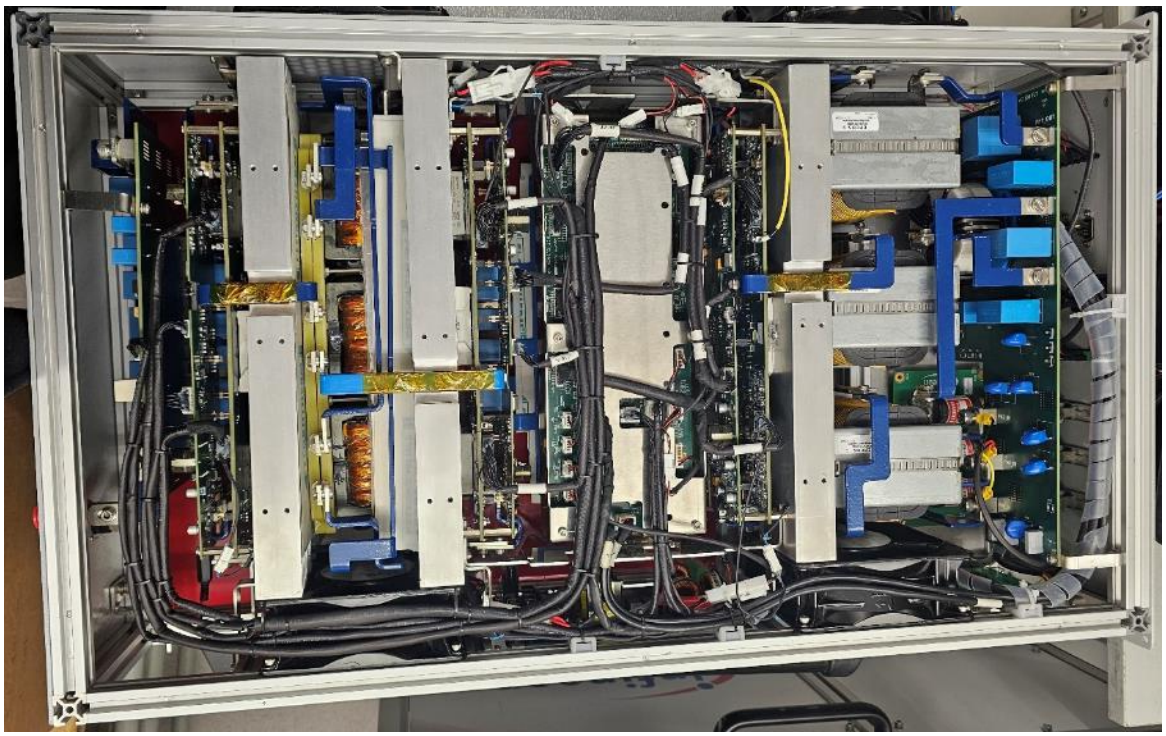


Figure 33 Possible realization of a DC EV charger subunit (example)

5 Testing and verification

5.1 Operation chart

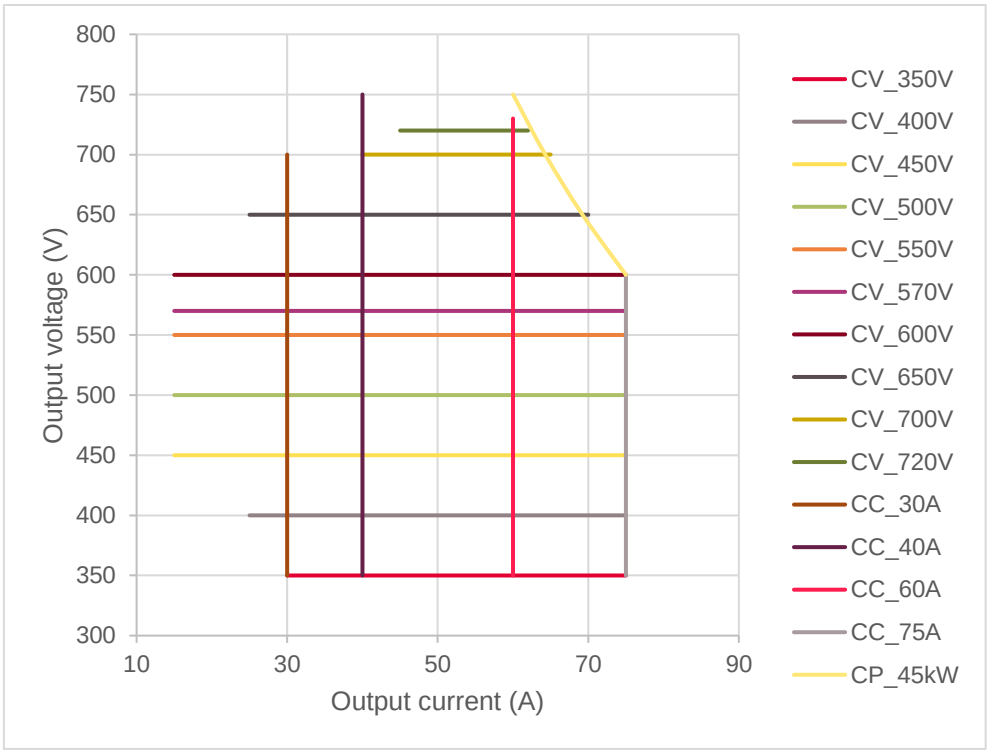


Figure 34 Operation chart for G2V mode

Figure 34 shows the operation chart for the Infineon DC EV charger demonstration system. Only the points in the chart have been tested and verified. The chart shows that with the current state of the loop regulation, the converter could not be operated without a load. The minimum load required for the different modes of operation can also be seen in the chart. At some points, the converter could reach the maximum power of 50 kW, however, the DC-link voltage will slightly deviate from the values given in control.

Efficiency variation for different loads at 570 V output voltage can be seen in Figure 35.

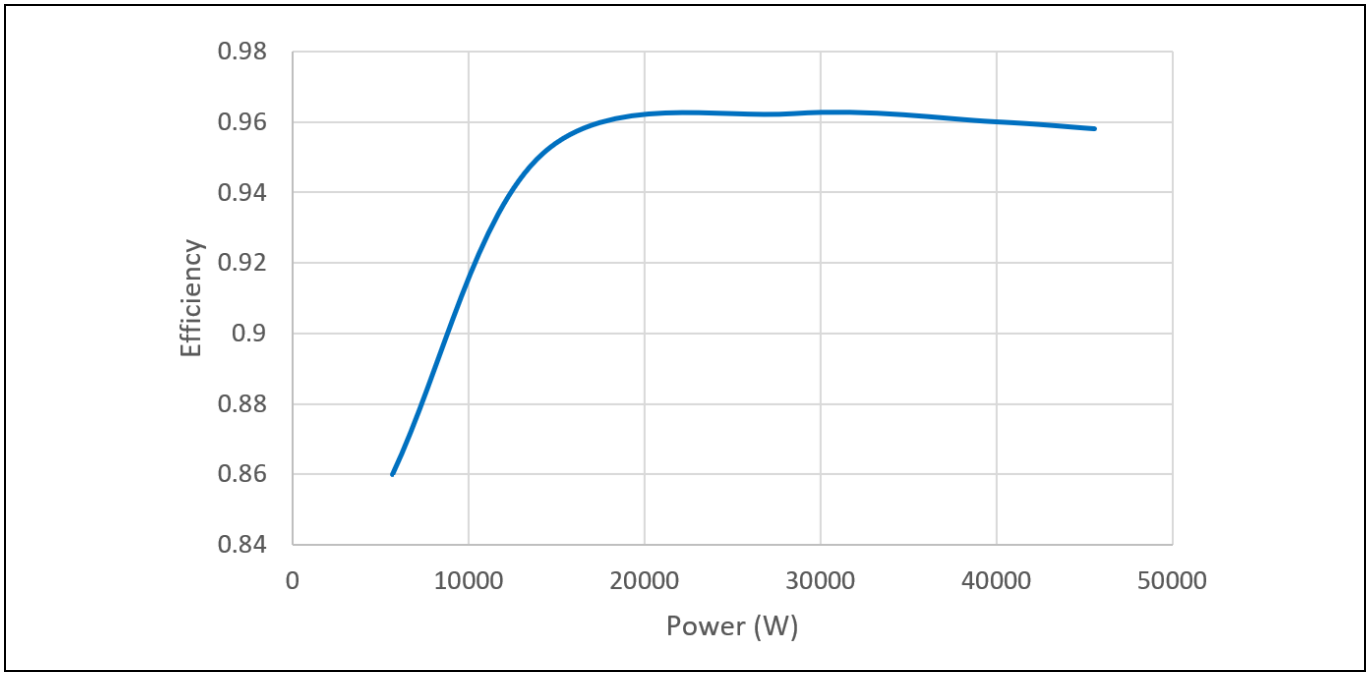


Figure 35 Efficiency variation over different load points

5.2 Test equipment

Table 14 Test equipment used for measurements on the EV charger demonstration system

Purpose		Item
Supply		3-phase grid connection (400 $V_{LL\text{-}rms}$, 50 Hz)
Load		2 x 30 kW EA-PSB 12000-40 programmable bi*directional DC power supply (resistive load mode)
Measurements	Power quality	ZIMMER precision power analyzer LMG670
	Oscilloscope	Tektronix 5 SERIES mixed signal oscilloscope

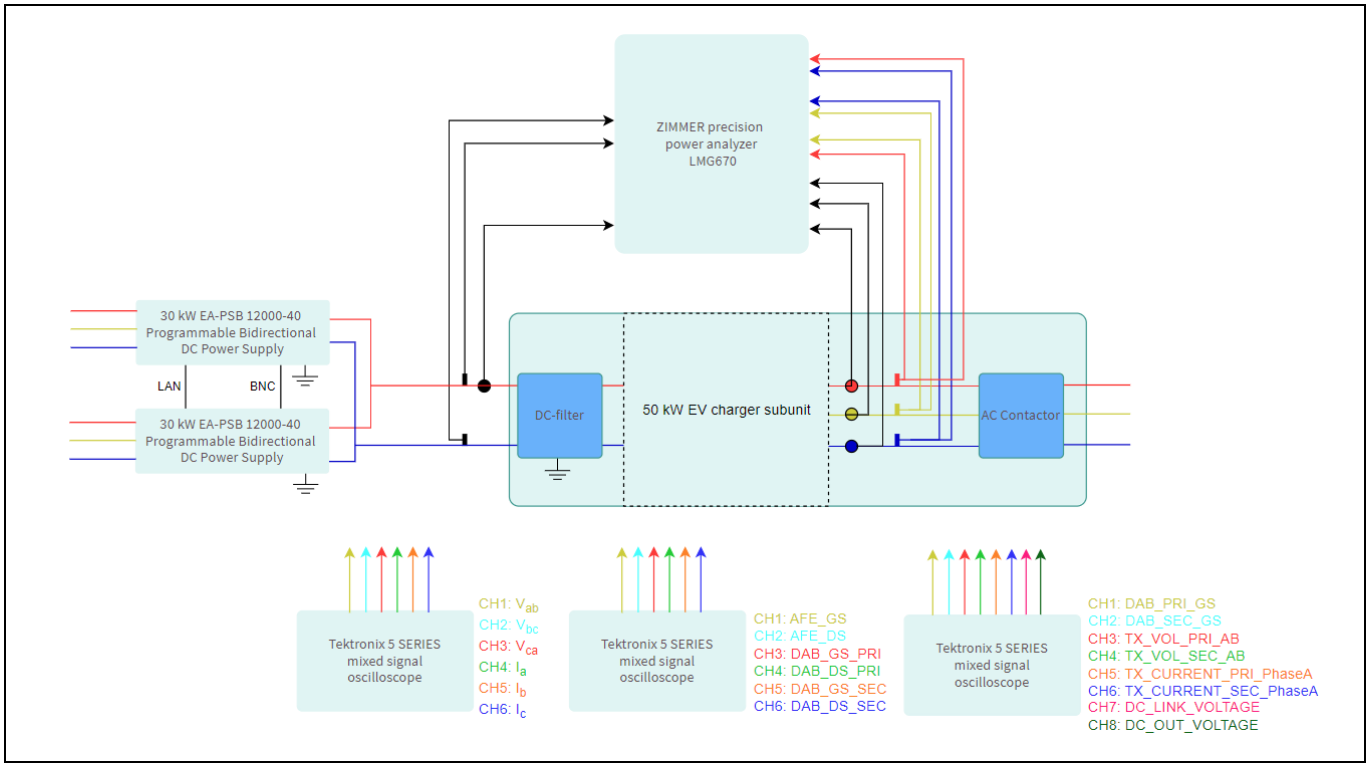


Figure 36 Test setup

5.3 Measurements

Table 15 Measurement signals

Signal	Description
AFE_GS	Vgs signal for one of the FETs on the AFE board
AFE_DS	Vds signal for the same FET on AFE board
DAB_DS_PRI	Vds signal for one of the FETs on DAB primary board
DAB_GS_PRI	Vgs signal for the same FET on the AFE board
DAB_DS_SEC	Vds signal for one of the FETs on DAB secondary board
DAB_GS_SEC	Vgs signal for the same FET on DAB secondary board
TX_VOL_PRI_AB	Voltage on the primary side of the transformer between the phases a and b
TX_VOL_SEC_AB	Voltage on the secondary side of the transformer between the phases a and b
TX_CURRENT_PRI_PhaseA	Transformer phase a current on the primary side
TX_CURRENT_SEC_PhaseA	Transformer phase a current on the secondary side

DC_LINK_VOLTAGE	Voltage on the DC-link between AFE and DAB
DC_OUT_VOLTAGE	DAB output voltage

5.3.1 G2V-CV mode: P_{out} = 45 kW, V_{in} = 400 V_{LL_rms}, V_o= 600 V

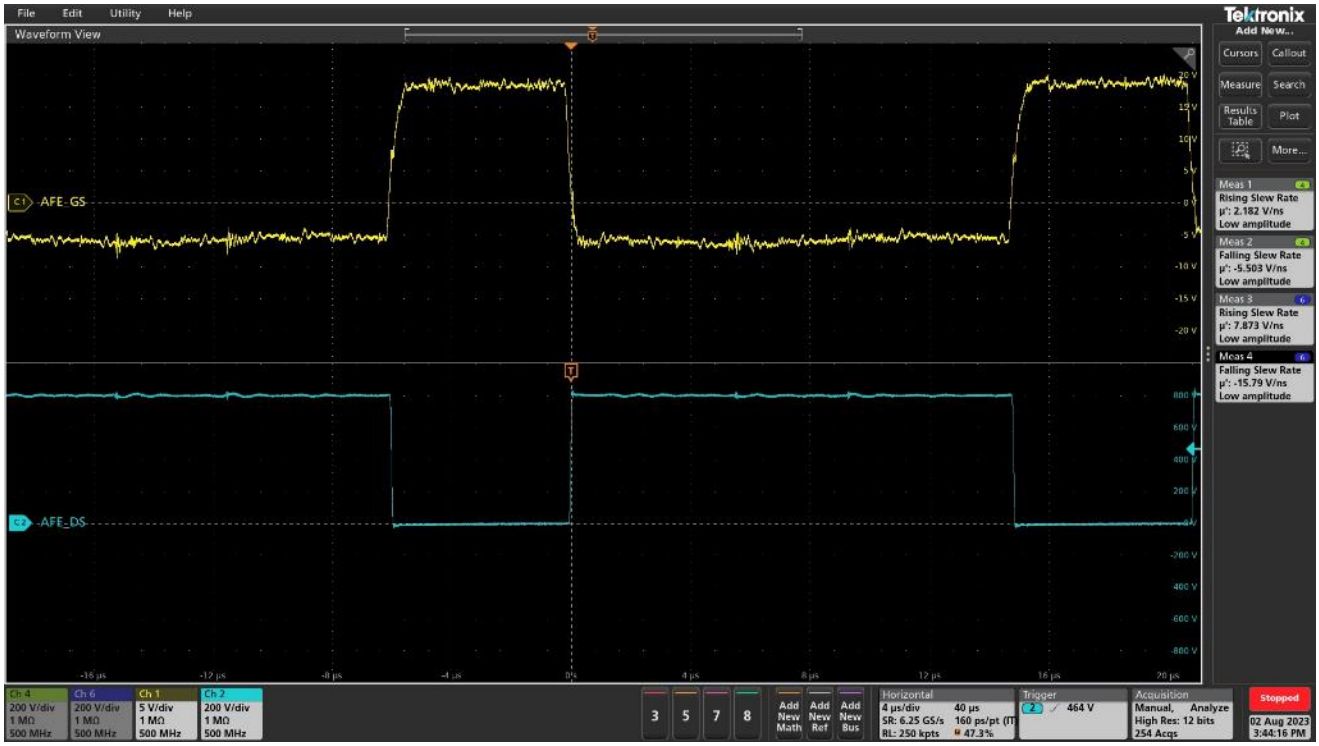


Figure 37 V_{gs} and V_{ds} waveforms for AFE at 600 V and 45 kW

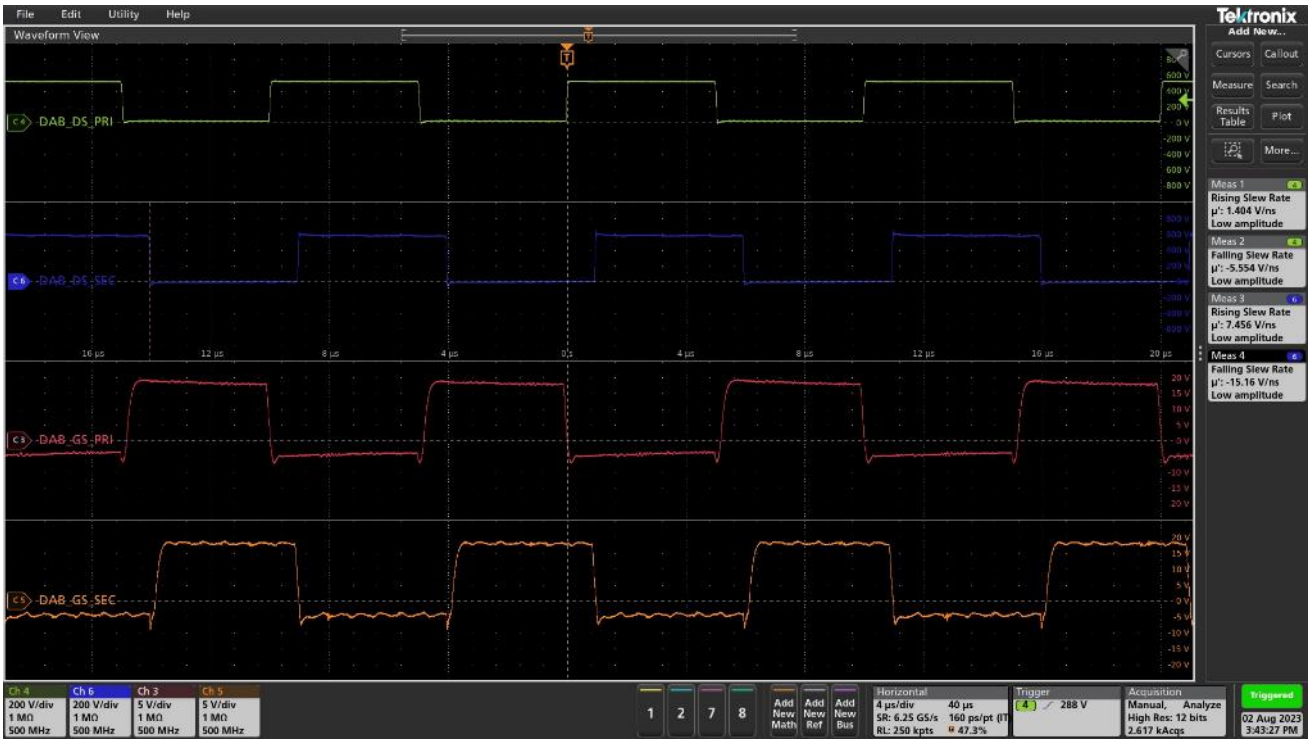


Figure 38 V_{gs} and V_{ds} waveforms for DAB at 600 V and 45 kW

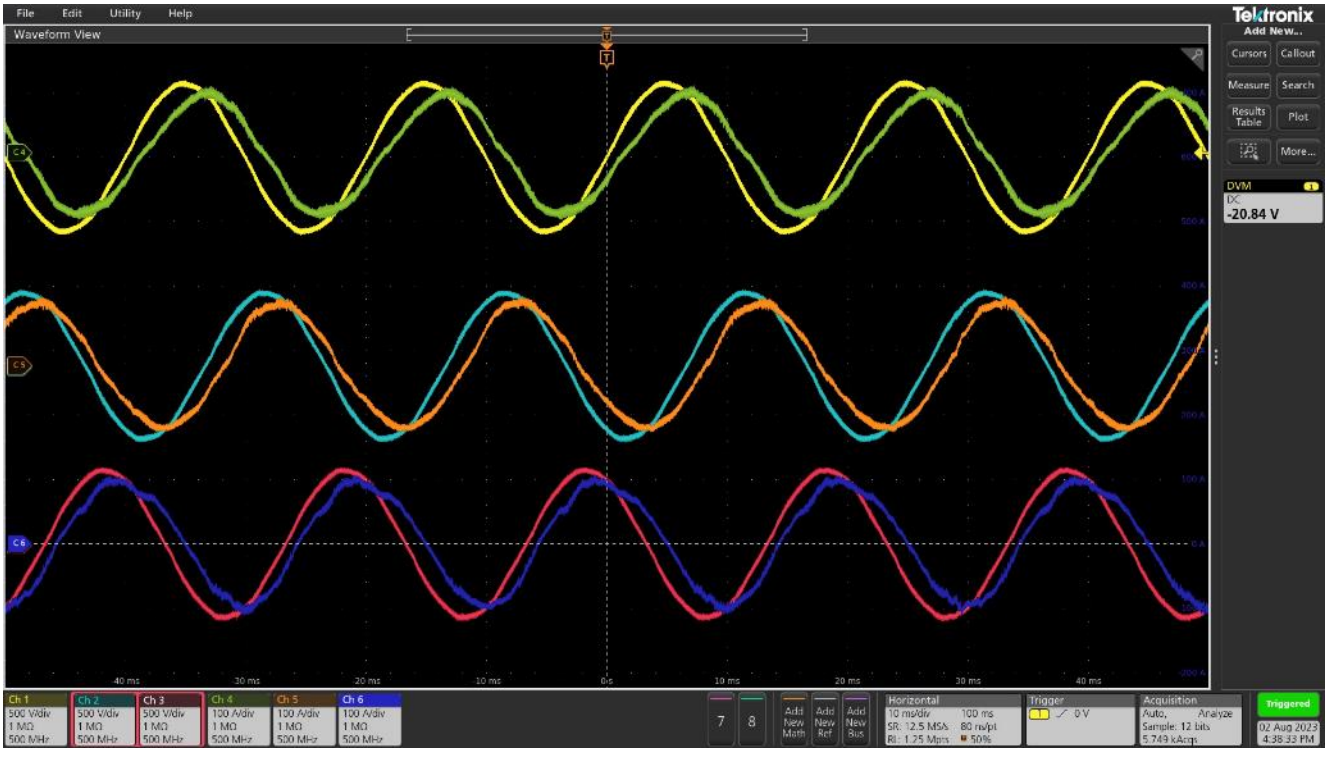


Figure 39 Input line-to-line voltages and currents at 600 V and 45 kW

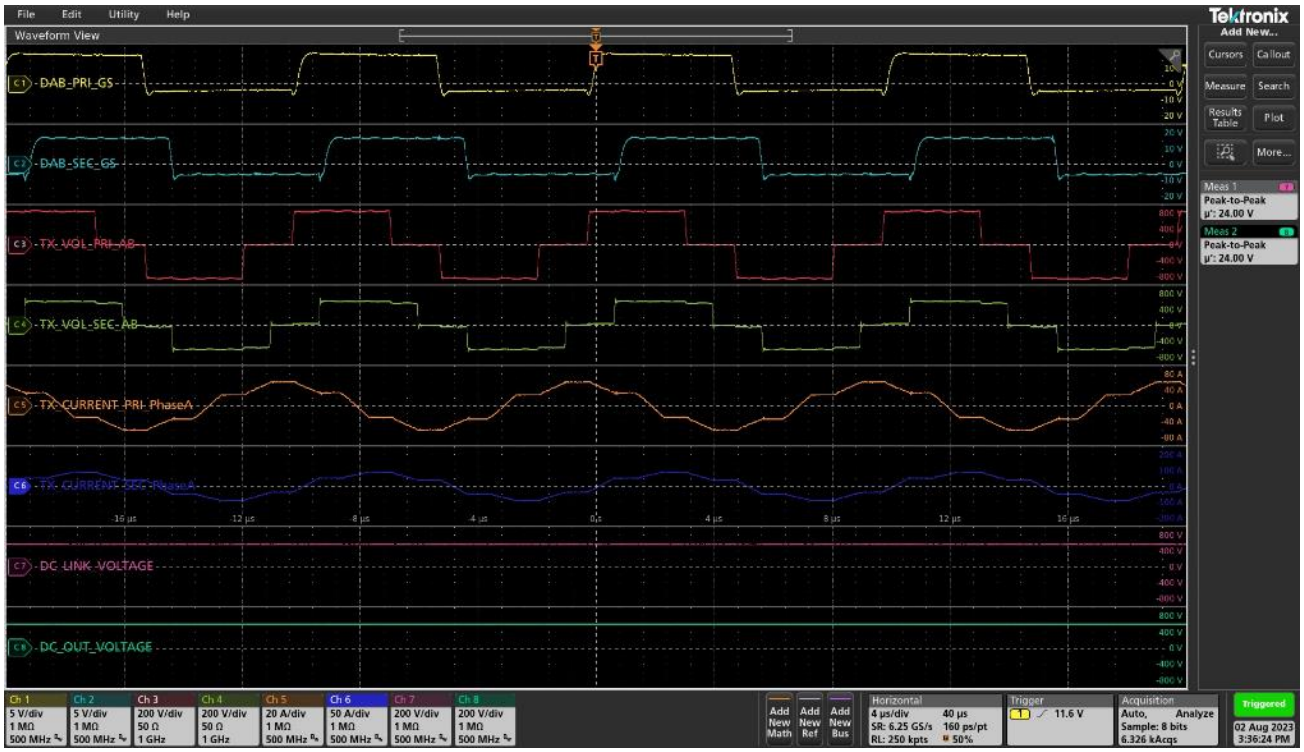


Figure 40 DAB waveforms at 600 V and 45 kW

5.3.2 G2V-CC mode: V_{in} = 400 V_{LL_rms}, V_o= 600 V , I_o= 75 A

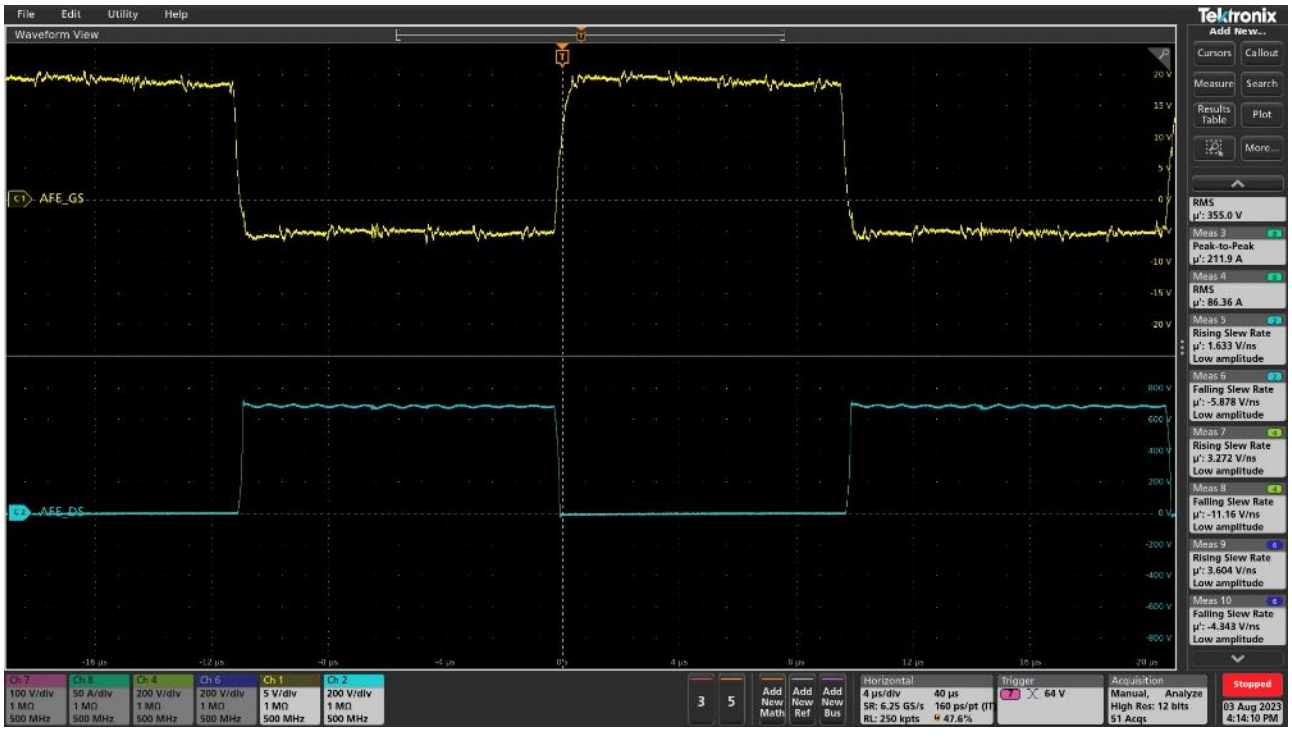


Figure 41 V_{gs} and V_{ds} waveforms for AFE at 350 V and 75 A



Figure 42 V_{gs} and V_{ds} waveforms for DAB at 350 V and 75 A

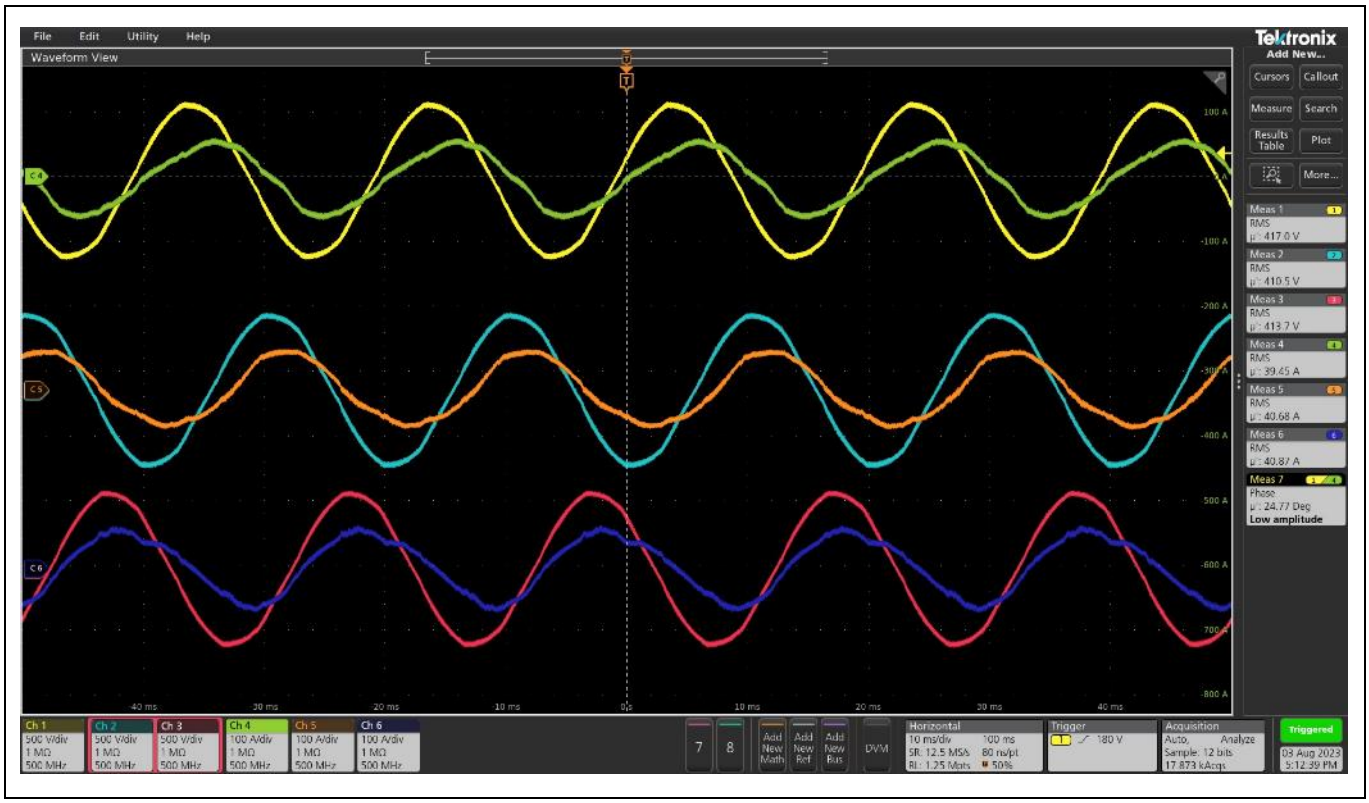


Figure 43 Input line-to-line voltages and currents at 350 V and 75 A



Figure 44 DAB waveforms at 350 V and 75 A

5.3.3 Voltage ripple: G2V-CP mode: P_{out} = 45 kW, V_{in} = 400 V_{LL_rms}, V_o= 570 V

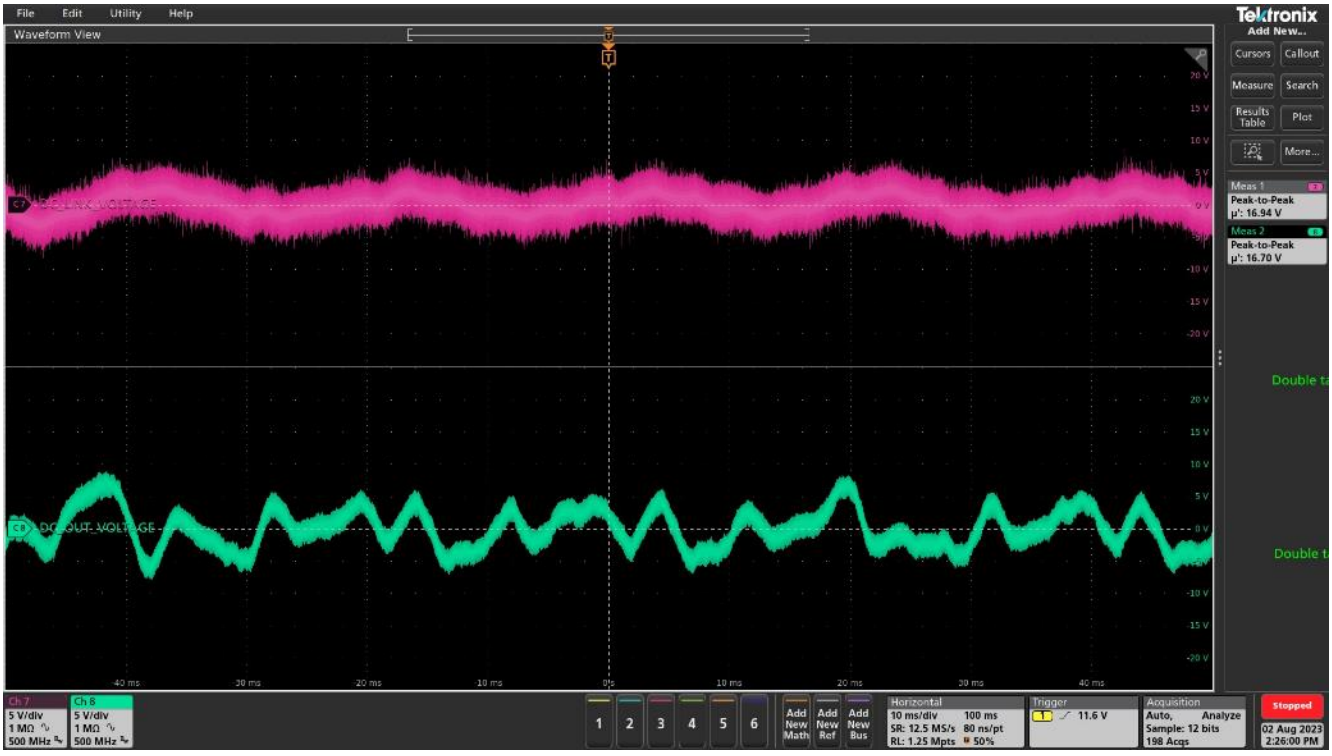


Figure 45 DC-link and output voltage ripple at 570 V and 45 kW

5.3.1 V2G (Reverse mode): P_{out} = 45 kW, V_{in} = 600 V



Figure 46 DAB waveforms in reverse mode at 45 kW

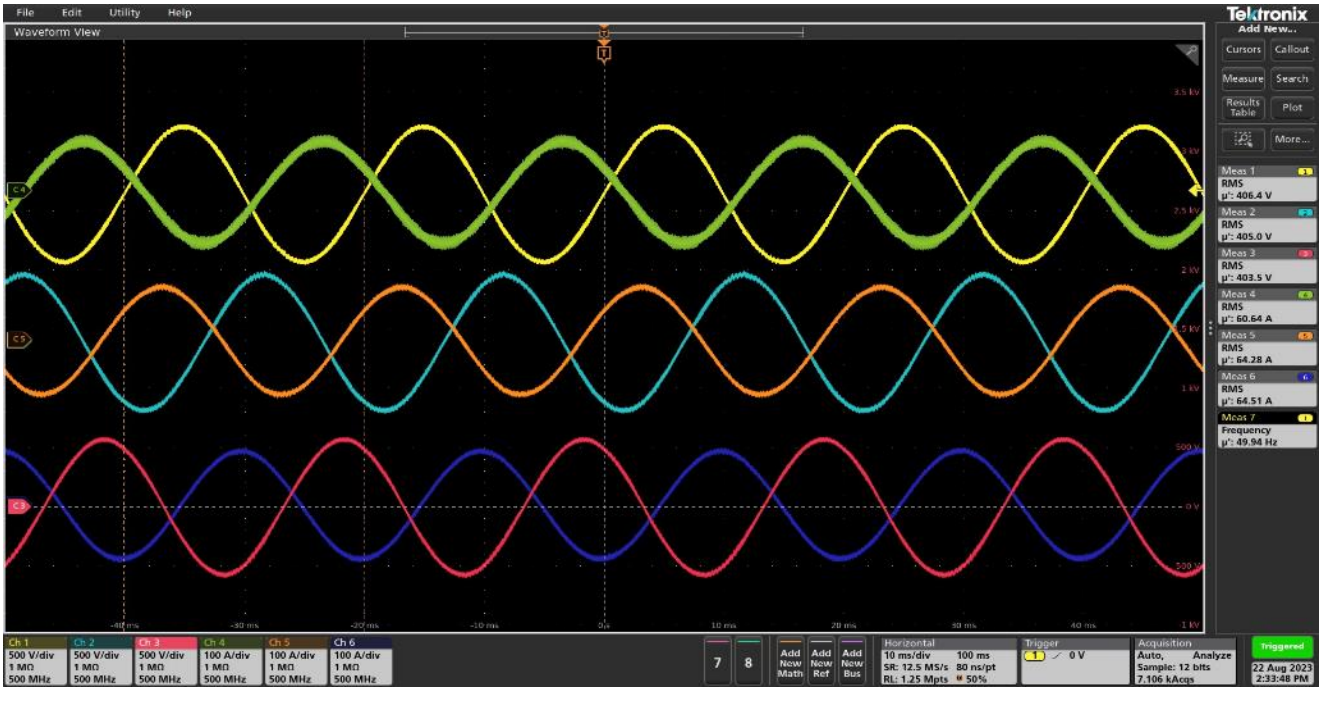


Figure 47 Output line-to-line voltages and currents in reverse mode

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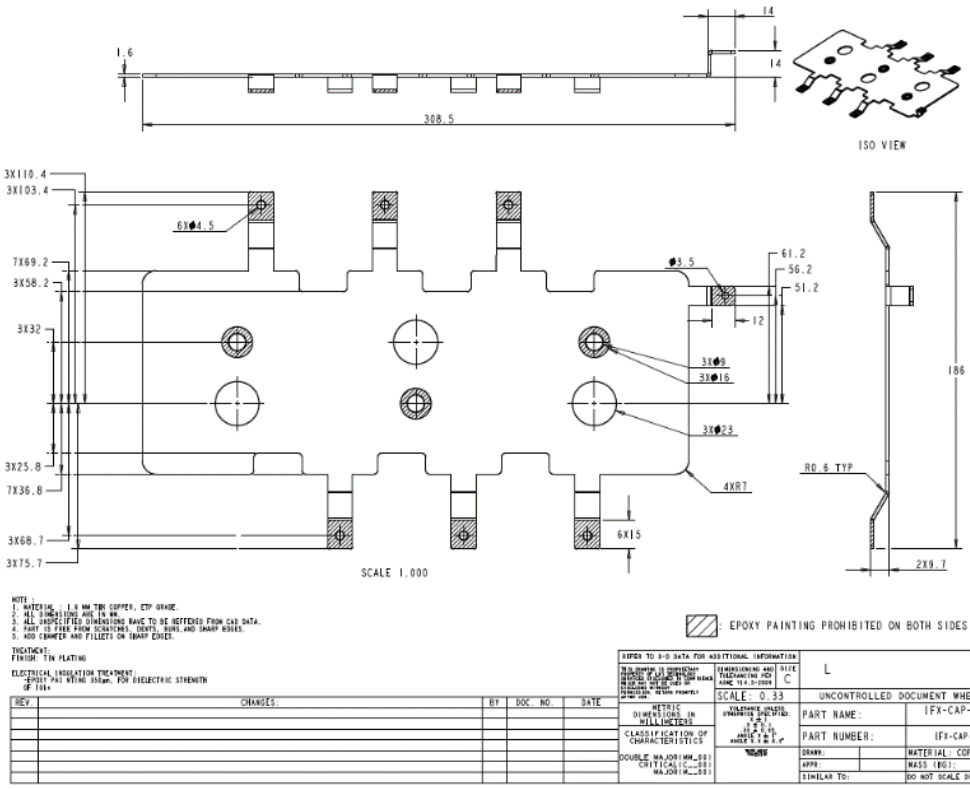
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7 Appendix


ISO VIEW
SCALE 1.000
EPOXY PAINTING PROHIBITED ON BOTH SIDES (MASKING)
UNCONTROLLED DOCUMENT WHEN PRINTED
PART NAME: IFX-CAP-8_8-P4140
PART NUMBER: IFX-CAP-8_8-P4140
MATERIAL: COPPER
DO NOT SCALE DRAWING

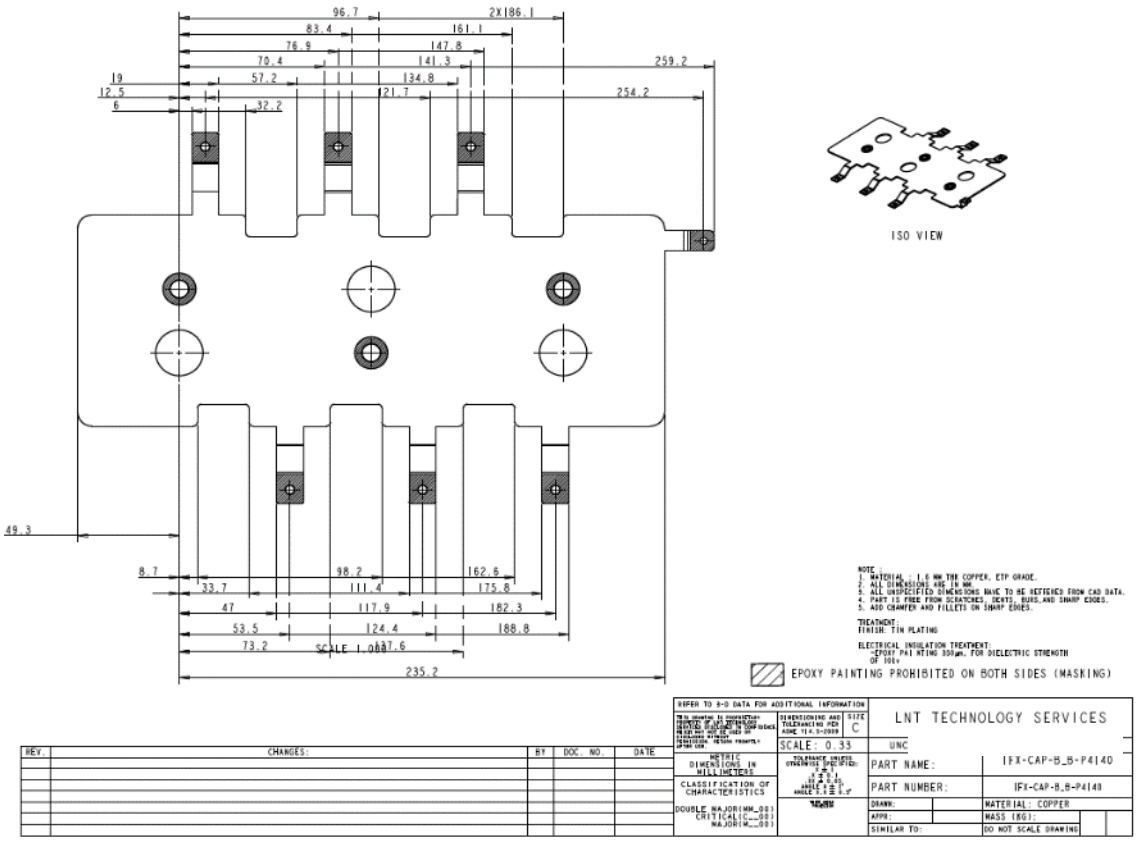

ISO VIEW
SCALE 1.000
EPOXY PAINTING PROHIBITED ON BOTH SIDES (MASKING)
LNT TECHNOLOGY SERVICES
PART NAME: IFX-CAP-8_8-P4140
PART NUMBER: IFX-CAP-8_8-P4140
MATERIAL: COPPER
DO NOT SCALE DRAWING

Figure 48 First part of the busbar used for the DC-link capacitors

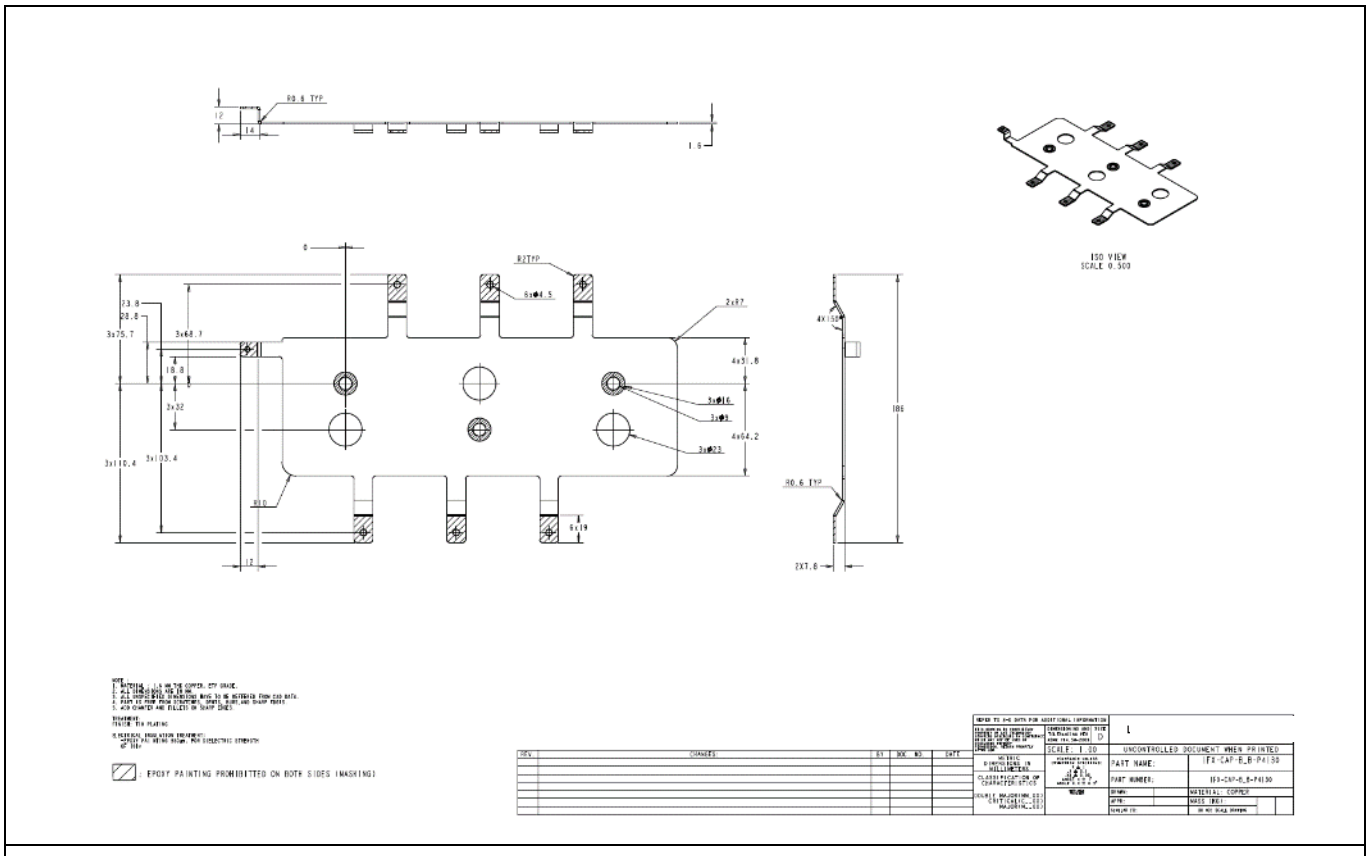
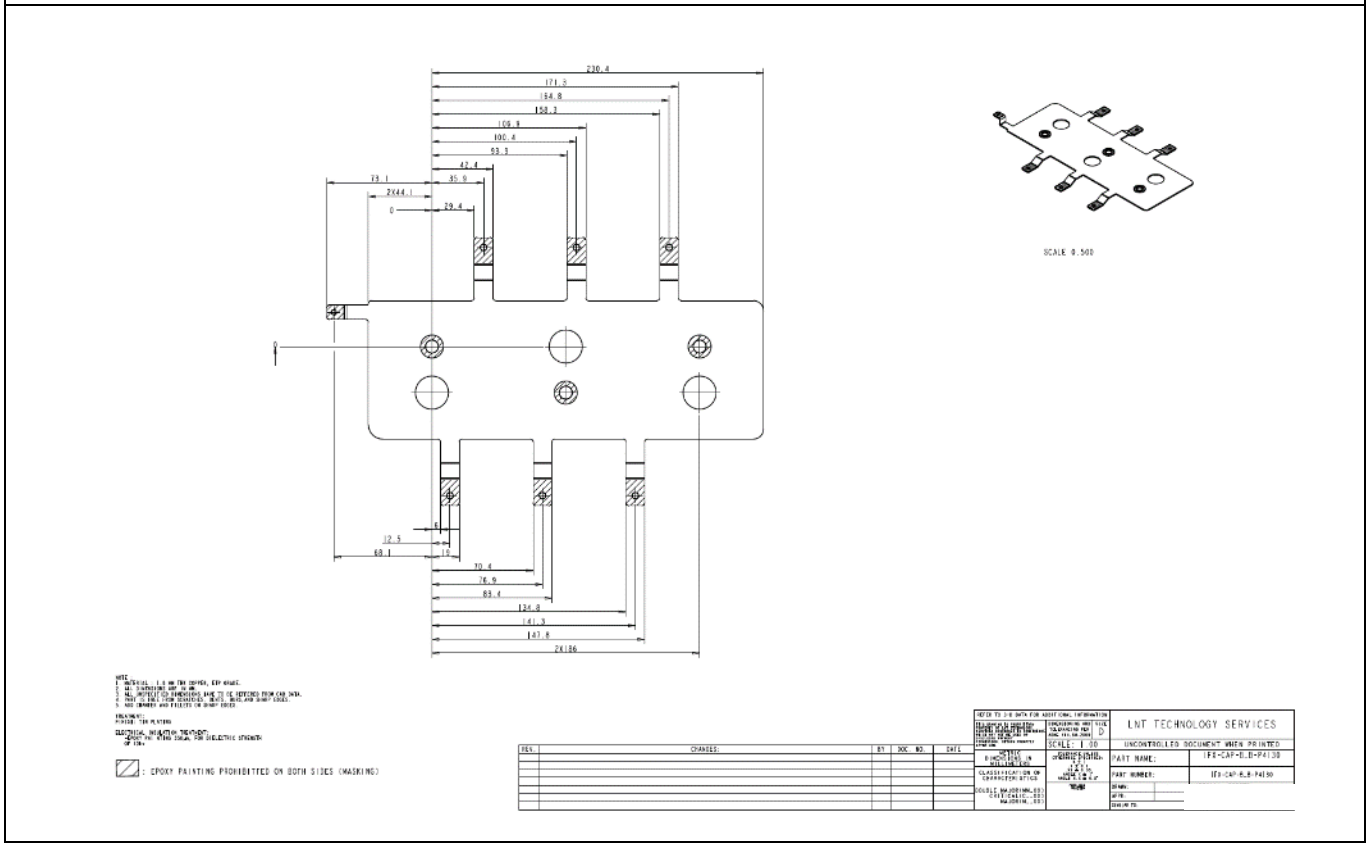


Figure 49 Second part of the busbar used for the DC-link capacitors



Revision history

Document revision	Date	Description of changes
1.0	2024-06-19	

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