400 W solar optimizer REF_4SBB_OPTIMIZER Buck-Boost reference board user guide

About this document

Scope and purpose

This document introduces the Infineon's REF_4SBB_OPTIMIZER reference board intended for 400 W buck-boost solar optimizers, including the hardware design, loss analysis, the maximum power point tracking (MPPT) software, and testing results. The newest OptiMOS™ 6 power MOSFET is used to yield in highest efficiency.

Solar optimizers are installed with solar panels, maximizing the energy from each panel and overcome the shading issue. In the residential/commercial solar system, the output of the optimizers are connected in series to build the DC link for string inverters. Solar optimizers are also used in portable energy storage, solar lightening, EV solar roof, and satellite power supply. The topology is typically buck or buck-boost.

Intended audience

The intended audience for this document are design engineers, technicians, and developers of electronic systems.

Infineon components featured

- OptiMOS™ 6 ISC056N08NM6 (Power MOSFET, 80 V, 5.6 mΩ)
- EiceDRIVER™ 2EDL8034G4B (Dual-channel junction-isolated gate driver IC)
- XMC™ XMC1302-Q040X0200 AB (32-bit microcontroller Arm® Cortex®-M0)
- OPTIREG™ TLS202A1MBV (Adjustable linear voltage post regulator)

Reference Board/Kit

Product(s) embedded on a PCB with a focus on specific applications and defined use cases that may include software. PCB and auxiliary circuits are optimized for the requirements of the target application.

Note: Boards do not necessarily meet safety, EMI, quality standards (for example UL, CE) requirements.

Important notice

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Safety precautions

Note: *Please note the following warnings regarding the hazards associated with development systems*

Table 1 Safety precautions

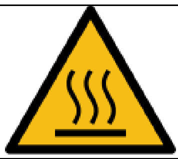
	**Warning:** *The DC link potential of this board is up to 1000 VDC. When measuring voltage waveforms by oscilloscope, high voltage differential probes must be used. Failure to do so may result in personal injury or death.*
	**Warning**: *The evaluation or reference board contains DC bus capacitors which take time to discharge after removal of the main supply. Before working on the drive system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *The evaluation or reference board is connected to the grid input during testing. Hence, high-voltage differential probes must be used when measuring voltage waveforms by oscilloscope. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Warning:** *Remove or disconnect power from the drive before you disconnect or reconnect wires, or perform maintenance work. Wait five minutes after removing power to discharge the bus capacitors. Do not attempt to service the drive until the bus capacitors have discharged to zero. Failure to do so may result in personal injury or death.*
	**Caution:** *The heat sink and device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *Only personnel familiar with the drive, power electronics and associated machinery should plan, install, commission and subsequently service the system. Failure to comply may result in personal injury and/or equipment damage.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*
	**Caution:** *A drive that is incorrectly applied or installed can lead to component damage or reduction in product lifetime. Wiring or application errors such as undersizing the motor, supplying an incorrect or inadequate AC supply, or excessive ambient temperatures may result in system malfunction.*
	**Caution:** *The evaluation or reference board is shipped with packing materials that need to be removed prior to installation. Failure to remove all packing materials that are unnecessary for system installation may result in overheating or abnormal operating conditions.*

Table of contents

1 The board at a glance

Solar optimizers, often referred to as power optimizers, are small electronic devices that play a significant role in the renewable energy sphere, particularly in the field of photovoltaic (PV) solar power systems. They enhance and optimize the performance of individual solar panels, thus maximizing the overall energy production of the solar power system.

Solar optimizers are connected to each solar panel in a PV system and installed at the site of the solar panel, usually on the back of the panel or integrated into its frame. They regulate the DC electricity output from each solar panel, converting it into a more efficient form that can then be used or stored. Additionally, they minimize the losses in energy output that can occur due to various factors, such as shading, dust, or misalignment of solar panels. They achieve this by individually tuning the output from each solar panel to ensure that all panels in the system produce their maximum possible power.

Solar optimizers utilize Maximum Power Point Tracking (MPPT) technology. MPPT continuously adjusts the voltage and current levels to find the maximum power output under any given set of conditions. This enables each solar panel to operate at its highest efficiency, regardless of what other panels in the system are doing. This is particularly helpful in situations where some panels may be shaded or operating under different conditions than others.

By allowing each panel to perform at its best, solar optimizers can significantly increase the overall efficiency and output of a solar power system. They also enable more flexible system design, as panels can be installed in different orientations and angles without adversely affecting the system's overall performance. Moreover, solar optimizers can provide detailed monitoring of each panel's performance, helping to quickly identify and address any issues.

Solar optimizers are sometimes compared to microinverters, another technology used to enhance solar system performance. While both serve to optimize power output, they operate differently. Unlike microinverters, which convert DC power to AC at each panel, solar optimizers simply condition the DC power before sending it to a central inverter. This approach generally results in a lower system cost and higher efficiency.

Infineon's REF_4SBB_OPTIMIZER is a reference design for a buck-boost optimizer that utilizes a buck converter to step down the input voltage from the solar panel to a lower output voltage. The main components of the reference board are listed in Figure 1.

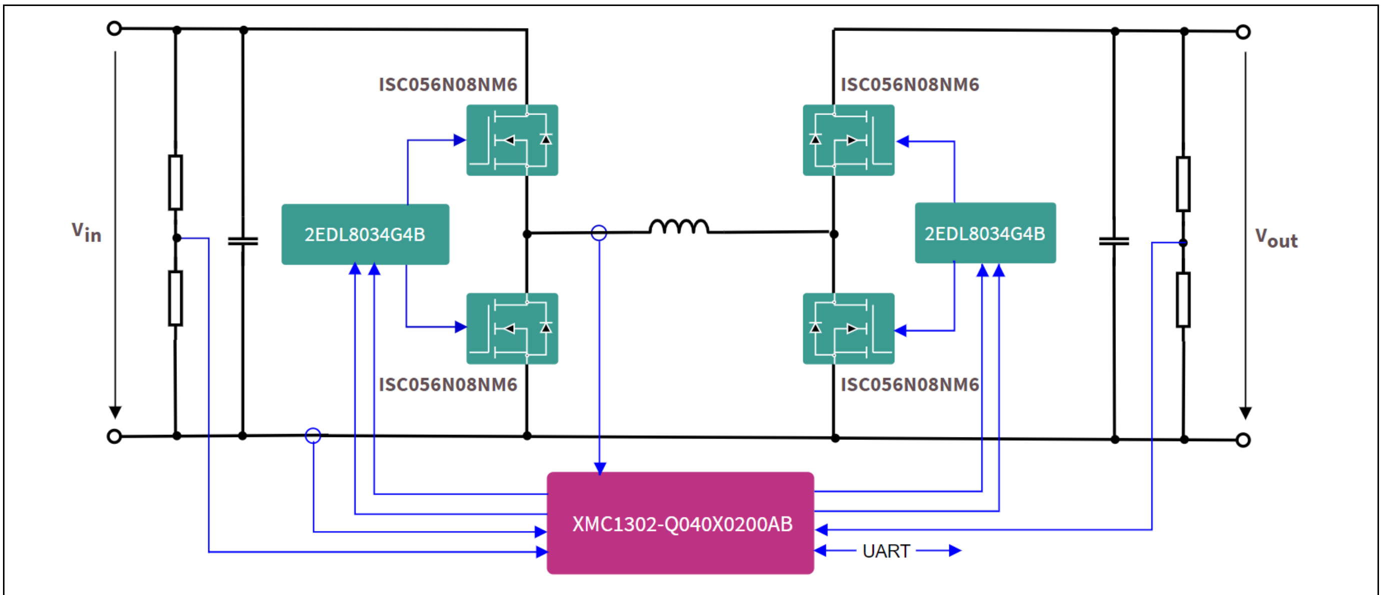


Figure 1 REF_4SBB_OPTIMIZER reference board block diagram

2 REF_4SBB_OPTIMIZER reference board design

Figure 2 shows the setup of the reference design. This section details the converter design for the buck-boost optimizer. Table 2 lists the board parameters.

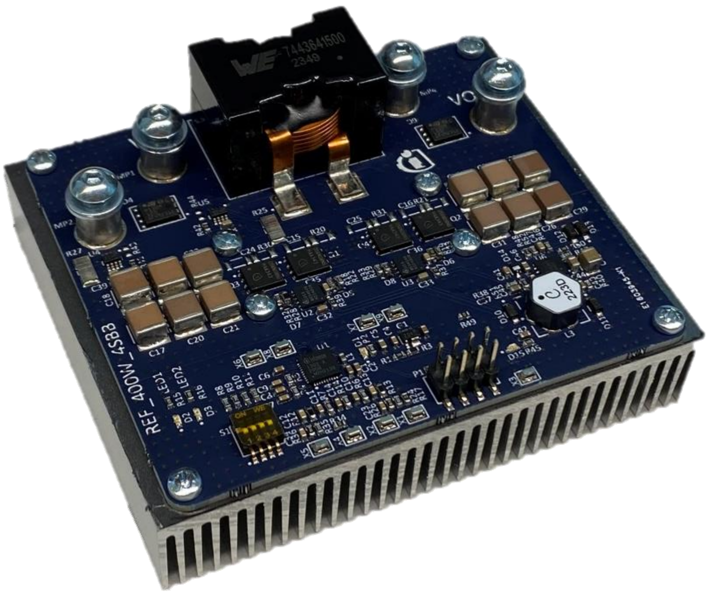


Figure 2 REF_4SBB_OPTIMIZER reference board

Table 2 REF_4SBB_OPTIMIZER reference board parameters

Parameters	Value
Maximum input power	400 W
Maximum input voltage	60 V
Maximum input current	15 A
MPPT voltage range	15-60 V
Switching frequency	200 kHz
Maximum efficiency	> 98%
MPPT efficiency	> 99%
Inductor current ripple	Ip-p 30% at VIN = 60, duty cycle = 75%, POUT = 400 W
Output voltage ripple	1%

2.1 Buck-boost converter

Depending on the input voltage and power level of the optimizer, different MOSFETs are used to optimize the efficiency accordingly. According to the parameters stated in Table 2, OptiMOS™ 6 ISC056N08NM6 80 V yields the lowest losses.

Depending on the EMI requirements, the switching waveforms are adapted by either using the gate resistance, capacitance, or utilizing the snubber network. The reference board uses a 15 µH inductor (744361500), which limits the ripple current to the specifications stated in Table 2.

The inductor current during slope compensation is measured via the shunt resistor (R25).

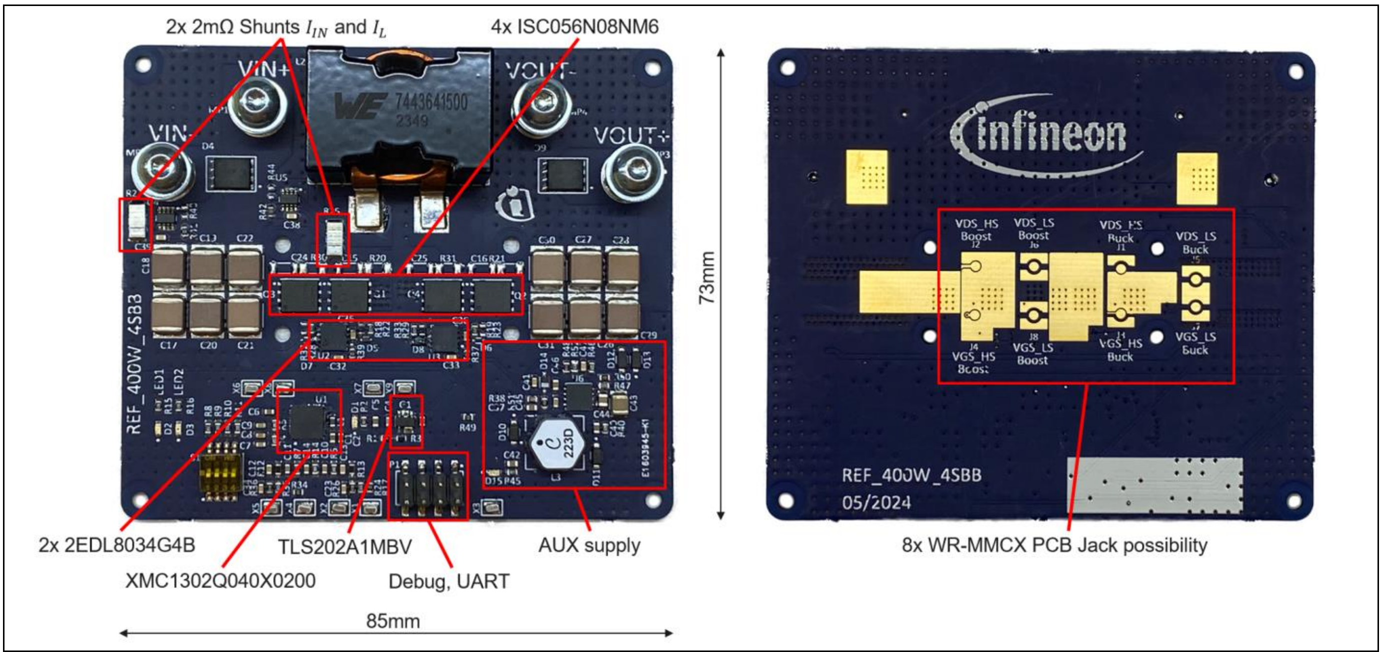


Figure 3 **600 W buck solar optimizer reference board with important sections highlighted**

The main components as listed earlier are described in Figure 3. The MMCX PCB jack connectors can be placed on the bottom side of the PCB for a proper measurement of the drain source and gate source signals.

Note: When the MMCX connectors are soldered to the board, it cannot be mounted on the heat sink.

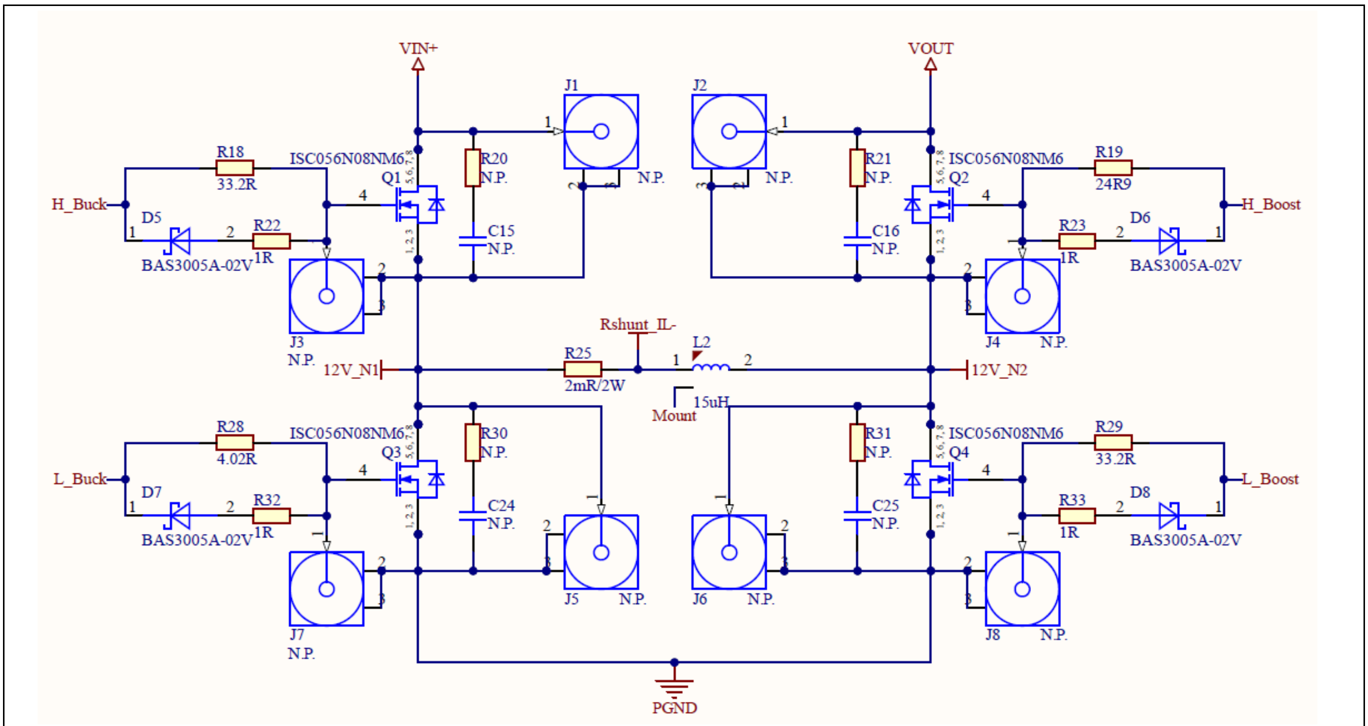


Figure 4 **Full-bridge including gate and snubber circuitry, inductor, and MMCX probe connectors**

EiceDRIVER™ 2EDL8034G4B gate driver IC drives both high-side and low-side MOSFETs in a half-bridge configuration. The IC only needs a minimum number of external components and features a 120 V integrated bootstrap diode. The power supply for the high-side MOSFET is done using an isolated buck with a 1:1:1

transformer, shown in Figure 6. Furthermore, the 12 V output from the buck converter is also utilized to generate the logic voltage for the microcontroller, as well as for the current sense amplifiers.

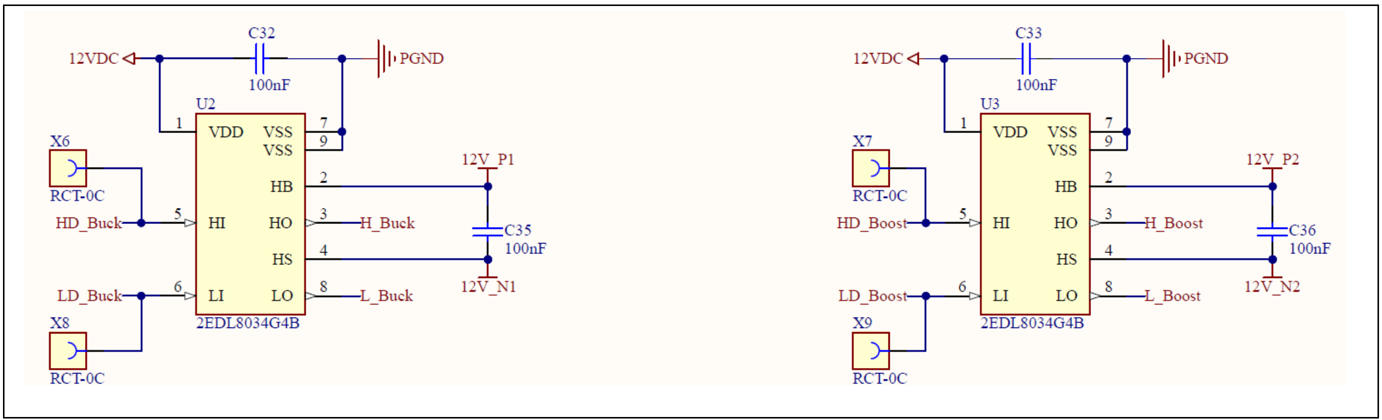


Figure 5 **Two dual gate driver with integrated bootstrap diode**

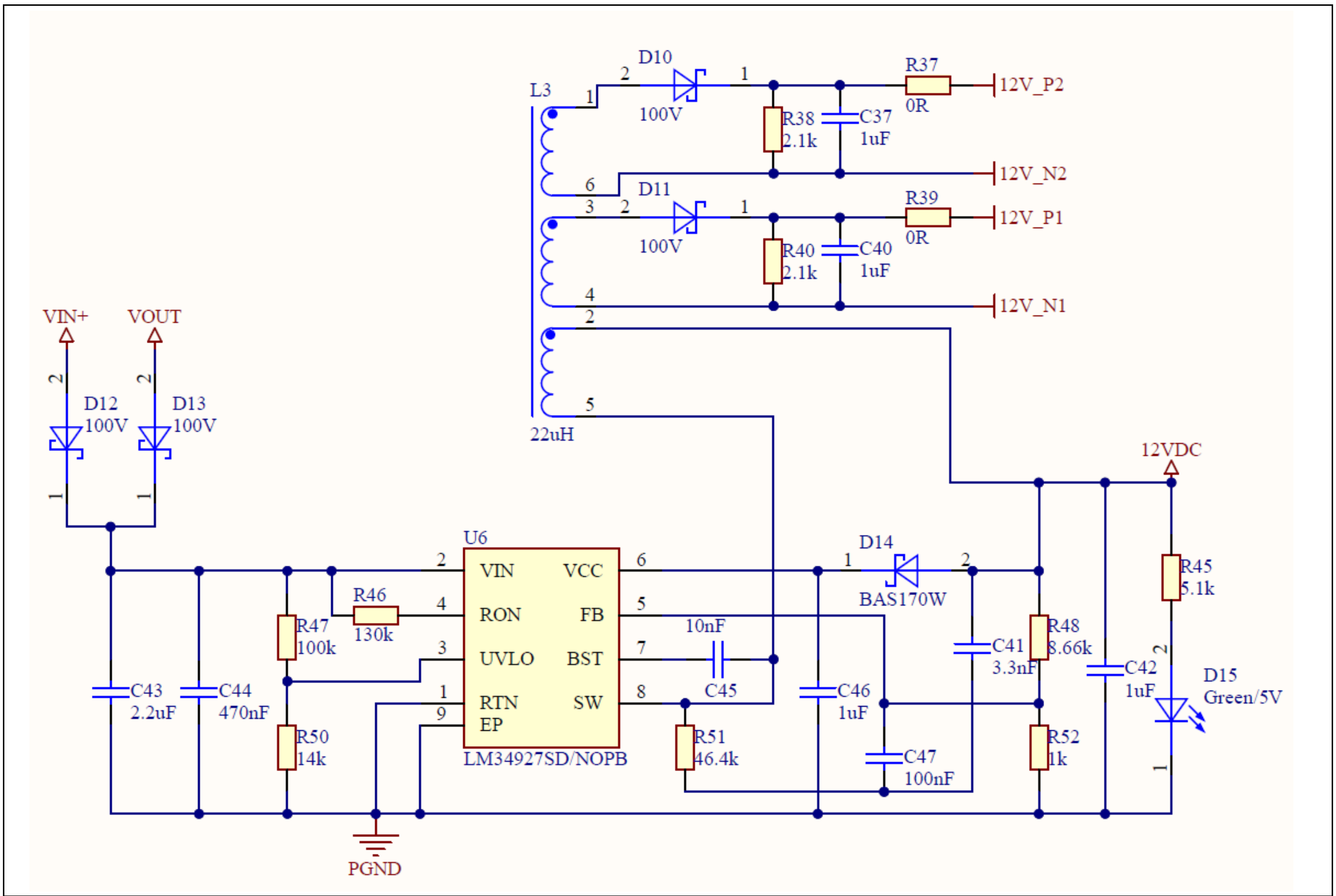


Figure 6 **Auxiliary supply with 1:1:1 transformer to ensure constant high-side driver supply**

2.2 Voltage and current measurement

The input and output voltage is measured via voltage dividers (Figure 8) and a low-pass filter. The inductor- and input current measurement is done via a current sense amplifier using an amplification of 50, shown in Figure 7.

In the default configuration, the current sense amplifiers outputs the amplified signal with an offset of 1.65 V. Therefore, it is also possible to measure the currents in the opposite direction. The amplified signal is then routed to XMC1302-Q040X0200, as shown in Figure 9. The MCU then feeds these signals into the control loop structure and operates them with a CCU8 the buck-boost converter. If the offset is not needed, R41 and R42 can be removed and R43 and R44 can be populated with a 0 Ω resistor.

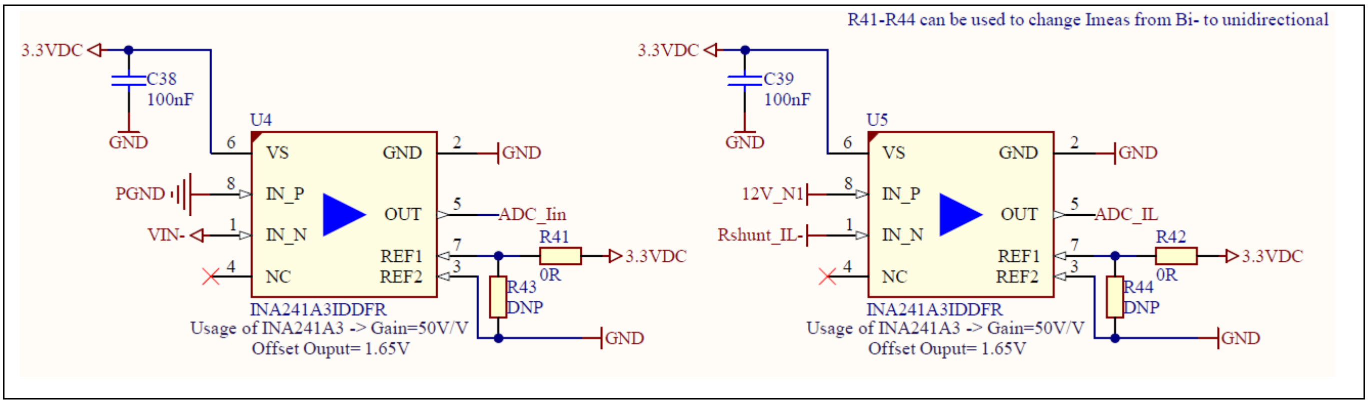


Figure 7 **Current sense amplifiers with an amplification of 50 and an offset voltage of 1.65 V**

R17 and R34 in combination with X1-X5 are used to inject a signal into the feedback loop of the buck-boost converter to tune the controller with the usage of Bode 100 from OMICRON Lab. These resistors are not required in the final design.

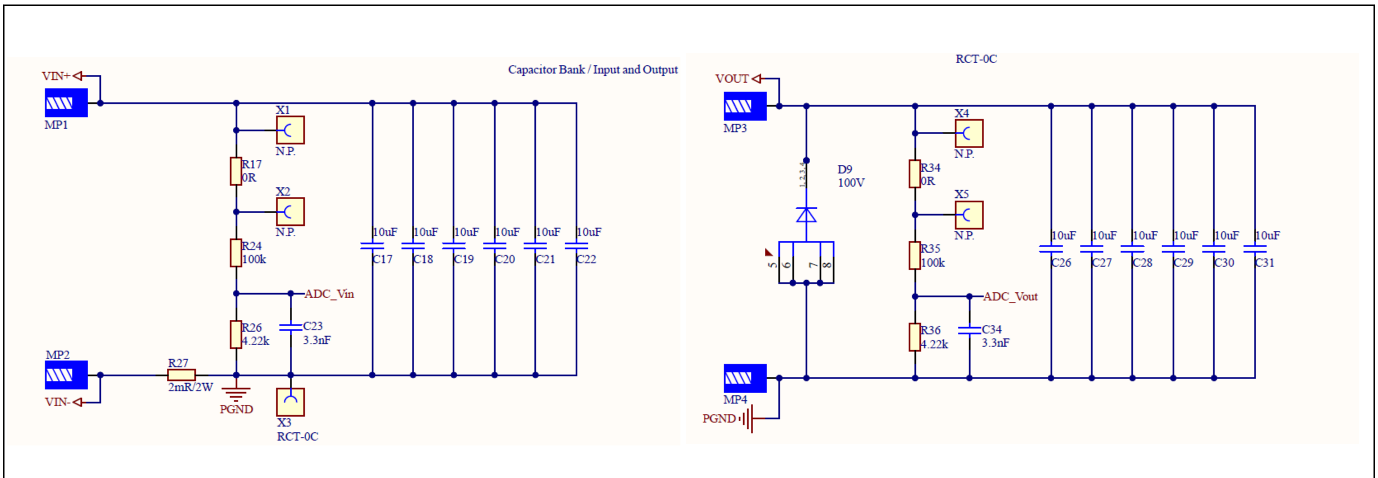


Figure 8 **Input and output terminals with the feedback voltage divider, bulk capacitors, and bypass diode**

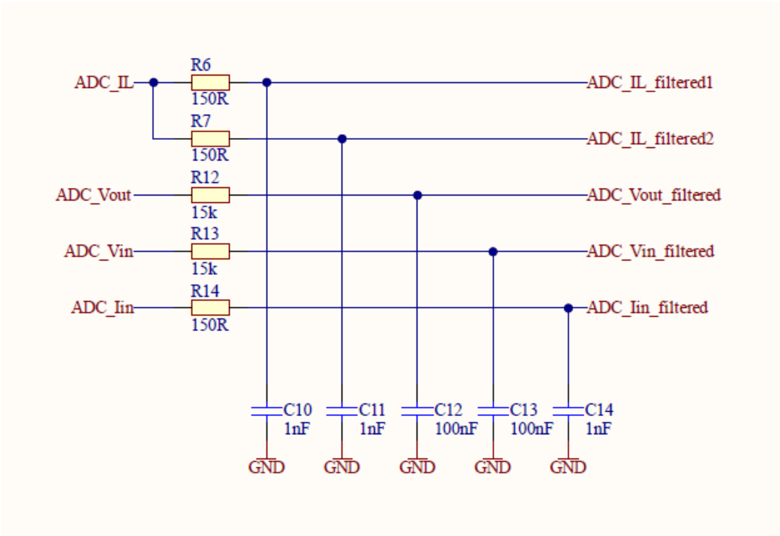


Figure 9 Low-pass filters for current and voltage feedback

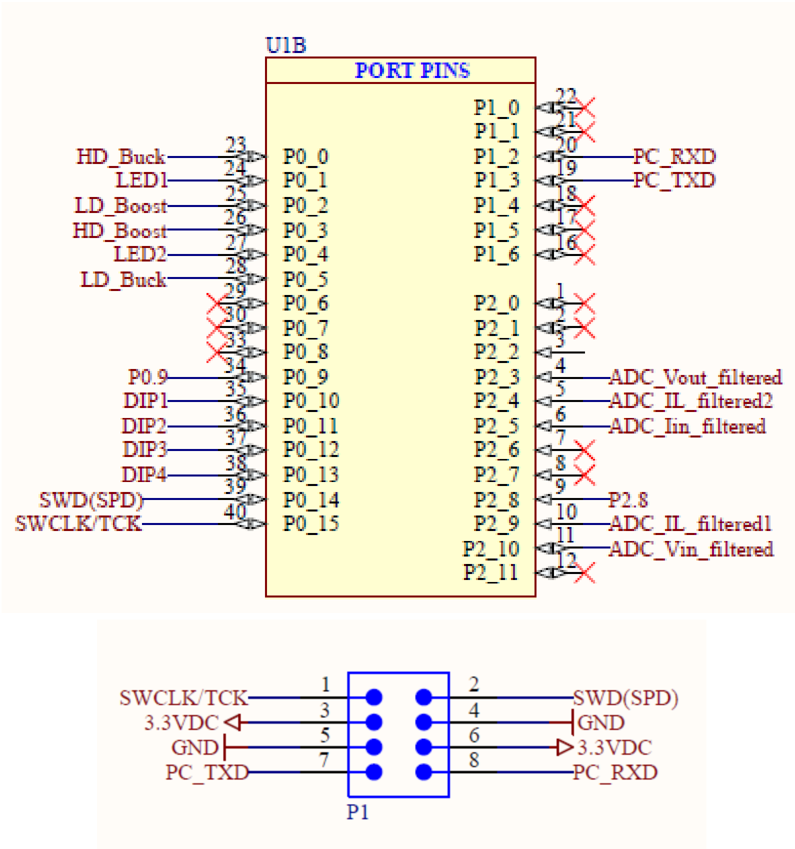


Figure 10 Microcontroller including the 8-pin debug interface

Figure 10 shows the pin assignment of the on-board microcontroller. The 8-pin connector is used to program the controller.

3 Thermal concept

The buck-boost converter board is designed to accommodate MOSFETs with a SuperSO8 5x6 footprint, offering flexibility in thermal management. This design allows for the use of SuperSO8 MOSFETs with bottom cooled or double-side cooled configurations (SuperSO8 DSC).

3.1 Thermal considerations

The thermal performance of the buck-boost converter is critical to ensure reliable operation and prevent overheating. The MOSFETs are the primary heat-generating components hence, their thermal management is crucial. The SuperSO8 footprint provides a compact design, which can lead to an increased thermal density. Therefore, a well-designed thermal management strategy is essential to dissipate heat efficiently.

The board's design foresees bottom cooled MOSFETs. In this configuration, the MOSFETs are mounted on the top side of the board and a heat sink is attached to the bottom of the board. The generated heat is transferred to the board and through the board to the heatsink. This design is suitable for applications where the converter is mounted on a metal chassis or a heat sink.

To ensure efficient heat transfer between the board and the heat sink, WE-TGS Graphite Sheet from Würth Elektronik is used as thermal interface material (TIMs). The graphite sheet has a thermal conductivity of 1800 W/(m*K).

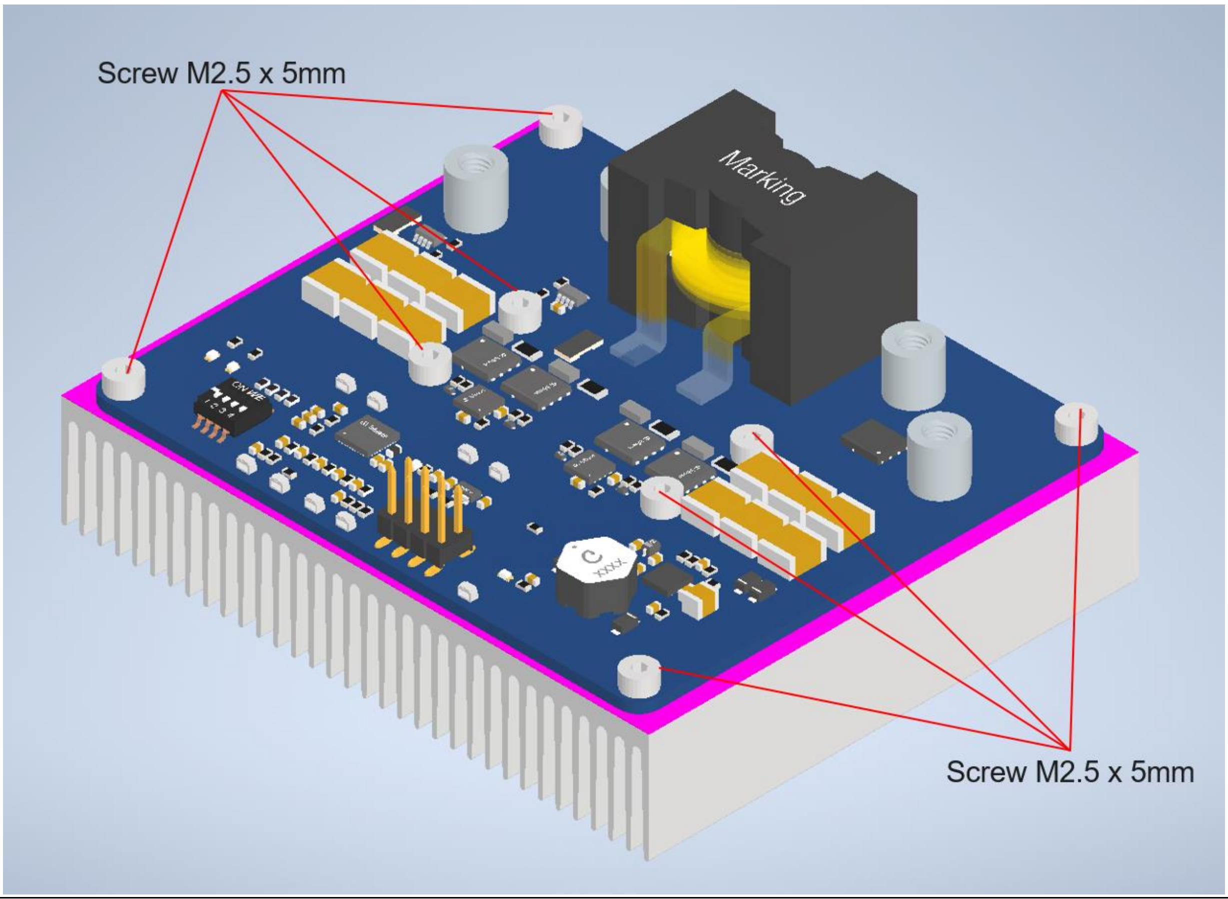


Figure 11 Heat sink assembly

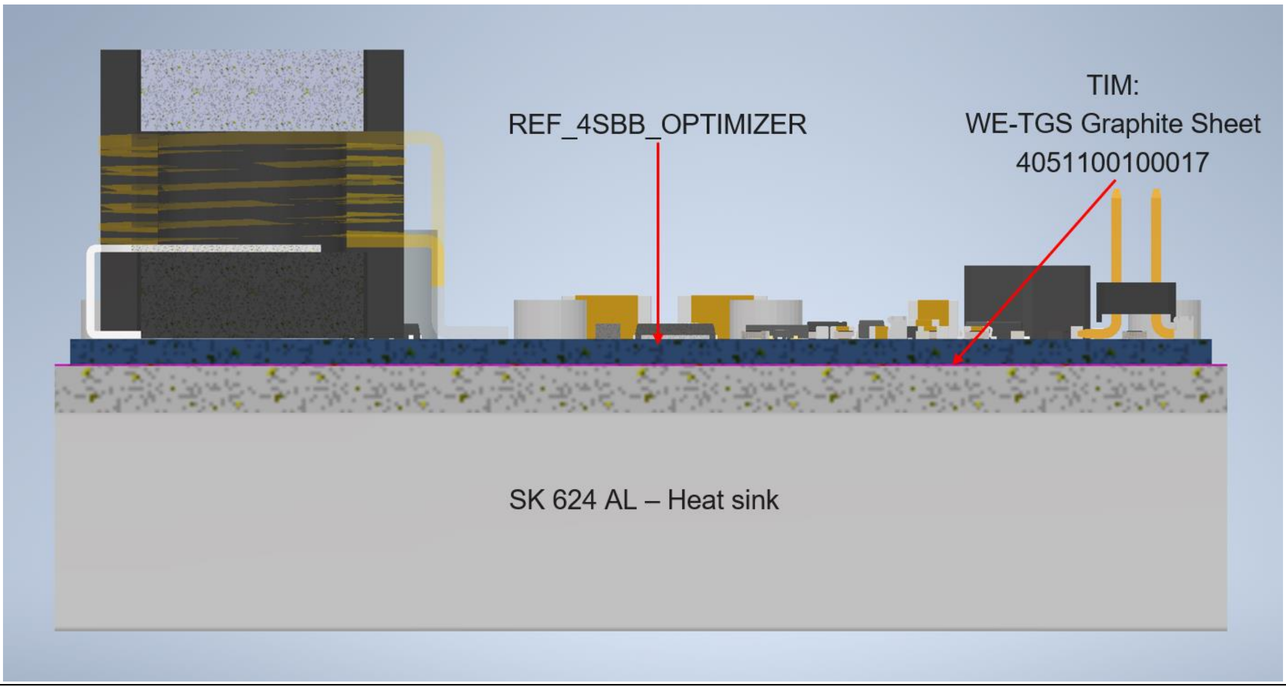


Figure 12 Cross-section view of the heat sink assembly

4 Measurements

Different factors impact the efficiency results such as the connected PV panel and its orientation and angle, and the input characteristic changes. In this section, the term 'efficiency' refers to the efficiency of the power electronics including auxiliaries. However, the latter needs to be distinguished from the MPPT efficiency, which depends on the measurement accuracy and the implemented algorithm. The combination of the above leads to the system efficiency.

4.1 Power electronics efficiency

The devices for the measurement setup are described in Table 1.

Note: As only one shunt was available, the setup has one limitation. Either the input current or the output current cannot go beyond 10 A as the Keysight 34461A is the limiting barrier.

Table 1 Measurement device description

Qty	Device	Part Number	Description
1	Power supply	62150H-1000S	80 V/18 A 650 W rating as minimum
1	Load	EA-ELR 9250-70	At least 650 W power dissipation
4	Multimeter	Keysight 34461A	Input/output current and voltage measured (10 A maximum) utilizing one 3 mΩ shunt either on input or output.
1	Shunt	YN01-07751BS000000	3 mΩ shunt either on input (boost mode) or output (buck mode)

For buck efficiency test, the duty cycle is set constant to 75% and the shunt is connected to the output. The high-side switch (Q2) is set to constant on. The input voltage is stepped from 30 V to 60 V in 10 V increments. The measurement points are taken 1 A output current apart up to either reaching the 10 A input current limit or the 400 W output power limit.

Depending on the input voltage, the efficiency curve follows a different trajectory. At lower input voltage, higher currents lead to higher conduction losses at the MOSFETs and shunts hence, the efficiency is lower. Furthermore, the higher the output power, the higher is the measured efficiency due to the lower influence of basic loads like auxiliary supply, microcontroller, and amplifier supply.

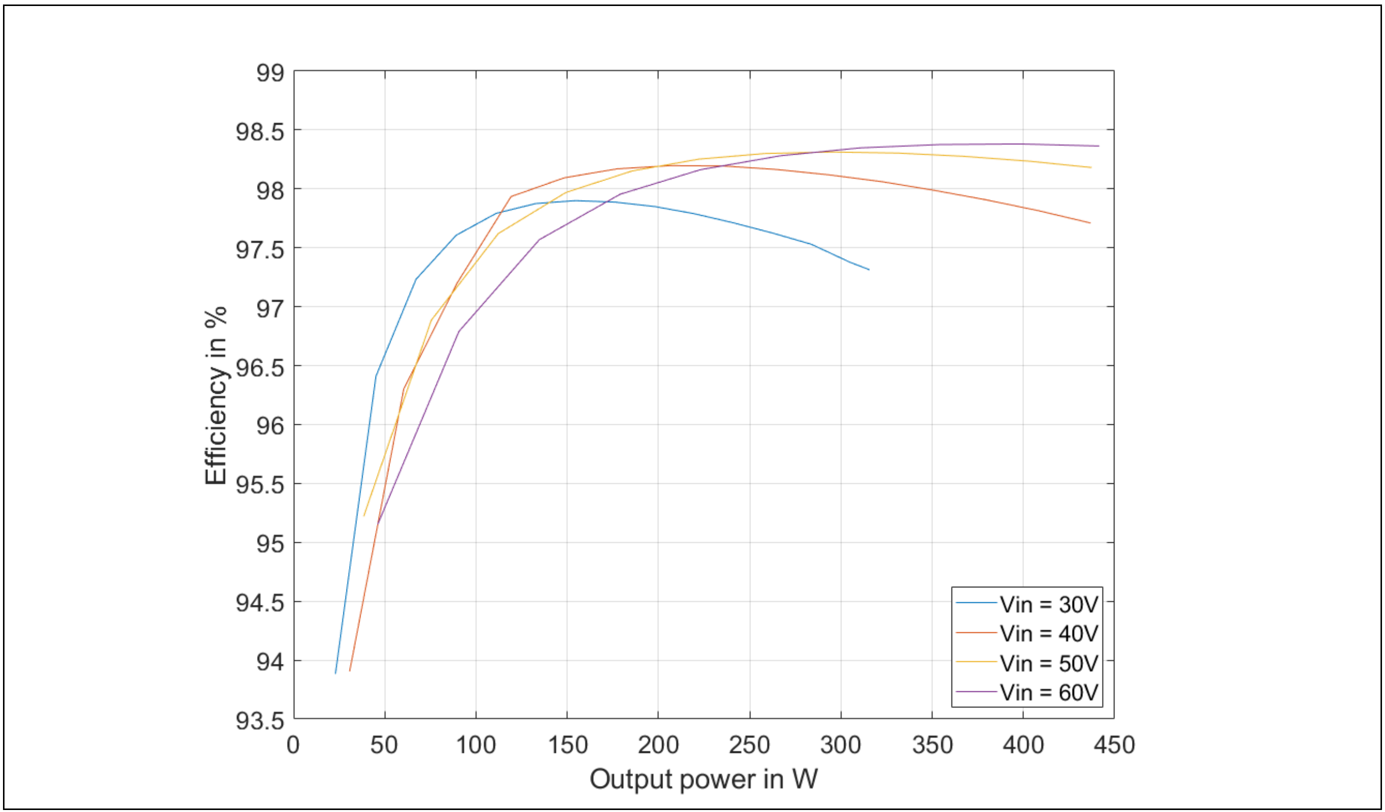


Figure 13 **Buck efficiency measurement at different input voltages at 75% duty cycle, HS boost constant on**

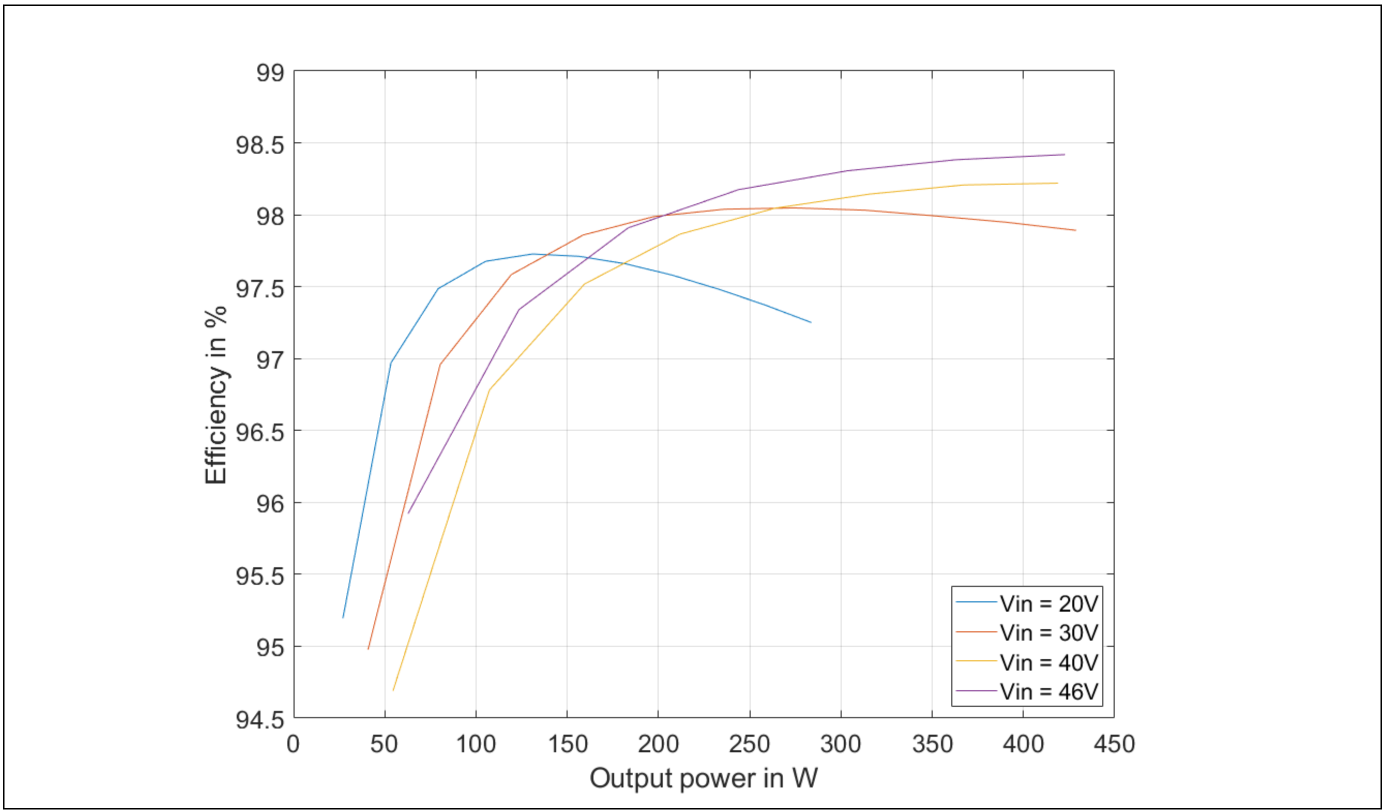


Figure 14 **Boost efficiency measurement at different input voltages at 25% duty cycle, HS buck constant on**

Comparing the results with a calculation according to [2] yields similar results. If V_{in} = 60 V and I_{out} = 8.89 A, the calculated losses are 6.49 W comparing to the 6.55 W observed in the measurement. The calculated losses are consisting of switching, conduction, shunt, inductance, and auxiliary losses. One can see that the switching losses dominate followed by auxiliary supply + current sense losses, conduction and inductance losses. In case higher efficiency is required, the auxiliaries and shunt section of the board should be revisited as the used switches are best in class. Furthermore, this would yield in high efficiency increases at low voltage levels.

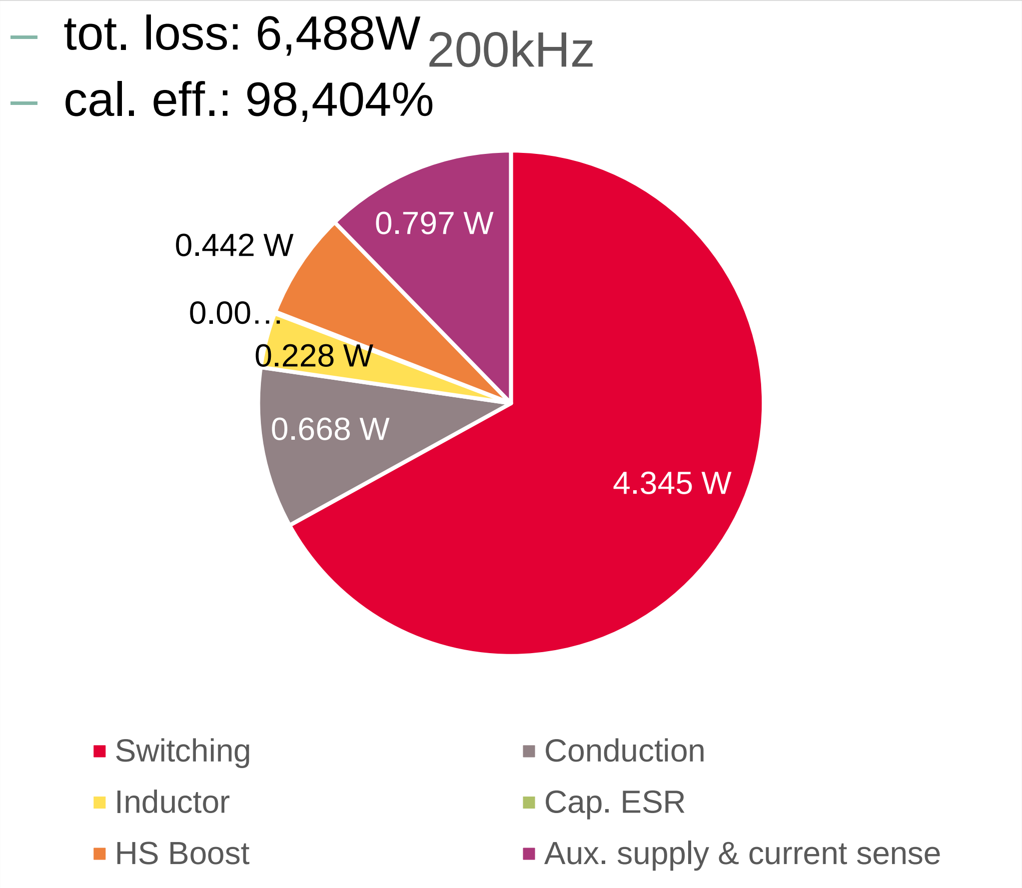


Figure 15 Calculated losses of the power stage at V_{IN} = 60 V and $I_{\_out}$ = 8.89 A with 75% duty cycle

4.2 Transient voltage measurement

In order to achieve high switching performance, the drain source voltages were measured. For the high-side VDS measurement, the PMK FireFly optically isolated probe was used. The low-side VDS measurement is done with a 1:10 passive probe head with spring. The dead-time has been set to 40 ns. In Figure 16 and Figure 17, the switching waveforms in buck mode can be seen for the case of V_{IN} = 60 V, V_{OUT} = 30 V, and P_{OUT} = 300 W. In Figure 18 and Figure 19, the switching waveforms in boost mode can be seen for the case of V_{IN} = 30 V, V_{OUT} = 60 V, and P_{OUT} = 300 W. The highest observed voltage is 67.2 V resulting out of a high and low frequent ringing. The higher frequency component originated out of the charging and discharging of the output capacitances, the low frequent part is depending on the distance to the input capacitances. As the overshoot is still well inside the limits the switching speed of here max. 11.92 V/ns could be still increased. In case a snubber is put in place, the transients could be increased even further.

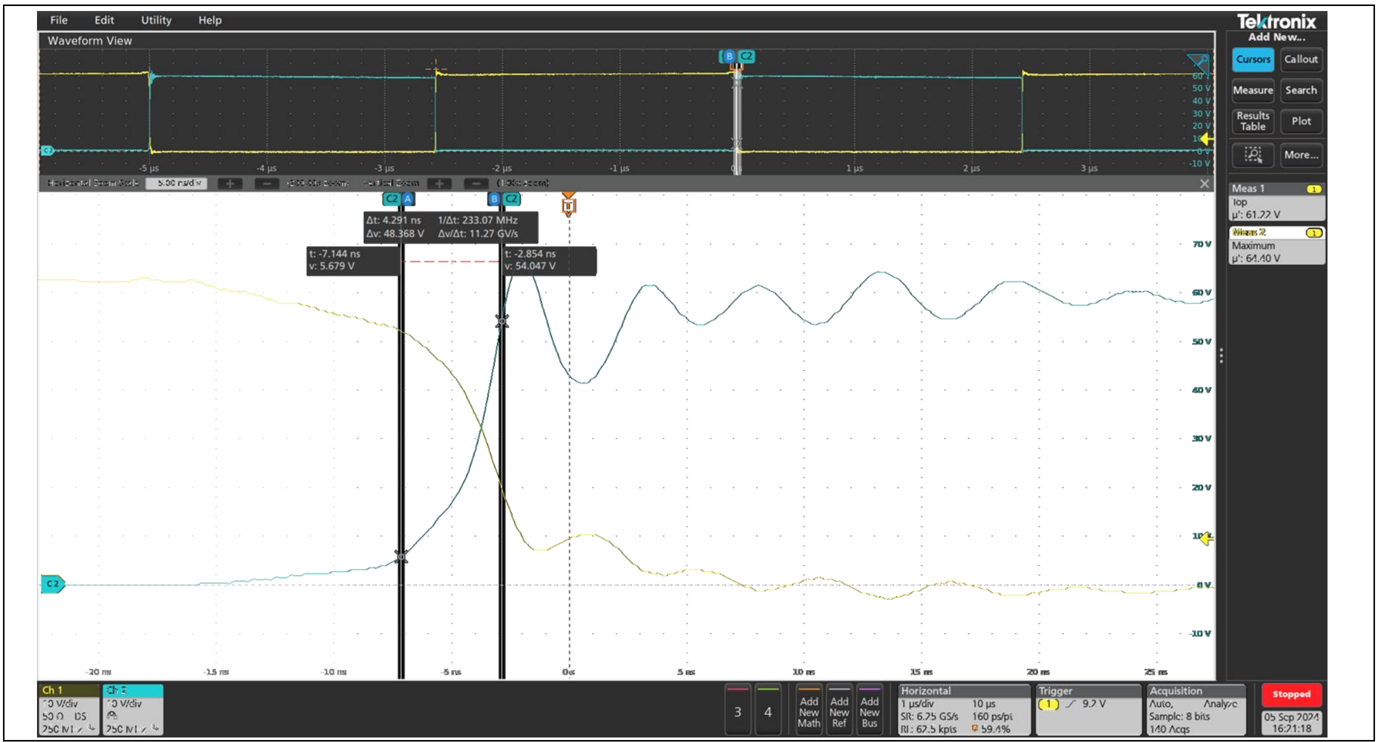


Figure 16 Buck mode: Drain source voltages at high side turn on

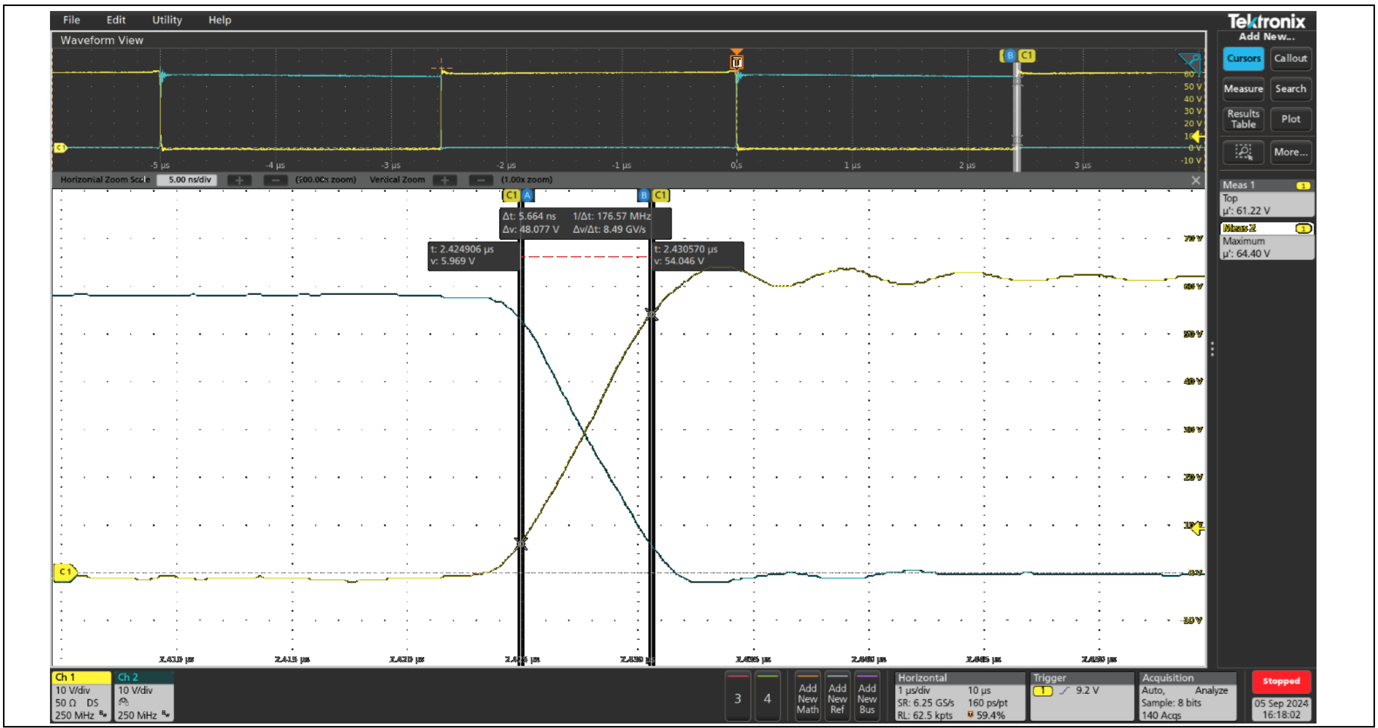


Figure 17 Buck mode: Drain source voltages at low side turn on

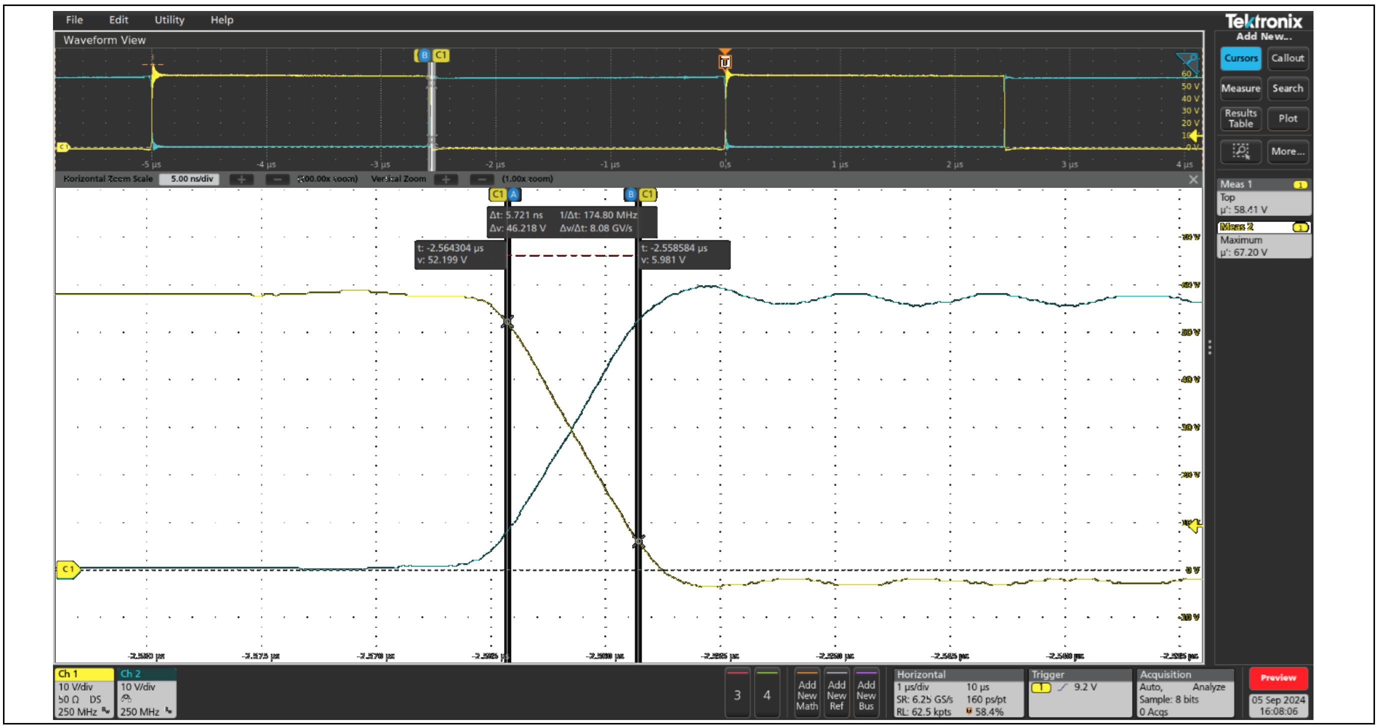


Figure 18 Boost mode: Drain source voltages at high side turn on

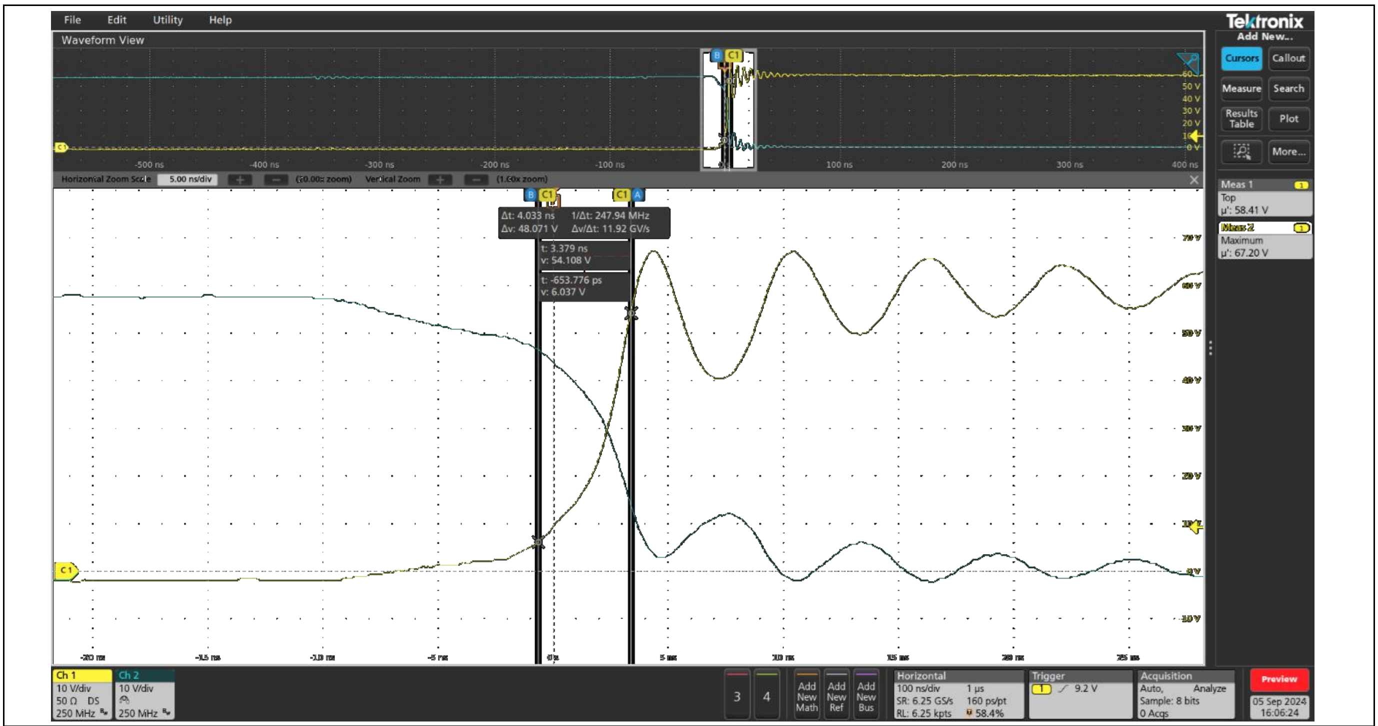


Figure 19 Boost mode: Drain source voltages at low side turn on

4.3 MPPT efficiency

In order to test the MPPT tracking efficiency, a PV module or emulator needs to be connected. Table 2 lists the equipment used for this measurement.

Table 2 Measurement device description

Device	Part Number	Description
Power supply	62150H-1000S	60V/15A 450W rating as minimum
Load	EA-ELR 9250-70	At least 450W power dissipation

Different modes can be set to see how the PV emulator changes its output characteristic over time. For these measurements, a Sandia Model was selected. The test was carried out with three different load settings – buck mode, boost mode, and buck-boost mode.

4.3.1 Buck mode

The first test was done with V_{load} = 30 V, which forces the buck-boost to run in buck mode. The input settings are displayed in Figure 20. The test shows an average MPPT efficiency of 99.61% with a peak efficiency of 99.93%. The maximum dT= 57.9°C and measured at the HS switch of the buck. The higher the output power the better is the tracking as small changes in the duty cycle result in a high change in power level resulting in a reduced influence of noise in the measurement.

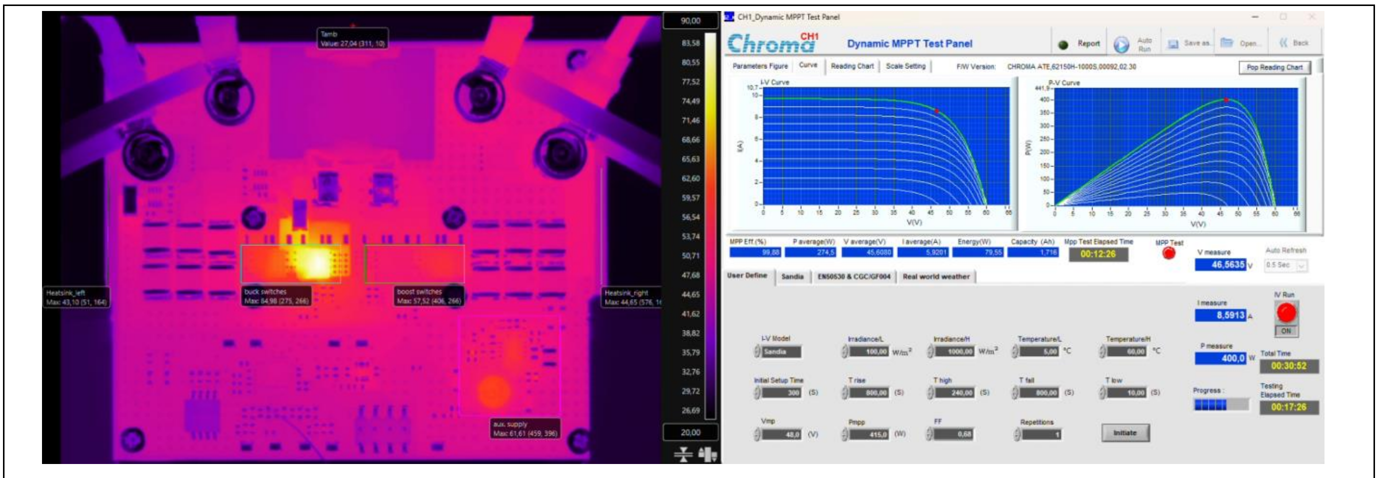


Figure 20 Buck mode: Solar emulator GUI and thermal image during MPPT testing at max. power

4.3.1 Boost mode

The second test was done with V_{load} = 60 V, which forces the buck-boost to run in boost mode. The input settings are displayed in Figure 21. The test shows an average MPPT efficiency of 99.60% with a peak efficiency of 99.90%. The maximum dT= 43.6°C and measured at the LS switch of the boost.

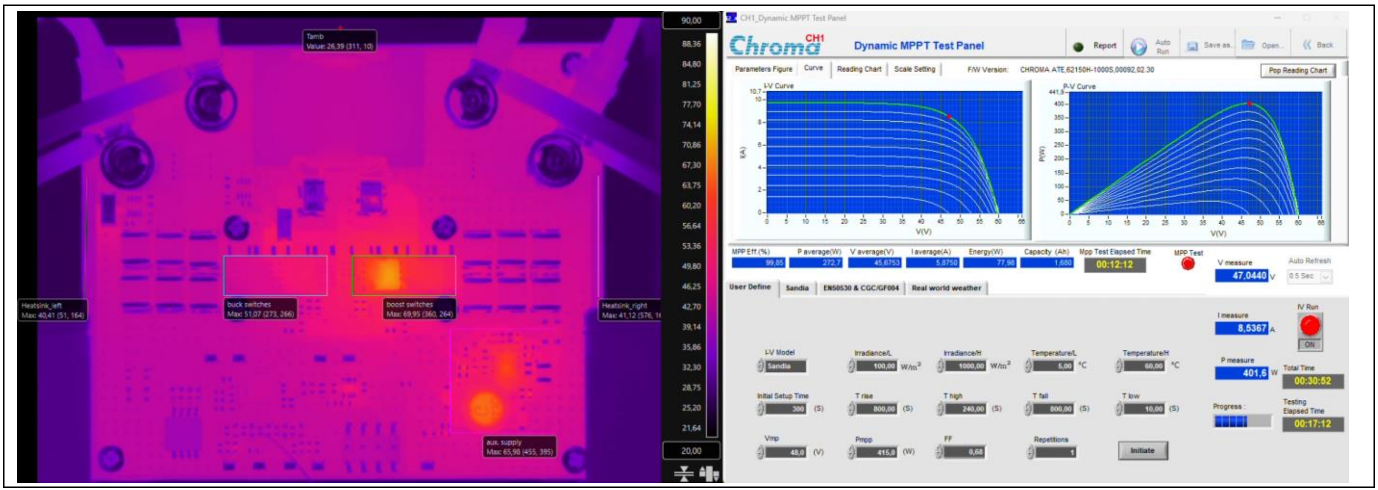


Figure 21 **Boost mode: Solar emulator GUI and thermal image during MPPT testing at max power**

4.3.1 Buck-boost mode

The third test was done with V_{load} = 48 V with same MPP, which forces the buck-boost to run most of the time in buck-boost mode (4-switch mode). The input are displayed in Figure 22. The test shows an average MPPT efficiency of 99.59% with a peak efficiency of 99.89%. The maximum dT = 57.8°C and measured at the HS switch of the buck.

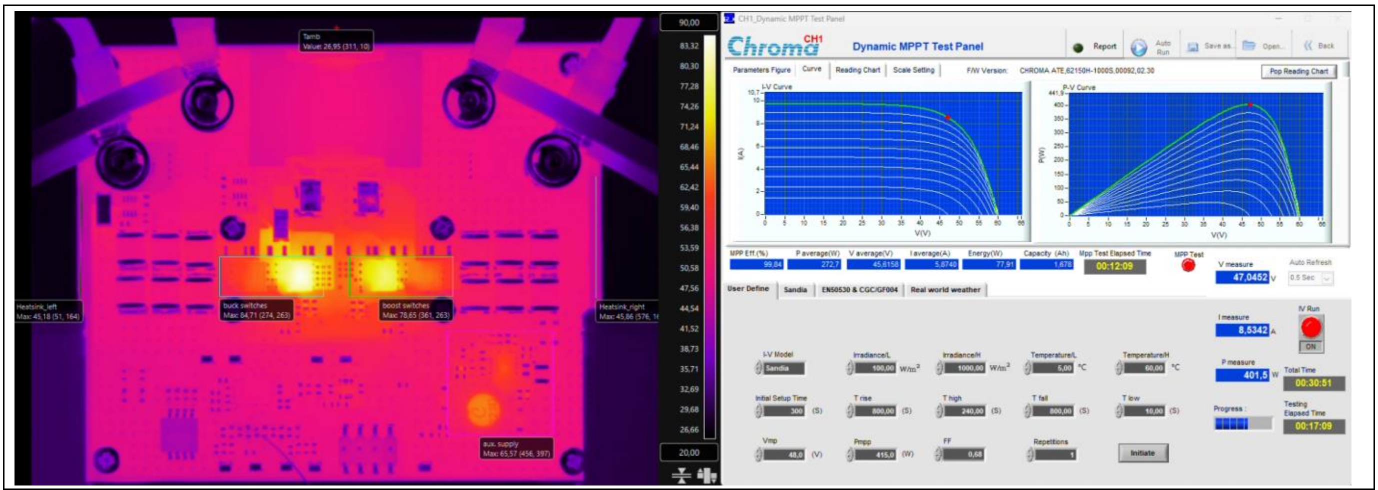


Figure 22 **Buck-boost mode: Solar emulator GUI and thermal image during MPPT testing at max. power**

5 Software

Unlike a typical buck converter, an optimizer controls the input voltage instead of just regulating the output voltage. This can be done due to the non-linear behavior of a PV cell. By increasing the duty cycle, the output current rises, which in turn increases the input current leading to a drop in the input voltage. If the input power is measured, a working point with the highest possible input power can be found.

In this optimizer, a cascaded control loop with an inner current control and output voltage control is used. The controllers itself are 2P2Z controllers. The current loop is called at a frequency of 25 kHz, whereas the voltage loop is called every 12.5 kHz. This leads to a quick response time in case the load or input power changes.

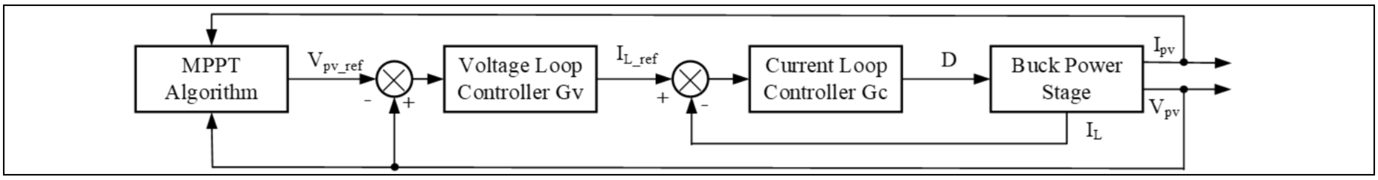


Figure 23 Control structure

The MPPT algorithm is called every second and checks if the power increases or decreases compared to the last function call. It then sets the reference voltage accordingly. In case the input power changes only marginally, the reference is kept constant as the maximum power point has already reached close enough. The stepsize of the reference voltage is set to ~0.3 V so that the algorithm can track the target voltage in case of shadowing yet reach the maximum power point accurately. The firmware itself can be adapted to fit the other voltage and current ranges. If the input voltage is too low, the power stage will remain inactive as the high side gate drive supply needs to have a minimum of 7.5 V plus some margin to function properly. Furthermore, the software will not start switching until a minimum of 15 V is reached.

Although the board is pre-flashed and ready to be used. However, if changes to the software are required, follow the instructions in Section 5.1.

5.1 Software deployment and debugging

Prerequisites:

- Download and install DAVE™ IDE from Infineon Developer Center.
- Register the board with the attached serial number on the Infineon website. Download the firmware that is already pre-flashed on the board.

Programming and debugging are carried out via the XMC™ Link isolated debug probe as shown in Figure 24.

Figure 24 XMC™ Link isolated debugger probe

5.1.1 Open the firmware project in DAVE™

Perform the following steps to set up and debug the firmware.

1. Connect the optimizer board to the debug probe using the larger 2.54 mm pitch ribbon cable and the 8-pin box header (X2)

   An additional external power supply is required when using an isolated debugging probe.
2. Import the downloaded firmware project in DAVE™ by navigating to **File** > **Import** > **Infineon** > **DAVE Project**

   This firmware project was created within DAVE™ IDE containing the device definition, settings, and source files required to compile and build the executable code, which can be downloaded into the Flash program memory of the XMC™ XMC1000 MCU.

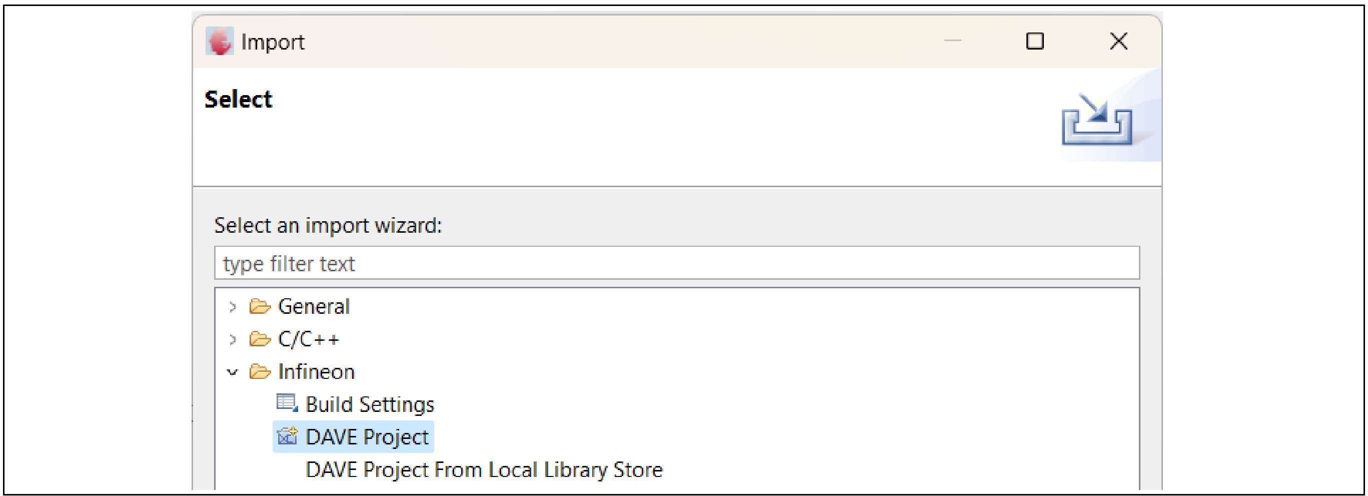


Figure 25 **DAVE™ IDE import window**

3. Open the **C/C++ Projects** tab

   The *main.c* file contains the main body of the source code, *mppt_pno.h* contains the main struct describing the MPPT algorithm, and the *xmc_2p2z_filter_fixed.h* contains all the necessary function calls for the current and voltage loops.

   The apps are listed in the app dependency tree window in the DAVE™ CE screen and displayed graphically in the app dependency window.
4. To configure the app, double-click on any app

   A menu appears with options for configuration.

   The manual pin allocator is used to select which I/O pins are mapped to each of the app inputs and outputs.
5. Once the configuration is complete, generate the corresponding *.c* and *.h* source code files by clicking the **Generate Code** button located on command bar as shown below

Note: *For a more complex functionality, download the necessary functions from the DAVE™ library.*

5.1.2 Setting the BMI in DAVE™

In case the board is used for the first time, the BMI (Boot Mode Index) needs to be set. The BMI value determines the start-up mode and debug configuration of the XMC1000. Bootstrap modes via UART or SPI as well as single pin debug or SWD are supported.

To set the BMI, perform the following steps.

1. Click **BMI Get Set** as shown in Figure 26

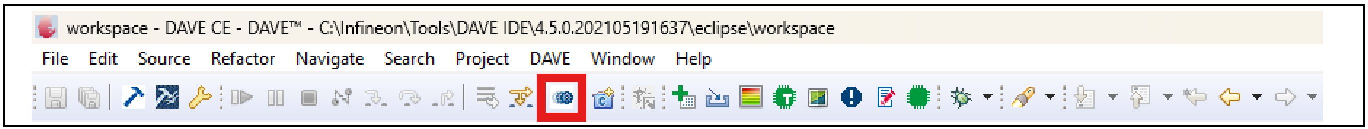


Figure 26 **DAVE™ IDE with BMI Set and Get button highlighted in red**

2. Press the **Get BMI** button to acquire the current set BMI value on the MCU
3. Click **Select** under the **BMI Selection** tab
   By default, the BMI value is **Detected BMI Value** is **ASC Bootstrap Load Mode (ASC_BSL), no debug**. However, the board cannot be debugged in this mode.
4. Change the BMI to **User Mode (Debug) SWD0 (SWDIO_P0.14, SWDCLK=P0.15)** and press the **Set BMI** button as shown in Figure 27

Note: In a different design, it is possible that instead of the SWD0 interface, the SWD1 interface is used, which is located at different pins. Hence, always consult the schematic before setting the BMI value.

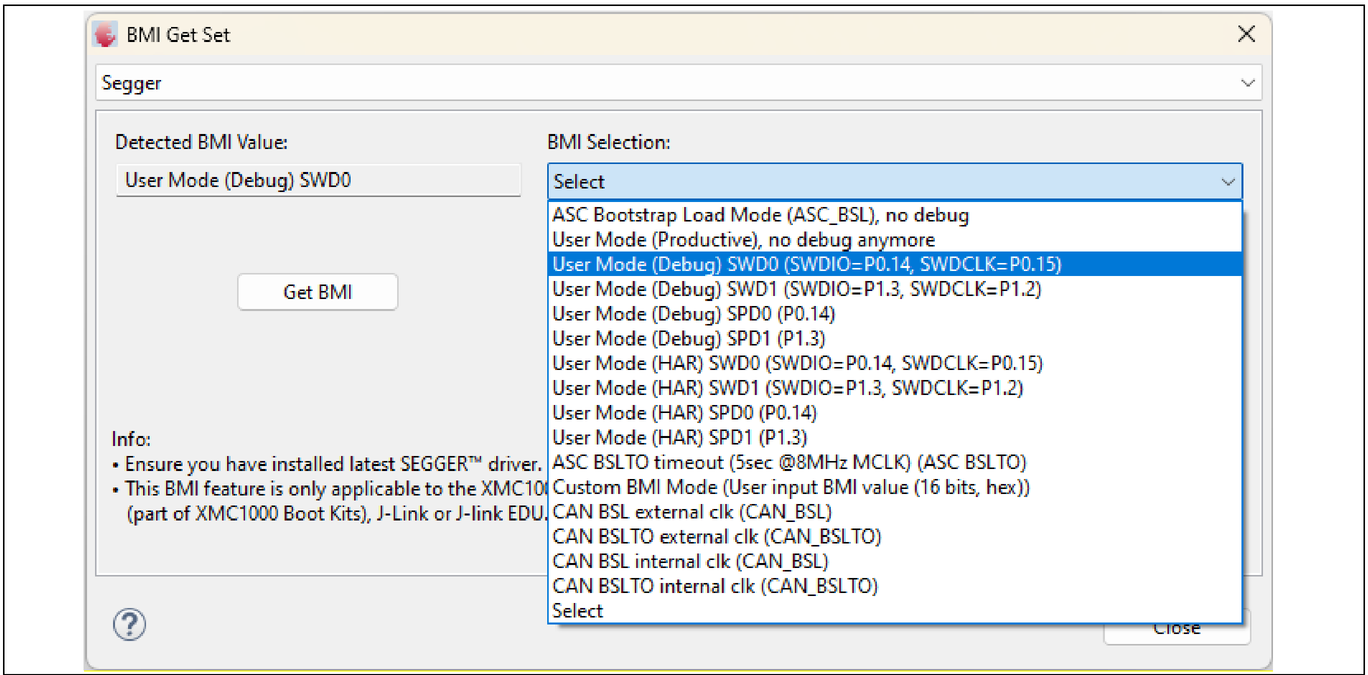


Figure 27 **BMI Set and Get window**

5. To apply the imported project to the board and build the project, click **Build Active Project**
6. Click **Debug** to program the board

   The debug screen appears, where the program can be launched. If the board is tested without any modifications, the firmware just needs to be built and flashed.

7. To flash the firmware, the microcontroller needs to be supplied with power as the debugger itself is isolated. Therefore, connect Pin 5 and 6 of the debug connector (P1) with an external supply of 3.3 V, while the remaining pins are connected to the isolated debugger probe
   Led D1 lights up.

Note: When flashed and before running the board with the power at the input terminals, ensure that the external supply is disconnected.

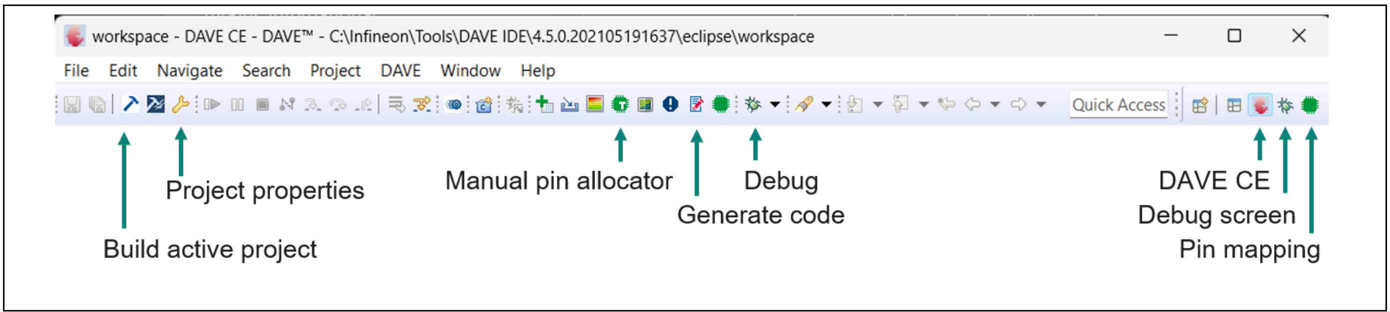


Figure 28 DAVE™ IDE main commands

5.2 Firmware settings

There are several parameters which can be changed in the firmware depending on the used PV module or the populated switches. One part which can be changed depending on the requirements on the control are the A and B parameters of voltage and current loop.

Code listing 1 2P2Z parameters

```
/*V loop parameter*/
#define V_B0 (+2.013)
#define V_B1 (-2.0070)
#define V_B2 (+0.00)
#define V_A1 (+1.0)
#define V_A2 (-0.0)
#define V_K  (+0.5)

...

/*I loop parameter*/
#define I_B0 (+0.3680)
#define I_B1 (-0.3520)
#define I_B2 (+0.0)
#define I_A1 (+1.0)
#define I_A2 (-0.0)
#define I_K  (+0.01)
```

The controller itself is simplified to a PI compensator, by defining the parameters as below:

- B2 = 0
- B1 = (Ki – KP)/K
- B0 = (Ki + KP)/K
- A2 = 0
- A1 = 1

K is the gain, so, in Z domain, the KP and Ki is,

- KP = 1/2×(B0-B1)×K
- Ki = 1/2×(B0+B1)×K

The control parameters are tuned for high stability over the whole operating range and quick responsiveness.

Depending on the used switches and gate driver as well as the corresponding gate and snubber settings, the dead-time needs to be adjusted. By default, the dead-time is set to 40 ns.

Depending on the used PV module and its characteristics, the MPPT controller settings can be fine-tuned to achieve the highest performance. The parameters in Code listing 2 can be changed:

- **DeltaPmin**: Minimum change in measured power in mW needed for change in operating point (50 equals 1.59 V)
- **MaxVolt**: Maximum reference voltage for voltage loop (3015 equals 60 V)
- **MinVolt**: Minimum voltage required at input for switches to start operation (754 equals 15 V)
- **Stepsize**: Change in reference voltage value for voltage control loop (15 equals 0.3 V)

All other parameters in the struct are status variables changing during runtime of the program.

Code listing 2 MPPT parameter settings

```
typedef struct {
      int32_t  Ipv;
      int32_t  Vpv;
      int32_t  DeltaPmin;
      int32_t  MaxVolt;
      int32_t  MinVolt;
      int32_t  Stepsize;
      int32_t  VmppOut;
      int32_t  DeltaP;
      uint32_t  PanelPower;
      uint32_t  PanelPower_Prev;
      uint16_t mppt_enable;
      uint16_t mppt_first;
}mppt_pno;

typedef mppt_pno *mppt_pno_handle;

#define mppt_pno_DEFAULTS {
      0,     \
      0,     \
      20,    \
      3015,  \
      754,   \
      15,    \
      0,     \
      0,     \
      0,     \
      0,     \
      0,     \
      1,     \

}
```

6 Startup

The board is delivered with heatsink, thermal interface material (graphite sheet) and screws. Heatsink is not mounted, to allow measurements close to the MOSFETs. However, the board can be used even without the heatsink if temperatures are externally monitored and the full power of 400 W is not needed.

The board comes pre-flashed so it can be operated as is. In case, a non-factory new board is obtained, follow all steps outlined in chapter 5.1.

The optimizer controls the input voltage and not the output voltage hence, when testing the board, if a PV panel or PV emulator is not used as source, a different test setup must be arranged.

A regular power supply can be used if a resistor is placed in series to the positive input terminal of the optimizer board. In this case, the maximum power point would correspond to half the input voltage. The resistor will generate heat according to half the output power. Hence, it has to be large enough to withstand the burnt energy. As reference, the PV emulator used for testing was the 62150H-1000S manufactured by Chroma and the used electronic load was the EA-EL 9080-170 B HP from Elektro-Automatik.

If further tests are conducted in terms of changing the switching frequency, the gate voltages need to be observed and changed accordingly, either by adjustment of the dead-time in the software, exchanging the gate resistances, or by making use of the possibility to place a snubber network. Depending on the target frequency and target power in a custom design, select the most efficient MOSFET and driver combination.

Note: For the assistance involving the selection of a suitable MOSFET and driver combination, reach out to Infineon Support.

7 REF_4SBB_OPTIMIZER schematics

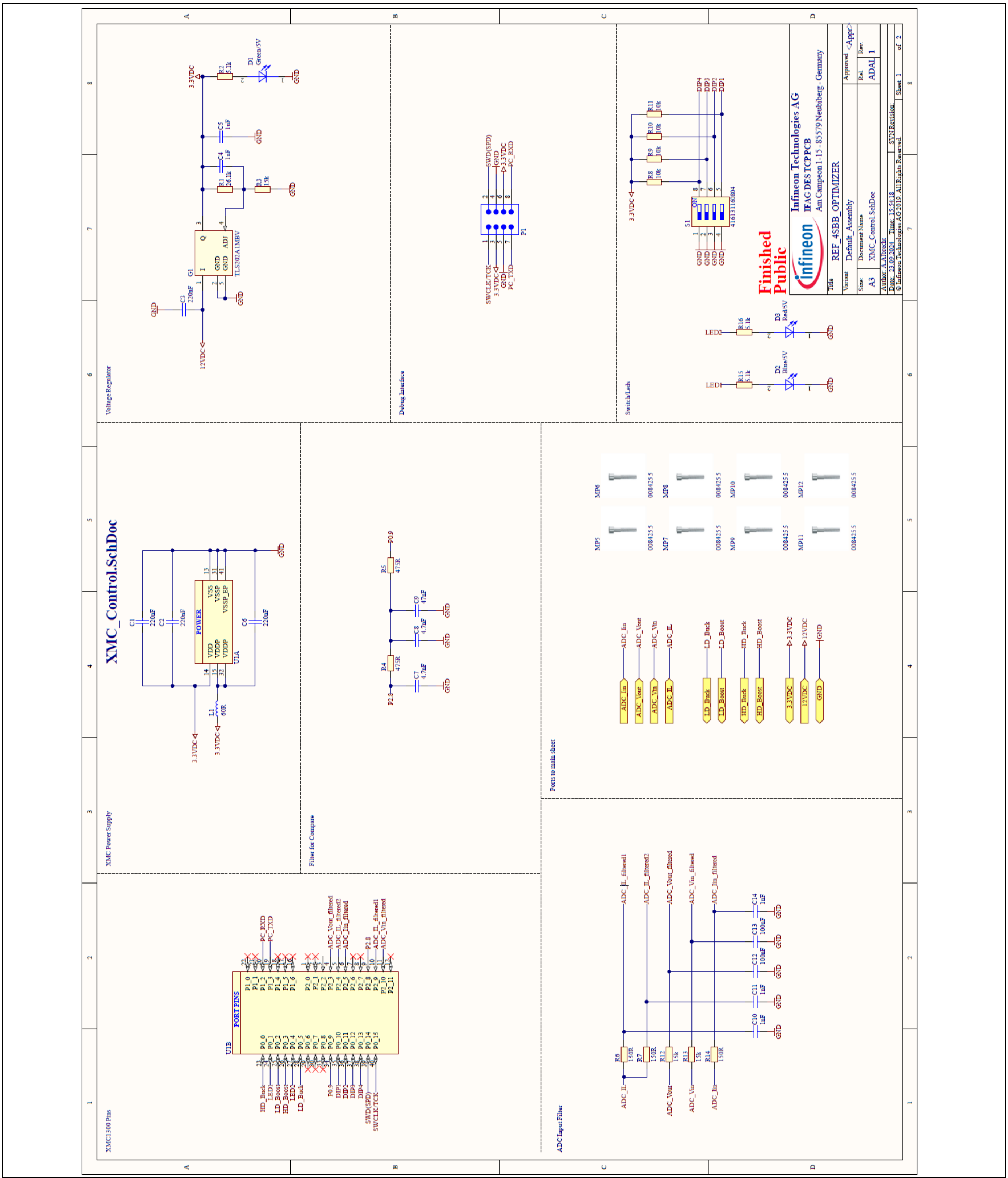


Figure 29 REF_4SBB_OPTIMIZER schematics page 1

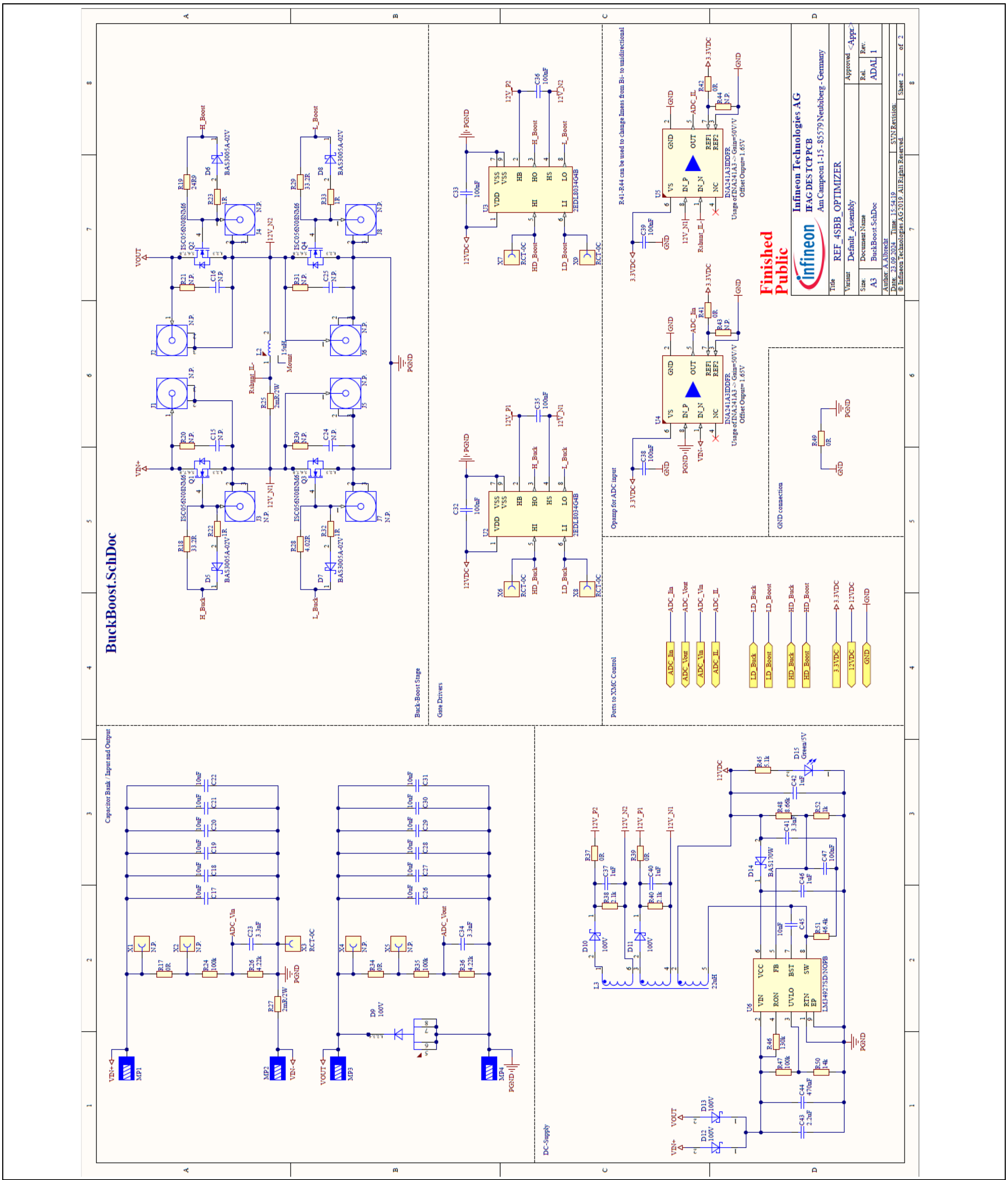


Figure 30 REF_4SBB_OPTIMIZER schematics page 2

8 PCB layout

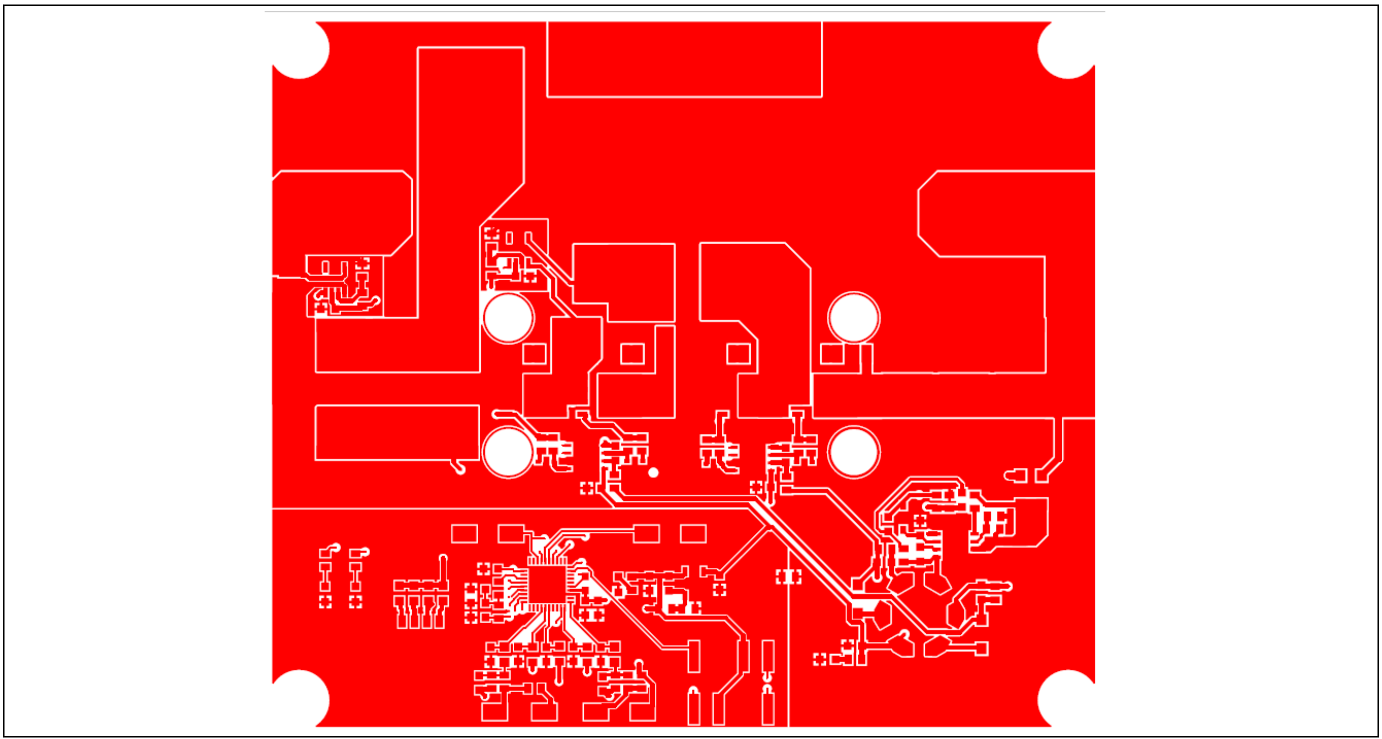


Figure 31 Top layer of the board

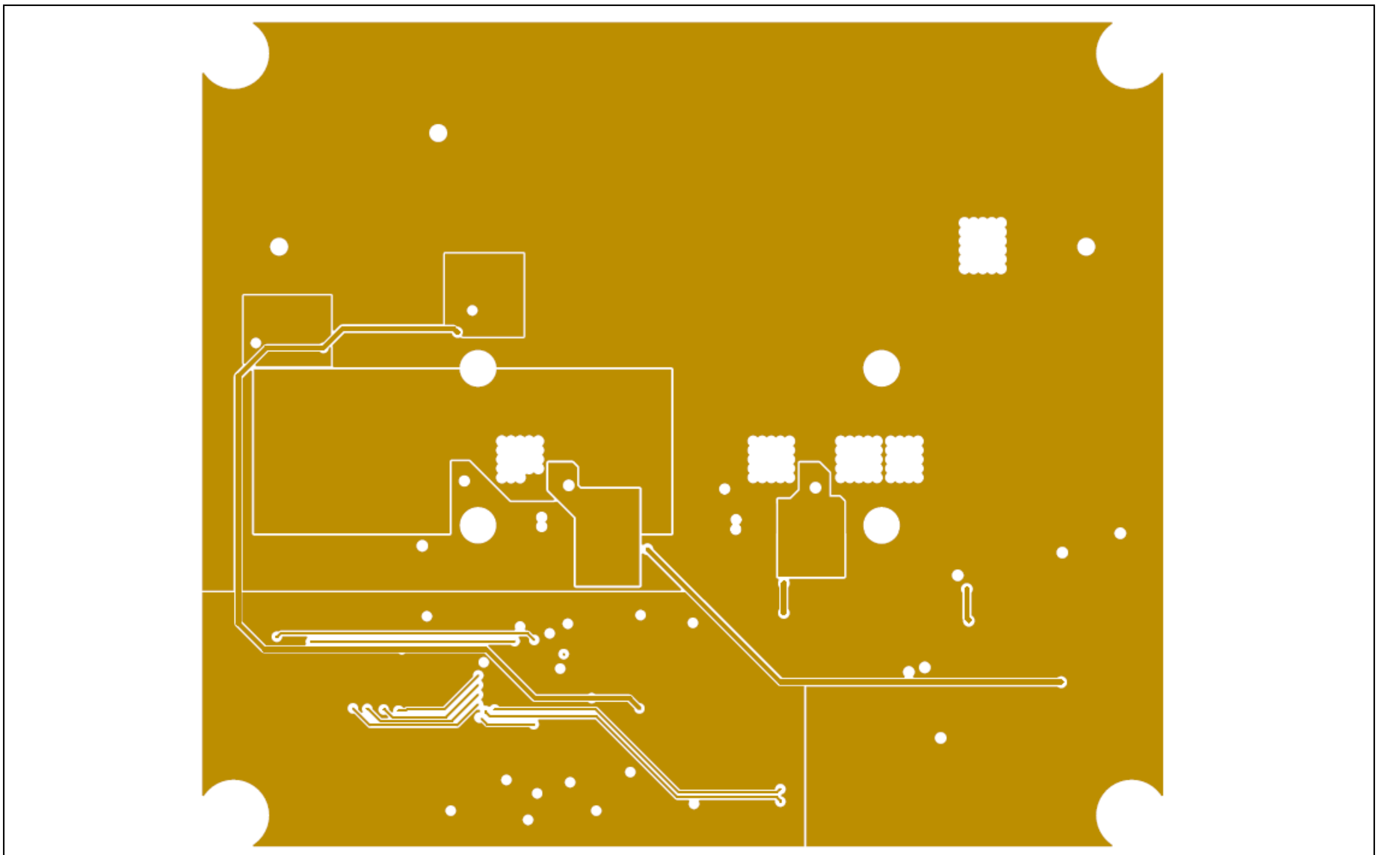


Figure 32 First inner layer

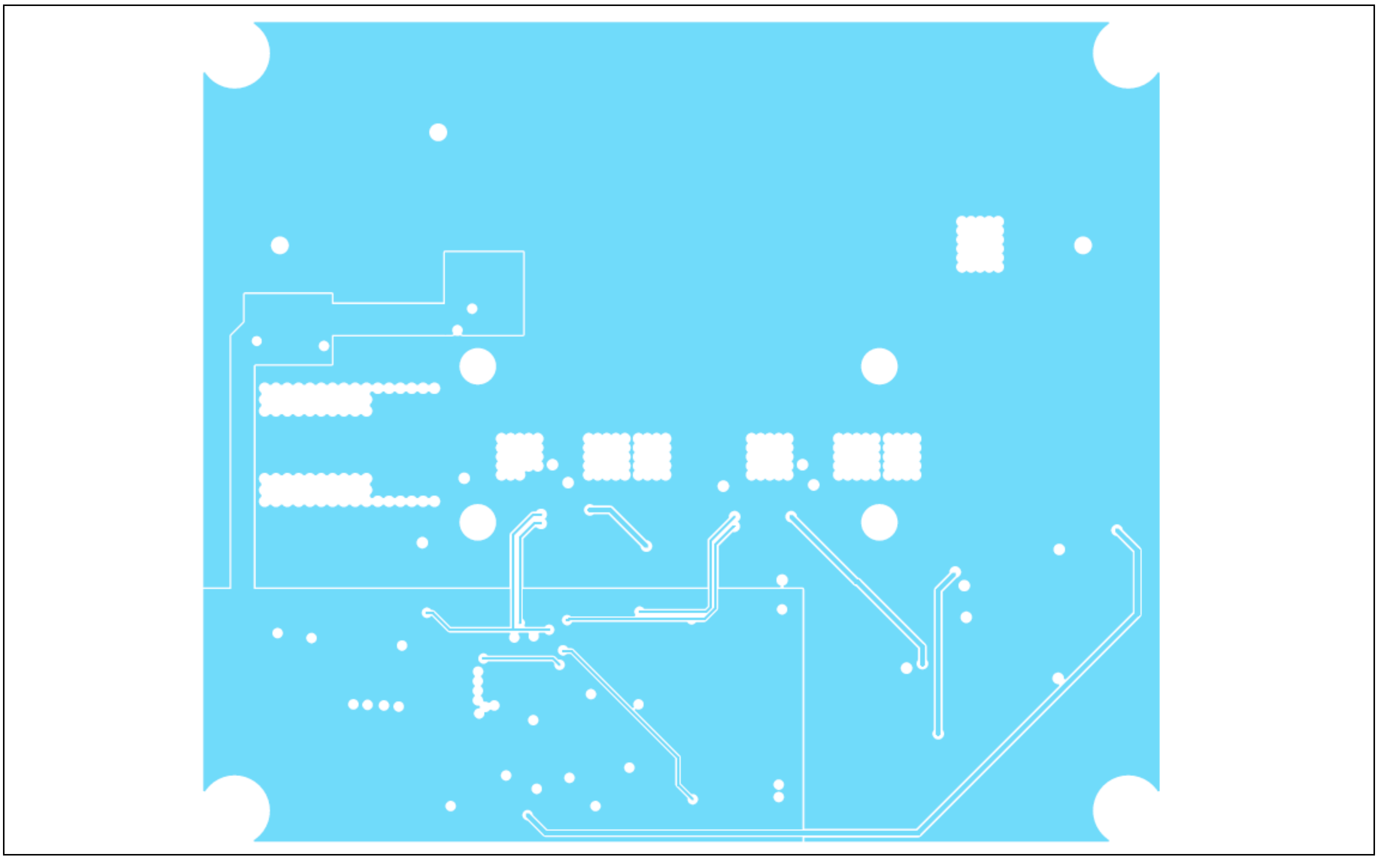


Figure 33 Second inner layer

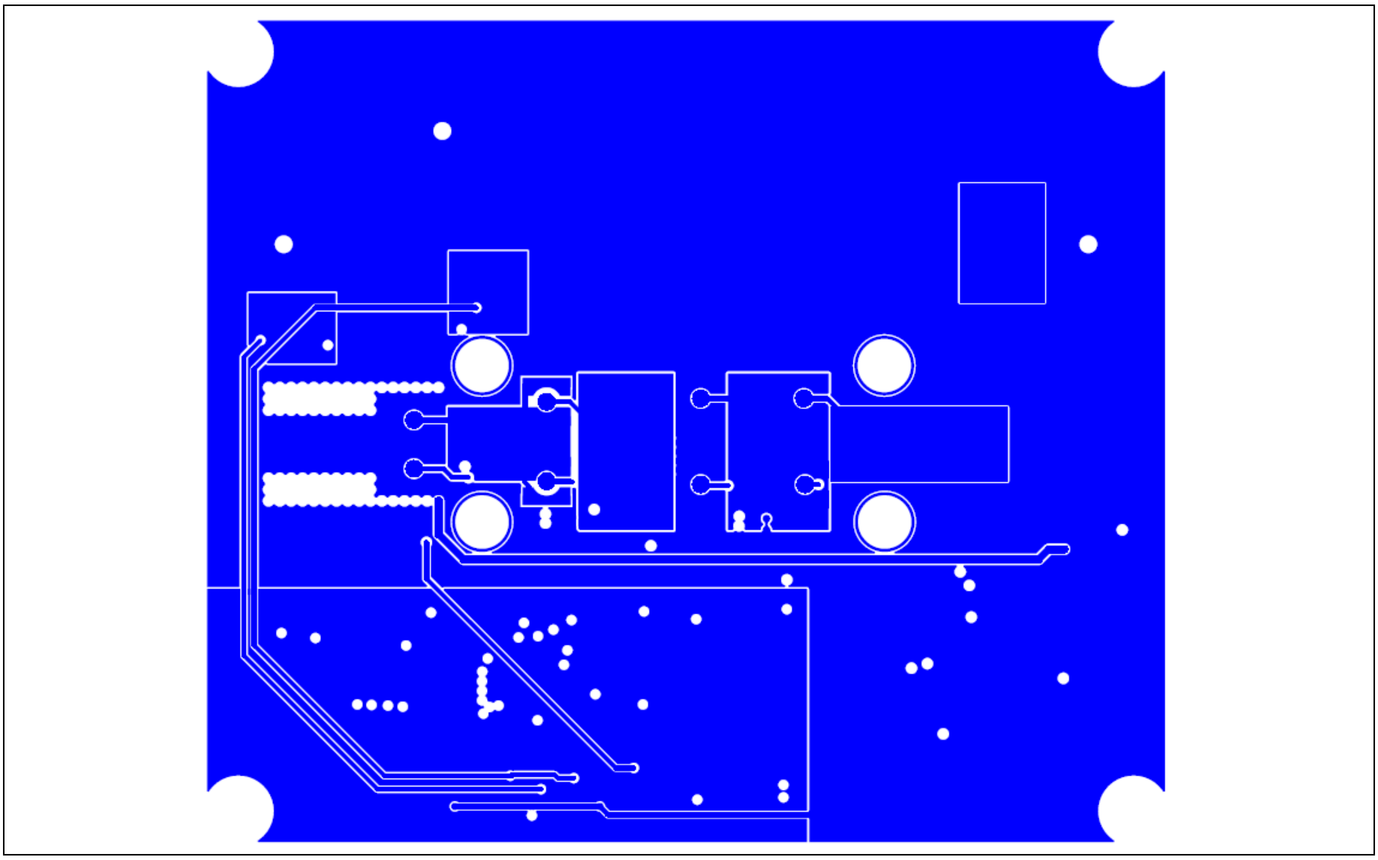


Figure 34 Bottom layer

9 Bill of materials

Table 3 Bill of materials

#	Quantity	Designator	Value	Description	Manufacturer	Manufacturer Order Number
1	7	R17, R34, R37, R39, R41, R42, R49	0R	RES / STD / 0R / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603 (1608) / SMD / -	Vishay	CRCW06030000Z0EB
2	1	R52	1k	RES / STD / 1k / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW06031K00FK
3	4	C4, C10, C11, C14	1 nF	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, NP0, 1nF, 25VDC	Würth Elektronik	885012006044
4	4	R22, R23, R32, R33	1R	RES / STD / 1R / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW06031R00FK
5	5	C5, C37, C40, C42, C46	1 µF	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R, 1 µF, 25VDC	Würth Elektronik	885012206076
6	2	U2, U3	2EDL8034G4B	EiceDRIVER™, 120 V Boot, 3 A / 4 A, Junction-Isolated High Side and Low Side Gate Driver IC	Infineon Technologies	2EDL8034G4B
7	2	R25, R27	2mR/2 W	RES / STD / 2mR/2W / 2 W / 1% / 50ppm/K / -65°C to 170°C / 2010(5025) / SMD / -	KOA Speer Electronics Inc.	TLR2HWDTE2L00F50
8	2	R38, R40	2.1k	RES / STD / 2.1k / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW06032K10FK
9	1	C43	2.2 uF	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 1210, X7R, 2.2 µF, 100VDC	Würth Elektronik	885012209071

#	Quantity	Designator	Value	Description	Manufacturer	Manufacturer Order Number
10	3	C23, C34, C41	3.3 nF	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R, 3.3 nF, 25VDC, WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R, 3.3 nF, 100VDC	Würth Elektronik	885012206062
11	1	R28	4.02R	RES / STD / 4.02R / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW06034R02FK
12	2	R26, R36	4.22k	RES / STD / 4.22k / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW06034K22FK
13	2	C7, C8		WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R, 4.7 nF, 25VDC	Würth Elektronik	885012206063
14	4	R2, R15, R16, R45	5.1k	RES / STD / 5.1k / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW06035K10FK
15	1	R48	8.66k	RES / STD / 8.66k / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW06038K66FK
16	4	R8, R9, R10, R11	10k	RES / - / 10k / 100mW / 1% / 100ppm/K / - / 0603(1608) / SMD / -	ROHM Semiconductors	MCR03EZPFX1002
17	1	C45	10 nF	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R, 10nF, 25VDC	Würth Elektronik	885012206065
18	12	C17, C18, C19, C20, C21, C22, C26, C27, C28, C29, C30, C31	10 uF	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 2220, X7R Class II, 10µF, 100VDC	Würth Elektronik	885012214006

#	Quantity	Designator	Value	Description	Manufacturer	Manufacturer Order Number
19	1	R50	14k	RES / STD / 14k / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW060314K0FK
20	1	R3	15k	RES / STD / 15k / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW060315K0FK
21	2	R12, R13	15k	RES / STD / 15k / 100 mW / 0.1% / 25ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Panasonic	ERA-3AEB153V
22	1	L2	15 uH	IND / STD / 15uH / 30A / 15% / -40°C to 125°C / 2.4mR / SMD / Inductor; SMD, 3pin, 19.40 mm L X 28.00 mm W X 18.50 mm H / SMD / -	Würth Elektronik	7443641500
23	1	L3	22 uH	IND / STD / 22uH / - / 20% / -40°C to 85°C / 400mR / SMD / Inductor, SMD, 6 pin, 8.05 mm L X 8.90 mm W X 4.70 mm H body / SMD / -	Coilcraft	LPH8045-223MRC
24	1	R19	24R9	RES / STD / 4.02R / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW06034R02FK
25	1	R1	26.1k	RES / STD / 26.1k / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW060326K1FKEA
26	2	R18, R29	33.2R	RES / STD / 4.02R / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW06034R02FK
27	1	R51	46.4k	RES / STD / 46.4k / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW060346K4FK

#	Quantity	Designator	Value	Description	Manufacturer	Manufacturer Order Number
28	1	C9		WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R, 47 nF, 25VDC	Würth Elektronik	
29	1	L1	60R	IND / FERR / 60R / 500A / 25% / -55°C to 125°C / 300mR / 0603(1608) / Inductor,Chip;1.60 mm L X 0.80 mm W X 1.00 mm H / SMD / -	Würth Elektronik	74279267
30	3	R24, R35, R47	100k	RES / STD / 100k / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW0603100KFK
31	9	C12, C13, C32, C33, C35, C36, C38, C39, C47	100 nF	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, NP0, 1 nF, 25VDC, WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R, 100 nF, 25VDC	Würth Elektronik	885012206069
32	1	D9	100 V	Power Schottky Rectifier Optimized for Switch Mode Power Supply	STMicroelectronics	STPS30M100DJF-TR
33	4	D10, D11, D12, D13	100 V	Schottky Trench Rectifier	STMicroelectronics	STPST1H100ZFY
34	1	R46	130k	RES / STD / 130k / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW0603130KFK
35	3	R6, R7, R14	150R	RES / STD / 150R / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Yageo	RC0603FR-07150RL
36	4	C1, C2, C3, C6	220 nF	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General Purpose, size 0603, X7R, 220 nF, 25VDC	Würth Elektronik	885012206073
37	1	C44	470 nF	WCAP-CSGP Multilayer Ceramic Chip Capacitor, General	Würth Elektronik	885012207130

#	Quantity	Designator	Value	Description	Manufacturer	Manufacturer Order Number
				Purpose, size 0805, X7R Class II, 470 nF, 100VDC		
38	2	R4, R5	475R	RES / STD / 475R / 100 mW / 1% / 100ppm/K / -55°C to 155°C / 0603(1608) / SMD / -	Vishay	CRCW0603475RFK
39	8	MP5, MP6, MP7, MP8, MP9, MP10, MP11, MP12	008425 5	Cheese Head Screw With Hexagon Socket, DIN 912 (ISO 4762), M2.5, 5mm length	Würth Elektronik	008425 5
40	1	P1		WR-PHD Pin Header, SMT, Vertical, pitch 2.54 mm, 2 Row, 8P	Würth Elektronik	61000821121
41	1	S1	416131160804	WS-DISV Small Compact SMT Dip Switch, 4Poles, 1.27 mm Pitch, 24V, 25 mA	Würth Elektronik	416131160804
42	8	J1, J2, J3, J4, J5, J6, J7, J8	N.P.	WR-MMCX PCB Jack, SMT, Straight, 6 GHz, 50Ω	Würth Elektronik	66012102111404
43	1	D14	BAS170W	Silicon Schottky Diode, General Purpose Diode for High Speed Switching	Infineon Technologies	BAS170W
44	4	D5, D6, D7, D8	BAS3005A-02 V	Low VF Schottky Diode	Infineon Technologies	BAS3005A-02V
45	1	D2	Blue/5 V	WL-SMCW SMT Mono-color Chip LED Waterclear, Blue, 465 nm	Würth Elektronik	150060BS75000
46	2	D1, D15	Green/5 V	WL-SMCW SMT Mono-color Chip LED Waterclear, Green, 515 nm	Würth Elektronik	150060GS75000
47	2	U4, U5	INA241A3IDDFR	Bidirectional, Ultra-Precise Current Sense Amplifier	Texas Instruments	INA241A3IDDFR
48	4	Q1, Q2, Q3, Q4	ISC056N08NM6	OptiMOS™ 6 Power Transistor with the Feature of Very Low On-Resistance	Infineon Technologies	ISC031N08NM6
49	1	U6	LM34927SD/NOPB	Integrated Secondary-Side Bias Regulator for Isolated DC-DC Converters (Integrated	Texas Instruments	LM34927SD/NOPB

#	Quantity	Designator	Value	Description	Manufacturer	Manufacturer Order Number
				600 mA High-Side and and Low-Side Switches)		
50	4	MP1, MP2, MP3, MP4		WP-SMBU SMT Internal blind-hole thread with pins, OD 7 mm, M4 x 4 mm, 50A	Würth Elektronik	7466104
51	2	R43, R44	N.P.	RES / STD / 0R / 100mW / 1% / 100ppm/K / -55°C to 155°C / 0603 (1608) / SMD / -	Vishay	CRCW06030000Z0EB
52	4	X1, X2, X4, X5	N.P.	SMD Circuit Probe Pad	TE Connectivity	RCT-0C
53	4	C15, C16, C24, C25	N.P.	CAP / CERA / 3.3nF / 630V / 10% / X7R (EIA) / -55°C to 125°C / 1206(3216) / SMD / -	MuRata	GRM31AR72J332KW01
54	4	R20, R21, R30, R31	N.P.	RES / STD / 2.05R / 250 mW / 1% / 100ppm/K / -55°C to 155°C / 1206(3216) / SMD / -	Vishay	CRCW12062R05FK
55	5	X3, X6, X7, X8, X9	RCT-0C	SMD Circuit Probe Pad	TE Connectivity	RCT-0C
56	1	D3	Red/5 V	WL-SMCW SMT Mono-color Chip LED Waterclear, Red,630nm	Würth Elektronik	150060RS75000
57	1	G1	TLS202A1MBV	Adjustable Linear Voltage Post Regulator, Adjustable Output Voltage from 1.2 V to 5.25 V	Infineon Technologies	TLS202A1MBV
58	1	U1	IFX_XMC1302-Q040X0200 AB	XMC™ XMC1000 family of microcontrollers based on the ARM® Cortex®-M0 processor core	Infineon Technologies	XMC1302-Q040X0200 AB

10 Assembly drawing

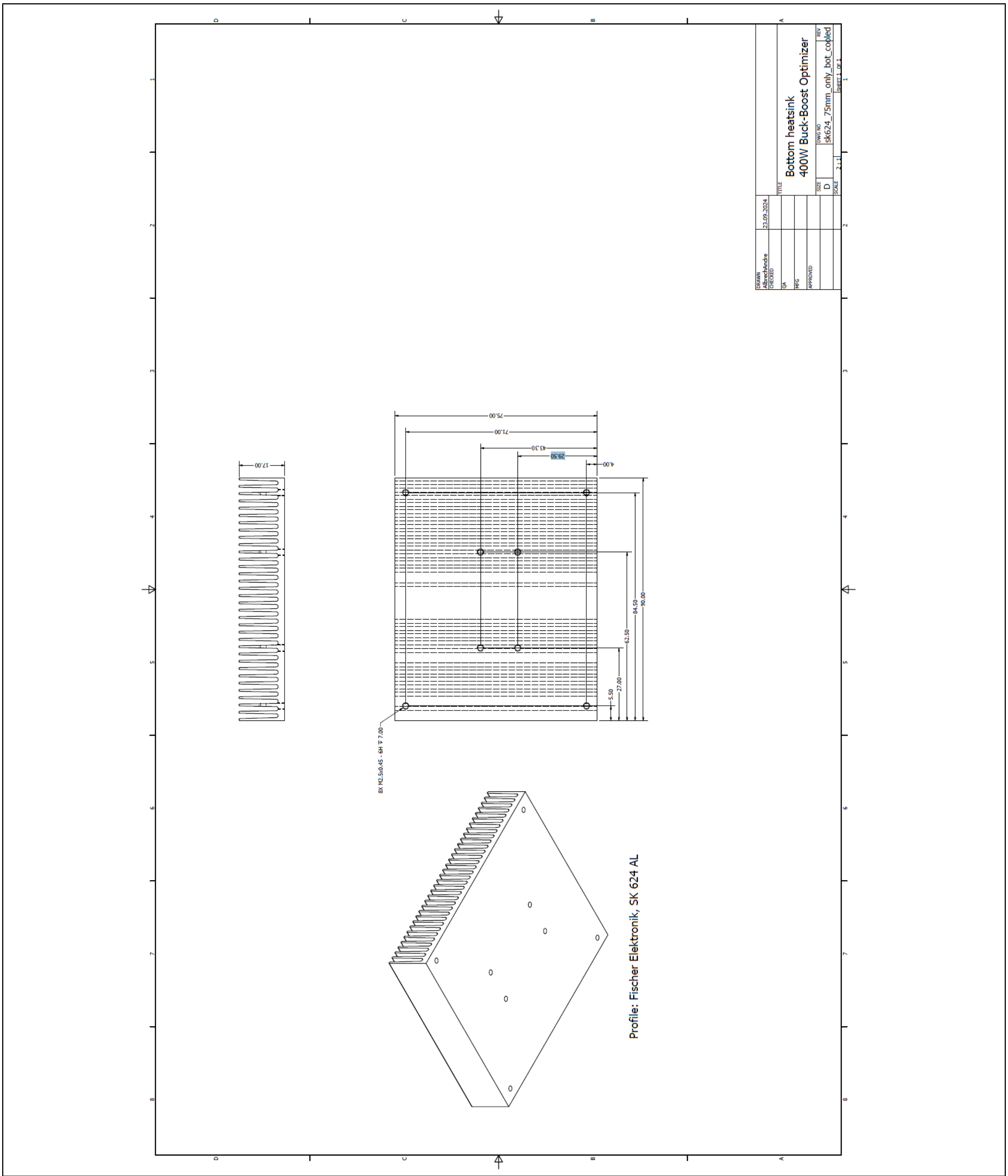


Figure 35 **Drawing of top heatsink**

References

[1] Damijan Zupancic: *Power optimizers for residential solar with MPPT tracking, Power Systems Design, 2024 Aug*; Available online

[2] Jauregui D, Wang B, Chen R.: *Power loss calculation with common source inductance consideration for synchronous buck converters. Application Report (SLPA009A), Texas Instruments. 2011 Jun*; Available online

Revision history

Document revision	Date	Description of changes
V 1.0	2024-12-20	Initial release
V 2.0	2025-07-15	Updated figures in Section 4.2.

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